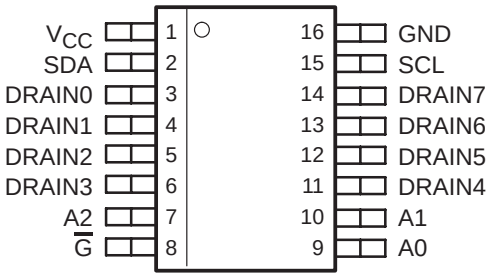
- **Low $r_{DS(on)}$ . . . 5 Ω Typical**
- **Eight Power DMOS Transistor Outputs of 100-mA Continuous Current**
- **210-mA Current Limit Capability**
- **Drain Output ESD Protection . . . 3000 V**
- **Output Clamp Voltage . . . 40 V**

D PACKAGE
(TOP VIEW)



description

The TPIC2810 device is a monolithic, medium-voltage, low-current, 8-bit shift register design to drive low-side switched resistive loads such as LEDs. The device is not recommended for switching inductive loads.

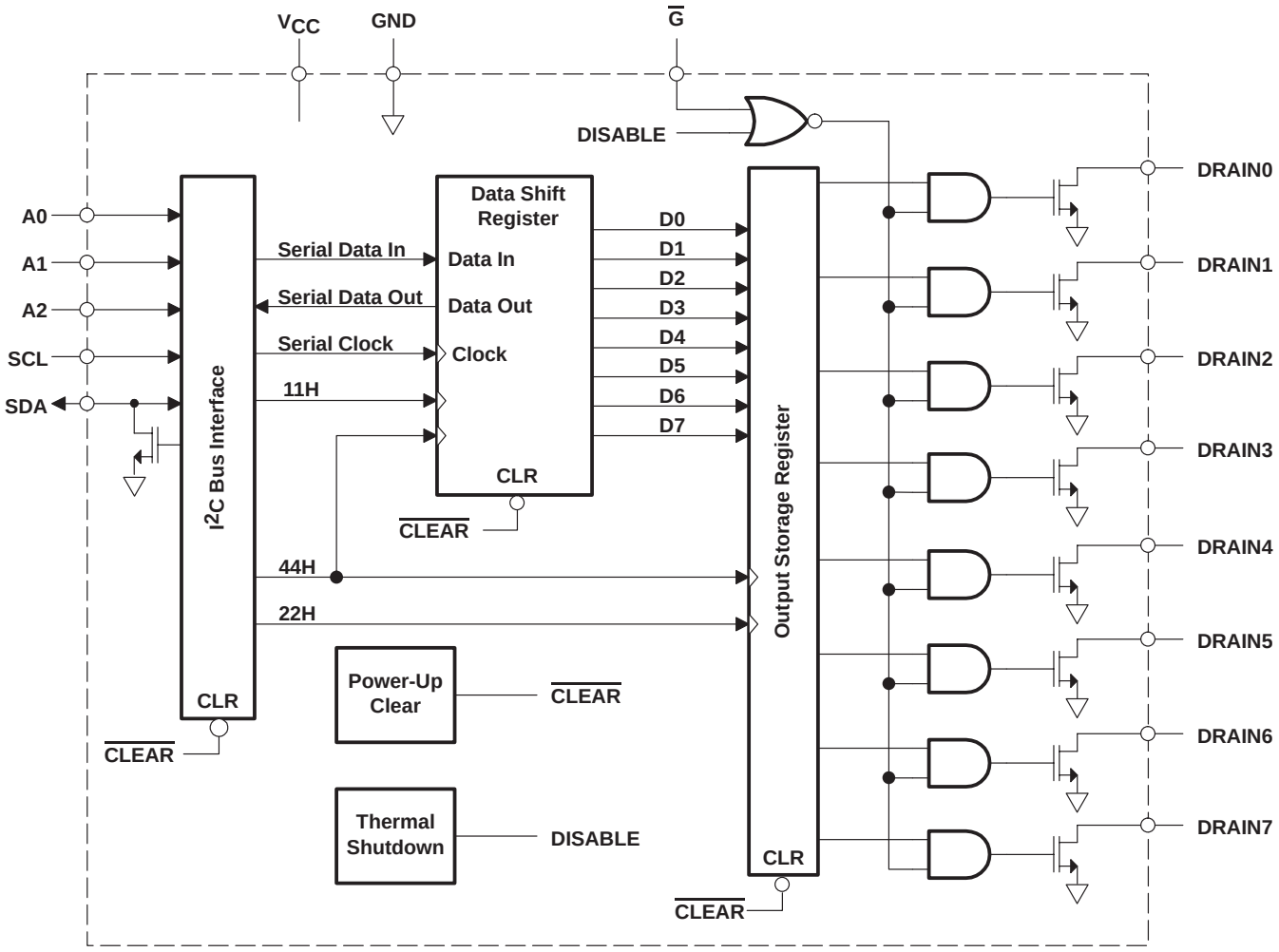
This device contains an 8-bit, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through the shift register via an I²C bus interface. Data is transferred into the data shift register only after the group ID and device address have been verified. The subaddress directs the I²C bus interface to read or write data to the device or transfer data to the output. When output enable ($\overline{G}$) is held high, all drain outputs are off. When $\overline{G}$ is held low, data from the output storage register is transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are off. When data is high, the DMOS transistor outputs have sink-current capability.

The TPIC2810 device has an internal power-up clear to initialize all registers to an off state when power is applied to the device. It also has a thermal sensor to monitor the die temperature and shut the drain outputs off, if an over current condition occurs.

Outputs are low-side, open-drain DMOS transistors with output ratings of 40 V and 100 mA continuous sink-current capability. Each output provides a 210-mA maximum current limit at T_C = 25°C. The current limit decreases as the junction temperature increases for additional device protection. The device also provides up to 3000 V of ESD protection on output terminals and 2000 V of ESD protection on input terminals when tested using the human-body model.

The TPIC2810 device is characterized for operation over the operating case temperature range of −40°C to 125°C.

functional block diagram

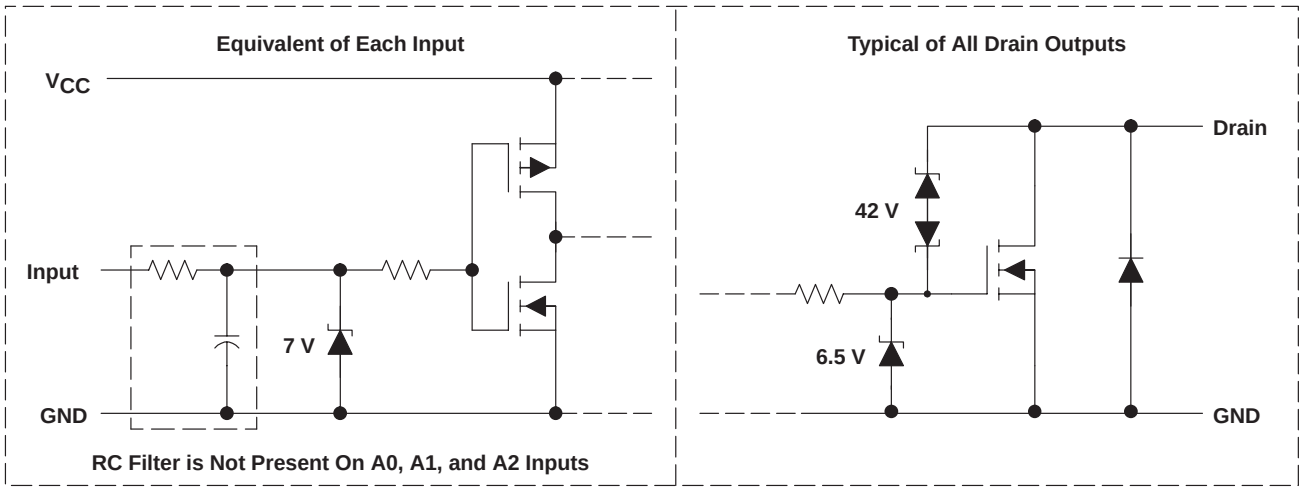


See the *TPIC2810 subaddress and I²C protocol definition* section of this data sheet for definition of the 11H, 22H, and 44H control signals.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
A0	9	I	Address input 0
A1	10	I	Address input 1
A2	7	I	Address input 2
DRAIN0	3	O	FET drain outputs. The DRAIN terminals are low-side switches for resistive loads.
DRAIN1	4		
DRAIN2	5		
DRAIN3	6		
DRAIN4	11		
DRAIN5	12		
DRAIN6	13		
DRAIN7	14		
$\overline{G}$	8	I	Output enable. Active low input enables output FETs when low and disables output FETs when high.
GND	16	O	Ground
SCL	15	I	Serial clock
SDA	2	I/O	Open drain, bidirectional serial data terminal
V_{CC}	1	I	Supply voltage input

schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

Logic supply voltage range, V_{CC} (see Note 1) . . . . . 7 V
Logic input voltage range, V_I . . . . . −0.3 V to 7 V
Power DMOS drain-to-source voltage, V_{DS} (see Note 2) . . . . . 40 V
Continuous source-to-drain diode anode current . . . . . 210 mA
Pulsed source-to-drain diode anode current (see Note 3) . . . . . 420 mA
Pulsed drain current, each output, all outputs on, I_D, T_C = 25°C (see Note 3) . . . . . 210 mA
Peak drain current, single output, I_{DM}, T_C = 25°C (see Note 3) . . . . . 210 mA
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . −40°C to 150°C
Operating case temperature range, T_C . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Each power DMOS source is internally connected to GND.
3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.

DISSIPATION RATING TABLE

PACKAGE	T_C = 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
D	1087 mW	8.7 mW/°C	217 mW

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC}	3.0	5.5	V
High-level input voltage, V_{IH}	$0.7V_{CC}$		V
Low-level input voltage, V_{IL}		$0.3V_{CC}$	V
Pulse drain output current, T_C = 25°C, V_{CC} = 5 V, all outputs on (see Notes 3 and 4 and Figure 8)		210	mA
Operating case temperature, T_C	−40	125	°C

NOTES: 3. Pulse duration ≤ 100 μs and duty cycle ≤ 2%.
4. Technique must limit $T_J - T_C$ to 10°C maximum.

electrical characteristics, V_{CC} = 5 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Logic supply voltage			3		5.5	V
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	I_D = 1 mA		40			V
V_{SD}	Source-to-drain diode forward voltage	I_F = 100 mA			0.85	1.2	V
V_{PUC}	Power-up clear voltage	V_{CC} rising no load,	See Note 5			2.84	V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	$V_I = V_{CC}$			1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0			−1	µA
V_{HYS}	Digital input hysteresis				1.1		V
I_{CC}	Logic supply current	V_{CC} = 5.5 V	All outputs off		0.62	1	mA
			All outputs on		0.7	1	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SCL} = 100 kHz, All outputs off,	C_L = 30 pF, See Figure 3		0.74	1	mA
I_{OL}	Low level output current; SDA	V_{OL} = 0.4 V			13		mA
I_L	Leakage current; SDA	$V_I = V_{CC}$		−1		1	µA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, T_C = 85°C,	$I_N = I_D$, See Notes 4, 6, 7		75		mA
I_{DSX}	Off-state drain current	V_{DS} = 30 V	V_{CC} = 5.5 V		0.3	0.6	µA
		V_{DS} = 30 V, T_C = 125°C			0.3	0.6	
T_{TSD}	Thermal shutdown set points			160			°C
T_{HYS}	Thermal shutdown hysteresis			10	20	30	°C
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 100 mA, V_{CC} = 3 V	See Notes 4 and 6 and Figures 4 and 5		8.0	10.8	Ω
		I_D = 100 mA, V_{CC} = 4.5 V			5.1	6.9	
		I_D = 100 mA, V_{CC} = 3.0 V, T_C = 125°C			13.0	18.2	
		I_D = 100 mA, V_{CC} = 4.5 V, T_C = 125°C			8.0	11.2	

NOTES: 4. Technique must limit $T_J - T_C$ to 10°C maximum
5. The power-up clear resets the I²C interface and clears all outputs.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage of 0.5 V at T_C = 85°C.

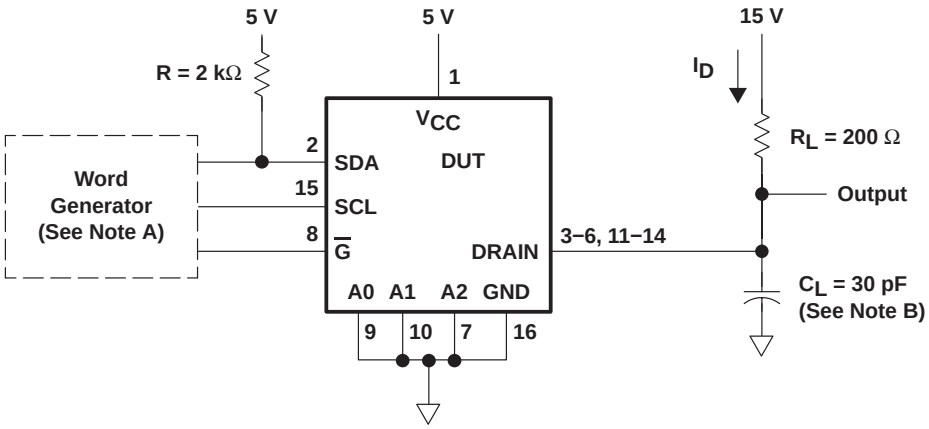
switching characteristics, V_{CC} = 5 V, T_C = 25°C, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_L = 30 pF, I_D = 75 mA, See Figures 1, 2, and 6		1.15		µs
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			0.64		
$t_{r(OUT)}$	Rise time, drain output			1.05		
$t_{f(OUT)}$	Fall time, drain output			0.89		µs
$f_{(SCL)}$	Serial clock frequency				100	kHz
					400	
					2	MHz
$t_{(BUF)}$	Bus free time between stop and start condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
$t_{(SP)}$	Tolerable spike width on bus				50	ns
$t_{pd(ACK)}$	SCL low to data out valid (acknowledge)			120		ns
t_{LOW}	SCL low time	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
		SCL = 2 MHz	250			ns
t_{HIGH}	SCL high time	SCL = 100 kHz	4.0			µs
		SCL = 400 kHz	600			ns
		SCL = 2 MHz	200			
$t_{su(DAT)}$	SDA → SCL setup time	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
		SCL = 2 MHz	10			
$t_{su(STA)}$	Start condition setup time	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	600			ns
		SCL = 2 MHz	300			
$t_{su(STO)}$	Stop condition setup time	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
		SCL = 2 MHz	140			
$t_{h(DAT)}$	SDA → SCL hold time		50			ns
$t_{h(STA)}$	Start condition hold time	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
		SCL = 2 MHz	160			ns
$t_{r(SCL)}$	Rise time of SCL signal	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
		SCL = 2 MHz			70	
$t_{f(SCL)}$	Fall time of SCL signal	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
		SCL = 2 MHz			70	
$t_{r(SDA)}$	Rise time of SDA signal	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
		SCL = 2 MHz			70	
$t_{f(SDA)}$	Fall time of SDA signal	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
		SCL = 2 MHz			140	

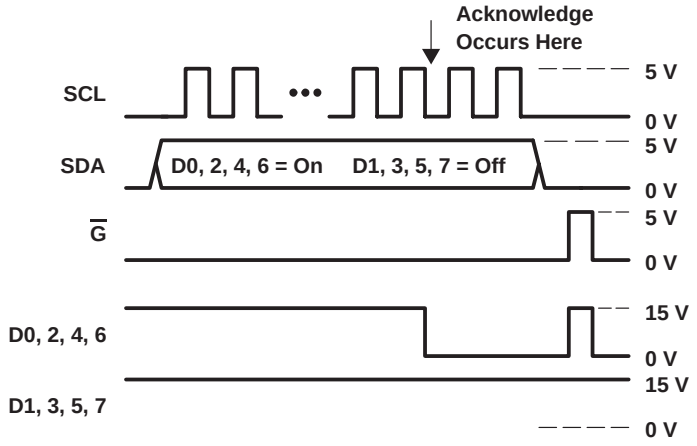
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All 8 outputs with equal power		115	°C/W

PARAMETER MEASUREMENT INFORMATION



Test Circuit

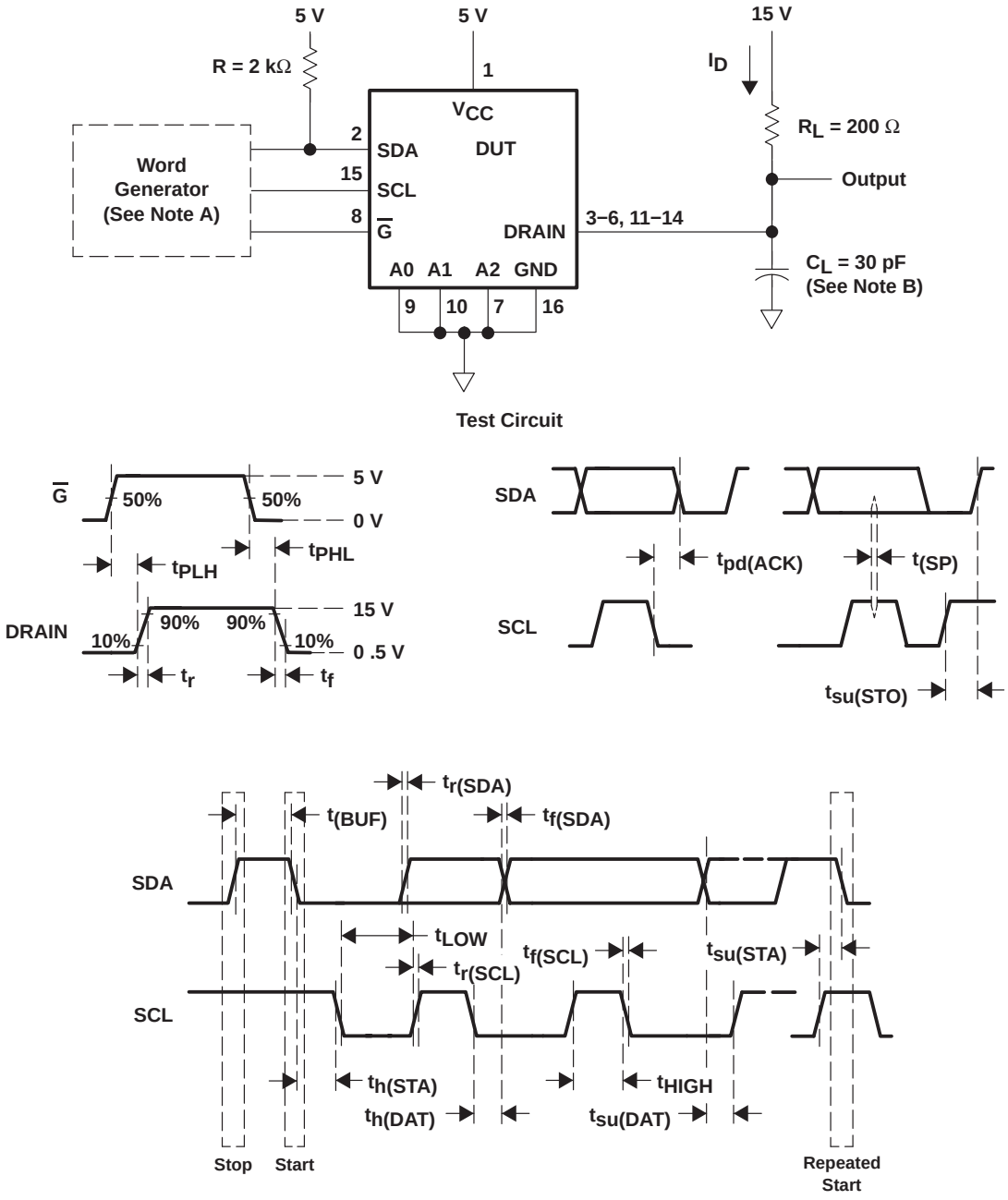


Voltage Waveforms

NOTES: A. The word generator has the following characteristics: $t_r \le 30$ ns, $t_f \le 30$ ns, pulsed repetition rate (PRR) = 400 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \le 30$ ns, $t_f \le 30$ ns, pulsed repetition rate (PRR) = 400 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times and Voltage Waveforms

TYPICAL CHARACTERISTICS

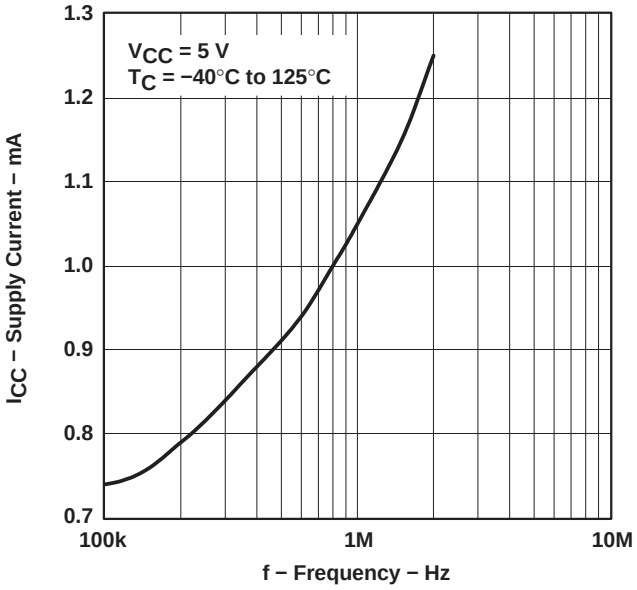


Figure 3. Supply Current vs Frequency

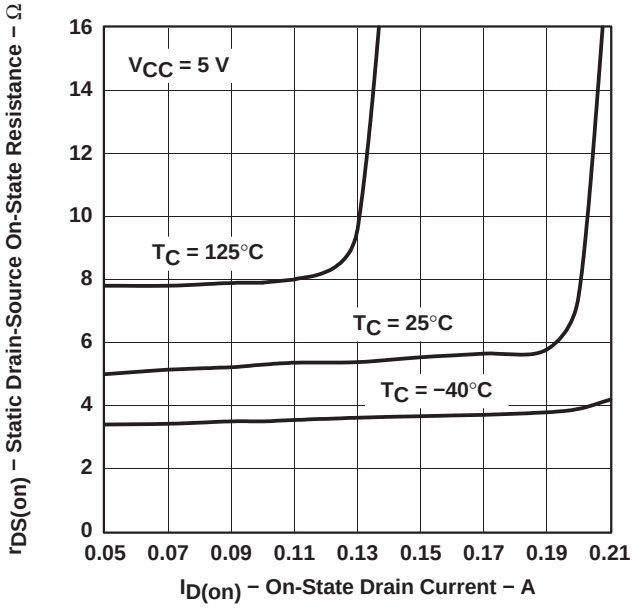


Figure 4. Static Drain-Source On-State Resistance vs On-State Drain Current

TYPICAL CHARACTERISTICS

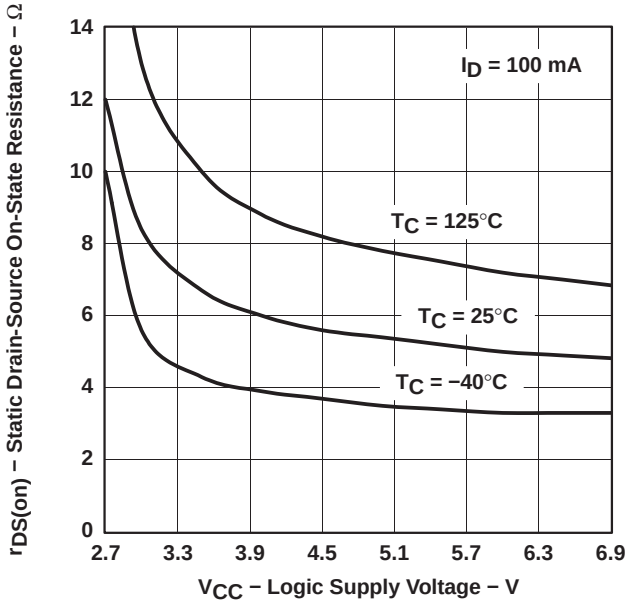


Figure 5. Static Drain-Source On-State Resistance vs Logic Supply Voltage

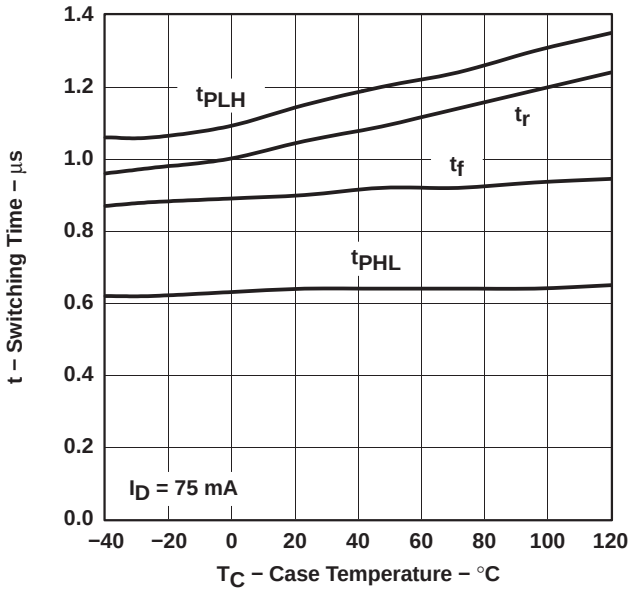


Figure 6. Switching Time vs Case Temperature

TYPICAL CHARACTERISTICS

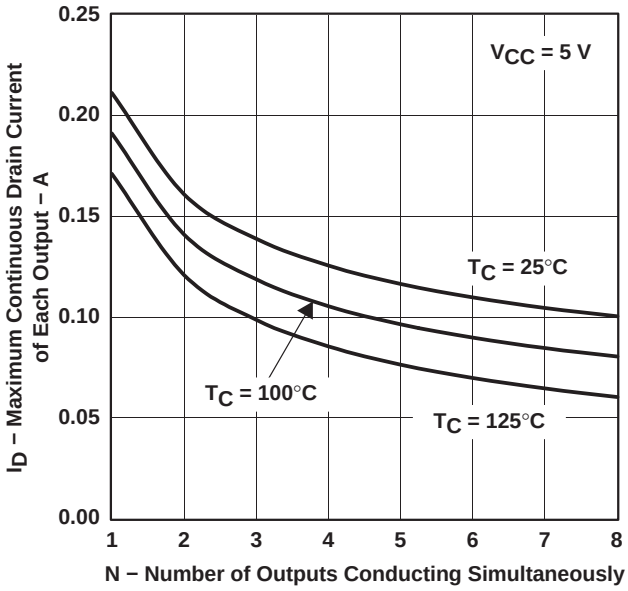


Figure 7. Maximum Continuous Drain Current Of Each Output vs Number Of Outputs Conducting Simultaneously

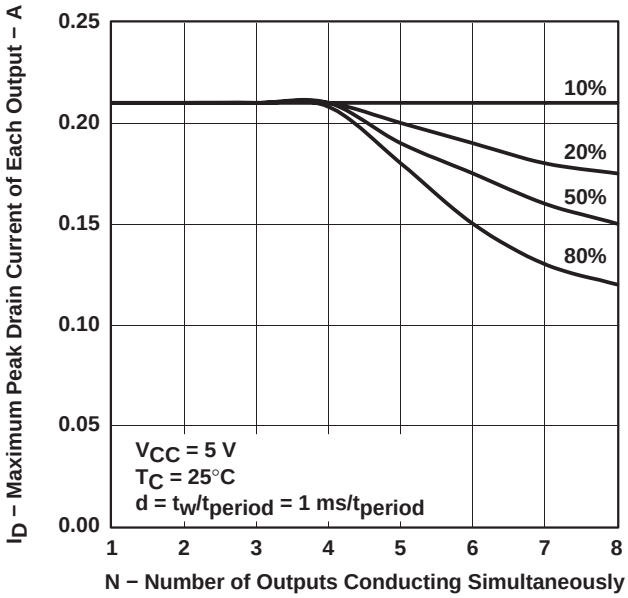
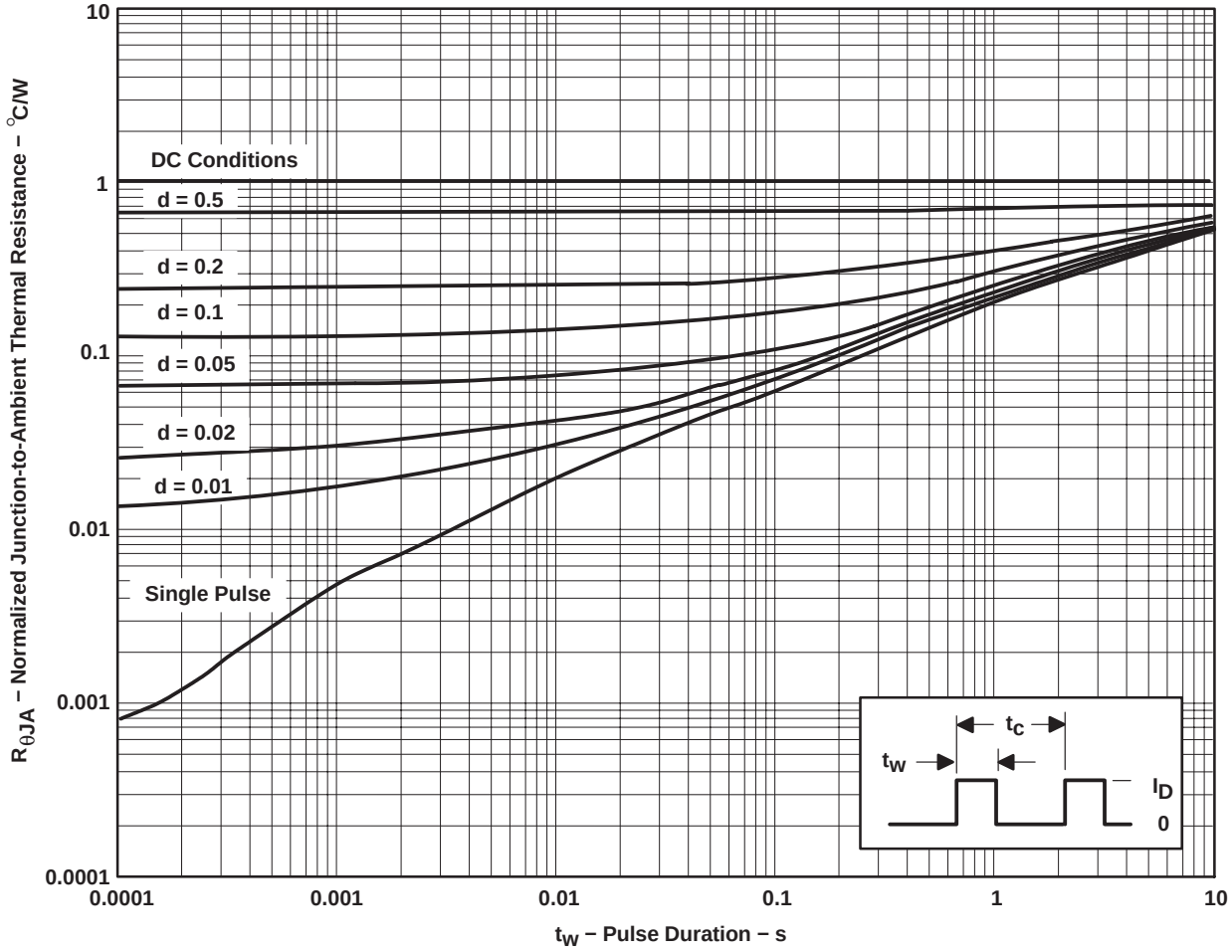


Figure 8. Maximum Peak Drain Current Of Each Output vs Number Of Outputs Conducting Simultaneously

THERMAL INFORMATION

D PACKAGE†



† Device mounted on FR4 printed-circuit board with no heat sink

NOTES: $Z_{\theta A}(t) = r(t)\ R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 9. Normalized Junction-to-Ambient Thermal Resistance vs Pulse Duration

PRINCIPLES OF OPERATION

TPIC2810 subaddress and I²C protocol definition

subaddress definition:

Summary:

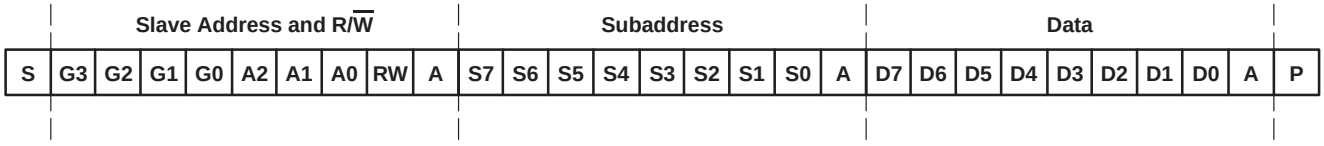
HEX Value	R/$\overline{W}$ Bit	Function
11H	1	Read data from the input register
11H	0	Write data to the data shift register, do not transfer to output register
22H	0	Command to transfer data from the data shift register to the output storage register
44H	0	Write data to the data shift register and transfer it to the output storage register immediately (extra load 22H command not needed)
Other	x	No action on undefined subaddresses

All other undefined subaddress values are not acknowledged.

register definition:

- The data shift register receives serial data from the I²C interface.
- The data shift register receives data from the input interface and holds it until it is transferred to the output storage register.
- The output storage register controls whether the FET is on or off.

TPIC2810 I²C input interface protocol definition



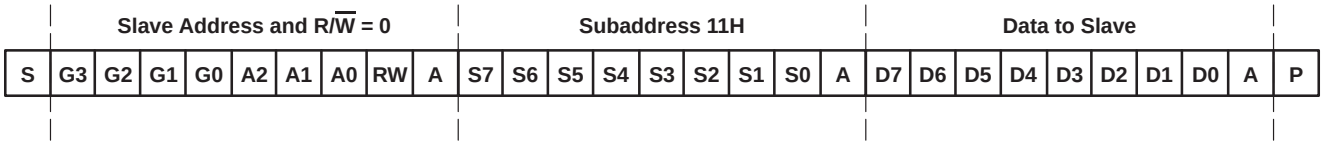
S	**Start Condition**
G	**Group ID: Defined as 1100**
A(0:2)	**Device Address Selectable Via Input Terminals**
RW	**Read/Write Select Bit**
A	**Acknowledge**
Subaddress	**Defined Per Subaddress Table**
Data	**Data to Be Loaded Into the Shift and Output Registers**
P	**Stop Condition**

PRINCIPLES OF OPERATION

Case 1: Read/Write serial data, but do not load output register

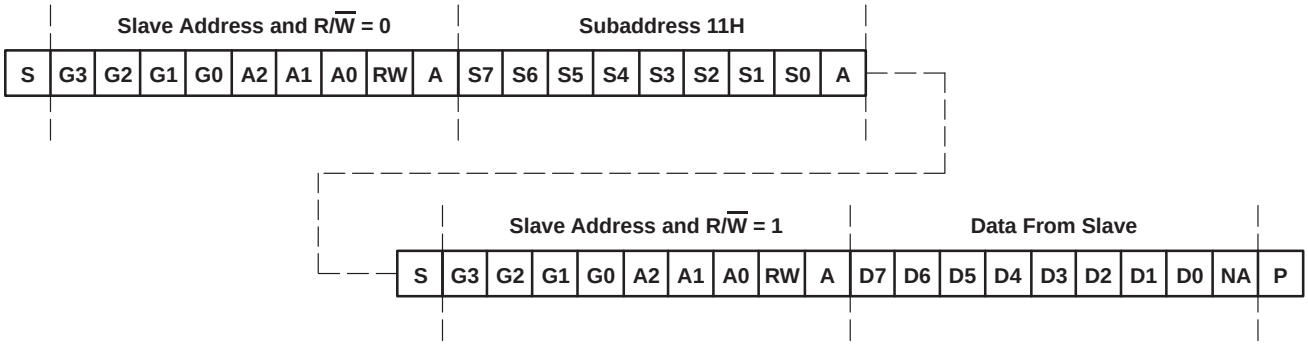
This case loads the data shift register with data via the I²C interface. Data is not transferred to the output storage register.

write operation:



G[3:0]: Fixed at 1100
A[2:0]: Selectable Via Input Terminals
RW: 0 = Write Shift Register
Subaddress: 11H (0001 0001)
Data: Output Data to the TPIC2810 Device
Acknowledge: Occurs After Valid Address Byte, After the Subaddress Byte, and After the Data Byte

read operation:

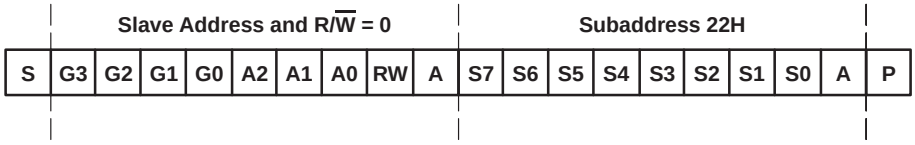


G[3:0]: Fixed at 1100
A[2:0]: Selectable Via Input Terminals
RW: 1 = Read Shift Register (Note the Slave Address RW Bit = 0)
Subaddress: 11H (0001 0001)
Data: Input Data From the TPIC2810 Device
Acknowledge: Occurs After Valid Address Byte and After the Subaddress Byte

PRINCIPLES OF OPERATION

Case 2: Transfer serial data to output storage register

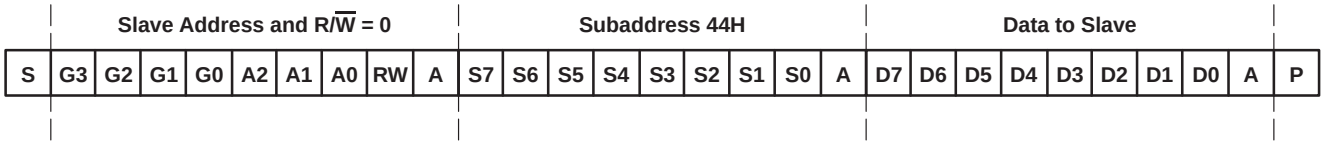
This case transfers data from the data shift register to the output storage register. The transfer must occur during the subaddress acknowledge bit and the data byte is ignored.



G[3:0]: Fixed at 1100
A[2:0]: Selectable Via Input Terminals
RW: 0 = Write Shift Register
Subaddress: 22H (0010 0010)
Data: Output Data to the TPIC2810 Device
Acknowledge: Occurs After Valid Address Byte and After the Subaddress Byte

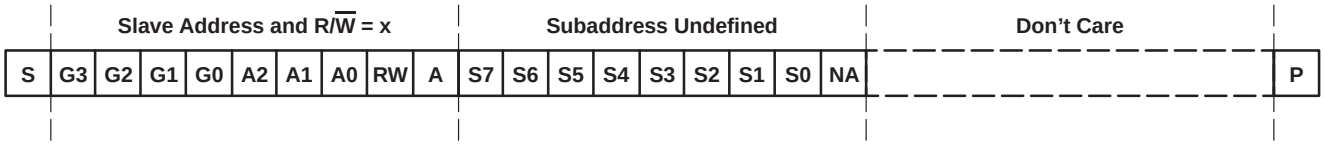
Case 3: Read serial data and load output storage register

This case loads the data shift register with data via the I2C interface and transfers the data to output storage register, if R/$\overline{W}$ = 0. The transfer occurs during the acknowledge bit following the data byte. Data byte and transfer to the output register is ignored if R/$\overline{W}$ = 1.



G[3:0]: Fixed at 1100
A[2:0]: Selectable Via Input Terminals
RW: 0 = Write Shift Register
Subaddress: 44H (0100 0100)
Data: Output Data to the TPIC2810 Device
Acknowledge: Occurs After Valid Address Byte, After the Subaddress Byte and After the Data Byte

Case 4: Undefined subaddress values



G[3:0]: Fixed at 1100
A[2:0]: Selectable Via Input Terminals
RW: Don't Care
Subaddress: All Bit Combinations Except 11H, 22H, and 44H
Data: Don't Care; Data Is Ignored
Acknowledge: Occurs After Valid Address Byte, But Is Not Issued After an Undefined Subaddress Byte or After the Data Byte Following an Undefined Subaddress Byte

PRINCIPLES OF OPERATION

I2C bus operation

The I2C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data signal is bidirectional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data signal to provide the high level portion of the data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 10. Both the SCL and SDA signals must remain in a logic high state when the controller is not communicating with the slave devices. A start condition is recognized by the slave devices when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the TPIC2810 device receives serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device issues an acknowledge pulse and prepares the receive subaddress data. The group ID for the TPIC2810 device is hard coded to be 1100. The slave address bits are set to correspond to the A(0:2) inputs for the device. Up to eight TPIC2810 devices can be placed on the bus. Subaddress data is decoded and responded to as per the *TPIC2810 subaddress and I2C protocol definition* section of this data sheet. Data transmission is complete by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low-to-high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal.

An acknowledge is issued by the TPIC2810 device after the reception of valid address, subaddress and data words as per the *TPIC2810B subaddress and I2C protocol definition* section of this document. Reference Figure 10. The device acknowledges each byte of data that it receives from the controller.

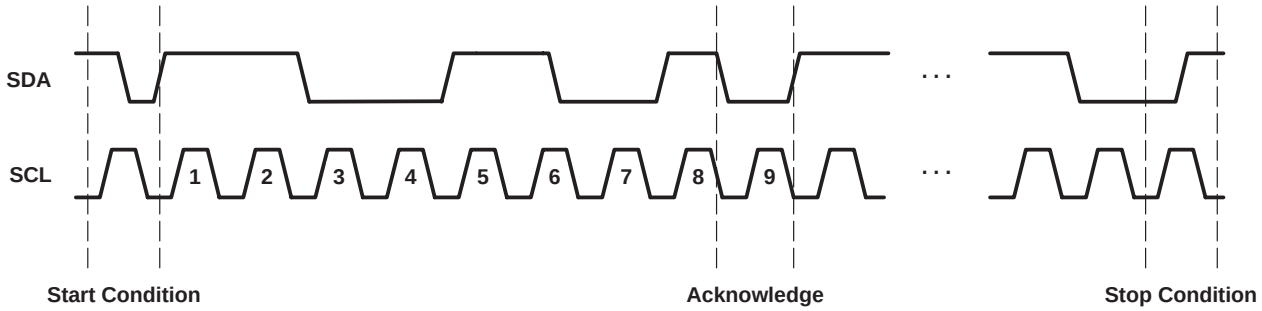


Figure 10. Start/Stop/Acknowledge Protocol

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPIC2810D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC2810	Samples
TPIC2810DG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TPIC2810	Samples
TPIC2810DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC2810	Samples
TPIC2810DRG4	LIFEBUY	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		IC2810	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

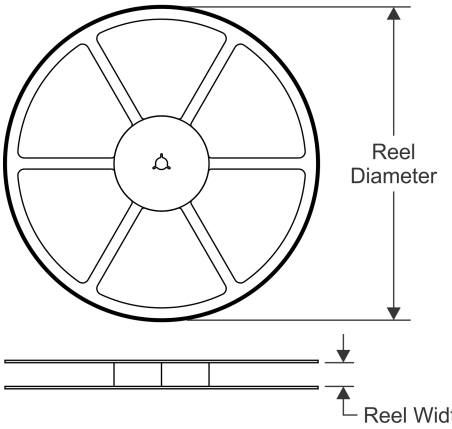
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

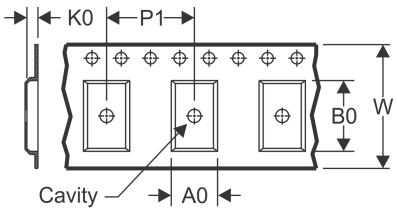
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

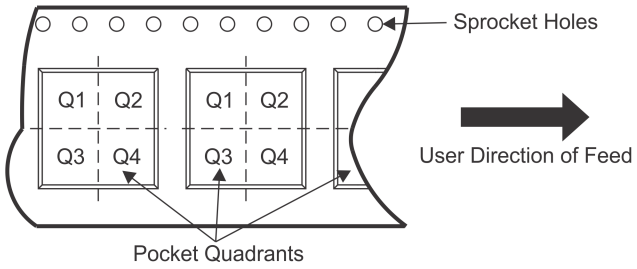


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

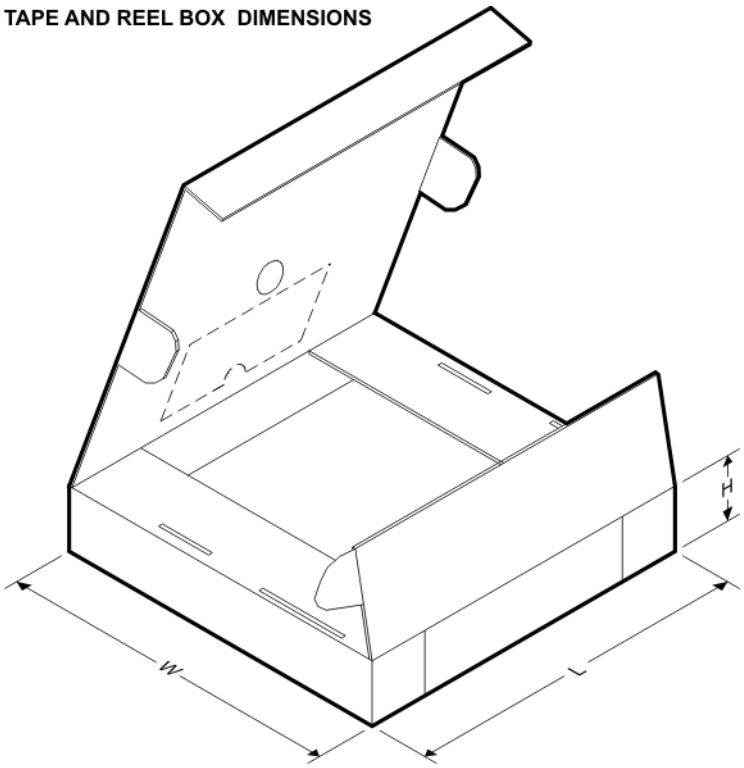
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC2810DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPIC2810DRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

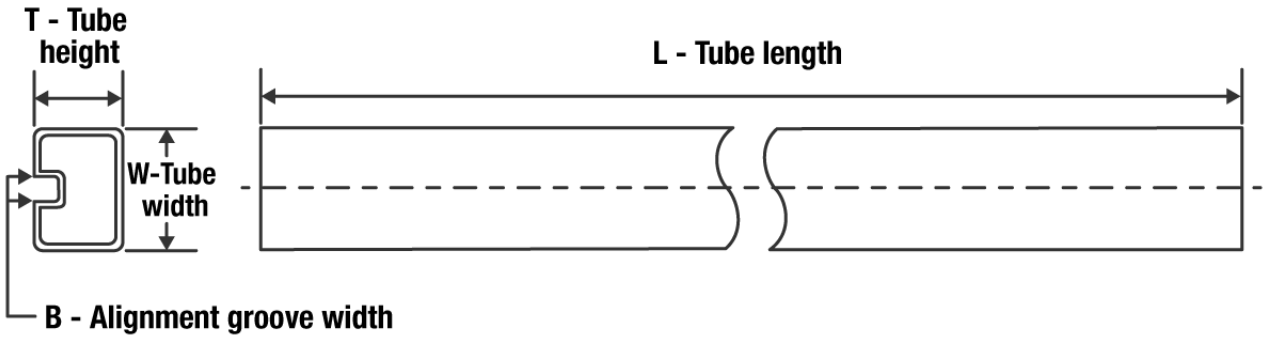
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC2810DR	SOIC	D	16	2500	350.0	350.0	43.0
TPIC2810DRG4	SOIC	D	16	2500	350.0	350.0	43.0

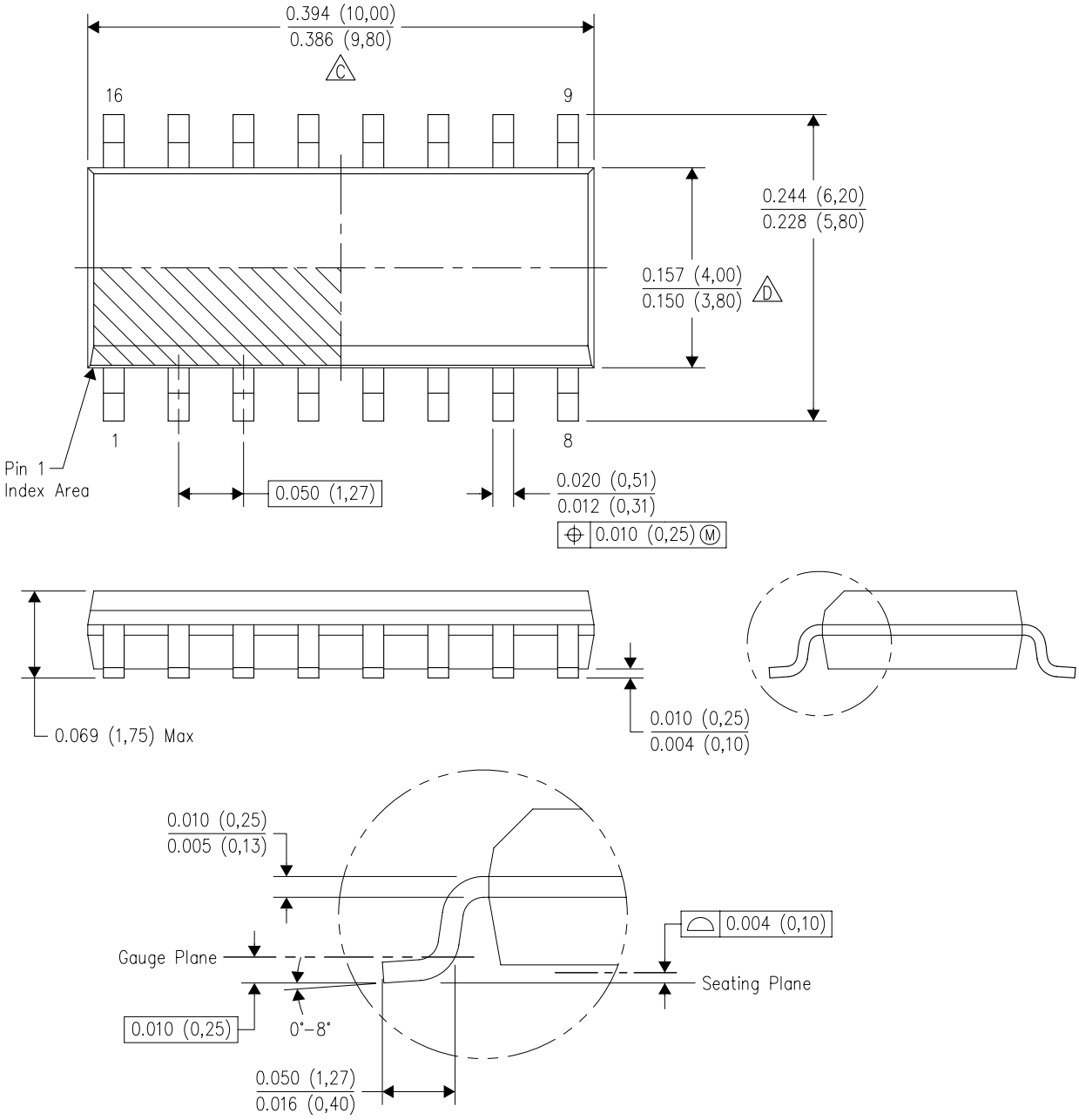
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPIC2810D	D	SOIC	16	40	505.46	6.76	3810	4
TPIC2810DG4	D	SOIC	16	40	505.46	6.76	3810	4

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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