TPS388C0x-Q1 Multichannel Overvoltage and Undervoltage I²C Programmable Voltage Supervisor and Monitor with Window Watchdog

1 Features

- ASIL-B Functional Safety-Compliant product
  - Development target for Functional Safety applications
  - Documentation to aid ISO 26262 system design
  - Systematic capability up to ASIL D
  - Hardware capability up to ASIL B
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C
- Monitor state-of-the art SoCs
  - Available in 2 to 6 voltage monitor channel options
  - Input voltage range: 2.6V to 5.5V
  - Undervoltage lockout (UVLO) (falling): 2.6V
  - High threshold accuracy:
    - ±6mV (–40°C to +125°C)
  - Fixed window threshold levels
    - 5mV steps from 0.2V to 1.475V
    - 20mV steps from 0.8V to 5.5V
- Trigger Window Watchdog
  - Programmable OPEN/CLOSE watchdog timing via I²C (1ms to 864ms)
  - Start-up delay for SoC boot up initialization (2ms to 3.48s)
  - Programmable maximum violation count (up to 7 errors) before WDO assertion
  - Programmable WDO Delay
  - Watchdog disable pin (WDE)
- Miniature package and minimal component cost
  - 3mm x 3mm QFN package
  - User adjustable voltage threshold levels via I²C
  - User adjustable glitch immunity and hysteresis levels via I²C
- Designed for safety applications
  - CRC Error Check (static and dynamic)
  - Active-low open-drain NIRQ, NRST, and WDO outputs

2 Applications

- Advanced driver assistance system (ADAS)
- Sensor fusion

3 Description

The TPS388C0x-Q1 device is an integrated multichannel window monitor reset IC with remote sense pin options and integrated window watchdog available in a 16-pin 3mm x 3mm QFN package.

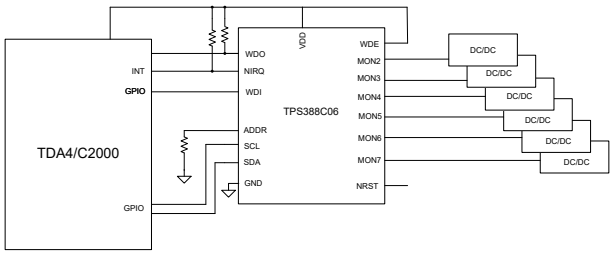
This highly accurate multichannel voltage supervisor is designed for systems that operate on low-voltage supply rails and have marginal supply tolerances. Internal glitch immunity and noise filters further eliminate false resets resulting from erroneous signals. This TPS388C0x-Q1 device does not require any external resistors for setting overvoltage and undervoltage reset thresholds, which further optimizes overall accuracy, cost, size, and improves reliability for safety systems. I²C functionality gives flexibility in selecting thresholds, reset delays, glitch filters, and pin functionality. This device offers CRC error checking. The device has a built in window watchdog with independent watchdog enable.

This device has a low typical quiescent current specification of 1500µA (typical). The TPS388C0x-Q1 is designed for automotive applications and is qualified for AEC-Q100 Grade 1 and qualified as a functional safety compliant device with ASIL-B rating.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM) (2)
TPS388C0x-Q1	WQFN (16)	3mm x 3mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS388C0x-Q1 Typical Circuit

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4 Device Comparison

Figure 4-1 illustrates the device nomenclature.Table 4-1 provides a summary of available device functions and corresponding part number. Contact TI sales representatives or go online to TI's E2E forum for details and availability of other options; minimum order quantities apply.

See Section 9.1 for more information regarding the device ordering codes.

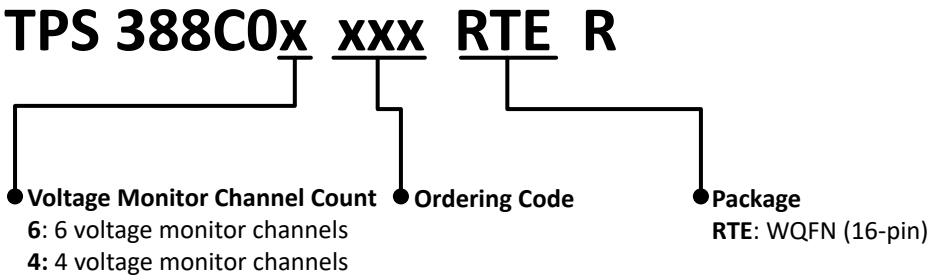

Figure 4-1. TPS388C0x-Q1 Device Nomenclature

Table 4-1. Multichannel Supervisor Summary Table

Specification	TPS38900x-Q1	TPS389R0x-Q1	TPS38800x-Q1	TPS388R0x-Q1	TPS389C0x-Q1	TPS388C0x-Q1
Hardware ASIL Rating	D	D	B	B	D	B
Monitoring Channel Count	4 to 8	4 to 7	4 to 8	4 to 7	3 to 6	3 to 6
Monitoring Range	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V	0.2 to 5.5V
Comparator Monitoring (HF Faults)	✓	✓	✓	✓	✓	✓
ADC Monitoring (LF Faults)	✓	✓	x	x	✓	x
Watchdog	x	x	x	x	Q&A	Window
Voltage Telemetry	✓	✓	x	x	✓	x
Monitor Glitch Filtering	✓	✓	✓	✓	✓	✓
Sequence Logging	✓	✓	✓	✓	x	✓
NIRQ PIN	✓	✓	✓	✓	✓	✓
NRST PIN	x	✓	x	✓	✓	✓
SYNC PIN	✓	x	x	x	x	x
WDO PIN	x	x	x	x	✓	✓
WDI PIN	x	x	x	x	x	✓
ESM PIN	x	x	x	x	✓	x

5 Pin Configuration and Functions

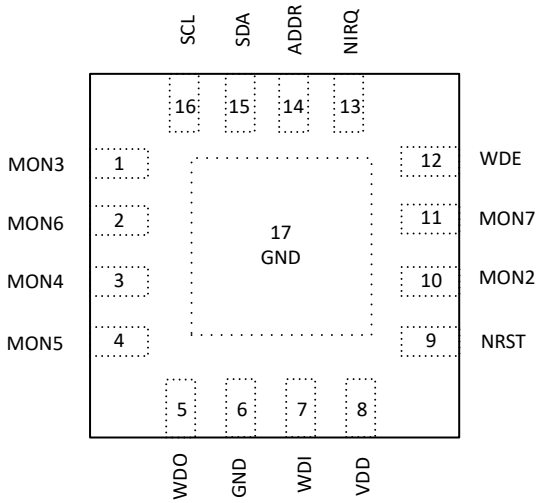

Figure 5-1. RTE Package
16-Pin WQFN
TPS388C06-Q1 Top View

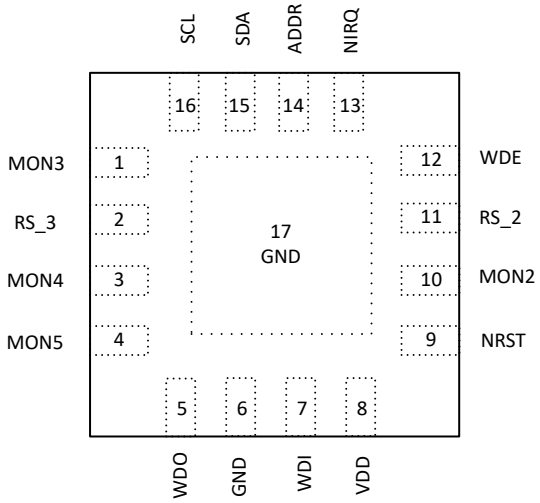

Figure 5-2. RTE Package
16-Pin WQFN
TPS388C04-Q1 Top View

Table 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NO.	TPS388C06-Q1	TPS388C04-Q1		
	NAME	NAME		
1	MON3	MON3	I	Voltage monitor channel 3
2	MON6	RS_3	I	MON6:Voltage monitor channel 6 RS_3: Remote sense for voltage monitor channel 3
3	MON4	MON4	I	Voltage monitor channel 4
4	MON5	MON5	I	Voltage monitor channel 5
5	WDO	WDO	O	Open drain Watchdog Error output
6	GND	GND	-	Power ground
7	WDI	WDI	I	Watchdog input
8	VDD	VDD	-	Power supply rail
9	NRST	NRST	I/O	Open drain Reset pin
10	MON2	MON2	I	Voltage monitor channel 2
11	MON7	RS_2	I	MON7: Voltage monitor channel 7 RS_2: Remote sense for voltage monitor channel 2
12	WDE	WDE	I	Watchdog enable
13	NIRQ	NIRQ	O	Active-low open-drain interrupt output
14	ADDR	ADDR	I	I^2C address select pin
15	SDA	SDA	I/O	I^2C data pin
16	SCL	SCL	I	I^2C clock pin
17	GND	GND	-	Exposed power ground pad

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	6	V
Voltage	NIRQ,NRST,WDO,WDI,WDE	–0.3	6	V
Voltage	SCL,SDA	–0.3	6	V
Voltage	ADDR	–0.3	2	V
Voltage	MONx	–0.3	6	V
Voltage	RS_x	-0.2	0.2	V
Current	NIRQ,NRST,WDO		±10	mA
Temperature (2)	Continuous total power dissipation	See the Thermal Information		
	Operating junction temperature, T_J	-40	150	°C
	Operating free-air temperature, T_A	-40	125	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
VDD	Supply pin voltage	2.6		5.5	V
NIRQ,NRST,WDI,WDO,WDE	Pin voltage	0		5.5	V
I_{NIRQ},I_{NRST},I_{WDO}	Pin Currents	0		±5	mA
ADDR	Address pin voltage	0		1.8	V
MONx	Monitor Pins	0		5.5	V
SCL,SDA	Pin Voltage	0		5.5	V
RS_x	Remote sense pins	-0.1		0.1	V
R_{UP} (1)	Pull-up resistor (Open Drain config)	1		100	kΩ
T_J	Junction temperature (free-air temperature)	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS388C0-Q1 RTE (WQFN) PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

At 2.6V ≤ VDD≤ 5.5V, 0.2V ≤ V_{MONX} ≤ 5.5V, NIRQ,NRST,WDO Rpullup = 10kΩ to V_{DD}, NIRQ,NRST,WDO load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
VDD	Input supply voltage		2.6		5.5	V
VDD_{UVLO}	Rising Threshold		2.67		2.81	V
	Falling Threshold		2.48		2.6	V
V_{POR}	Power on Reset Voltage [2]				1.65	V
I_{DD_Active}	Supply current into VDD pin (MON=HF active)	VDD≤5.5V		1.55	2	mA
V_{MONX}	MON voltage range		0.2		5.5	V
I_{MONX}	Input current MONx pins	V_{MON}=5V			20	µA
VMON_HF	No scaling		0.2		1.475	V
	with 4X scaling		0.8		5.5	V
Threshold Granularity	No scaling			5		mV
	with 4X scaling			20		mV
Accuracy	VMON	0.2V≤V_{MONX}≤1.0V	–6		6	mV
		1.0V≤V_{MONX}≤1.475V	-7.5		7.5	mV
		1.475V≤V_{MONX}≤2.95V	-0.6		0.6	%
		VMONX>2.95V	-0.5		0.5	%
V_{HYS}	Hysteresis on UV,OV pin(Hysteresis is with respect of the tripoint ((UV),(OV)) [1]	0.2V<V_{MONX}≤1.475V		5	11	mV
		1.475V≤V_{MONX}≤2.95V		9	16	
		VMONX>2.95V		17	28	mV
MON_OFF	OFF Voltage threshold	Monitored falling edge of V_{MON}	140		215	mV
I_{LKG}	Output leakage current -NIRQ,NRST	VDD=V_{NIRQ}=V_{NRST} =5.5V			300	nA
V_{OL}	Low level output voltage-NIRQ	NIRQ external 10K pull up to 3.3V			100	mV
$I_{lkg(OD)}$	Open-Drain output leakage current-NIRQ	NIRQ pin in High Impedance,V_{NIRQ}= 5.5V, V_{IT+} < VDD			90	nA
NIRQ	Internal Pull down	Open Drain		100		Ω
V_{OL}	Low level output voltage-NRST	NRST external 10K pull up to 3.3V			100	mV
$I_{lkg(OD)}$	Open-Drain output leakage current-NRST	NRST pin in High Impedance,V_{NRST}= 5.5, V_{IT+} < VDD			90	nA

6.5 Electrical Characteristics (continued)

At 2.6V ≤ VDD≤ 5.5V, 0.2V ≤ V_{MONX} ≤ 5.5V, NIRQ,NRST,WDO Rpullup = 10kΩ to V_{DD}, NIRQ,NRST,WDO load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD= 3.3V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low level output voltage-WDO	WDO external 10K pull up to 3.3V			100	mV
$I_{lkg(OD)}$	Open-Drain output leakage current-WDO	WDO pin in High Impedance,$V_{WDO=}$ 5.5, V_{IT+} < VDD			500	nA
WDO	On resistance when asserted low	Open drain		12	17	Ω
NRST	Internal Pull down	Open Drain		100		Ω
WDI_L	Logic Low Input				0.24xVDD	V
WDI_H	Logic High Input	VDD>4.5V	0.55xVDD			V
WDI_H	Logic High Input	VDD<4.5V	0.60xVDD			V
WDE_L	Logic Low Input				0.36	V
WDE_H	Logic High Input		1.26			V
I_{ADDR}	ADDR pin current			20		µA
I²C ADDR	(Hex format)	R=5.36k		0x30		
		R=16.2k		0x31		
		R=26.7k		0x32		
		R=37.4k		0x33		
		R=47.5k		0x34		
		R=59.0k		0x35		
		R=69.8k		0x36		
		R=80.6k		0x37		
TSD	Thermal Shutdown			155		℃
TSD Hys	Thernal Shutdown Hysterisis			25		℃
I²C ELECTRICAL SPECIFICATIONS						
C_B	Capacitive load for SDA and SCL				400	pF
SDA,SCL	Low Threshold	I²C logic for 1.2V			0.36	V
SDA,SCL	High Threshold	I²C logic for 1.2V	0.84			V
SDA,SCL	Low Threshold	I²C logic for 1.8V			0.54	V
SDA,SCL	High Threshold	I²C logic for 1.8V	1.26			V
SDA,SCL	Low Threshold	I²C logic for 3.3V			0.99	V
SDA,SCL	High Threshold	I²C logic for 3.3V	2.31			V
SDA	V_{OL}	I_{OL}=5mA			0.4	V

(1) Hysteresis is with respect of the tripoint ($V_{IT-(UV)}$, $V_{IT+(OV)}$).
(2) V_{POR} is the minimum V_{DDX} voltage level for a controlled output state.

6.6 Timing Requirements

At 2.6V ≤ VDD ≤ 5.5V, 0.2V ≤ VMON ≤ 5.5V, NIRQ,NRST,WDO Voltage = 10kΩ to VDD, NIRQ,NRST,WDO load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
COMMON PARAMETERS						
t_{BIST}	POR to ready with BIST, TEST_CFG.AT_POR=1	includes OTP load			12	ms
tNBIST	POR to ready without BIST, TEST_CFG.AT_POR=0	includes OTP load			2	ms
BIST	BIST time,TEST_CFG.AT_POR=1 or TEST_CFG.AT_SHDN=1				10	ms
t_{I2C_ACT}	I^2C active from BIST complete				0	µs
t_{NRST}	Fault detection to NRST assertion latency				25	µs
t_{WDO}	Fault detection to WDO assertion latency				25	µs
t_{NIRQ}	Fault detection to NIRQ assertion latency (except OV/UV faults)				25	µs
$t_{PD\_NIRQ\_1X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 100mV			650	ns
$t_{PD\_NIRQ\_4X}$	HF fault Propagation detect delay (default deglitch filter) includes digitial delay	VIT_OV/UV +/- 400mV			750	ns
t_D	RESET time delay	I^2C Register time delay =000		200		µs
		I^2C Register time delay =001		1		ms
		I^2C Register time delay =010		10		ms
		I^2C Register time delay =011		16		ms
		I^2C Register time delay =100		20		ms
		I^2C Register time delay =101		70		ms
		I^2C Register time delay =110		100		ms
		I^2C Register time delay =111		200		ms
t_{D_WD}	WDT delay	I^2C Register time delay =000		1		ms
		I^2C Register time delay =001		2		
		I^2C Register time delay =010		5		
		I^2C Register time delay =011		10		
		I^2C Register time delay =100		20		
		I^2C Register time delay =101		50		
		I^2C Register time delay =110		100		
		I^2C Register time delay =111		200		
t_{GI_R}	UV & OV debounce range via I^2C	FLT_HF(N)	0.1		102.4	µs

6.6 Timing Requirements (continued)

At 2.6V ≤ VDD ≤ 5.5V, 0.2V ≤ VMON ≤ 5.5V, NIRQ,NRST,WDO Voltage = 10kΩ to VDD, NIRQ,NRST,WDO load = 10pF, and over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C, typical conditions at VDD = 3.3V.

			MIN	NOM	MAX	UNIT
I²C TIMING CHARACTERISTICS						
f_{SCL}	Serial clock frequency	Standard mode			100	kHz
f_{SCL}	Serial clock frequency	Fast mode			400	kHz
f_{SCL}	Serial clock frequency	Fast mode +			1	MHz
t_{LOW}	SCL low time	Standard mode	4.7			µs
t_{LOW}	SCL low time	Fast mode	1.3			µs
t_{LOW}	SCL low time	Fast mode +	0.5			µs
t_{HIGH}	SCL high time	Standard mode	4			µs
t_{HIGH}	SCL high time	Fast mode +	0.26			µs
$t_{SU;DAT}$	Data setup time	Standard mode	250			ns
$t_{SU;DAT}$	Data setup time	Fast mode	100			ns
$t_{SU;DAT}$	Data setup time	Fast mode +	50			ns
$t_{HD;DAT}$	Data hold time	Standard mode	10		3450	ns
$t_{HD;DAT}$	Data hold time	Fast mode	10		900	ns
$t_{HD;DAT}$	Data hold time	Fast mode +	10			ns
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Standard mode	4.7			µs
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Fast mode	0.6			µs
$t_{SU;STA}$	Setup time for a Start or Repeated Start condition	Fast mode +	0.26			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Standard mode	4			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Fast mode	0.6			µs
$t_{HD:STA}$	Hold time for a Start or Repeated Start condition	Fast mode +	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
t_{BUF}	Bus free time between a STOP and START condition	Fast mode	1.3			µs
t_{BUF}	Bus free time between a STOP and START condition	Fast mode +	0.5			µs
$t_{SU;STO}$	Setup time for a Stop condition	Standard mode	4			µs
$t_{SU;STO}$	Setup time for a Stop condition	Fast mode	0.6			µs
$t_{SU;STO}$	Setup time for a Stop condition	Fast mode +	0.26			µs
t_{rDA}	Rise time of SDA signal	Standard mode			1000	
t_{rDA}	Rise time of SDA signal	Fast mode	20		300	ns
t_{rDA}	Rise time of SDA signal	Fast mode +			120	ns
t_{fDA}	Fall time of SDA signal	Standard mode			300	ns
t_{fDA}	Fall time of SDA signal	Fast mode	1.4		300	ns
t_{fDA}	Fall time of SDA signal	Fast mode +	6.5		120	ns
t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
t_{rCL}	Rise time of SCL signal	Fast mode	20		300	ns
t_{rCL}	Rise time of SCL signal	Fast mode +			120	ns
t_{fCL}	Fall time of SCL signal	Standard mode			300	ns
t_{fCL}	Fall time of SCL signal	Fast mode	6.5		300	ns
t_{fCL}	Fall time of SCL signal	Fast mode +	6.5		120	ns
t_{SP}	Pulse width of SCL and SDA spikes that are suppressed	Standard mode, Fast mode and Fast mode +			50	ns

6.7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3V , and R_{PU} = 10kΩ, unless otherwise noted.

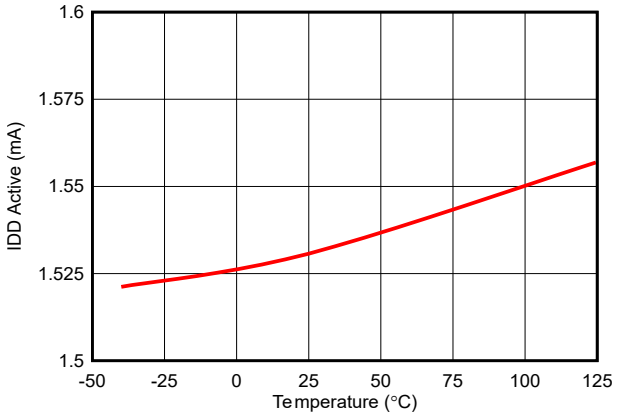

Figure 6-1. Active Input Current Vs Temperature

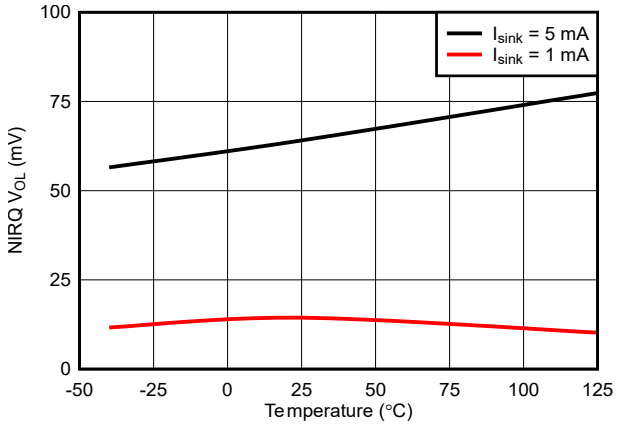

Figure 6-2. NIRQ Low Level Output Voltage Vs Temperature

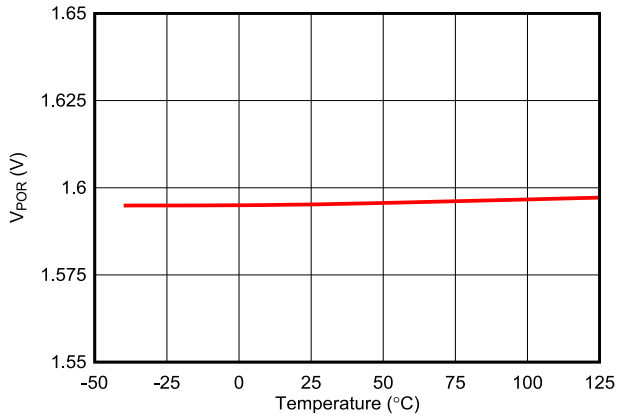

Figure 6-3. Power-on-Reset Voltage Vs Temperature

7 Detailed Description

7.1 Overview

The TPS388C0x-Q1 family of devices has two to six channels that can be configured for over voltage, under voltage or both in a window configuration. The TPS388C0x-Q1 features highly accurate window threshold voltages (up to ±6mV) and a variety of voltage thresholds which can be factory configured or set on boot up by I^2C commands.

The TPS388C0x-Q1 includes the resistors used to set the overvoltage and undervoltage thresholds internal to the device. These internal resistors allow for lower component counts and greatly simplifies the design because no additional margins are needed to account for the accuracy of external resistors.

The TPS388C0x-Q1 is designed to assert active low output signals (NIRQ and/or NRST) when the monitored voltage is outside the safe window. TPS388C0x-Q1 is highly configurable through I^2C and factory programming options for interrupt enabling, sequence timeout, BIST, voltage monitoring windows, wathdog window timing, and glitch debounce timing.

7.2 Functional Block Diagram

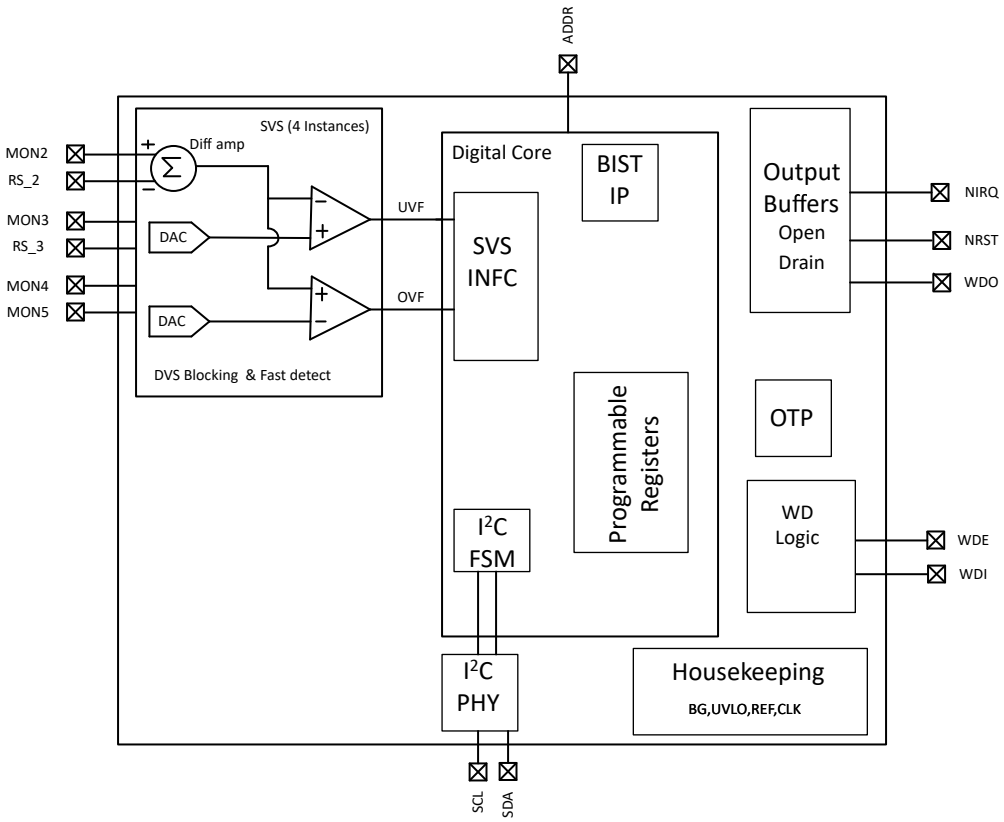

Figure 7-1. TPS388C04-Q1 Block Diagram

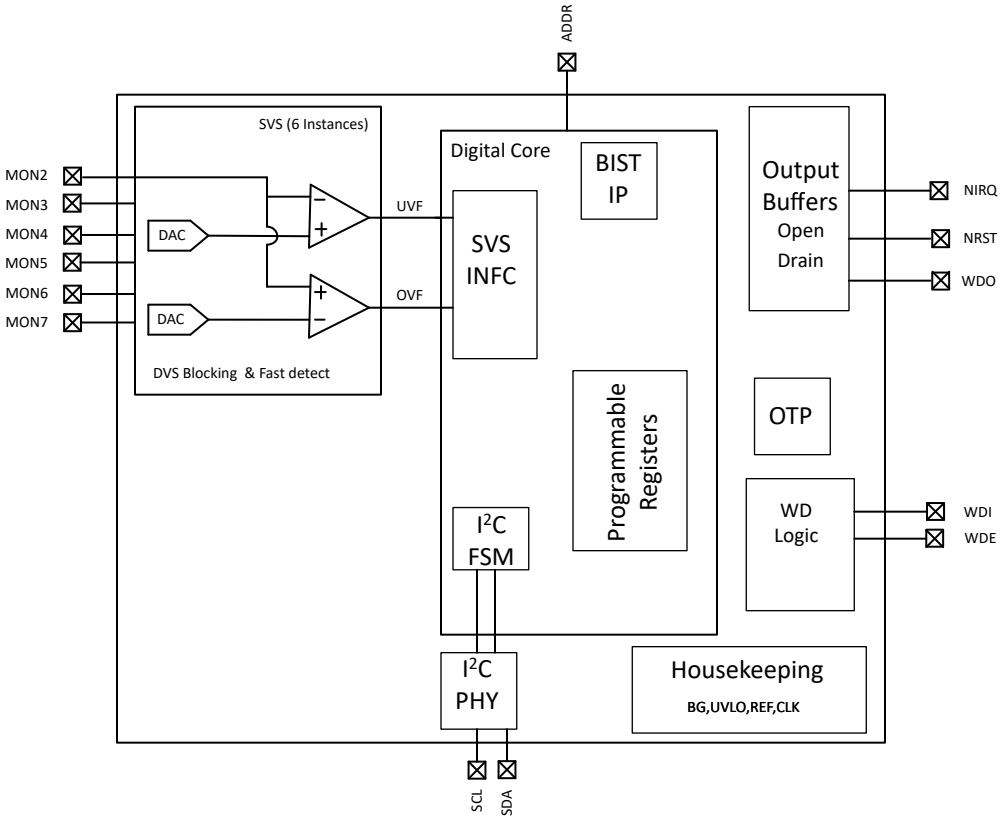

Figure 7-2. TPS388C06-Q1 Block Diagram

7.3 Device Functional Modes

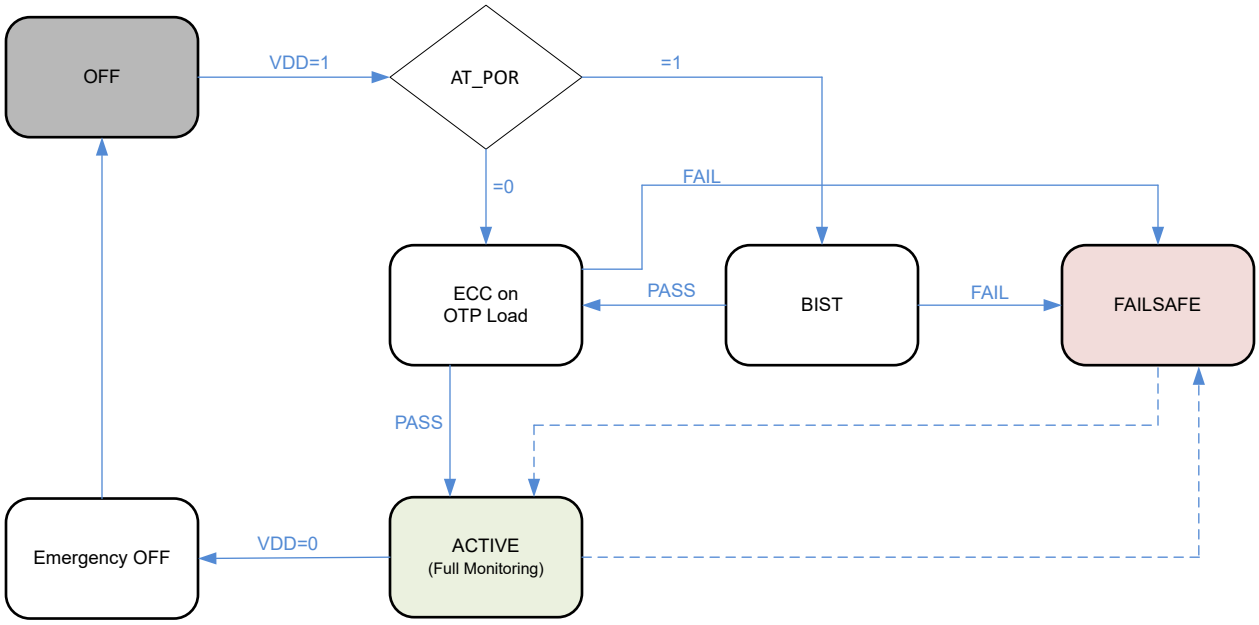

Figure 7-3. TPS388C0x-Q1 State Diagram

7.3.1 TPS388C0x-Q1 Power ON

When the TPS388C0x-Q1 is powered ON, BIST is optionally executed (depending on TEST_CFG.AT_POR register bit); I^2C and fault reporting (through NIRQ) become active as soon as BIST is completed and configuration is loaded from OTP (assisted by ECC, supporting SEC-DED).

The details of the configuration load ECC and BIST results are reported are reported in TEST_INFO register.

Upon detection of the Vin rising edge past UVLO, the TPS388C0x-Q1 starts the sequence timeout timer and the monitoring of the power ON sequence.

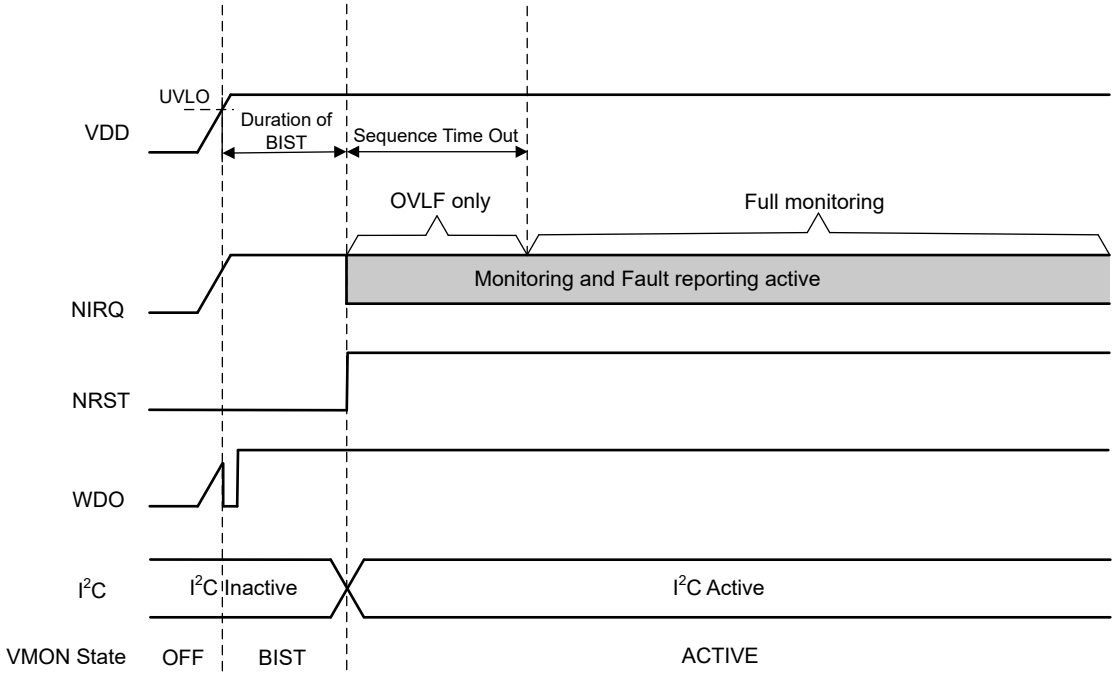

Figure 7-4. TPS388C0x-Q1 Power ON Signaling and Internal States

BIST completion can be detected through interrupt or register polling:

- Interrupt: INT_TEST.I_BIST_C flag is set and NIRQ is asserted if IEN_TEST.BIST_C=1
- Polling: VMON_STAT register can be polled to read the ST_BIST_C bit

7.3.2 Built-In Self Test and Configuration Load

Built-In Self Test (BIST) is performed:

1. At Power On Reset (POR), if TEST_CFG.AT_POR=1

Configuration load from OTP is assisted by ECC (supporting SEC-DED). This is to protect against data integrity issues and to maximize system availability.

During BIST, NIRQ is de-asserted (asserted in case of failure), input pins are ignored, and the I^2C block is inactive with SDA and SCL de-asserted. The BIST includes device testing to meet the Technical Safety Requirements. Once BIST is completed without failure, I^2C is immediately active and the device enters the IDL sate after loading the configuration data from OTP. If BIST fails and/or ECC reports Double-Error Detection (DED), NIRQ is asserted, the device enters FAILSAFE state, and a best effort attempt is made to active I^2C. TEST_INFO register can provide additional information on the test results.

The detailed behavior upon success/failure of the BIST is controlled by INT_TEST and IEN_TEST registers. Reporting of the BIST results is carried out through:

- NIRQ pin: pulled low depending on the test result and BIST_C and BIST bits in IEN_TEST
- I_BIST_C and BIST bits in INT_TEST register depending on IEN_TEST settings
- VMON_STAT.ST_BIST_C register bit
- TEST_INFO[3:0] register bits

7.3.2.1 Notes on BIST Execution

Upon POR the TPS388C0x-Q1 needs to make a decision whether to run BIST or not, based on the value of the TEST_CFG.AT_POR register bit. Assuming that ECC on this register is performed after BIST has checked the ECC logic, not possible to prove data integrity before running BIST.

7.3.3 General Monitoring

7.3.3.1 ACTIVE Monitoring

The TPS388C0x-Q1 is in ACTIVE state when BIST and SEQ_TOUT (Auto-mask) timeout have completed as seen in Figure 7-5.

During SEQ_TOUT all TPS388C0x-Q1 inputs selected with auto-mask register AMSK_ON start with masked (disabled) interrupts for Under-Voltage High Frequency (UVHF) and Over-Voltage High Frequency (OVHF) conditions. As each rail passes the MON's OFF threshold, automatically (and expected to happen within about 5-10 µs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVHF and IEN_OVHF registers.

Once SEQ_TOUT has expired active state has been entered VMON monitors High Frequency channel levels against Under-Voltage High Frequency (UVHF) and Over-Voltage High Frequency (OVHF) thresholds. Table 7-1 summaries the specifics of the active state.

Table 7-1. ACTIVE Mode of Operation Summary

Mode	Condition	Iq	Monitored- Triggers NIRQ if CHx enabled
ACTIVE	Auto-Mask Timeout	1.5mA	OVHF, UVHF

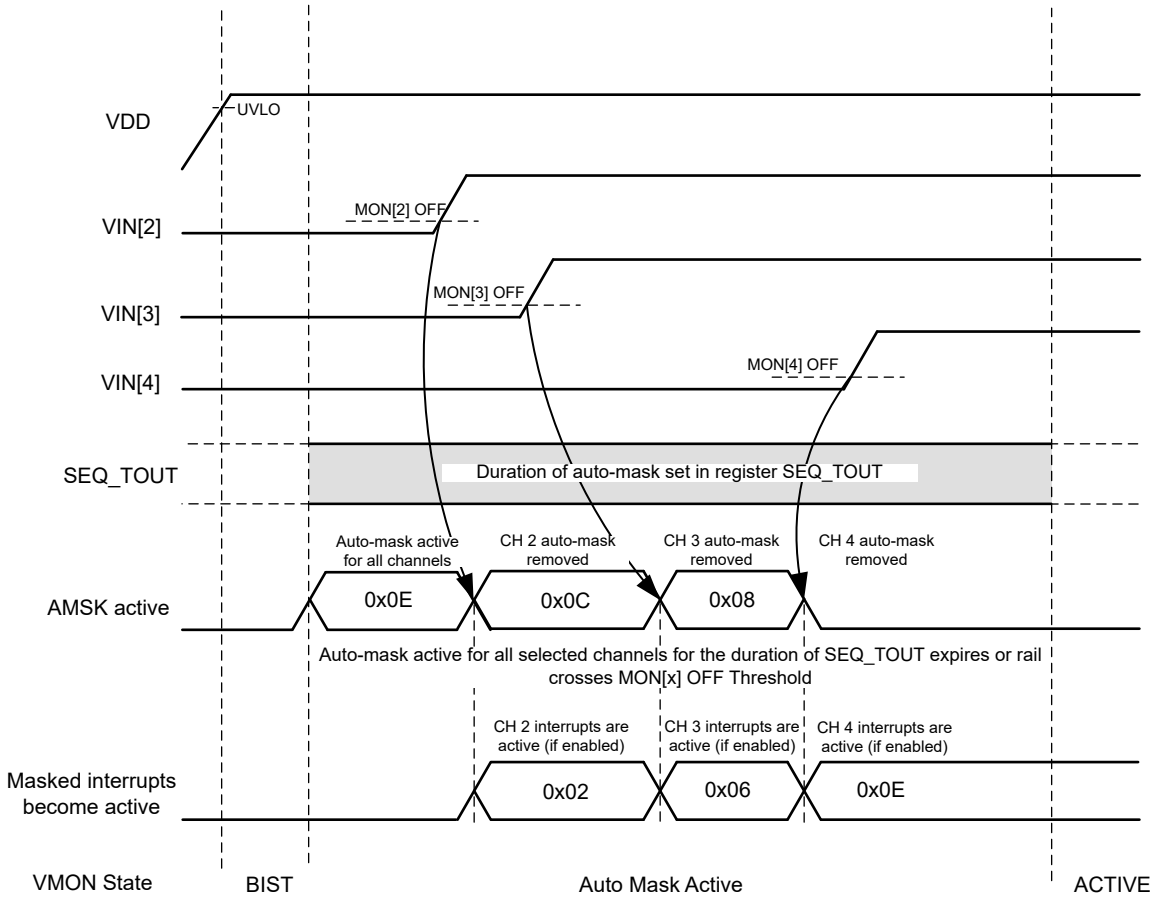

Figure 7-5. Active State Timing Diagram

The TPS388C0x-Q1 takes several actions on power up transition:

1. After VDD has reached UVLO and BIST has completed TPS388C0x-Q1 enters sequence monitoring 1 state where automask is enabled according to the following :

a. All TPS388C0x-Q1 inputs selected with auto-mask register AMSK_ON start with masked (disabled) interrupts for Under-Voltage High Frequency (UVHF) and Over-Voltage High Frequency (OVHF) conditions.
b. As each rail passes the MON's OFF threshold, automatically (and expected to happen within about 5-10 µs) the relevant UV and OV interrupts are unmasked and enabled/disabled according to the IEN_UVHF and IEN_OVHF registers.

2. After SEQ_TOUT timeout:
   a. TPS388C0x-Q1 is in ACTIVE state and starts normal monitoring.

7.4 Feature Description

7.4.1 VDD

The TPS388C0x-Q1 is designed to operate from an input voltage supply range between 2.6V to 5.5V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 1µF capacitor between the VDD pin and the GND pin.

V_{DD} needs to be at or above VDD_{UVLO} for at least the start-up delay (t_{BIST}) for the device to be fully functional.

7.4.2 Maskable Interrupt (AMSK)

In the case of power up, AMSK_ON register applies. AMSK_ON masks interrupts until the MON voltage crosses the MON's OFF threshold or sequence timeout expires, whichever is sooner. In the case of power down AMSK_OFF register applies. AMSK_OFF masks interrupts until the MON voltage is below the OFF threshold .

Table 7-2 summarizes the auto-mask operation for power up and power down.

Table 7-2. Auto-Mask Operation for the Power Up and Power Down

TRANSITION	AUTO-MASK APPLIED	AUTO-MASK APPLIES TO	AUTO-MASK INACTIVE	INTERRUPTS ACTIVE FOR MON CHANNELS NOT IN AUTO-MASK
Power Up	AMSK_ON	IEN_UVHF, IEN_OVHF	SEQ_TOUT expires or rail crosses MON's OFF threshold	At Power Up
Power Down	AMSK_OFF		Auto-mask active in transition until SEQ_TOUT expires	Until SEQ_TOUT expires

7.4.3 MON

The TPS388C0x-Q1 combines two comparators with a precision reference voltage and a trimmed resistor divider per monitor (MON) channel. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Both comparators also include built-in hysteresis that provides noise immunity and stable operation.

Each MON channel can be configured for High Frequency (HF) fault detection. HF fault detection uses a comparator for UV and OV measurements referenced to the threshold voltage. A debounce filter for glitch immunity can be configured for HF faults using the FLT_HF registers in BANK1 associated with each MON channel. HF faults are configured using the UV_HF and OV_HF registers in BANK1. Each MON channel has unique UV_HF and OV_HF registers.

Although not required in most cases, for noisy applications good analog design practice is to place a 1nF to 10nF bypass capacitor at the MON input to reduce sensitivity to transient voltages on the monitored signal. Specific debounce times or deglitch times can also be set independently for each MON via I^2C registers

When monitoring VDD supply voltage, the MON pin can be connected directly to VDD. The outputs NIRQ and NRST are high impedance when voltage at the MON pin is between upper and lower boundary of threshold.

7.4.4 NRST

The NRST pin features a programmable reset delay time that can be adjusted from 0.2ms to 200ms when using TI_CONTROL register. NRST is an open-drain output that must be pulled up through a 1kΩ to 100kΩ pullup resistor. When the device is powered up and POR is complete, NRST is asserted low until the BIST is complete. After the BIST, NRST remains high (not asserted) until triggered by a mappable fault condition. An NRST_MISMATCH fault asserts if the NRST pin is pulled to an unexpected state. For example, if the NRST pin is in a high-impedence state (logic high) and is externally pulled low, then an NRST_MISMATCH fault asserts. During an NRST toggle NRST mismatch is active after 2µs, NRST must exceed 0.6*VDD to be considered in a logic high state.

NRST is mappable to the watchdog fault using the IEN_VENDOR register. If NRST is mapped to the watchdog fault, the NRST pin asserts during a watchdog fault and de-assert following the reset delay (t_D).

NRST is also mappable to the OVHF and UVHF faults using the FC_LF[n] registers. If a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds, then NRST is asserted, driving the NRST pin low. When the monitored voltage comes back into the valid window, a reset delay circuit is enabled that holds NRST low for a specified reset delay period (t_D). Note if NRST is un-mapped from OVHF and UVHF faults while NRST is asserted then NRST de-asserts, NRST re-asserts when re-mapped assuming the voltage is still outside the valid window

The t_D period is determined by the RST_DLY[2:0] value found in the TI_CONTROL register. When the reset delay has elapsed, the NRST pin goes to a high-impedance state and uses a pullup resistor to hold NRST high. The pullup resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To design for proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (VOL), capacitive loading, and leakage current.

7.4.5 NIRQ

NIRQ is a interrupt error ouput with latched behavior, if a monitored voltage falls or rises outside of the programmed OVHF and UVHF thresholds NIRQ is asserted. NIRQ remains in a low state until the action causing the fault is no longer present and a 1-to-clear is written to the bit signaling the fault. Un-mapping NIRQ from a fault reporting register does not de-assert the NIRQ signal. NIRQ is In a typical TPS389C03-Q1 application, the NIRQ output is connected to a reset or enable input of a processor [such as a digital signal processor (DSP) or application-specific integrated circuit (ASIC), or other processor type].

The TPS388C0x-Q1 has an open drain active low output that requires a pull-up resistor to hold these lines high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. To design for proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by V_{OL}, output capacitive loading, and output leakage current. These values are specified in *Section 6*. The open drain output can be connected as a wired-OR logic with other open drain signals such as another TPS388C0x-Q1 NIRQ pin.

7.4.6 I^2C

The TPS388C0x-Q1 device follows the I^2C protocol (up to 1MHz) to manage communication with host devices such as an MCU or System on Chip (SoC). I^2C is a two wire communication protocol implmented using two signals, clock (SCL) and data (SDA). The host device is primary controller of communication. TPS388C0x-Q1 device responds over the data line during read or write operation as defined by I^2C protocol. Both SCL and SDA signals are open drain topology and can be used in a wired-OR configuration with other devices to share the communication bus. Both SCL and SDA pins need an external pull up resistance to supply voltage (10kΩ recommended).

Figure 7-6 shows the timing relationship between SCL and SDA lines to transfer 1 byte of data. SCL line is always controlled by host. To transfer 1 byte data, host needs to send 9 clocks on SCL. 8 clocks for data and 1 clock for ACK or NACK. SDA line is controlled by either host or TPS388C0x-Q1 device based on the read or write operation. Figure 7-7 and Figure 7-8 highlight the communication protocol flow and which device controls SDA line at various instances during active communication.

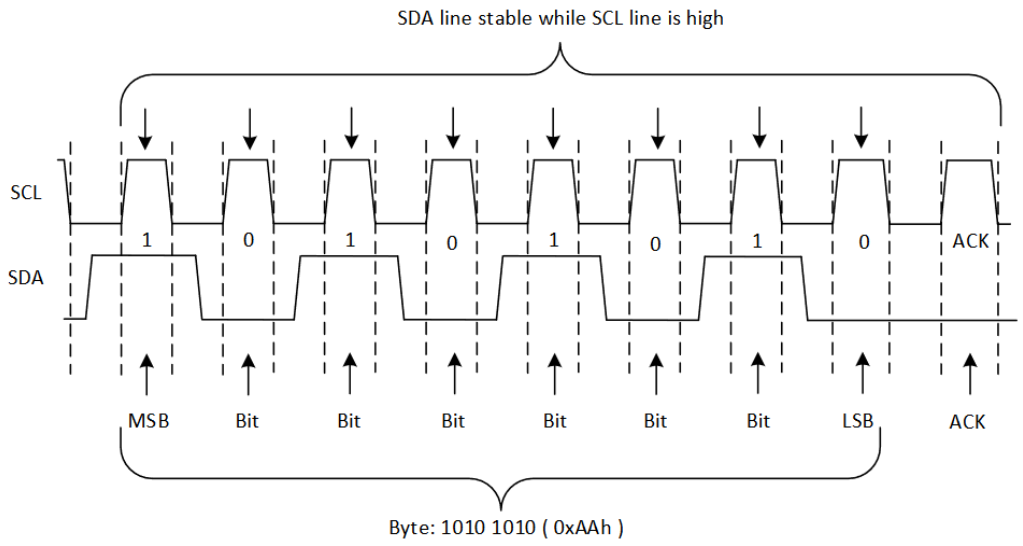

Figure 7-6. SCL to SDA timing for 1 byte data transfer

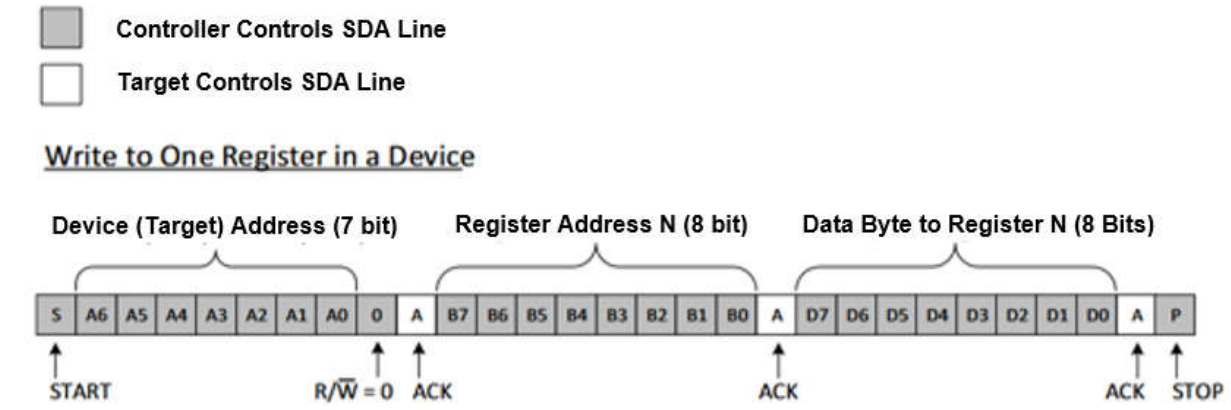

Figure 7-7. I²C write protocol

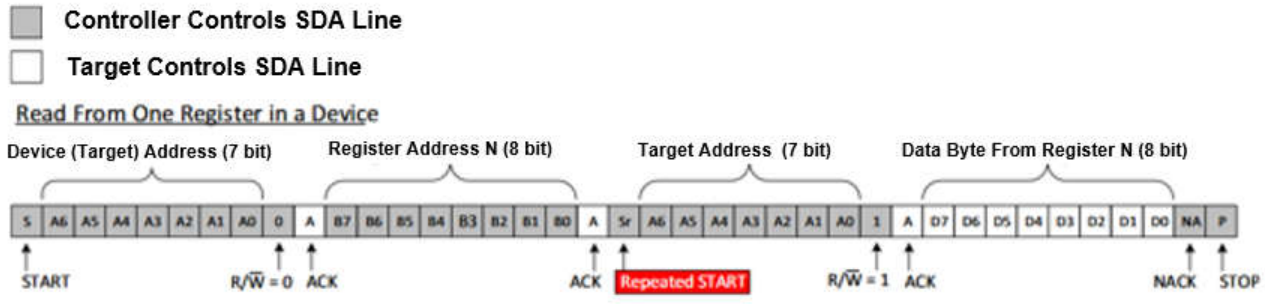

Figure 7-8. I²C read protocol

Before initiating communication over I²C protocol, host needs to confirm the I²C bus is available for communication. Monitor the SCL and SDA lines, if any line is pulled low, the I²C bus is occupied. Host needs to wait until the bus is available for communication. Once the bus is available for communication, the host can

initiate read or write operation by issuing a START condition. Once the I²C communication is complete, release the bus by issuing STOP command. Figure 7-9 shows how to implement START and STOP condition.

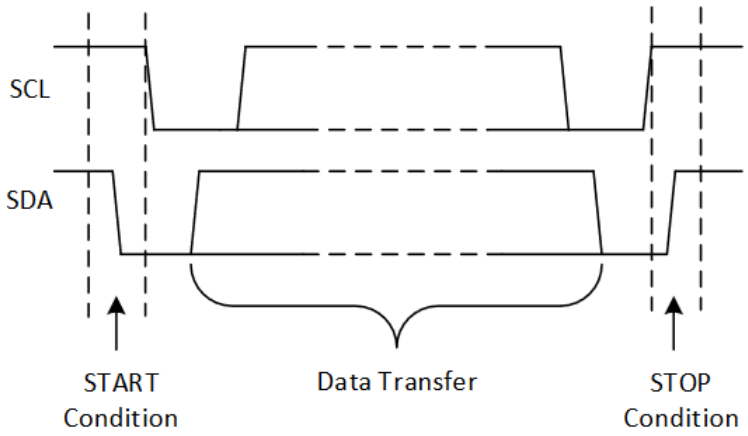

Figure 7-9. I²C START and STOP condition

The SDA line can get stuck in logic low level if required number of clocks are not provided by the host. In this scenario, host can provide multiple clocks on SCL line until the SDA line goes high. After this event, host can issue I²C stop command. This releases the I²C bus and other devices can use the I²C bus.

Table 7-3 shows the different functionality available when programming with I²C.

Table 7-3. User Programmable I²C Functions

FUNCTIONS	DESCRIPTION
Thresholds for OV/UV- HF	Adjustable in 5mV steps from 0.2V to 1.475V and 20mV steps from 0.8V to 5.5V
Voltage Monitoring scaling	1 or 4
Glitch immunity for OV/UV- HF	0.1us to 102.4us
Enable sequence timeout	1ms to 4s
Packet error checking for I²C	Enabling or Disabling
Force NIRQ/NRST/WDO assertion	Controlled by I²C register
Individual channel MON	Enable or Disable
Interrupt disable functions	BIST, PEC, TSD, CRC
Reset Delay	200us to 200ms
MAX Violation Count	0 to 7
Watchdog Startup Delay Multiplier	0 to 7
Watchdog Open and Close Window Times	1ms to 864ms
Watchdog Output Delay	200 us to 200ms (only applicable for non-latched WDO)
OV/UV/WDT	Mappable individually to NIRQ, NRST, and WDO

7.4.7 Packet Error Checking (PEC)

TPS388C0x-Q1 supports Packet Error Checking (PEC) as a way to implement Cyclic Redundancy Checking (CRC). PEC is a dynamic CRC that happens only during read or write transactions if enabled. With the initial value of CRC set to 0x00, the PEC uses a CRC-8 represented by the polynomial:

$$C(x) = x^8 + x^2 + x + 1 \quad (1)$$

The polynomial is meant to catch any bit flips or noise in I²C communication which cause data and PEC byte to have a mismatch. The PEC calculation includes all bytes in the transmission, including address, command and data. The PEC calculation does not include ACK or NACK bits or START, STOP or REPEATED

START conditions. If PEC is enabled, and the TPS388C0x-Q1 is transmitting data, then the TPS388C0x-Q1 is responsible for sending the PEC byte. If PEC is enabled, and the TPS388C0x-Q1 is reveiving data from the MCU, then the MCU is responsible for sending the PEC byte. In case of faster communications needs like servicing the watchdog the required PEC feature can be effectively used to handle missing PEC information and to avoid triggering faults. Figure 7-10 and Figure 7-11 highlight the communication protocol flow when PEC is required and which device controls SDA line at various instances during active communication.

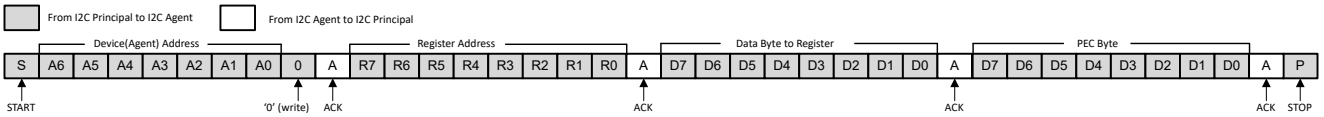

Figure 7-10. Single Byte Write with PEC

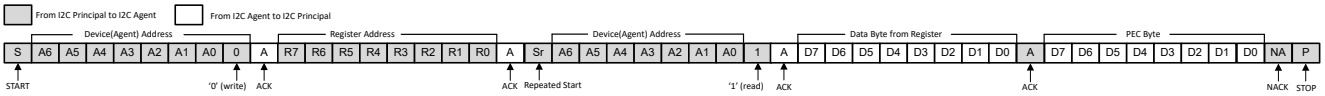

Figure 7-11. Single Byte Read with PEC

Table 7-4 summarises the registers associated with a PEC Write command and resulting device behavior. Table 7-5 summarises the registers associated with a PEC Read command and resulting device behavior.

Table 7-4. PEC Write Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	x	x	PEC byte is not required in write operation, NO NIRQ assertion.
1	0	x	A write command missing a PEC byte is treated as OK, the write command executes and result in a I^{2}C ACK. A write command with an incorrect PEC is treated as an error, the write command does not execute and result in a I^{2}C NACK. NO NIRQ assertion.
1	1	0	A missing PEC is treated as an error, a write command only executes if the correct PEC byte is provided. I^{2}C communication still responds with an ACK although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and result in a I^{2}C NACK. NO NIRQ assertion.
1	1	1	A missing PEC is treated as an error, a write command only executes if the correct PEC byte is provided. I^{2}C communication still responds with an ACK although write command did not execute. A write command with an incorrect PEC is treated as an error, the write command does not execute and results in a I^{2}C NACK. NIRQ is asserted when a write command with a incorrect or missing PEC byte is attempted.

Table 7-5. PEC Read Summary

EN_PEC	REQ_PEC	PEC_INT	Interrupt Status
0	x	x	I^{2}C read operation reponds with data stored in register, I^{2}C read command does not respond with registers corresponding PEC byte.
1	x	x	I^{2}C read operation reponds with data stored in register and corresponding PEC byte.

7.4.8 Window Watchdog

The TPS388C0x-Q1 features the ability to enable and disable the watchdog timer with a WDE pin. This feature allows the user to start with the watchdog timer disabled and then enable the watchdog timer using the WDE pin. The ability to enable and disable the watchdog is useful to avoid undesired watchdog faults during initialization and shutdown. When the WDE pin is low to disable the watchdog timer, changes on the pin is responded to immediately. When the watchdog goes from disabled to enabled, there is a startup delay and close and open window sequence.

7.4.9 Window Watchdog Timer

This section provides information for the window watchdog modes of operation. A window watchdog is typically employed in safety critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog, there is a maximum time in which a pulse must be issued to prevent the reset from occurring. However, in a window watchdog the pulse must be issued in the open window. Figure 7-12 shows the valid region for a WDI pulse to be issued to prevent the WDO from being triggered and being pulled low.

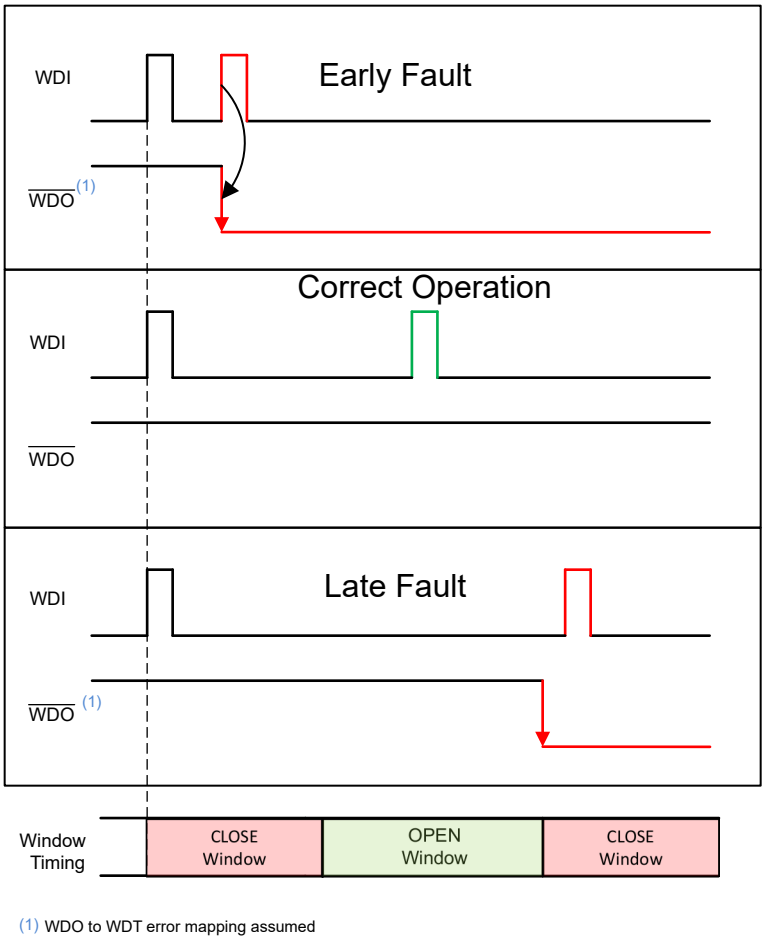

Figure 7-12. Window Watchdog Valid Window

When WDE goes from low to high, the watchdog begins operation in a startup window. There must be a WDI pulse in the startup window before the window expires otherwise it's a bad event. A valid WDI pulse is a positive going pulse with a pulse width of at least 32us. The start up delay is defined by the open and close windows and the WDT_Start_DLY_Multiplier[2:0] register value according to Equation 2.

In Equation 2 WDT_Startup_DLY_MULTIPLIER [2:0], OPEN[7:0], and CLOSE[7:0] are assumed to be used in a decimal format.

$$WD\_StartUp\_DLY = (WDT\_Startup\_DLY\_MULTIPLIER[2:0] + 1)*(CLOSE[7:0] + OPEN[7:0]) \quad (2)$$

Once receiving a pulse in the startup window the watchdog immediately moves to the close window. After the fixed time duration for the close window (set in I^2C register 0xAB in Bank 1), the watchdog moves to the open window. During the open window a valid WDI pulse must be present to avoid a bad event. If a valid pulse is registered in the open window then the closed window starts immediately. The open window is considered dynamic and the windows duration is determined when the WDI pulse is seen. During proper operation the

watchdog cycles between open window and close window as seen in Figure 7-13.TPS388C0x-Q1 offers a Open and Close window delay accuracy of ±5%

Figure 7-13 demonstrates the WD behavior during proper operation. Note a valid pulse is present in each open window and the open window duration is determined by when the WDI pulse is seen. The closed window then follows immediately after the rising edge of the WDI pulse, this cycle continues so long as a valid pulse is registerd in the open window.

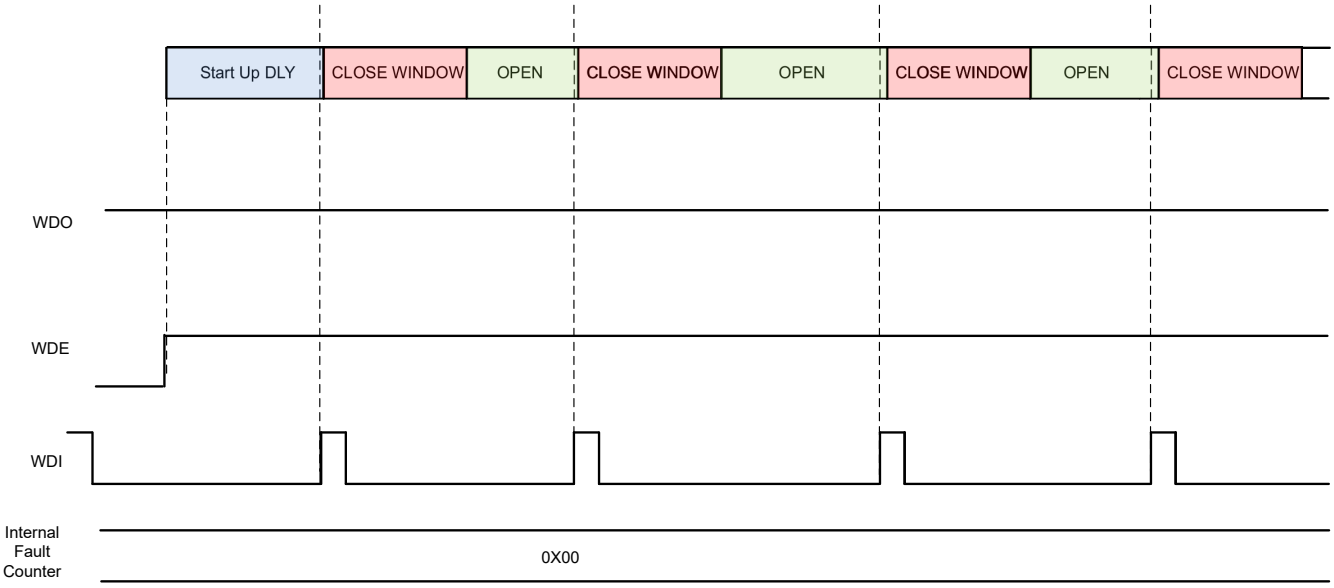

Figure 7-13. WD No Fault

If a valid pulse is not registered during the open window TPS388C0x-Q1 logs a bad event (after open window timeout) and the close window repeats. After a bad event TPS388C0x-Q1 logs the fault in a violation counter, the total violation count is then compared to register MAX_Violation_COUNT[2:0]. Register MAX_Violation_COUNT[2:0] represents the max number of faults allowed to transpire before WDO (and any mapped error output) is asserted, the register can be set from 1 to 7 faults. If set to 1 the first fault event triggers WDO, if set to 3 then 3 faults must transpire for the WDO (and any mapped error output) to assert as seen in Figure 7-14. Both NIRQ and NRST error outputs can be mapped to report a watchdog fault through the use of register IEN_VENDOR. Note a good event decrements the violation count if the violation count is not already equal to zero.

Figure 7-14 demonstrates the watchdog behavior when MAX_Violation_COUNT[2:0] is set to three. In this figure both NRST and NRST are mapped to report a watchdog fault and WDO is program to reflect timeout functionality. Note the open window duration is determined by when the WDI pulse is seen, the full duration of the open window is only seen when no WDI pulse is present and the window has timed out. Simarly the duration of the startup window is determined by when the first WDI pulse is seen. The full duration of the start up window is only seen when no WDI pulse is present and the window has timed out, a timeout of the start up window is considered a bad event.

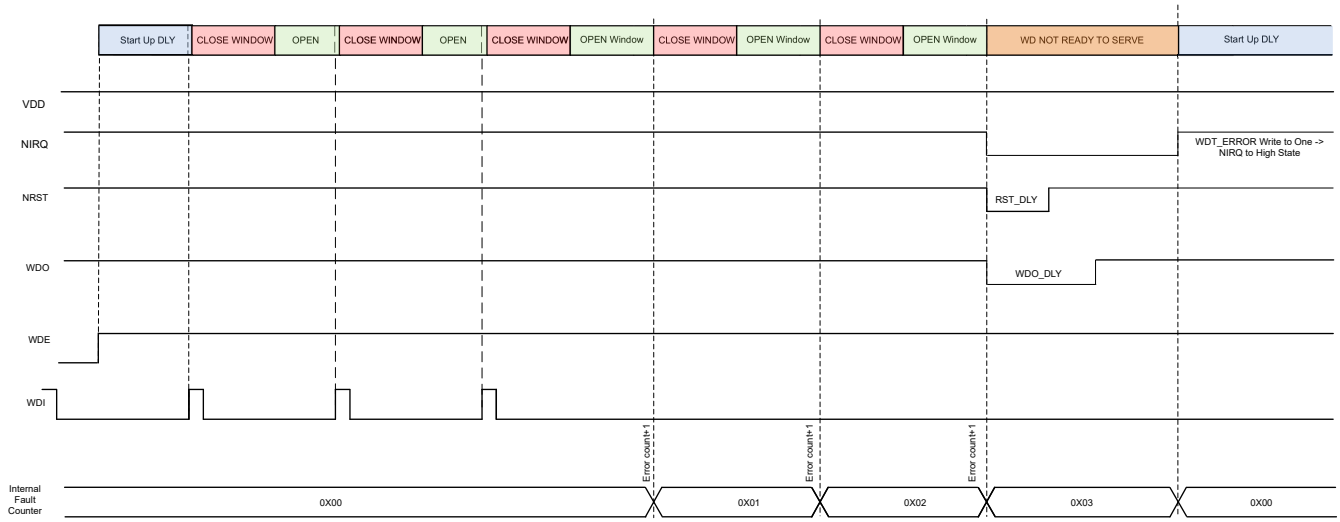

Figure 7-14. WD Fault WDO TimeOut and NRST NIRQ Mapping

7.5 Register Maps

7.5.1 Registers Overview

The register map is designed to support up to 16 channels through register banks, with the following organization:

- Bank 0 - Status Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Interrupt registers
  - Status registers
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)
- Bank 1 - Channel 2-7 Configuration Register Set Summary:
  - Vendor info and usage registers (bank independent)
  - Control registers (device global registers)
  - Monitor configuration registers (channel specific registers)
  - Sequence configuration registers (both device global and channel specific registers)
  - Bank selection register (bank independent)
  - Protection registers (bank independent)
  - Device configuration registers (bank independent)

Bank independent registers are accessible at the same address irrespective of the current bank selection. Access to other registers requires the proper bank being selected.

All registers are 8-bit wide, and are loaded at boot with the default value described here or with the OTP value programmed at the factory.OTP values are denoted by X and these values depends on the configuration for the orderable.

Unused registers addresses are reserved for future use and support up to 16 channels.

Write accesses to protected registers (see PROT1/2 details), invalid registers, or valid registers with invalid data is NACK'd.

7.5.1.1 BANK0 Registers

Table 7-6 lists the memory-mapped registers for the BANK0 registers. All register offset addresses not listed in Table 7-6 should be considered as reserved locations and the register contents should not be modified.

Table 7-6. BANK0 Registers

Address	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	INT_SRC	F_OTHER	RSVD				TEST	CONTROL	MONITOR
0x11	INT_MONITOR	OVHF						RSVD	UVHF
0x12	INT_UVHF	F_UVHF[7]		F_UVHF[6]	F_UVHF[5]	F_UVHF[4]	F_UVHF[3]	F_UVHF[2]	RSVD
0x16	INT_OVHF	F_OVHF[7]		F_OVHF[6]	F_OVHF[5]	F_OVHF[4]	F_OVHF[3]	F_OVHF[2]	RSVD
0x22	INT_CONTROL	F_CRC				F_NIRQ	F_TSD	RSVD	F_PEC
0x23	INT_TEST	RSVD				ECC_SEC	ECC_DED	BIST_Complete_INT	BIST_Fail_INT
0x24	INT_VENDOR	Self-Test_CRC	LDO_OV_Error	NRST_MISMATCH	Freq_DEV_Error	SHORT_DET	OPEN_DET	RSVD	WDT_ERROR
0x30	VMON_STAT	FAILSAFE	ST_BIST_C	ST_VDD	ST_NIRQ	ACTIVE		RSVD	
0x31	TEST_INFO	RSVD		ECC_SEC	ECC_DED	BIST_VM	BIST_NVM	BIST_L	BIST_A
0x32	OFF_STAT	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xF0	BANK_SEL	RSVD							BANK_Select
0xF1	PROT1	WRKC			RSVD	CFG	IEN	MON	SEQ
0xF2	PROT2	WRKC			RSVD	CFG	IEN	MON	SEQ
0xF3	PROT_MON	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xF9	I2C ADDR	RSVD	ADDR_NVM[3:0]				ADDR_STRAP[2:0]		

Complex bit access types are encoded to fit into small table cells. Table 7-7 shows the codes that are used for access types in this section.

Table 7-7. BANK0 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.1.1 INT_SRC Register (Address = 0x10) [Reset = 0x00]

INT_SRC is shown in Table 7-8.

Return to the Summary Table.

Global Interrupt Source Status register.

Table 7-8. INT_SRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	F_OTHER	R	0b	Vendor internal defined faults. Details reported in INT_Vendor. Represents ORed value of all bits in INT_Vendor. 0 = No Vendor defined faults detected 1 = Vendor defined faults detected
6:3	RSVD	R	0000b	RSVD
2	TEST	R	0b	Internal test or configuration load fault. Details reported in INT_TEST. Represents ORed value of all bits in INT_TEST. 0 = No test/configuration fault detected 1 = Test/configuration fault detected
1	CONTROL	R	0b	Control status or communication fault. Details reported in INT_CONTROL. Represents ORed value of all bits in INT_CONTROL. 0 = No status or communication fault detected 1 = Status or communication fault detected
0	MONITOR	R	0b	Voltage monitor fault. Details reported in INT_MONITOR. Represents ORed value of all bits in INT_MONITOR. 0 = No voltage fault detected 1 = Voltage fault detected

7.5.1.1.2 INT_MONITOR Register (Address = 0x11) [Reset = 0x00]

INT_MONITOR is shown in Table 7-9.

Return to the Summary Table.

Voltage Monitor Interrupt Status register.

Table 7-9. INT_MONITOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RSVD	R	00000b	RSVD
2	OVHF	R	0b	Over-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_OVHF. Represents ORed value of all bits in INT_OVHF. 0 = No OVHF fault detected 1 = OVHF fault detected
1	RSVD	R	0b	RSVD
0	UVHF	R	0b	Under-Voltage High Frequency Fault reported by comparator based monitoring. Details reported in INT_UVHF. Represents ORed value of all bits in INT_UVHF. 0 = No UVHF fault detected 1 = UVHF fault detected

7.5.1.1.3 INT_UVHF Register (Address = 0x12) [Reset = 0x00]

INT_UVHF is shown in Table 7-10.

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High Frequency channel Under-Voltage Interrupt Status register.

Table 7-10. INT_UVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD

Table 7-10. INT_UVHF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	F_UVHF[7]	R/W1C	0b	Under-Voltage High Frequency Fault for MON7. Trips if MON7 High Frequency signal goes below UVHF[7]. 0 = MON7 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON7 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON7 High Frequency signal is above UVHF[7]).
5	F_UVHF[6]	R/W1C	0b	Under-Voltage High Frequency Fault for MON6. Trips if MON6 High Frequency signal goes below UVHF[6]. 0 = MON6 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON6 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON6 High Frequency signal is above UVHF[6]).
4	F_UVHF[5]	R/W1C	0b	Under-Voltage High Frequency Fault for MON5. Trips if MON5 High Frequency signal goes below UVHF[5]. 0 = MON5 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON5 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON5 High Frequency signal is above UVHF[5]).
3	F_UVHF[4]	R/W1C	0b	Under-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes below UVHF[4]. 0 = MON4 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON4 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON4 High Frequency signal is above UVHF[4]).
2	F_UVHF[3]	R/W1C	0b	Under-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes below UVHF[3]. 0 = MON3 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON3 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON3 High Frequency signal is above UVHF[3]).
1	F_UVHF[2]	R/W1C	0b	Under-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes below UVHF[2]. 0 = MON2 has no UVHF fault detected (or interrupt disabled in IEN_UVHF register) 1 = MON2 has UVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the UVHF fault condition is also removed (MON2 High Frequency signal is above UVHF[2]).
0	RSVD	R	0b	RSVD

7.5.1.1.4 INT_OVHF Register (Address = 0x16) [Reset = 0x00]

INT_OVHF is shown in Table 7-11.

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High Frequency channel Over-Voltage Interrupt Status register

Table 7-11. INT_OVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD
6	F_OVHF[7]	R/W1C	0b	Over-Voltage High Frequency Fault for MON7. Trips if MON7 High Frequency signal goes above OVHF[7]. 0 = MON7 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON7 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON7 High Frequency signal is below OVHF[7])
5	F_OVHF[6]	R/W1C	0b	Over-Voltage High Frequency Fault for MON6. Trips if MON6 High Frequency signal goes above OVHF[6]. 0 = MON6 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON6 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON6 High Frequency signal is below OVHF[6])
4	F_OVHF[5]	R/W1C	0b	Over-Voltage High Frequency Fault for MON5. Trips if MON5 High Frequency signal goes above OVHF[5]. 0 = MON5 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON5 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON5 High Frequency signal is below OVHF[5])
3	F_OVHF[4]	R/W1C	0b	Over-Voltage High Frequency Fault for MON4. Trips if MON4 High Frequency signal goes above OVHF[4]. 0 = MON4 has noOVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON4 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON4 High Frequency signal is below OVHF[4])
2	F_OVHF[3]	R/W1C	0b	Over-Voltage High Frequency Fault for MON3. Trips if MON3 High Frequency signal goes above OVHF[3]. 0 = MON3 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON3 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON3 High Frequency signal is below OVHF[3])
1	F_OVHF[2]	R/W1C	0b	Over-Voltage High Frequency Fault for MON2. Trips if MON2 High Frequency signal goes above OVHF[2]. 0 = MON2 has no OVHF fault detected (or interrupt disabled in IEN_OVHF register) 1 = MON2 has OVHF fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the OVHF fault condition is also removed (MON2 High Frequency signal is below OVHF[2])
0	RSVD	R	0b	RSVD

7.5.1.1.5 INT_CONTROL Register (Address = 0x22) [Reset = 0x00]

INT_CONTROL is shown in Table 7-12.

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Control and Communication Interrupt Status register.

Table 7-12. INT_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R	000b	RSVD
4	F_CRC	R/W1C	0b	Runtime register CRC Fault: 0 = No fault detected (or IEN_CONTROL.RT_CRC is disabled) 1 = Register CRC fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. The bit is set again during next register CRC check if the same fault is detected
3	F_NIRQ	R/W1C	0b	Interrupt pin fault (fault bit always enabled no enable bit available): 0 = No fault detected on NIRQ pin 1 = Low resistance path to supply detected on NIRQ pin The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the NIRQ fault condition is also removed.
2	F_TSD	R/W1C	0b	Thermal Shutdown fault: 0 = No TSD fault detected (or IEN_CONTROL.TSD is disabled) 1 = TSD fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the TSD fault condition is also removed
1	RSVD	R	0b	RSVD
0	F_PEC	R/W1C	0b	Packet Error Checking fault: 0 = PEC mismatch has not occurred (or IEN_CONTROL.PEC is disabled) 1 = PEC mismatch has occurred, or VMON_MISC.REQ_PEC=1 and PEC is missing in a write transaction The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit. The bit is set again during next I2C transaction if the same fault is detected.

7.5.1.1.6 INT_TEST Register (Address = 0x23) [Reset = 0x00]

INT_TEST is shown in Table 7-13.

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Internal Test and Configuration Load Interrupt Status register.

Table 7-13. INT_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RSVD	R	0000b	RSVD
3	ECC_SEC	R/W1C	0b	ECC single-error corrected on OTP configuration load: 0 = No single-error corrected (or IEN_TEST.ECC_SEC is disabled) 1 = Single-error corrected Write-1-to-clear clears the bit. The bit is set again during next OTP configuration load if the same fault is detected.

Table 7-13. INT_TEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	ECC_DED	R/W1C	0b	ECC double-error detected on OTP configuration load: 0 = No double-error detected on OTP load 1 = Double-error detected on OTP load The fault bit is always enabled (there is no associated interrupt enable bit). The device moves to failsafe mode on double error detection.
1	BIST_Complete_INT	R/W1C	0b	Indication of Built-In Self-Test complete: 0 = BIST not complete (or IEN_TEST.BIST_C is disabled) 1 = BIST complete Write-1-to-clear clears the bit. The bit is set again on completion of next BIST execution
0	BIST_Fail_INT	R/W1C	0b	Built-In Self-Test fault: 0 = No BIST fault detected (or IEN_TEST.BIST is disabled) 1 = BIST fault detected Write-1-to-clear clears the bit. The bit is set again during next BIST execution if the fault is detected

7.5.1.1.7 INT_VENDOR Register (Address = 0x24) [Reset = 0x00]

INT_VENDOR is shown in Table 7-14.

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Vendor Specific Internal Interrupt Status register.

Table 7-14. INT_VENDOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Self-Test_CRC	R/W1C	0b	Startup register CRC self-test. 0 = Self-test Pass 1 = Self-test Fail Write-1-to-clear to clear the fault
6	LDO_OV_Error	R/W1C	0b	Internal LDO Overvoltage error. 0 = No internal LDO overvoltage fault detected 1 = Internal LDO overvoltage fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the LDO fault condition is also removed.
5	NRST_MISMATCH	R/W1C	0b	Designates error due to drive state and read back. During an NRST toggle NRST mismatch is active after 2µs, NRST must exceed 0.6*VDD to be considered in a logic high state. 0 = No fault detected on NRST pin 1 = Error due to drive state and read back. The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the NRST fault condition is also removed.
4	Freq_DEV_Error	R/W1C	0b	Designates internal frequency errors. 0 = No internal frequency fault detected 1 = Internal frequency fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the frequency fault condition is also removed.
3	SHORT_DET	R/W1C	0b	Address pin short detect. 0 = No internal address pin short fault detected 1 = Internal address pin short fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the internal address pin short fault condition is also removed.

Table 7-14. INT_VENDOR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	OPEN_DET	R/W1C	0b	Address pin open detect. 0 = No internal address pin open fault detected 1 = Internal address pin open fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the internal address pin open fault condition is also removed.
1	RSVD	R	0b	RSVD
0	WDT_ERROR	R/W1C	0b	Indication of Watchdog fault. 0 = No internal Watchdog fault detected 1 = Internal Watchdog fault detected The recovery of the fault condition does NOT clear the bit. The fault can only be cleared by the host with a write-1-to-clear. Write-1-to-clear clears the bit only if the internal Watchdog fault condition is also removed.

7.5.1.1.8 VMON_STAT Register (Address = 0x30) [Reset = 0x00]

VMON_STAT is shown in Table 7-15.

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Status flags for internal operations and other non critical conditions.

Table 7-15. VMON_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FAILSAFE	R	0b	1 = Device in FAILSAFE state
6	ST_BIST_C	R	0b	Built-In Self-Test state: 0 = BIST not complete 1 = BIST complete
5	ST_VDD	R	0b	Status VDD
4	ST_NIRQ	R	0b	Status NIRQ pin
3	RSVD	R	0b	RSVD
2	ACTIVE	R	0b	1 = Device in ACTIVE state
1	RSVD	R	0b	RSVD
0	RSVD	R	0b	RSVD

7.5.1.1.9 TEST_INFO Register (Address = 0x31) [Reset = 0x00]

TEST_INFO is shown in Table 7-16.

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Internal Self-Test and ECC information.

Table 7-16. TEST_INFO Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RSVD	R	00b	RSVD
5	ECC_SEC	R	0b	Status of ECC single-error correction on OTP configuration load. 0 = no error correction applied 1 = single-error correction applied
4	ECC_DED	R	0b	Status of ECC double-error detection on OTP configuration load. 0 = no double-error detected 1 = double-error detected

Table 7-16. TEST_INFO Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	BIST_VM	R	0b	Status of Volatile Memory test output from BIST. 0 = Volatile Memory test pass 1 = Volatile Memory test fail
2	BIST_NVM	R	0b	Status of Non-Volatile Memory test output from BIST. 0 = Non-Volatile Memory test pass 1 = Non-Volatile Memory test fail
1	BIST_L	R	0b	Status of Logic test output from BIST. 0 = Logic test pass 1 = Logic test fail
0	BIST_A	R	0b	Status of Analog test output from BIST. 0 = Analog test pass 1 = Analog test fail

7.5.1.1.10 OFF_STAT Register (Address = 0x32) [Reset = 0x00]

OFF_STAT is shown in Table 7-17.

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Channel OFF status.

Table 7-17. OFF_STAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD
6	MON[7]	R	0b	Represents the OFF status of each channel: 0 = channel 7 is NOT OFF 1 = channel 7 is OFF (below OFF threshold)
5	MON[6]	R	0b	Represents the OFF status of each channel: 0 = channel 6 is NOT OFF 1 = channel 6 is OFF (below OFF threshold)
4	MON[5]	R	0b	Represents the OFF status of each channel: 0 = channel 5 is NOT OFF 1 = channel 5 is OFF (below OFF threshold)
3	MON[4]	R	0b	Represents the OFF status of each channel: 0 = channel 4 is NOT OFF 1 = channel 4 is OFF (below OFF threshold)
2	MON[3]	R	0b	Represents the OFF status of each channel: 0 = channel 3 is NOT OFF 1 = channel 3 is OFF (below OFF threshold)
1	MON[2]	R	0b	Represents the OFF status of each channel: 0 = channel 2 is NOT OFF 1 = channel 2 is OFF (below OFF threshold)
0	RSVD	R	0b	RSVD

7.5.1.1.11 BANK_SEL Register (Address = 0xF0) [Reset = 0x00]

BANK_SEL is shown in Table 7-18.

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Bank Select.

Table 7-18. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RSVD	R/W	0000000b	RSVD

Table 7-18. BANK_SEL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BANK_Select	R/W	0b	Represents bank selection. 0 = Bank 0 1 = Bank 1

7.5.1.1.12 PROT1 Register (Address = 0xF1) [Reset = 0x00]

PROT1 is shown in Table 7-19.

Return to the Summary Table.

Protection selection registers. To write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, it cannot be cleared to 0 by the host. It can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON_CTL.RESET BIST executed on exiting Sequence 2 (if TEST_CFG.AT_SHDN=1).

Table 7-19. PROT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RSVD	R	00b	RSVD
5	WRKC	R/W	0b	Represents Protection from writes for WRKC group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
4	RSVD	R	0b	RSVD
3	CFG	R/W	0b	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
2	IEN	R/W	0b	Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
1	MON	R/W	0b	Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
0	SEQ	R/W	0b	Represents Protection from writes for SEQ group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible

7.5.1.1.13 PROT2 Register (Address = 0xF2) [Reset = 0x00]

PROT2 is shown in Table 7-20.

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Protection selection registers. To write-protect a register group, the host must set the relevant bit in both registers. For security, registers PROT1 and PROT2 need to have POR value = 0x00 and become read-only once set until power cycle. Once set to 1, it cannot be cleared to 0 by the host. It can be cleared (and allow writing different VMON registers configurations) through: A power cycle A reset through VMON_CTL.RESET BIST executed on exiting Sequence 2 (if TEST_CFG.AT_SHDN=1).

Table 7-20. PROT2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RSVD	R	00b	RSVD

Table 7-20. PROT2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	WRKC	R/W	0b	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
4	RSVD	R	0b	RSVD
3	CFG	R/W	0b	Represents Protection from writes for CFG group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
2	IEN	R/W	0b	Represents Protection from writes for IEN group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
1	MON	R/W	0b	Represents Protection from writes for MON group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible
0	SEQ	R/W	0b	Represents Protection from writes for SEQ group. Both PROT1 and PROT2 need to be set for protection. 0 = Changes to register are possible 1 = Changes to register are not possible

7.5.1.1.14 PROT_MON Register (Address = 0xF3) [Reset = 0x00]

PROT_MON is shown in Table 7-21.

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Locks MON registers in tandem with PROT1 and PROT2.

Table 7-21. PROT_MON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD
6	MON[7]	R/W	0b	Protects MON7 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
5	MON[6]	R/W	0b	Protects MON6 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
4	MON[5]	R/W	0b	Protects MON5 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
3	MON[4]	R/W	0b	Protects MON4 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
2	MON[3]	R/W	0b	Protects MON3 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
1	MON[2]	R/W	0b	Protects MON2 from writes along with PROT1 and PROT2. 0= Changes are possible 1= Changes are not possible
0	RSVD	R	0b	RSVD

7.5.1.1.15 I2C ADDR Register (Address = 0xF9) [Reset = 0x00]

I2C ADDR is shown in Table 7-22.

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I2C Address

Table 7-22. I2C ADDR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	0b	RSVD
6:3	ADDR_NVM[3:0]	R	0000b	HASH(0x555fa8296158)
2:0	ADDR_STRAP[2:0]	R	000b	HASH(0x555fa82b52e8)

7.5.1.2 BANK1 Registers

Table 7-23 lists the memory-mapped registers for the BANK1 registers. All register offset addresses not listed in Table 7-23 should be considered as reserved locations and the register contents should not be modified.

Table 7-23. BANK1 Registers

Address	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x10	VMON_CTL	FORCE_WDO_LOW				RESET_PROT	RSVD		FORCE_NIRQ_LOW
0x11	VMON_MISC	WDO_DLY[2:0]				RSVD		REQ_PEC	EN_PEC
0x12	TEST_CFG	RSVD					AT_SHDN	AT_POR[1]	AT_POR[0]
0x13	IEN_UVHF	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0x15	IEN_OVHF	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0x1B	IEN_CONTROL	RT_CRC_Int				TSD_INT		RSVD	PEC_INT
0x1C	IEN_TEST	ECC_SEC					RSVD	BIST_Complete_INT	BIST_Fail_INT
0x1D	IEN_VENDOR	Startup Self-Test_CRC	RESERVED	NRST_MISMATCH	RESERVED		WDT_TO_NIRQ	RSVD	WDT_TO_NRST
0x1E	MON_CH_EN	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0x1F	VRANGE_MULT	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0x30	UV_HF[2]	THRESHOLD[7:0]							
0x31	OV_HF[2]	THRESHOLD[7:0]							
0x34	FLT_HF[2]	OV_DEB[3:0]				UV_DEB[3:0]			
0x35	FC_LF[2]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		
0x40	UV_HF[3]	THRESHOLD[7:0]							
0x41	OV_HF[3]	THRESHOLD[7:0]							
0x44	FLT_HF[3]	OV_DEB[3:0]				UV_DEB[3:0]			
0x45	FC_LF[3]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		
0x50	UV_HF[4]	THRESHOLD[7:0]							
0x51	OV_HF[4]	THRESHOLD[7:0]							
0x54	FLT_HF[4]	OV_DEB[3:0]				UV_DEB[3:0]			
0x55	FC_LF[4]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		
0x60	UV_HF[5]	THRESHOLD[7:0]							
0x61	OV_HF[5]	THRESHOLD[7:0]							
0x64	FLT_HF[5]	OV_DEB[3:0]				UV_DEB[3:0]			
0x65	FC_LF[5]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		
0x70	UV_HF[6]	THRESHOLD[7:0]							
0x71	OV_HF[6]	THRESHOLD[7:0]							
0x74	FLT_HF[6]	OV_DEB[3:0]				UV_DEB[3:0]			
0x75	FC_LF[6]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		
0x80	UV_HF[7]	THRESHOLD[7:0]							
0x81	OV_HF[7]	THRESHOLD[7:0]							
0x84	FLT_HF[7]	OV_DEB[3:0]				UV_DEB[3:0]			
0x85	FC_LF[7]	OVHF_TO_NRST				UVHF_TO_NRST	RSVD		

Table 7-23. BANK1 Registers (continued)

Address	Acronym	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9F	TI_CONTROL	ENTER_BIST	WDT_EN	I2C_MR	RSVD		RST_DLY[2:0]		
0xA1	AMSK_ON	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xA2	AMSK_OFF	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xA5	SEQ_TOUT_MSB	MILLISEC[15:8]							
0xA6	SEQ_TOUT_LSB	MILLISEC[7:0]							
0xA8	SEQ_UP_THLD	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xA9	SEQ_DN_THLD	MON[7]		MON[6]	MON[5]	MON[4]	MON[3]	MON[2]	RSVD
0xAA	WDT_CFG	MAX_VIOLATION_COUNT				RSVD	WDT_Startup_DLY_MULTIPLIER[2:0]		
0xAB	WDT_CLOSE	CLOSE[7:0]							
0xAC	WDT_OPEN	OPEN[7:0]							
0xF0	BANK_SEL	RSVD							BANK_Select

Complex bit access types are encoded to fit into small table cells. Table 7-24 shows the codes that are used for access types in this section.

Table 7-24. BANK1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.5.1.2.1 VMON_CTL Register (Address = 0x10) [Reset = 0x00]

VMON_CTL is shown in Table 7-25.

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VMON device control register.

Table 7-25. VMON_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	FORCE_WDO_LOW	R/W	0b	Write 1 to force assertion of WDO
3	RESET_PROT	R/W	0b	Write 1 to clear Protection registers
2:1	RSVD	R/W	00b	RSVD
0	FORCE_NIRQ_LOW	R/W	0b	Write 1 to force assertion of NIRQ

7.5.1.2.2 VMON_MISC Register (Address = 0x11) [Reset = 0xXX]

VMON_MISC is shown in Table 7-26.

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Miscellaneous VMON configurations.

Table 7-26. VMON_MISC Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6:4	WDO_DLY[2:0]	R/W	xxxb	WDO_Delay (not applicable for latched WDO) 000 = 1ms 001 = 2ms 010 = 5ms 011 = 10ms 100 = 20ms 101 = 50ms 110 = 100ms 111 = 200ms
3:2	RSVD	R/W	00b	RSVD
1	REQ_PEC	R/W	xb	Require PEC. 0 = PEC not required 1 = PEC required
0	EN_PEC	R/W	xb	Enable PEC. 0 = PEC not enabled 1 = PEC enabled

7.5.1.2.3 TEST_CFG Register (Address = 0x12) [Reset = 0x0X]

TEST_CFG is shown in Table 7-27.

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Built-In Self Test (BIST) execution configuration.

Table 7-27. TEST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RSVD	R/W	00000b	RSVD
2	AT_SHDN	R/W	xb	Run BIST at SHDN, 0 = Disable, 1 = Enable
1	AT_POR[1]	R/W	xb	Run BIST at POR, 2nd bit for redundancy, 0 = Disable, 1 = Enable
0	AT_POR[0]	R/W	xb	Run BIST at POR, 0 = Disable, 1 = Enable

7.5.1.2.4 IEN_UVHF Register (Address = 0x13) [Reset = 0xXX]

IEN_UVHF is shown in Table 7-28.

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High Frequency channel Under-Voltage Interrupt Enable register

Table 7-28. IEN_UVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	UVHF interrupt enable for MON7, 0 = Disable, 1 = Enable

Table 7-28. IEN_UVHF Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	MON[6]	R/W	xb	UVHF interrupt enable for MON6, 0 = Disable, 1 = Enable
4	MON[5]	R/W	xb	UVHF interrupt enable for MON5, 0 = Disable, 1 = Enable
3	MON[4]	R/W	xb	UVHF interrupt enable for MON4, 0 = Disable, 1 = Enable
2	MON[3]	R/W	xb	UVHF interrupt enable for MON3, 0 = Disable, 1 = Enable
1	MON[2]	R/W	xb	UVHF interrupt enable for MON2, 0 = Disable, 1 = Enable
0	RSVD	R/W	0b	RSVD

7.5.1.2.5 IEN_OVHF Register (Address = 0x15) [Reset = 0xXX]

IEN_OVHF is shown in Table 7-29.

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High Frequency channel Over-Voltage Interrupt Enable register.

Table 7-29. IEN_OVHF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	OVHF interrupt enable for MON7, 0 = Disable, 1 = Enable
5	MON[6]	R/W	xb	OVHF interrupt enable for MON6, 0 = Disable, 1 = Enable
4	MON[5]	R/W	xb	OVHF interrupt enable for MON5, 0 = Disable, 1 = Enable
3	MON[4]	R/W	xb	OVHF interrupt enable for MON4, 0 = Disable, 1 = Enable
2	MON[3]	R/W	xb	OVHF interrupt enable for MON3, 0 = Disable, 1 = Enable
1	MON[2]	R/W	xb	OVHF interrupt enable for MON2, 0 = Disable, 1 = Enable
0	RSVD	R/W	0b	RSVD

7.5.1.2.6 IEN_CONTROL Register (Address = 0x1B) [Reset = 0xXX]

IEN_CONTROL is shown in Table 7-30.

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Control and Communication Fault Interrupt Enable register.

Table 7-30. IEN_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	RT_CRC_Int	R/W	xb	Register Run time CRC (Cyclic Redundancy Checking) error Interrupt is a static CRC perfomed on the register map content. If enabled there does not need to be any data read or write for this CRC check to occur. The purpose of this CRC is to identify if a static bit flip or random error in the register map content has occured. This is the safety mechanism is carried out using a CRC-8 polynomial, in the case of a read or write operation the register map content changes and the polynomial is re-calculated with the new value after the changes. Interrupt is reported in INT_CONTROL_F_CRC register of Bank 0. 0 = Disable Interrupt Mapping, 1 = Enable Interrupt Mapping
3	RSVD	R/W	0b	RSVD
2	TSD_INT	R/W	xb	Thermal shutdown Interrupt. 0 = Disable, 1 = Enable
1	RSVD	R/W	0b	RSVD
0	PEC_INT	R/W	xb	PEC Error Interrupt. 0 = Disable, 1 = Enable

7.5.1.2.7 IEN_TEST Register (Address = 0x1C) [Reset = 0x0X]

IEN_TEST is shown in Table 7-31.

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Internal Test and Configuration Load Fault Interrupt Enable register

Table 7-31. IEN_TEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RSVD	R/W	0000b	RSVD
3	ECC_SEC	R/W	xb	SEC Error Interrupt. 0 = Disable, 1 = Enable
2	RSVD	R/W	0b	RSVD
1	BIST_Complete_INT	R/W	xb	BIST complete Interrupt. 0 = Disable, 1 = Enable
0	BIST_Fail_INT	R/W	xb	BIST Fail Interrupt. 0 = Disable, 1 = Enable

7.5.1.2.8 IEN_VENDOR Register (Address = 0x1D) [Reset = 0xXX]

IEN_VENDOR is shown in Table 7-32.

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Vendor Specific Internal Interrupt Enable register.

Table 7-32. IEN_VENDOR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	Startup Self-Test_CRC	R/W	xb	Startup Self-Test_CRC Interrupt. 0 = Disable Interrupt Mapping, 1 = Enable Interrupt Mapping

Table 7-32. IEN_VENDOR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RESERVED	R	0b	
5	NRST_MISMATCH	R/W	xb	NRST mismatch Interrupt. 0 = Disable, 1 = Enable
4:3	RESERVED	R	0b	
2	WDT_TO_NIRQ	R/W	xb	Maps Watchdog fault to NIRQ. 0 = Not mapped 1 = Mapped
1	RSVD	R/W	0b	RSVD
0	WDT_TO_NRST	R/W	xb	Maps Watchdog fault to NRST. 0 = Not mapped 1 = Mapped

7.5.1.2.9 MON_CH_EN Register (Address = 0x1E) [Reset = 0xXX]

MON_CH_EN is shown in Table 7-33.

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Channel Voltage Monitoring Enable.

Table 7-33. MON_CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	Enables MON7 monitoring. 0 = Disabled, 1 = Enabled
5	MON[6]	R/W	xb	Enables MON6 monitoring. 0 = Disabled, 1 = Enabled
4	MON[5]	R/W	xb	Enables MON5monitoring. 0 = Disabled, 1 = Enabled
3	MON[4]	R/W	xb	Enables MON4 monitoring. 0 = Disabled, 1 = Enabled
2	MON[3]	R/W	xb	Enables MON3 monitoring. 0 = Disabled, 1 = Enabled
1	MON[2]	R/W	xb	Enables MON2 monitoring. 0 = Disabled, 1 = Enabled
0	RSVD	R/W	0b	RSVD

7.5.1.2.10 VRANGE_MULT Register (Address = 0x1F) [Reset = 0xXX]

VRANGE_MULT is shown in Table 7-34.

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Channel Voltage Monitoring Range/Scaling.

Table 7-34. VRANGE_MULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD

Table 7-34. VRANGE_MULT Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MON[7]	R/W	xb	Scalar for MON7. 0 = 1x, 1 = 4x
5	MON[6]	R/W	xb	Scalar for MON6. 0 = 1x, 1 = 4x
4	MON[5]	R/W	xb	Scalar for MON5. 0 = 1x, 1 = 4x
3	MON[4]	R/W	xb	Scalar for MON4. 0 = 1x, 1 = 4x
2	MON[3]	R/W	xb	Scalar for MON3. 0 = 1x, 1 = 4x
1	MON[2]	R/W	xb	Scalar for MON2. 0 = 1x, 1 = 4x
0	RSVD	R/W	0b	RSVD

7.5.1.2.11 UV_HF[2] Register (Address = 0x30) [Reset = 0xXX]

UV_HF[2] is shown in Table 7-35.

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Channel 2 High Frequency channel Under-Voltage threshold.

Table 7-35. UV_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.12 OV_HF[2] Register (Address = 0x31) [Reset = 0xXX]

OV_HF[2] is shown in Table 7-36.

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Channel 2 High Frequency channel Over-Voltage threshold.

Table 7-36. OV_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.13 FLT_HF[2] Register (Address = 0x34) [Reset = 0xXX]

FLT_HF[2] is shown in Table 7-37.

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Channel 2 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-37. FLT_HF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.14 FC_LF[2] Register (Address = 0x35) [Reset = 0xXX]

FC_LF[2] is shown in Table 7-38.

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Channel 2 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-38. FC_LF[2] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON2 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON2 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.15 UV_HF[3] Register (Address = 0x40) [Reset = 0xXX]

UV_HF[3] is shown in Table 7-39.

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Channel 3 High Frequency channel Under-Voltage threshold.

Table 7-39. UV_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.16 OV_HF[3] Register (Address = 0x41) [Reset = 0xXX]

OV_HF[3] is shown in Table 7-40.

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Channel 3 High Frequency channel Over-Voltage threshold.

Table 7-40. OV_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.17 FLT_HF[3] Register (Address = 0x44) [Reset = 0xXX]

FLT_HF[3] is shown in Table 7-41.

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Channel 3 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-41. FLT_HF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.18 FC_LF[3] Register (Address = 0x45) [Reset = 0xXX]

FC_LF[3] is shown in Table 7-42.

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Channel 3 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-42. FC_LF[3] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON3 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON3 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.19 UV_HF[4] Register (Address = 0x50) [Reset = 0xXX]

UV_HF[4] is shown in Table 7-43.

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Channel 4 High Frequency channel Under-Voltage threshold.

Table 7-43. UV_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.20 OV_HF[4] Register (Address = 0x51) [Reset = 0xXX]

OV_HF[4] is shown in Table 7-44.

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Channel 4 High Frequency channel Over-Voltage threshold.

Table 7-44. OV_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.21 FLT_HF[4] Register (Address = 0x54) [Reset = 0xXX]

FLT_HF[4] is shown in Table 7-45.

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Channel 4 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-45. FLT_HF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.22 FC_LF[4] Register (Address = 0x55) [Reset = 0xXX]

FC_LF[4] is shown in Table 7-46.

Return to the Summary Table.

Channel 4 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-46. FC_LF[4] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON4 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON4 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.23 UV_HF[5] Register (Address = 0x60) [Reset = 0xXX]

UV_HF[5] is shown in Table 7-47.

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Channel 5 High Frequency channel Under-Voltage threshold.

Table 7-47. UV_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.24 OV_HF[5] Register (Address = 0x61) [Reset = 0xXX]

OV_HF[5] is shown in Table 7-48.

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Channel 5 High Frequency channel Over-Voltage threshold.

Table 7-48. OV_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.25 FLT_HF[5] Register (Address = 0x64) [Reset = 0xXX]

FLT_HF[5] is shown in Table 7-49.

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Channel 5 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-49. FLT_HF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.26 FC_LF[5] Register (Address = 0x65) [Reset = 0xXX]

FC_LF[5] is shown in Table 7-50.

Return to the Summary Table.

Channel 5 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-50. FC_LF[5] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON5OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON5 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.27 UV_HF[6] Register (Address = 0x70) [Reset = 0xXX]

UV_HF[6] is shown in Table 7-51.

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Channel 6 High Frequency channel Under-Voltage threshold.

Table 7-51. UV_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.28 OV_HF[6] Register (Address = 0x71) [Reset = 0xXX]

OV_HF[6] is shown in Table 7-52.

Return to the Summary Table.

Channel 6 High Frequency channel Over-Voltage threshold.

Table 7-52. OV_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.29 FLT_HF[6] Register (Address = 0x74) [Reset = 0xXX]

FLT_HF[6] is shown in Table 7-53.

Return to the Summary Table.

Channel 6 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-53. FLT_HF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.30 FC_LF[6] Register (Address = 0x75) [Reset = 0xXX]

FC_LF[6] is shown in Table 7-54.

Return to the Summary Table.

Channel 6 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-54. FC_LF[6] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON6OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON6UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.31 UV_HF[7] Register (Address = 0x80) [Reset = 0xXX]

UV_HF[7] is shown in Table 7-55.

Return to the Summary Table.

Channel 7 High Frequency channel Under-Voltage threshold.

Table 7-55. UV_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Undervoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.32 OV_HF[7] Register (Address = 0x81) [Reset = 0xXX]

OV_HF[7] is shown in Table 7-56.

Return to the Summary Table.

Channel 7 High Frequency channel Over-Voltage threshold.

Table 7-56. OV_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	THRESHOLD[7:0]	R/W	xxxxxxxxb	Overvoltage threshold for High Frequency component of monitored channel. The 8-bit value interpretation depends on the scaling setting in register VRANGE_MULT. With scaling = 1x, the 8-bit value represents the range 0.2V to 1.475V with 1 LSB = 5mV. With scaling = 4x, the 8-bit value represents the range 0.8V to 5.9V with 1 LSB = 20mV.

7.5.1.2.33 FLT_HF[7] Register (Address = 0x84) [Reset = 0xXX]

FLT_HF[7] is shown in Table 7-57.

Return to the Summary Table.

Channel 7 UV and OV debouncing for High Frequency thresholds comparator output.

Table 7-57. FLT_HF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	OV_DEB[3:0]	R/W	xxxxb	Overvoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs
3:0	UV_DEB[3:0]	R/W	xxxxb	Undervoltage comparator output debounce time (dont assert until output is stable for debounce time) for High Frequency monitoring path. 0000b = 0.1µs 1000b = 25.6µs 0001b = 0.2µs 1001b = 51.2µs 0010b = 0.4µs 1010b = 102.4µs 0011b = 0.8µs 1011b = 102.4µs 0100b = 1.6µs 1100b = 102.4µs 0101b = 3.2µs 1101b = 102.4µs 0110b = 6.4µs 1110b = 102.4µs 0111b = 12.8µs 1111b = 102.4µs

7.5.1.2.34 FC_LF[7] Register (Address = 0x85) [Reset = 0xXX]

FC_LF[7] is shown in Table 7-58.

Return to the Summary Table.

Channel 7 Register allows for an Over-Voltage or Under-Voltage fault to be mapped to NRST.

Table 7-58. FC_LF[7] Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RSVD	R/W	000b	RSVD
4	OVHF_TO_NRST	R/W	xb	Maps MON7 OVHF fault to NRST 0 = Not mapped, 1 = Mapped
3	UVHF_TO_NRST	R/W	xb	Maps MON7 UVHF fault to NRST 0 = Not mapped, 1 = Mapped
2:0	RSVD	R/W	000b	RSVD

7.5.1.2.35 TI_CONTROL Register (Address = 0x9F) [Reset = 0xXX]

TI_CONTROL is shown in Table 7-59.

Return to the Summary Table.

Manual BIST/WD EN/Manual Reset via I2C/ESM deglitch/Reset delay

Table 7-59. TI_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ENTER_BIST	R/W	0b	Manual BIST. 1 = Enter BIST
6	WDT_EN	R/W	xb	Watchdog EN to be used along with hardware WD_EN pin. 1 = Watchdog Enabled, 0 = Watchdog Disabled
5	I2C_MR	R/W	0b	Manual Reset. 1 = Assert NRST low
4:3	RSVD	R/W	00b	RSVD
2:0	RST_DLY[2:0]	R/W	xxxb	Reset delay 000 = 200µs 001 = 1ms 010 = 10ms 011 = 16ms 100 = 20ms 101 = 70ms 110 = 100ms 111 = 200ms

7.5.1.2.36 AMSK_ON Register (Address = 0xA1) [Reset = 0xXX]

AMSK_ON is shown in Table 7-60.

Return to the Summary Table.

Auto-mask UVHF, and OVHF interrupts on power up transitions.

Table 7-60. AMSK_ON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD

Table 7-60. AMSK_ON Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	MON[7]	R/W	xb	Automask at power on for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	xb	Automask at power on for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	xb	Automask at power on for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	xb	Automask at power on for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	xb	Automask at power on for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	xb	Automask at power on for MON2. 0 = Disabled 1 = Enabled
0	RSVD	R/W	0b	RSVD

7.5.1.2.37 AMSK_OFF Register (Address = 0xA2) [Reset = 0xXX]

AMSK_OFF is shown in Table 7-61.

Return to the Summary Table.

Auto-mask UVHF, and OVHF interrupts on power down transitions.

Table 7-61. AMSK_OFF Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	Automask at power off for MON7. 0 = Disabled 1 = Enabled
5	MON[6]	R/W	xb	Automask at power off for MON6. 0 = Disabled 1 = Enabled
4	MON[5]	R/W	xb	Automask at power off for MON5. 0 = Disabled 1 = Enabled
3	MON[4]	R/W	xb	Automask at power off for MON4. 0 = Disabled 1 = Enabled
2	MON[3]	R/W	xb	Automask at power off for MON3. 0 = Disabled 1 = Enabled
1	MON[2]	R/W	xb	Automask at power off for MON2. 0 = Disabled 1 = Enabled
0	RSVD	R/W	0b	RSVD

7.5.1.2.38 SEQ_TOUT_MSB Register (Address = 0xA5) [Reset = 0xXX]

SEQ_TOUT_MSB is shown in Table 7-62.

Return to the Summary Table.

Timeout for UV faults during powerup and power down.

Table 7-62. SEQ_TOUT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MILLISEC[15:8]	R/W	xxxxxxxxb	Sequence timeout duration MSB, after the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active. 0x0000 = 1ms 0x0001 = 2ms While the max value is not specified, it is desirable to be able to set this timeout up to 4s, and at least 256ms (using only the lower byte at address 0xA6).

7.5.1.2.39 SEQ_TOUT_LSB Register (Address = 0xA6) [Reset = 0xXX]

SEQ_TOUT_LSB is shown in Table 7-63.

Return to the Summary Table.

Timeout for UV faults during powerup and power down.

Table 7-63. SEQ_TOUT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MILLISEC[7:0]	R/W	xxxxxxxxb	Sequence timeout duration LSB, after the timeout, the auto-masks (AMSK_xxx) are released and the IEN_xVxF interrupts become active. 0x0000 = 1ms 0x0001 = 2ms While the max value is not specified, it is desirable to be able to set this timeout up to 4s, and at least 256ms (using only the lower byte at address 0xA6).

7.5.1.2.40 SEQ_UP_THLD Register (Address = 0xA8) [Reset = 0xXX]

SEQ_UP_THLD is shown in Table 7-64.

Return to the Summary Table.

Threshold at which AMSK is released (VMON considered on) for power up.

Table 7-64. SEQ_UP_THLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
5	MON[6]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
4	MON[5]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
3	MON[4]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
2	MON[3]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
1	MON[2]	R/W	xb	OFF (200mV) threshold selection for Power ON monitor masking: 00b = Use OFF threshold (200mV)
0	RSVD	R/W	0b	RSVD

7.5.1.2.41 SEQ_DN_THLD Register (Address = 0xA9) [Reset = 0xXX]

SEQ_DN_THLD is shown in Table 7-65.

Return to the Summary Table.

Threshold at which AMSK is released (VMON considered off) for power down.

Table 7-65. SEQ_DN_THLD Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6	MON[7]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
5	MON[6]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
4	MON[5]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
3	MON[4]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
2	MON[3]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
1	MON[2]	R/W	xb	OFF (200mV) threshold selection for Power OFF monitor masking: 00b = Use OFF threshold (200mV)
0	RSVD	R/W	xb	RSVD

7.5.1.2.42 WDT_CFG Register (Address = 0xAA) [Reset = 0xXX]

WDT_CFG is shown in Table 7-66.

Return to the Summary Table.

Max violation count for WD and Delay multiplier for Start Up Window.

Table 7-66. WDT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R/W	0b	RSVD
6:4	MAX_VIOLATION_COUNT	R/W	xxxb	Max violation count for Watchdog 000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7
3	RSVD	R/W	0b	RSVD
2:0	WDT_Startup_DLY_MULTIPLIER[2:0]	R/W	xxxb	Watchdog Startup delay multiplier 000 = 0 001 = 1 010 = 2 011 = 3 100 = 4 101 = 5 110 = 6 111 = 7

7.5.1.2.43 WDT_CLOSE Register (Address = 0xAB) [Reset = 0xXX]

WDT_CLOSE is shown in Table 7-67.

Return to the Summary Table.

Close Window Time.

Table 7-67. WDT_CLOSE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CLOSE[7:0]	R/W	xxxxxxxxb	Close window time (1ms to 864ms)

7.5.1.2.44 WDT_OPEN Register (Address = 0xAC) [Reset = 0xXX]

WDT_OPEN is shown in Table 7-68.

Return to the Summary Table.

Open Window Time.

Table 7-68. WDT_OPEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OPEN[7:0]	R/W	xxxxxxxxb	Open window time (1ms to 864ms)

7.5.1.2.45 BANK_SEL Register (Address = 0xF0) [Reset = 0x00]

BANK_SEL is shown in Table 7-69.

Return to the Summary Table.

Bank Select.

Table 7-69. BANK_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RSVD	R/W	0000000b	RSVD
0	BANK_Select	R/W	0b	Represents bank selection. 0 = Bank 0 1 = Bank 1

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Modern SOC and FPGA devices typically have multiple power rails to provide power to the different blocks within the IC. Accurate voltage level and timing requirements are common and must be met to maintain proper operation of these devices. By utilizing TPS388C0x-Q1 along with a multichannel voltage sequencer, the power up and power down sequencing requirements as well as the core voltage requirements of the target SoC or FPGA device can be met. This design focuses on meeting the timing requirements for an SoC by using the TPS388C0x-Q1.

8.2 Typical Application

8.2.1 Automotive Multichannel Sequencer and Monitor

A typical application for the TPS388C0x-Q1 is shown in Figure 8-1. TPS388C0x-Q1 is used to provide the proper voltage monitoring for the target SOC device. A multichannel voltage monitor TPS388C0x-Q1 is used to monitor the voltage rails as these rails power up and power down to verify that the correct sequence occurs in both occasions. A safety microcontroller is also used to provide ACT, NIRQ, and I^2C commands to the TPS388C0x-Q1 and sequencer. The ACT signal from the safety microcontroller determines when the TPS388C0x-Q1enters into ACTIVE or SHDN states while the NIRQ pin of the TPS388C0x-Q1 acts as an interrupt pin that is set when a fault has occurred. The host microcontroller can clear the fault by writing 1 to the affected register. The power rails for the safety microcontroller are not shown in TPS388C0-Q1 Voltage Monitor Design Block Diagram for simplicity.

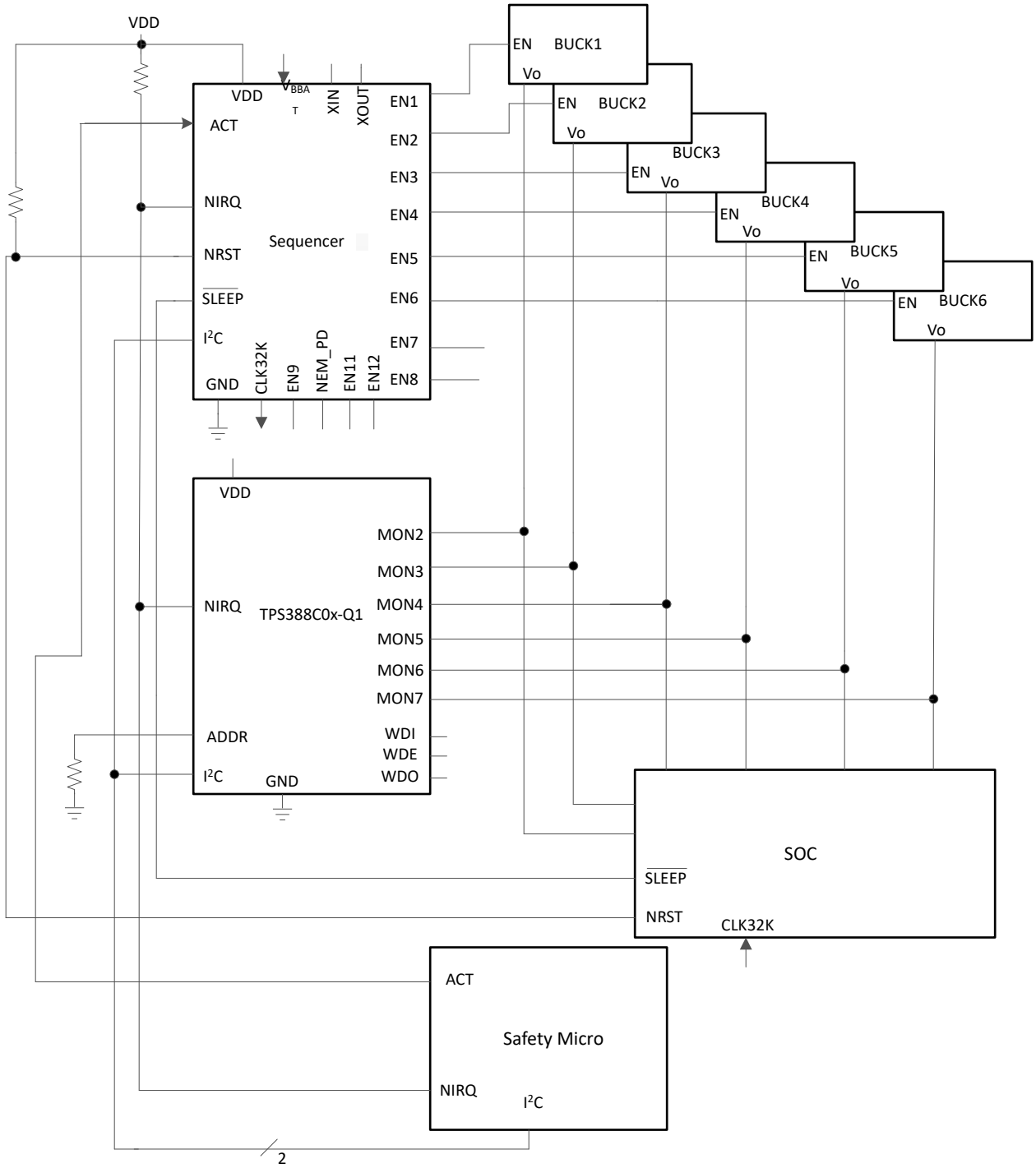


Figure 8-1. TPS388C0-Q1 Voltage Monitor Design Block Diagram

8.2.2 Design Requirements

- Three different voltage rails supplied by DC/DC converters need to be properly monitored in this design.
- All detected failures in sequencing are reported via an external hardware interrupt signal.
- All detected failures are logged in internal registers and be accessible to an external processor via I^2C.

8.2.3 Detailed Design Procedure

- TPS388C0x-Q1 device option comes preprogrammed with default values for over voltage, under voltage.

- NIRQ pin requires a pull up resistor in the range of 1kΩ to 100kΩ.
- NRST pin requires a pull up resistor in the range of 1kΩ to 100kΩ.
- ACT pin requires a pull up resistor in the range of 1kΩ to 100kΩ.
- SDA and SCL lines require pull up resistors in the range of 10kΩ.
- The safety microcontroller is used to clear fault interrupts reported through the NIRQ interrupt pin and the INT_SCR1 and INT_SCR2 registers. The interrupt flags can only be cleared by the host mircontroller with a write-1-to-clear operation; interrupt flags are not automatically cleared if the fault condition is no longer present.

8.2.4 Application Curves

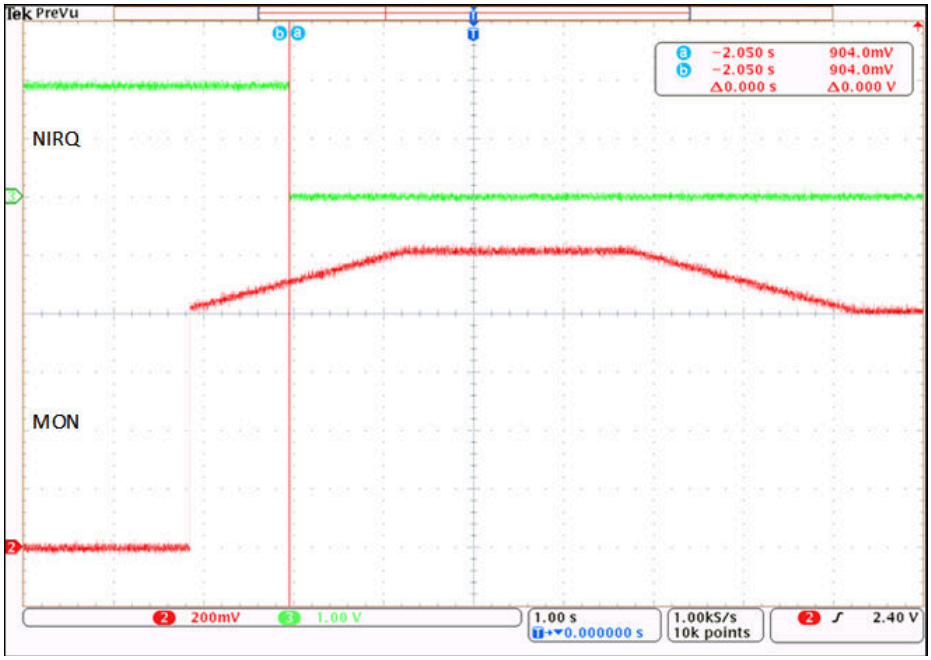


Figure 8-2. NIRQ Triggered After an Overvoltage Fault

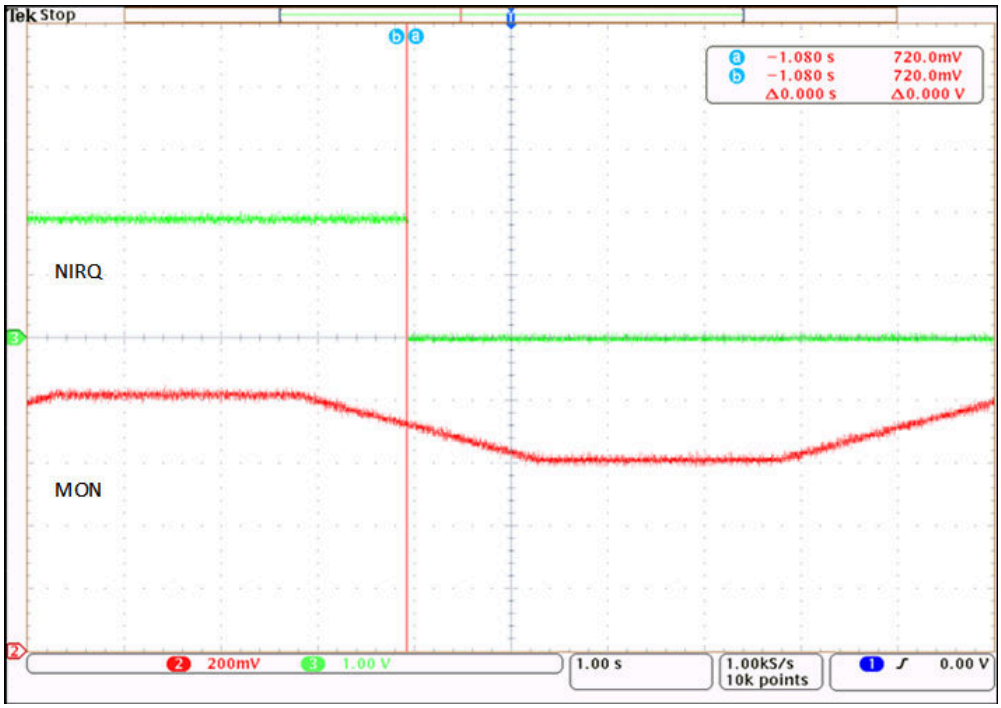


Figure 8-3. NIRQ Triggered After an Undervoltage Fault

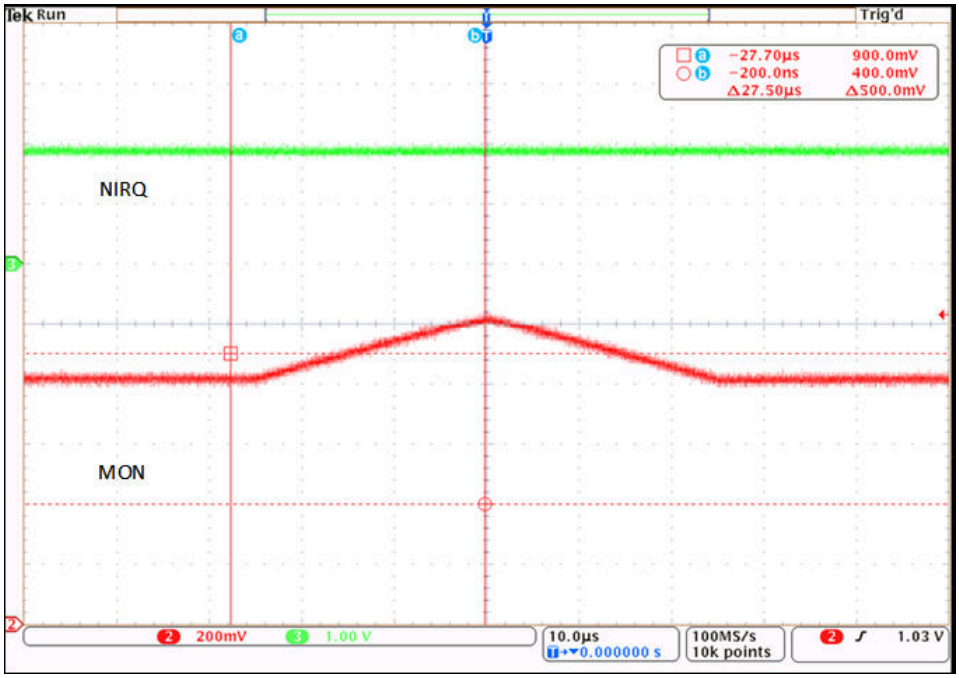


Figure 8-4. NIRQ Not Triggered on Overvoltage Fault with 51.2us OV Debounce Filter

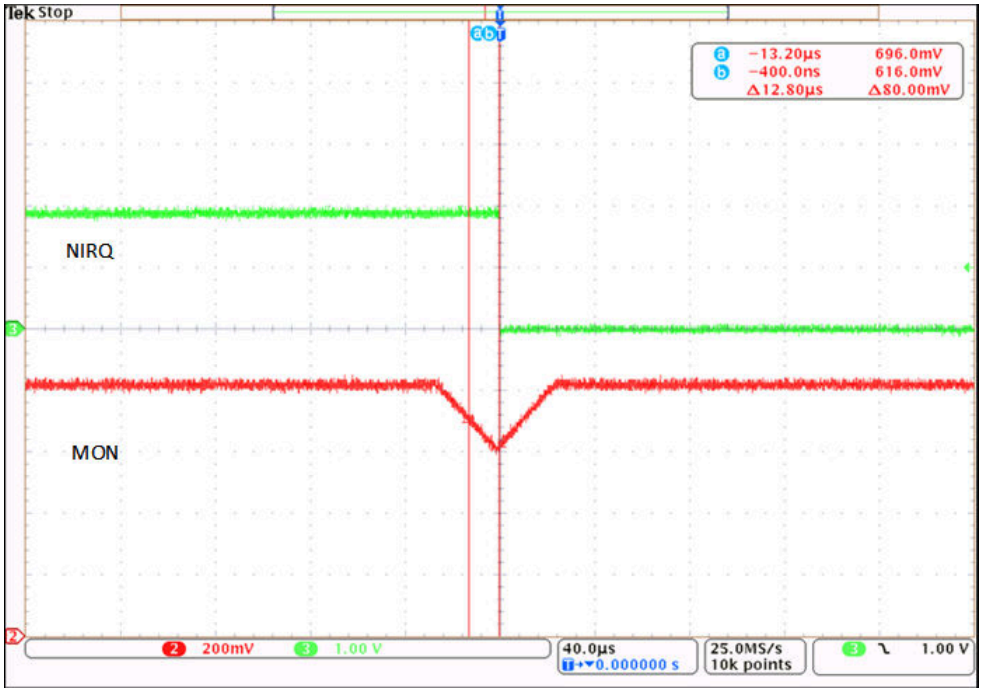


Figure 8-5. NIRQ Triggered on Undervoltage Fault with 12.8us UV Debounce Filter

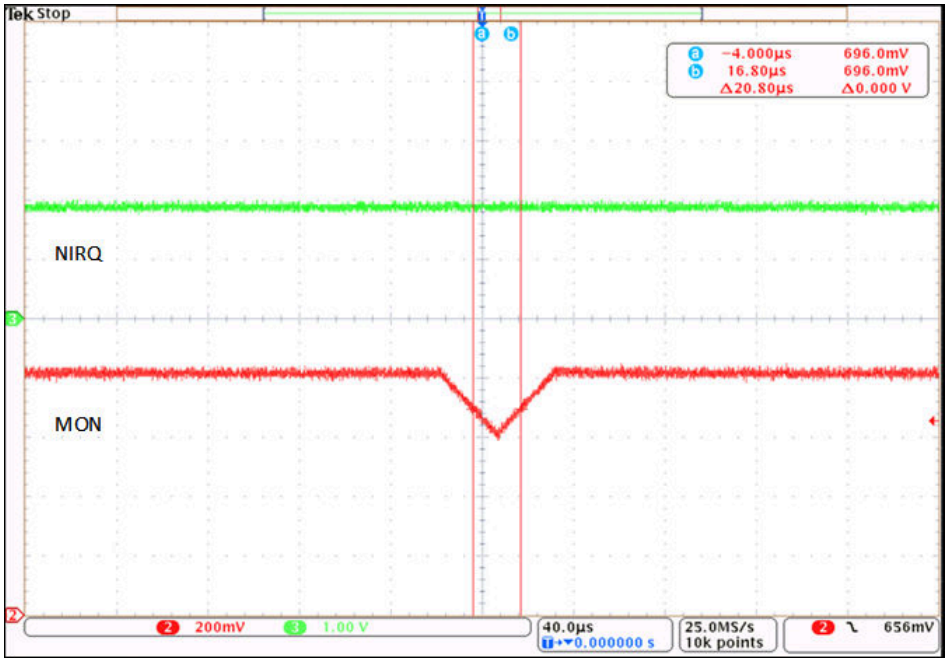


Figure 8-6. NIRQ Not Triggered on Undervoltage Fault with 25us UV Debounce Filter

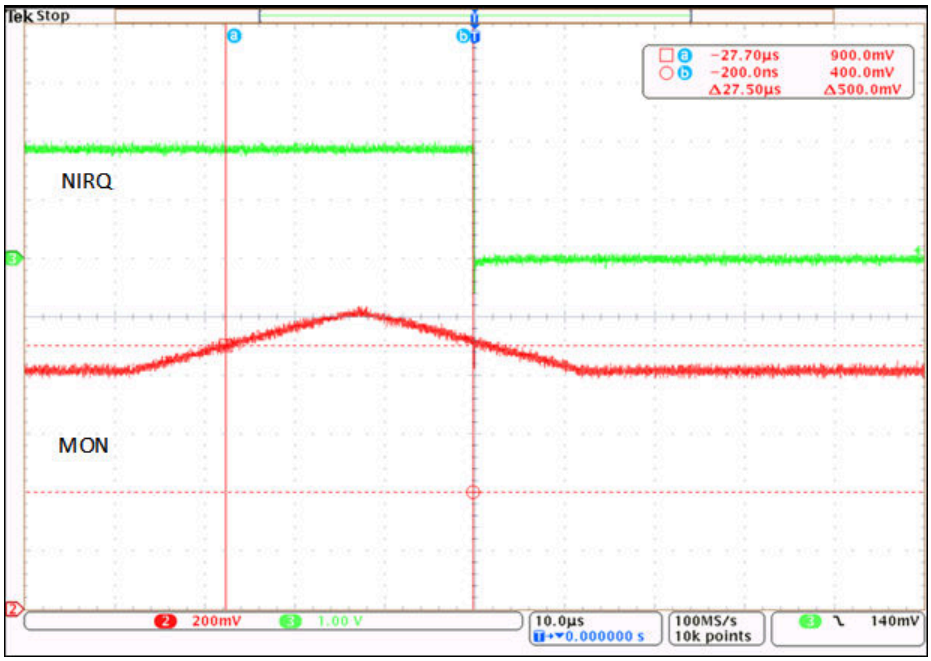


Figure 8-7. NIRQ Triggered on Overvoltage Fault with 25us OV Debounce Filter

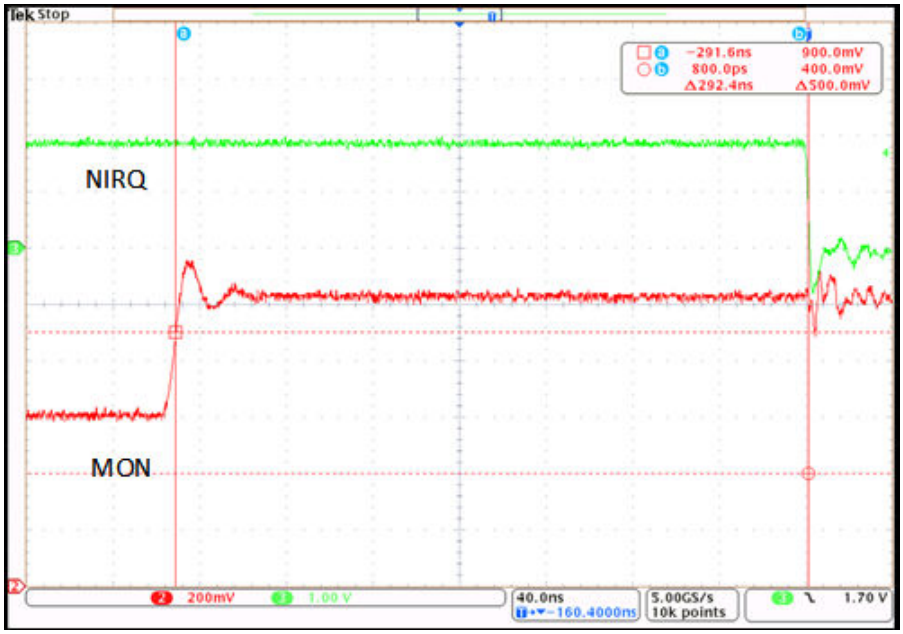


Figure 8-8. NIRQ Propagation Delay Resulting from Overvoltage Fault

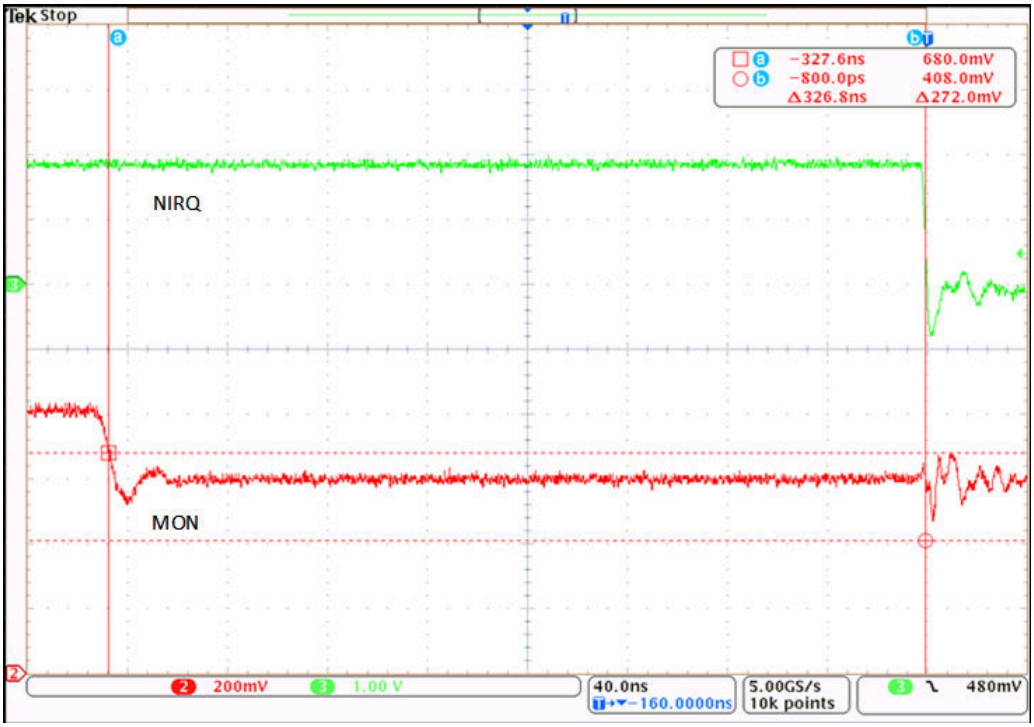


Figure 8-9. NIRQ Propagation Delay Resulting from Undervoltage Fault

8.3 Power Supply Recommendations

8.3.1 Power Supply Guidelines

This device is designed to operate from an input supply with a voltage range between 2.5V to 5.5V. TPS388C0x-Q1 has a 6V absolute maximum rating on the VDD pin. A good analog practice to place a 0.1µF to 1µF capacitor between the VDD pin and the GND pin depending on the input voltage supply noise. If the voltage

supply providing power to VDD is susceptible to any large voltage transient that exceed maximum specifications, additional precautions must be taken. See SNVA849 for more information.

8.4 Layout

8.4.1 Layout Guidelines

- Place the external components as close to the device as possible. This configuration prevents parasitic errors from occurring.
- Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC circuit and create ringing with peak voltages above the maximum VDD voltage.
- Avoid using long traces of voltage to the MON pin. Long traces increase parasitic inductance and cause inaccurate monitoring and diagnostics.
- If differential voltage sensing is required for MON1 and/or MON2 route RS_1/2 pin to the point of measurement
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

8.4.2 Layout Example

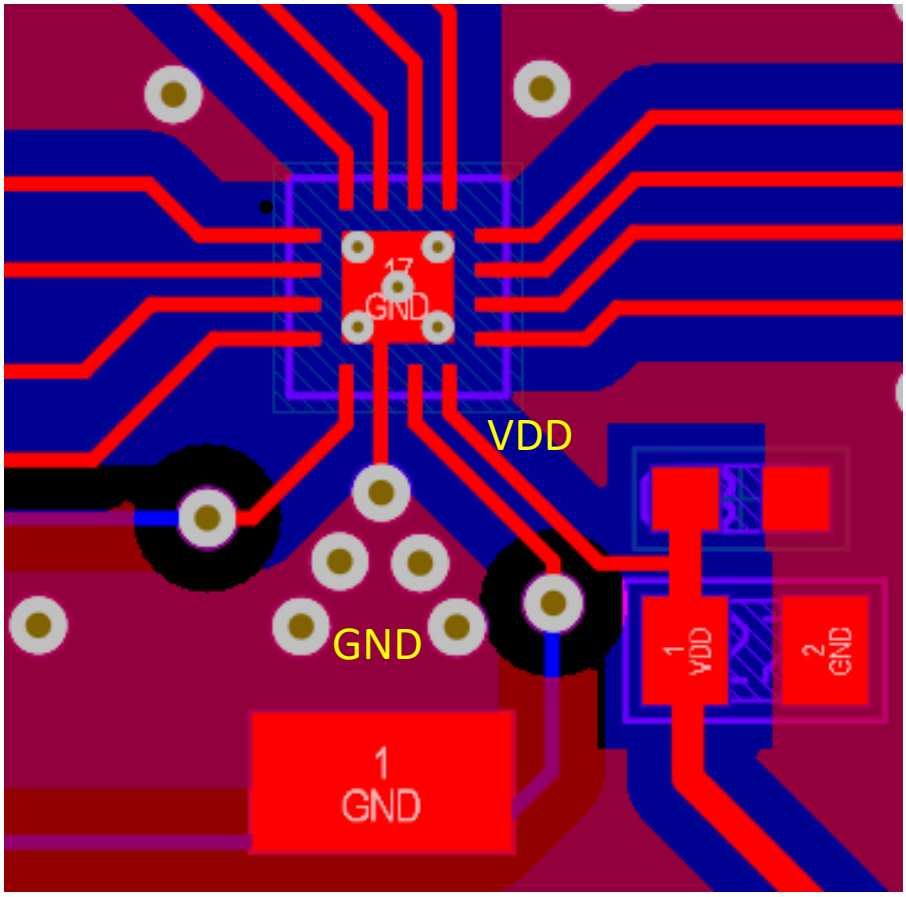


Figure 8-10. Recommended Layout

9 Device and Documentation Support

9.1 Device Nomenclature

Table 9-1 and Table 9-2 show how to decode the function of the device based on the part number.

Table 9-1. Device Thresholds TPS388C06-Q1

ORDERING CODE	Thresholds	VMON2 (V)	VMON3 (V)	VMON4 (V)	VMON5 (V)	VMON6 (V)	VMON7 (V)
TPS388C06001RTER-Q1	UV_HF/ OV_HF	3.0/3.6	1.08/1.30	1.60/1.98	0.90/1.1	1.60/1.98	2.72/3.6

Table 9-2. Device Configuration Table

ORDERING CODE	WD Close/ Open Windows	SCALING	OV/UV DEBOUNCE	NRST mapping	WD Fault mapping	BIST	SEQ TIMEOUT/ RESET DELAY	PEC (1)	I²C PULL-UP VOLTAGE (V)	WD Violation count/WD startup multiplier
TPS388C06001RTER	10ms/ 188ms	4/4/4/4/4/4	102.4µsec	MON7	NIRQ	at POR	25ms/20ms	Disable	3.3	1/0

(1) For parts with PEC enabled:
- a. PEC calculation is based on initializing to 0x00.
- b. In case of a PEC violation there needs to be a subsequent I^2C transaction before NIRQ is asserted.
- c. If incorrect PEC is given TPS388C0x-Q1 asserts NIRQ.
- d. If there is an extra byte after successfully writing the correct PEC byte, NIRQ asserts and the write fails.

9.2 Documentation Support

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

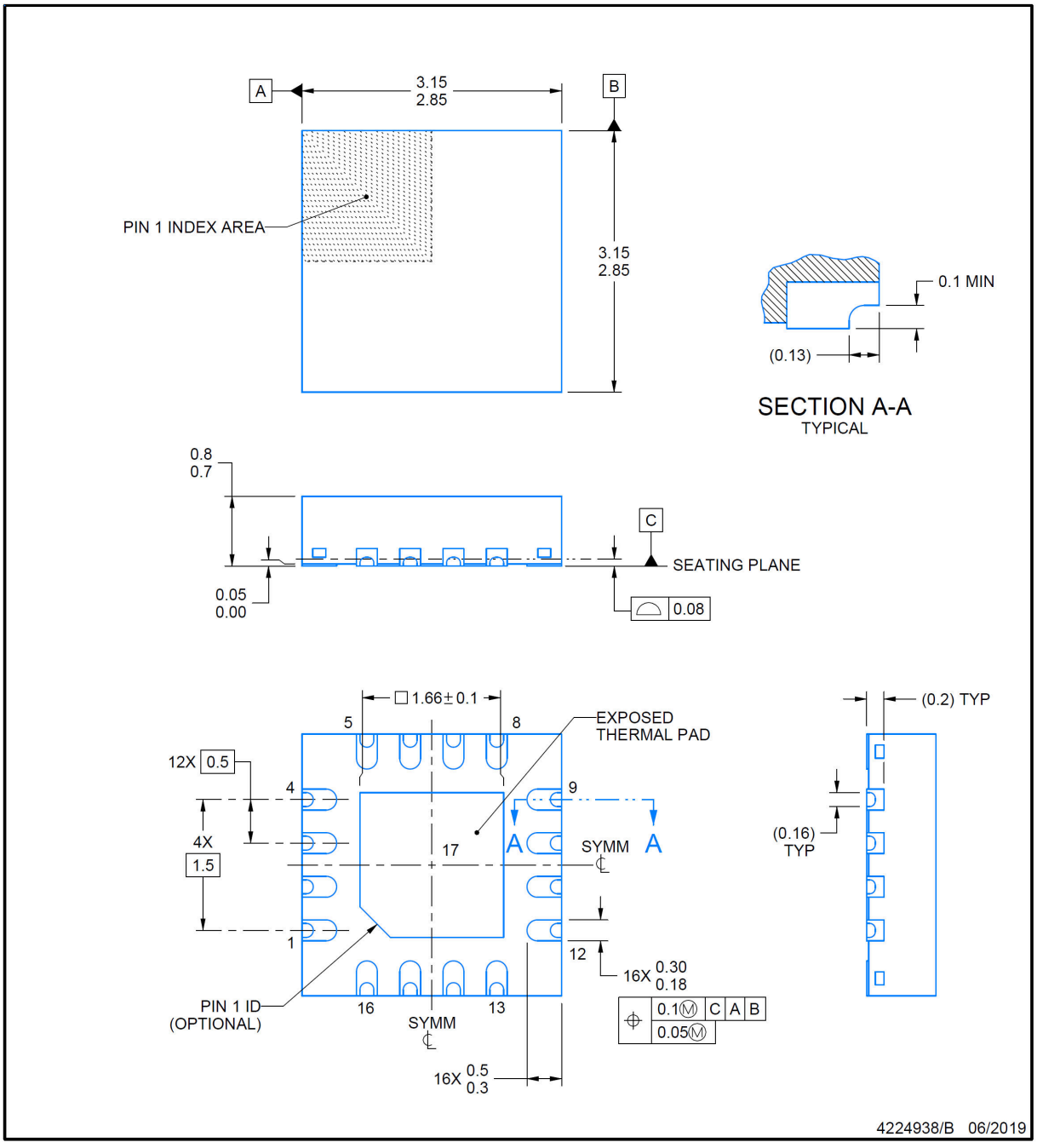
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

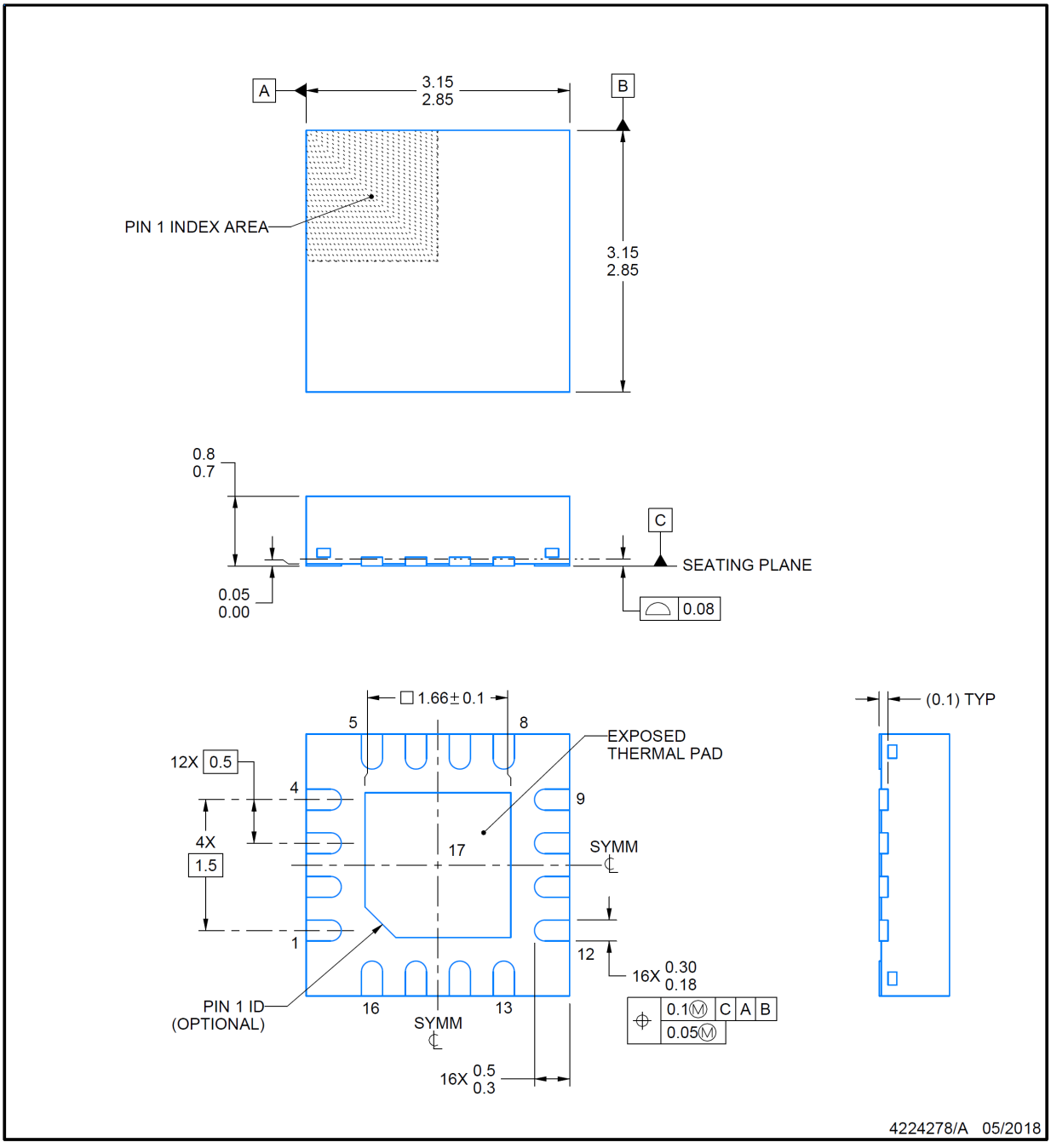
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

PACKAGE OUTLINE

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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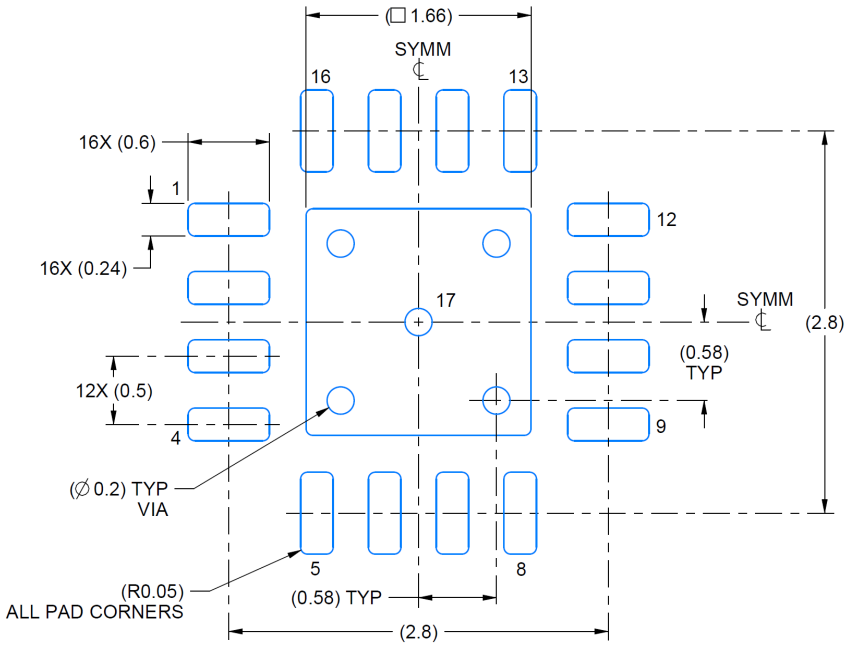
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

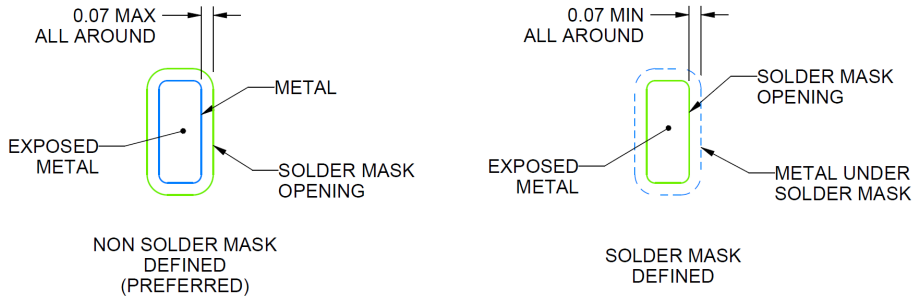
RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224938/B 06/2019

NOTES: (continued)

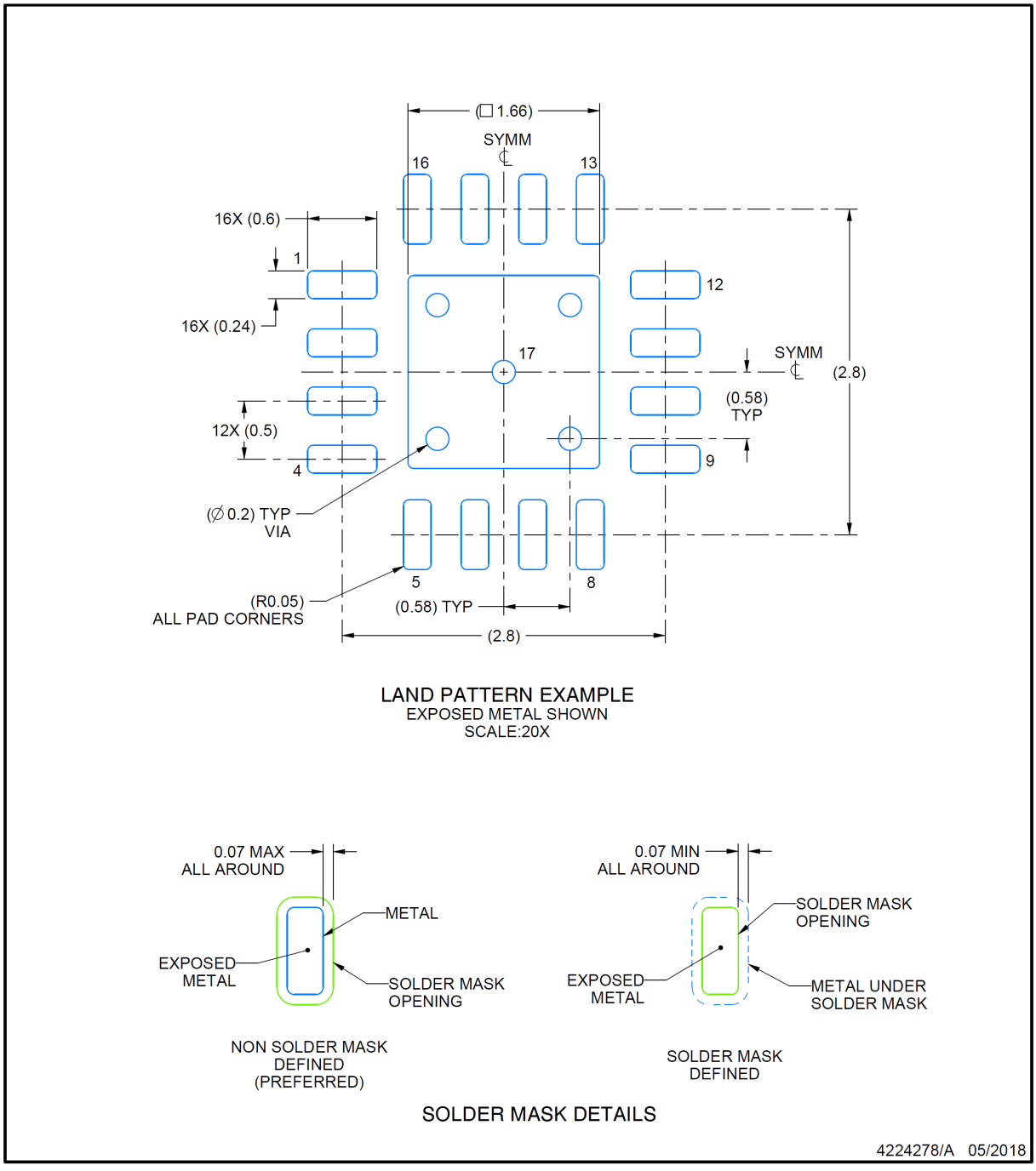
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE BOARD LAYOUT

RTE0016J

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
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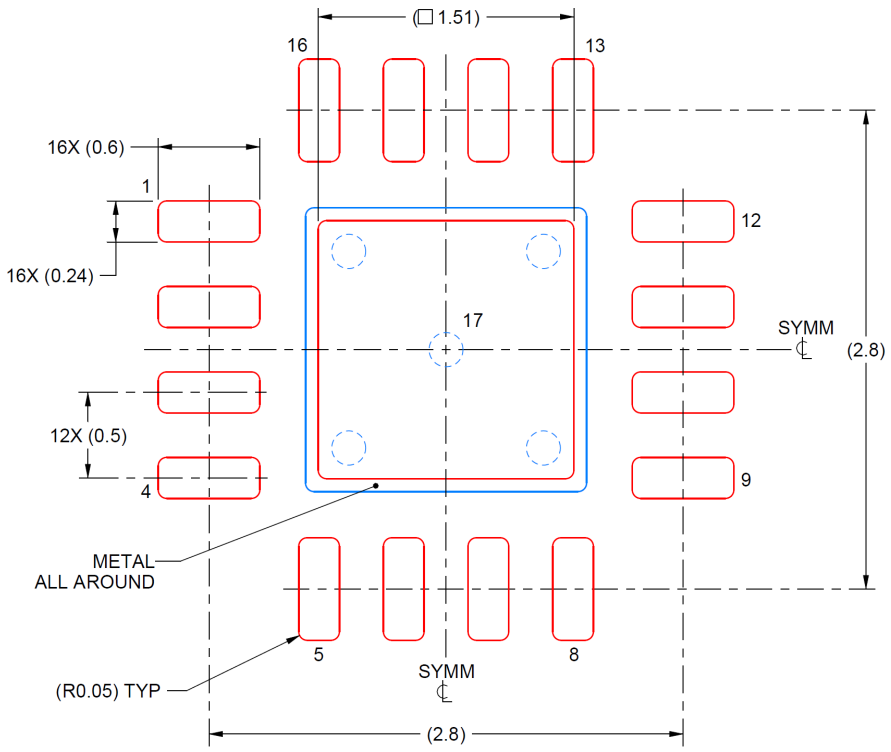
EXAMPLE STENCIL DESIGN

RTE0016K

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/B 06/2019

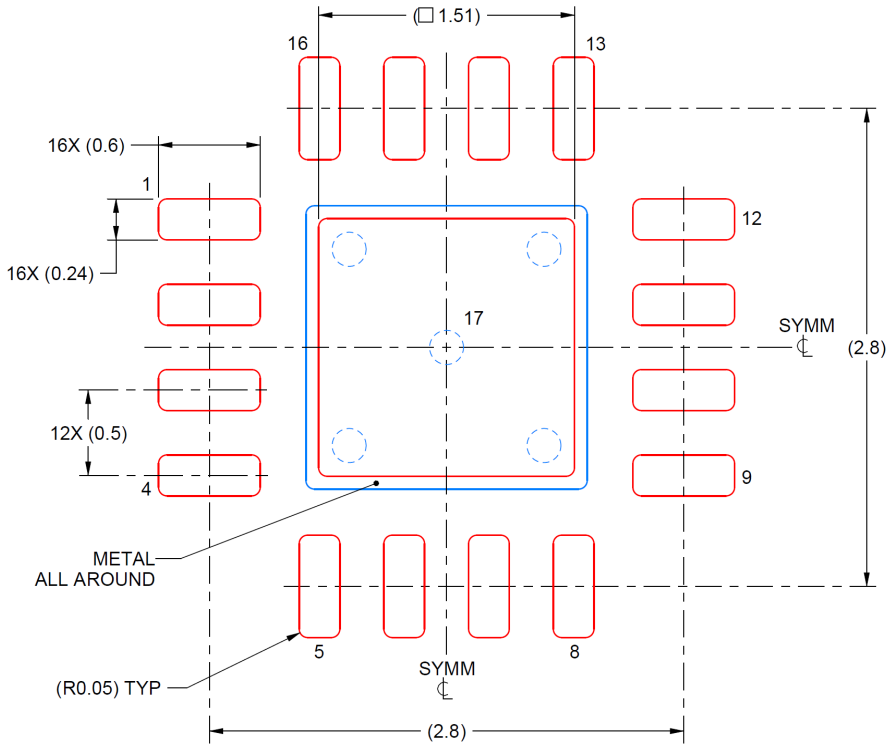
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE STENCIL DESIGN

RTE0016J — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224278/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS388C06001RTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TC060

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

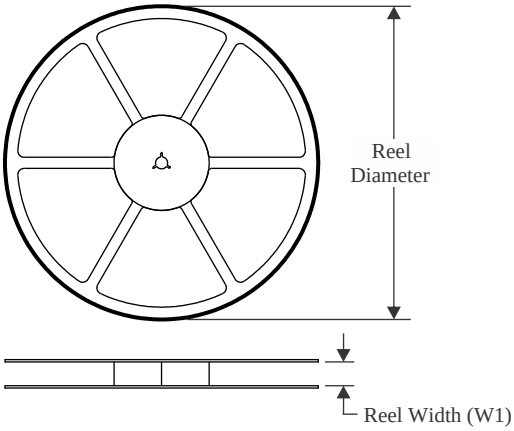
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

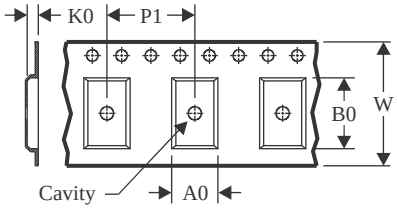
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

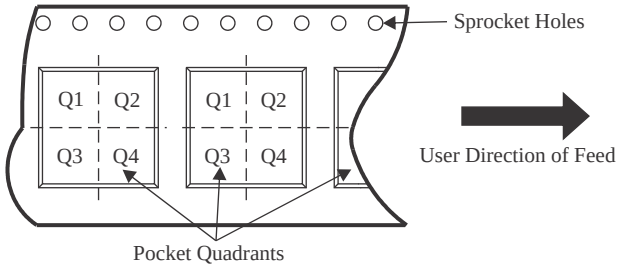


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

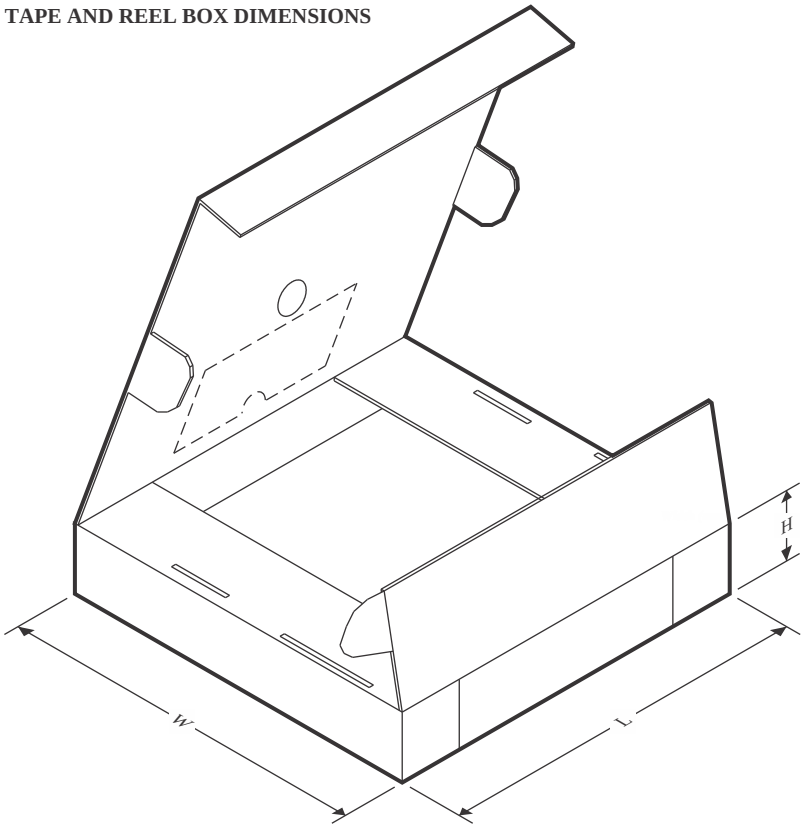
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS388C06001RTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS388C06001RTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

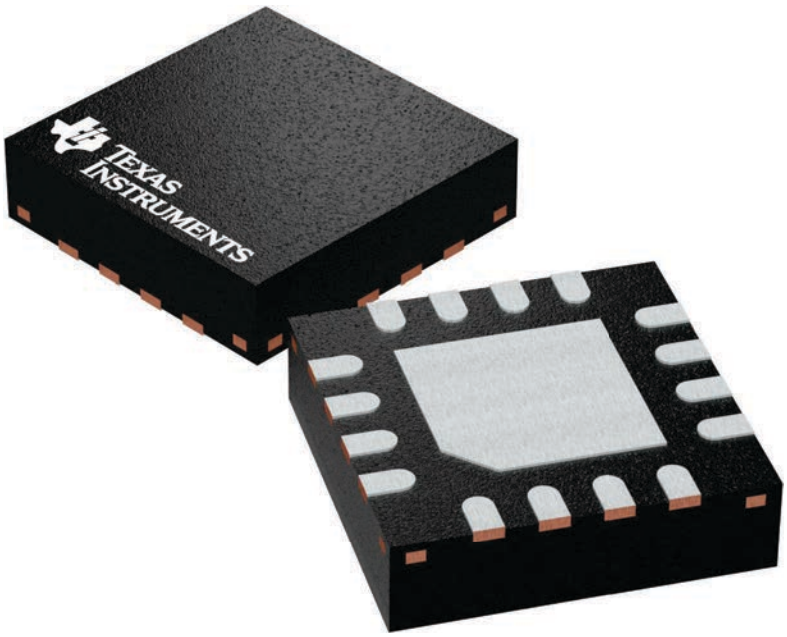
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



RTE0016K

PACKAGE OUTLINE

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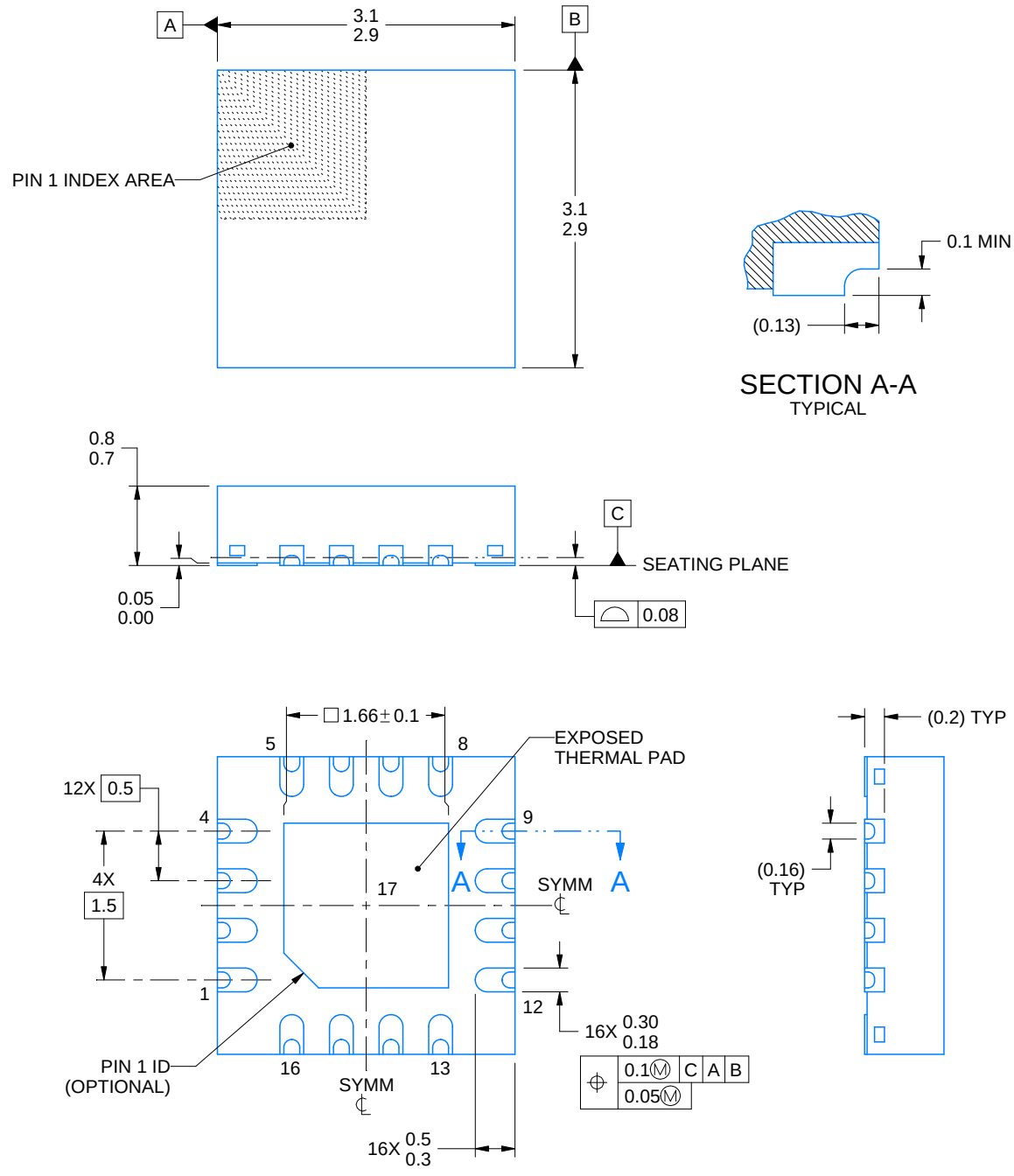

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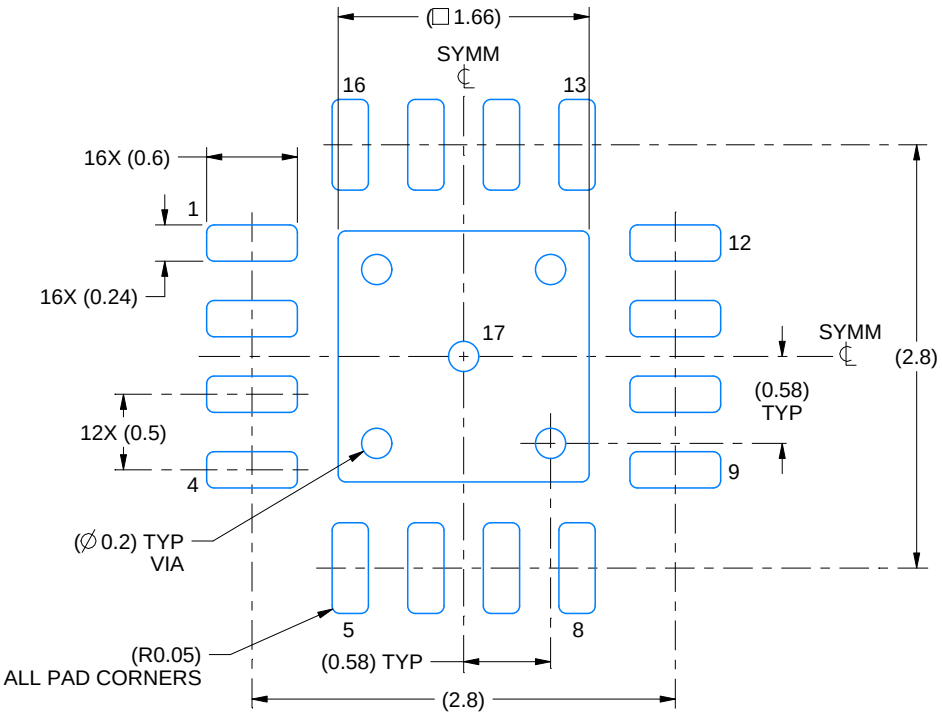
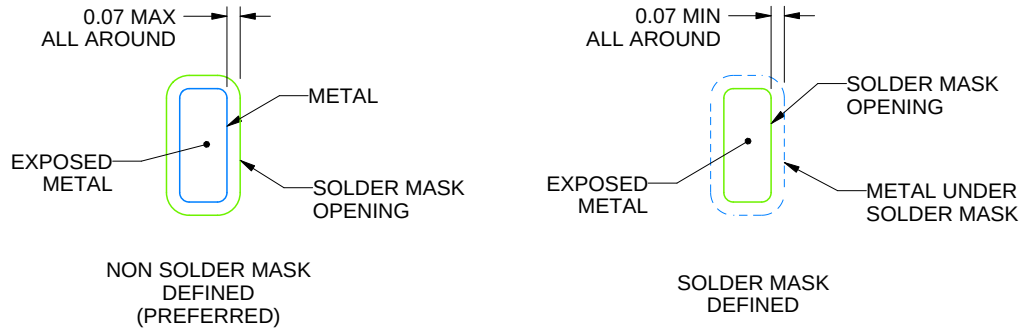


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4224938/C 03/2022

NOTES: (continued)

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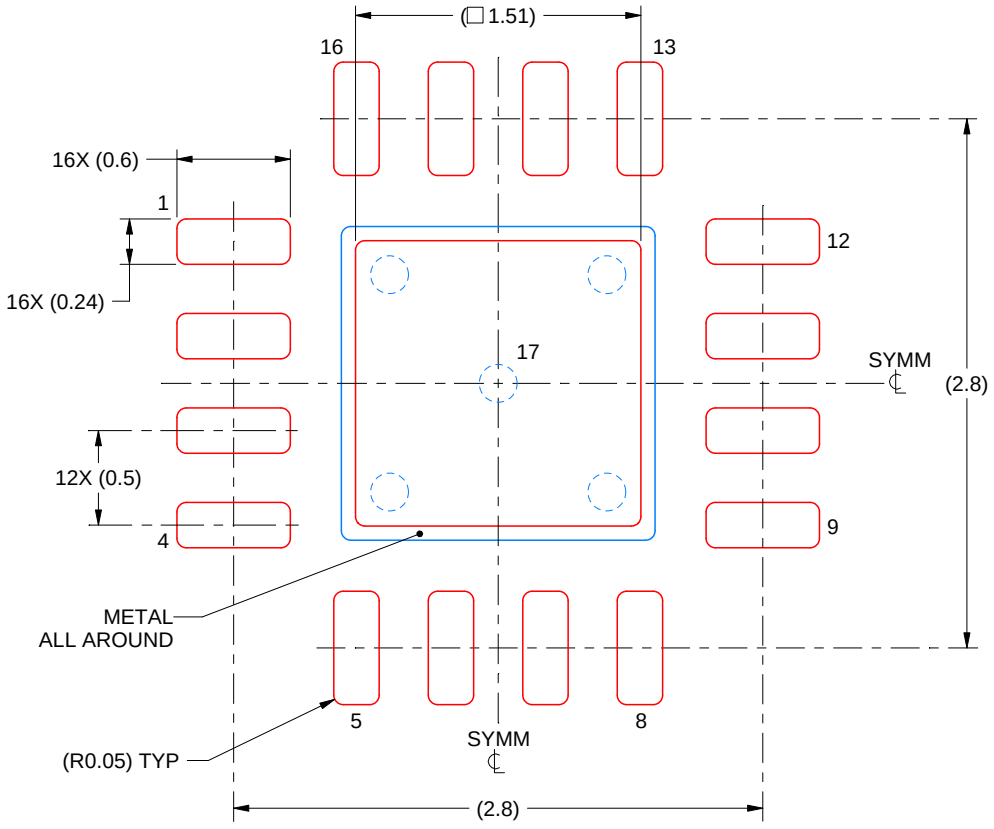

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265