TPS3899 Nano-Power 高精度電圧スーパーバイザ、プッシュ・ボタン・モニタ、プログラム可能なセンスおよびリセット遅延付き

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 高精度の電圧およびプッシュ ボタン モニタ
- VDD 範囲:0.85V～6V (DL および PL 出力)
- VDD 範囲:1V～6V (PH 出力)
- プログラム可能なセンスおよびリセット遅延
- わずかな静止電流:125nA (標準値)
- 高いスレッショルド精度:±0.5% (標準値)
- 高精度ヒステリシス:5% (標準値)
- 調整可能なスレッショルド電圧:0.505V (標準値)
- 固定スレッショルド電圧:0.8V～5.4V
  - 固定スレッショルド レベルは 100mV 刻みで利用可能
- 複数の出力トポロジ
  - DL:オープン ドレイン アクティブ LOW
  - PL:プッシュプル アクティブ LOW
  - PH:プッシュプル アクティブ HIGH
- 温度範囲:-40℃～+125℃
- パッケージ:1.5mm × 1.5mm WSON

2 アプリケーション

- 電気メーター
- ビル・オートメーション
- ボディ・コントロール・モジュール (BCM)
- データ・センターおよびエンタープライズ・コンピューティング
- ノートブック / デスクトップ PC、サーバー
- スマートフォン、ハンドヘルド製品
- 携帯用、バッテリ駆動機器
- ソリッドステート・ドライブ
- STB / DVR

3 概要

TPS3899 は、±0.5% のスレッショルド精度とプログラム可能なセンスおよびリセット時間遅延を持つ nano power 高精度電圧スーパーバイザで、6 ピンの省スペース 1.5mm × 1.5mm WSON パッケージに搭載されています。TPS3899 は、豊富な機能を持つ電圧スーパーバイザで、クラス最小のソリューション サイズを実現します。ヒステリシスに加えてプログラム可能な遅延が内蔵されているので、電圧レールやプッシュ ボタン信号を監視するときに誤リセット信号が発生することを防止できます。

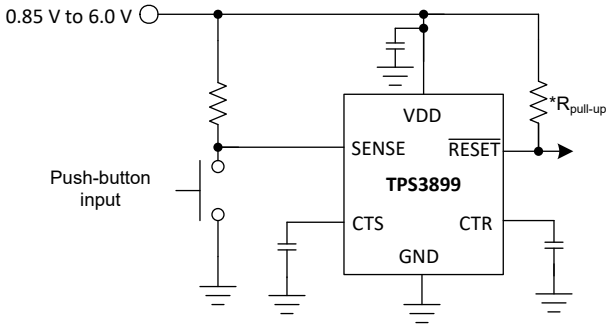
VDD ピンと SENSE ピンが別になっているので、高信頼性システムで求められる冗長性を実現できます。SENSE は VDD から分離されており、VDD 以外のレール電圧も監視できます。SENSE ピンは高インピーダンス入力なので外付け抵抗を使うこともできます。CTS と CTR は、リセット信号の立ち上がり / 立ち下がりエッジで遅延を調整するのに使います。CTS は、監視対象の電圧レールの電圧グリッチを無視するデバウンシング機能として機能し、また、システムを強制的にリセットするための「手動リセット」としても動作します。

TPS3899 は、高精度とクラス最高の機能をコンパクトなフォーム ファクタで実現するため、ファクトリ / ビル オートメーション、モーター駆動、コンシューマ製品などの広範な産業用 / バッテリ駆動アプリケーションに最適なソリューションです。このデバイスは、-40℃～+125℃ (T_A) の温度範囲にわたって完全に動作が規定されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3899	WSON (6) DSE	1.5mm × 1.5mm

1. 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照



*$R_{pull-up}$ is required for open-drain variants only

代表的なアプリケーション回路

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison

図 4-1 shows the device naming nomenclature of the TPS3899. For all possible output types and threshold voltages options, see Device Naming Convention for a more detailed explanation. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

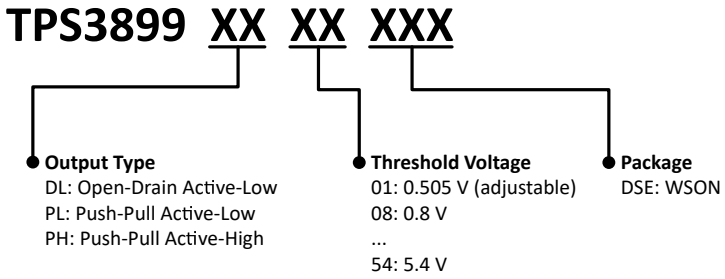

図 4-1. Device Naming Nomenclature

Pin Configuration and Functions

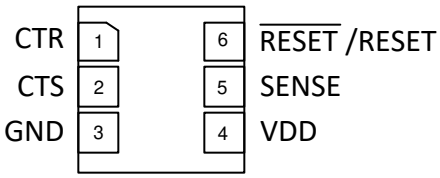

**図 5-1. DSE Package,
6 Pin,
TPS3899 Top View**

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTR	—	Capacitor programmable reset delay: The CTR pin offers a user-adjustable delay time when returning from reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to deassert.
2	CTS	—	Capacitor programmable sense delay: The CTS pin offers a user-adjustable delay time when asserting reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$/RESET delay time to assert.
3	GND	—	Ground
4	VDD	I	Supply voltage pin: Good analog design practice is to place a 0.1µF ceramic capacitor close to this pin.
5	SENSE	I	This pin is connected to the voltage that will be monitored for fixed variants or to a resistor divider for the adjustable variant. When the voltage on the SENSE pin transistions below the negative threshold voltage V_{IT-}, $\overline{\text{RESET}}$/RESET asserts to active logic after the sense delay set by CTS. When the voltage on the SENSE pin transistions above the positive threshold voltage $V_{IT-} + V_{HYS}$, $\overline{\text{RESET}}$/RESET releases to inactive logic (deasserts) after the reset delay set by CTR. For noisy applications, placing a 10nF to 100nF ceramic capacitor close to this pin may be needed for optimum performance.
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ active-low output that asserts to a logic low state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. $\overline{\text{RESET}}$ remains logic low (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires.
6	RESET	O	RESET active-high output that asserts to a logic high state after CTS delay when the monitored voltage on the SENSE pin is lower than the negative threshold voltage V_{IT-}. RESET remains logic high (asserted) until the SENSE input rises above $V_{IT-} + V_{HYS}$ and the CTR reset delay expires.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD, SENSE	–0.3	6.5	V
Voltage	CTR, CTS	–0.3	V_{DD}+0.3 (3)	V
Voltage	$\overline{\text{RESET}}$ (TPS389DL)	–0.3	6.5	V
	$\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH)	-0.3	V_{DD}+0.3 (3)	
Current	$\overline{\text{RESET}}$ pin and RESET pin		±20	mA
Temperature(2)	Operating ambient temperature, T_A	–40	125	°C
Temperature(2)	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD, SENSE	0		6	V
Voltage	CTR, CTS	0		VDD	V
Voltage	$\overline{\text{RESET}}$ (TPS3899DL)	0		6	V
	$\overline{\text{RESET}}$ (TPS3899PL), RESET (TPS3899PH)	0		VDD	
Current	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_A	Operating free air temperature	–40		125	°C
C_{CTR}	CTR pin capacitor range	0		10	µF
C_{CTS}	CTS pin capacitor range	0		10	µF

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5.4 Thermal Information

THERMAL METRIC(1)		TPS3899 DSE 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	214.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	153.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	112.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	111.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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5.5 Electrical Characteristics

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. V_{DD} ramp rate ≤ 1 V/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage (Open Drain Low and Push Pull Low)		0.85		6	V
V_{DD}	Input supply voltage (Push Pull High)		1		6	V
V_{IT-} (1)	Negative-going input threshold range	for all output configs	0.8		5.4	V
$V_{ADJ-VIT-}$	Negative-going input threshold for adjustable sense threshold version			0.505		V
V_{IT-} accuracy	Negative-going input threshold accuracy	V_{IT-} = 0.505 V (ADJ version) or 0.8 V to 1.7 V (Fixed threshold)	–2.5	±0.5	2.5	%
		V_{IT-} = 1.8 V to 5.4 V (Fixed threshold)	–2	±0.5	2	
V_{HYS}	Hysteresis on V_{IT-}	V_{IT-} = 0.505 V and 0.8 V	3	5	8	%
		V_{IT-} = 0.9 V to 5.4 V	3	5	7	%
I_{SENSE}	Current into Sense pin, fixed threshold version	V_{DD} = V_{SENSE} = 6 V		0.025	0.1	µA
	Current into Sense pin, ADJ version	V_{DD} = V_{SENSE} = 6 V		0.025	0.05	µA
I_{DD}	Supply current into VDD pin when sense pin is separate	V_{DD} = V_{SENSE} = 6 V V_{IT-} = 0.505 V and 0.8 V to 5.4 V		0.125	1	µA
V_{TH_CTS}	Voltage threshold to stop CTS capacitor charge and assert RESET			0.73 * V_{DD}		V
V_{TH_CTR}	Voltage threshold to stop CTR capacitor charge and deassert RESET			0.73 * V_{DD}		V
R_{CTS}	CTS pin internal pull up resistance			500		kΩ
R_{CTR}	CTR pin internal pull up resistance			500		kΩ
TPS3899DL (Open-drain active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6 V, T_A = –40°C to 85°C		10	100	nA
		V_{DD} = V_{PULLUP} = 6 V		10	350	nA
TPS3899PL (Push-pull active-low)						
V_{POR}	Power on reset voltage (2)	$V_{OL(max)}$ = 300 mV $I_{\overline{RESET}(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.85 V $I_{\overline{RESET}(Sink)}$ = 15 µA			300	mV
		V_{DD} = 3.3 V $I_{\overline{RESET}(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1.8 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{\overline{RESET}(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 6 V $I_{\overline{RESET}(Source)}$ = 2 mA	0.8V_{DD}			V

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5.5 Electrical Characteristics (続き)

CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. V_{DD} ramp rate ≤ 1 V/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TPS3899PH (Push-pull active-high)						
V_{POR}	Power on reset voltage(2)	$V_{OH(min)}$ = 0.8V_{DD} $I_{RESET\ (Source)}$ = 15 uA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 500 µA			300	mV
		V_{DD} = 6 V $I_{RESET(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	V_{DD} = 1V $I_{RESET(Sink)}$ = 15 µA	0.8V_{DD}			V
		V_{DD} = 1.5 V $I_{RESET(Sink)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{RESET(Sink)}$ = 2 mA	0.8V_{DD}			V

(1) V_{IT-} threshold voltage range from 0.8 V to 5.4 V (for DL, PL) and 1 to 5.4 V (for PH) in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) Minimum V_{DD} voltage level for a controlled output state. Below V_{POR}, the output cannot be determined.

5.6 Timing Requirements

At 0.85 V ≤ V_{DD} ≤ 6 V, CTR = CTS = Open, $\overline{\text{RESET}}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to V_{DD}, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range –40°C to 125°C, unless otherwise noted. V_{DD} ramp rate ≤ 1 V / µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay(1)	CTR pin = Open or NC			300	µs
$t_{D-SENSE}$	Detect time delay V_{DD} = (V_{IT+} + 10%) to (V_{IT-} – 10%)(2)	CTS pin = Open or NC		30	50	µs
		CTS pin = 10 nF		6.2		ms
		CTS pin = 1 µF		619		ms
t_D	Reset time delay	CTR pin = Open or NC		40	80	µs
		CTR pin = 10 nF (3)		6.2		ms
		CTR pin = 1 µF (3)		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(4)		10		µs

(1) When VDD starts from less than V_{POR} and then exceeds the specified minimum V_{DD}, reset is asserted till startup delay (t_{STRT}) + t_D delay based on capacitor on CTR pin. After this time, the device controls the RESET pin based on the SENSE pin voltage.
(2) t_{D_SENSE} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Ideal capacitor
(4) Overdrive % = [(V_{DD}/ V_{IT-}) - 1] × 100%

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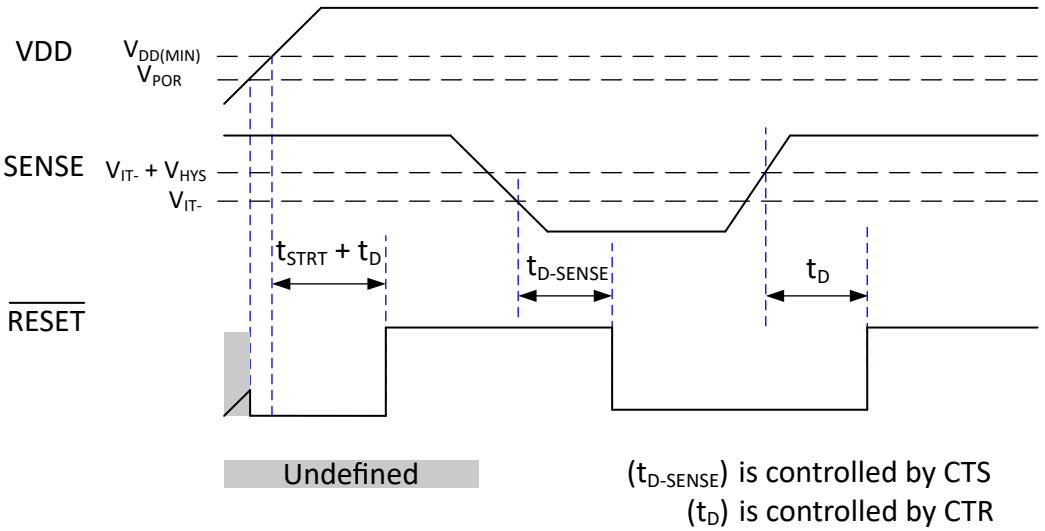
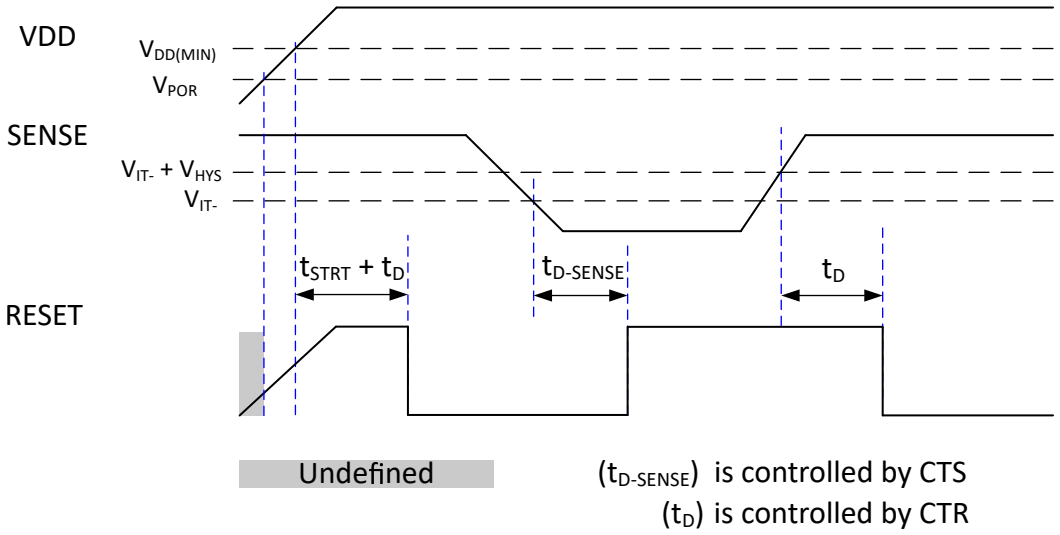
5.7 Timing Diagrams



(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

図 5-1. TPS3899DL01 and TPS3899PL01 Timing Diagram



(2) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to the CTR pin then t_D programmed time will be added to the startup time.

図 5-2. TPS3899PH01 Timing Diagram

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5.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3V, and $R_{pull-up}$ = 100kΩ, unless otherwise noted.

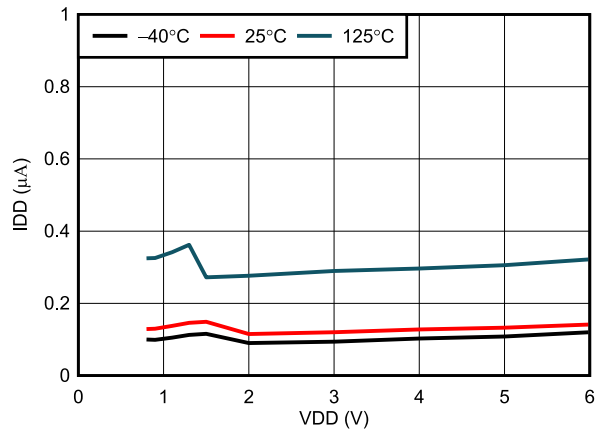

図 5-3. Supply Current vs Supply Voltage

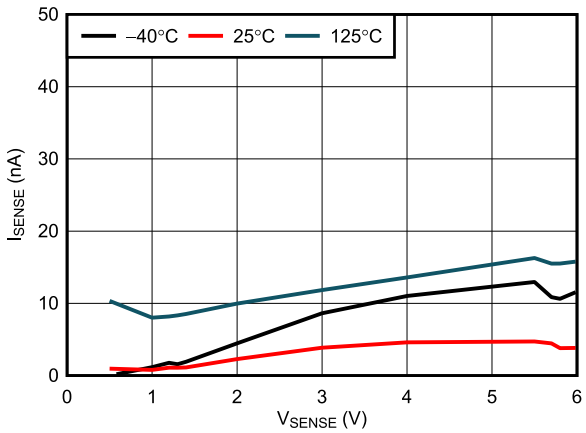

図 5-4. SENSE Current vs V_{SENSE}

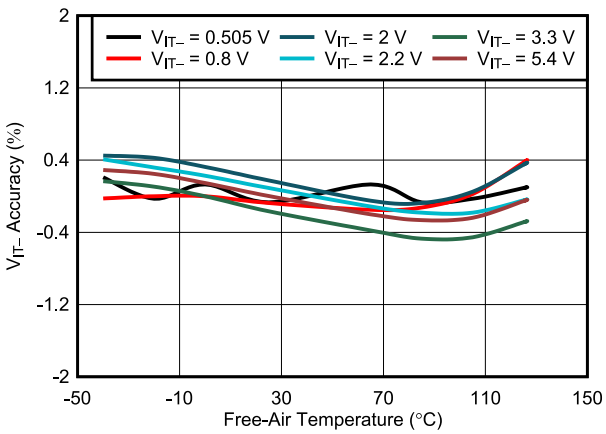

図 5-5. V_{IT-} Accuracy vs Temperature

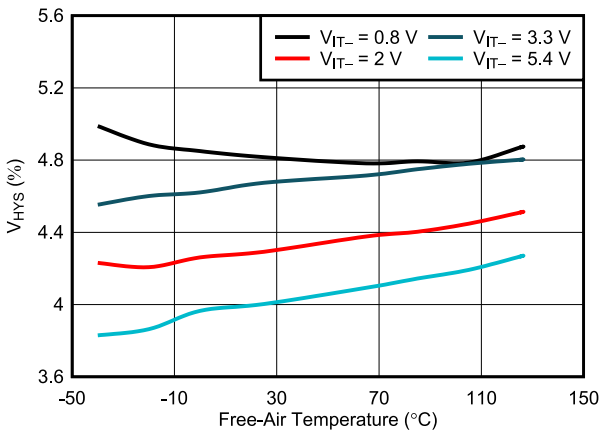

図 5-6. V_{HYS} vs Temperature

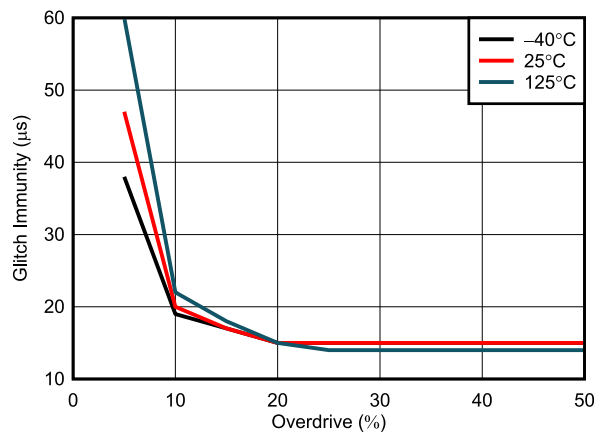

図 5-7. SENSE Glitch Immunity (V_{IT-}) vs Overdrive

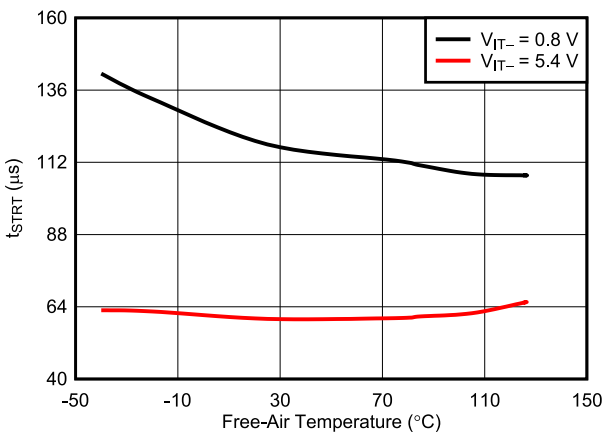

図 5-8. Startup Delay vs Temperature

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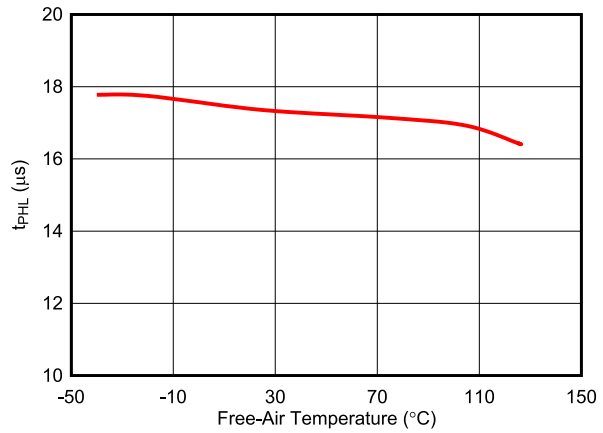
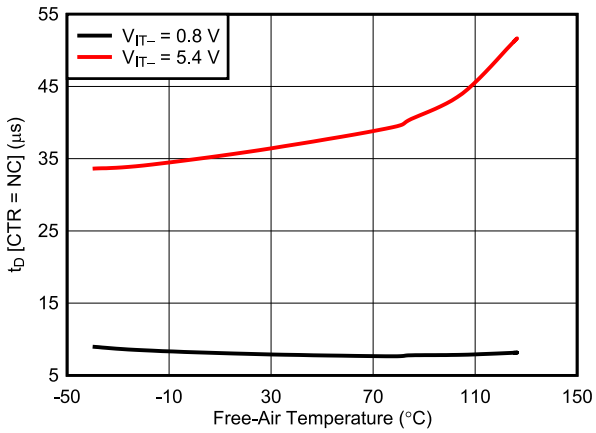
5.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3V, and $R_{pull-up}$ = 100kΩ, unless otherwise noted.



V_{DD} falling below V_{IT-}

図 5-9. Propagation Delay vs Temperature



CTR = OPEN

図 5-10. Reset Time Delay vs Temperature

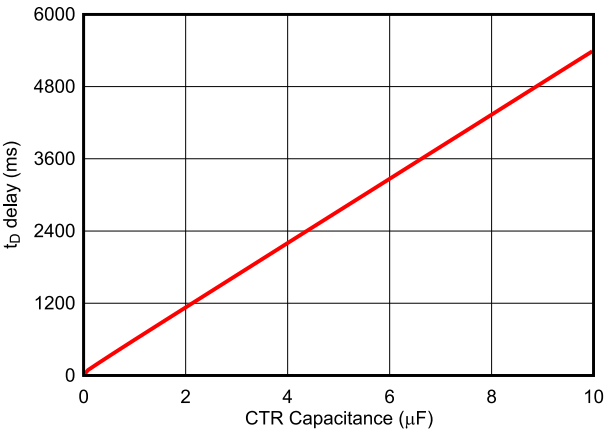
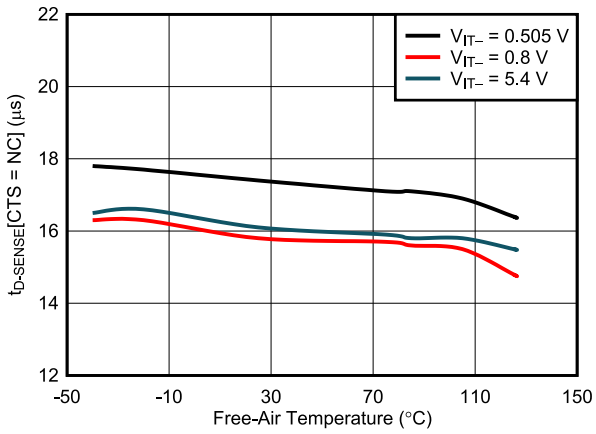


図 5-11. RESET Delay vs CTR Capacitance



CTS = OPEN

図 5-12. SENSE Delay vs Temperature

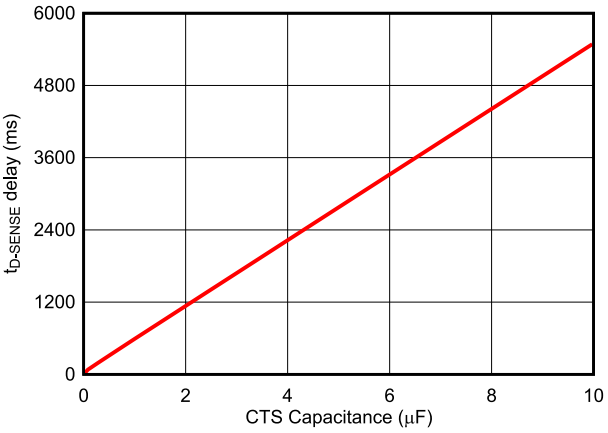


図 5-13. SENSE Delay vs CTS Capacitance

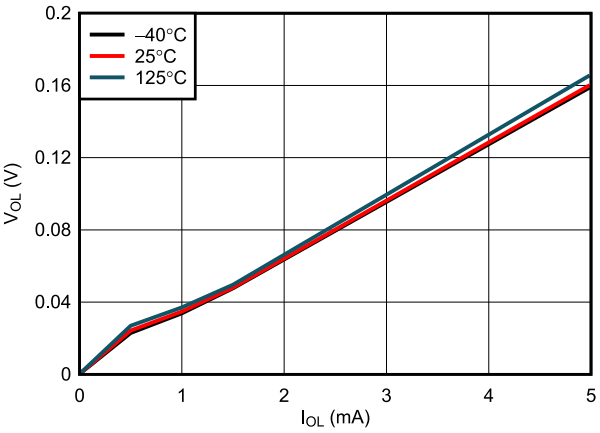


図 5-14. V_{OL} vs I_{OL}

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5.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3899 device. Test conditions are T_A = 25°C, V_{DD} = 3.3V, and $R_{pull-up}$ = 100kΩ, unless otherwise noted.

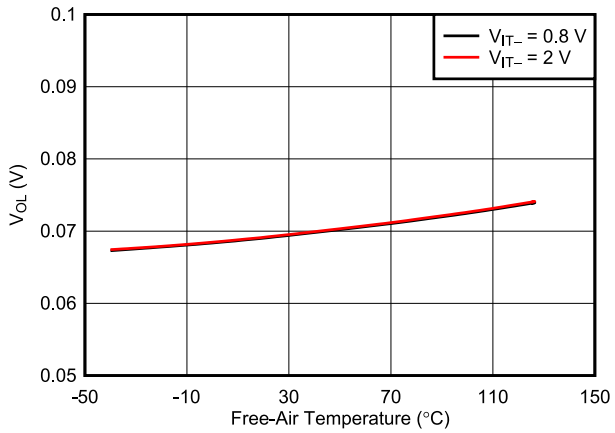

図 5-15. V_{OL} vs Temperature

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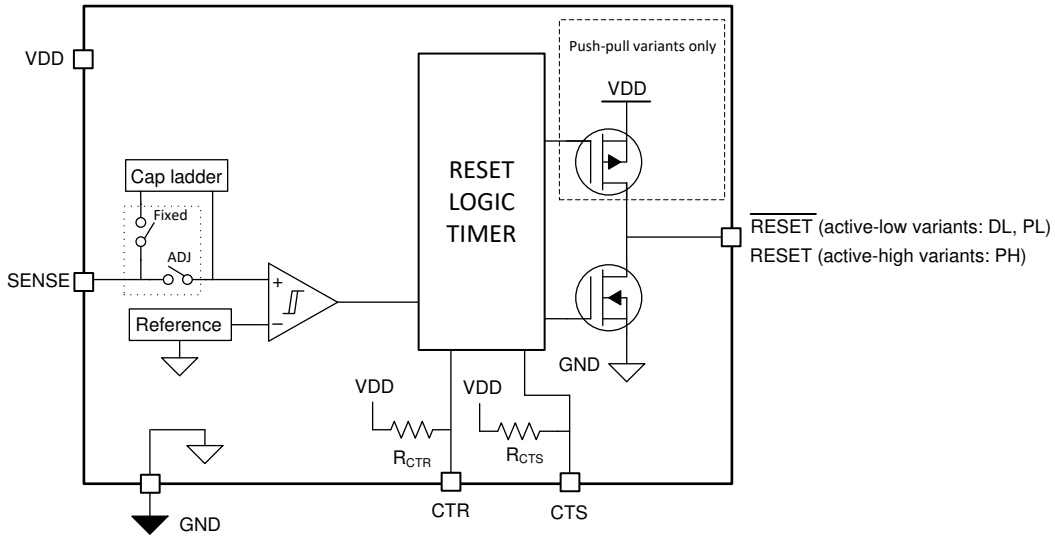
6 Detailed Description

6.1 Overview

The TPS3899 voltage supervisor with push-button monitor asserts a $\overline{\text{RESET}}$/RESET signal when the SENSE pin voltage drops below V_{IT-} for the duration of the sense delay set by CTS. If the SENSE pin voltage rises above V_{IT-} + V_{HYS} before the sense delay expires, the $\overline{\text{RESET}}$/RESET pin does not assert. When asserted, the $\overline{\text{RESET}}$/RESET output remains asserted until SENSE voltage returns above V_{IT-} + V_{HYS} for the duration of the reset delay set by CTR. If the SENSE pin voltage falls below V_{IT-} before the reset delay expires while $\overline{\text{RESET}}$ is asserted, $\overline{\text{RESET}}$/RESET will remain asserted.

Like most voltage supervisors, the TPS3899 includes a reset delay t_D to provide time for the power and clocks to settle before letting the processor out of reset. At power up, the circuits inside the TPS3899 need additional time to start the reset delay timer after its power supply VDD has reached minimum $V_{DD(MIN)}$ for these circuits to start operating properly. This additional time is specified with the parameter start-up delay t_{STRT}. 図 5-1 shows the timing diagram indicating this additional delay. After VDD is stable and above $V_{DD(MIN)}$ subsequent changes of the sense voltage across the threshold voltage will trigger reset after only the reset delay. The reset time delay t_D is set by a capacitor on the CTR pin. The start-up delay has a max spec limit of 300µs for a ramp rate of V_{DD} ≤ 1V/µS.

6.2 Functional Block Diagram



6.3 Feature Description

The combination of user-adjustable sense delay time via CTS and reset delay time via CTR with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages V_{IT-} can be factory set from 0.8V to 5.4V in steps of 100mV [1.1V to 5.4V for the -PH (push-pull active high) variants]. CTS and CTR pins allow the sense delay and reset delay to be set to typical values of 30µs and 40µs, respectively, by leaving these pins floating. External capacitors can be placed on the CTS and CTR pins to program the sense and reset delays independently.

6.3.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

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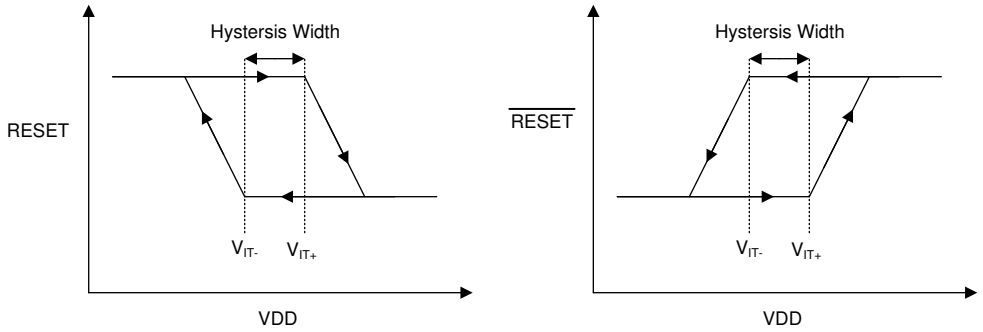

図 6-1. Hysteresis Diagram

6.3.2 User-Programmable Sense and Reset Time Delay

The sense delay corresponds to the configuration of CTS and the reset delay corresponds to the configuration of CTR. The sense and reset time delay can be set to a minimum value of 50µs and 80µs by leaving the CTS and CTR pins floating respectively, or a maximum value of approximately 6.5 seconds by connecting 10µF delay capacitor.

The relationship between external capacitor (C_{CT_EXT}) in Farads at CTS or CTR pins and the time delay in seconds is given by 式 1.

$$t_D = -\ln(0.27) \times R_{CT} \times C_{CT_EXT} + t_{D\ (CTS\ or\ CTR\ =\ OPEN)} \quad (1)$$

式 1 is simplified to 式 2 and 式 3 by plugging R_{CT} and $t_{D\ (CTS\ or\ CTR\ =\ OPEN)}$ given in セクション 5.5 and セクション 5.6 section:

$$t_{D\text{-}SENSE} = 654666 \times C_{CTS_EXT} + 50\mu s \quad (2)$$

$$t_D = 654666 \times C_{CTR_EXT} + 80\mu s \quad (3)$$

式 4 and 式 5 solves for both external capacitor values (C_{CTS_EXT}) and (C_{CTR_EXT}) in units of Farads where $t_{D\text{-}SENSE}$ and t_D are in units of seconds

$$C_{CTS_EXT} = (t_{D\text{-}SENSE} - 50\mu s) \div 654666 \quad (4)$$

$$C_{CTR_EXT} = (t_D - 80\mu s) \div 654666 \quad (5)$$

The sense or reset delay varies according to three variables: the external capacitor (C_{CT_EXT}), CTS and CTR pin internal resistance (R_{CT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is show in 式 6 and 式 7 .

$$t_{D\text{-}SENSE(min)} = -\ln(0.29) \times R_{CT\ (min)} \times C_{CT_EXT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (6)$$

$$t_{D\text{-}SENSE(max)} = -\ln(0.25) \times R_{CT\ (max)} \times C_{CT_EXT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (7)$$

The recommended maximum sense and reset delay capacitors for the TPS3899 is limited to 10µF as this makes sure there is enough time for either capacitors to fully discharge when a voltage fault occurs. When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before either delay capacitors discharges completely, both delays can be shorter than expected. The capacitors can begin charging from a voltage above zero and resulting in shorter than expected time delays. Larger delay capacitors can be used so long as the capacitors have enough time to fully discharge during the duration of the voltage fault. To make sure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

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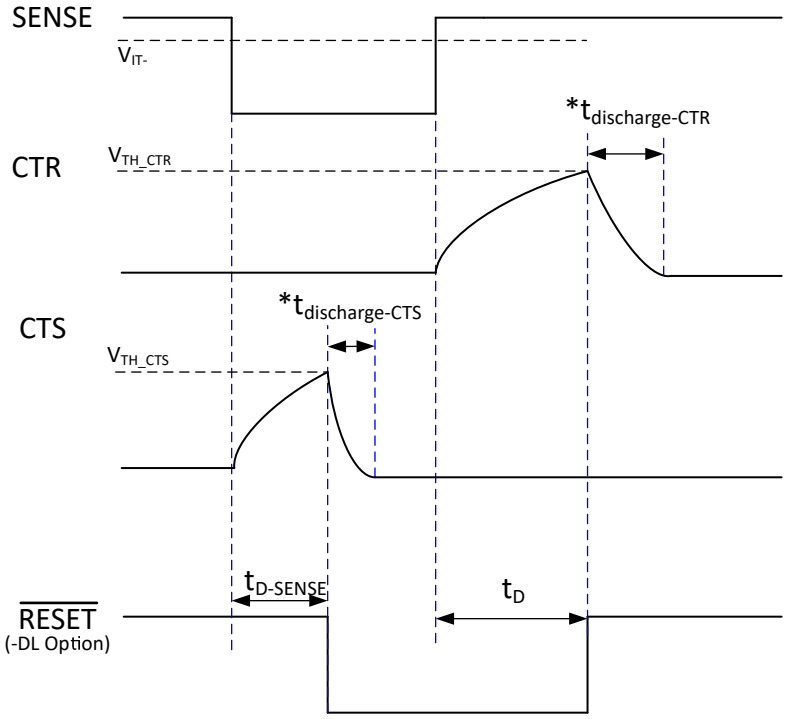
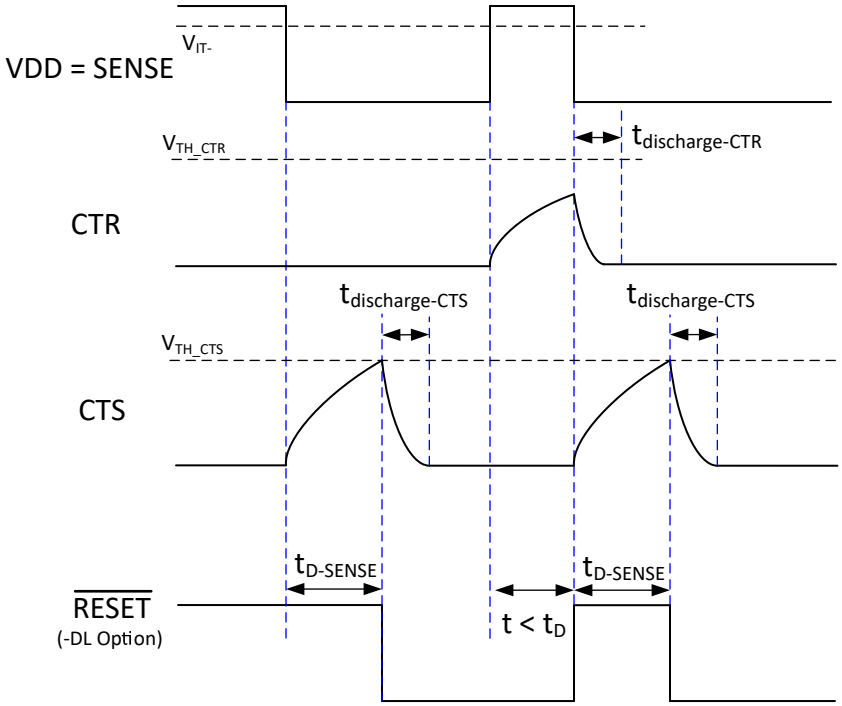
図 6-2 shows the charge and discharge behavior on CTS and CTR that defines the sense and reset delays respectively. When SENSE transitions below V_{IT-}, the capacitor connected to CTS begins to charge. Once the CTS capacitor charges to an internal threshold shown as V_{TH_CTS}, $\overline{RESET}$ transitions to active-low logic state and the CTS capacitor then begins to discharge immediately. When SENSE transitions above V_{IT-} + V_{HYS}, the capacitor connected to CTR begins to charge. Once the CTR capacitor charges to the internal threshold V_{TH_CTR}, $\overline{RESET}$ releases back to inactive logic high state and the CTR capacitor begins to discharge immediately. Please note that for active-high variants, RESET follows the inverse behavior of $\overline{RESET}$.



* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

図 6-2. CTS and CTR Charge and Discharge Behavior Relative to SENSE and $\overline{RESET}$

図 6-3 shows the charge and discharge behavior on CTS and CTR where the monitored voltage is VDD. Similar to 図 6-2, 図 6-3 illustrates a SENSE signal that is transitioning below V_{IT-} before the CTR capacitor reaches to an internal threshold voltage V_{TH_CTR} and t < t_D. The result of the CTR capacitor not reaching the internal threshold voltage V_{TH_CTR} is $\overline{\text{RESET}}$ becomes deasserted. Once $\overline{\text{RESET}}$ is deasserted, charging beings for the CTS capacitor. When the CTS voltage reaches the internal threshold V_{TH_CTS}, $\overline{\text{RESET}}$ becomes asserted. This phenomenon is caused by the SENSE falling edge triggering the discharging of the CTR capacitor and producing a deassert signal on the $\overline{\text{RESET}}$ output.



* $t_{discharge-CTS}$ and $t_{discharge-CTR}$: To ensure the capacitors are fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

図 6-3. CTS and CTR Charge and Discharge Behavior Relative to VDD, SENSE and $\overline{\text{RESET}}$

6.3.3 $\overline{\text{RESET}}$/RESET Output

Upon power up, $\overline{\text{RESET}}$/RESET begins asserted and remains asserted until the SENSE pin voltage rises above the positive voltage threshold V_{IT-} + V_{HYS} for the duration of the reset delay set by CTR. After the SENSE pin voltage is above V_{IT-} + V_{HYS} for the reset delay, $\overline{\text{RESET}}$/RESET deasserts. $\overline{\text{RESET}}$/RESET remains deasserted long as the SENSE pin voltage is above the positive threshold. If the SENSE pin voltage falls below the negative threshold (V_{IT-}) for the duration of the sense delay set by CTS, then $\overline{\text{RESET}}$/RESET is asserted.

An external pull-up resistor is required for the open-drain variants. Connect the external pull-up resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$/RESET can be pulled up to any voltage up to 6.0V, independent of the device supply voltage.

6.3.4 SENSE Input

The SENSE input can vary from 0V to 6.0V, regardless of the device supply voltage used. The SENSE pin is used to monitor a critical voltage rail or push-button input. If the voltage on this pin drops below V_{IT-}, then $\overline{\text{RESET}}$/RESET is asserted after the sense delay time set by CTS. When the voltage on the SENSE pin rises above the positive threshold voltage V_{IT-} + V_{HYS}, $\overline{\text{RESET}}$/RESET deasserts after the reset delay time set by CTR. The internal comparator has built-in hysteresis to make sure well-defined $\overline{\text{RESET}}$/RESET assertions and deassertions even when there are small changes on the voltage rail being monitored.

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The TPS3899 device is relatively immune to short transients on the SENSE pin. Glitch immunity ($t_{GI_V_{IT-}SENSE}$), found in セクション 5.6, is dependent on threshold overdrive, as illustrated in 図 5-7. Although not required in most cases, for noisy applications, good analog design practice is to place a 10nF to 100nF bypass capacitor at the SENSE input to reduce sensitivity to transient voltages on the monitored signal.

6.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3899 is immune to short voltage transient spikes on the input pins. To further improve the noise immunity on the SENSE pin, placing a 10nF to 100nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.

Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much V_{SENSE} exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 8.

$$\text{Overdrive} = | ((V_{SENSE} / V_{IT-}) - 1) \times 100\% | \quad (8)$$

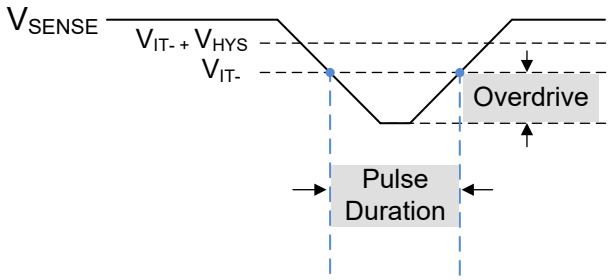

図 6-4. Overdrive vs Pulse Duration

6.4 Device Functional Modes

表 6-1 summarizes the various functional modes of the device.

表 6-1. Truth Table

V_{DD}	SENSE(1)	$\overline{RESET}$	RESET
$V_{DD} < V_{POR}$	—	Undefined	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}$ (2)	—	L	H
$V_{DD} \geq V_{DD(MIN)}$	$V_{SENSE} < V_{IT-}$	L	H
$V_{DD} \geq V_{DD(MIN)}$	$V_{SENSE} > V_{IT-} + V_{HYS}$	H	L

(1) SENSE pin voltage must be less than V_{IT-} for the sense delay set by CTS or greater than $V_{IT-} + V_{HYS}$ for the reset delay set by CTR before RESET transistions

(2) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and $\overline{RESET}$ is held logic low (RESET is held logic high) until V_{DD} falls below V_{POR} at which the $\overline{RESET}$/RESET output is undefined.

6.4.1 Normal Operation ($V_{DD} > V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$/RESET pin is determined by the voltage on the SENSE pin and the sense delay and reset delay set by CTS and CTR respecively.

6.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ($V_{POR} < V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage V_{POR}, the $\overline{RESET}$/RESET signal is asserted regardless of the voltage on the SENSE pin.

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6.4.3 Below Power-On-Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR}, the device does not have enough voltage to internally pull the asserted $\overline{\text{RESET}}$ output low and $\overline{\text{RESET}}$ is undefined. RESET is also undefined and can pull up to V_{DD} or to the pull-up voltage. Neither output can be relied upon for proper device function.

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7 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

7.2 Typical Application

Design 1: Adjustable Voltage Supervisor with Push-Button Functionality

A typical application for the TPS3899 is voltage rail monitoring with push-button functionality and specific timing requirements.

In this design application, the TPS3899DL01 is being used to monitor a 3.3V power rail and triggers a reset when the voltage drops below 2.9V or when the push-button is pressed. The reset output connects to an MCU for system resetting or servicing the push-button.

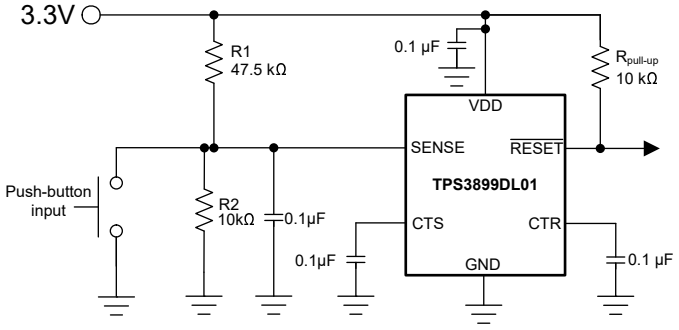

図 7-1. Design 1 - Adjustable Voltage Supervisor with Push-Button Functionality Circuit

7.2.1 Design Requirements

The design requirements, described in 表 7-1, for this design has a defined reset threshold voltage of 2.9V, a sense delay of 60ms, a reset delay of 60ms, and an output current no larger than 500µA.

表 7-1. Design Requirements

PARAMETER	DESIGN REQUIREMENTS	DESIGN RESULTS
Reset Asserting	Reset needs to assert when under the reset condition of a button press or VDD ≤ 2.9V.	Reset asserts when under the reset condition of a button press or VDD ≤ 2.93V.
Reset Asserting Timing	Reset output needs to assert when the reset conditions are met for 60ms, and needs to de-assert after 60ms of no reset conditions.	Reset output asserts when the reset conditions are met for 62ms and deasserts after 62ms of no reset conditions.
Output Current	The output current must not exceed 500µA.	The output current is 300µA under the reset condition.

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7.2.2 Detailed Design Procedure

The TPS3899DL01 can monitor any voltage above 0.505V using an external voltage divider. This device has a negative going input threshold voltage of 0.505V; however, the design needs to assert a reset when VDD drops below 2.9V. By using a resistor divider (R1 = 47.5kΩ, R2 = 10kΩ) the negative going threshold voltage becomes 2.93V. The device's positive going voltage threshold is V_{IT-} + V_{HYS}. The typical V_{HYS} is 25.5mV. This in combination with the resistor divider makes the design's positive going threshold voltage equal to 3.08V. If VDD falls below 2.93V for the duration of sense delay ($t_{D-SENSE}$), the reset asserts. If VDD rises above 3.08V for the duration of reset delay (t_D), the reset deasserts. See 図 7-2 for a timing diagram detailing the voltage levels and reset assertion/deassertion conditions.

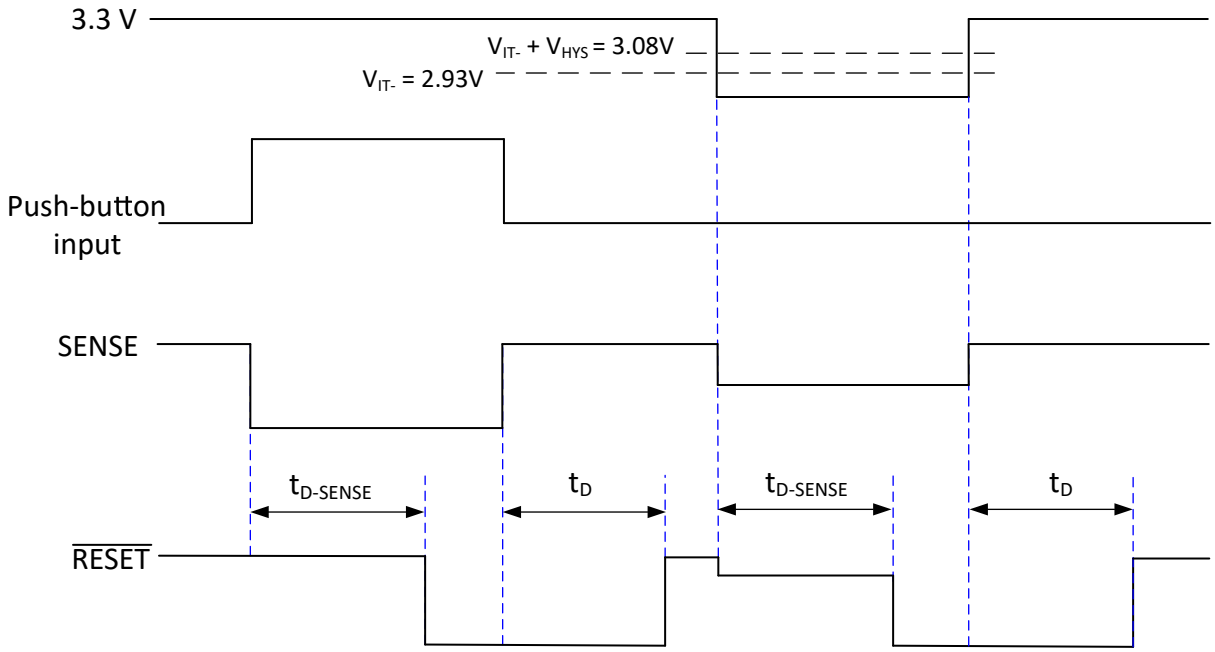

図 7-2. Design 1 Timing Diagram

This design also enters a reset condition when the push-button (PB) is asserted. The push-button is tied to ground and when pressed drops the SENSE voltage to 0V, making the device assert a reset. As a good analog practice, a 0.1µF capacitor was also placed on VDD.

The desired reset timing conditions are sense delay time of 60ms (the time to trigger a reset) and a reset delay time of 60ms (the time to recover from a reset). Using 式 4 and 式 5, respectively, to solve for CTS and CTR capacitor values, CTS = 0.1µF and CTR = 0.1µF. These capacitor values give a nominal sense delay time of 62ms and nominal reset delay time of 62ms. 図 7-3 and
図 7-4 are the results of the described application where the measured sense and reset delay time are shown respectively.

For the requirement of a maximum output current, an external pull-up resistor needs to be selected so that the current through the external pull-up resistor exceeds no more than 500µA. When the reset output is low, the voltage drop across the external pull-up resistor is equal to VDD. Ohm’s law is used to calculate the minimum resistor value. The resistor needs to be greater than 6kΩ to pull less than 500µA in the reset asserted low condition. A resistor value of 10kΩ was selected to accomplish this.

Note that this design does not account for tolerances.

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7.2.3 Application Curves

図 7-3. Sense Delay

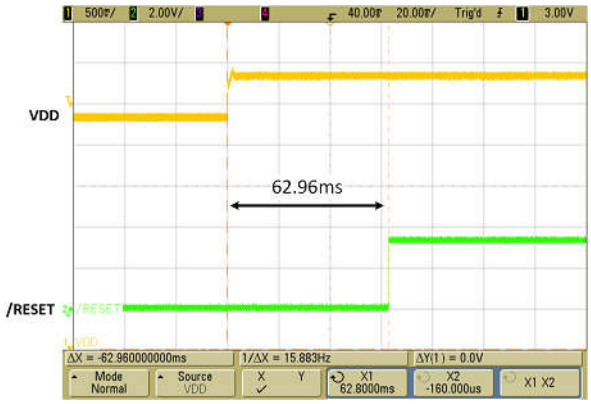

図 7-4. Reset Delay

7.2.4 Power Supply Recommendations

The TPS3899 is designed to operate from an input supply with a voltage range between 0.85V and 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin. Also, placing a 10nF to 100nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. This device has a 6.5V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5V, additional precautions must be taken.

7.2.5 Layout

7.2.5.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1µF ceramic capacitor near the VDD pin. If a capacitor is not connected to the CTS or CTS pins, then minimize parasitic capacitance on this pin so the sense delay or reset delay times are not adversely affected. For fixed voltage threshold devices, good analog design practice is to place a 0.1µF ceramic capacitor near the SENSE pin.

7.2.5.2 Layout Example

The layout example in 図 7-5 shows how the TPS3899 is laid out on a printed circuit board (PCB) with a user-defined sense delay and reset delay.

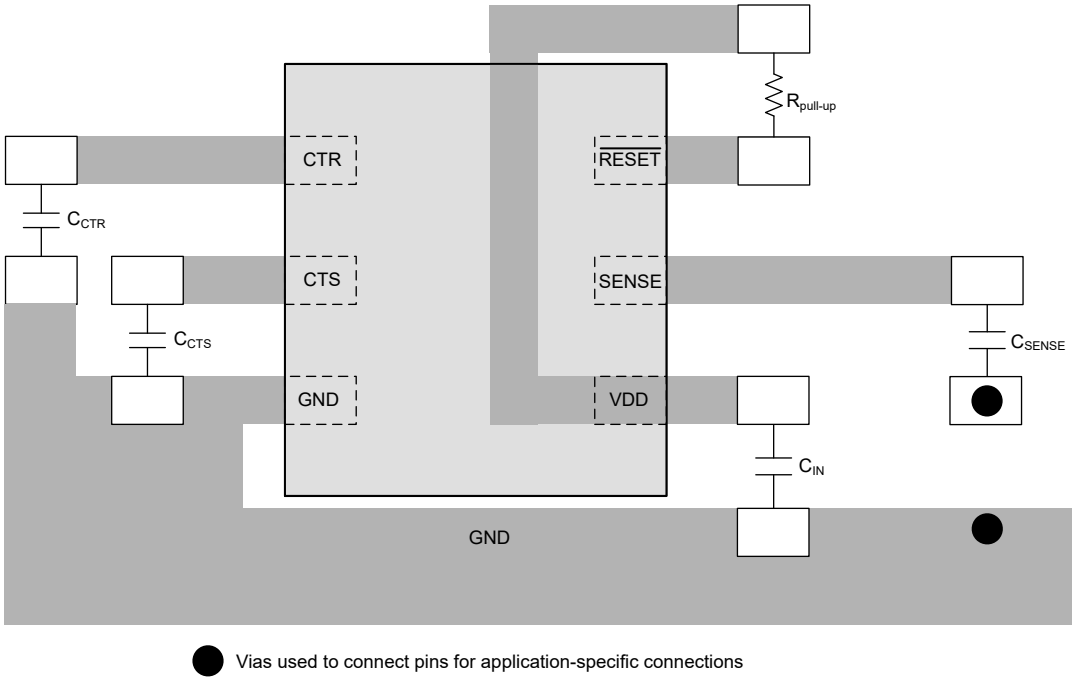

図 7-5. Recommended Layout

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

図 4-1 in Device Comparison shows how to decode the function of the device based on its part number shown in 表 8-1.

表 8-1. Device Naming Convention

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL01DSE	TPS3899PL01DSE	TPS3899PH01DSE	0.505
TPS3899DL08DSE	TPS3899PL08DSE	N/A	0.80
TPS3899DL09DSE	TPS3899PL09DSE	N/A	0.90
TPS3899DL10DSE	TPS3899PL10DSE	N/A	1.00
TPS3899DL11DSE	TPS3899PL11DSE	TPS3899PH11DSE	1.10
TPS3899DL12DSE	TPS3899PL12DSE	TPS3899PH12DSE	1.20
TPS3899DL13DSE	TPS3899PL13DSE	TPS3899PH13DSE	1.30
TPS3899DL14DSE	TPS3899PL14DSE	TPS3899PH14DSE	1.40
TPS3899DL15DSE	TPS3899PL15DSE	TPS3899PH15DSE	1.50
TPS3899DL16DSE	TPS3899PL16DSE	TPS3899PH16DSE	1.60
TPS3899DL17DSE	TPS3899PL17DSE	TPS3899PH17DSE	1.70
TPS3899DL18DSE	TPS3899PL18DSE	TPS3899PH18DSE	1.80
TPS3899DL19DSE	TPS3899PL19DSE	TPS3899PH19DSE	1.90
TPS3899DL20DSE	TPS3899PL20DSE	TPS3899PH20DSE	2.00
TPS3899DL21DSE	TPS3899PL21DSE	TPS3899PH21DSE	2.10
TPS3899DL22DSE	TPS3899PL22DSE	TPS3899PH22DSE	2.20
TPS3899DL23DSE	TPS3899PL23DSE	TPS3899PH23DSE	2.30
TPS3899DL24DSE	TPS3899PL24DSE	TPS3899PH24DSE	2.40
TPS3899DL25DSE	TPS3899PL25DSE	TPS3899PH25DSE	2.50
TPS3899DL26DSE	TPS3899PL26DSE	TPS3899PH26DSE	2.60
TPS3899DL27DSE	TPS3899PL27DSE	TPS3899PH27DSE	2.70
TPS3899DL28DSE	TPS3899PL28DSE	TPS3899PH28DSE	2.80
TPS3899DL29DSE	TPS3899PL29DSE	TPS3899PH29DSE	2.90
TPS3899DL30DSE	TPS3899PL30DSE	TPS3899PH30DSE	3.00
TPS3899DL31DSE	TPS3899PL31DSE	TPS3899PH31DSE	3.10
TPS3899DL32DSE	TPS3899PL32DSE	TPS3899PH32DSE	3.20
TPS3899DL33DSE	TPS3899PL33DSE	TPS3899PH33DSE	3.30
TPS3899DL34DSE	TPS3899PL34DSE	TPS3899PH34DSE	3.40
TPS3899DL35DSE	TPS3899PL35DSE	TPS3899PH35DSE	3.50
TPS3899DL36DSE	TPS3899PL36DSE	TPS3899PH36DSE	3.60
TPS3899DL37DSE	TPS3899PL37DSE	TPS3899PH37DSE	3.70
TPS3899DL38DSE	TPS3899PL38DSE	TPS3899PH38DSE	3.80

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表 8-1. Device Naming Convention (続き)

ORDERABLE DEVICE NAME			THRESHOLD VOLTAGE (V)
-DL (OPEN-DRAIN ACTIVE-LOW)	-PL (PUSH-PULL ACTIVE-LOW)	-PH (PUSH-PULL ACTIVE-HIGH)	
TPS3899DL39DSE	TPS3899PL39DSE	TPS3899PH39DSE	3.90
TPS3899DL40DSE	TPS3899PL40DSE	TPS3899PH40DSE	4.00
TPS3899DL41DSE	TPS3899PL41DSE	TPS3899PH41DSE	4.10
TPS3899DL42DSE	TPS3899PL42DSE	TPS3899PH42DSE	4.20
TPS3899DL43DSE	TPS3899PL43DSE	TPS3899PH43DSE	4.30
TPS3899DL44DSE	TPS3899PL44DSE	TPS3899PH44DSE	4.40
TPS3899DL45DSE	TPS3899PL45DSE	TPS3899PH45DSE	4.50
TPS3899DL46DSE	TPS3899PL46DSE	TPS3899PH46DSE	4.60
TPS3899DL47DSE	TPS3899PL47DSE	TPS3899PH47DSE	4.70
TPS3899DL48DSE	TPS3899PL48DSE	TPS3899PH48DSE	4.80
TPS3899DL49DSE	TPS3899PL49DSE	TPS3899PH49DSE	4.90
TPS3899DL50DSE	TPS3899PL50DSE	TPS3899PH50DSE	5.00
TPS3899DL51DSE	TPS3899PL51DSE	TPS3899PH51DSE	5.10
TPS3899DL52DSE	TPS3899PL52DSE	TPS3899PH52DSE	5.20
TPS3899DL53DSE	TPS3899PL53DSE	TPS3899PH53DSE	5.30
TPS3899DL54DSE	TPS3899PL54DSE	TPS3899PH54DSE	5.40

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 サポート・リソース

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8.5 静電気放電に関する注意事項

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

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9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (January 2022) to Revision C (January 2024)	Page
• Updated equations in User-Programmable Sense and Reset Time Delay section	14

Changes from Revision A (December 2020) to Revision B (January 2022)	Page
• 機能安全対応を追加	1
• Changed IDD from 1.2µA to 1µA	5

Changes from Revision * (September 2020) to Revision A (November 2020)	Page
• APL から RTM へのリリース	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3899DL01DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	KH
TPS3899DL01DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KH
TPS3899DL01DSERG4	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KH
TPS3899DL01DSERG4.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	KH
TPS3899DL08DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LJ
TPS3899DL08DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LJ
TPS3899DL09DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M3
TPS3899DL09DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M3
TPS3899DL10DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LS
TPS3899DL10DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LS
TPS3899DL11DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LZ
TPS3899DL11DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LZ
TPS3899DL13DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX
TPS3899DL13DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LX
TPS3899DL14DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN
TPS3899DL14DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LN
TPS3899DL15DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL
TPS3899DL15DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LL
TPS3899DL20DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M1
TPS3899DL20DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M1
TPS3899DL22DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP
TPS3899DL22DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LP
TPS3899DL26DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV
TPS3899DL26DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV
TPS3899DL28DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LI
TPS3899DL28DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LI
TPS3899DL29DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LK
TPS3899DL29DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LK
TPS3899DL30DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3899DL30DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM
TPS3899DL31DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M6
TPS3899DL31DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M6
TPS3899DL35DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LT
TPS3899DL35DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LT
TPS3899DL41DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LU
TPS3899DL41DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LU
TPS3899DL43DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2
TPS3899DL43DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	M2
TPS3899PL31DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH
TPS3899PL31DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LH
TPS3899PL42DSER	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LG
TPS3899PL42DSER.A	Active	Production	WSON (DSE) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LG

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS3899 :

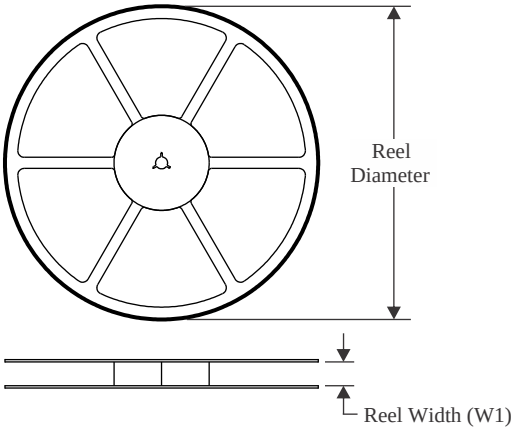
- Automotive : TPS3899-Q1

NOTE: Qualified Version Definitions:

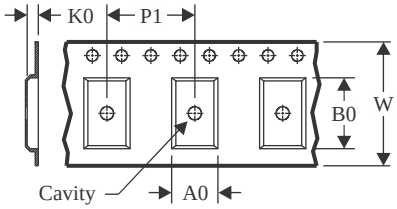
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

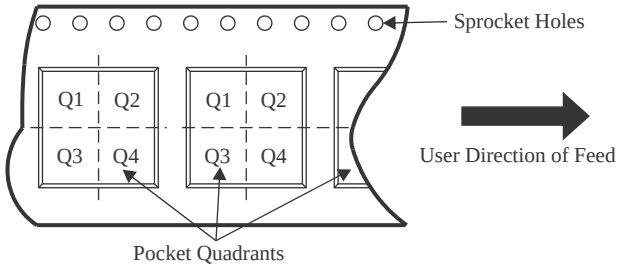


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

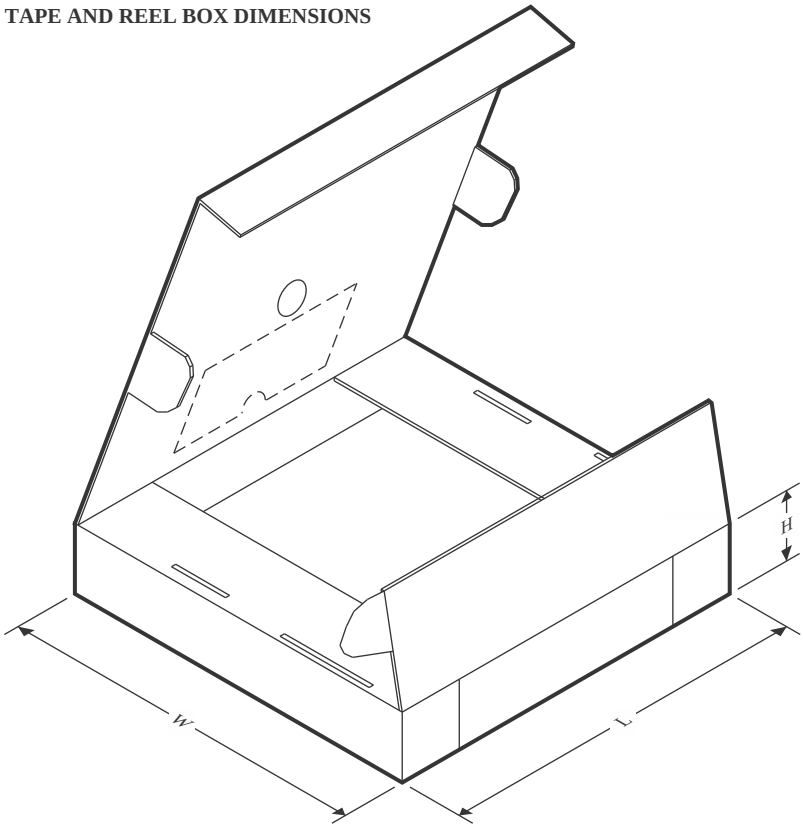


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3899DL01DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL01DSERG4	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL08DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL09DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL10DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL11DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL13DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL14DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL15DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL20DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL22DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL26DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL28DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL29DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL30DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL31DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3899DL35DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL41DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899DL43DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899PL31DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2
TPS3899PL42DSER	WSON	DSE	6	3000	180.0	8.4	1.75	1.75	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3899DL01DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL01DSERG4	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL08DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL09DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL10DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL11DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL13DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL14DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL15DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL20DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL22DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL26DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL28DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL29DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL30DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL31DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL35DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899DL41DSER	WSON	DSE	6	3000	210.0	185.0	35.0

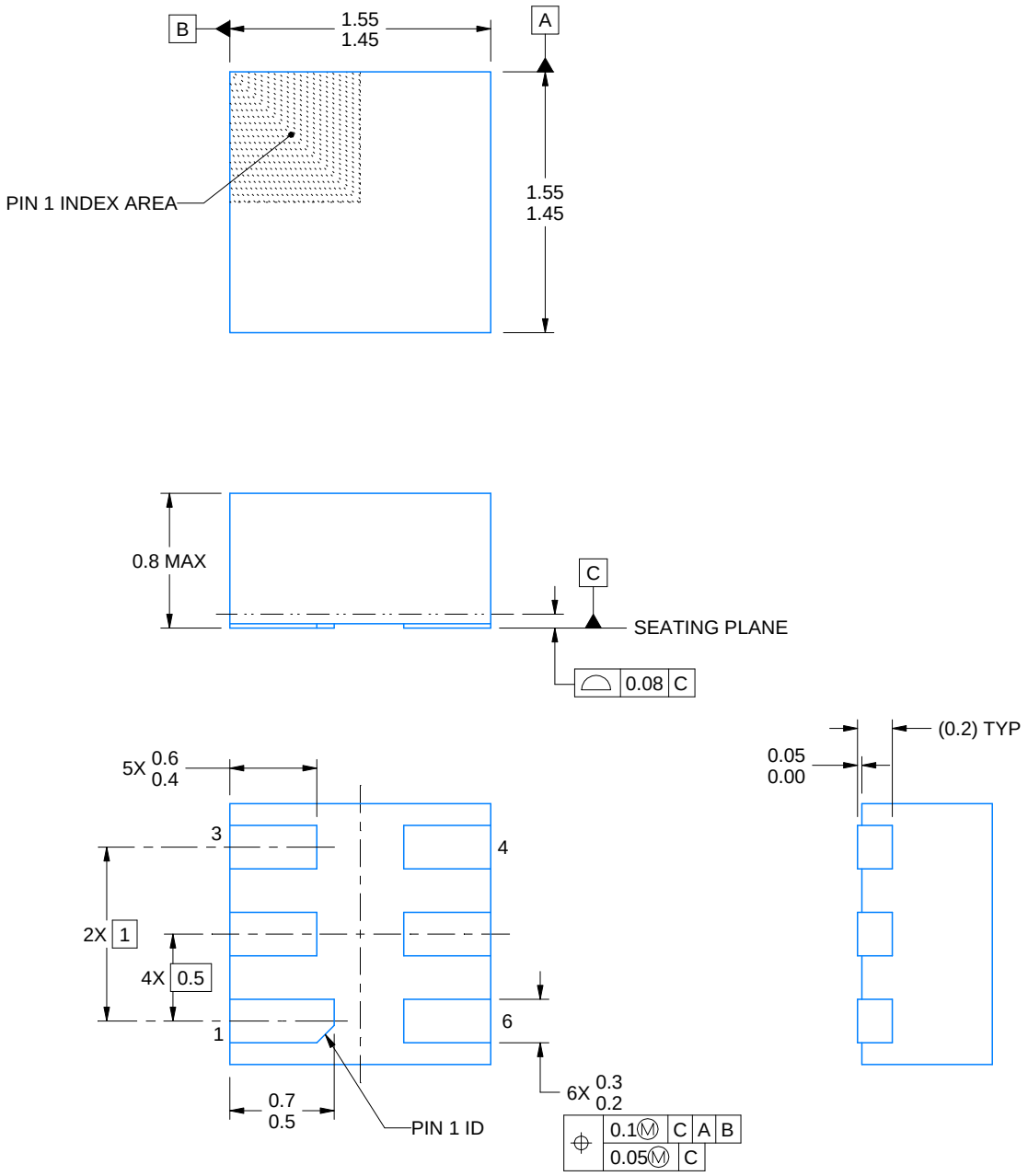
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3899DL43DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899PL31DSER	WSON	DSE	6	3000	210.0	185.0	35.0
TPS3899PL42DSER	WSON	DSE	6	3000	210.0	185.0	35.0

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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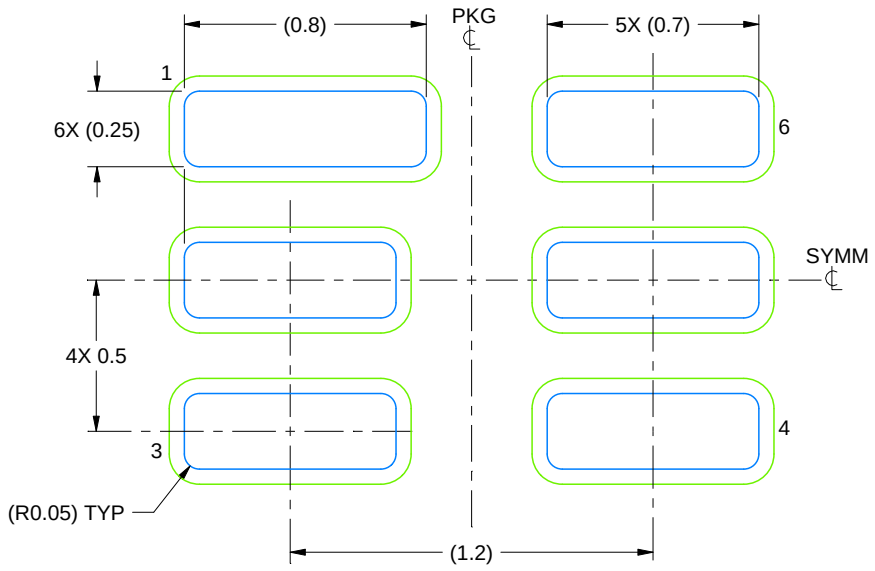
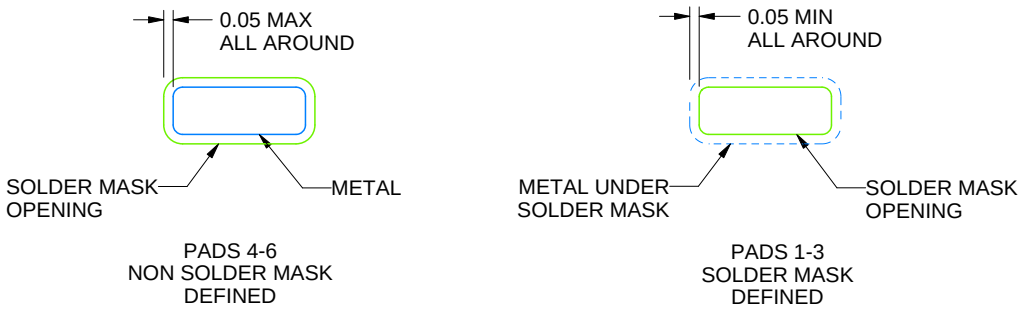
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS

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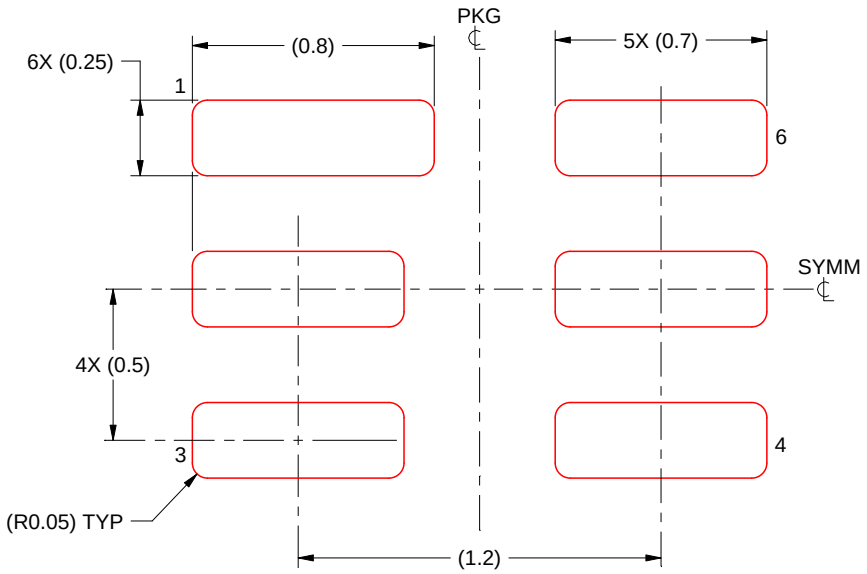
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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