TPS54318 2.95V～6V入力、3A出力、2MHz、同期整流降圧型 SWIFT™コンバータ

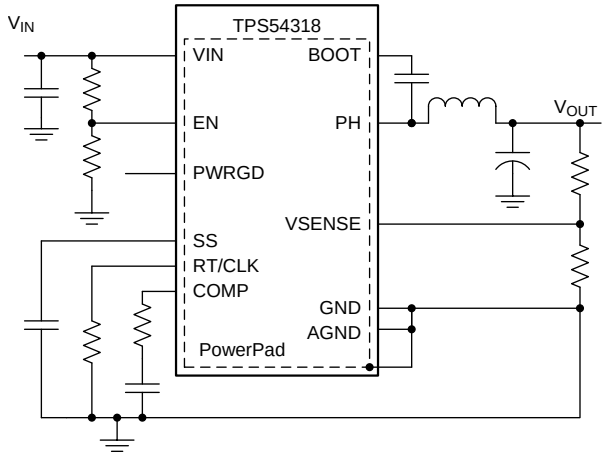
1 特長

- 2つの30mΩ (標準値) MOSFETにより3Aの負荷で高効率を実現
- スイッチング周波数: 200kHz～2MHz
- 温度範囲内での基準電圧: 0.8V ±1%
- 外部クロックに同期
- 調整可能なスロー・スタートとシーケンシング
- UVおよびOVのパワー・グッド出力
- 動作時およびシャットダウン時の低い静止電流
- プリバイアス出力への安全なスタートアップ
- サイクル単位の電流制限、過熱保護、周波数フォールドバック保護機能
- 動作時の接合部温度範囲: -40℃～150℃
- 熱的に強化された3mm×3mmの16ピンWQFNパッケージ
- WEBENCH® Power Designerにより、TPS54318を使用するカスタム設計を作成

2 アプリケーション

- 低電圧、高密度の電源システム
- 高性能DSP、FPGA、ASIC、マイクロプロセッサのポイント・オブ・ロード・レギュレーション
- ブロードバンド、ネットワーク、光通信インフラ

概略回路図



3 概要

TPS54318デバイスは完全な機能を持つ6V、3A、同期整流降圧型電流モード・コンバータで、2つのMOSFETが内蔵されています。

TPS54318デバイスにはMOSFETが内蔵され、電流モード制御の実装により外付け部品数が減少し、最高2MHzのスイッチング周波数が可能なためインダクタのサイズが小さくなり、小型の3mm×3mmの熱的に強化されたQFNパッケージによりデバイスの占有面積が最小化されるため、小型のデバイスを設計できます。

TPS54318デバイスは、±1%の高精度基準電圧(V_{REF})により、温度にかかわらず各種の負荷について正確なレギュレーションを行います。

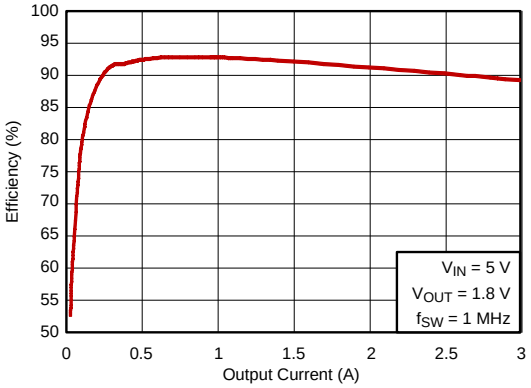
内蔵の30mΩ MOSFETと標準値350μAの消費電流により、効率が最大化されます。ENピンを使用してシャットダウン・モードに移行でき、シャットダウン時の消費電流は2μAに低下します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS54318	WQFN (16)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

効率と出力電流との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (December 2014) から **Revision C** に変更 **Page**

- タイトルを更新 ... 3

Revision A (September 2013) から **Revision B** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 3

2009年9月発行のものから更新 **Page**

- Added "Instantaneous peak current" specification to the Current Limit section in the *Electrical Characteristics* table ... 6
- Added Figure 22 to *Typical Characteristics section* ... 10

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5 概要（続き）

低電圧誤動作防止は内部で2.6Vに設定されていますが、イネーブル・ピンの抵抗回路でスレッショルドをプログラムすることにより、さらに高い電圧に設定できます。起動時の出力電圧の上昇は、ソフト・スタート・ピンによって制御されます。出力が公称電圧の93%～107%の範囲内にあるとき、オープン・ドレインのパワー・グッド信号で示されます。周波数のフォールドバックとサーマル・シャットダウンにより、過負荷状態時にデバイスが保護されます。

SWIFT™の詳しいドキュメントについては、TIのWebサイト(www.ti.com/swift)を参照してください。

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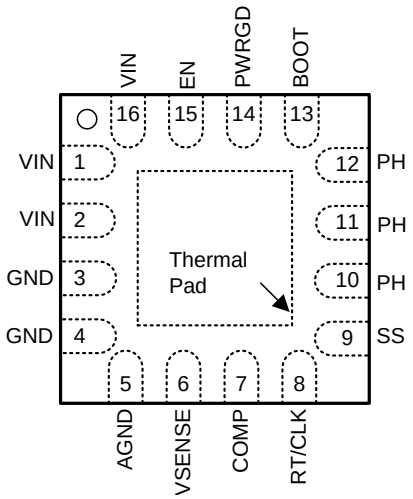
6 Pin Configuration and Functions

RTE Package
16 Pin WQFN
(TOP VIEW)



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	5	G	Analog ground should be electrically connected to GND close to the device.
BOOT	13	I	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin, internal pull-up current source. Pull below 1.2 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3	G	Power ground. This pin should be electrically connected directly to the power pad under the device.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
	11		
	12		
PWRGD	14	O	An open drain output, asserts low if output voltage is low due to thermal shutdown, overcurrent, over/under-voltage or EN shut down.
RT/CLK	8	I/O	Resistor Timing or External Clock input pin.
SS	9	I/O	Slow-start. An external capacitor connected to this pin sets the output voltage rise time. Soft
VIN	1	I	Input supply voltage, 2.95 V to 6 V.
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier.
Thermal Pad		G	GND pin should be connected to the exposed power pad for proper operation. This power pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = Input, O = Output, G = Ground

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	EN, PWRGD, VIN	–0.3	7	V
	RT/CLK	–0.3	6	
	COMP, SS, VSENSE	–0.3	3	
	BOOT		V_{PH}+ 8 V	
Output voltage	BOOT-PH		8	V
	PH	–0.6	7	
	PH (10 ns transient)	–2	7	
Source current	EN, RT/CLK		100	µA
Sink current	COMP, SS		100	µA
	PWRGD		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VIN}	Input voltage	3	6	V
T_J	Operating junction temperature	–40	150	°C

7.4 Thermal Information(1)

THERMAL METRIC(2)		TPS54318 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (3)	37	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.1	
ψ_{JT}	Junction-to-top characterization parameter	1.4	
ψ_{JB}	Junction-to-board characterization parameter	23.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	

(1) Unless otherwise specified, metrics listed in this table refer to JEDEC high-K board measurements
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(3) Test Board Conditions:
  (a) 2 inches × 2 inches, 4 layers, thickness: 0.062 inch
  (b) 2 oz. copper traces located on the top of the PCB
  (c) 2 oz. copper ground planes located on the two internal layers and bottom layer
  (d) 4 thermal vias (10 mil) located under the device package

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7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 150°C, 2.95 ≤ V_{VIN} ≤ 6 V (unless otherwise noted) over operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
V_{VIN}	Operating input voltage		2.95		6	V
V_{UVLO}	Internal under voltage lockout threshold	No voltage hysteresis, rising and falling		2.6	2.8	V
$I_{Q(vin)}$	Shutdown supply current	V_{EN} = 0 V, T_A = 25°C, 2.95 V ≤ V_{VIN} ≤ 6 V		2	5	µA
I_q	Quiescent current	V_{VSENSE} = 0.9 V, V_{VIN} = 5 V, 25°C, R_T = 400 kΩ		350	500	µA
ENABLE AND UVLO (EN)						
$V_{TH(en)}$	Enable threshold	Rising	1.16	1.25	1.37	V
		Falling		1.18		
I_{EN}	Input current	Enable rising threshold + 50 mV		–3.2		µA
		Enable falling threshold – 50 mV		–0.65		
VOLTAGE REFERENCE (VSENSE)						
V_{REF}	Voltage reference	2.95 V ≤ V_{VIN} ≤ 6 V, –40°C < T_J < 150°C	0.795	0.803	0.811	V
MOSFET						
$R_{DS(HFET)}$	High-side switch resistance	(V_{BOOT} – V_{PH}) = 5 V		30	60	mΩ
		(V_{BOOT} – V_{PH}) = 2.95 V		44	70	
$R_{DS(LFET)}$	Low-side switch resistance	V_{VIN} = 5 V		30	60	mΩ
		V_{VIN} = 2.95 V		44	70	
ERROR AMPLIFIER						
I_{IN}	Input current			7		nA
$g_{M(ea)}$	Error amplifier transconductance	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		225		µS
$g_{m(EA,ss)}$	Error amplifier transconductance during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{VSENSE} = 0.4 V		70		µS
I_{COMP}	Error amplifier source/sink	V_{COMP} = 1 V, 100 mV overdrive		±20		µA
g_M	COMP to I_{SWITCH} transconductance			13		A/V
CURRENT LIMIT						
I_{LIM}	Current limit threshold	Instantaneous peak current	3.7	5.5		A
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown			175		°C
$T_{SD(hyst)}$	Hysteresis			15		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK)						
f_{SW}	Switching frequency range using RT mode		200		2000	kHz
f_{SW}	Switching frequency	R_{RT} = 400 kΩ	400	500	600	kHz
f_{SW}	Switching frequency range using CLK mode		300		2000	kHz
$t_{MIN(CLK)}$	Minimum CLK pulse width		75			ns
$V_{RT/CLK}$	RT/CLK voltage	$R_{RT/CLK}$ = 400 kΩ		0.5		V
$V_{IH(CLK)}$	RT/CLK high threshold			1.6	2.2	V
$V_{IL(CLK)}$	RT/CLK low threshold		0.4	0.6		V
t_{DLY}	RT/CLK falling edge to PH rising edge delay	f_{SW} = 500 kHz with R_{RT} resistor in series		90		ns
$t_{LOCK(PLL)}$	PLL lock-in time	f_{SW} = 500 kHz		14		µs

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Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 150°C, 2.95 ≤ V_{VIN} ≤ 6 V (unless otherwise noted) over operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH-SIDE POWER MOSFET (PH)						
$t_{ON(min)}$	Minimum on time	Measured at 50% points on PH, I_{OUT} = 3		60		ns
		Measured at 50% points on PH, V_{VIN} = 5 V, I_{OUT} = 0 A		110		
$t_{OFF(min)}$	Minimum off time	Prior to skipping off pulses, (V_{BOOT} – V_{PH}) = 2.95 V, I_{OUT} = 3		60		ns
t_{RISE}	Rise time	V_{VIN} = 5 V		1.5		V/ns
t_{FALL}	Fall time	V_{VIN} = 5 V		1.5		V/ns
BOOT (BOOT)						
R_{BOOT}	BOOT charge resistance	V_{VIN} = 5 V		16		Ω
$V_{UVLO(Boot)}$	BOOT-PH UVLO	V_{VIN} = 2.95 V		2.1		V
SOFT-START (SS)						
I_{CHG}	Charge current	V_{SS} = 0.4 V		1.8		μA
V_{SSxREF}	SS to reference crossover	98% nominal		0.9		V
$V_{DSCHG(SS)}$	SS discharge voltage (overload)	V_{VSENSE} = 0 V		20		μA
$I_{DSCHG(SS)}$	SS discharge current (UVLO, EN, thermal fault)	V_{VIN} = 5 V, V_{SS} = 0.5 V		1.25		mA
POWER GOOD (PWRGD)						
$V_{TH(PG)}$	VSENSE threshold	V_{VSENSE} falling (fault)		91%		V_{REF}
		V_{VSENSE} rising (good)		93%		
		V_{VSENSE} rising (fault)		107%		
		V_{VSENSE} falling (Good)		105%		
$V_{HYST(PG)}$	Hysteresis	V_{VSENSE} falling		2%		
$I_{PH(lkg)}$	Output high leakage	V_{VSENSE} = V_{REF}, V_{PWRGD} = 5.5 V		2		nA
R_{PG}	Power Good on-resistance			100		Ω
V_{OL}	Low-level output voltage	I_{PWRGD} = 3.5 mA		0.3		V
$V_{MIN(PG)}$	Minimum input voltage for valid output	V_{PWRGD} < 0.5 V , I_{OUT} = 100 μA		1.2	1.6	V

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7.6 Typical Characteristics

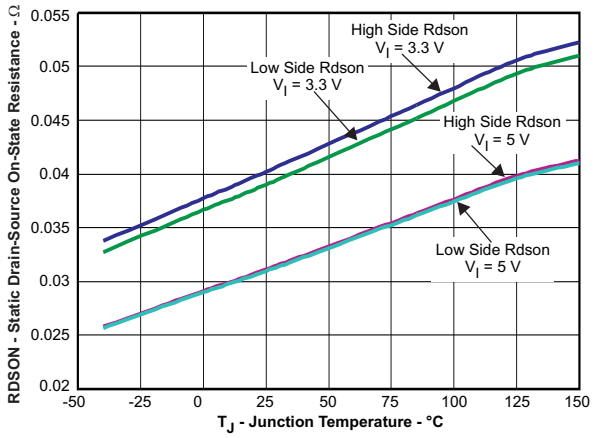

Figure 1. High-Side and Low-Side On Resistance vs Junction Temperature

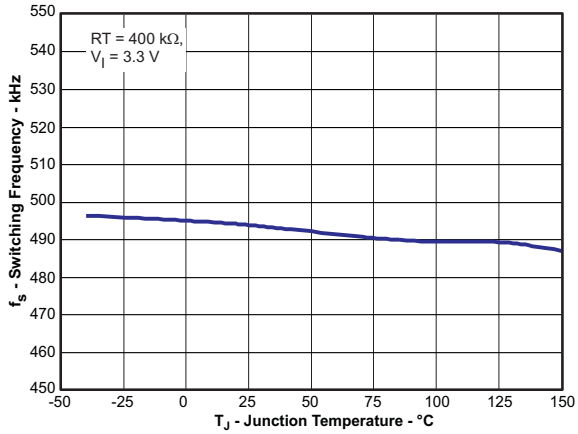

Figure 2. Frequency vs Junction Temperature

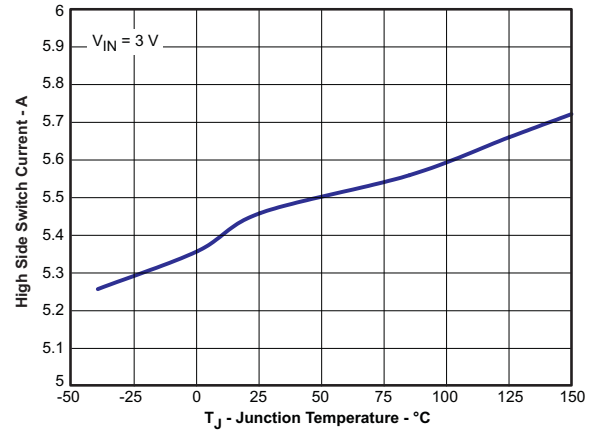

Figure 3. High-Side Current Limit vs Junction Temperature

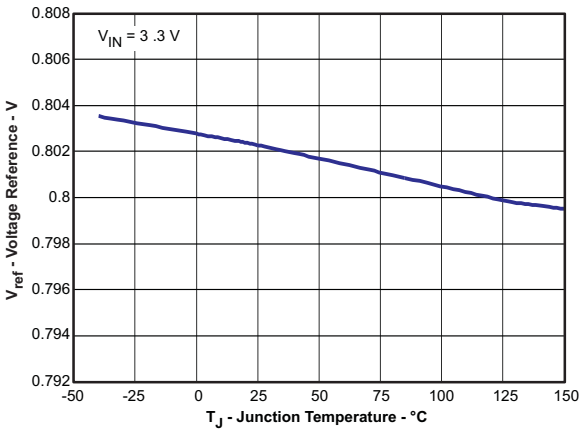

Figure 4. Voltage Reference vs Junction Temperature

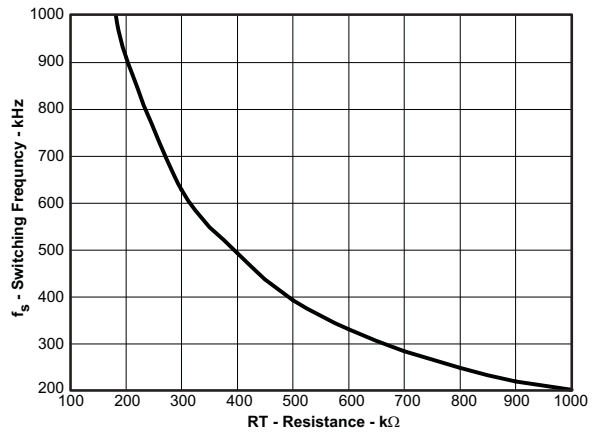

Figure 5. Switching Frequency vs RT Resistance Low Frequency Range

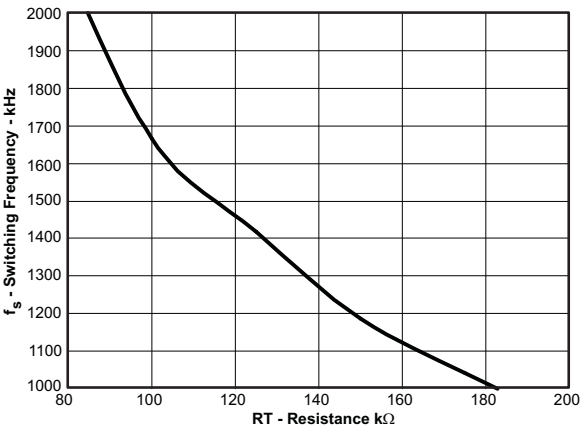

Figure 6. Switching Frequency vs RT Resistance High Frequency Range

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Typical Characteristics (continued)

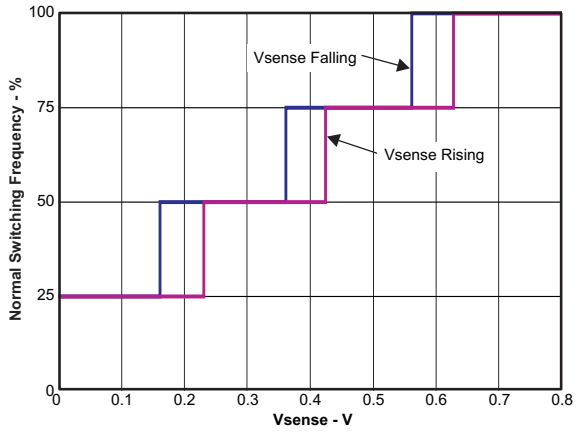

Figure 7. Switching Frequency vs Vsense

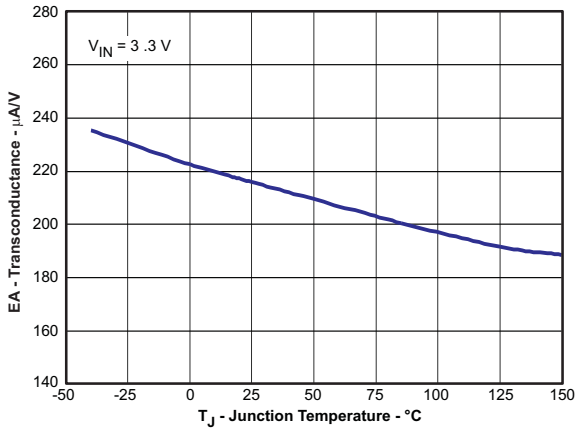

Figure 8. Transconductance vs Junction Temperature

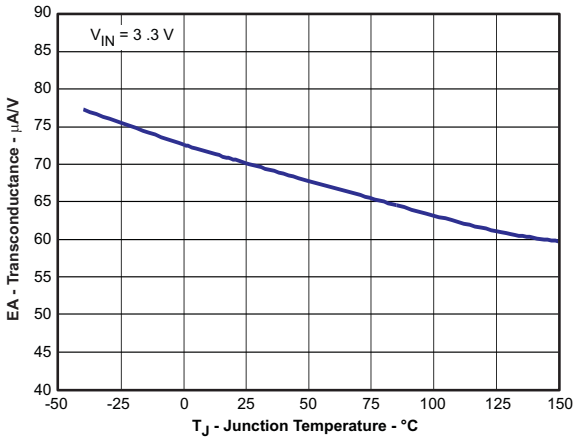

Figure 9. Transconductance (Soft-Start) vs Junction Temperature

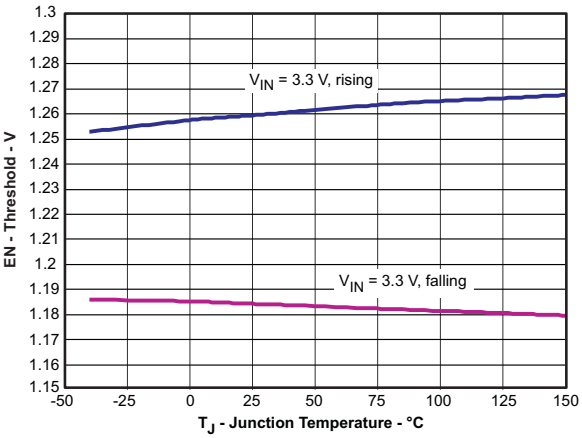

Figure 10. Enable Pin Voltage vs Junction Temperature

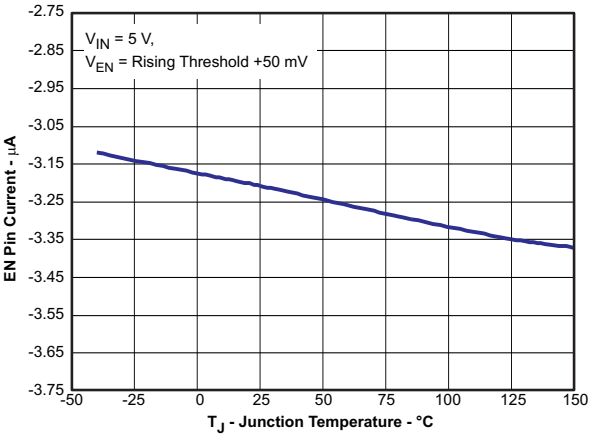

Figure 11. Pin Current vs Junction Temperature

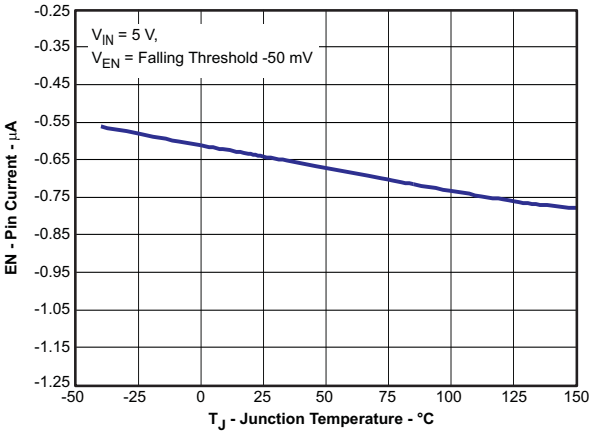

Figure 12. Pin Current vs Junction Temperature

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Typical Characteristics (continued)

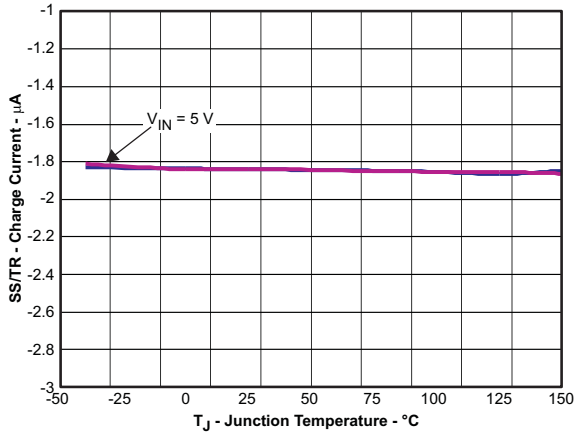

Figure 13. Charge Current vs Junction Temperature

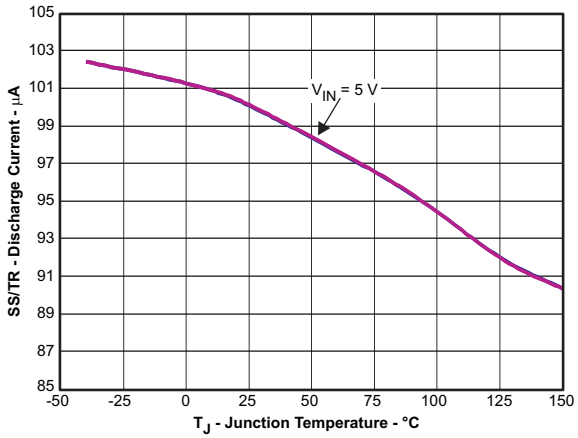

Figure 14. Discharge Current vs Junction Temperature

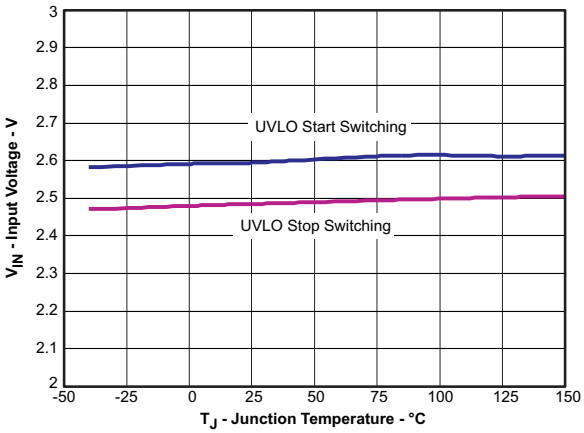

Figure 15. Input Voltage vs Junction Temperature

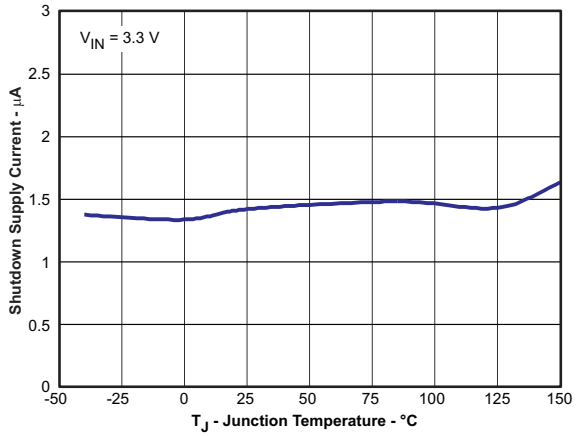

Figure 16. Shutdown Supply Current vs Junction Temperature

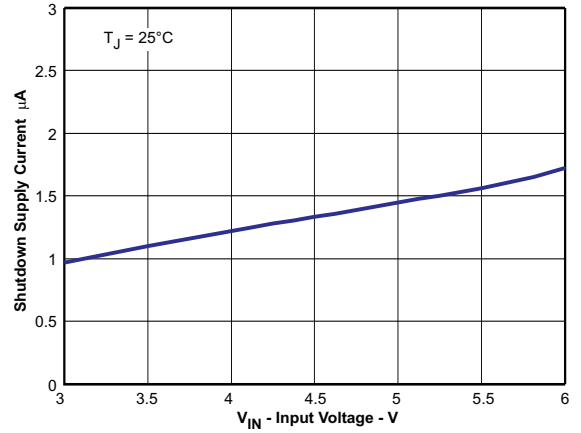

Figure 17. Shutdown Supply Current vs Input Voltage

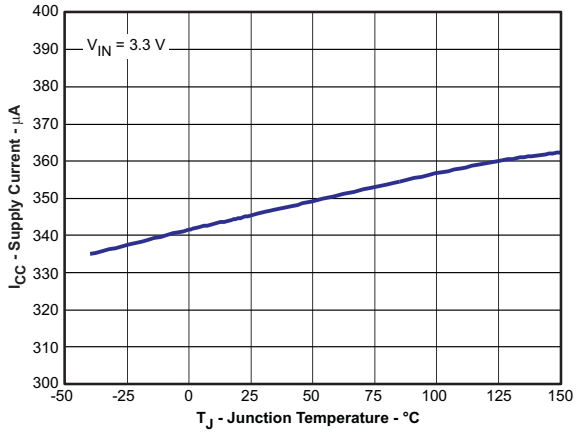

Figure 18. Supply Current vs Junction Temperature

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Typical Characteristics (continued)

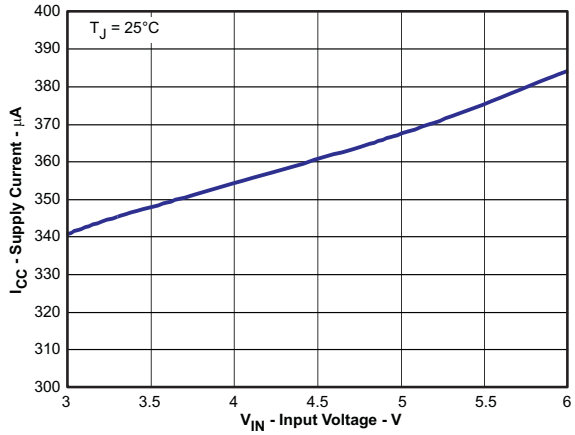

Figure 19. Supply Current vs Input Voltage

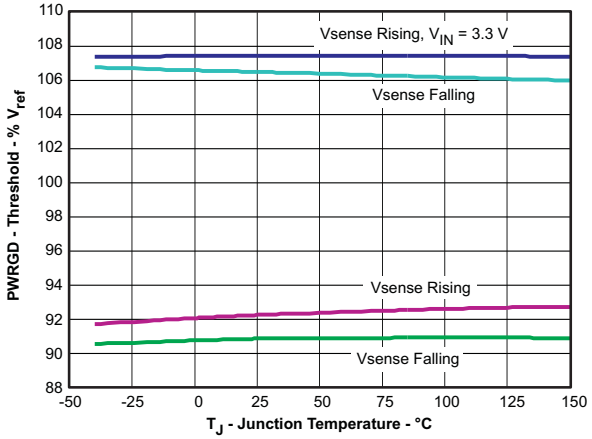

Figure 20. PWRGD Threshold vs Junction Temperature

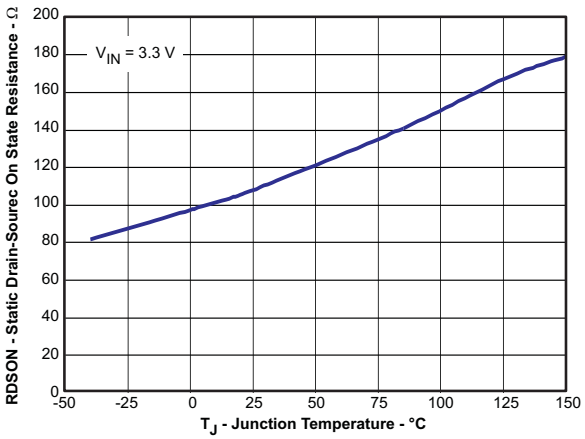

Figure 21. PWRGD On Resistance vs Junction Temperature

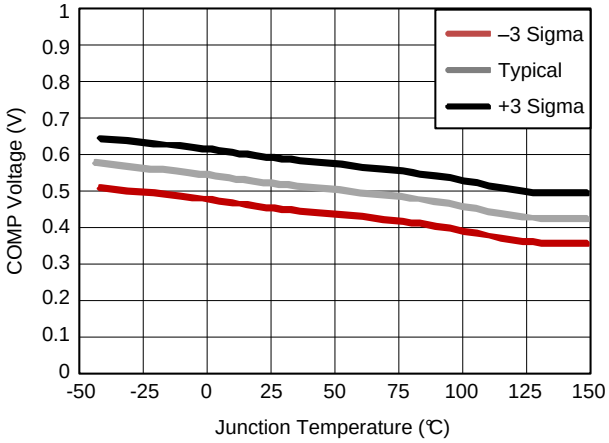

Figure 22. Minimum Comp Voltage Clamp vs Junction Temperature

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8 Detailed Description

8.1 Overview

The TPS54318 device is a 6-V, 3-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide supported switching frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54318 device has a typical default start up voltage of 2.6 V. The EN pin has an internal pull-up current source that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pull up current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54318 device is 350 μA when not switching and under no load. When the device is disabled, the supply current is less than 5 μA.

The integrated, 30-mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 3 amperes.

The TPS54318 device reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54318 device to operate approaching 100%. The output voltage can be stepped down to as low as the 0.8 V reference.

The TPS54318 device has a power good comparator (PWRGD) with 2% hysteresis.

The TPS54318 device minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 109% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 105%.

The SS (soft-start) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for soft-start. The SS pin is discharged before the output power up to ensure a repeatable re-start after an over-temperature fault, UVLO fault or disabled condition.

The use of a frequency-foldback circuit reduces the switching frequency during startup and over current fault conditions to help limit the inductor current.

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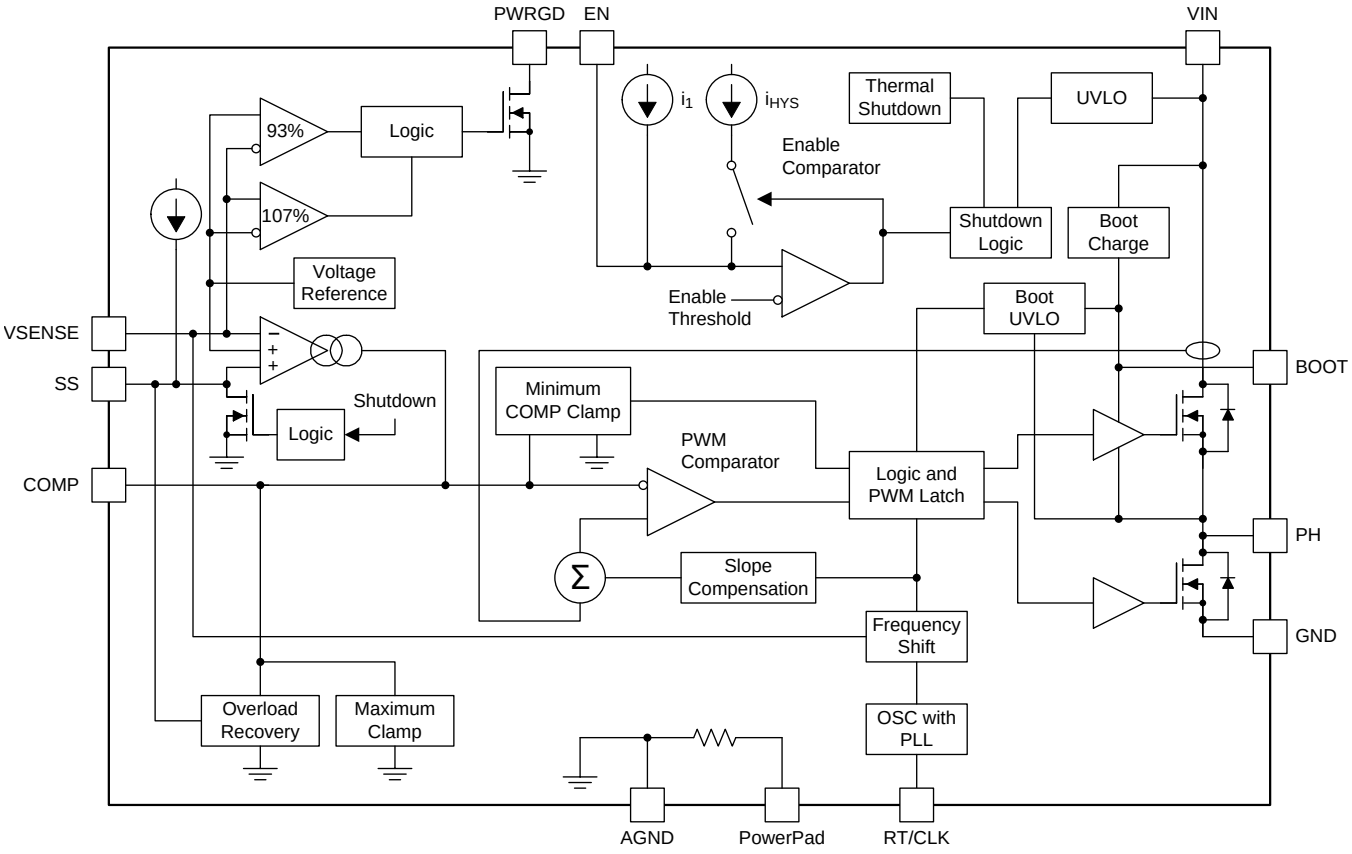
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS54318 device uses an adjustable fixed-frequency peak-current-mode control. The output voltage is compared through external resistors on the VSENSE to pin an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power-switch current. When the power switch reaches the COMP voltage, the high-side power switch is turned off and the low-side power switch is turned on.

The COMP pin voltage increases and decreases as the peak switch current increases and decreases. The device implements a current-limit function by clamping the COMP pin voltage to a maximum value, which limits the maximum peak current the device supplies. The device also implements a minimum COMP pin voltage clamp for improved transient response. When the COMP pin voltage is pushed low to the minimum clamp, such as during a load release event, turn-on of the high-side power switch is inhibited.

8.3.2 Slope Compensation and Output Current

The TPS54318 device adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

8.3.3 Bootstrap Voltage (Boot) and Low Dropout Operation

The TPS54318 device has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics overtemperature and voltage.

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Feature Description (continued)

To improve drop out, the TPS54318 device is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.5 V. The high-side MOSFET is turned off using an UVLO circuit, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.5 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

8.3.4 Error Amplifier

The TPS54318 device has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS pin voltage or the internal 0.8 V voltage reference. The transconductance of the error amplifier is 225 μA/V during normal operation. When the voltage of VSENSE pin is below 0.8 V and the device is regulating using the SS voltage, the transconductance is 70 μA/V. The frequency compensation components are placed between the COMP pin and ground.

8.3.5 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference overtemperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.8 V at the non-inverting input of the error amplifier.

8.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a value of 100 kΩ for the R1 resistor and use Equation 1 to calculate R2. To improve efficiency at very light loads, consider using larger resistor values. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.8\ V}{V_O - 0.8\ V} \right) \quad (1)$$

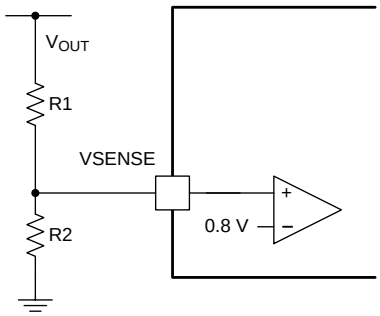

Figure 23. Voltage Divider Circuit

8.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54318 device is disabled when the VIN pin voltage falls below 2.6 V. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 24 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (V_{STOP}) above 2.7 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pull-up current source that provides the default condition of the TPS54318 device operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.55 μA of hysteresis is added. When the EN pin is pulled below 1.18 V, the 2.55 μA is removed. This additional current facilitates input voltage hysteresis.

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Feature Description (continued)

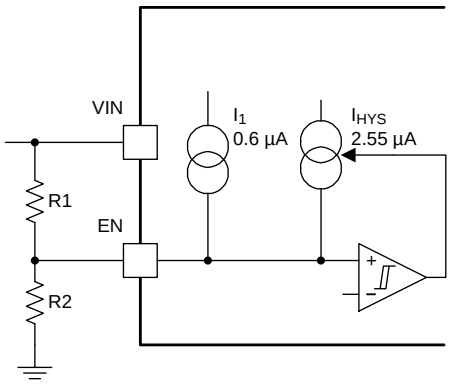

Figure 24. Adjustable Undervoltage Lockout

$$R1 = \frac{0.944 \cdot V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad (2)$$

$$R2 = \frac{1.18 \cdot R1}{V_{STOP} - 1.18 + R1 \cdot 3.2 \times 10^{-6}} \quad (3)$$

8.3.8 Soft-Start Pin

The TPS54318 device regulates to the lower of the SS pin and the internal reference voltage. A capacitor on the SS pin to ground implements a soft-start time. The TPS54318 device has an internal pull-up current source of 1.8 µA which charges the external soft-start capacitor. Equation 4 calculates the required soft-start capacitor value where t_{SS} is the desired soft-start time in ms, I_{SS} is the internal soft-start charging current of 1.8 µA, and V_{REF} is the internal voltage reference of 0.8 V. it is recommended to maintain the soft-start time in the range between 1 ms and 10 ms.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

where

- C_{SS} is in nF
- t_{SS} is in ms
- I_{SS} is in µA
- V_{REF} is in V (4)

If during normal operation, the input voltage goes below the UVLO, EN pin pulled below 1.2 V, or a thermal shutdown event occurs, the TPS54318 device stops switching and the SS is discharged to 0 volts before reinitiating a powering up sequence.

8.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS, EN and PWRGD pins. The sequential method can be implemented using an open drain or collector output of a power on reset pin of another device. Figure 25 shows the sequential method. The power good is coupled to the EN pin on theTPS54318 device which enables the second power supply once the primary supply reaches regulation.

Ratiometric start up can be accomplished by connecting the SS pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time the pull up current source must be doubled in Equation 4. The ratiometric method is shown in Figure 27.

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Feature Description (continued)

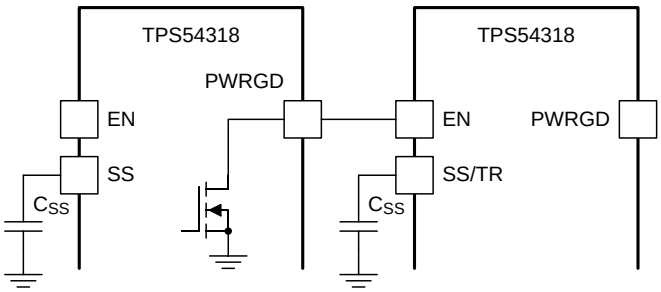

Figure 25. Sequencial Start-Up Schematic

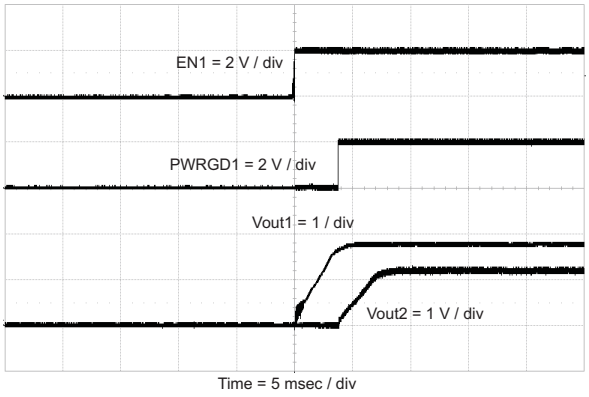

Figure 26. Sequential Startup using EN and PWRGD

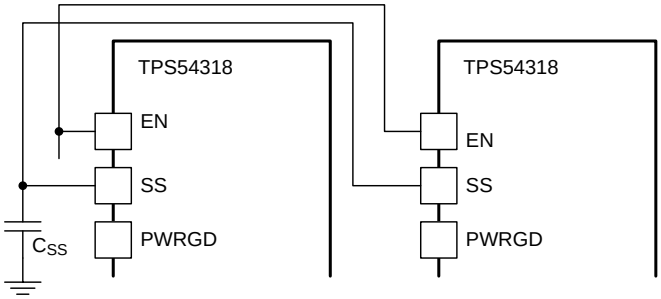

Figure 27. Ratiometric Start-Up Schematic

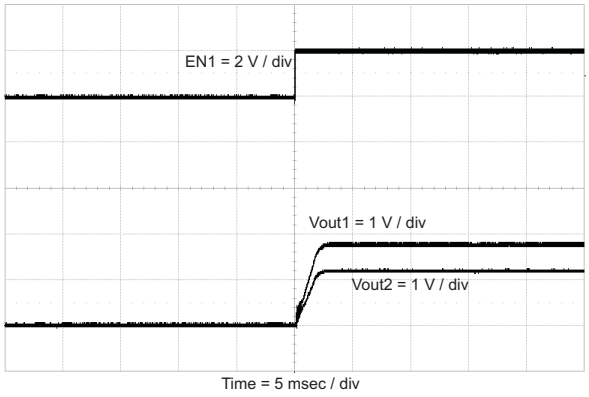

Figure 28. Ratiometric Start-Up Using Coupled SS Pins

8.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54318 device is adjustable over a wide range from 200 kHz to 2000 kHz by placing a maximum of 1000 kΩ and minimum of 85 kΩ, respectively, on the RT/CLK pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 5 or Figure 6 or Equation 5.

$$R_{RT} = \frac{311890}{(f_{SW})^{1.0793}}$$

where

- R_{RT} is in kΩ
- f_{SW} is in kHz

(5)

$$f_{SW} = \frac{133870}{(R_{RT})^{0.9393}}$$

where

- R_{RT} is in kΩ
- f_{SW} is in kHz

(6)

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage and minimum controllable on time should be considered.

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Feature Description (continued)

The minimum controllable on time is typically 60 ns at full current load and 110 ns at no load, and limits the maximum operating input voltage or output voltage.

8.3.11 Overcurrent Protection

The TPS54318 device implements a cycle-by-cycle current limit. During each switching cycle the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

8.3.12 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54318 device implements a frequency shift. If frequency shift was not implemented, during an overcurrent condition the low-side MOSFET may not be turned off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition the switching frequency is reduced from 100%, then 75%, then 50%, then 25% as the voltage decreases from 0.8 to 0 volts on VSENSE pin to allow the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.8 volts. See Figure 7 for details.

8.3.13 Reverse Overcurrent Protection

The TPS54318 device implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is more than 1.3 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

8.3.14 Synchronize Using the RT/CLK Pin

The RT/CLK pin is used to synchronize the converter to an external system clock. See Figure 29. To implement the synchronization feature in a system, connect a square wave to the RT/CLK pin with an on time of at least 75ns. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the mode returns to the frequency set by the resistor. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V typically. The recommended synchronization frequency range is 300 kHz to 2000 kHz. If the external system clock is to be removed, TI recommends that it be removed on the falling edge of the clock.

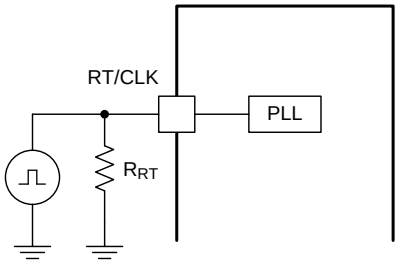

Figure 29. Synchronizing to a System Clock

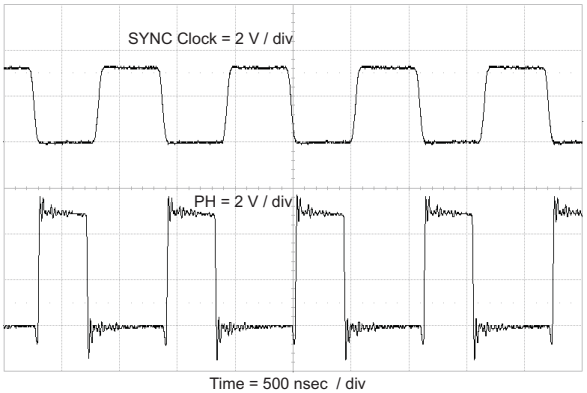

Figure 30. Plot of Synchronizing to System Clock

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Feature Description (continued)

8.3.15 Power Good (PWRGD Pin)

The PWRGD pin output is an open drain MOSFET. The output is pulled low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 107% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 105% of the internal voltage reference the PWRGD output MOSFET is turned off. It is recommended to use a pull-up resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.2 V.

8.3.16 Overvoltage Transient Protection

The TPS54318 device incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold which is 109% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold the high-side MOSFET is allowed to turn on the next clock cycle.

8.3.17 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 160°C, the device reinitiates the power up sequence by discharging the SS pin to 0 volts. The thermal shutdown hysteresis is 15°C.

8.4 Device Functional Modes

8.4.1 Small Signal Model for Loop Response

Figure 31 shows an equivalent model for the TPS54318 device control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a g_M of 225 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor $R_{OUT(ea)}$ and capacitor $C_{OUT(ea)}$ model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_{LOAD} with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

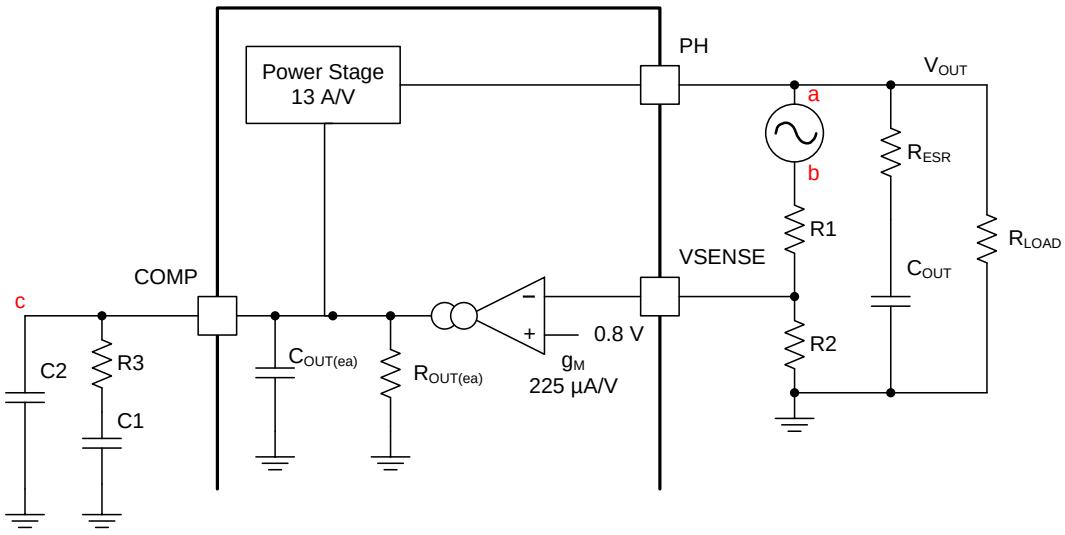

Figure 31. Small Signal Model for Loop Response

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Device Functional Modes (continued)

8.4.2 Simple Small Signal Model for Peak Current Mode Control

Figure 32 is a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54318 device power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 7 and consists of a dc gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 31) is the power stage transconductance. The g_M for the TPS54318 device is 13 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 8. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but the dominant pole moves with load current [see Equation 9]. The combined effect is highlighted by the dashed line in the right half of Figure 33. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

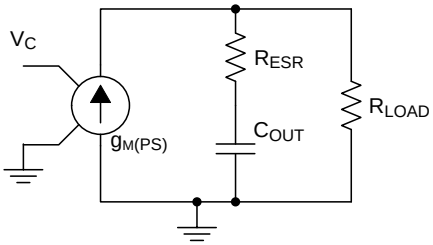

Figure 32. Simple Small Signal Model

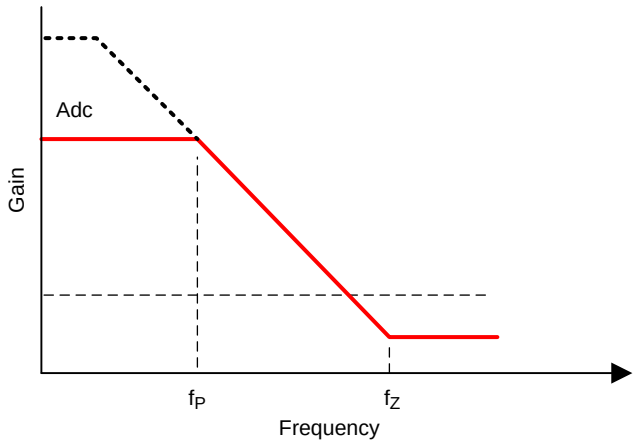

Figure 33. Frequency Response

$$\frac{V_{OUT}}{V_C} = Adc \times \frac{1+\left(\frac{s}{2\pi \times f_Z}\right)}{1+\left(\frac{s}{2\pi \times f_P}\right)} \quad (7)$$

$$Adc = g_{M(PS)} \times R_{LOAD} \quad (8)$$

$$f_P = \frac{1}{C_{OUT} \times R_{LOAD} \times 2\pi} \quad (9)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (10)$$

8.4.3 Small Signal Model for Frequency Compensation

The TPS54318 device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 34. The Type-II circuits are most likely implemented in high bandwidth power supply designs using low ESR output capacitors. In Type-IIA, one additional high frequency pole is added to attenuate high-frequency noise.

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Device Functional Modes (continued)

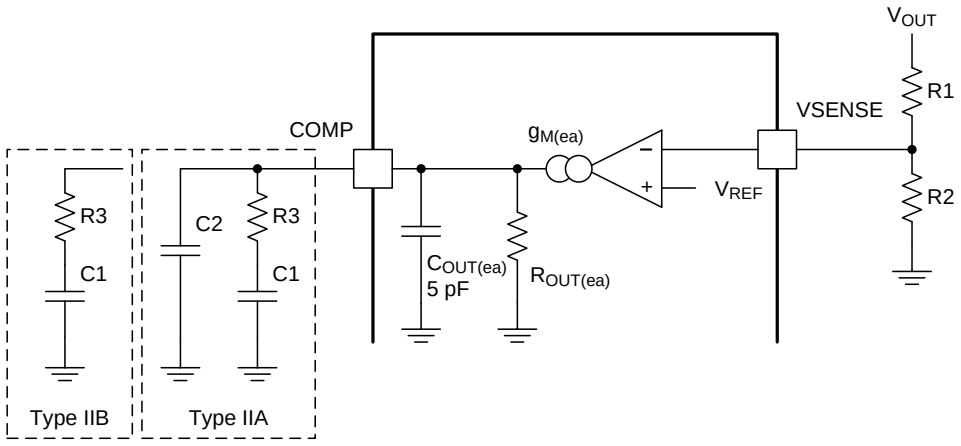

Figure 34. Types of Frequency Compensation

The design guidelines for TPS54318 device loop compensation are as follows:

1. Calculate the modulator pole ($f_{P(MOD)}$) and the esr zero, (f_{Z1}) using Equation 11 and Equation 12. If the output voltage is a high percentage of the capacitor rating it may be necessary to derate the output capacitor (C_{OUT}). Use the capacitor manufacturer information to derate the capacitor value. Use Equation 13 and Equation 14 to estimate a starting point for the crossover frequency, f_C. Equation 13 shows the geometric mean of the modulator pole and the ESR zero and Equation 14 is the mean of modulator pole and the switching frequency. Use the lower value of Equation 13 or Equation 14 as the maximum crossover frequency.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (11)$$

$$f_{Z1} = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (12)$$

$$f_C = \sqrt{f_{P(mod)} + f_{Z1}} \quad (13)$$

$$f_C = \sqrt{f_{P(mod)} \times \frac{f_{SW}}{2}} \quad (14)$$

2. Calculate resistor R3. Equation 15 shows the calculation for resistor R3.

$$R3 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{g_{M(ea)} \times V_{REF} \times g_{M(ps)}} \quad (15)$$

where

- $g_{M(ea)}$ is the amplifier gain (225 μA/V)
- $g_{M(ps)}$ is the power stage gain (13 A/V)

3. Place a compensation zero at the dominant pole. f_P. Equation 16 shows the calculation for capacitor C1.

$$f_P = \frac{1}{C_{OUT} \times R_{LOAD} \times 2\pi} \quad (16)$$

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (17)$$

4. Capacitor C2 is optional. It can be used to cancel the zero from the output capacitor (C_{OUT}) ESR.

$$C2 = \frac{R_{ESR} \times C_{OUT}}{R3} \quad (18)$$

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This design example describes a high-frequency switching regulator design using ceramic output capacitors. This design is available as the HPA512 (SLVU330) evaluation module (EVM).

9.2 Typical Application

This section details a high-frequency, 1.8-V output power supply design application with adjusted UVLO.

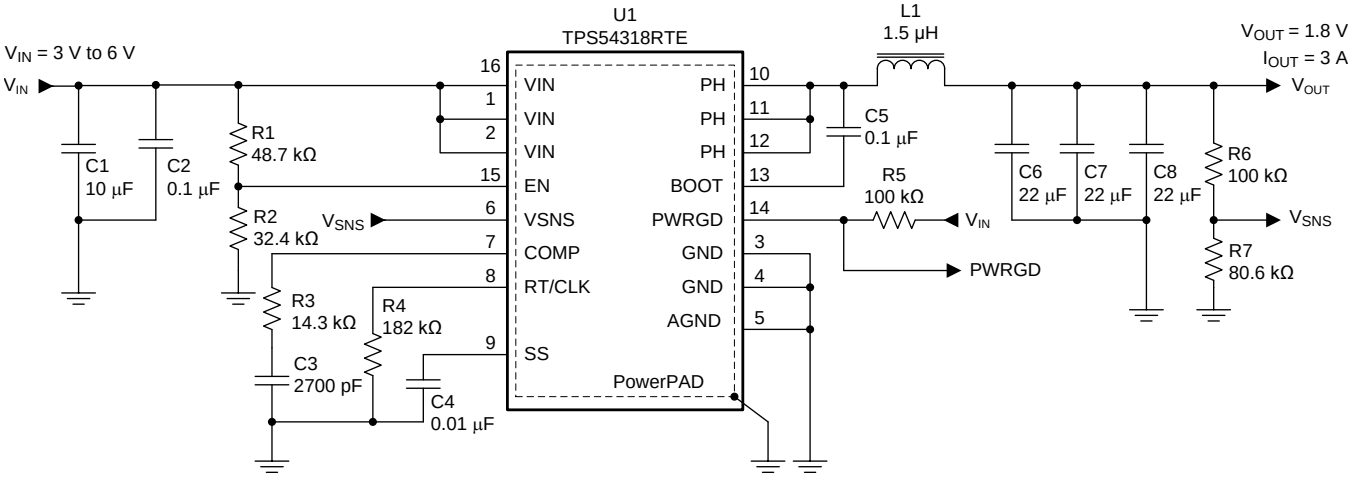

Figure 35. Typical Application Schematic, TPS54318

9.2.1 Design Requirements

Table 1. Design Parameters

PARAMETER		NOTES AND CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Operating	3	3.3	6	V
V_{START}	Start input voltage	Rising		3.1		
V_{STOP}	Stop input voltage	Falling		2.8		
V_{OUT}	Output voltage			1.8		V
ΔV_{OUT}	Transient response	1-A to 2-A load step		3%		
$I_{OUT(max)}$	Maximum output current				3	A
$V_{OUT(ripple)}$	Output voltage ripple				30	mV_{P-P}
f_{SW}	Switching frequency			1		MHz

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9.2.2 Detailed Design Procedure

9.2.2.1 Step One: Select the Switching Frequency

Choose the highest switching frequency possible in order to produce the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which in turn decrease the device performance. The device is capable of operating between 200 kHz and 2 MHz. Select a moderate switching frequency of 1 MHz in order to achieve both a small solution size and a high-efficiency operation. Using Equation 5, R4 is calculates to 180 kΩ. A standard 1%, 182-kΩ resistor is used in the design.

9.2.2.2 Step Two: Select the Output Inductor

The inductor selected must operate across the entire TPS54318 device input voltage range. To calculate the value of the output inductor, use Equation 19. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use a K_{IND} of 0.3 and the inductor value is calculated to be 1.40 μH. For this design, use an inductor with the nearest standard value of 1.50 μH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be calculated in Equation 21 and Equation 22.

For this design, the RMS inductor current is 3.01 A and the peak inductor current is 3.42 A. The chosen inductor is a Coilcraft XPL7030-152ML. It has a RMS current rating of 12.3 A and a saturation current rating of 20.2 A. The current ratings for this exceed the requirement, but the inductor was chosen for small physical size and low series resistance for high efficiency.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{\left(V_{IN(max)} - V_{OUT}\right)}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{19}$$

$$I_{RIPPLE} = \frac{\left(V_{IN(max)} - V_{OUT}\right)}{L1} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} \tag{20}$$

$$I_{L(rms)} = \sqrt{\left(I_{OUT}\right)^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L1 \times f_{SW}} \right)^2} \tag{21}$$

$$I_{L(peak)} = I_{OUT} + \left(\frac{I_{RIPPLE}}{2} \right) \tag{22}$$

9.2.2.3 Step Three: Choose the Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

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The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator cannot. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 25 shows the necessary minimum output capacitance.

For this example, the transient load response is specified as a 3% change in V_{OUT} for a load step from 1.25 A (50% load) to 2.75 A (100%).

$$\Delta I_{OUT} = 2.75 - 1.25 = 1.5 \text{ A} \quad (23)$$

$$\Delta V_{OUT} = 0.03 \times 1.8 = 0.054 \text{ V} \quad (24)$$

Using these numbers gives a minimum capacitance of 56 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 26 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{SW} is the switching frequency, V_{RIPPLE} is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. In this case, the maximum output voltage ripple is 30 mV. Equation 26 yields 3.2 µF.

$$C_{OUT\,(transient\ )} > \frac{2 \times \Delta I_{IOUT}}{f_{SW} \times \Delta V_{OUT}} \quad (25)$$

$$C_{OUT\,(ripple\ )} > \frac{I_{Ripple}}{8 \times f_{SW} \times V_{OUT\,(ripple\ )}} \quad (26)$$

where

- ΔI_{OUT} is the load step size
- ΔV_{OUT} is the acceptable output deviation
- f_{SW} is the switching frequency
- I_{Ripple} is the inductor ripple current
- $V_{OUT(Ripple)}$ is the acceptable DC output voltage ripple

Equation 27 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 27 indicates the ESR should be less than 39 mΩ. In this case, the ESR of the ceramic capacitor is much less than 39 mΩ.

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, three 22-µF, 10-V, X5R ceramic capacitors with 3 mΩ of ESR are used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Equation 28 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 28 yields 222 mA.

$$R_{ESR} < \frac{V_{OUT\,(ripple\ )}}{I_{Ripple}} \quad (27)$$

$$I_{CO(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L1 \times f_{SW}} \quad (28)$$

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9.2.2.4 Step Four: Select the Input Capacitor

The TPS54318 device requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 4.7 μF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the device. The input ripple current can be calculated using Equation 29.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the dc bias taken into account. The capacitance value of a capacitor decreases as the dc bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10 V voltage rating is required to support the maximum input voltage. For this example, one 10 μF and one 0.1 μF 10 V capacitors in parallel have been selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 30.

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \tag{29}$$

$$\Delta V_{IN} = \frac{I_{OUT(max)} \times 0.25}{C_{IN} \times f_{SW}} \tag{30}$$

Using the design example values, $I_{OUT(max)}$ = 3 A, C_{IN} = 10 μF, f_{SW} = 1 MHz, yields an input voltage ripple of 51 mV and a rms input ripple current of 1.47 A.

9.2.2.5 Step Five: Minimum Load DC COMP Voltage

The TPS54318 implements a minimum COMP voltage clamp for improved load-transient response. The COMP voltage tracks the peak inductor current, increasing as the peak inductor current increases, and decreases as the peak inductor current decreases. During a severe load-dump event, for instance, the COMP voltage decreases suddenly, falls below the minimum clamp value, then settles to a lower DC value as the control loop compensates for the transient event. During the time when COMP reaches the minimum clamp voltage, turnon of the high-side power switch is inhibited, keeping the low-side power switch on to discharge the output voltage overshoot more quickly.

Proper application circuit design must ensure that the minimum load steady-state COMP voltage is above the +3 sigma minimum clamp to avoid unwanted inhibition of the high side power switch. For a given design, the steady-state DC level of COMP must be measured at the minimum designed load and at the maximum designed input voltage, then compared to the minimum COMP clamp voltage shown in Figure 22. These conditions give the minimum COMP voltage for a given design. Generally, the COMP voltage and minimum clamp voltage move by about the same amount with temperature. Increasing the minimum load COMP voltage is accomplished by decreasing the output inductor value or the switching frequency used in a given design.

9.2.2.6 Step Six: Choose the Soft-Start Capacitor

The soft-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the device reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The soft-start capacitor value can be calculated using Equation 31. For the example circuit, the soft-start time is not too critical since the output capacitor value is 66 μF which does not require much current to charge to 1.8 V. The example circuit has the soft-start time set to an arbitrary value of 4 ms which requires a 10 nF capacitor. In the device, I_{SS} is 2 μA and V_{REF} is 0.8 V. For this application, maintain the soft-start time in the range between 1 ms and 10 ms.

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$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}}$$

where

- C_{SS} is in nF
- I_{SS} is in µA
- t_{SS} is in ms
- V_{REF} is in V

(31)

9.2.2.7 Step Seven: Select the Bootstrap Capacitor

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

9.2.2.8 Step Eight: Undervoltage Lockout Threshold

The undervoltage lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54318. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 3.1 V (V_{START}). Switching continues until the input voltage falls below 2.8 V (V_{STOP}).

The programmable UVLO and enable voltages are set using a resistor divider between the VIN pin and GND to the EN pin. Equation 32 and Equation 33 can be used to calculate the resistance values necessary. From Equation 32 and Equation 33, a 48.7 kΩ between the VIN pin and the EN pin and a 32.4-kΩ resistor between the EN pin and GND are required to produce the 3.1-V start voltage and the 2.8-V stop voltage.

$$R1 = \frac{0.944 \cdot V_{START} - V_{STOP}}{2.59 \times 10^{-6}} \quad (32)$$

$$R2 = \frac{1.18 \cdot R1}{V_{STOP} - 1.18 + R1 \cdot 3.2 \times 10^{-6}} \quad (33)$$

9.2.2.9 Step Nine: Select Output Voltage and Feedback Resistors

For the example design, 100 kΩ was selected for R6. Using Equation 34, R7 is calculated as 80 kΩ. The nearest standard 1% resistor is 80.6 kΩ.

$$R7 = \frac{V_{ref}}{V_{OUT} - V_{ref}} R6 \quad (34)$$

9.2.2.9.1 Output Voltage Limitations

Due to the internal design of the TPS54318, there are limitations to the minimum and maximum achievable output voltages. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by Equation 35. There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 36. These equations represent the results when the power MOSFETs are matched. Refer to SLYT293 for more information.

$$V_{OUT(min)} = t_{ON(min)} \times f_{SW(max)} \times V_{IN(max)} - I_{OUT(min)}\left(R_{LS(min)} + R_{DCR}\right)$$

where

- $V_{OUT(min)}$ is the minimum achievable output voltage
- $t_{ON(min)}$ is the minimum controllable on-time (110 nsec typical)
- $f_{SW(max)}$ is the maximum switching frequency including tolerance
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(min)}$ is the minimum load current
- $R_{LS(min)}$ is the minimum low-side MOSFET on-resistance. (30 mΩ typical)
- R_{DCR} is the series resistance of output inductor

(35)

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$$V_{OUT(max)} = (1 - t_{OFF(max)} f_{SW(max)}) V_{IN(min)} - I_{OUT(max)} (R_{LS(max)} + R_{DCR})$$

where

- $V_{OUT(max)}$ is the maximum achievable output voltage
- $t_{OFF(max)}$ is the maximum, minimum controllable off time (60 ns typical)
- $f_{SW(max)}$ is the maximum switching frequency including tolerance
- $V_{IN(min)}$ is the minimum input voltage
- $I_{OUT(max)}$ is the maximum load current
- $R_{HS(max)}$ is the maximum high-side MOSFET on-resistance. (70 mΩ max)
- R_{DCR} is the series resistance of output inductor (36)

9.2.2.10 Step 10: Select Loop Compensation Components

There are several industry techniques used to compensate DC/DC regulators. The method presented here is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 and 90 degrees. The method presented here ignores the effects of the slope compensation that is internal to the TPS54318. Because the slope compensation is ignored, the actual crossover frequency is usually lower than the crossover frequency used in the calculations. Use SwitcherPro software for a more accurate design.

To get started, the modulator pole, $f_{P(mod)}$, and the esr zero, f_{Z1} must be calculated using Equation 37 and Equation 38. For C_{OUT}, derating the capacitor is not needed as the 1.8 V output is a small percentage of the 10 V capacitor rating. If the output is a high percentage of the capacitor rating, use the capacitor manufacturer information to derate the capacitor value. Use Equation 39 and Equation 40 to estimate a starting point for the crossover frequency, f_C. For the example design, $f_{P(mod)}$ is 4.02 kHz and f_{Z1} is 804 kHz. Equation 39 is the geometric mean of the modulator pole and the esr zero and Equation 40 is the mean of modulator pole and the switching frequency. Equation 39 yields 56 kHz and Equation 40 gives 44.8 kHz. Use the lower value of Equation 39 or Equation 40 as the maximum crossover frequency. For this example, fc is 45 kHz. Next, the compensation components are calculated. A resistor in series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole (if needed).

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (37)$$

$$f_{Z1} = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (38)$$

$$f_C = \sqrt{f_{P(mod)} \times f_{Z1}} \quad (39)$$

$$f_C = \sqrt{f_{P(mod)} \times \frac{f_{SW}}{2}} \quad (40)$$

The compensation design takes the following steps:

1. Set up the anticipated cross-over frequency. Use Equation 41 to calculate the compensation network's resistor value. In this example, the anticipated cross-over frequency f_C is 45 kHz. The power stage gain ($g_{M(ps)}$) is 13 A/V and the error amplifier gain ($g_{M(ea)}$) is 225uA/V.

$$R3 = \frac{2\pi \times f_C \times V_{OUT} \times C_{OUT}}{g_{M(ea)} \times V_{REF} \times g_{M(ps)}} \quad (41)$$

2. Place compensation zero at the pole formed by the load resistor and the output capacitor. The compensation network's capacitor can be calculated from Equation 42.

$$C3 = \frac{R_{OUT} \times C_{OUT}}{R3} \quad (42)$$

3. An additional pole can be added to attenuate high frequency noise. In this application, it is not necessary to add it.

From the procedures above, start with a 14.3 kΩ resistor and a 2760 pF capacitor. After prototyping and bode plot measurement, the optimized compensation network selected for this design includes a 14.3 kΩ resistor and a 2700 pF capacitor.

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9.2.2.11 Power Dissipation Estimate

Use Equation 43 through Equation 52 to help estimate the device power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the device (P_{TOT}) includes conduction loss (P_{COND}), dead time loss (P_D), switching loss (P_{SW}), gate drive loss (P_{GD}) and supply current loss (P_Q).

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \quad (43)$$

$$P_D = f_{SW} \times I_{OUT} \times 0.7 \times 60 \times (10)^{-9} \quad (44)$$

$$P_D = f_{SW} \times I_{OUT} \times 0.7 \times 60 \times (10)^{-9} \quad (45)$$

$$P_{SW} = 2 \times (V_{IN})^2 \times f_{SW} \times I_{OUT} \times 0.25 \times (10)^{-9} \quad (46)$$

$$P_{SW} = 2 \times (V_{IN})^2 \times f_{SW} \times I_{OUT} \times 0.25 \times (10)^{-9} \quad (47)$$

$$P_{GD} = 2 \times V_{IN} \times 3 \times (10)^{-9} \times f_{SW} \quad (48)$$

$$P_Q = 350 \times (10)^{-6} \times V_{IN}$$

where

- I_{OUT} is the output current (A)
- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)
- f_{SW} is the switching frequency (Hz) (49)

$$P_{TOT} = P_{COND} + P_D + P_{SW} + P_{GD} + P_Q \quad (50)$$

For a given ambient temperature,

$$T_J = T_A + R_{TH} \times P_{TOT} \quad (51)$$

For maximum junction temperature ($T_{J(max)}$ = 150°C)

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT}$$

where

- P_{TOT} is the total device power dissipation (W)
- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{TH} is the thermal resistance of the package (°C/W)
- $T_{J(max)}$ is maximum junction temperature (°C)
- $T_{A(max)}$ is maximum ambient temperature (°C) (52)

Additional power can be lost in the regulator circuit due to the inductor ac and dc losses and trace resistance that impact the overall regulator efficiency. Figure 36 and Figure 37 show power dissipation for the EVM.

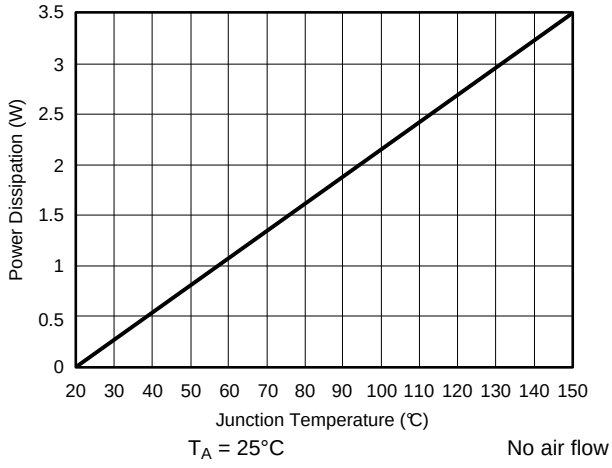

Figure 36. Power Dissipation vs Junction Temperature

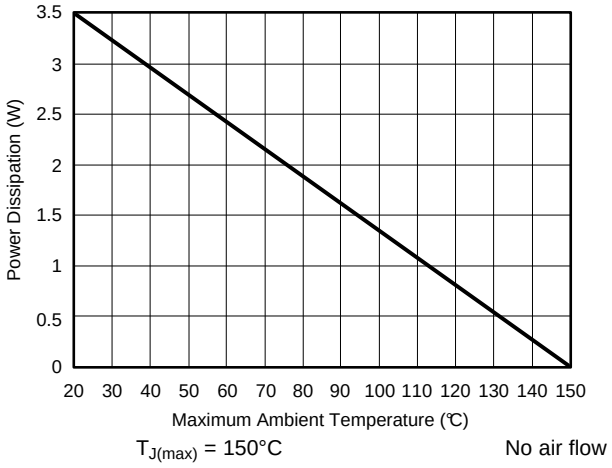

Figure 37. Power Dissipation vs Ambient Temperature

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9.2.3 Application Curves

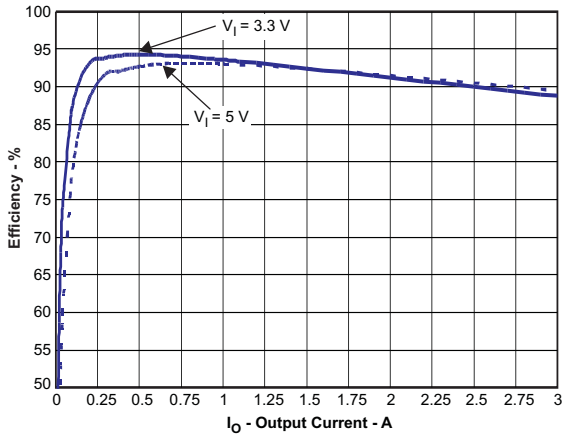

Figure 38. Efficiency vs Load Current

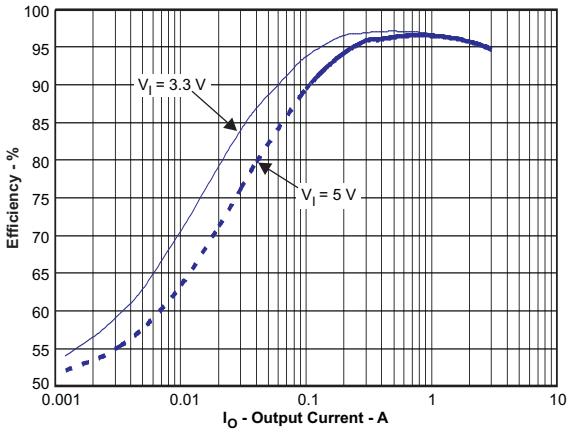

Figure 39. Efficiency vs Load Current

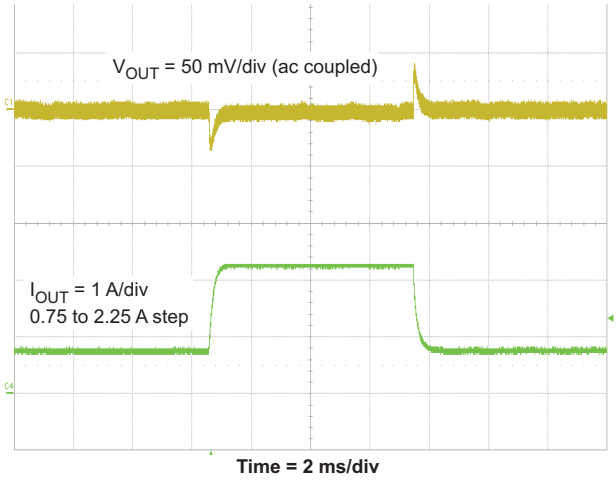

Figure 40. Transient Response

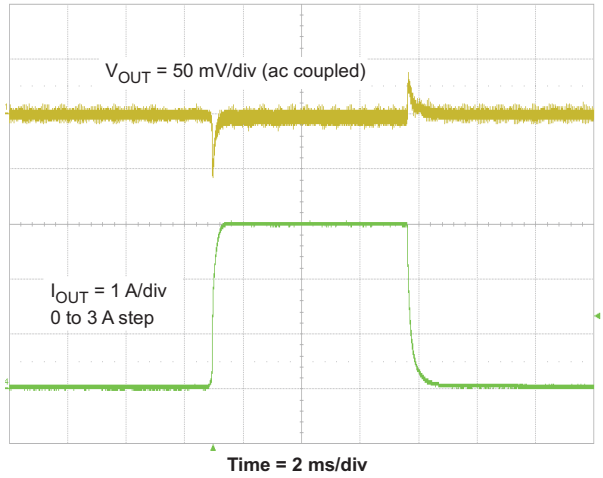

Figure 41. Transient Response

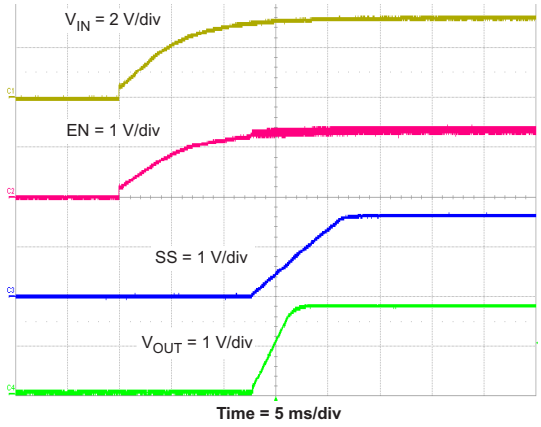

Figure 42. Power-Up, V_{OUT}, V_{IN}

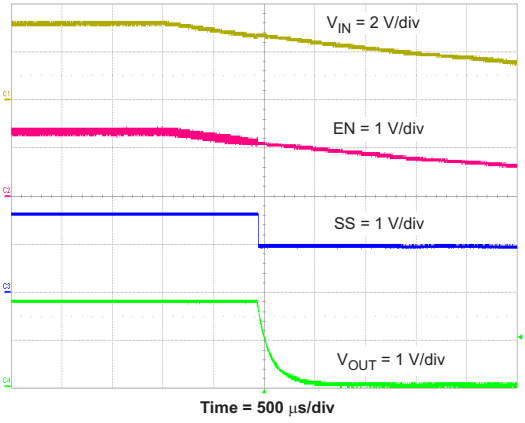

Figure 43. Power-Down, V_{OUT}, V_{IN}

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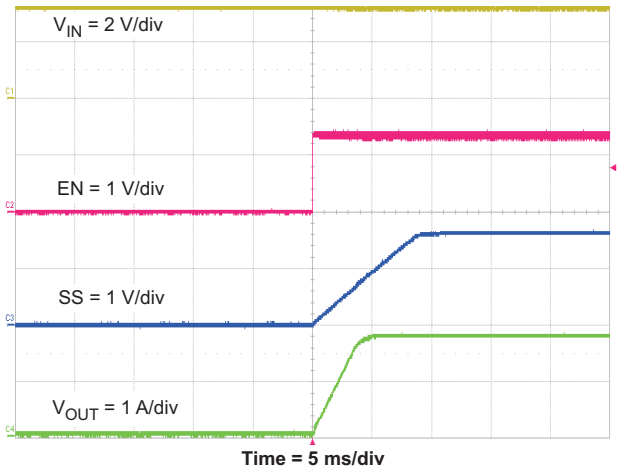

Figure 44. Power-Up, V_{OUT}, EN

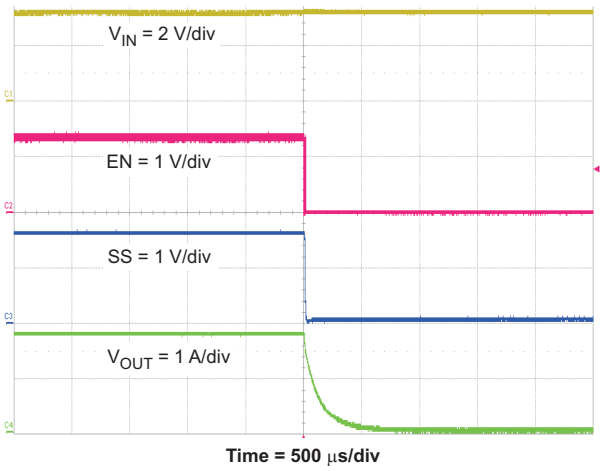

Figure 45. Power-Down, V_{OUT}, EN

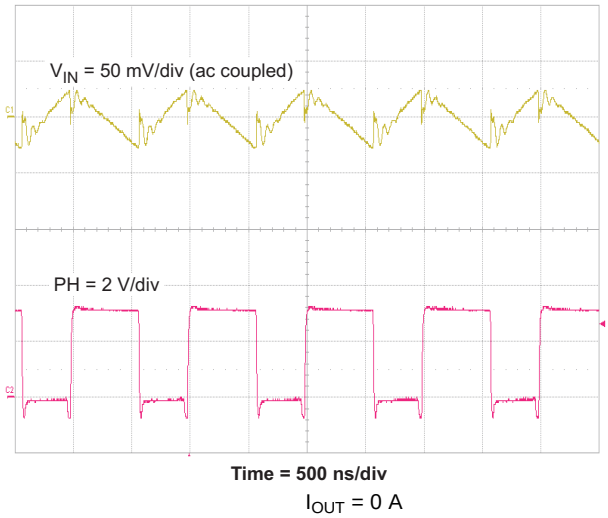

Figure 46. Output Ripple

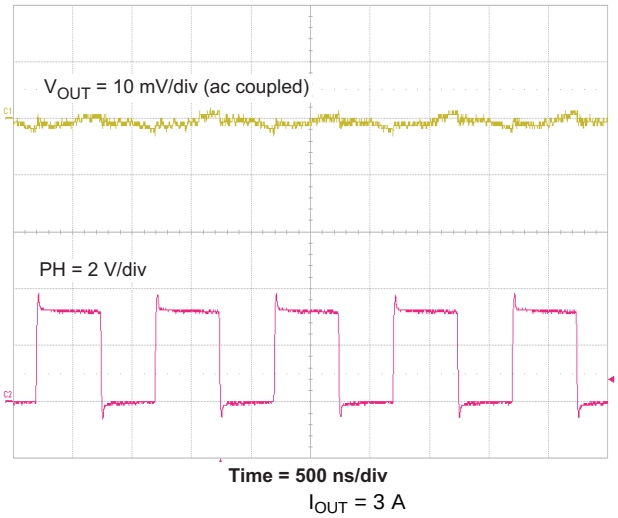

Figure 47. Output Ripple

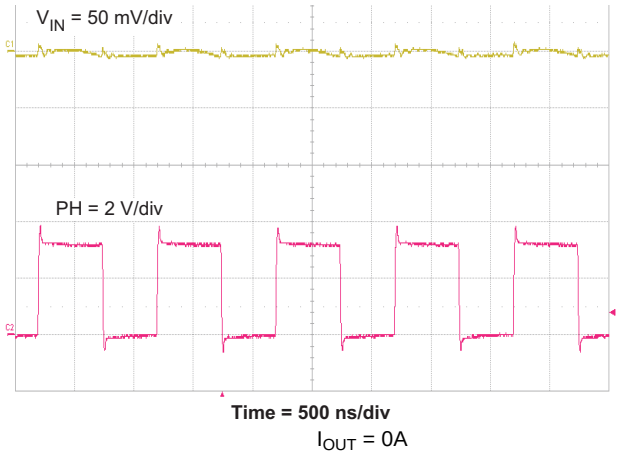

Figure 48. Input Ripple

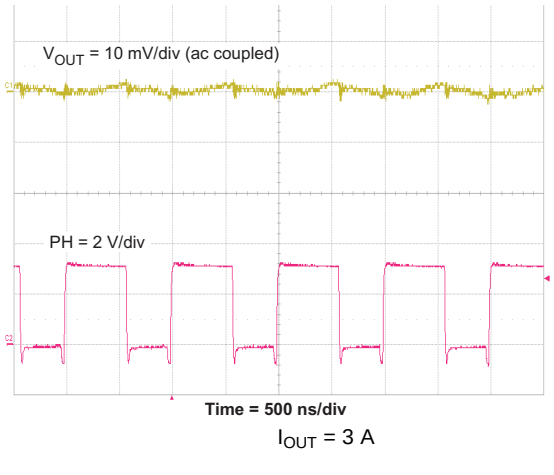

Figure 49. Input Ripple

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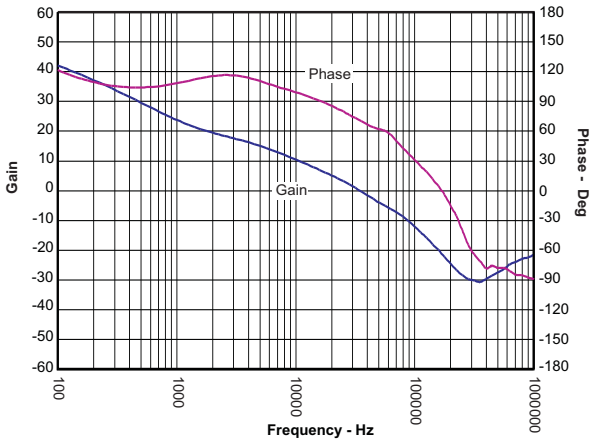

V_{IN} = 3.3. V I_{OUT} = 3 A

Figure 50. Closed-Loop Response

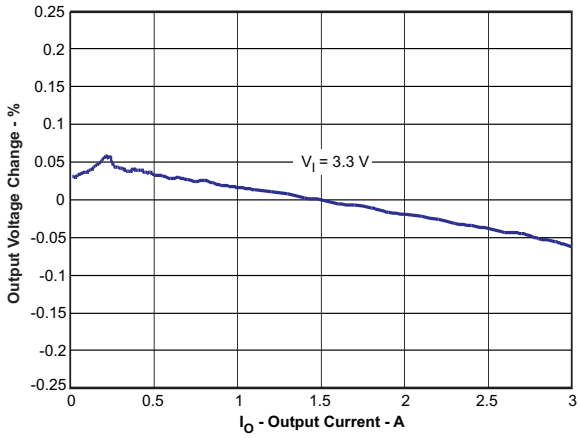

Figure 51. Load Regulation vs Load Current

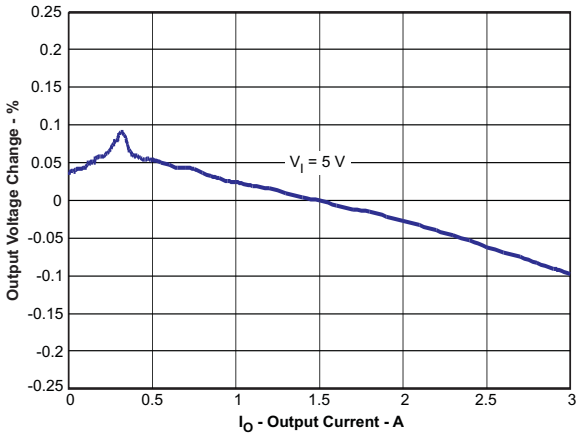

Figure 52. Load Regulation vs Load Current

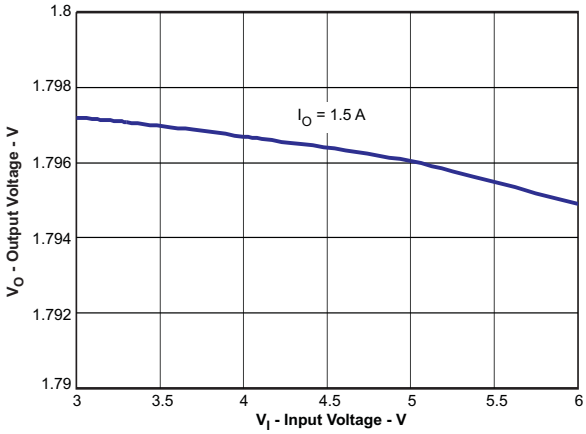

Figure 53. Regulation vs Input Voltage

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10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 2.95 V and 6 V. This supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

- Minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 54 for a PCB layout example.
- The GND pins and AGND pin should be tied directly to the power pad under the TPS54318 device. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the device. Additional vias can be used to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat dissipating area.
- Place the input bypass capacitor as close to the device as possible.
- Route the PH pin to the output inductor. Because the PH connection is the switching node, place the output inductor close to the PH pins. Minimize the area of the PCB conductor to prevent excessive capacitive coupling.
- The boot capacitor must also be located close to the device.
- The sensitive analog ground connections for the feedback voltage divider, compensation components, soft-start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown in Figure 54.
- The RT/CLK pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the device and routed with minimal trace lengths.
- The additional external components can be placed approximately as shown. It is possible to obtain acceptable performance with alternate PCB layouts, however, this layout has been shown to produce good results and can be used as a guide.

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11.2 Layout Example

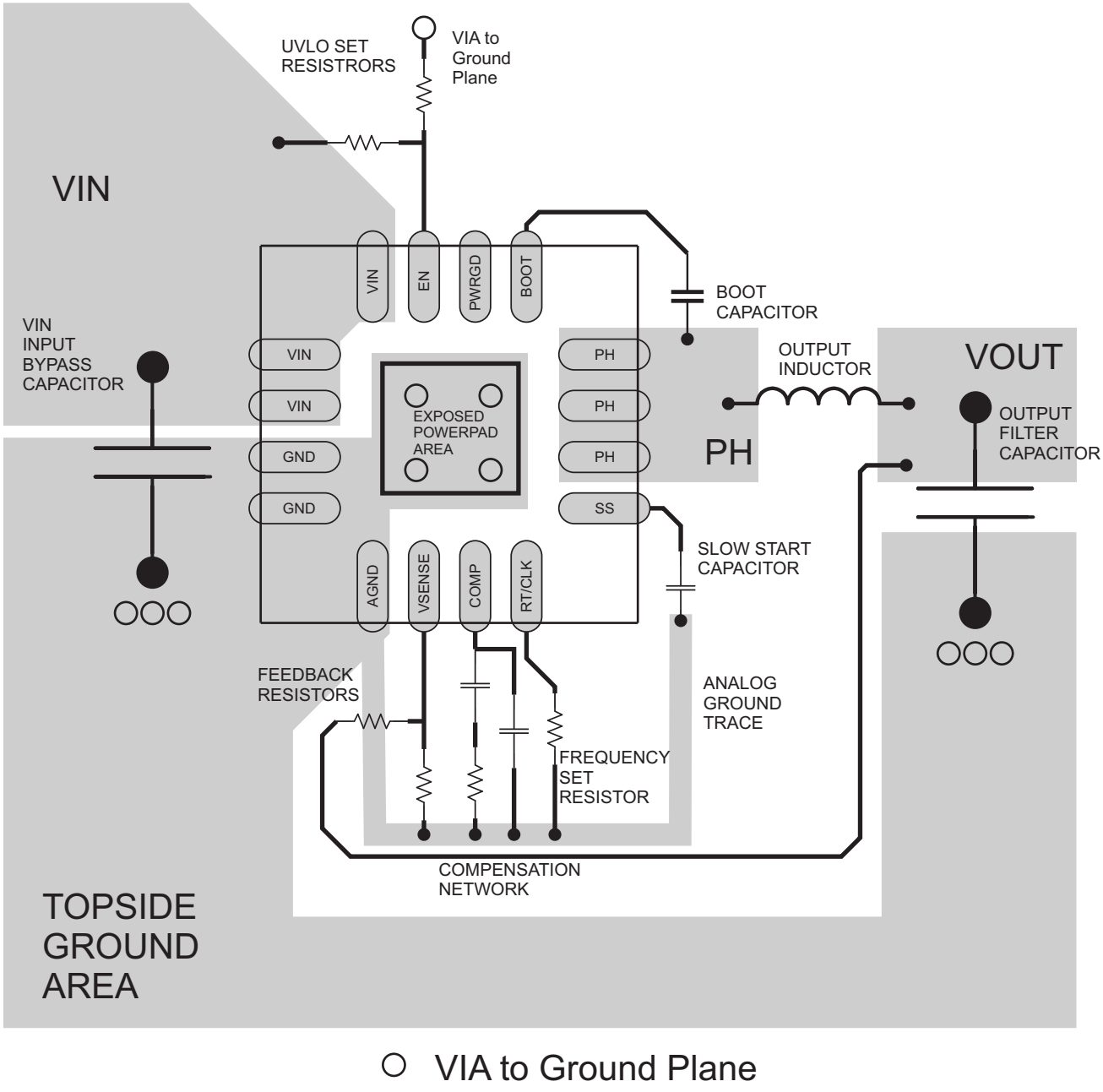

Figure 54. PCB Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、TPS54318デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.1.2 開発サポート

SWIFT™の他のドキュメントについては、TI Webサイトのwww.ti.com/swiftを参照してください。

12.2 商標

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WEBENCH is a registered trademark of Texas Instruments.
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12.3 静電気放電に関する注意事項

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12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS54318RTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318
TPS54318RTER.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318
TPS54318RTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318
TPS54318RTET.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318
TPS54318RTETG4	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318
TPS54318RTETG4.A	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54318

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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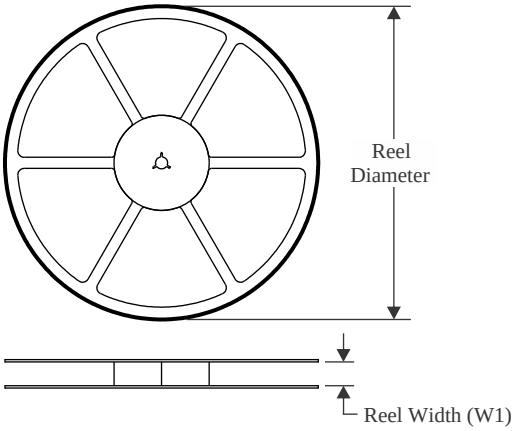
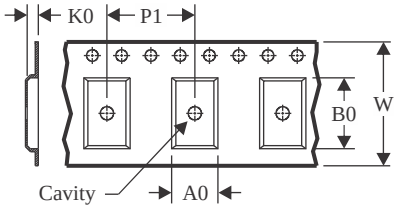
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

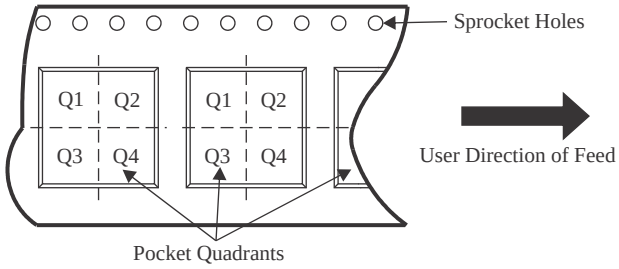


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

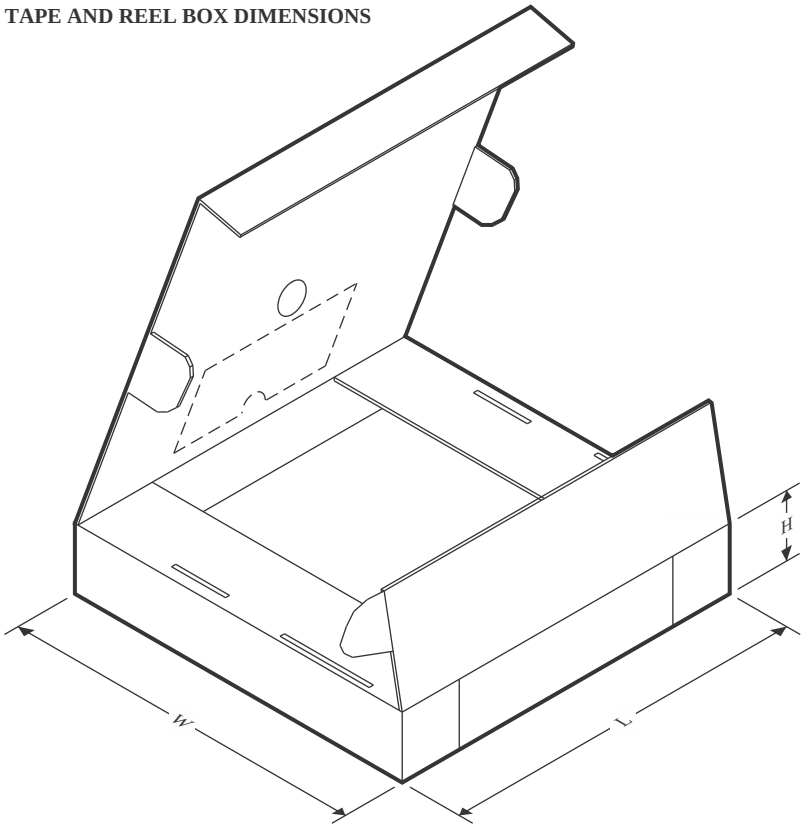
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54318RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54318RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54318RTETG4	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54318RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS54318RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS54318RTETG4	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

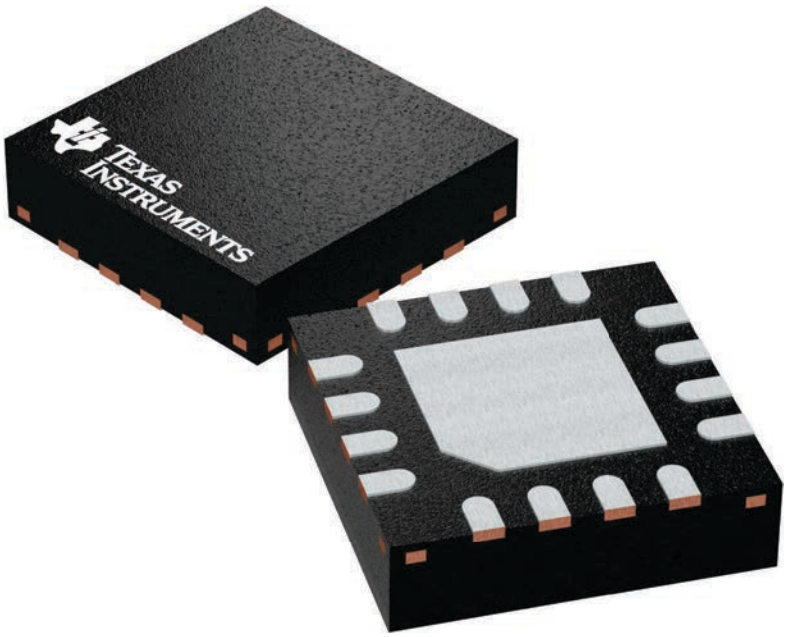
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



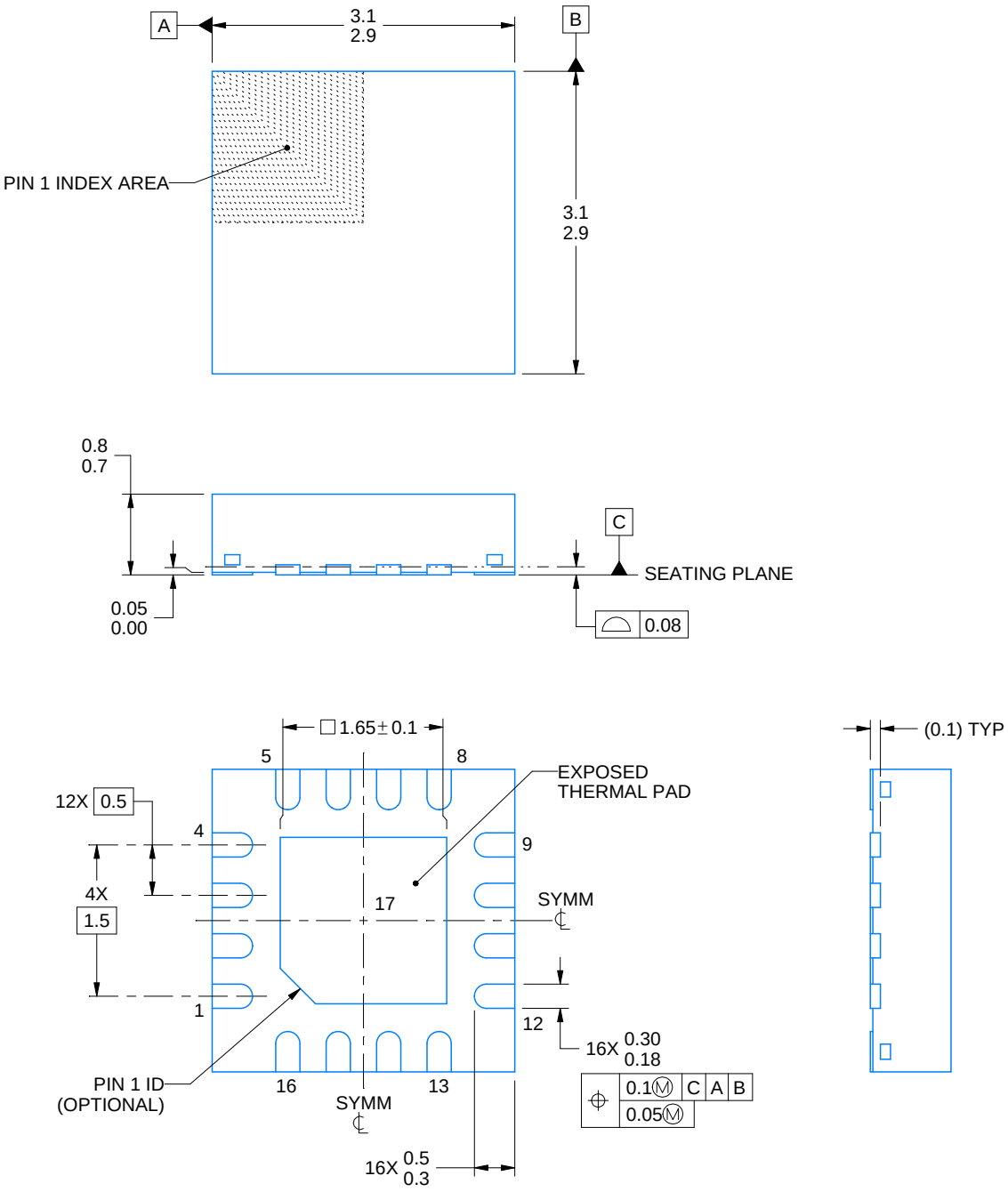
4225944/A

RTE0016F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

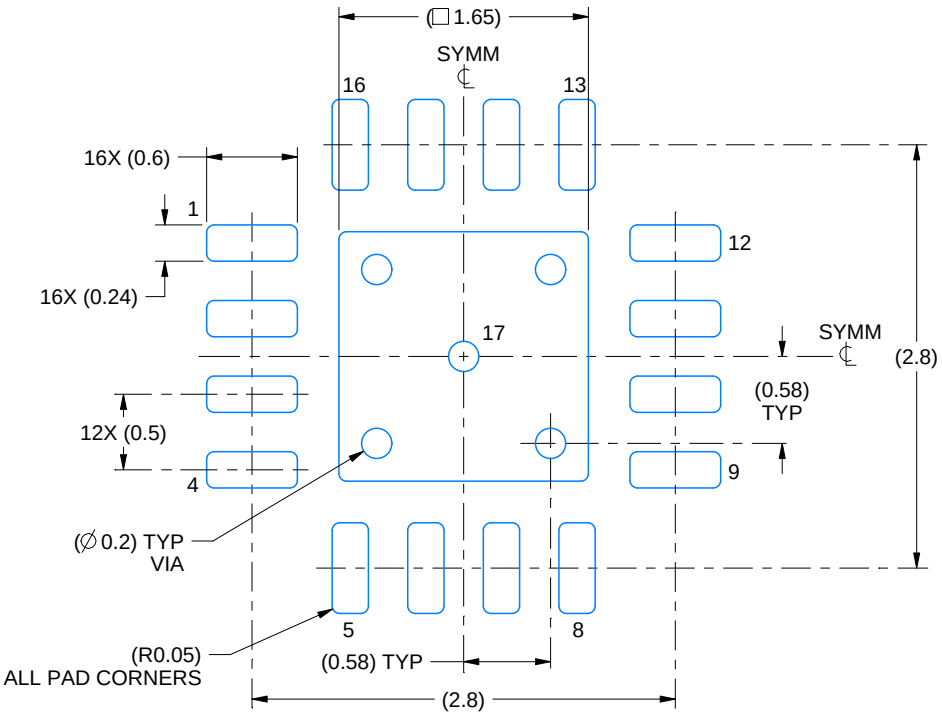
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

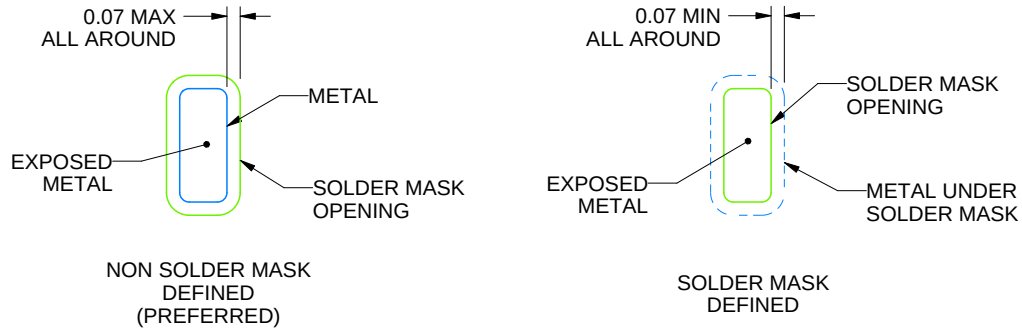
RTE0016F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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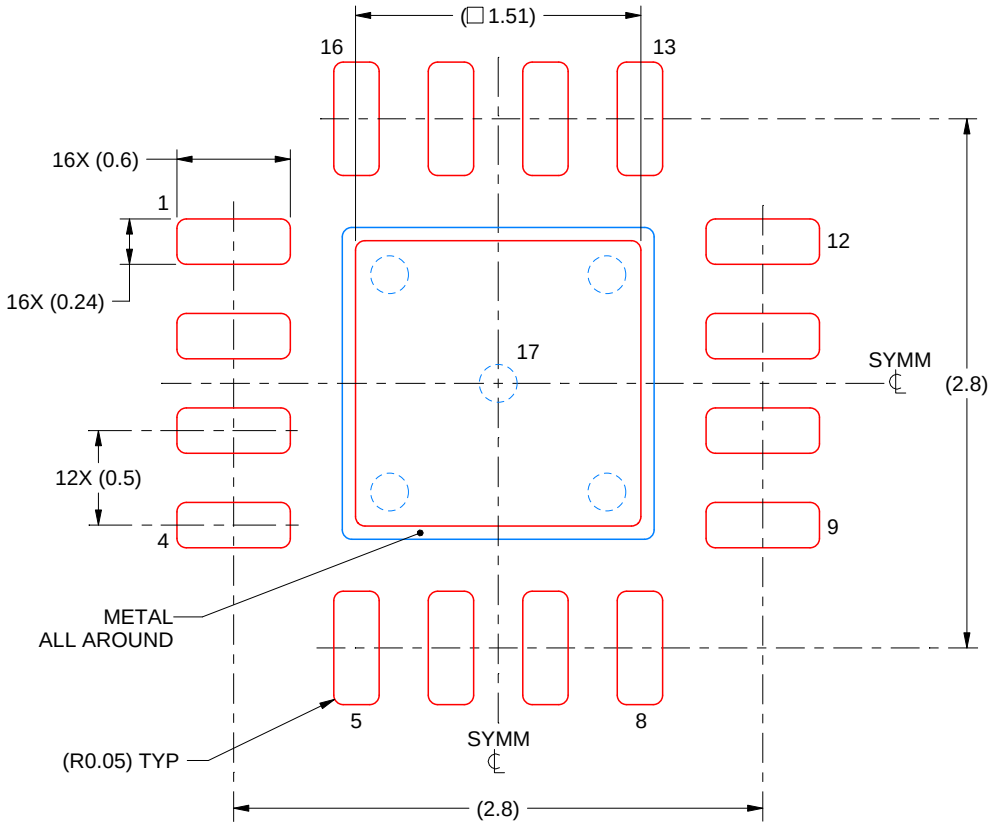
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219119/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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