Digital PWM System Controller

FEATURES

- Fully Configurable Multi-Output and Multi-Phase Non-Isolated DC/DC PWM Controller
- Controls Up to 2 Voltage Rails and Up to 4 Phases
- Supports Switching Frequencies Up to 2MHz with 250 ps Duty-Cycle Resolution
- Up To 1mV Closed Loop Resolution
- Hardware-Accelerated, 3-Pole/3-Zero Compensator with Non-Linear Gain for Improved Transient Performance
- Supports Multiple Soft-Start and Soft-Stop Configurations Including Prebias Start-up
- Supports Voltage Tracking, Margining and Sequencing
- Supports Current and Temperature Balancing for Multi-Phase Power Stages
- Supports Phase Adding/Shedding for Multi-Phase Power Stages
- Sync In/Out Pins Align DPWM Clocks Between Multiple UCD92xx Devices
- 12-Bit Digital Monitoring of Power Supply Parameters Including:
  - Input/Output Current and Voltage
  - Temperature at Each Power Stage
- Multiple Levels of Over-current Fault Protection:
  - External Current Fault Inputs
  - Analog Comparators Monitor Current Sense Voltage
  - Current Continually Digitally Monitored
- Over- and Under-voltage Fault Protection
- Over-temperature Fault Protection
- Enhanced Nonvolatile Memory with Error Correction Code (ECC)
- Device Operates From a Single Supply with an Internal Regulator Controller That Allows Operation Over a Wide Supply Voltage Range
- Supported by Fusion Digital Power™ Designer, a Full Featured PC Based Design Tool to Simulate, Configure, and Monitor Power Supply Performance

APPLICATIONS

- Industrial/ATE
- Networking Equipment
- Telecommunications Equipment
- Servers
- Storage Systems
- FPGA, DSP and Memory Power

DESCRIPTION

The UCD9224 is a multi-rail, multi-phase synchronous buck digital PWM controller designed for non-isolated DC/DC power applications. This device integrates dedicated circuitry for DC/DC loop management with flash memory and a serial interface to support configurability, monitoring and management.

The UCD9224 was designed to provide a wide variety of desirable features for non-isolated DC/DC converter applications while minimizing the total system component count by reducing external circuits. The solution integrates multi-loop management with sequencing, margining, tracking and intelligent phase management to optimize for total system efficiency. Additionally, loop compensation and calibration are supported without the need to add external components.

To facilitate configuring the device, the Texas Instruments Fusion Digital Power™ Designer is provided. This PC based Graphical User Interface offers an intuitive interface to the device. This tool allows the design engineer to configure the system operating parameters for the application, store the configuration to on-chip non-volatile memory and observe both frequency domain and time domain simulations for each of the power stage outputs.

TI has also developed multiple complementary power stage solutions – from discrete drivers in the UCD7k family to fully tested power train modules in the PTD family. These solutions have been developed to complement the UCD9k family of system power controllers.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

OPERATING TEMPERATURE RANGE, T_A	ORDERABLE PART NUMBER	PIN COUNT	SUPPLY	PACKAGE	TOP SIDE MARKING
–40°C to 125°C	UCD9224RGZR	48-pin	Reel of 2500	QFN	UCD9224
	UCD9224RGZT	48-pin	Tray of 250	QFN	UCD9224

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
Voltage applied at V_{33D} to DGND1	–0.3 to 3.8	V
Voltage applied at V_{33A} to AGND	–0.3 to 3.8	V
Voltage applied to any pin(2)	–0.3 to 3.8	V
Storage temperature (T_{STG})	–40 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V	Supply voltage during operation, V_{33D}, V_{33DIO}, V_{33A}	3	3.3	3.6	V
T_A	Operating free-air temperature range(1)	–40		125	°C
T_J	Junction temperature (1)			125	°C

(1) When operating, the UCD9224's typical power consumption causes a 15°C temperature rise from ambient.

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current	V_{33A} = 3.3 V		8	15	mA
I_{V33D}		V_{33D} = 3.3 V		42	55	
I_{V33D}		V_{33D} = 3.3 V storing configuration parameters in flash memory		53	65	
INTERNAL REGULATOR CONTROLLER INPUTS/OUTPUTS						
V_{33}	3.3-V linear regulator	Emitter of NPN transistor	3.25	3.3	3.6	V
V_{33FB}	3.3-V linear regulator feedback			4	4.6	
I_{V33FB}	Series pass base drive	V_{VIN} = 12 V, curent into V_{33FB} pin		10		mA
Beta	Series NPN pass device		40			
EXTERNALLY SUPPLIED 3.3 V POWER						
V_{33D}	Digital 3.3-V power	T_A = 25° C	3.0		3.6	V
V_{33A}	Analog 3.3-V power	T_A = 25°C	3.0		3.6	V

ELECTRICAL CHARACTERISTICS (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER INPUTS EAPn, EANn						
V_{CM}	Common mode voltage each pin		–0.15		1.848	V
V_{ERROR}	Internal error voltage range	AFE_GAIN field of CLA_GAINS = 0(1)	–256		248	mV
EAP-EAN	Error voltage digital resolution	AFE_GAIN field of CLA_GAINS = 3		1		mV
R_{EA}	Input Impedance	Ground reference	0.5	1.5	3	MΩ
I_{OFFSET}	Input offset current	1 kΩ source impedence	–5		5	µA
Vref 10-bit DAC						
V_{ref}	Reference voltage setpoint		0		1.6	V
V_{refres}	Reference voltage resolution			1.56		mV
ANALOG INPUTS CS-1A, CS-1B, CS-2A, CS-3A, V_{in}/I_{in}, Temperature, ADDR-0, ADDR-1, Vtrack, ADCref						
V_{ADDR_OPEN}	Voltage indicating open pin	ADDR-0, ADDR-1 open	2.37			V
V_{ADDR_SHORT}	Voltage indicating shorted pin	ADDR-0, ADDR-1 short to ground			0.36	V
V_{ADC_RANGE}	Measurement range for voltage monitoring	Inputs: V_{in}/I_{in}, V_{track}, $V_{temperature}$ CS-1A, CS-1B, CS-2A, CS-3A	0		2.5	V
V_{OC_THRS}	Over-current comparator threshold voltage range(2)	Inputs: CS-1A, CS-1B, CS-2A, CS-3A	0.032		2	V
V_{OC_RES}	Over-current comparator threshold voltage range	Inputs: CS-1A, CS-1B, CS-2A, CS-3A		31.25		mV
ADCref	External reference input		1.8		V33A	V
$Temp_{internal}$	Int. temperature sense accuracy	Over range from 0°C to 125°C	–5		5	°C
INL	ADC integral nonlinearity		–2.5		2.5	mV
I_{lkg}	Input leakage current	3V applied to pin			100	nA
R_{IN}	Input impedance	Ground reference	8			MΩ
C_{IN}	Current Sense Input capacitance				10	pF
DIGITAL INPUTS/OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(3), V_{33D} = 3 V			DGND1 +0.25	V
V_{OH}	High-level output voltage	I_{OH} = -6 mA(4), V_{33D} = 3 V	V_{33D} –0.6V			V
V_{IH}	High-level input voltage	V_{33D} = 3V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33D} = 3.5 V			1.4	V
SYSTEM PERFORMANCE						
V_{RESET}	Voltage where device comes out of reset	V_{33D} Pin	2.3		2.4	V
t_{RESET}	Pulse width needed for reset	nRESET pin	2			µs
V_{RefAcc}	Setpoint reference accuracy	V_{ref} commanded to be 1V at 25°C, AFEgain = 4, 1V input to EAP/N measured at output of the EADC(5)	–10		10	mV
	Setpoint reference accuracy over temperature	–40°C to 125°C	–20		20	mV
$V_{DiffOffset}$	Differential offset between gain settings	AFEgain = 4 compared to AFEgain = 1, 2, or 8	–4		4	mV
t_{Delay}	Digital compensator delay		240		240 + 1 switching cycle	ns
F_{SW}	Switching frequency		15.260		2000	kHz
Duty	Max and Min duty cycle		0%		100%	
V_{33}Slew	Minimum V_{33} slew rate during power on	V_{33} slew rate between 2.3V and 2.9V, V_{33A} = V_{33D}	0.25			V/ms
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

(1) See the UCD92xx PMBus Command Reference for the description of the AFE_GAIN field of CLA_GAINS command.
(2) Can be disabled by setting to '0'0
(3) The maximum I_{OL}, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(4) The maximum I_{OH}, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.
(5) With default device calibration. PMBus calibration can be used to improve the regulation tolerance

ADC MONITORING INTERVALS AND RESPONSE TIMES

The ADC operates in a continuous conversion sequence that measures each rail's output voltage, each power stage's output current, plus four other variables (external temperature, Internal temperature, input voltage and current, and tracking input voltage). The length of the sequence is determined by the number of output rails (NumRails) and total output power stages (NumPhases) configured for use. The time to complete the monitoring sampling sequence is give by the formula:

$$t_{ADC\_SEQ} = t_{ADC} \times (\text{NumRAILS} + \text{NumPHASE} + 4)$$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ADC}	ADC single-sample time			3.84		µs
t_{ADC_SEQ}	ADC sequencer interval	Min = 1 Rail + 1 Phase + 4 = 6 samples Max = 2 Rails + 4 Phases + 4 = 10 samples	23.04		38.4	µs

The most recent ADC conversion results are periodically converted into the proper measurement units (volts, amperes, degrees), and each measurement is compared to its corresponding fault and warning limits. The monitoring operates asynchronously to the ADC, at intervals shown in the table below.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Vout}	Output voltage monitoring interval			200		µs
t_{Iout}	Output current monitoring interval			200 × NRails		µs
t_{Vin}	Input voltage monitoring interval			2		ms
t_{Iin}	Input current monitoring interval			2		ms
t_{TEMP}	Temperature monitoring interval			100		ms
t_{Ibal}	Output current balancing interval			2		ms

Because the ADC sequencer and the monitoring comparisons are asynchronous to each other, the response time to a fault condition depends on where the event occurs within the monitoring interval and within the ADC sequence interval. Once a fault condition is detected, some additional time is required to determine the correct action based on the FAULT_RESPONSE code, and then to perform the appropriate response. The following table lists the worse-case fault response times.

PARAMETER		TEST CONDITIONS	MAX TIME	UNIT
t_{OVF}, t_{UVF}	Over-/under-voltage fault response time during normal operation	Normal regulation, no PMBus activity, 4 stages enabled	300	µs
	Over-/under-voltage fault response time, during data logging	During data logging to nonvolatile memory (1)	800	µs
	Over-/under-voltage fault response time, when tracking or sequencing enable	During tracking and soft-start ramp.	400	µs
t_{OCF}, t_{UCF}	Over-/under-current fault response time during normal operation	Normal regulation, no PMBus activity, 4 stages enabled 75% to 125% current step	100 + (600 × NRails)	µs
	Over-/under-current fault response time, during data logging	During data logging to nonvolatile memory 75% to 125% current step	600 + (600 × N_{Rails})	µs
	Over-/under-current fault response time, when tracking or sequencing enable	During tracking and soft start ramp 75% to 125% current step	300 + (600 × N_{Rails})	µs
t_{OTF}	Over-temperature fault response time	Temperature rise of 10°C/sec, OT threshold = 100°C	2.5	S

(1) During a STORE_DEFAULT_ALL command, which stores the entire configuration to nonvolatile memory, the fault detection latency can be up to 10 ms.

HARDWARE FAULT DETECTION LATENCY

The controller contains hardware fault detection circuits that are independent of the ADC monitoring sequencer.

PARAMETER		TEST CONDITIONS	MAX	UNIT
t_{FLT}	Time to disable DPWM output based on corresponding active FLT pin	High level on FLT pin	15 + 3 × NumPhases	µs
t_{CLF}	Time to disable the first DPWM output based on internal analog comparator fault	Step change in CS voltage from 0V to 2.5V	4	Switch Cycles
	Time to disable all remaining DPWM and SRE outputs configured for the voltage rail after an internal analog comparator fault	Step change in CS voltage from 0V to 2.5V	10 + 3 × NumPhases	µs

PMBUS/SMBUS/I2C

The timing characteristics and timing diagram for the communications interface that supports I^2C, SMBus and PMBus are shown below.

I^2C/SMBus/PMBus TIMING CHARACTERISTICS

T_A = –40°C to 125°C, 3V < V_{33} < 3.6V, typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB}	SMBus/PMBus operating frequency	Slave mode; SMBC 50% duty cycle	10		1000	kHz
f_{I2C}	I^2C operating frequency	Slave mode; SCL 50% duty cycle	10		1000	kHz
$t_{(BUF)}$	Bus free time between start and stop		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.26			µs
$t_{(SU:STA)}$	Repeated start setup time		0.26			µs
$t_{(SU:STO)}$	Stop setup time		0.26			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		50			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		0.5			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.26		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
t_{FALL}	Clock/data fall time	See (4)			120	ns
t_{RISE}	Clock/data rise time	See (5)			120	ns

(1) The UCD9224 times out when any clock low exceeds t(TIMEOUT).
(2) $t_{(HIGH)}$, max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction involving UCD9224 that is in progress.
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Rise time $t_{RISE} = V_{ILMAX} – 0.15$) to ($V_{IHMIN} + 0.15$)
(5) Fall time $t_{FALL} = 0.9\ V_{33}$ to ($V_{ILMAX} – 0.15$)

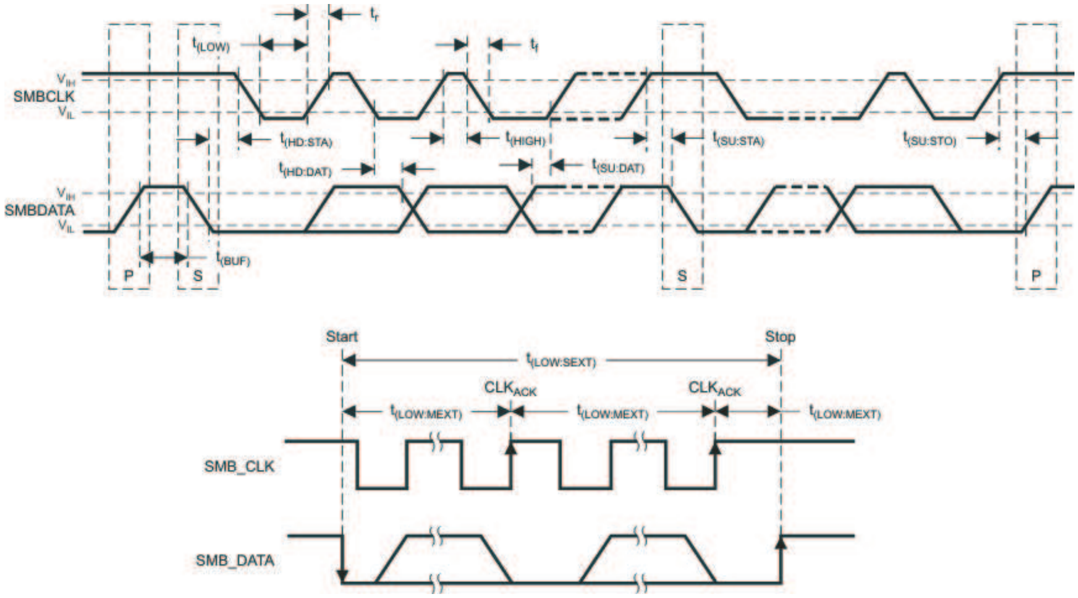

Figure 1. \I2C/SMBus/PMBus Timing in Extended Mode Diagram

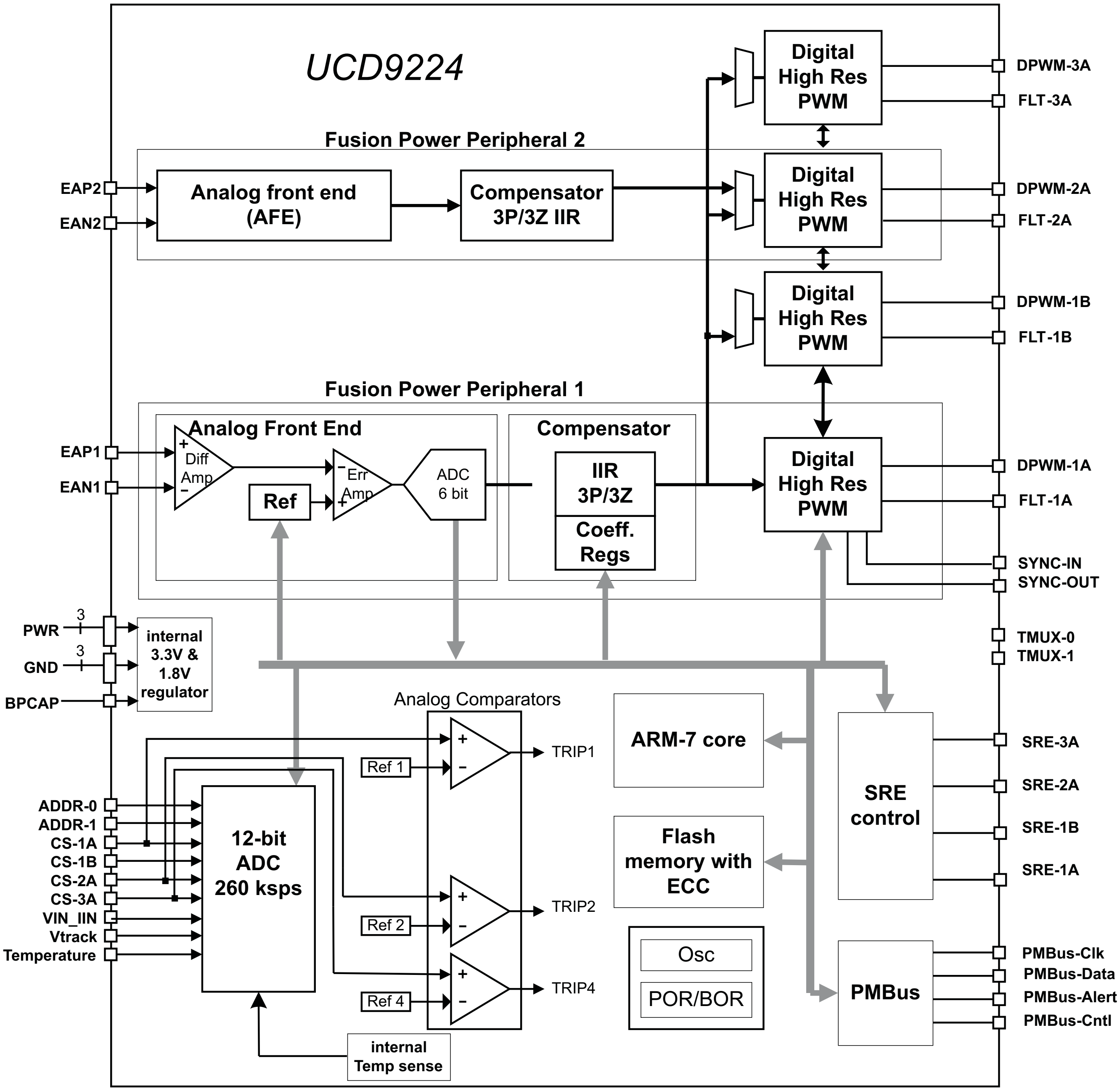

Figure 2. Functional Block Diagram

The UCD9224 is available in an 48-pin QFP package (RGZ).

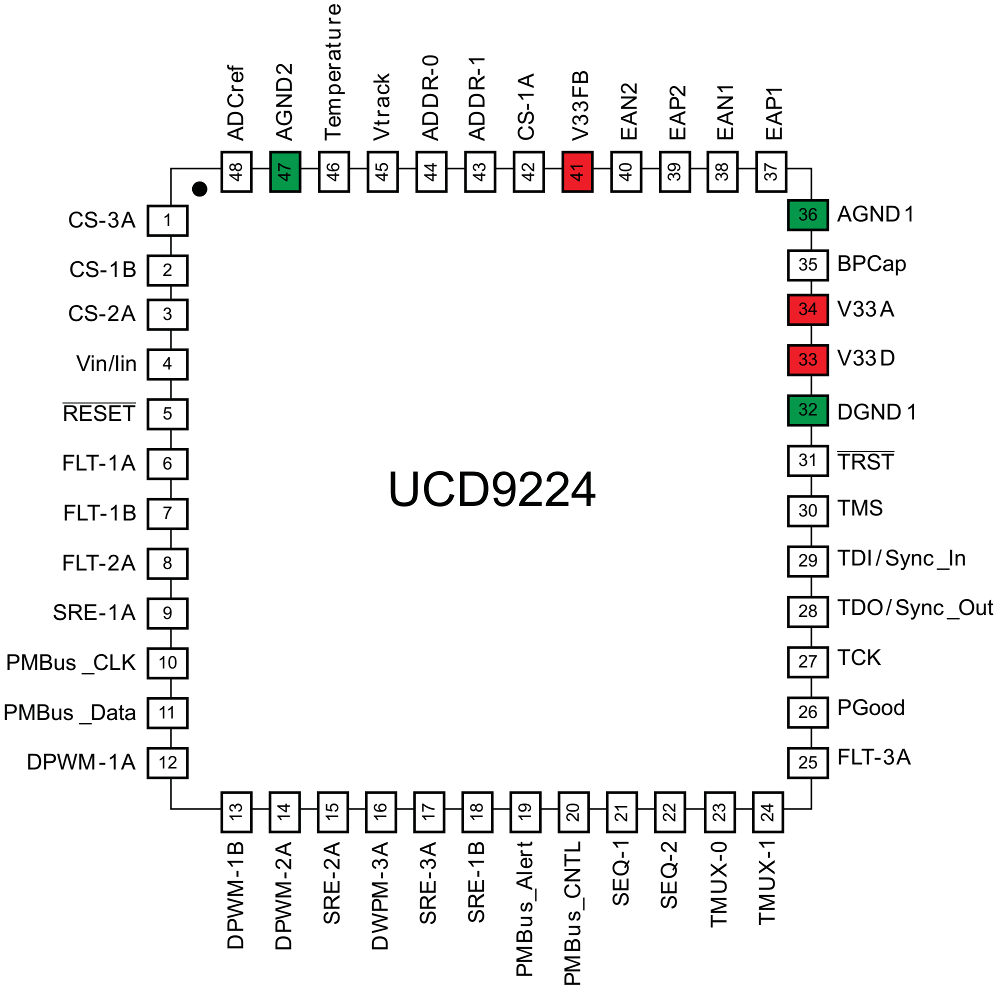

Figure 3. Pin Assignment Diagram

TYPICAL APPLICATION SCHEMATIC

Figure 4 shows the UCD9224 power supply controller as part of a system that provides the regulation of one eight-phase power supply. The loop for the power supply is created by the voltage output feeding into the differential voltage error ADC (EADC) input, and completed by DPWM outputs feeding into the gate drivers for each power stage (PTD modules in this example).

The ±VsA and ±VsB signal must be routed to the EAp/EAn input that matches the number of the lowest DPWM configured as part of the rail. (See more detail in *Flexible Rail/Power Stage Configuration*.)

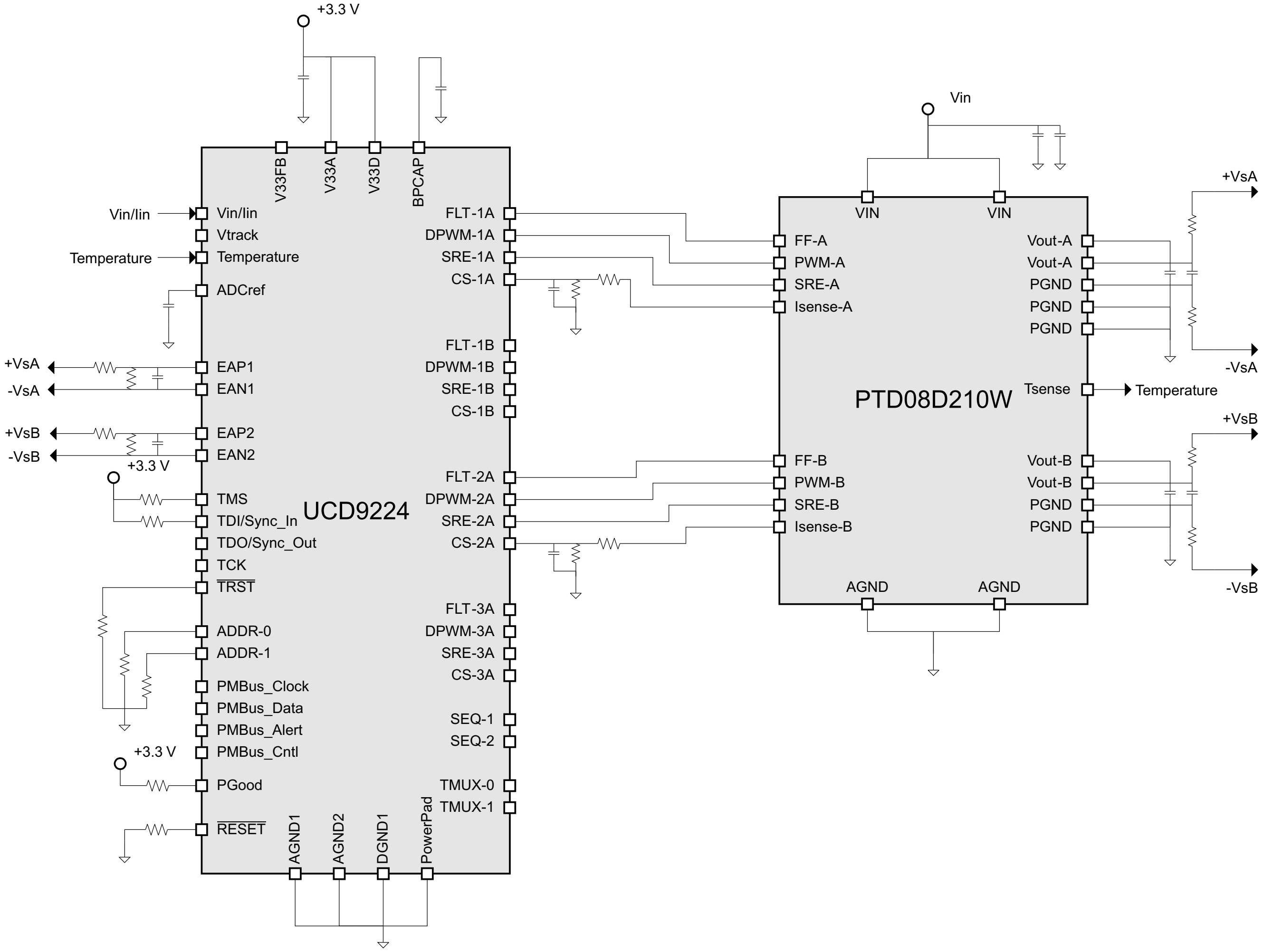

Figure 4. Typical Application Schematic Using PTD Driver Module

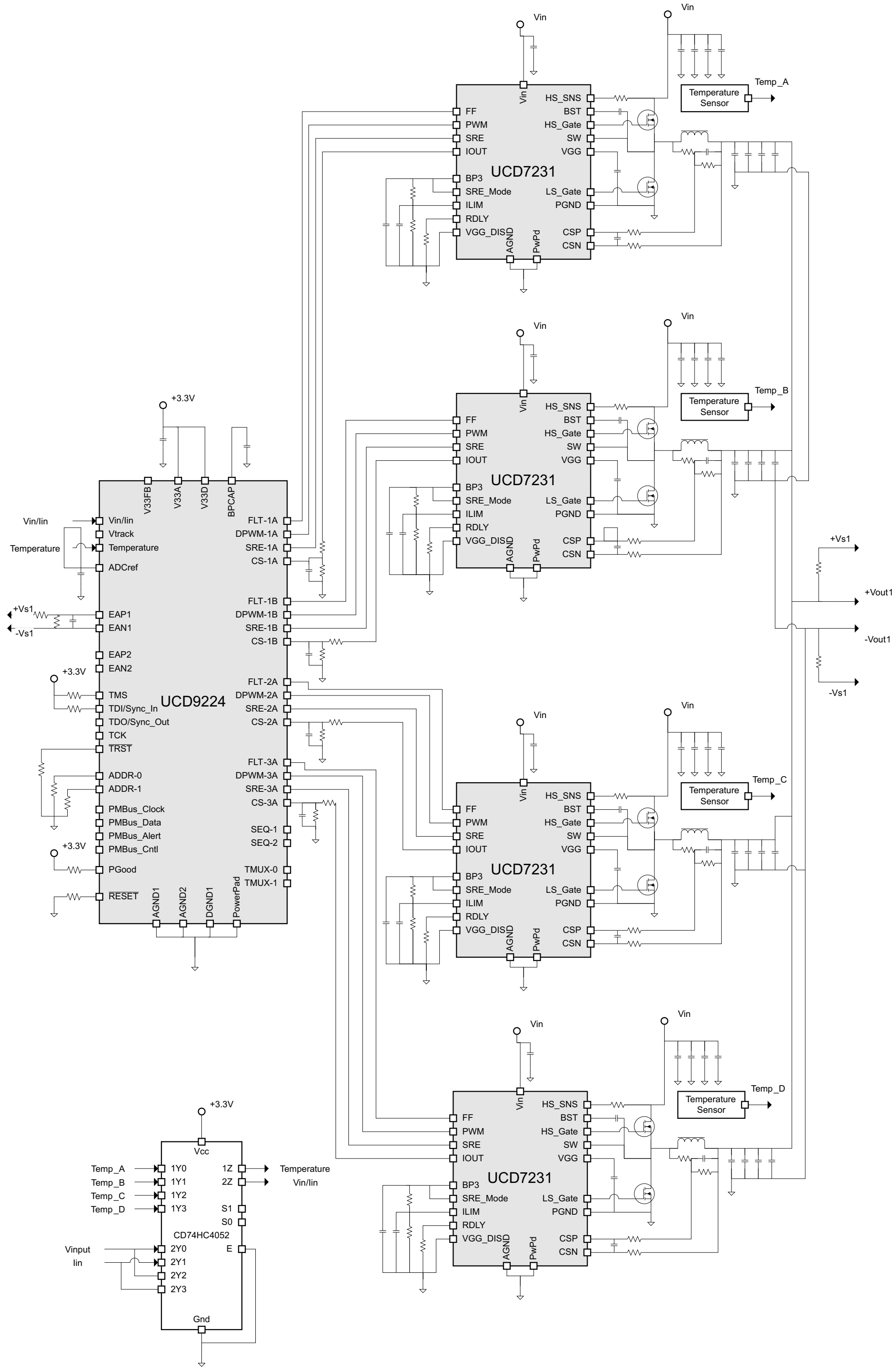

Figure 5. Typical Application Schematic Using UCD7231 Drivers

PIN DESCRIPTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	CS-3A	Power stage 3A current sense input and input to analog comparator 4
2	CS-1B	Power stage 1B current sense input
3	CS-2A	Power stage 2A current sense input and input to analog comparator 2
4	V_{in}/I_{in}	Input supply sense, alternates between V_{in} and I_{in}
5	nRESET	Active low device reset input, pullup to 3.3V with 10kΩ resistor
6	FLT-1A	External fault input 1A, active high
7	FLT-1B	External fault input 1B, active high
8	FLT-2A	External fault input 2A, active high
9	SRE-1A	Synchronous rectifier enable output 1A, active high
10	PMBus_Clock	PMBus Clock, pullup to 3.3V with 2kΩ resistor
11	PMBus_Data	PMBus Data, pullup to 3.3V with 2kΩ resistor
12	DPWM-1A	Digital Pulse Width Modulator output 1A
13	DPWM-1B	Digital Pulse Width Modulator output 1B
14	DPWM-2A	Digital Pulse Width Modulator output 2A
15	SRE-2A	Synchronous rectifier enable output 2A, active high
16	DPWM-3A	Digital Pulse Width Modulator output 3A
17	SRE-3A	Synchronous rectifier enable output 3A, active high
18	SRE-1B	Synchronous rectifier enable output 1B, active high
19	PMBus_Alert	PMBus Alert, pullup to 3.3V with 2kΩ resistor
20	PMBus_Cntl	PMBus Control, pullup to 3.3V with 2kΩ resistor
21	SEQ-1	Sequencing Input/Output
22	SEQ-2	Sequencing Input/Output
23	TMUX-0	Temperature multiplexer select output S0, V_{in}/I_{in} select
24	TMUX-1	Temperature multiplexer select output S1
25	FLT-3A	External fault input 3A, active high
26	PGood	Power Good indication, Active high open-drain output. Pull-up to 3.3V with 10kΩ resistor.
27	TCK	JTAG Test clock
28	TDO / Sync_Out	JTAG Test data out (muxed with Sync_Out for synchronizing switching frequency across devices)
29	TDI / Sync_In	JTAG Test data in (muxed with Sync_In for synchronizing switching frequency across devices) tie to V33D with 10kOhm resistor
30	TMS	JTAG Test mode select – tie to V33D with 10kΩ resistor
31	nTRST	JTAG Test reset – tie to ground with 10kΩ resistor
32	DGND1	Digital ground
33	V33D	Digital core 3.3V supply
34	V33A	Analog 3.3V supply
35	BPCap	1.8V bypass capacitor connection
36	AGND1	Analog ground
37	EAP1	Error analog, differential voltage. Positive channel #1 input
38	EAN1	Error analog, differential voltage. Negative channel #1 input
39	EAP2	Error analog, differential voltage. Positive channel #2 input
40	EAN2	Error analog, differential voltage. Negative channel #2 input
41	V33FB	Connection to the base of the 3.3V linear regulator transistor. (no connect if not using an external transistor)
42	CS-1A	Power stage 1A current sense input and input to analog comparator 1
43	ADDR-1	Address sense input. Channel 1
44	ADDR-0	Address sense input. Channel 0
45	Vtrack	Voltage track input

PIN NO.	PIN NAME	DESCRIPTION
46	Temperature	Temperature sense input
47	AGND2	Analog ground
48	ADCref	ADC Decoupling capacitor – tie 0.1µF capacitor to ground
PowerPad	PowerPad	It is recommended that this pad be connected to analog ground

FUNCTIONAL OVERVIEW

The UCD9224 contains two fusion power peripherals (FPP). Each FPP can be configured to regulated up to four DC/DC converter outputs. There are four PWM outputs that can be assigned to drive the converter outputs. Each FPP consists of:

- A differential input error voltage amplifier
- A 10-bit DAC used to set the output regulation reference voltage.
- A fast ADC with programmable input gain to digitally measure the error voltage.
- A dedicated 3-pole/3-zero digital filter to compensate the error voltage.
- A digital PWM (DPWM) engine that generates the PWM pulse width based on the compensator output.

Each controller is configured through a PMBus serial interface.

PMBus Interface

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface that is built on the I^2C physical specification. The UCD9224 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD9224, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the *UCD92xx PMBUS Command Reference*.

The UCD9224 is PMBus compliant, in accordance with the "Compliance" section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support 100 kHz, 400 kHz, or 1 MHz PMBus operation.

Resistor Programmed PMBus Address Decode

Two pins are allocated to decode the PMBus address. At power-up, the device applies a bias current to each address detect pin, and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows:

PMBus Address = 12 × PMBus Address 1 + PMBus Address 0

Where PMBus Address 1 and 0 are selected from Table 1.

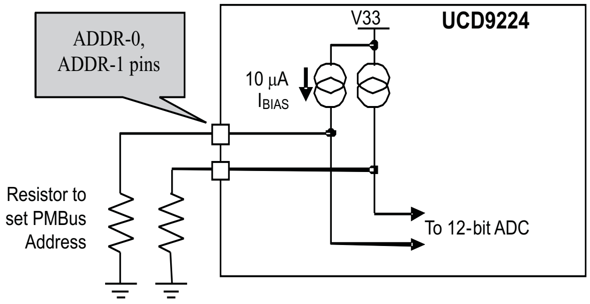

Figure 6. PMBus Address Detection Method

Table 1. PMBus Address Bins

PMBus ADDRESS	R_{PMBus} PMBus RESISTANCE (kΩ)
open	–
11	205
10	178
9	154
8	133
7	115
6	100

Table 1. PMBus Address Bins (continued)

PMBus ADDRESS	R_{PMBus} PMBus RESISTANCE (kΩ)
5	86.6
4	75
3	64.9
2	56.2
1	48.7
0	42.2
short	–

A low impedance (short) on either address pin that produces a voltage below the minimum voltage causes the PMBus address to default to address 126. A high impedance (open) on either address pin that produces a voltage above the maximum voltage also causes the PMBus address to default to address 126.

Some addresses should be avoid, see Table 2

Table 2. PMBus Address Assignment Rules

ADDRESS	STATUS	REASON
0	Prohibited	SMBus generall address call
1-10	Avaliable	
11	Avoid	Causes confilcts with other devices during program flash updates.
12	Prohibited	PMBus alert response protocol
13–125	Avaliable	
126	Avoid	Default value; may cause conflicts with other devices.
127	Prohibited	Used by TI manufacturing for device tests.

JTAG Interface

The JTAG interface can provide an alternate interface for programming the device. It is disabled by default in order to enable the Sync_Out and Sync_In pins with which it is multiplexed. There are three conditions under which the JTAG interface is enabled:

1. When the ROM_MODE PMBus command is issued.
2. On power-up if the Data Flash is blank. This allows JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction.
3. When an invalid address is detected at power-up. By opening or shorting one of the address pins to ground, an invalid address can be generated that enables JTAG. When the JTAG port is enabled the JTAG pins are not available as sequencing pins.

Bias Supply Generator (Shunt Regulator Controller)

Internally, the circuits in the UCD9224 require 3.3V to operate. This can be provided using an existing 3.3V supply or it can be generated from the power supply input voltage using an internal shunt regulator and an external transistor. The requirements for the external transistor are that it be an NPN device with a beta of at least 40. Figure 7 shows the typical application using the external series pass transistor. The base of the transistor is driven by a resistor to Vin and a transconduction amplifier whose output is on the V33FB pin. The NPN emitter becomes the 3.3 V supply for the chip and requires bypass capacitors of 0.1 µF and 4.7 µF.

The transconductance amplifier sinks current into the V33FB pin, in order to regulate the amount of current allowed into the base of the transistor, which regulates the collector current, which determines the emitter voltage (3.3V). The resistor value should be sized low enough to give sufficient base drive at minimum input voltage, yet large enough to not exceed the maximum current sink capability of the V33FB pin at maximum input voltage. Higher beta transistors help in increasing the minimum resistance value, as less base current is needed to sufficiently drive the higher beta transistor. A resistor value of 10kΩ works well for most applications that use the FCX491A BJT

Some circuits in the device require 1.8V that is generated internally from the 3.3V supply. This voltage requires a 0.1 µF to 1 µF bypass capacitor from BPCap to ground.

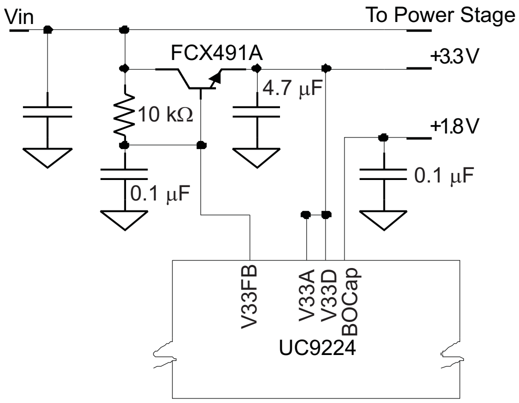

Figure 7. Series-Pass 3.3V Regulator Controller I/O

Power On Reset

The UCD9224 has an integrated power-on reset (POR) circuit that monitors the supply voltage. At power-up, the POR circuit detects the V33D rise. When V33D is greater than V_{RESET}, the device initiates an internal startup sequence. At the end of the delay sequence, the device begins normal operation, as defined by the downloaded device PMBus configuration.

External Reset

The device can be forced into the reset state by an external circuit connected to the nRESET pin. A logic low voltage on this pin holds the device in reset. To avoid an erroneous trigger caused by noise, a 10 kΩ pull up resistor to 3.3V is recommended.

Output Voltage Adjustment

The nominal output voltage is programmed by a combination of PMBus commands: VOUT_COMMAND, VOUT_CAL_OFFSET, VOUT_SCALE_LOOP, and VOUT_MAX. Their relationship is shown in Figure 8. These PMBus parameters need to be set such that the resulting Vref DAC value does not exceed the maximum value of V_{ref}.

Output voltage margining is configured by the VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW commands. The OPERATION command selects between the nominal output voltage and either of the margin voltages. The OPERATION command also includes an option to suppress certain voltage faults and warnings while operating at the margin settings.

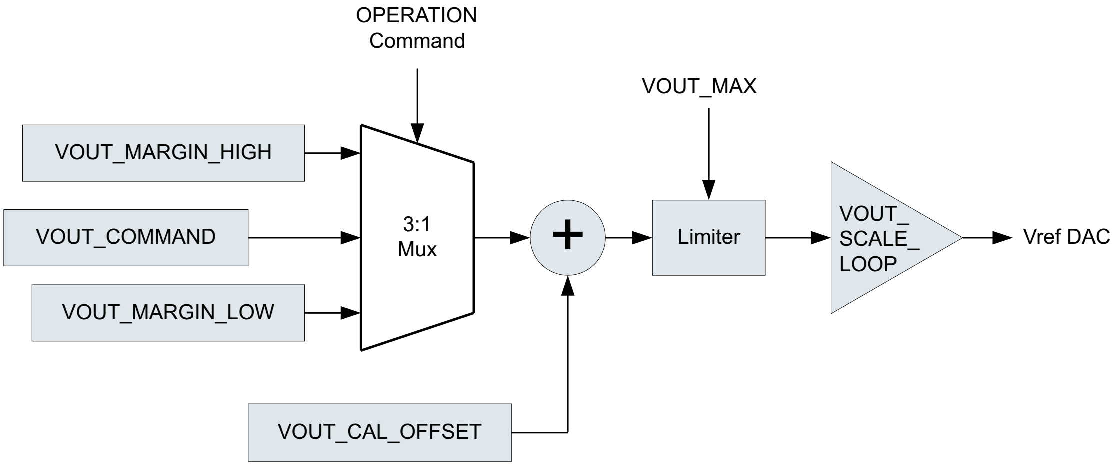

Figure 8. PMBus Voltage Adjustment Methods

For a complete description of the commands supported by the UCD9224 see the UCD92xx PMBUS Command Reference (SLUU337). Each of these commands can also be issued from the Texas Instruments Fusion Digital Power™ Designer program. This Graphical User Interface (GUI) PC program issues the appropriate commands to configure the UCD9224 device.

Calibration

To optimize the operation of the UCD9224, PMBus commands are supplied to enable fine calibration of output voltage, output current, and temperature measurements. The supported commands and related calibration formulas may be found in the UCD92xx PMBUS Command Reference (SLUU337).

Analog Front End (AFE)

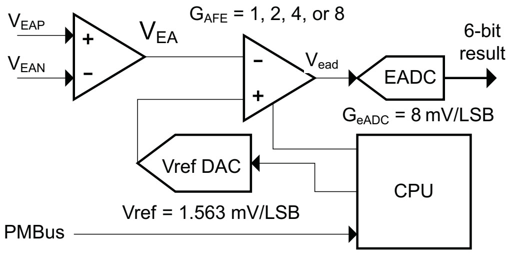

Figure 9. Analog Front End Block Diagram

The UCD9224 senses the power supply output voltage differentially through the EAP and EAN pins. The error amplifier utilizes a switched capacitor topology that provides a wide common mode range for the output voltage sense signals. The fully differential nature of the error amplifier also ensures low offset performance.

The output voltage is sampled at a programmable time (set by the EADC_SAMPLE_TRIGGER PMBus command). When the differential input voltage is sampled, the voltage is captured in internal capacitors and then transferred to the error amplifier where the value is subtracted from the set-point reference which is generated by the 10-bit Vref DAC as shown in Figure 9. The resulting error voltage is then amplified by a programmable gain circuit before the error voltage is converted to a digital value by the error ADC. This programmable gain is configured through the PMBus and affects the dynamic range and resolution of the sensed error voltage as shown in Table 3.

Table 3. Analog Front End Resolution

AFE_GAIN for PMBus COMMAND	AFE GAIN	EFFECTIVE ADC RESOLUTION (mV)	DIGITAL ERROR VOLTAGE DYNAMIC RANGE (mV)
0	1	8	–256 to 248
1	2	4	–128 to 124
2	4	2	–64 to 62
3	8	1	–32 to 31

The AFE variable gain is one of the compensation coefficients that are stored when the device is configured by issuing the CLA_GAINS PMBus command. Compensator coefficients are arranged in several banks: one bank for start/stop ramp or tracking, one bank for normal regulation mode and one bank for light load mode. This allows the user to trade-off resolution and dynamic range for each operational mode.

The EADC, which samples the error voltage, has high accuracy, high resolution, and a fast conversion time. However, its range is limited as shown in Table 3. If the output voltage is different from the reference by more than this, the EADC reports a saturated value at –32 LSBs or 31 LSBs. The UCD9224 overcomes this limitation by adjusting the Vref DAC up or down in order to bring the error voltage out of saturation. In this way, the effective range of the ADC is extended. When the EADC saturates, the Vref DAC is slewed at a rate of 0.156 V/ms, referred to the EA differential inputs.

The differential feedback error voltage is defined as $V_{EA} = V_{EAP} – V_{EAN}$. An attenuator network using resistors R1 and R2 (see Figure 10) should be used to ensure that V_{EA} does not exceed the maximum value of V_{ref} when operating at the commanded voltage level. The commanded voltage level is determined by the PMBus settings described in the *Output Voltage Adjustment* section.

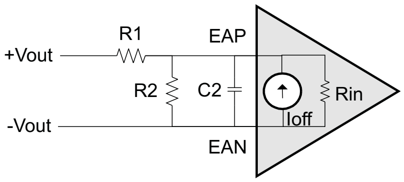

Figure 10. Input Offset Equivalent Circuit

Voltage Sense Filtering

Conditioning should be provided on the EAP and EAN signals. Figure 10 shows a divider network between the output voltage and the voltage sense input to the controller. The resistor divider is used to bring the output voltage within the dynamic range of the controller. When no attenuation is needed, R2 can be left open and the signal conditioned by the low-pass filter formed by R1 and C2.

As with any power supply system, maximize the accuracy of the output voltage by sensing the voltage directly across an output capacitor as close to the load as possible. Route the positive and negative differential sense signals as a balanced pair of traces or as a twisted pair cable back to the controller. Put the divider network close to the controller. This ensures that there is low impedance driving the differential voltage sense signal from the voltage rail output back to the controller. The resistance of the divider network is a trade-off between power loss and minimizing interference susceptibility. A parallel resistance (R_P) of 1kΩ to 4kΩ is a good compromise. Once R_P is chosen, R_1 and R_2 can be determined from the following formulas.

$$R_1 = \frac{R_P}{K} \tag{1}$$

$$R_2 = \frac{R_p}{1 - K} \tag{2}$$

Where

$$K = \frac{V_{EA}}{V_{OUT}} \cong \text{VOUT\_SCALE\_LOOP} \tag{3}$$

It is recommended that a capacitor be placed across the lower resistor of the divider network. This acts as an additional pole in the compensation and as an anti-alias filter for the EADC. To be effective as an anti-alias filter, the corner frequency should be 35% to 40% of the switching frequency. Then the capacitor is calculated as:

$$C_2 = \frac{1}{2\pi \times 0.35 \times F_{SW} \times R_P} \tag{4}$$

To obtain the best possible accuracy, the input resistance and offset current on the device should be considered when calculating the gain of a voltage divider between the output voltage and the EA sense inputs of the UCD9224. The input resistance and input offset current are specified in the parametric tables in this datasheet. $V_{EA} = V_{EAP} – V_{EAN}$ in the equation below.

$$V_{EA} = \frac{R_2}{R_1 + R_2 + \left(\frac{R_1R_2}{R_{EA}}\right)} V_{OUT} + \frac{R_1R_2}{R_1 + R_2 + \left(\frac{R_1R_2}{R_{EA}}\right)} I_{OFFSET} \tag{5}$$

The effect of the offset current can be reduced by making the resistance of the divider network low.

Digital Compensator

Each voltage rail controller in the UCD9224 includes a digital compensator. The compensator consists of a nonlinear gain stage, followed by a digital filter consisting of a second order infinite impulse response (IIR) filter section cascaded with a first order IIR filter section.

The Texas Instruments Fusion Digital Power™ Designer development tool can be used to assist in defining the compensator coefficients. The design tool allows the compensator to be described in terms of the pole frequencies, zero frequencies and gain desired for the control loop. In addition, the Fusion Digital Power™ Designer can be used to characterize the power stage so that the compensator coefficients can be chosen based on the total loop gain for each feedback system. The coefficients of the filter sections are generated through modeling the power stage and load.

Additionally, the UCD9224 has three banks of filter coefficients: Bank-0 is used during the soft start/stop ramp or tracking; Bank-1 is used while in regulation mode; and Bank-2 is used when the measured output current is below the configured light load threshold.

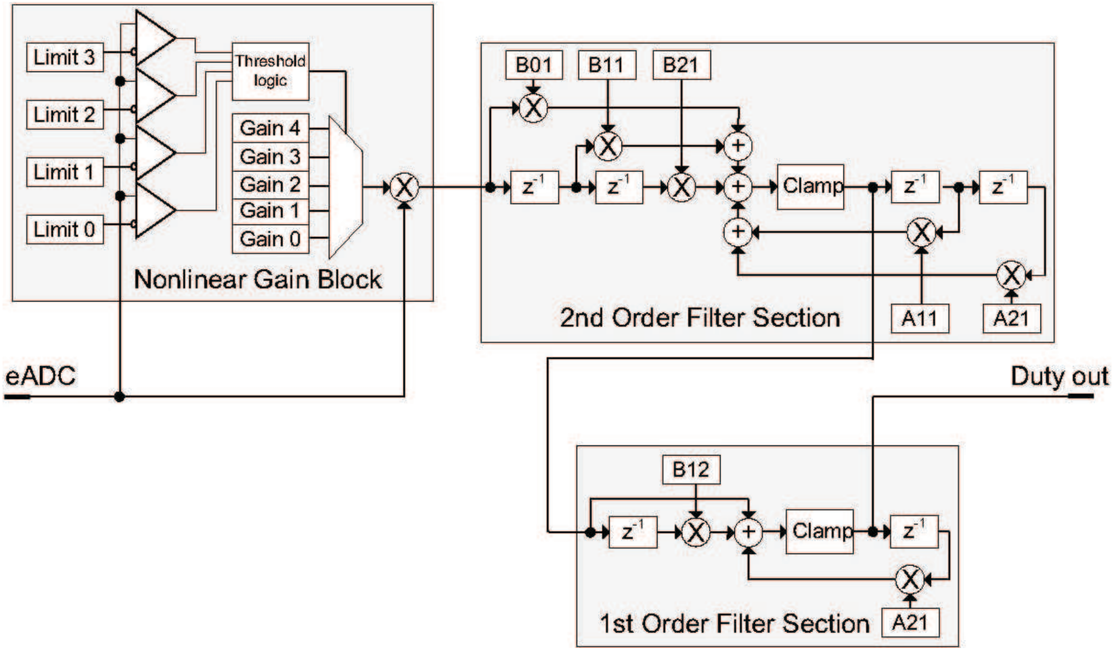

Figure 11. Digital Compensation

The nonlinear gain block allows a different gain to be applied to the system when the error voltage deviates from zero. Typically Limit 0 and Limit 1 would be configured with negative values between –1 and –32 and Limit 2 and Limit 3 would be configured with positive values between 1 and 31. However, the gain thresholds do not have to be symmetrical. For example, the four limit registers could all be set to positive values causing the Gain 0 value to set the gain for all negative errors and a nonlinear gain profile would be applied to only positive error voltages.

The cascaded 1st order filter section is used to generate the third zero and third pole.

DPWM Engine

The output of the compensator feeds the high resolution DPWM engine. The DPWM engine produces the pulse width modulated gate drive output from the device. In operation, the compensator calculates the necessary duty cycle as a digital number representing a percentage from 0 to 100%. The duty cycle value is multiplied by the configured period to generate a comparator threshold value. This threshold is compared against the high speed switching period counter to generate the desired DPWM pulse width. This is shown in Figure 12.

Each DPWM engine can be synchronized to another DPWM engine or to an external sync signal via the SYNC_IN pin. The SYNC_OUT pin can be used to synchronize the DPWM engine in another UCD92xx device. Configuration of the synchronization function is done through a MFR_SPECIFIC PMBus command. See the DPWM Synchronization section for more details.

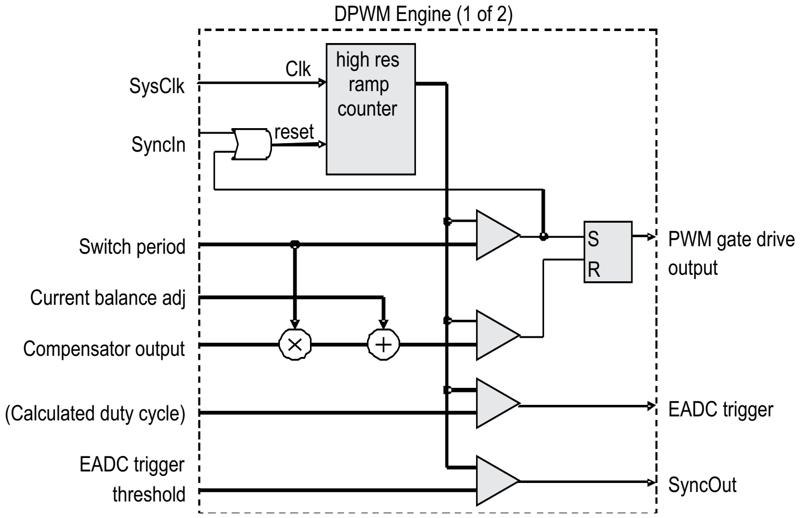

Figure 12. DPWM Engine

Flexible Rail/Power Stage Configuration

The UCD9224 can control one to two voltage rails, each of which can comprise a programmable number of power stages (up to a maximum of four). The following chart shows all possible rail / power stage configurations. Configuration is made through the PHASE_INFO command which is described in detail in the UCD92xx PMBus Command Reference (SLUU337).

Table 4. Power Stage Configuration(1)

NUMBER OF STAGES Rail#1 : Rail#2	POWER STAGES Rail#1	POWER STAGES Rail#2
4:0	1A, 1B, 2A, 3A	(none)
3:0	1A, 1B, 2A	(none)
2:0	1A, 1B	(none)
1:0	1A	(none)
3:1	1A, 1B, 3A	2A
2:1	1A, 1B	2A
1:1	1A	2A
2:2	1A, 1B	2A, 3A
1:2	1A	2A, 3A
1:3	Invalid (use 3:1 instead)	
0:4	Invalid (use 4:0 instead)	
0:3	Invalid (use 3:0 instead)	
0:2	Invalid (use 2:0 instead)	
0:1	Invalid (use 1:0 instead)	

(1) Phases should be selected in the order listed. For a two single phase rail configuration, power stage selections should be 1A and 2A.

DPWM Phase Distribution

When two rails are configured, the UCD9224 offsets (in time) the phase of the 1st power stage assigned to each rail in order to minimize input current ripple. The constant time used for this offset is:

$$t_{\text{rail-rail spread}} = \frac{3}{13} t_{sw} \quad (6)$$

Where t_{SW} is the period of the rail with the fastest switching frequency.

The ratio 3/13 is chosen because it is close to 1/4, but it is a prime ratio. This should ensure that any configuration of rails and power stages should not have the leading edge of the DPWM signal aligned.

The PHASE_INFO PMBus command is also used to configure the number of power stages driving each voltage rail. When multiple power stages are configured to drive a voltage rail, the UCD9224 automatically distributes the phase of each DPWM output to minimize ripple. This is accomplished by setting the rising edge of each DPWM pulse to be separated by:

$$t_{\text{phase-phase spread}} = \frac{t_{sw}}{N_{phases}} \quad (7)$$

Where t_{SW} is the switching period and N_{Phases} is the number of power stages driving a voltage rail.

DPWM Synchronization

DPWM synchronization provides a method to link the timing between rails on two distinct devices at the switching rate; i.e., two rails on different devices can be configured to run at the same frequency and sync forcing them not to drift from each other. (Note that within a single device, because all rails are driven off a common clock there is no need for an internal sync because rails will not drift.)

The PMBus SYNC_IN_OUT command sets which rails (if any) should follow the sync input, and which rail (if any) should drive the sync output.

For rails that are following the sync input, the DPWM ramp timer for that output is reset when the sync input goes high. This allows the slave device to sync to inputs that are faster. There is no limit to how much faster the input is compared to the defined frequency of the rail; when the pulse comes in, the timer is reset and the frequencies are locked. This is the standard mode of operation – setting the slave to run slower, and letting the sync speed it up.

The Sync Input and Output Configuration Word set by the PMBus command consists of two bytes. The upper byte (sync_out) controls which rail drives the sync output signal (0=DPWM1A, 1=DPWM1B, 2=DPWM2A, 3=DPWM3A. Any other value disables sync_out). The lower byte (sync_in) determines which rail(s) respond to the sync input signal (each bit represents one rail – note that multiple rails can be synchronized to the input). The DPWM period is aligned to the sync input. For more information, see the UCD92xx PMBUS Command Reference (SLUU337).

Note that once a rail is synchronized to an external source, the rail-to-rail spacing that attempts to minimize input current ripple is lost. Rail-to-rail spacing can only be restored by power cycling or issuing a SOFT_RESET command.

Phase Shedding at Light Current Load

By issuing LIGHT_LOAD_LIMIT_LOW, LIGHT_LOAD_LIMIT_HIGH, and LIGHT_LOAD_CONFIG commands, the UCD9224 can be configured to shed (disable) power stages when at light load. When this feature is enabled, the device disables the configured number of power stages when the average current drops below the specified LIGHT_LOAD_LIMIT_LOW. In addition, a separate set of compensation coefficients can be loaded into the digital compensator when entering a light load condition.

Phase Adding at Normal Current Load

After shedding phases, if the current load is increased past the LIGHT_LOAD_LIMIT_HIGH threshold, all phases are re-enabled. If the compensator was configured for light load, the normal load coefficients are restored as well. See the UCD92xx PMBUS Command Reference (SLUU337) for more information.

Output Current Measurement

Pins CS-1A, CS-1B, CS-2A, and CS-3A are used to measure either output current or inductor current in each of the controlled power stages. PMBus commands IOUT_CAL_GAIN and IOUT_CAL_OFFSET are used to calibrate each measurement. See the UCD92xx PMBus Command Reference (SLUU337) for specifics on configuring this voltage to current conversion.

If the measured current is outside the range of either the over-current or under-current fault threshold, a current limit fault is declared and the UCD9224 performs the PMBus configured fault recovery. ADC current measurements are digitally averaged before they are compared against the over-current and under-current warning and fault thresholds. The output current is measured at a rate of one output rail per t_{Iout} microseconds. The current measurements are then passed through a digital smoothing filter to reduce noise on the signal and prevent false errors. The output of the smoothing filter asymptotically approaches the input value with a time constant that is approximately 3.5 times the sampling interval.

Table 5. Output Current Filter Time Constants

NUMBER OF OUTPUT RAILS	OUTPUT CURRENT SAMPLING INTERVALS (µs)	FILTER TIME CONSTANTS τ (ms)
1	200	0.7
2	400	1.4

For example, with a single rail, the filter has the transfer function characteristics that shows the signal magnitude at the output of the averaging filter due to a sine wave input for a range of frequencies. This plot includes an RC analog low pass network, with a corner frequency of 3 kHz, on the current sense inputs.

This averaged current measurement is used for output current fault detection; see “Over-Current Detection” section.

In response to a PMBus request for a current reading, the device returns an average current value. When the UCD9224 is configured to drive a multi-phase power converter, the device adds the average current measurement for each of the power stages tied to a power rail.

Current Sense Input Filtering

Each power stage current is monitored by the device at the CS pins. There are 3 "A" channel pins and 1 "B" channel pins. The B channel monitors the current with a 12-bit ADC and samples each current sense voltage in turn. The A channels monitor the current with the same12-bit ADC and also monitor the current with a digitally programmable analog comparator. The comparator can be disabled by writing a zero to the FAST_OC_FAULT_LIMIT.

Because the current sense signal is both digitally sampled and compared to the programmable over-current threshold, it should be conditioned with an RC network acting as an anti-alias filter. If the comparator is disabled, the CS input should be filtered at 35% of the sampling rate. An RC network with this characteristic can be calculated as

$$R = 0.45 \, \frac{N_{rails} T_{Iout}}{C} \tag{8}$$

Where N_{rails} is the number of rails configured and T_{Iout} is the sample period for the current sense inputs. Therefore, when the comparator is not used, the recommended component values for the RC network are C = 10 nF and R = 35.7 kΩ.

When the fast over-current comparator is used, the filter corner frequency based on the ADC sample rate may be too slow and a corner frequency that is a compromise between the requirements of fast over-current detection and attenuating aliased content in the sampled current must be sought. In this case, the filter corner frequency can be calculated based on the time to cross the over-current threshold.

$$V_{OC\_thres} = V_{CS\_nom} + \Delta V_{Imon} \left(1 - e^{-t/\tau}\right) \tag{9}$$

Where V_{OC_thres} is the programmed OC comparator threshold, V_{CS_nom} is the nominal CS voltage, ΔV_{Imon} is the change in CS voltage due to an over-current fault and τ is the filter time constant. Using the equation for the comparator voltage above, the RC network values can be calculated as

$$R = \frac{T_{det}}{C} \, \frac{1}{\ln(\Delta V_{Imon}) - \ln(\Delta V_{Imon} - V_{OC\_thres} + V_{CS\_nom})} \tag{10}$$

Where T_{det} is the time to cross the over-current comparator threshold. For T_{det} = 10 µsec, ΔV_{Imon} = 1.5V, V_{OC_thres} = 2.0V and V_{CS_nom} = 1.5V, the corner frequency is 6.4 kHz and the recommended RC network component values are C = 10 nF and R = 2.49 kΩ.

Output Current Balancing

When the UCD9224 is configured to drive multiple power stage circuits from one compensator, current balancing is implemented by adjusting each gate drive output pulse width to correct for current imbalance between the connected power stage sections. The UCD9224 balances the current by monitoring the current at the CS analog input for each power stage and then adding a current balance adjustment value to the DPWM ramp threshold value for each power stage.

When there is more than one power stage connected to the voltage rail, the device continually determines which stage has the highest measured current and which stage has the lowest measured current. To balance the currents while maintaining a constant total current, the adjustment value for the power stage with the lowest current is increased by the same amount as the adjustment value for the power stage with the highest current is decreased. A slight modification to this algorithm is made to keep the adjustment values positive in order to ensure that a positive DPWM duty cycle is commanded under all conditions.

Over-Current Detection

Several mechanisms are provided to sense output current fault conditions. This allows for the design of power systems with multiple layers of protection.

1. An integrated gate driver, such as the UCD72xx family of integrated gate drivers, can be used to generate the FLT signal. The driver monitors the voltage drop across the high side FET and if it exceeds a resistor/voltage programmed threshold, the driver activates its fault output. The FLT input can be disabled by reconfiguring the FLT pin to be a sequencing pin in the GUI. A logic high signal on the FLT input causes a hardware interrupt to the internal CPU. The CPU then determines which DPWM outputs are configured to be associated with the voltage rail that contained the fault and disables those DPWM and SRE outputs. This process takes about 14 microseconds.
2. Inputs CS-1A, CS-1B, CS-2A and CS-3A each drive an internal analog comparator. These comparators can be used to detect the voltage output of a current sense circuit. Each comparator has a separate PMBus configurable threshold. This threshold is set by issuing the FAST_OC_FAULT_LIMIT command. Though the command is specified in amperes, the hardware threshold is programmed with a value between 31mV and 2V in 64 steps. The relationship between amperes to sensed volts is configured by issuing the IOUT_CAL_GAIN command. When the current sense voltage exceeds the configured threshold the corresponding DPWM and SRE outputs are driven low on the voltage rail with the fault.
3. Each Current Sense input to the UCD9224 is also monitored by the 12-bit ADC. Each measured value is scaled using the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands. The currents for each power stage configured as part of a voltage rail are summed and compared to the over-current limit set by the IOUT_OC_FAULT_LIMIT command. The action taken when a fault is detected is defined by the IOUT_OC_FAULT_RESPONSE command.

Because the current measurement is averaged with a smoothing filter, the response time to an over-current condition depends on a combination of the time constant (τ) from Table 5, the recent measurement history, and how much the measured value exceeds the over-current limit. When the current steps from a current (I_1) that is less than the limit to a higher current (I_2) that is greater than the limit, the output of the smoothing filter is:

$$I_{smoothed}(t) = I_1 + (I_2 - I_1)\left(1 - e^{-t/\tau}\right) \quad (11)$$

At the point when $I_{smoothed}$ exceeds the limit, the smoothing filter lags time, t_{lag} is:

$$t_{lag} = \tau \ln\left(\frac{I_2 - I_1}{I_2 - I_{limit}}\right) \quad (12)$$

The worst case response time to an over-current condition is the sum of the sampling interval (see Table 5) and the smoothing filter lag, t_{lag} from the equation above.

Current Foldback Mode

When the measured output current exceeds the value specified by the IOUT_OC_FAULT_LIMIT command, the UCD9224 attempts to continue to operate by reducing the output voltage in order to maintain the output current at the value set by IOUT_OC_FAULT_LIMIT. This continues indefinitely as long as the output voltage remains above the minimum value specified by IOUT_OC_LV_FAULT_LIMIT. If the output voltage is pulled down to less than that value, the device responds as programmed by the IOUT_OC_LV_FAULT_RESPONSE command.

Input Voltage and Current Monitoring

The V_{in}/I_{in} pin on the UCD9224 monitors the input voltage and current. To measure both input voltage and input current, an external multiplexer is required, see Figure 4. If measurement of only the input voltage, and not input current, is desired, then a multiplexer is not needed. The multiplexer is switched between voltage and current using the TMUX-0 signal. (This signal is the LSB of the temperature mux select signals, so the TMUX-0 signal is connected both to the temperature multiplexer as well as the voltage/current multiplexer). When TMUX-0 is low the V_{in}/I_{in} pin will be sampled for V_{in}. When TMUX-0 is high the V_{in}/I_{in} pin will be sampled for I_{in}. The V_{in}/I_{in} pin is monitored using the internal 12-bit ADC and so has a dynamic range of 0 to V_{ADC_RANGE}. The fault thresholds for the input voltage are set using the VIN_OV_FAULT_LIMIT and VIN_UV_FAULT_LIMIT commands. The scaling for V_{in} is set using the VIN_SCALE_MONITOR command, and the scaling for I_{in} is set using the IIN_SCALE_MONITOR command.

Input Under-Voltage Lockout

The input supply lock-out voltage thresholds are configured with the VIN_ON and VIN_OFF commands. When input supply voltage drops below the value set by VIN_OFF, the device starts a normal soft stop ramp. When the input supply voltage drops below the voltage set by VIN_UV_FAULT_LIMIT, the device performs per the configuration using the VIN_UV_FAULT_RESPONSE command. For example, when the bias supply for the controller is derived from another source, the response code can be set to "Continue" or "Continue with delay," and the controller attempts to finish the soft stop ramp. If the bias voltages for the controller and gate driver are uncertain below some voltage, the user can set the UV fault limit to that voltage and specify the response code to be "shut down immediately" disabling all DPWM and SRE outputs. VIN_OFF sets the voltage at which the output voltage soft-stop ramp is initiated, and VIN_UV_FAULT_LIMIT sets the voltage where power conversion is stopped.

Temperature Monitoring

Both the internal device temperature and up to four external temperatures are monitored by the UCD9224. The controller supports multiple PMBus commands related to temperature, including READ_TEMPERATURE_1, which reads the internal temperature, READ_TEMPERATURE_2, which reads the external power stage temperatures, OT_FAULT_LIMIT, which sets the over temperature fault limit, and OT_FAULT_RESPONSE, which defines the action to take when the configured limit is exceeded.

If more than one external temperature is to be measured, the UCD9224 provides analog multiplexer select pins (TMUX0-1) to allow up to 4 external temperatures to be measured. The output of the multiplexer is routed to the Temperature pin. The controller cycles through each of the power stage temperature measurement signals. The signal from the external temperature sensor is expected to be a linear voltage proportional to temperature. The PMBus commands TEMPERATURE_CAL_GAIN and TEMPERATURE_CAL_OFFSET are used to scale the measured temperature-dependent voltage to °C.

The inputs to the multiplexer are mapped in the order that the outputs are assigned using the PHASE_INFO PMBus command. For example, if only one power stage is wired to each DPWM, the two temperature signals should be wired to the first two multiplexer inputs.

The UCD9224 monitors temperature using the 12-bit monitor ADC, sampling each temperature in turn with an 100 ms sample period. These measurements are smoothed by a digital filter, similar to that used to smooth the output current measurements. The filter has a time constant 15.5 times the sample interval, or 1.55 s (15.5 × 100 ms = 1.55 seconds). This filtering reduces the probability of false fault detections.

Figure 5 is an example of a system with one output voltage rail driven by 4 power stages. The output voltage rail is driven with DPWM-1A, DPWM-1B, DPWM-2A and DPWM-3A. The order in which the temperature multiplexer inputs are assigned is shown in Table 6.

Table 6. Temperature Sensor Mapping

TEMPERATURE MUX INPUT	POWER STAGE
1Y0	DPWM-1A
1Y1	DPWM-1B
1Y2	DPWM-2A
1Y3	DPWM-3A

Temperature Balancing

Temperature balancing between phases is performed by adjusting the current such that cooler phases draw a larger share of the current. Temperature balancing occurs slowly (the loop runs at a 10 Hz rate), and only when the phase currents exceeds the PMBus settable TEMP_BALANCE_IMIN. This minimum current threshold prevents the controller from "winding up" and forcing one phase to carry all the current under a low-load condition, when the total current may be insufficient to significantly affect phase temperatures.

Soft Start, Soft Stop Ramp Sequence

The UCD9224 performs soft start and soft stop ramps under closed loop control.

Performing a start or stop ramp or tracking is considered a separate operational mode. The other operational modes are normal regulation and light load regulation. Each operational mode can be configured to have an independent loop gain and compensation. Each set of loop gain coefficients is called a "bank" and is configured using the CLA_GAINS PMBus command.

The soft-start ramp is performed by waiting for the configured start delay TON_DELAY and then ramp the internal reference toward the commanded reference voltage at the rate specified by the TON_RISE time and VOUT_COMMAND. The DPWM and SRE outputs are enabled when the internal ramp reference equals the preexisting voltage (pre-bias) on the output and the calculated DPWM pulse width exceeds the pulse width specified by DRIVER_MIN_PULSE. This ensures that a constant ramp rate is maintained, and that the ramp is completed at the same time it would be if there were not a pre-bias condition.

Figure 13 shows the operation of soft-start ramps and soft-stop ramps.

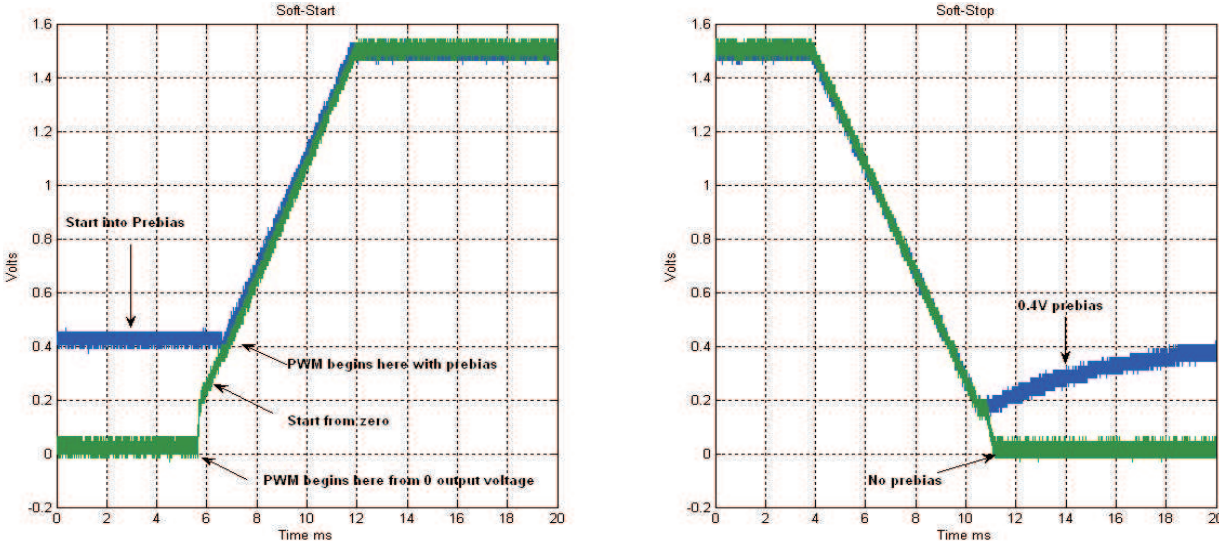

Figure 13. Start and Stop Ramps

When a voltage rail is in its idle state, the DPWM and SRE outputs are disabled, and the differential voltage on the EAP/EAN pins are monitored by the controller. During idle the Vref DAC is adjusted to minimize the error voltage. If there is a pre-bias (that is, a non-zero voltage on the regulated output), then the device can begin the start ramp from that voltage with a minimum of disturbance. This is done by calculating the duty cycle that is required to match the measured voltage on the rail. Nominally this is calculated as Vout / Vin. If the pre-bias voltage on the output requires a smaller pulse width than the driver can deliver, as defined by the DRIVER_MIN_PULSE PMBus command, then the start ramp is delayed until the internal ramp reference voltage has increased to the point where the required duty cycle exceeds the specified minimum duty.

Once a soft start/stop ramp has begun, the output is controlled by adjusting the Vref DAC at a fixed rate and allowing the digital compensator control engine to generate a duty cycle based on the error. The Vref DAC adjustments are made at a rate of 10 kHz and are based on the TON_RISE or TOFF_FALL PMBus configuration parameters.

Although the presence of a pre-bias voltage or a specified minimum DPWM pulse width affects the time when the DPWM and SRE signals become active, the time from when the controller starts processing the turn-on command to the time when it reaches regulation is TON_DELAY plus TON_RISE, regardless of the pre-bias or minimum duty cycle.

During a normal ramp (i.e. no tracking, no current limiting events and no EADC saturation), the set point slews at a pre-calculated rate based on the commanded output voltage and TON_RISE. Under closed loop control, the compensator follows this ramp up to the regulation point.

Because the EADC in the controller has a limited range, it may saturate due to a large transient during a start/stop ramp. If this occurs, the controller overrides the calculated set point ramp value, and adjusts the Vref DAC in the direction to minimize the error. It continues to step the Vref DAC in this direction until the EADC comes out of saturation. Once it is out of saturation, the start ramp continues, but from this new set point voltage; and therefore, has an impact on the ramp time.

Voltage Tracking

Each voltage rail can be configured to operate in a tracking mode. When a voltage rail is configured to track another voltage rail, it adjusts the set point to follow the master, which can be either the other internal rail or the external Vtrack pin. As in standard non-tracking mode, a target Vout is still specified for the voltage rail. If the tracking input exceeds this target, the tracking voltage rail stops following the master signal, switches to regulation gains, and regulates at the target voltage. When the tracking input drops back below the target with 20 mV of hysteresis, tracking gains are re-loaded, and the voltage rail follows the tracking reference. Note that the target can be set above the range of the tracking input, forcing the voltage rail to always remain in tracking mode with the start-stop gains.

During tracking, the Vref DAC is permitted to change only as fast as is possible without inducing the EADC to saturate. This limit may be reached if the master ramps at an extremely fast rate, or if the master is at a significantly different voltage when the rail is turned on. A current limit (current foldback) or the detection of the EADC saturating will force the rail to temporarily deviate from the tracking reference. This behavior is the same in normal regulation mode.

The PMBus command TRACKING_SOURCE is available to enable tracking mode and select the master to track. The tracking mode is set individually for each rail, allowing each rail to have a different master, both rails to share a master, or one rail to track while the other remains independent. Additionally, TRACKING_SCALE_MONITOR permits tracking a voltage with a fixed ratio to a master voltage. For example, a ratio of 0.5 causes the rail to regulate at one half of the master’s voltage.

Sequencing

There are three methods to sequence voltage rails controlled by the UCD9224 that allow for a variety of system sequencing configurations. Each of these options is configurable in the GUI. These methods include:

1. Use the PMBus to set the soft start/stop parameters for each rail. Multiple start/stop sequences may be triggered simultaneously. Each voltage rail performs its sequencing in an open-loop manner. If any rail fails to complete its sequence, all other rails are unaffected.
2. Daisy-chain the Power Good output signal from one controller to the PMBus_Cntl input on another.
3. Use the GPIO_SEQ_CONFIG command to assign dependencies between rails, or to configure unused pins as sequencing control inputs or sequencing status outputs.

Method 1: Each rail has programmable delay times, TON_DELAY and TOFF_DELAY, before beginning a soft start ramp or a soft stop ramp, and programmable ramp times, TON_RISE and TOFF_FALL determine how long the ramp takes. These PMBus commands are defined in the UCD92xx PMBUS Command Reference (SLUU337). The parameters can also be configured using the Fusion Digital Power™ Designer GUI (see http://focus.ti.com/docs/toolsw/folders/print/fusion_digital_power_designer.html). The configurable times can be used to program a time based sequence for each voltage rail. Using this method each rail ramps independently and completes the ramp regardless of the success of the other rails.

The start/stop sequence is initiated for a single rail by the PMBus_Cntl pin or via the PMBus using the OPERATION or ON_OFF_CONTROL commands.

The start/stop sequence may be initiated simultaneously for multiple rails within the same controller by configuring each rail to respond to the PMBus_Cntl pin. Alternatively, after setting the PMBus PAGE variable to 255, subsequent OPERATION or ON_OFF_CONTROL commands applies to all rails at the same time.

To simultaneously initiate start/stop sequences in multiple controllers, a common PMBus_Cntl signal can be fed into each controller. Alternatively, the PMBus Group Command Protocol may be used to send separate commands to multiple controllers. All the commands are sent in one continuous transmission and wait for the final STOP signal in order to start executing their commands simultaneously.

Method 2: The PGood pin can be used to coordinate multiple controllers by running the PGood pin output from one controller to the PMBus_Cntl input pin of another. This imposes a master/slave relationship between multiple devices. During startup, the slave controllers initiate their start sequences after the master completes its start sequence and reaches its regulation voltage. During shut-down, as soon as the master starts its shut-down sequence, the shut-down signals to its slaves.

Unlike Method 1, a shut-down on one or more rails on the master can initiate shut-downs of the slave devices. The master shut-downs can initiate intentionally or by a fault condition.

The PMBus specification implies that the PGood signal is active when ALL the rails in a controller are above their power-good “on” threshold setting. The UCD9224 allows the PGood pin to be reprogrammed using the GPIO_SEQ_CONFIG command so that the pin responds to a desired subset of rails.

This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

Method 3: Using the GPIO_SEQ_CONFIG command, several sequencing options can be configured using undedicated pins for input/output. As many as four pins can be configured as inputs, and as many as six as outputs. The outputs can be open-drain or actively driven with selectable polarity.

Each rail can be configured to respond to a combination of the power-good status of other internal rails and/or the state of sequencing input pins. The output pins can be configured to reflect the power-good status of a combination of rails, or to one of several status indicators including power-good, an over-current warning, or the “open-drain outputs valid” signal.

When using the output signals for sequencing, they may be routed to sequencing control inputs or to the PMBus_Cntl inputs on other controllers.

Once each rail’s turn-on and stay-on dependencies are configured, the rail responds to those input pins or internal rails. Like method 2, shut-downs on one rail or controller can initiate shut-downs of other rails or controllers. Unlike method 2, GPIO_SEQ_CONFIG offers much more flexibility in assigning relationships between multiple rails within a single controller or between multiple controllers. It is possible for each controller to be both a master and a slave to another controller.

GPIO_SEQ_CONFIG allows the configuration of fault relationships such that a fault on one rail can result in the shut down of any selection of rails in addition to the rail at fault. These fault interactions are not constrained to a single master/slave relationship; for example, a system can be configured such that a fault on any rail shuts down all rails. If the fault response of the failing rail is to shut down immediately, all dependent rails follow suit and shuts down immediately regardless of their programmed response code. The fault slaves can be configured to shut-down when the master first reports the fault or after the master has exhausted its retries.

Each rail can be optionally configured to monitor a sequencing input pin for a specified period of time after it turns on and reaches its power good threshold. If the programmable timeout is reached before the input pin state matches its defined logic level, the rail is shut down, and a status error posted. This feature could be used, for example, to ensure that an LDO on the board did turn on when the main system voltage came up. Each rail is enabled independently of the other rails and has a unique timeout value; a single input pin is used as the timeout source.

The setup of the GPIO_SEQ_CONFIG command is aided by the use of the Fusion Digital Power™ Designer, which graphically displays relationships between rails and provides intuitive controls to allocate and configure available resources.

The following pins are available for use as sequencing control, provided they are not being used for their primary purpose:

PIN NAME	48-PIN
DPWM-1A	IN/OUT
DPWM-1B	IN/OUT
DPWM-2A	IN/OUT
DPWM-3A	IN/OUT
FAULT-1A	IN/OUT
FAULT-1B	IN/OUT
FAULT-2A	IN/OUT
FAULT-3A	IN/OUT
SRE-1A	IN/OUT
SRE-1B	IN/OUT
SRE-2A	IN/OUT
SRE-3A	IN/OUT
PGOOD	IN/OUT
SEQ-1	IN/OUT
SEQ-2	IN/OUT

Non-volatile Memory Error Correction Coding

The UCD9224 uses Error Correcting Code (ECC) to improve data integrity and provide high reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single bit error to be detected and corrected when the Data Flash is read.

ADCRef Pin

The ADCRef pin is the decoupling pin for the ADC12. Connect this pin to ground through a 0.1µF to 1µF capacitor.

Sequencing I/O Pins

The UCD9224 has two dedicated sequencing I/O pins that can be used for sequencing. For more information about sequencing see the ‘Sequencing’ section above and the GPIO_SEQ_CONFIG command in the UCD92xx PMBus Command Reference (SLUU337).

APPLICATION INFORMATION

Automatic System Identification (Auto-ID™)

By using digital circuits to create the control function for a switch-mode power supply, additional features can be implemented. One of those features is the measurement of the open loop gain and stability margin of the power supply without the use of external test equipment. This capability is called automatic system identification or

Auto-ID™. To identify the frequency response, the UCD9224 internally synthesizes a sine wave signal and injects it into the loop at the Vref DAC. This signal excites the system, and the closed-loop response to that excitation can be measured at another point in the loop. The UCD9224 measures the response to the excitation at the output of the digital compensator. From the closed-loop response, the open-loop transfer function is calculated. The open-loop transfer function may be calculated from the closed-loop response.

Note that since the compensator and DPWM are digital, their transfer functions are known exactly and can be divided out of the measured open-loop gain. In this way the UCD9224 can accurately measure the power stage/load plant transfer function in situ (in place), on the factory floor or in an end equipment application and send the measurement data back to a host through the PMBus interface without the need for external test equipment. Details of the Auto-ID™ PMBus measurement commands can be found in the UCD92xx PMBus Command Reference (SLUU337).

Data Logging

The UCD9224 maintains a data log in non-volatile memory. This log tracks the peak internal and external temperature sensor measurements, peak current measurements and fault history. The PMBus commands and data format for the Data Logging can be found in the *UCD92xx PMBus Command Reference* (SLUU337).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UCD9224RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD9224
UCD9224RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	NIPDAU | NIPDAU	Level-3-260C-168 HR	-40 to 125	UCD9224

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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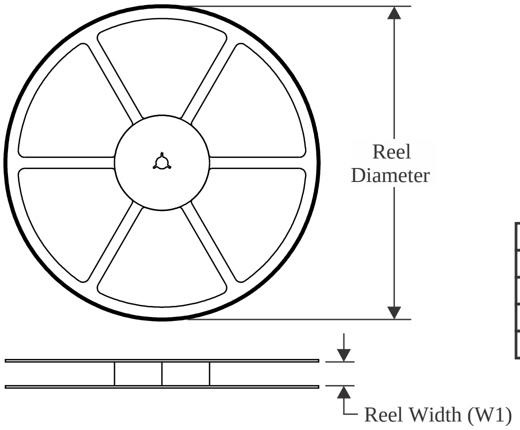
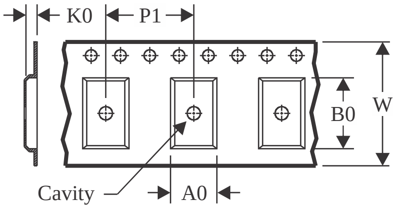
TAPE AND REEL INFORMATION

REEL DIMENSIONS

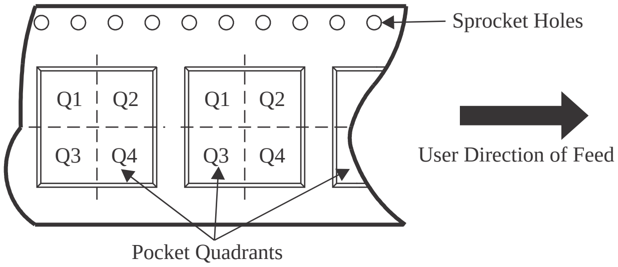


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

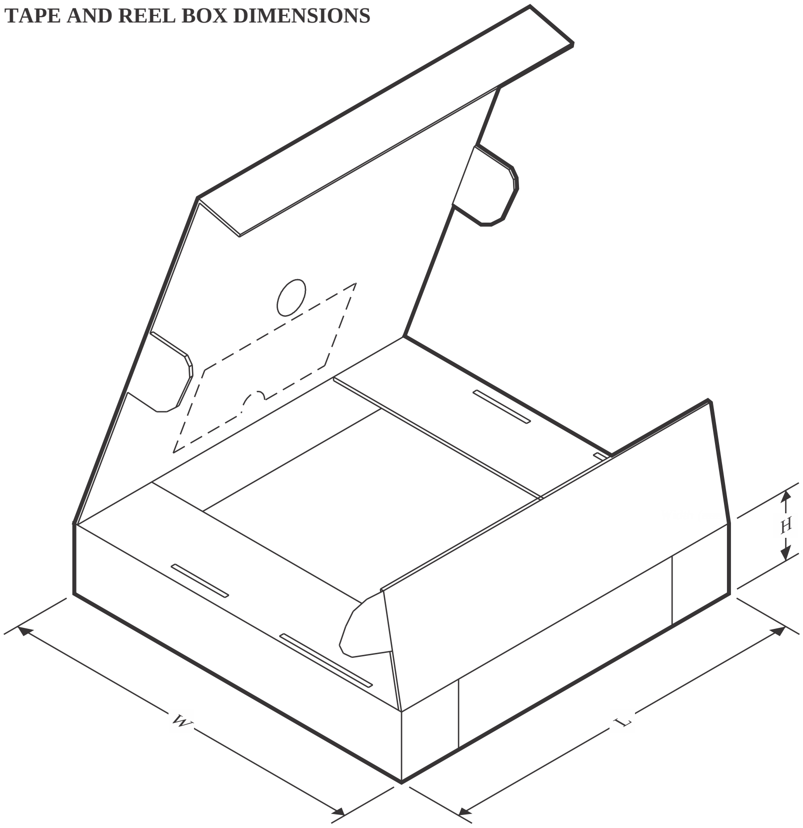
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD9224RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
UCD9224RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD9224RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
UCD9224RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

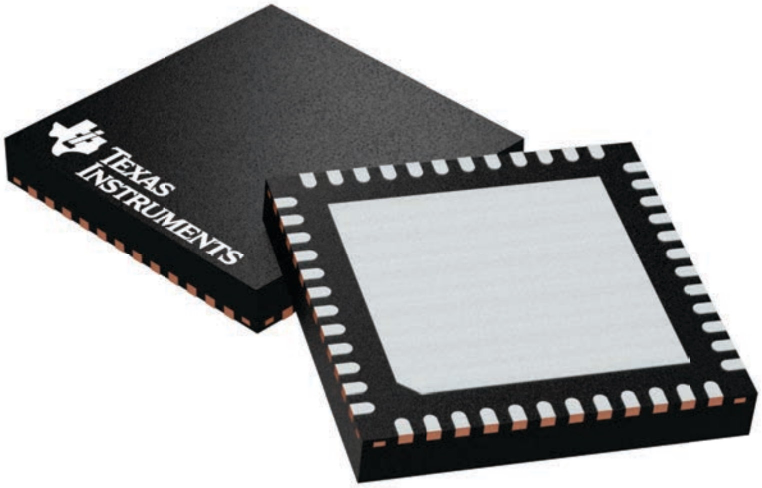
GENERIC PACKAGE VIEW

RGZ 48

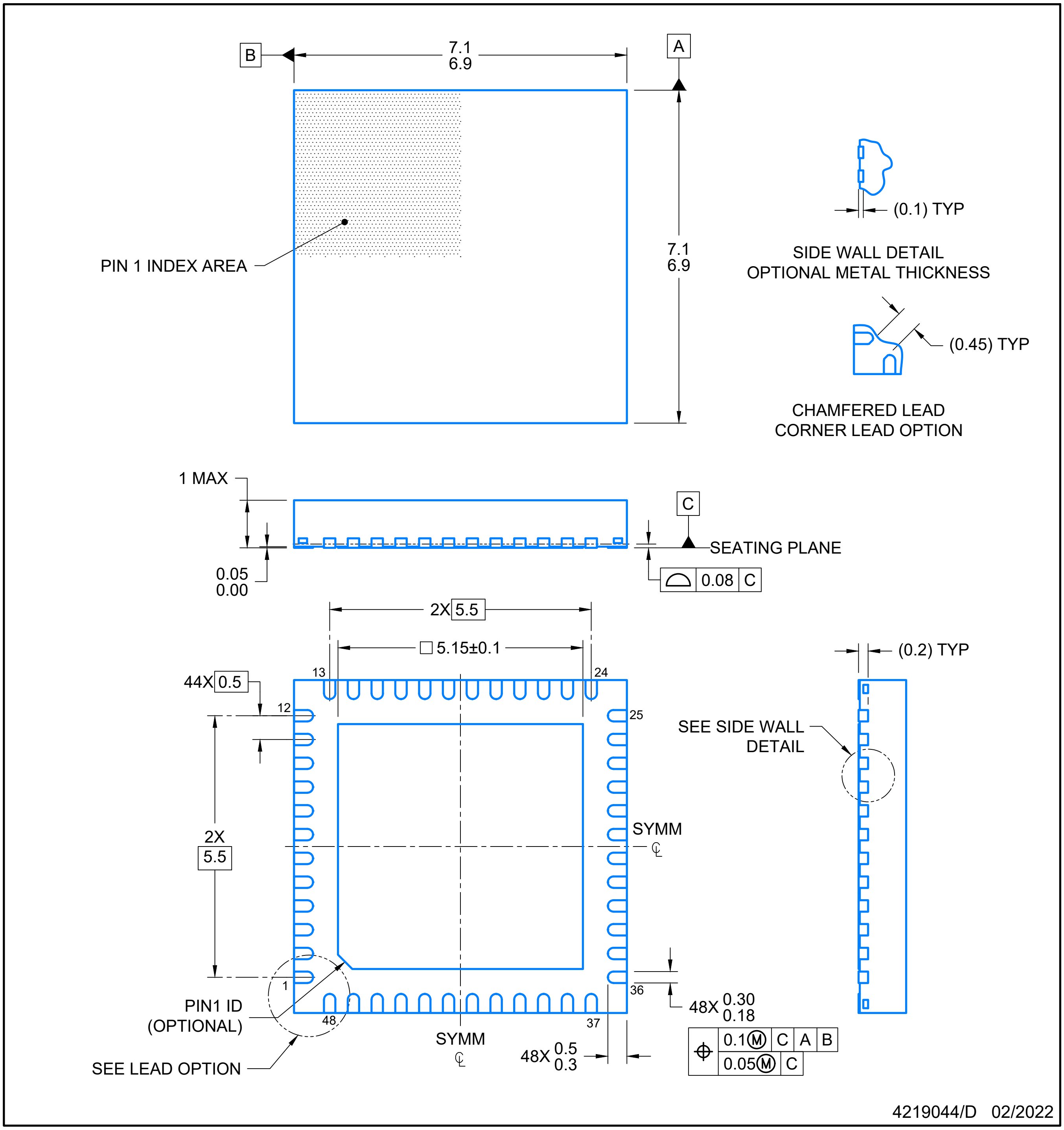
VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

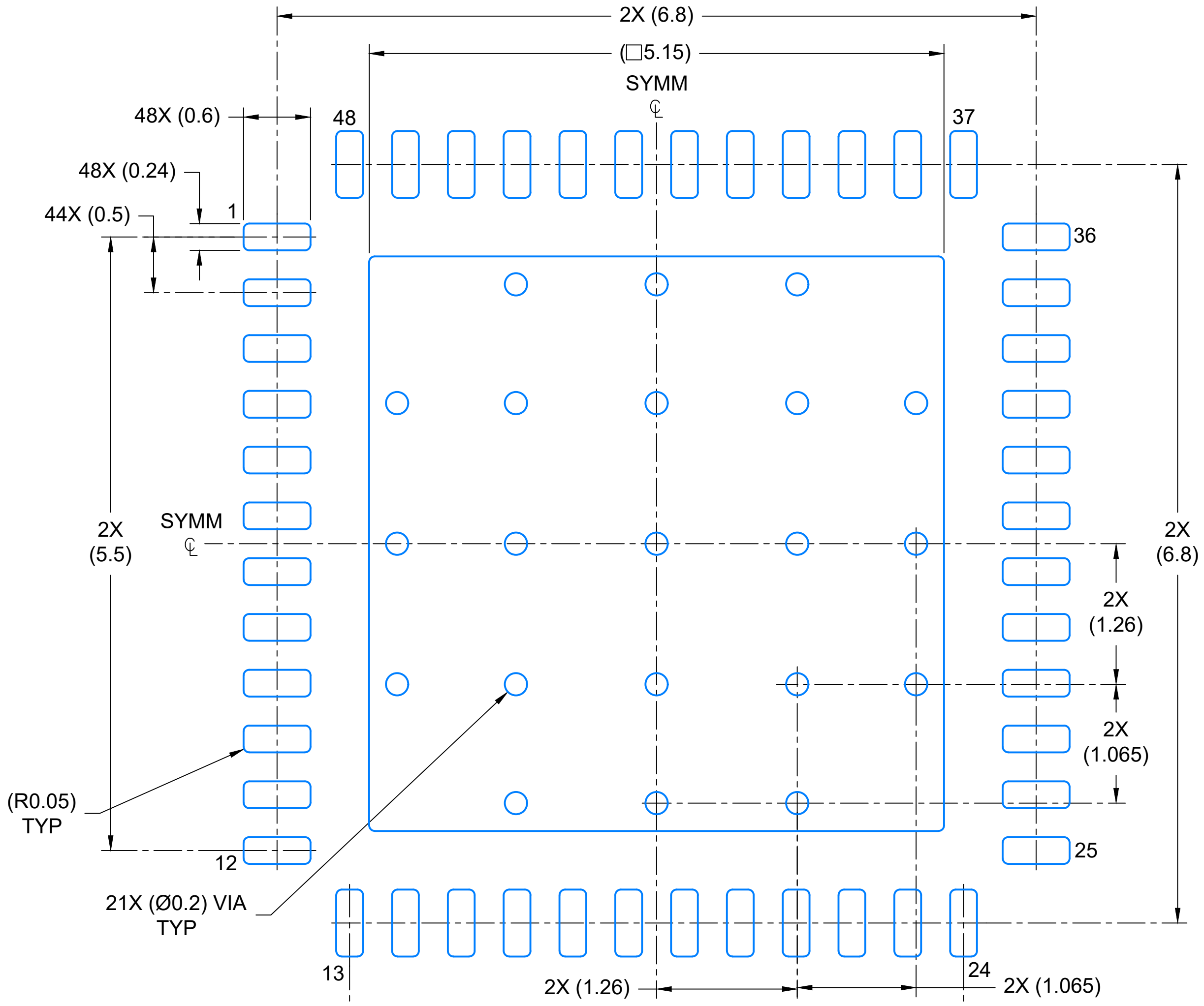


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

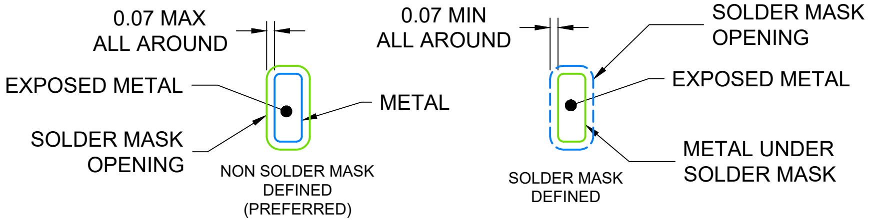


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

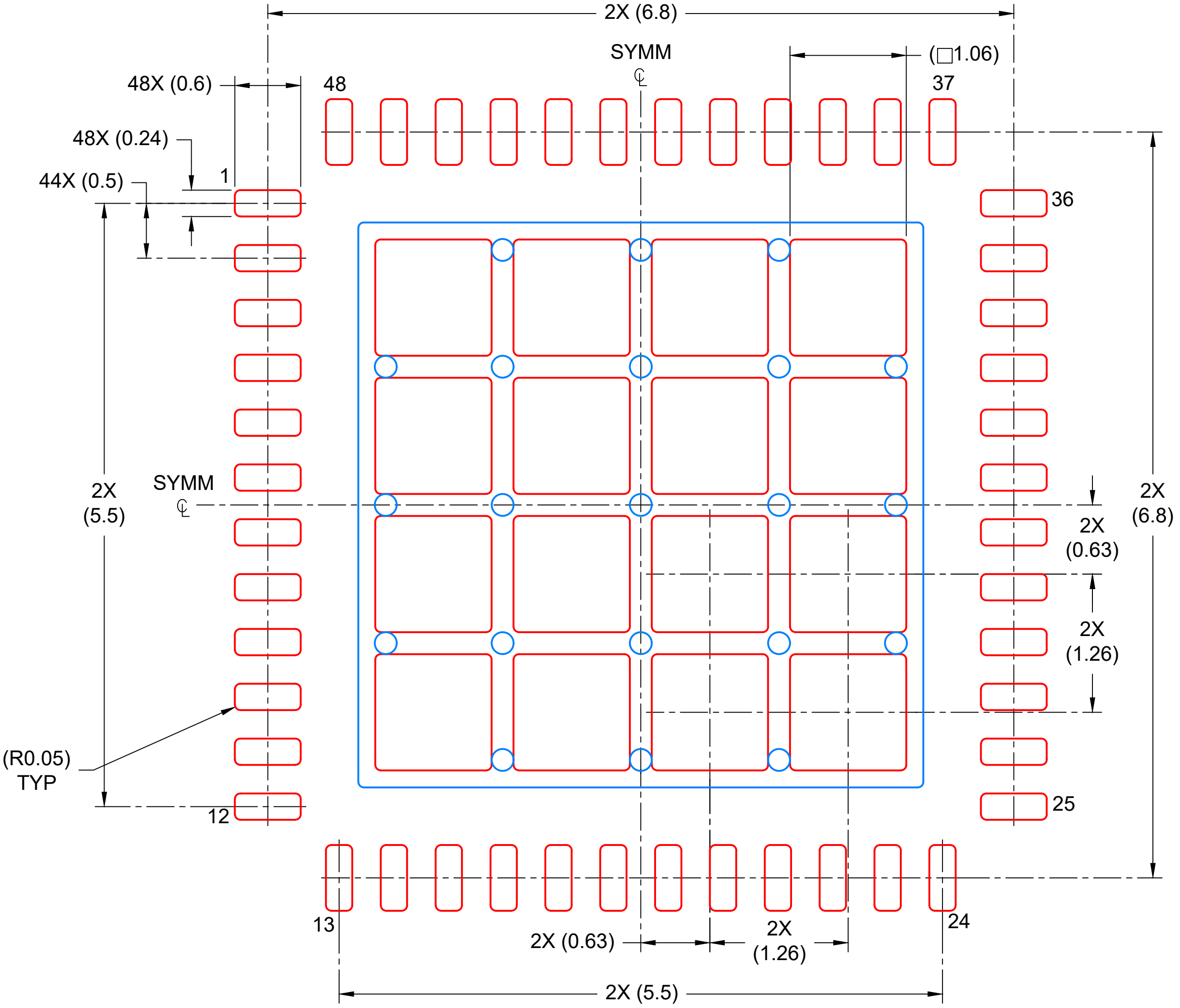


SOLDER MASK DETAILS

4219044/D 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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