# PCI2050B Errata

## 1 Errata #1

### 1.1 Brief Description of Issue

Trst – CLK timing is out of specification.

### 1.2 Detailed Description of Issue

When PCI2050B is in 66-MHz primary, 33-MHz secondary mode, the dividing DFF is in reset when primary reset is asserted, so SCLK outputs will stay low when primary reset is asserted and the 66/33 mode is selected. When primary reset is de-asserted, the design will always have 22 secondary PCI clock cycles from the removal of primary bus reset (and the secondary bus clock starting) to the removal of secondary bus reset. So to calculate that time, it is 22 $\times$ (1/33) = 667 ns. However, according to the PCI specification, S_CLK should become active 100 µs before S_RST is de-asserted. So PCI2050B is out of PCI specification. The problem does not exist when PCI2050B is in 66-MHz primary, 66-MHz secondary mode or 33-MHz primary, 33-MHz secondary mode.

### 1.3 Impact to Customer and Probability of Bug Occurring in Actual Applications

None.

### 1.4 SW or HW Workarounds Defined

After the de-assertion of the primary reset, write a ‘1’ to bit 6 of the Bridge Control Register to initiate a secondary bus reset. Then after 100 µs, write a ‘0’ to bit 6 of the Bridge Control Register to de-assert the secondary bus reset.

Add a circuit to the S_RST# to delay the de-assertion of secondary bus reset by 100 µs.

### 1.5 Affected Devices

PCI2050A, PCI2050B

## 2 Errata #2

### 2.1 Brief Description of Issue

Upstream MWI transactions may result in an address parity error after a disconnect.

## 2.2 Detailed Description

There is a certain set of conditions that may result in an address parity error and corresponding SERR# when a MWI transaction passes through the bridge to an upstream device.

This issue occurs when multiple downstream devices are sending traffic through the bridge. One of the devices begins an upstream MWI transaction which begins passing through the bridge correctly, but after some period of time the upstream target issues a disconnect to the PCI2050B on a non cache-line aligned boundary. When the PCI2050B data buffer is full, it is unable to continue receiving data from the downstream device and issues a disconnect to the downstream device.

After the initiator of the MWI transaction is disconnected, if a new device is now granted ownership of the secondary PCI bus then when the PCI2050B retries its transaction on the upstream bus again, it converts the MWI transaction (C/BE# = 1111) to a Memory Write transaction (C/BE# = 0111). Since the Command has changed by 1 bit, the parity bit should be inverted, however the parity is not inverted by the PCI2050B causing an address parity error on the primary bus and consequently a SERR# occurs.

## 2.3 Impact to Customer and Probability of Bug Occurring in Actual Application

SERR# assertion may result in system crash.

## 2.4 SW or HW Workarounds Defined

Setting the cache line size register (offset 0xC in PCI Configuration Space) to a value greater than 16 (0x10) will result in the PCI2050B to convert all MWI transactions to MW. In this situation the address parity error does not occur. A value of 0x20 for the cache line size is recommended to maintain reasonable throughput.

Furthermore as long as there is no backpressure on to the PCI2050B causing a disconnect the transaction will complete without the retry resulting the command conversion.

Alternatively if the downstream devices do not use the MWI command or have the use of the command disabled so that no MWI commands are initiated on the secondary bus, then MW transactions on the secondary bus will always be forwarded as MW commands on the primary bus also preventing this issue from occurring.

## 2.5 Affected Devices

PCI2050B

## Errata History

Errata #1: Issued on September 23, 2005

Errata #2: Issued on March 1, 2009

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