

TUSB8040 Errata

1 PASSIVE RESET CIRCUIT

1.1 Problem

If the 3.3-V supply of the TUSB8040 ramps before the 1.1-V supply, the device I/O is in an unknown state before the core logic is active. This allows the potential for the GRSTz I/O cell to incorrectly configure as an output and drive the GRSTz signal high until the core logic is powered on and correctly configures the cell. The behavior can shorten or eliminate the needed reset pulse if a passive reset circuit is used.

Work Around

Ramp the 1.1-V power supply before or at the same time as the 3.3-V power supply if a passive reset circuit is used. Another option is to use an active reset source such as a power good signal from the 1.1-V voltage regulator or a voltage supervisory circuit. The reset pulse must be at least 3 ms long, but shorter than 100 ms.

2 U1/U2 LOW POWER STATES

2.1 Problem

The TUSB8040 may fail to recognize a device initiated U1 exit. Problem only occurs with SS devices that have short LFPS signals.

Work Around

Disable U1/U2 support via the SDA_SMBAT input.

2.2 Problem

If the TUSB8040 upstream port is in low power state U1, transitions to U0 and sends an ERDY packet from its interrupt endpoint to the USB 3.0 host controller, it may initiate or accept a LGO to the U1 power state before the USB 3.0 host controller sends the expected data or transaction packet or the 500-ms timeout is reached. Problem only occurs in tiered hub configurations.

Work Around

Disable U1/U2 support via the SDA_SMBAT input.

2.3 Problem

The TUSB8040 does not initiate a transition to U2 when all its downstream ports are in low power state U2 or lower when both U1 and U2 low power states are enabled. Issue only seen in compliance testing. The hub will enter U1 power state instead of U2 power state with no system impact.

Work Around

None needed.

2.4 Problem

The TUSB8040 does not clear its U1 and U2 timers after a port reset. Issue only seen in compliance testing. Host drivers will reset timer values after a port reset.

Work Around

Disable U1/U2 support via the SDA_SMBAT input.

2.5 Problem

The TUSB8040 does not defer a packet to a downstream port while it is in recovery transitioning from U1/U2 back to U0. Issue only seen in compliance testing.

Work Around

Disable U1/U2 support via the SDA_SMBAT input.

3 STATUS/CHANGE BITS

3.1 Problem

When a warm reset or hot reset is sent to a downstream port of the TUSB8040, the reset change bits are set in the port change register as soon as the reset completes which may be before the downstream port has finished its transition back to the U0 state.

Work Around

None needed, all tested host drivers accommodate this condition.

3.2 Problem

The TUSB8040 will set the port reset status bit on an unconnected downstream port when the upstream port receives and propagates a reset. The TUSB8040 does not check the disconnect status before propagating the reset. The reset port status bit will be set for up to 100 ms and then cleared.

Work Around

None needed.

3.3 Problem

The TUSB8040 does not clear the port connection and port enable status bits on a downstream port that enters the SS.Inactive state due to an error condition.

Work Around

None needed, the host driver must reset the port to get it out of the SS.Inactive state.

4 SPECIFICATION COMPLIANCE

4.1 Problem

When the TUSB8040 is in U3 and a device is connected on a downstream port while remote wakeup for a connect event is masked by the host driver, the TUSB8040 does not force the downstream device to U3. Issue only seen in compliance testing.

Work Around

None.

4.2 Problem

The TUSB8040 will accept and discard port commands for non-existent ports instead of failing the port commands. Issue only seen in compliance testing.

Work Around

None.

4.3 Problem

Hub incorrectly issues STALL for a control transfer in some cases: if the SETUP DP for a control transfer to the HUB and the ITP from the host come back to back without any IDLE cycles on the bus, then the hub issues a STALL in the status phase of the control transfer. This occurs only when the ITP comes immediately after the SETUP DP and before the ACK TP from the HUB.

Work Around

None.

4.4 Problem

Hub fails to respond after Abnormal STALLED control transfer from host.

Work Around

None.

5 SMBUS INTERFACE

5.1 Problem

Setting the smbusRst in the Device Status and Command Register at F8H resets the SMBUS interface but does not return the registers to their default values. This reset is only used when the TUSB8040 is in SMBUS mode.

Work Around

Do not use reset to set the registers to their default values.

5.2 Problem

The TUSB8040 SMBUS interface doesn't support the optional 35-ms clock low timeout. The 35-ms parameter allows a master or slave SMBUS device to conclude that a defective device is holding the clock low indefinitely or a master is intentionally trying to drive devices off the bus. This is an optional function of the SMBUS specification.

Work Around

None.

6 INTEROPERABILITY

6.1 *Problem*

Some brands of USB 2.0 Full Speed Cameras may exhibit packet drops when used in high ambient light settings. The issue occurs because of a longer than expected delay between receiving the last CRC byte of the data packet from the camera and updating the CRC16 of the packet sent to the host.

Work Around

None. Problem does not occur with USB 2.0 High Speed Cameras.

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