# TMS320LC2406A, TMS320LC2404A, TMS320LC2402A

# DSP Controllers

# Silicon Errata

*SPRZ185C*
May 2001
Revised June 2004

TEXAS INSTRUMENTS

# Contents

# 1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320LC2406A, TMS320LC2404A, and the TMS320LC2402A DSP Controllers, silicon revision 1.0 and 2.0. The updates are applicable to:

- TMS320LC2406A (100-pin LQFP, PZ suffix)
- TMS320LC2404A (100-pin LQFP, PZ suffix)
- TMS320LC2402A (64-pin QFP, PG suffix)

## 1.1 Quality and Reliability Conditions

### TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature range and voltage range should not, in any way, be construed as a warranty of performance.

### TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

### TMS Definition

Fully-qualified production device.

## 1.2 Revision Identification for TMS320LC2404A/2406A

The device revision can be determined by the lot trace code marked on the top of the package. The location of the lot trace code is shown in Figure 1.

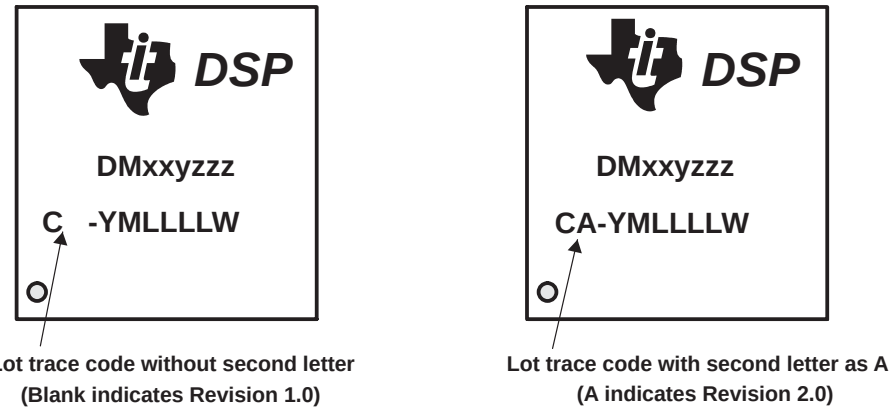


**Figure 1. Example of Lot Trace Code for TMS320LC2404A/2406A**

| Second Letter in Prefix of Lot Trace Code | Silicon Revision | Comments |
|---|---|---|
| **Blank** (no first letter in prefix) | Indicates Revision 1.0 | This silicon revision is available as TMS. |
| **A** (first letter in prefix is a “C” and the second is an “A”) | Indicates Revision 2.0 | This silicon revision is available as TMS. |

## 1.3 Revision Identification for TMS320LC2402A

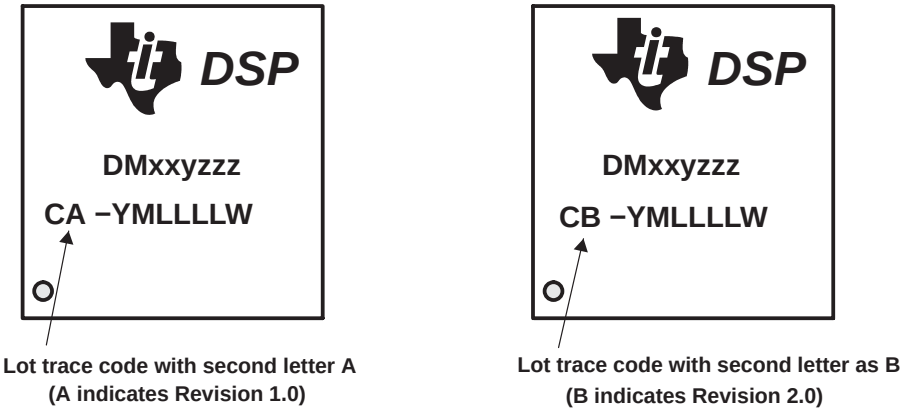


**Figure 2. Example of Lot Trace Code for TMS320LC2404A/2402A**

| Second Letter in Prefix of Lot Trace Code | Silicon Revision | Comments |
|---|---|---|
| **A** (Second letter in prefix) | Indicates Revision 1.0 | This silicon revision is available as TMS. |
| **B** (First letter in prefix is a “C” and the second is an “B”) | Indicates Revision 2.0 | This silicon revision is available as TMS. |

# 2 Known Design Marginality/Exceptions to Functional Specifications

**Table 1. Summary of Exceptions**

| Description | Revision(s) Affected | Page |
|---|---|---|
| LPM1 Mode With an External Crystal/Resonator | 1.0, 2.0 | 5 |
| Internal Oscillator | 1.0, 2.0 | 5 |
| ADC — ADC Sequencer Operation | 1.0, 2.0 | 6 |
| CAN — CAN Bit Timing | 1.0, 2.0 | 6 |
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| $\overline{\text{PDPINTx}}$ Pin Operation | 1.0, 2.0 | 7 |
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| $\overline{\text{SPISTE}}$ Timing Anomaly | 1.0, 2.0 | 8 |
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| Peripheral Clocks Not Turned Off in LPM1 | 1.0 | 9 |
| ADC — ADC Module Clock Not Turned Off | 1.0 | 9 |

## 2.1 Advisories for Revisions 1.0 and 2.0

**Advisory** — *LPM1 Mode With an External Crystal/Resonator*

**Revision(s) Affected**: 1.0, 2.0

**Details**: The device does not come out of LPM1 mode when the internal oscillator (in conjunction with an external crystal/resonator) is used. This is not an issue if an external oscillator is used.

**Workaround**: Do not use LPM1 if using the internal oscillator.

**Advisory** — *Internal Oscillator*

**Revision(s) Affected**: 1.0, 2.0

**Details**: The internal oscillator of the 240xA device has a design marginality that may prevent the internal oscillator from starting upon power-up under certain conditions pertaining to board layout, ground bounce, and power-supply ramp rate. This is a concern only when the internal oscillator is used in conjunction with an external quartz crystal/ceramic resonator and not with an external oscillator.

**Workaround**: Use of a 1M-Ω resistor in parallel with the crystal across the XTAL1 and XTAL2 pins removes this condition.

| Advisory | *ADC — ADC Sequencer Operation* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: The ADC sequencer operation has an issue when CPS = 1 *and* ACQ_Prescaler = 0. When an ADC sequence is started, the sequence stops after performing the first conversion. For example, if there are five conversions programmed for a sequence, the sequencer may stop after performing the first conversion. When CPS = 0, all the conversions are performed. The issue surfaces only when CPS = 1 **and** ACQ_Prescaler = 0. CPS can be 1 for any other ACQ_Prescaler value.

**Workaround**: ACQ_Prescaler = 0 should not be used in conjunction with CPS = 1.

| Advisory | *CAN — CAN Bit Timing* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: When the SBG bit (bit 10 of the BCR1 register) is set to 1, the “high” bit may be one TQ shorter/longer than it should be.

**Workaround**: Set SBG = 0.

| Advisory | *CAN — Method to Service Multiple Interrupts Through the Existing Two-Interrupt Structure* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: A CAN module interrupt will not assert a core-level interrupt if a CAN_IFR bit (set by any previous CAN interrupt) still remains set at the time of occurence of the new interrupt. For example, when a new CAN interrupt is asserted before the processor has had a chance to clear the CAN_IFR bit that caused the interrupt to happen, the CAN module does not assert a core-level CPU interrupt (INTn) for the new interrupt and may “lose” interrupts. However, the occurence of any interrupt-causing event will always set the appropriate flag bit in the CAN_IFR register.

**Workaround**: The CAN_IFR bit that causes an interrupt must be cleared as early as possible within the ISR. This can be done by copying the CAN_IFR register to a memory variable and then clearing the set bit. The memory variable can then be examined to determine which interrupt was asserted. If all CAN_IFR bits are cleared (i.e., zero) when a “new” interrupt is asserted, the “new” interrupt will be recognized and serviced by the core.

| Advisory | *EV−CAPn Input* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: If a CAPn input is high while the capture units are being enabled, it triggers spurious captures. The CAPFIFO status bits would indicate that there are two words in the FIFO when, in reality, no capture was triggered. If the capture interrupt is enabled, it will trigger the capture interrupt as well.

**Workaround**: Initialize the CAPFIFO status bits (and enable the capture interrupt) after configuring the capture units.

| Advisory | *$\overline{\text{PDPINTx}}$ Pin Operation* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: If the $\overline{\text{PDPINTx}}$ pin is active during a device reset, it prevents the recognition of valid PDPINTx interrupts in the future.

**Workaround**: To overcome this problem, bit PIRQR0.0 (for $\overline{\text{PDPINTA}}$) and bit PIRQR2.0 (for $\overline{\text{PDPINTB}}$) need to be cleared to zero. This can be achieved by writing a zero to these bits or by writing a one to the corresponding PIACKRn.0 bits. In addition to this, the EVAIFRA.0 bit (or EVBIFRA.0 bit) should be cleared as appropriate.

The PIRQRn and PIACKRn registers are ***not*** intended to be used in user applications. The workaround mentioned herein is a special case during the initialization of the device. After initialization, these registers should not be used by the user code.

| Advisory | *QEP Circuit* |
|---|---|

**Revision(s) Affected**: 1.0, 2.0

**Details**: After a DSP reset, the QEP module fails to detect the first transition that occurs on QEP input pins. Therefore, if the first transition occurs after a GP Timer has been initialized and enabled as the QEP counter (i.e., to use QEP as source of clock), the first transition will not be counted by the GP Timer. The result is an error of one count in the GP Timer out of a total of 1024 counts for a 256-line encoder, or 4096 counts for a 1024-line encoder. However, the issue is not a concern under any of the following conditions:

1. *The first transition happens **before** the GP Timer is initialized and enabled as QEP counter.* This ensures that all transitions are counted after initialization.
2. *After the first index pulse is received and if the index pulse is used to recalibrate the GP Timer (through capture interrupt).* The recalibration corrects the error in the GP Timer; therefore, from the time the first index pulse is received, the QEP counter becomes accurate.

*QEP Circuit (Continued)*

**Workaround(s)**:

1. Make the first transition happen before the GP timer is initialized and enabled as QEP counter. This is usually the case because typically the rotor shaft is locked to a known position before the GP Timer is initialized. Locking the rotor shaft will generate transitions on QEP input pins, unless the rotor shaft is exactly aligned to the known position (which is a rare case). Disturbing the rotor shaft on purpose takes care of the rare case.
2. Use the index pulse of the encoder to recalibrate the GP Timer used as QEP counter.

## Advisory — *$\overline{\text{SPISTE}}$ Timing Anomaly*

**Revision(s) Affected**: 1.0, 2.0

**Details**:

The $\overline{\text{SPISTE}}$ signal has a timing anomaly because of which it goes high sooner than it should (i.e., before the last bit has ended). This results in unreliable read of the last bit of the word by both the master and the slave. Following is a summary of the bug description depending on which SPI clocking scheme is used:

- CLOCK POLARITY = 0, PHASE = 0
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the falling edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 0, PHASE = 1
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the rising edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 1, PHASE = 0
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the rising edge of the SPICLK for the last bit of transmission.
- CLOCK POLARITY = 1, PHASE = 1
  The $\overline{\text{SPISTE}}$ signal goes high 3 CPU clock cycles after the falling edge of the SPICLK for the last bit of transmission.

Note that the timing issue is aggravated when PHASE = 1, since the time window for which the $\overline{\text{SPISTE}}$ signal is valid for the last bit gets reduced further.

**Workaround**:

The $\overline{\text{SPISTE}}$ pin should be used in its GPIO configuration. This pin can then be manipulated manually in software. Note that this workaround does not require any hardware change.

## 2.2 Advisories for Revision 1.0

| Advisory | *CSM — Code Security Module* |
|---|---|

**Revision(s) Affected**: 1.0

**Details**: Unsecuring a secured part does not work as documented.

**Workaround**: This has been fixed in the next revision of the silicon.

| Advisory | *Peripheral Clocks Not Turned Off in LPM1* |
|---|---|

**Revision(s) Affected**: 1.0

**Details**: Clocks to peripheral modules are not automatically turned off in LPM1.

**Workaround**: Clocks must be turned off by the code prior to entering LPM1. This has been fixed in the next revision of the silicon.

| Advisory | *ADC — ADC Module Clock Not Turned Off* |
|---|---|

**Revision(s) Affected**: 1.0

**Details**: Clock to the ADC module is not turned off even when bit 7 of the SCSR1 register is cleared.

**Workaround**: This has been fixed in the next revision of the silicon.

## 3 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com**

To access documentation on the web site:

1. Go to **http://www.ti.com**
2. Click on **DSP Product Tree**
3. Click on the **C2000** tab
4. Click on **TMS320C24x DSP Generation**
5. Click on a device name and then click on the documentation type you prefer.

For further information regarding the TMS320LC2406A, TMS320LC2404A, and TMS320LC2402A devices, please refer to the following publications:

- *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (literature number SPRU357)
- Manual Update Sheet for *TMS320LF/LC240xA DSP Controllers Reference Guide: System and Peripherals* (SPRU357B) [literature number SPRZ015]
- *TMS320F/C24x DSP Controllers Reference Guide: CPU and Instruction Set* (literature number SPRU160)
- *3.3V DSP for Digital Motor Control* application report (literature number SPRA550)
- *TMS320LF2407A, TMS320LF2406A, TMS320LF2403A, TMS320LF2402A, TMS320LC2406A, TMS320LC2404A, TMS320LC2402A DSP Controllers* data sheet (literature number SPRS145)

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