Functional Safety Information

ADS127L11

Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for the ADS127L11 (PW and RUK packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

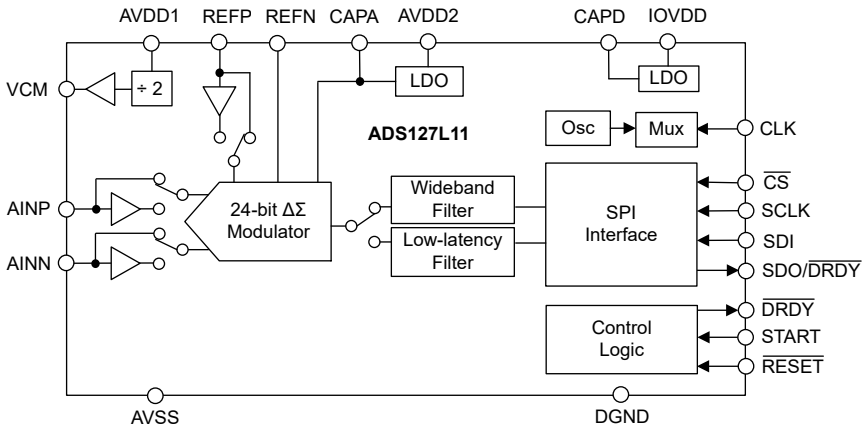

Figure 1-1. Functional Block Diagram

The ADS127L11 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 PW Package

This section provides functional safety failure in time (FIT) rates for the PW package of the ADS127L11 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	13
Die FIT rate	2
Package FIT rate	11

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 18.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS digital, analog, or mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 RUK Package

This section provides functional safety failure in time (FIT) rates for the RUK package of the ADS127L11 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from Table 11
- Power dissipation: 18.5 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	70 FIT	70°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the ADS127L11 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Analog input stuck at	20%
Digital control pins stuck at	20%
Output code bit stuck at	10%
Communication error	10%
10x input leakage current	10%
10% shift of gain or offset	20%
Oscillator frequency exceeds specification	5%
VCM pin voltage exceeds specification	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the ADS127L11 (PW and RUK package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3
- Pin short-circuited to an adjacent pin (see Table 4-4
- Pin short-circuited to supply (see Table 4-5

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- AVDD1 = AVDD2 = IOVDD = 5 V
- AVSS = thermal pad voltage = 0 V
- IOVDD power supply voltage is the same supply voltage used for driving the digital inputs
- *Short Circuit to Supply* means short to AVDD1 = AVDD2 = IOVDD
- *Short Circuit to Ground* means short to DGND = AVSS
- VCM output voltage actively used in external circuit to establish the input common-mode voltage
- Device is the only peripheral device on the SPI bus.
- Series resistors are used on analog inputs and are sized to limit the input currents into the analog inputs to <10 mA in all circumstances, such as in case the device is unpowered with input signal applied.

4.1 PW Package

Figure 4-1 shows the ADS127L11 pin diagram for the PW package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ADS127L11 data sheet.

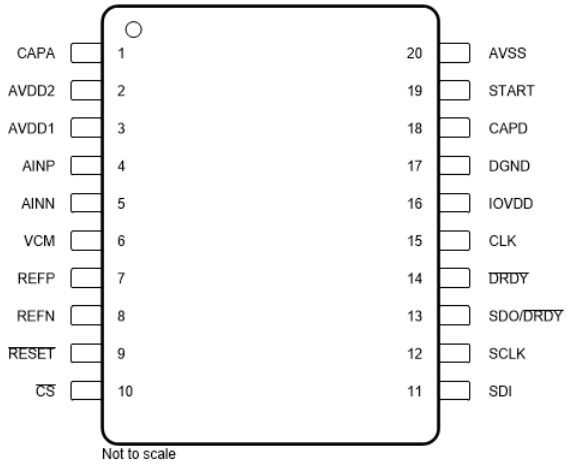

Figure 4-1. PW Package Pin Diagram

Table 4-2. PW Package Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CAPA	1	Device partially unpowered. Device not functional. Device damage plausible if CAPA shorted to ground for extended period of time.	A
AVDD2	2	Device unpowered. Device not functional.	B
AVDD1	3	Device unpowered. Device not functional. Observe that the absolute maximum ratings for analog input and reference voltage pins of the device are met, otherwise device damage may be plausible.	A
AINP	4	AINP stuck low. Conversion results correct only if AINP tied to DGND in actual use, otherwise conversion results incorrect.	B
AINN	5	AINN stuck low. Conversion results correct only if AINN tied to DGND in actual use, otherwise conversions results incorrect.	B
VCM	6	VCM stuck low. Conversion results incorrect if actively used for external driver stage to set signal common-mode voltage.	B
REFP	7	REFP stuck low. Conversion results incorrect.	B
REFN	8	REFN stuck low. Conversion data correct only if REFN is tied to DGND in actual use, otherwise conversions results incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ stuck low. Device not functional.	B
$\overline{\text{CS}}$	10	$\overline{\text{CS}}$ stuck low in four-wire SPI mode. SPI communication not functional because of inability to control SPI data frames.	B
		$\overline{\text{CS}}$ stuck low in three-wire SPI mode. No effect, conversions results correct.	D
SDI	11	SDI stuck low. Loss of SPI input communications to the device. Conversion data readout remains functional.	B
SCLK	12	SCLK stuck low. SPI communication not possible.	B
SDO/$\overline{\text{DRDY}}$	13	SDO/$\overline{\text{DRDY}}$ stuck low. SPI *output* communication not possible. SPI input communications remains functional. Data-ready function via this pin not functional. Device damage plausible if SDO/$\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ stuck low, pin *is not* monitored by host. Normal operation. Device damage plausible if $\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
		$\overline{\text{DRDY}}$ stuck low, pin *is* monitored by host. No data-ready indication via $\overline{\text{DRDY}}$ to host possible. Device damage plausible if $\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
CLK	15	CLK stuck low in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK stuck low in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	Device unpowered. Device not functional.	B
DGND	17	No effect. Normal operation.	D
CAPD	18	Device partially unpowered. Device not functional. Device damage plausible if CAPD shorted to ground for extended period of time.	A
START	19	START stuck low, pin is in active use by host. Loss of ability to control conversion timing. Conversion results incorrect.	B
		START stuck low, pin tied low in actual use (software control mode). No effect. Normal operation.	D
AVSS	20	No effect. Normal operation.	D

Table 4-3. PW Package Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CAPA	1	CAPA voltage indeterminate. Conversion results indeterminate.	B
AVDD2	2	Device partially unpowered and held in reset. Device not functional.	B
AVDD1	3	Device functionality indeterminate. Device partially unpowered and not functional if analog input or voltage reference pins are held low. Device can be powered through input or voltage reference drivers through internal ESD diode conduction path.	B
AINP	4	State of AINP indeterminate. Conversion results indeterminate.	B
AINN	5	State of AINN indeterminate. Conversion results indeterminate.	B
VCM	6	VCM output voltage indeterminate. Conversion results indeterminate.	B
REFP	7	State of REFP indeterminate. Conversion results indeterminate.	B
REFN	8	State of REFN indeterminate. Conversion results indeterminate.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ stuck high. Loss of ability to reset the ADC via this pin.	B
$\overline{\text{CS}}$	10	State of $\overline{\text{CS}}$ indeterminate. SPI communication corrupted.	B
SDI	11	State of SDI indeterminate. Loss of SPI *input* communications to the device. Conversion data readout remains functional.	B
SCLK	12	State of SCLK indeterminate. SPI communication corrupted.	B
SDO/$\overline{\text{DRDY}}$	13	State of SDO/$\overline{\text{DRDY}}$ indeterminate. SPI *output* communication not possible. SPI input communications remains functional. Loss of data-ready function from this pin.	B
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ unconnected, pin *is not* monitored by host. No effect. Normal operation.	D
		$\overline{\text{DRDY}}$ unconnected, pin *is* monitored by host. No data-ready indication via $\overline{\text{DRDY}}$ to host possible.	B
CLK	15	CLK open-circuit in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK open-circuit in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	Device functionality indeterminate. Device partially unpowered and not functional if START digital input pin is held low. Device can be powered through START digital input pin via internal ESD diode conduction path to IOVDD.	B
DGND	17	Device functionality indeterminate. Device may be unpowered, or powered through digital inputs via ESD diode path.	B
CAPD	18	CAPD voltage indeterminate. Conversion results indeterminate.	B
START	19	State of START indeterminate. Conversion results indeterminate.	B
AVSS	20	Device functionality indeterminate. Device unpowered and not functional if analog input or voltage reference pins are held low. Device can be powered through input or voltage reference drivers through internal ESD diode conduction path.	B

Table 4-4. PW Package Pin FMA for Device Pins Short-Circuited to Adjacent Pins

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CAPA	1	AVDD2	Device damage.	A
AVDD2	2	AVDD1	No effect. Normal operation.	D
AVDD1	3	AINP	Conversion results correct only if AINP tied to AVDD1 in actual use, otherwise conversion results incorrect.	B
AINP	4	AINN	Conversion results incorrect. Conversion result is close to 0 V.	B
AINN	5	VCM	Conversion results incorrect.	B
VCM	6	REFP	Conversion results incorrect.	B
REFP	7	REFN	Conversion results incorrect.	B
REFN	8	$\overline{\text{RESET}}$	Conversion results incorrect. Device held in reset and not functional if driver source impedance of REFN exceeds that of $\overline{\text{RESET}}$, driving $\overline{\text{RESET}}$ to low threshold. Otherwise, conversion results incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{CS}}$	Conversion results incorrect. Device not functional.	B
$\overline{\text{CS}}$	10	SDI	Not considered. Corner pins.	D
SDI	11	SCLK	Loss of SPI *input* communications to the device if driver source impedance of SCLK exceeds that of SDI. Loss of *all* SPI communications to the device if driver source impedance of SDI exceeds that of SCLK.	B
SCLK	12	SDO/$\overline{\text{DRDY}}$	Loss of SPI *output* communications from the device if driver source impedance of SCLK exceeds that of SDO/$\overline{\text{DRDY}}$. Loss of *all* SPI communications to the device if driver source impedance of SDO/$\overline{\text{DRDY}}$ exceeds that of SCLK. Device damage plausible if shorted together for an extended period of time.	A
SDO/$\overline{\text{DRDY}}$	13	$\overline{\text{DRDY}}$	Indeterminate state of both digital outputs. Loss of SPI *output* communications from the device. Device damage plausible if shorted together for an extended period of time.	A
$\overline{\text{DRDY}}$	14	CLK	*External* clock mode. Device not functional if driver source impedance of $\overline{\text{DRDY}}$ exceeds that of CLK. Indeterminate state of $\overline{\text{DRDY}}$ if driver source impedance of CLK exceeds that of $\overline{\text{DRDY}}$. Device damage plausible if shorted together for an extended period of time.	A
			Internal clock mode. CLK pin has external pull-up/down resistor to supply or ground (no active driver used). Normal operation.	D
CLK	15	IOVDD	*External* clock mode. Device not functional. Conversion results incorrect.	B
			Internal clock mode. Normal operation.	D
IOVDD	16	DGND	Device unpowered. Device not functional.	B
DGND	17	CAPD	Device partially unpowered. Device not functional. Device damage plausible if CAPD shorted to ground for extended period of time.	A
CAPD	18	START	Device not functional. Permanent device damage if START driver source impedance exceeds that of CAPD, resulting in CAPD exceeding maximum voltage rating.	A
START	19	AVSS	Conversion results correct only if START tied to DGND = AVSS in actual use. Otherwise, conversion results not correct because of inability to control conversions.	B
AVSS	20	CAPA	Not considered. Corner pins.	D

Table 4-5. PW Package Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CAPA	1	CAPA stuck high. Permanent device damage.	A
AVDD2	2	No effect. Normal operation.	D
AVDD1	3	No effect. Normal operation.	D
AINP	4	AINP stuck high. Conversion results correct only if AINP tied to AVDD1 in actual use, otherwise conversion results incorrect.	B
AINN	5	AINN stuck high. Conversion results correct only if AINN tied to AVDD1 in actual use, otherwise conversion results incorrect.	B
VCM	6	VCM stuck high. Conversion results incorrect.	B
REFP	7	REFP stuck high. Conversion results correct only if REFP is tied to AVDD1 in actual use, otherwise conversions results incorrect.	B
REFN	8	REFN stuck high. Conversion results incorrect.	B
$\overline{\text{RESET}}$	9	$\overline{\text{RESET}}$ stuck high. Normal operation except loss of $\overline{\text{RESET}}$ functionality.	B
$\overline{\text{CS}}$	10	$\overline{\text{CS}}$ stuck high. SPI communication not functional.	B
SDI	11	SDI stuck high. Loss of SPI input communications to the device. Conversion data readout remains functional.	B
SCLK	12	SCLK stuck high. SPI communication not possible.	B
SDO/$\overline{\text{DRDY}}$	13	SDO/$\overline{\text{DRDY}}$ stuck high. SPI communication not functional. Data ready not functional. Device damage plausible if SDO/$\overline{\text{DRDY}}$ is shorted to supply for extended period of time.	A
$\overline{\text{DRDY}}$	14	$\overline{\text{DRDY}}$ stuck high pin *is not* monitored. Normal operation. Device damage plausible if $\overline{\text{DRDY}}$ shorted to supply for extended period of time.	A
		$\overline{\text{DRDY}}$ stuck high, pin *is* monitored. No data-ready indication via $\overline{\text{DRDY}}$ to host possible. Device damage plausible if $\overline{\text{DRDY}}$ shorted to supply for extended period of time.	A
CLK	15	CLK stuck high in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK stuck high in *internal* clock mode. No effect. Normal operation.	D
IOVDD	16	No effect. Normal operation.	D
DGND	17	Device unpowered. Device not functional.	B
CAPD	18	CAPD stuck high. Permanent device damage.	A
START	19	START stuck high. Conversion results correct only if START tied to IOVDD in actual use. Otherwise conversion results incorrect because of loss of ability to control conversions.	B
AVSS	20	Device unpowered. Device not functional.	B

4.2 RUK Package

Figure 4-2 shows the ADS127L11 pin diagram for the RUK package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the ADS127L11 data sheet.

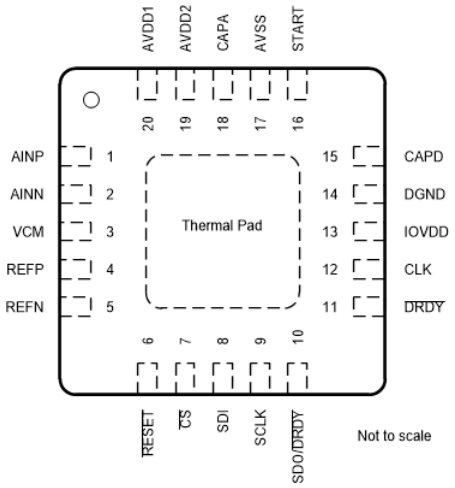

Figure 4-2. Pin Diagram (RUK Package)

Table 4-6. RUK Package Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP	1	AINP stuck low. Conversion results correct only if AINP tied to DGND in actual use, otherwise conversion results incorrect.	B
AINN	2	AINN stuck low. Conversion results correct only if AINN tied to DGND in actual use, otherwise conversions results incorrect.	B
VCM	3	VCM stuck low. Conversion results incorrect if actively used for external driver stage to set signal common-mode voltage.	B
REFP	4	REFP stuck low. Conversion results incorrect.	B
REFN	5	REFN stuck low. Conversion data correct only if REFN is tied to DGND in actual use, otherwise conversions results incorrect.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ stuck low. Device not functional.	B
$\overline{\text{CS}}$	7	$\overline{\text{CS}}$ stuck low in four-wire SPI mode. SPI communication not functional because of inability to control SPI data frames.	B
		$\overline{\text{CS}}$ stuck low in three-wire SPI mode. No effect, conversions results correct.	D
SDI	8	SDI stuck low. Loss of SPI input communications to the device. Conversion data readout remains functional.	B
SCLK	9	SCLK stuck low. SPI communication not possible.	B
SDO/$\overline{\text{DRDY}}$	10	SDO/$\overline{\text{DRDY}}$ stuck low. SPI *output* communication not possible. SPI input communications remains functional. Data-ready function via this pin not functional. Device damage plausible if SDO/$\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ stuck low, pin *is not* monitored by host. Normal operation. Device damage plausible if $\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
		$\overline{\text{DRDY}}$ stuck low, pin *is* monitored by host. No data-ready indication via $\overline{\text{DRDY}}$ to host possible. Device damage plausible if $\overline{\text{DRDY}}$ is shorted to ground for extended period of time.	A
CLK	12	CLK stuck low in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK stuck low in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	Device unpowered. Device not functional.	B
DGND	14	No effect. Normal operation.	D
CAPD	15	Device partially unpowered. Device not functional. Device damage plausible if CAPD shorted to ground for extended period of time.	A
START	16	START stuck low, pin is in active use by host. Loss of ability to control conversion timing. Conversion results incorrect.	B
		START stuck low, pin tied low in actual use (software control mode). No effect. Normal operation.	D
AVSS	17	No effect. Normal operation.	D
CAPA	18	Device partially unpowered. Device not functional. Device damage plausible if CAPA shorted to ground for extended period of time.	A
AVDD2	19	Device unpowered. Device not functional.	B
AVDD1	20	Device unpowered. Device not functional. Observe that the absolute maximum ratings for analog input and reference voltage pins of the device are met, otherwise device damage may be plausible.	A
Thermal pad	—	No effect. Normal operation.	D

Table 4-7. RUK Package Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP	1	State of AINP indeterminate. Conversion results indeterminate.	B
AINN	2	State of AINN indeterminate. Conversion results indeterminate.	B
VCM	3	VCM output voltage indeterminate. Conversion results indeterminate.	B
REFP	4	State of REFP indeterminate. Conversion results indeterminate.	B
REFN	5	State of REFN indeterminate. Conversion results indeterminate.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ stuck high. Loss of ability to reset the ADC via this pin.	B
$\overline{\text{CS}}$	7	State of $\overline{\text{CS}}$ indeterminate. SPI communication corrupted.	B
SDI	8	State of SDI indeterminate. Loss of SPI *input* communications to the device. Conversion data readout remains functional.	B
SCLK	9	State of SCLK indeterminate. SPI communication corrupted.	B
SDO/$\overline{\text{DRDY}}$	10	State of SDO/$\overline{\text{DRDY}}$ indeterminate. SPI *output* communication not possible. SPI input communications remains functional. Loss of data-ready function from this pin.	B
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ unconnected, pin *is not* monitored by host. No effect. Normal operation.	D
		$\overline{\text{DRDY}}$ unconnected, pin *is* monitored by host. No data-ready indication via $\overline{\text{DRDY}}$ to host possible.	B
CLK	12	CLK open circuit in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK open circuit in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	Device functionality undetermined. Device partially unpowered and not functional if START digital input pin is held low. Device can be powered through START digital input pin via internal ESD diode conduction path to IOVDD.	B
DGND	14	Device functionality indeterminate. Device may be unpowered, or powered through digital inputs via ESD diode path.	B
CAPD	15	CAPD voltage indeterminate. Conversion results indeterminate.	B
START	16	State of START indeterminate. Conversion results indeterminate.	B
AVSS	17	Device functionality indeterminate. Device unpowered and not functional if analog input or voltage reference pins are held low. Device can be powered through input or voltage reference drivers through internal ESD diode conduction path.	B
CAPA	18	CAPA voltage indeterminate. Conversion results indeterminate.	B
AVDD2	19	Device partially unpowered and held in reset. Device not functional.	B
AVDD1	20	Device functionality indeterminate. Device partially unpowered and not functional if analog input or voltage reference pins are held low. Device can be powered through input or voltage reference drivers through internal ESD diode conduction path.	B
Thermal pad	—	Device remains functional but possible performance degradation.	C

Table 4-8. RUK Package Pin FMA for Device Pins Short-Circuited to Adjacent Pins

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AINP	1	AINN	Conversion results incorrect. Conversion result is close to 0 V.	B
AINN	2	VCM	Conversion results incorrect.	B
VCM	3	REFP	Conversion results incorrect.	B
REFP	4	REFN	Conversion results incorrect.	B
REFN	5	$\overline{\text{RESET}}$	Not considered. Corner pins.	D
$\overline{\text{RESET}}$	6	$\overline{\text{CS}}$	Conversion results incorrect. Device not functional.	B
$\overline{\text{CS}}$	7	SDI	Loss of SPI *input* communications to the device if driver source impedance of $\overline{\text{CS}}$ exceeds that of SDI. Loss of *all* SPI communications to the device if driver source impedance of SDI exceeds that of $\overline{\text{CS}}$.	B
SDI	8	SCLK	Loss of SPI *input* communications to the device if driver source impedance of SCLK exceeds that of SDI. Loss of *all* SPI communications to the device if driver source impedance of SDI exceeds that of SCLK.	B
SCLK	9	SDO/$\overline{\text{DRDY}}$	Loss of SPI *output* communications from the device if driver source impedance of SCLK exceeds that of SDO/$\overline{\text{DRDY}}$. Loss of *all* SPI communications to the device if driver source impedance of SDO/$\overline{\text{DRDY}}$ exceeds that of SCLK. Device damage plausible if shorted together for an extended period of time.	A
SDO/$\overline{\text{DRDY}}$	10	$\overline{\text{DRDY}}$	Not considered. Corner pins.	D
$\overline{\text{DRDY}}$	11	CLK	*External* clock mode. Device not functional if driver source impedance of $\overline{\text{DRDY}}$ exceeds that of CLK. Indeterminate state of $\overline{\text{DRDY}}$ if driver source impedance of CLK exceeds that of $\overline{\text{DRDY}}$. Device damage plausible if shorted together for an extended period of time.	A
			Internal clock mode. The CLK pin has an external pullup or pulldown resistor to supply or ground (no active driver used). Normal operation.	D
CLK	12	IOVDD	*External* clock mode. Device not functional. Conversion results incorrect.	B
			Internal clock mode. Normal operation.	D
IOVDD	13	DGND	Device partially unpowered. Device not functional.	B
DGND	14	CAPD	Device partially unpowered. Device not functional. Device damage plausible if CAPD shorted to ground for extended period of time.	A
CAPD	15	START	Not considered. Corner pins.	D
START	16	AVSS	Conversion results correct only if START tied to DGND = AVSS in actual use. Otherwise, conversion results not correct because of inability to control conversions.	B
AVSS	17	CAPA	Device partially unpowered. Device not functional.	B
CAPA	18	AVDD2	CAPA stuck high. Permanent device damage.	A
AVDD2	19	AVDD1	No effect. Normal operation.	D
AVDD1	20	AINP	Not considered. Corner pins.	D
Thermal pad	—	All pins	See device pins short circuited to ground table (Table 4-6).	-

Table 4-9. RUK Package Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AINP	1	AINP stuck high. Conversion results correct only if AINP tied to AVDD1 in actual use, otherwise conversion results incorrect.	B
AINN	2	AINN stuck high. Conversion results correct only if AINN tied to AVDD1 in actual use, otherwise conversion results incorrect.	B
VCM	3	VCM stuck high. Conversion results incorrect.	B
REFP	4	REFP stuck high. Conversion results correct only if REFP is tied to AVDD1 in actual use, otherwise conversions results incorrect.	B
REFN	5	REFN stuck high. Conversion results incorrect.	B
$\overline{\text{RESET}}$	6	$\overline{\text{RESET}}$ stuck high. Normal operation except loss of $\overline{\text{RESET}}$ functionality.	B
$\overline{\text{CS}}$	7	$\overline{\text{CS}}$ stuck high. SPI communication not functional.	B
SDI	8	SDI stuck high. Loss of SPI input communications to the device. Conversion data readout remains functional.	B
SCLK	9	SCLK stuck high. SPI communication not possible.	B
SDO/$\overline{\text{DRDY}}$	10	SDO/$\overline{\text{DRDY}}$ stuck high. SPI communication not functional. Data ready not functional. Device damage plausible if SDO/$\overline{\text{DRDY}}$ is shorted to supply for extended period of time.	A
$\overline{\text{DRDY}}$	11	$\overline{\text{DRDY}}$ stuck high pin *is not* monitored. Normal operation. Device damage plausible if $\overline{\text{DRDY}}$ shorted to supply for extended period of time.	A
		$\overline{\text{DRDY}}$ stuck high, pin *is* monitored. No data-ready indication via $\overline{\text{DRDY}}$ to host possible. Device damage plausible if $\overline{\text{DRDY}}$ shorted to supply for extended period of time.	A
CLK	12	CLK stuck high in *external* clock mode. Device not functional. Conversion results incorrect.	B
		CLK stuck high in *internal* clock mode. No effect. Normal operation.	D
IOVDD	13	No effect. Normal operation.	D
DGND	14	Device not powered. Device not functional.	B
CAPD	15	CAPD stuck high. Permanent device damage.	A
START	16	START stuck high. Conversion results correct only if START tied to 5 V in actual use. Otherwise conversion results incorrect because of loss of ability to control conversions.	B
AVSS	17	Device unpowered. Device not functional.	B
CAPA	18	CAPA stuck high. Permanent device damage.	A
AVDD2	19	No effect. Normal operation.	D
AVDD1	20	No effect. Normal operation.	D
Thermal pad	—	Device unpowered. Device not functional.	B

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