Functional Safety Information

LMK00804B-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the LMK00804B-Q1 (VQFN-16 package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

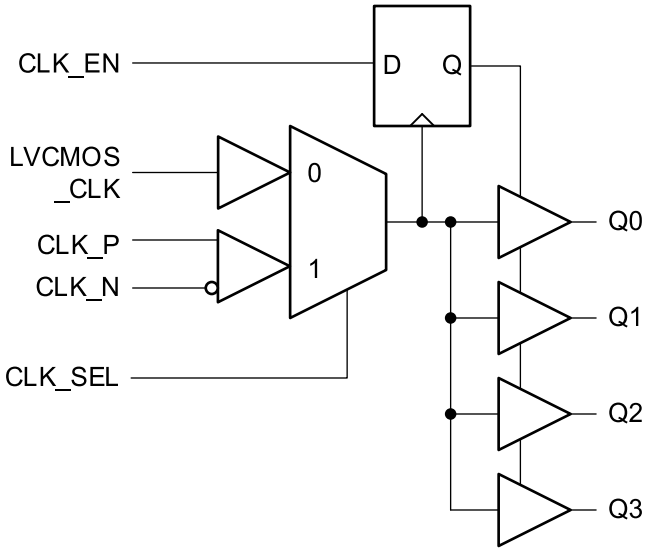

Figure 1-1. Functional Block Diagram

The LMK00804B-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the LMK00804B-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	8
Die FIT rate	2
Package FIT rate	6

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 100 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS ASICs Analog & Mixed =< 50 V supply	20 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the LMK00804B-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Incorrect input selected	60
Performance degradation of output clocks	40

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the LMK00804B-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VDD (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the LMK00804B-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the LMK00804B-Q1 data sheet.

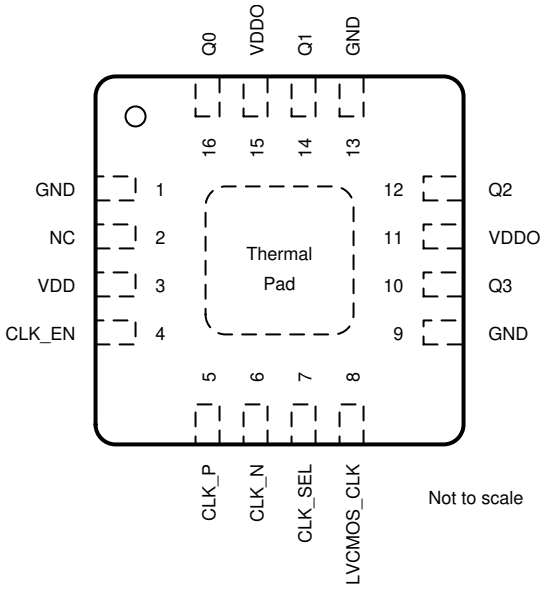

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- VDD = VDDO = 3.3 V
- CLK_EN and CLK_SEL pulled to VDD with 1k Ohm resistor.
- 100 MHz LVDS signal applied to CLK_P/N.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	No effect. Normal operation.	D
NC	2	Outputs disabled.	B
VDD	3	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
CLK_EN	4	CLK_EN pulled low. Outputs disabled to logic low state.	B

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
CLK_P	5	Invalid input clock. No output clocks if CLK_P/N input is selected.	B
CLK_N	6	Invalid input clock. No output clocks if CLK_P/N input is selected.	B
CLK_SEL	7	CLK_SEL pulled low. LVCMOS_CLK selected as input.	B
LVCMOS_CLK	8	Invalid input clock. No output clocks if LVCMOS_CLK input is selected.	B
GND	9	No effect. Normal operation.	D
Q3	10	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	11	Outputs not functional.	B
Q2	12	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
GND	13	No effect. Normal operation.	D
Q1	14	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	15	Outputs not functional.	B
Q0	16	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation possible.	C
NC	2	No effect. Normal operation.	D
VDD	3	Device unpowered. Device not functional.	B
CLK_EN	4	Internally pulled high. Outputs enabled.	D
CLK_P	5	Internally pulled low. No output clock.	B
CLK_N	6	Internally biased to VDD/2 when left floating. Normal operation for single ended input.	D
CLK_SEL	7	Internally pulled high. CLK_P, CLK_N (pins 5, 6) selected.	D
LVCMOS_CLK	8	The internal pulldown resistor ensures a low state when this input is left floating.	B
GND	9	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation possible.	C
Q3	10	No output.	C
VDDO	11	Outputs not powered. No output.	B
Q2	12	No output.	C
GND	13	With this pin open, the device has a weaker ground connection than intended by design. Other ground pins maintain connection. Performance degradation possible.	C
Q1	14	No output.	C
VDDO	15	Outputs not powered. No output.	B
Q0	16	No output.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	NC	Outputs disabled.	B
NC	2	VDD	No effect. Normal operation.	D
VDD	3	CLK_EN	Pulled high. Outputs enabled.	D
CLK_EN	4	CLK_P	Not considered. Corner pin.	D
CLK_P	5	CLK_N	Clock input shorted. May create noise on output, if selected.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
CLK_N	6	CLK_SEL	CLK_N pulled high. Potential duty cycle distortion. CLK_SEL pulled high. CLK_P, CLK_N (pins 5, 6) selected.	C
CLK_SEL	7	LVCMOS_CLK	Both pins pulled to Vdd/2. CLK_SEL will randomly selects LVCMOS_CLK or CLK_P/N.	B
LVCMOS_CLK	8	GND	Not considered. Corner pin.	D
GND	9	Q3	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Q3	10	VDDO	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	11	Q2	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Q2	12	GND	Not considered. Corner pin.	D
GND	13	Q1	Output pulled low. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Q1	14	VDDO	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	15	Q0	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
Q0	16	GND	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	1	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
NC	2	No effect. Normal operation.	D
VDD	3	No effect. Normal operation.	D
CLK_EN	4	Pulled high. Outputs enabled.	D
CLK_P	5	If selected with CLK_SEL, input signal may not be recognized.	B
CLK_N	6	If selected with CLK_SEL, input signal may not be recognized.	B
CLK_SEL	7	Pulled high. CLK_P, CLK_N (pins 5, 6) selected.	D
LVCMOS_CLK	8	If input selected, outputs remain steady low or high.	B
GND	9	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
Q3	10	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	11	No effect. Normal operation.	D
Q2	12	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
GND	13	Device unpowered. Device not functional. Observe that the absolute maximum ratings for all pins of the device are met, otherwise device damage may be plausible.	A
Q1	14	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A
VDDO	15	No effect. Normal operation.	D
Q0	16	Output pulled high. No output clock. Long periods of high current flow through output transistors may cause device damage.	A

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265