*Functional Safety Information*

# *TPS7B4255-Q1*
# *Functional Safety FIT Rate, FMD and Pin FMA*

## Table of Contents



## Trademarks

# 1 Overview

This document contains information for the TPS7B4255-Q1 (DBV and DYB packages) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

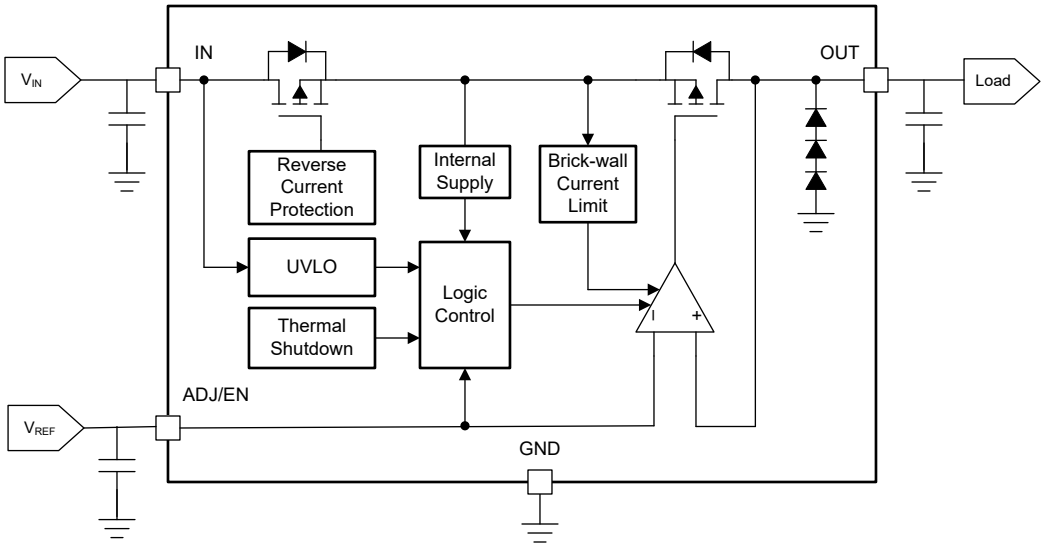


**Figure 1-1. Functional Block Diagram**

The TPS7B4255-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

# 2 Functional Safety Failure In Time (FIT) Rates

## 2.1 DBV Package

This section provides functional safety failure in time (FIT) rates for the DBV package of the TPS7B4255-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 16 |
| Die FIT rate | 12 |
| Package FIT rate | 4 |

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Power amplifier and regulator ≤ 1 Watt – (LDO) | 40 FIT | 70°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

## 2.2 DYB Package

This section provides functional safety failure in time (FIT) rates for the DYB package of the TPS7B4255-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

**Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11**

| FIT IEC TR 62380 / ISO 26262 | FIT (Failures Per $10^9$ Hours) |
|---|---|
| Total component FIT rate | 12 |
| Die FIT rate | 8 |
| Package FIT rate | 4 |

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Motor control from table 11
- Power dissipation: 300 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

**Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2**

| Table | Category | Reference FIT Rate | Reference Virtual $T_J$ |
|---|---|---|---|
| 4 | Power amplifier and regulator ≤ 1 Watt – (LDO) | 40 FIT | 70°C |

The reference FIT rate and reference virtual $T_J$ (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

# 3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPS7B4255-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

**Table 3-1. Die Failure Modes and Distribution**

| Die Failure Modes | Failure Mode Distribution (%) |
|---|---|
| No output (output low) | 40 |
| Output high (following input) | 40 |
| Short any two adjacent pins | 5 |
| Output not in specification | 5 |

# 4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the TPS7B4255-Q1 (DBV and DYB packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

**Table 4-1. TI Classification of Failure Effects**

| Class | Failure Effects |
|---|---|
| A | Potential device damage that affects functionality |
| B | No device damage, but loss of functionality |
| C | No device damage, but performance degradation |
| D | No device damage, no impact to functionality or performance |

## 4.1 DBV Package

Figure 4-1 shows the TPS7B4255-Q1 pin diagram for the DBV package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4255-Q1 data sheet.

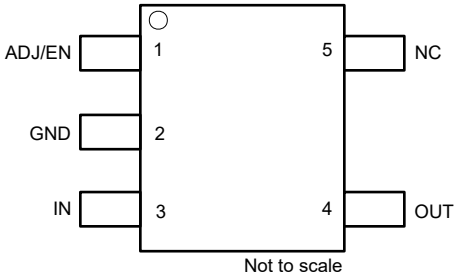


**Figure 4-1. Pin Diagram (DBV) Package**

**Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device is disabled, resulting in no output voltage. | B |
| GND | 2 | No effect. Normal operation. | D |
| IN | 3 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| OUT | 4 | Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. | B |
| NC | 5 | No effect. Normal operation. | D |

**Table 4-3. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device state is unknown. If the device is on, the output voltage is indeterminate. | B |
| GND | 2 | There is no current loop for the supply voltage. The device is not operational and does not regulate. | B |
| IN | 3 | Power is not supplied to the device. | B |
| OUT | 4 | The device output is disconnected from the load. | B |
| NC | 5 | No effect. Normal operation. | D |

**Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| ADJ/EN | 1 | GND | The device is disabled, resulting in no output voltage. | B |
| GND | 2 | IN | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| OUT | 4 | NC | No effect. Normal operation. | D |

**Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device operates as a switch in dropout mode. The output tracks the input minus the dropout voltage. | B |
| GND | 2 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| IN | 3 | No effect. Normal operation. | D |
| OUT | 4 | Regulation is not possible. $V_{OUT} = V_{IN}$. | B |
| NC | 5 | No effect. Normal operation. | D |

## 4.2 DYB Package

Figure 4-2 shows the TPS7B4255-Q1 pin diagram for the DYB package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the TPS7B4255-Q1 data sheet.

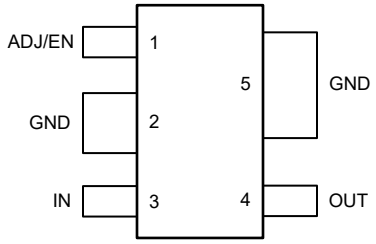


**Figure 4-2. Pin Diagram (DYB Package)**

**Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device is disabled, resulting in no output voltage. | B |
| GND | 2 | No effect. Normal operation. | D |
| IN | 3 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| OUT | 4 | Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. | B |
| GND | 5 | No effect. Normal operation. | D |

**Table 4-7. Pin FMA for Device Pins Open-Circuited**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device state is unknown. If the device is on, the output voltage is indeterminate. | B |
| GND | 2 | The device operates normally with slightly degraded performance as long as pin 5 is connected properly. | C |
| IN | 3 | Power is not supplied to the device. | B |
| OUT | 4 | The device output is disconnected from the load. | B |
| GND | 5 | The device operates normally with slightly degraded performance as long as pin 2 is connected properly. | C |

**Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin**

| Pin Name | Pin No. | Shorted to | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|---|
| ADJ/EN | 1 | GND | The device is disabled, resulting in no output voltage. | B |
| GND | 2 | IN | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| OUT | 4 | GND | Regulation is not possible, the device operates at current limit. The device can cycle in and out of thermal shutdown. | B |

**Table 4-9. Pin FMA for Device Pins Short-Circuited to Supply**

| Pin Name | Pin No. | Description of Potential Failure Effects | Failure Effect Class |
|---|---|---|---|
| ADJ/EN | 1 | The device operates as a switch in dropout mode. The output tracks the input minus the dropout voltage. | B |
| GND | 2 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |
| IN | 3 | No effect. Normal operation. | D |
| OUT | 4 | Regulation is not possible. $V_{OUT} = V_{IN}$. | B |
| GND | 5 | Power is not supplied to the device. System performance depends on upstream current limiting. | B |

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