ADC3683-SEP ADC3683-EP 18 ビット、65MSPS、低ノイズ、低消費電力デュアル チャネル ADC

1 特長

- 耐放射線特性 (-SEP のみ):
  - 単一イベント ラッチアップ (SEL) 耐性 (最大): LET = 43 MeV-cm^2/mg
  - LET = 43MeV-cm^2/mg まで、SEFI (Single-Event Functional Interrupt) 特性を評価済み
  - 吸収線量 (TID):30krad(Si)
- エンハンスド製品 (- EP と -SEP):
  - ASTM E595 アウトガス仕様に適合
  - ベンダー品目の図面 (VID)
  - 温度範囲:-55℃ ～ 105℃
  - 単一の製造、アセンブリ、テスト施設
  - 金ボンド ワイヤ、NiPdAu リード仕上げ
  - ウェハー ロットをトレース可能
  - 長期にわたる製品ライフ サイクル
- 2 チャネル、65 MSPS ADC
- 18 ビットの分解能 (ミッシング コードなし)
- ノイズ・フロア:-160dBFS/Hz
- チャネルあたり 94mW の低消費電力 (65MSPS 時)
- レイテンシ:1～2 クロック サイクル
- INL:±7、DNL:±0.7LSB (標準値)
- リファレンス オプション:外部または内部
- オンチップ DSP (オプション / バイパス可能)
  - デシメーション比:2、4、8、16、32
  - 32 ビット NCO
- シリアル LVDS デジタル インターフェイス (2 線式、1 線式、1/2 線式)
- 小さい占有面積:40-QFN (5 x 5mm) パッケージ
- スペクトル性能 (f_{IN} = 5MHz):
  - 信号対雑音比:83.8dBFS
  - SFDR:89dBc HD2、HD3
  - SFDR:101dBFS の最大スプリアス

2 アプリケーション

- 衛星光通信ペイロード
- 衛星画像処理ペイロード
- 衛星通信ペイロード
- 衛星レーダーおよび LIDAR ペイロード

3 概要

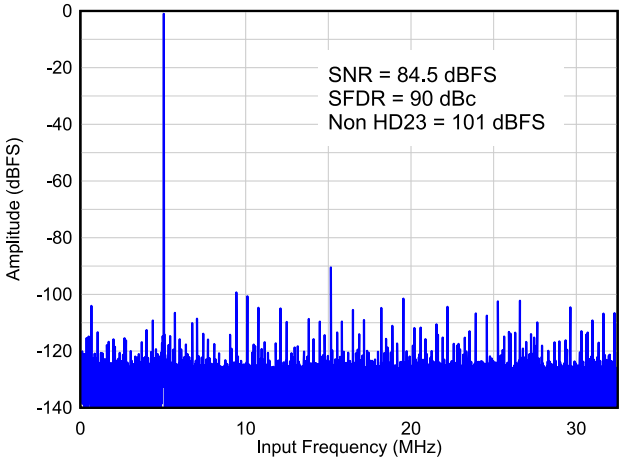
ADC3683-xEP は、低ノイズ、超低消費電力、18 ビット、65MSPS のデュアル チャネル高速 A/D コンバータ (ADC) です。きわめて低いノイズ性能を実現するように設計されており、デバイスのノイズ スペクトル密度は -160dBFS/Hz となり、直線性とダイナミック レンジを備えています。ADC3683-xEP は、IF サンプリングをサポートすると共に、優れた DC 精度を達成しています。多様なアプリケーションに合わせて設計されたデバイスを作成できます。レイテンシがわずか 1 クロック サイクルと短いため、高速な制御ループを実現できます。この ADC の消費電力は 1 チャネルあたりわずか 94mW (65MSPS 時) であり、サンプリング レートを下げることで、消費電力を良好に低減できます。

ADC3683-xEP は、シリアル LVDS (SLVDS) インターフェイスを使用してデータを出力し、デジタル相互接続の数を最小限に抑えます。このデバイスは、2 レーン、1 レーン、およびハーフ レーンのオプションをサポートしています。本デバイスは 40 ピンの QFN パッケージ (5mm x 5mm) で供給され、-55～+105℃の拡張温度範囲をサポートしています。

パッケージ情報

部品番号	パッケージ(1)	パッケージ サイズ(2)
ADC3683-SEP	VQFN (40)	5 mm × 5mm
ADC3683-EP		

(1) 詳細については、セクション 12 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



FFT : Fs = 65MSPS、f_{in} = 5MHz

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

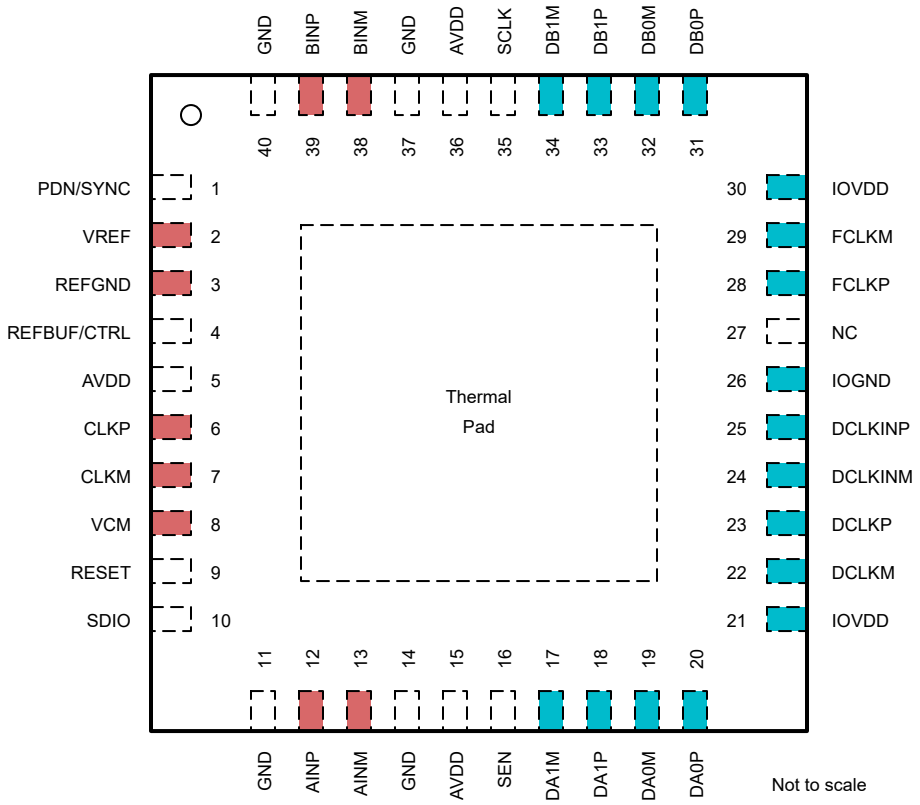


図 4-1. RSB (WQQFN) Package, 40-Pin (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
INPUT/REFERENCE			
AINP	12	I	Positive analog input, channel A
AINM	13	I	Negative analog input, channel A
BINP	39	I	Positive analog input, channel B
BINM	38	I	Negative analog input, channel B
VCM	8	O	Common-mode voltage output for the analog inputs, 0.95V
VREF	2	I	External voltage reference input, 1.6V
REFGND	3	I	Reference ground input, 0V
CLOCK			
CLKP	6	I	Positive differential sampling clock input for the ADC
CLKM	7	I	Negative differential sampling clock input for the ADC
CONFIGURATION			
PDN/SYNC	1	I	Power down/Synchronization input. This pin is configured via the SPI interface. Active high. This pin has an internal 21kΩ pull-down resistor.

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表 4-1. Pin Functions (続き)

PIN		TYPE	DESCRIPTION
NAME	NO.		
REFBUF/ CTRL	4	I	This pin is used to configure the default sampling clock type and voltage reference source upon power up. There is an internal 100kΩ pull up resistor to AVDD
RESET	9	I	Hardware reset. Active high. This pin has an internal 21kΩ pull-down resistor.
SEN	16	I	Serial interface enable. Active low. This pin has an internal 21kΩ pull-up resistor to AVDD.
SCLK	35	I	Serial interface clock input. This pin has an internal 21kΩ pull-down resistor.
SDIO	10	I/O	Serial interface data input and output. This pin has an internal 21kΩ pull-down resistor.
NC	27	-	Do not connect
DIGITAL INTERFACE			
DA0P	20	O	Positive differential serial LVDS output for lane 0, channel A
DA0M	19	O	Negative differential serial LVDS output for lane 0, channel A
DA1P	18	O	Positive differential serial LVDS output for lane 1, channel A
DA1M	17	O	Negative differential serial LVDS output for lane 1, channel A
DB0P	31	O	Positive differential serial LVDS output for lane 0, channel B
DB0M	32	O	Negative differential serial LVDS output for lane 0, channel B
DB1P	33	O	Positive differential serial LVDS output for lane 1, channel B
DB1M	34	O	Negative differential serial LVDS output for lane 1, channel B
DCLKP	23	O	Positive differential serial LVDS bit clock output.
DCLKM	22	O	Negative differential serial LVDS bit clock output.
FCLKP	28	O	Positive differential serial LVDS frame clock output.
FCLKM	29	O	Negative differential serial LVDS frame clock output.
DCLKINP	25	I	Positive differential serial LVDS bit clock input. Internal 100Ω differential termination.
DCLKINM	24	I	Negative differential serial LVDS bit clock input. Internal 100Ω differential termination.
POWER SUPPLY			
AVDD	5, 15, 36	I	Analog 1.8V power supply
GND	11, 14, 37, 40,	I	Ground, 0V, PowerPAD™
IOVDD	21, 30	I	1.8V power supply for digital interface
IOGND	26	I	Ground, 0V for digital interface

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD, IOVDD		–0.3	2.1	V
Supply voltage range, GND, IOGND, REFGND		–0.3	0.3	V
Voltage applied to input pins	AINP/M, BINP/M, CLKP/M, VREF, REFBUF	–0.3	MIN(2.1, AVDD+0.3)	V
	PDN/SYNC, RESET, SCLK, SEN, SDIO	–0.3	MIN(2.1, AVDD+0.3)	
	DCLKINP/M	–0.3	MIN(2.1, IOVDD+0.3)	
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	AVDD(1)	1.75	1.8	1.85	V
	IOVDD(1)	1.75	1.8	1.85	V
T_A	Operating free-air temperature	–55		105	°C
T_J	Operating junction temperature			105(2)	°C

(1) Measured to GND.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

5.4 Thermal Information

THERMAL METRIC(1)		ADC3683-SEP RSB (QFN) 40 Pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	30.7	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	16.4	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.5	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics - Power Consumption

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, external 1.6 V reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC3683-SEP: 65 MSPS						
I_{AVDD}	Analog supply current	External reference		63	82	mA
I_{IOVDD}	I/O supply current	2-wire		41	47	mA
P_{DIS}	Power dissipation	External reference, 2-wire		187	232	mW
I_{IOVDD}	I/O supply current	2-wire, 1/2-swing		30		mA
		4x real decimation, 1-wire		39		
		4x real decimation, 1/2-wire		36		
		16x real decimation, 1-wire		37		
		16x real decimation, 1/2-wire		33		
		4x complex decimation, 1-wire		44		
		16x complex decimation, 1-wire		40		
		16x complex decimation, 1/2-wire		36		
I_{AVDD}	Internal reference, additional analog supply current			3		mA
	External 1.2V reference (REFBUF), additional analog supply current			0.3		
	Single ended clock input, reduces analog supply current by	Enabled via SPI		0.7		
P_{DIS}	Power consumption in global power down mode	Default mask settings, internal reference		5		mW
		Default mask settings, external reference		9		

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5.6 Electrical Characteristics - DC Specifications

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
No missing codes			18			bits
PSRR		F_{IN} = 1 MHz		50		dB
DNL	Differential nonlinearity	F_{IN} = 5 MHz	-1.8	± 0.7	+1.8	LSB
INL	Integral nonlinearity	F_{IN} = 5 MHz		± 7	± 19	LSB
V_{OS_ERR}	Offset error			± 130	± 510	LSB
V_{OS_DRIFT}	Offset drift over temperature			± 0.2		LSB/°C
$GAIN_{ERR}$	Gain error	External 1.6V Reference		± 2.3		%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	External 1.6V Reference		68		ppm/°C
$GAIN_{ERR}$	Gain error	Internal Reference		± 3.5		%FSR
$GAIN_{ERR}$	Gain error	Internal Reference, Fs= 10 MSPS	-2.5	-0.6	+2.5	%FSR
$GAIN_{DRIFT}$	Gain drift over temperature	Internal Reference		242		ppm/°C
Transition Noise	Transition Noise			5		LSB

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5.6 Electrical Characteristics - DC Specifications (続き)

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC ANALOG INPUT (AINP/M, BINP/M)						
FS	Input full scale	Differential		3.2		Vpp
V_{CM}	Input common model voltage		0.9	0.95	1.0	V
R_{IN}	Differential input resistance	F_{IN} = 100 kHz		8		kΩ
C_{IN}	Differential input Capacitance	F_{IN} = 100 kHz		7		pF
V_{OCM}	Output common mode voltage			0.95		V
BW	Analog Input Bandwidth (-3dB)			200		MHz
Internal Voltage Reference						
V_{REF}	Internal reference voltage			1.6		V
V_{REF} Output Impedance				8		Ω
Reference Input Buffer (REFBUF)						
External reference voltage				1.2		V
External voltage reference (VREF)						
V_{REF}	External voltage reference			1.6		V
Input Current				0.3		mA
Input impedance				5.3		kΩ
Clock Input (CLKP/M)						
Input clock frequency			1		65	MHz
V_{ID}	Differential input voltage		0.5	1	3.6	Vpp
V_{CM}	Input common mode voltage			0.9		V
R_{IN}	Single ended input resistance to common mode			5		kΩ
C_{IN}	Single ended input capacitance			1.5		pF
Clock duty cycle			40	50	60	%
Digital Inputs (RESET, PDN, SCLK, SEN, SDIO)						
V_{IH}	High level input voltage		1.4			V
V_{IL}	Low level input voltage				0.4	V
I_{IH}	High level input current			90	150	uA
I_{IL}	Low level input current		-150	-90		uA
C_I	Input capacitance			1.5		pF
Digital Output (SDOUT)						
V_{OH}	High level output voltage	I_{LOAD} = -400 uA	IOVDD – 0.1	IOVDD		V
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.1	V
SLVDS Interface						
Output data rate		per differential SLVDS output pair			1000	Mbps
V_{ID}	Differential input voltage	DCLKIN	200	350	650	mVpp
V_{CM}	Input common mode voltage		1	1.2	1.3	V
V_{OD}	Differential output voltage		500	700	850	mVpp
V_{CM}	Output common mode voltage			1.0		V

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5.7 Electrical Characteristics - AC Specifications

Typical values at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC3683-SEP 65 MSPS:						
NSD	Noise Spectral Density	f_{IN} = 1.1 MHz, A_{IN} = –20 dBFS		–160		dBFS/Hz
SNR	Signal to noise ratio	f_{IN} = 1.1 MHz, A_{IN} = –20 dBFS		84.8		dBFS
		f_{IN} = 1.1 MHz		84.2		
		f_{IN} = 5 MHz	81.0	83.8		
		f_{IN} = 10 MHz		83.6		
		f_{IN} = 20 MHz		82.6		
		f_{IN} = 40 MHz		81.0		
		f_{IN} = 70 MHz		77.3		
SINAD	Signal to noise and distortion ratio	f_{IN} = 1.1 MHz		80.0		dBFS
		f_{IN} = 5 MHz		82.7		
		f_{IN} = 10 MHz		82.7		
		f_{IN} = 20 MHz		80.2		
		f_{IN} = 40 MHz		78.7		
		f_{IN} = 70 MHz		75.8		
ENOB	Effective number of bits	f_{IN} = 1.1 MHz		13.7		bits
		f_{IN} = 5 MHz		13.6		
		f_{IN} = 10 MHz		13.6		
		f_{IN} = 20 MHz		13.4		
		f_{IN} = 40 MHz		13.2		
		f_{IN} = 70 MHz		12.5		
THD	Total Harmonic Distortion (First five harmonics)	f_{IN} = 1.1 MHz		81		dBc
		f_{IN} = 5 MHz	80.5	88		
		f_{IN} = 10 MHz		89		
		f_{IN} = 20 MHz		83		
		f_{IN} = 40 MHz		82		
		f_{IN} = 70 MHz		80		
SFDR	Spur free dynamic range including second and third harmonic distortion	f_{IN} = 1.1 MHz		82		dBc
		f_{IN} = 5 MHz	81.5	89		
		f_{IN} = 10 MHz		92		
		f_{IN} = 20 MHz		85		
		f_{IN} = 40 MHz		84		
		f_{IN} = 70 MHz		82		
Non HD2,3	Spur free dynamic range (excluding HD2 and HD3)	f_{IN} = 1.1 MHz		101		dBFS
		f_{IN} = 5 MHz	90	101		
		f_{IN} = 10 MHz		100		
		f_{IN} = 20 MHz		97		
		f_{IN} = 40 MHz		91		
		f_{IN} = 70 MHz		88		
IMD3	Two tone inter-modulation distortion	f_1 = 10 MHz, f_2 = 12 MHz, A_{IN} = -7 dBFS/tone		89		dBc
		f_1 = 40 MHz, f_2 = 45 MHz, A_{IN} = -7 dBFS/tone		84		

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5.8 Timing Requirements

Typical values at T_A = 25°C, MIN and MAX timing values are characterized over the full temperature range T_{MIN} = –55°C to T_{MAX} = 105°C and are NOT production tested, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC Timing Specifications						
t_{AD}	Aperture Delay			0.85		ns
t_A	Aperture Jitter	Square wave clock with fast edges		180		fs
t_J	Jitter on DCLKIN				± 50	ps
t_{ACQ}	Signal acquisition period, referenced to sampling clock falling edge	F_S = 10 Msps		$-T_S/2$		Sampling Clock Period
		F_S = 25 Msps		$-T_S/2$		
		F_S = 65 Msps		$-T_S/4$		
t_{CONV}	Signal conversion period, referenced to sampling clock falling edge	F_S = 10 Msps		$+T_S \times 1/5$		Sampling Clock Period
		F_S = 25 Msps		$+T_S \times 3/8$		
		F_S = 65 Msps		$+T_S \times 5/8$		
Wake up time	Time to valid data after coming out of power down. Internal reference.	Bandgap reference enabled, single ended clock			17.6	us
		Bandgap reference enabled, differential clock			12.9	
		Bandgap reference disabled, single ended clock			2.2	ms
		Bandgap reference disabled, differential clock			2.2	
	Time to valid data after coming out of power down. External 1.6V reference.	Bandgap reference enabled, single ended clock			15.9	us
		Bandgap reference enabled, differential clock			12.9	
		Bandgap reference disabled, single ended clock			1.7	ms
		Bandgap reference disabled, differential clock			1.7	
$t_{S,SYNC}$	Setup time for SYNC input signal	Referenced to sampling clock rising edge	500			ps
$t_{H,SYNC}$	Hold time for SYNC input signal		600			
ADC Latency	Signal input to data output	SLVDS 2-wire		2		ADC clock cycles
		SLVDS 1-wire		1		
ADC Latency	Signal input to data output	SLVDS 2-wire		2		ADC clock cycles
		SLVDS 1-wire		1		
		SLVDS 1/2-wire		1		
Add Latency	Real decimation by 2			21		Output clock cycles
	Complex decimation by 2			22		
	Real or complex decimation by 4, 8, 16, 32			23		

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5.8 Timing Requirements (続き)

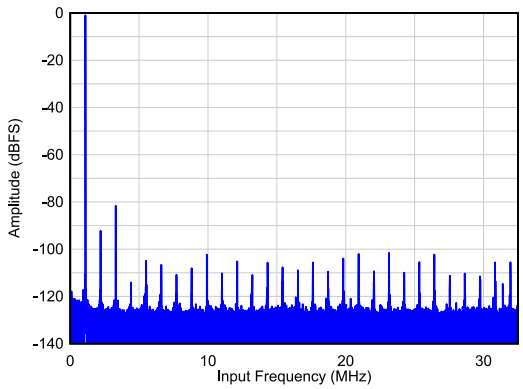
Typical values at T_A = 25°C, MIN and MAX timing values are characterized over the full temperature range T_{MIN} = –55°C to T_{MAX} = 105°C and are NOT production tested, ADC sampling rate = 65 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, 1.6 V external reference, and –1-dBFS differential input, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Interface Timing: Serial LVDS Interface						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + T_{DCLK} + t_{CDCLK}	3 + T_{DCLK} + t_{CDCLK}	4 + T_{DCLK} + t_{CDCLK}	ns
		Delay between sampling clock falling edge to DCLKIN falling edge >= 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + t_{CDCLK}	3 + t_{CDCLK}	4 + t_{CDCLK}	ns
t_{CD}	DCLK rising edge to output data delay, 2-wire SLVDS	Fout = 10 MSPS, DA/B0,1 = 90 MBPS	0	0.1		ns
		Fout = 25 MSPS, DA/B0,1 = 225 MBPS	0	0.1		
		Fout = 65 MSPS, DA/B0,1 = 585 MBPS	0	0.1		
	DCLK rising edge to output data delay, 1-wire SLVDS	Fout = 10 MSPS, DA/B0 = 180 MBPS	0.1	0.2		
		Fout = 25 MSPS, DA/B0 = 450 MBPS	0	0.1		
		Fout = 55 MSPS, DA/B0 = 990 MBPS	-0.4	0.1		
	DCLK rising edge to output data delay, 1/2-wire SLVDS	Fout = 5 MSPS, DA0 = 180 MBPS	0	0.1		
		Fout = 10 MSPS, DA0 = 360 MBPS	0	0.1		
		Fout = 25 MSPS, DA0 = 720 MBPS	0	0.1		
t_{DV}	Data valid, 2-wire SLVDS	Fout = 10 MSPS, DA/B0,1 = 90 MBPS	10.5	10.7		ns
		Fout = 25 MSPS, DA/B0,1 = 225 MBPS	4.0	4.1		
		Fout = 65 MSPS, DA/B0,1 = 585 MBPS	1.3	1.4		
	Data valid, 1-wire SLVDS	Fout = 10 MSPS, DA/B0 = 180 MBPS	4.7	4.8		
		Fout = 25 MSPS, DA/B0 = 450 MBPS	1.8	1.9		
		Fout = 55 MSPS, DA/B0 = 990 MBPS	0.5	0.6		
	Data valid, 1/2-wire SLVDS	Fout = 5 MSPS, DA0 = 180 MBPS	4.7	4.8		
		Fout = 10 MSPS, DA0 = 360 MBPS	2.4	2.5		
		Fout = 25 MSPS, DA0 = 900 MBPS	0.6	0.7		
SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input						
$f_{CLK(SCLK)}$	Serial clock frequency				20	MHz
$t_{SU(SEN)}$	SEN to rising edge of SCLK		10			ns
$t_{H(SEN)}$	SEN from rising edge of SCLK		9			ns
$t_{SU(SDIO)}$	SDIO to rising edge of SCLK		17			ns
$t_{H(SDIO)}$	SDIO from rising edge of SCLK		9			ns
SERIAL PROGRAMMING INTERFACE (SDIO) - Output						
$t_{(OZD)}$	SDIO tri-state to driven		3.9		10.8	ns
$t_{(ODZ)}$	SDIO data to tri-state		3.4		14	ns
$t_{(OD)}$	SDIO valid from falling edge of SCLK		3.9		10.8	ns

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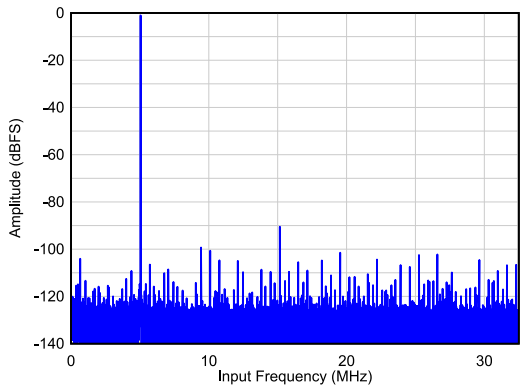
5.9 Typical Characteristics - ADC3683

Typical values at T_A = 25 °C, ADC sampling rate = 65MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



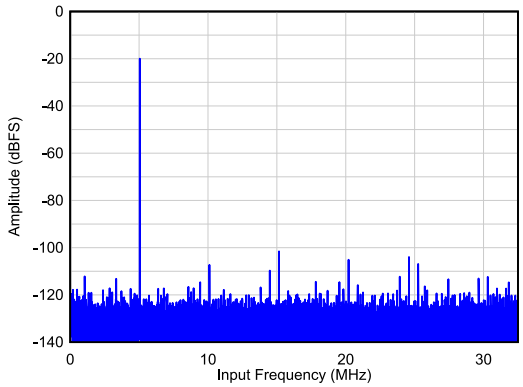
SNR = 84.2dBFS, SFDR = 81dBc, Non HD23 = 101dBFS

図 5-1. Single Tone FFT at F_{IN} = 1 MHz



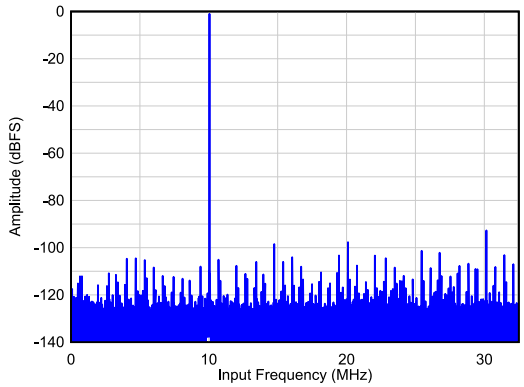
SNR = 83.8dBFS, SFDR = 89dBc, Non HD23 = 99dBFS

図 5-2. Single Tone FFT at F_{IN} = 5MHz



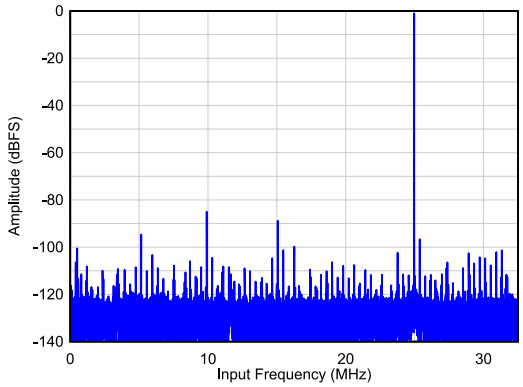
SNR = 84.8dBFS, SFDR = 81dBc, Non HD23 = 103dBFS

図 5-3. Single Tone FFT at F_{IN} = 5MHz, A_{IN} = -20dBFS



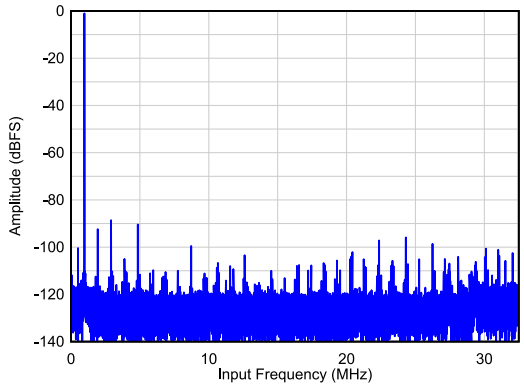
SNR = 83.8dBFS, SFDR = 92dBc, Non HD23 = 98dBFS

図 5-4. Single Tone FFT at F_{IN} = 10MHz



SNR = 81.1dBFS, SFDR = 84dBc, Non HD23 = 95dBFS

図 5-5. Single Tone FFT at F_{IN} = 40MHz



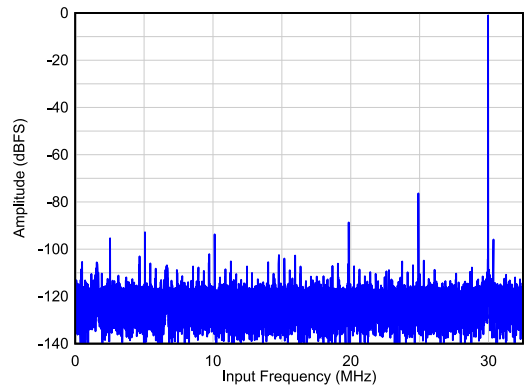
SNR = 77.3dBFS, SFDR = 86dBc, Non HD23 = 92dBFS

図 5-6. Single Tone FFT at F_{IN} = 64MHz

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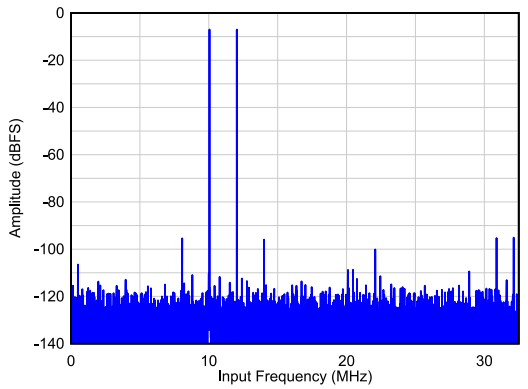
5.9 Typical Characteristics - ADC3683 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



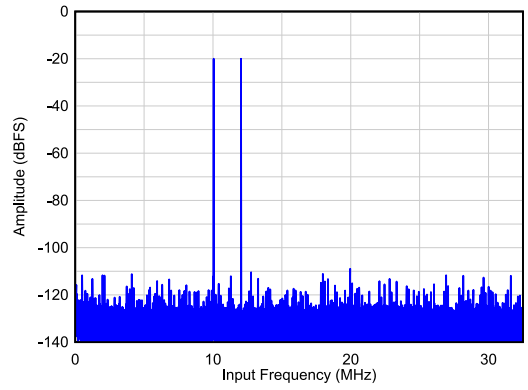
SNR = 75.1dBFS, SFDR = 75dBc, Non HD23 = 93dBFS

図 5-7. Single Tone FFT at F_{IN} = 100MHz



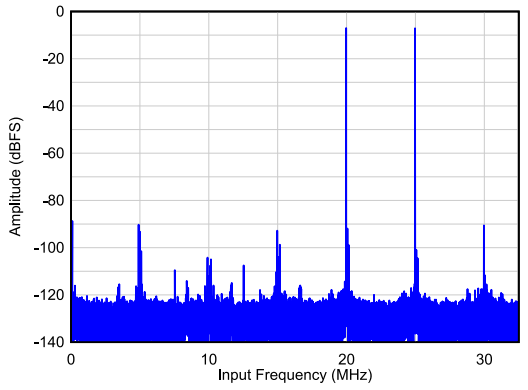
A_{IN} = -7dBFS/tone, IMD3 = 88dBc

図 5-8. Two Tone FFT at F_{IN} = 10/12MHz



A_{IN} = -20dBFS/tone, IMD3 = 95dBc

図 5-9. Two Tone FFT at F_{IN} = 10/12MHz



A_{IN} = -7dBFS/tone, IMD3 = 83dBc

図 5-10. Two Tone FFT at F_{IN} = 40/45MHz

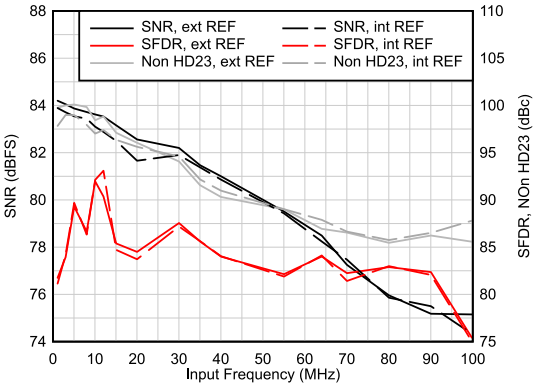


図 5-11. AC Performance vs Input Frequency

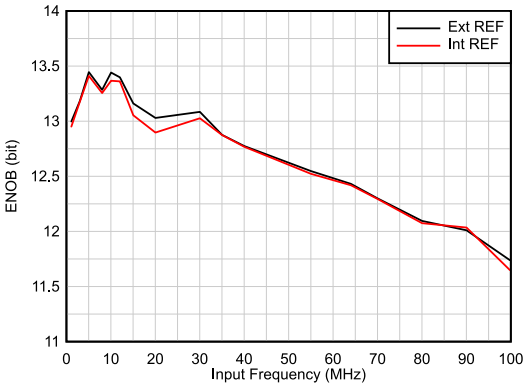
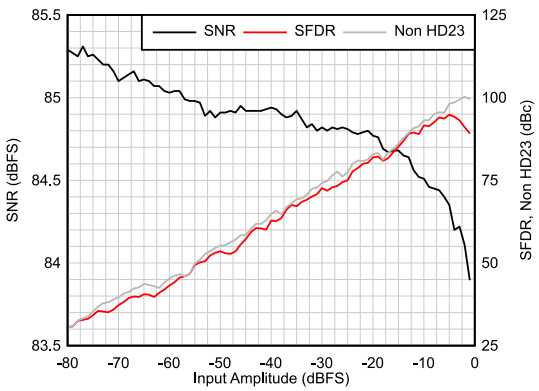


図 5-12. ENOB vs Input Frequency

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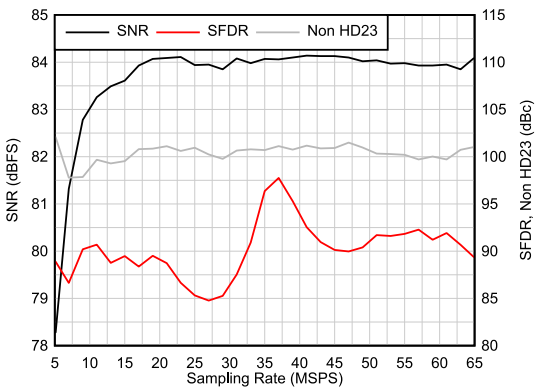
5.9 Typical Characteristics - ADC3683 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



F_{IN} = 5MHz

図 5-13. AC Performance vs Input Amplitude



F_{IN} = 5MHz

図 5-14. AC Performance vs Sampling Rate

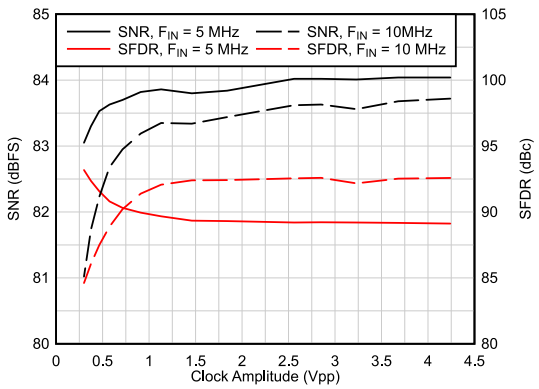
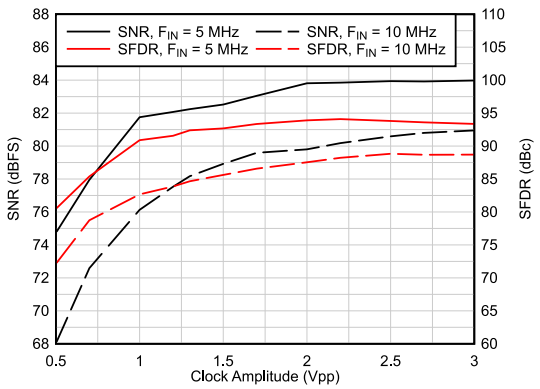
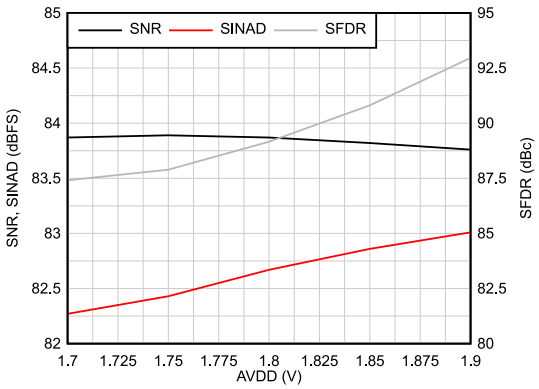


図 5-15. AC Performance vs Clock Amplitude



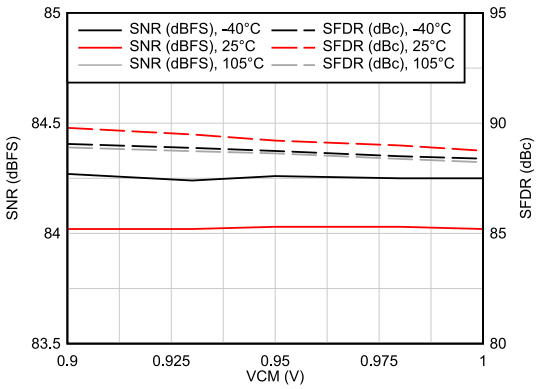
Single ended clock input

図 5-16. AC Performance vs Clock Amplitude



F_{IN} = 5MHz

図 5-17. AC Performance vs AVDD



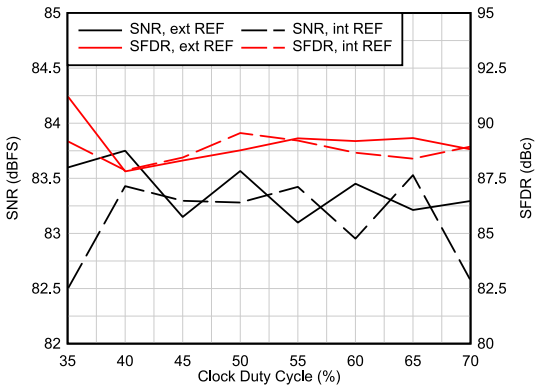
F_{IN} = 5MHz

図 5-18. AC Performance vs VCM vs Temperature

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5.9 Typical Characteristics - ADC3683 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



F_{IN} = 5MHz

図 5-19. AC Performance vs Clock Duty Cycle

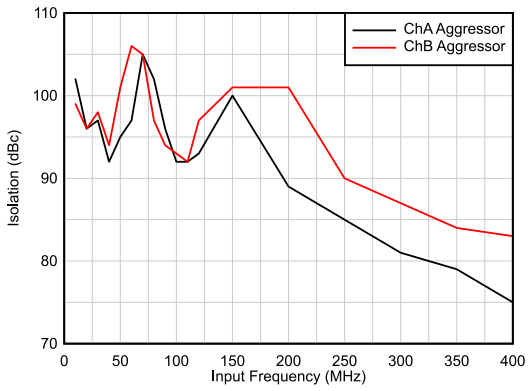
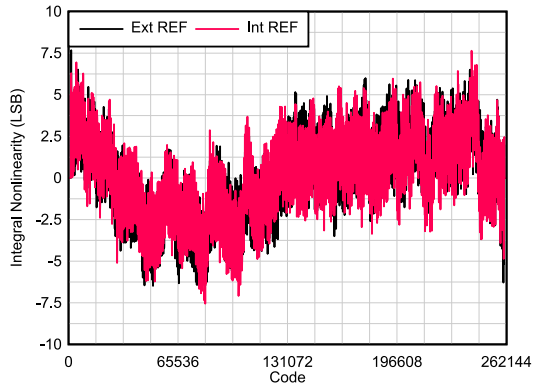
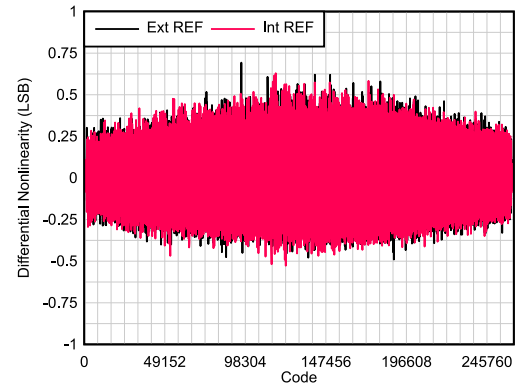


図 5-20. Isolation vs Input Frequency



F_{IN} = 5MHz

図 5-21. INL vs Code



F_{IN} = 5MHz

図 5-22. DNL vs Code

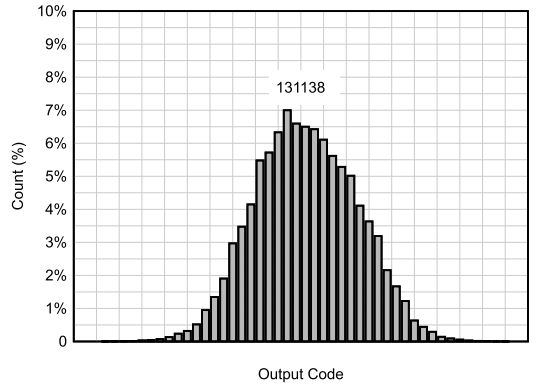
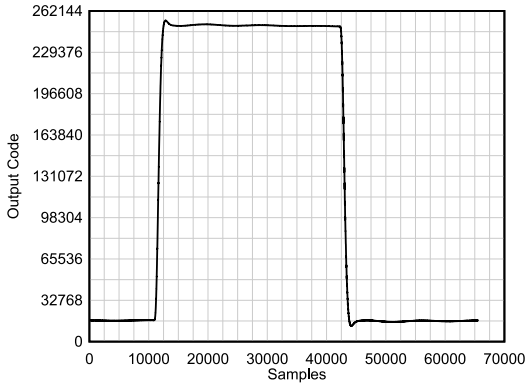


図 5-23. DC Offset Histogram



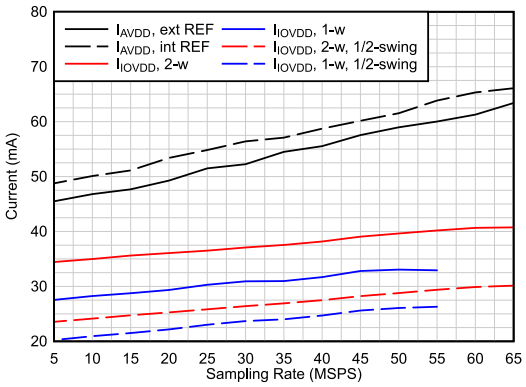
F_{IN} = 1MHz

図 5-24. Pulse Response

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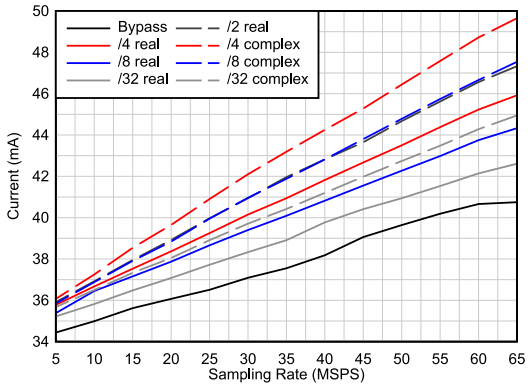
5.9 Typical Characteristics - ADC3683 (continued)

Typical values at T_A = 25 °C, ADC sampling rate = 65MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



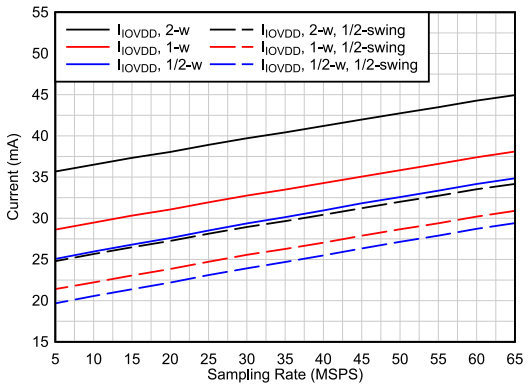
F_{IN} = 5MHz, DDC Bypass

図 5-25. Current vs Sampling Rate



F_{IN} = 5MHz, 2-wire

図 5-26. I_{IOVDD} Current vs Decimation



F_{IN} = 5MHz, Complex Decimation by 32

図 5-27. I_{IOVDD} Current vs Output Interface

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6 Parameter Measurement Information

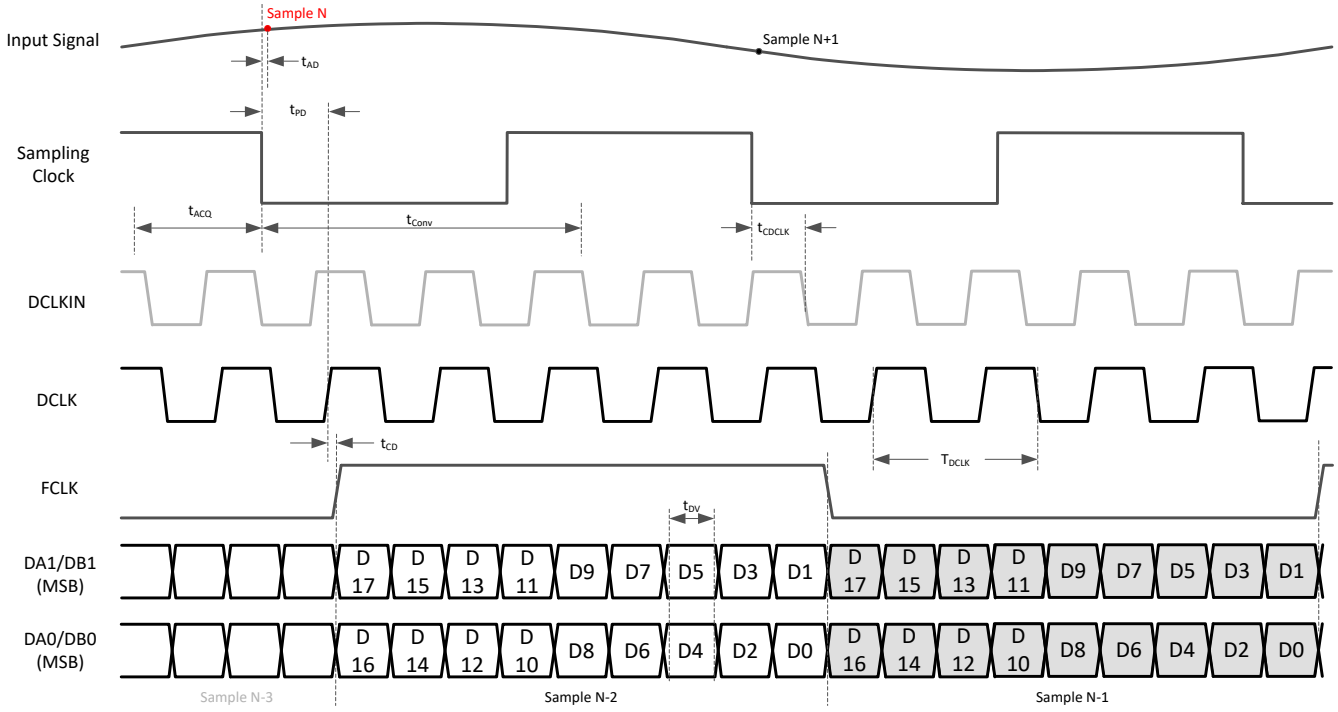


図 6-1. Timing diagram: 2-wire SLVDS (default output bit mapping)

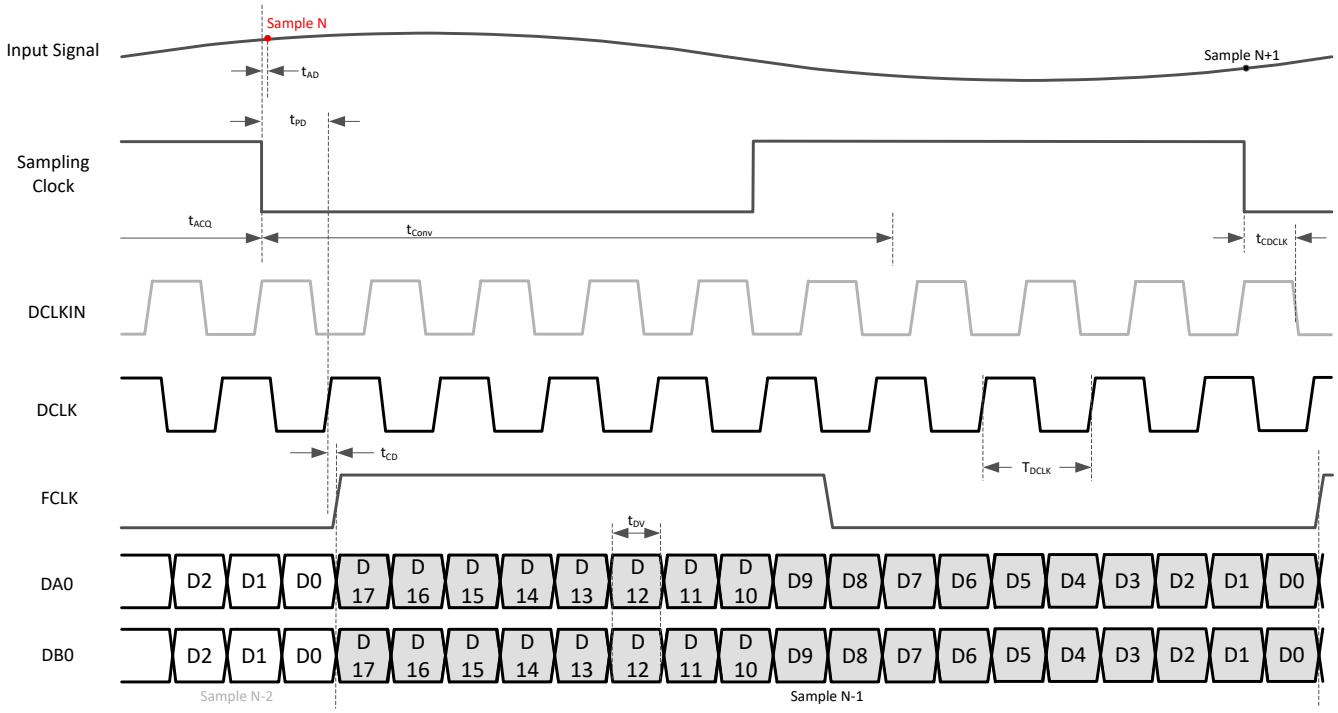


図 6-2. Timing diagram: 1-wire SLVDS (default output bit mapping)

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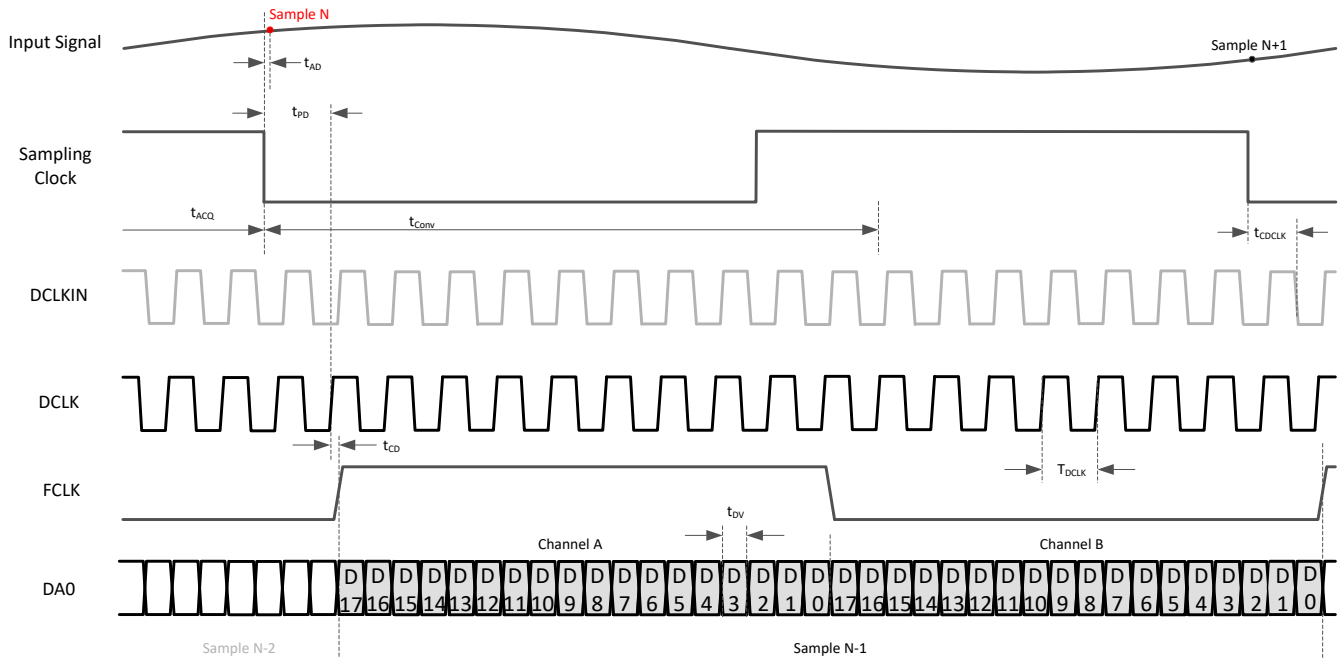


図 6-3. Timing diagram: 1/2-wire SLVDS (default output bit mapping)

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7 Detailed Description

7.1 Overview

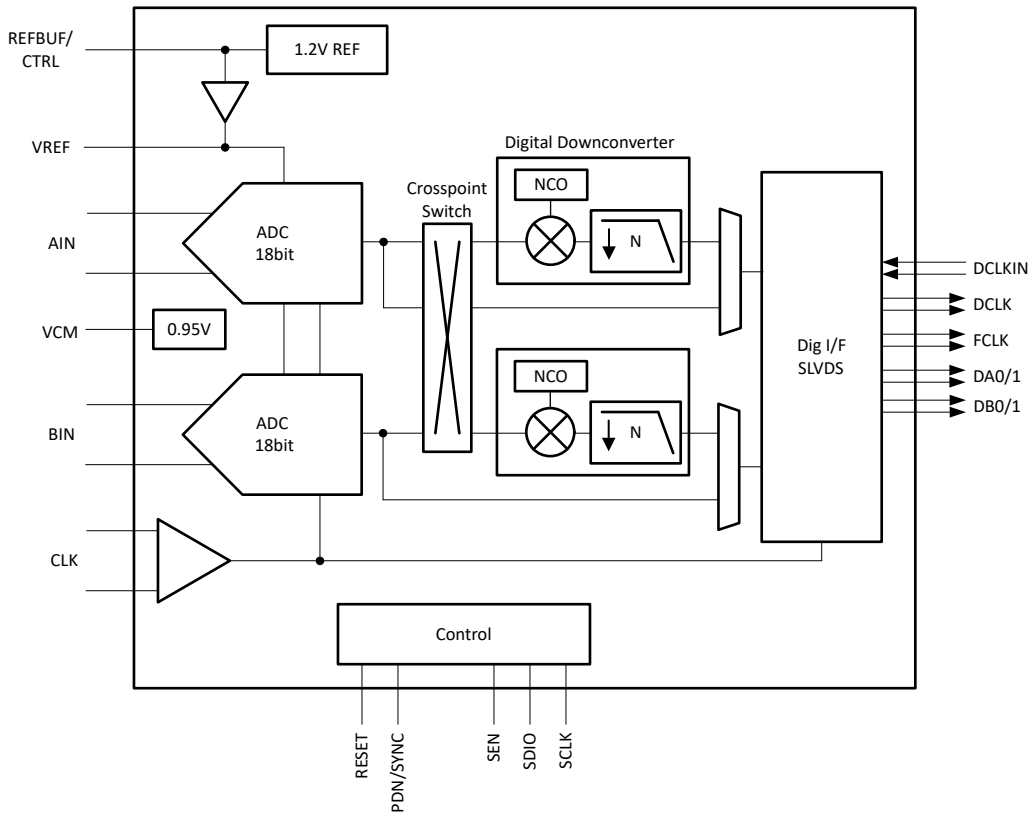
The ADC3683-xEP is a low noise, ultra-low power 18-bit high-speed dual channel ADC family supporting sampling rates up to 65 MSPS. The device offers DC precision together with IF sampling support. Making the device designed for a wide range of applications. The ADC3683-xEP is equipped with an internal reference option but it also supports the use of an external, high precision 1.6V voltage reference or an external 1.2V reference which is buffered and gained up internally. Because of the inherent low latency architecture, the digital output result is available after only one or two clock cycles depending on the digital output interface.

An optional programmable digital down converter enables external anti-alias filter relaxation as well as output data rate reduction. The digital filter provides a 32-bit programmable NCO and supports both real or complex decimation.

The ADC3683-xEP uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects. The device supports a two-lane (2-wire), a one-lane (1-wire) and a half-lane (1/2-wire) option. The ADC3683-xEP includes a digital output formatter which supports output resolutions from 14 to 20-bit.

The device features and control options are set up either through pin configurations or via SPI register writes.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The analog inputs of ADC3683-xEP are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common mode voltage of 0.95V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The equivalent input network diagram is shown in 図 7-1. All four sampling switches, on-resistance shown in red are in same position (open or closed) simultaneously.

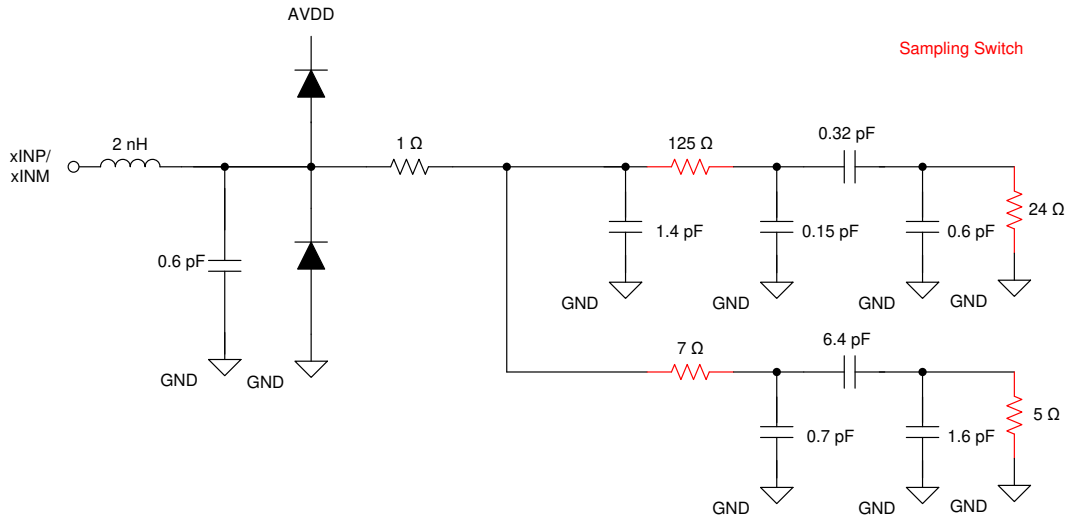


図 7-1. Equivalent input network

7.3.1.1 Analog Input Bandwidth

図 7-2 shows the analog full power input bandwidth of the ADC3683-xEP with a 50Ω differential termination. The −3dB bandwidth is approximately 900MHz and the useful input bandwidth with good AC performance is approximately 120MHz.

The equivalent differential input resistance R_{IN} and input capacitance C_{IN} vs frequency are shown in 図 7-3.

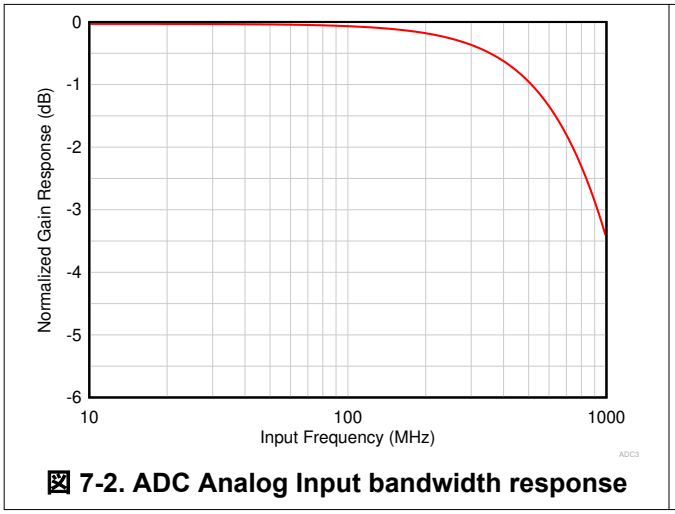


図 7-2. ADC Analog Input bandwidth response

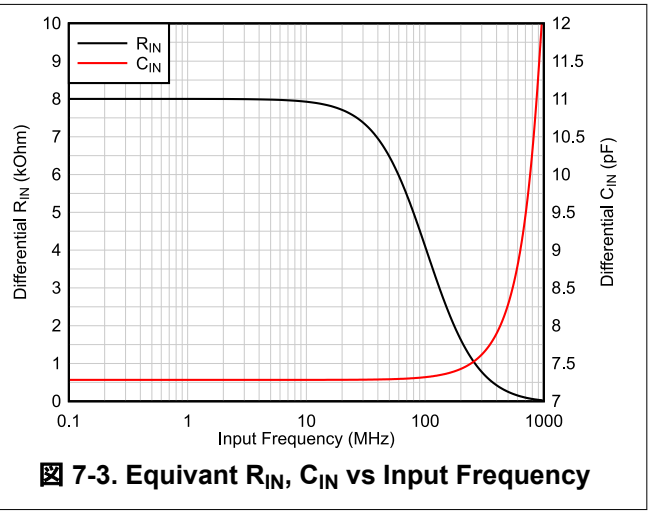


図 7-3. Equivant R_{IN}, C_{IN} vs Input Frequency

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7.3.1.2 Analog Front End Design

The ADC3683-xEP is an unbuffered ADC and thus a passive kick-back filter is recommended to absorb the glitch from the sampling operation. Depending on if the input is driven by a balun or a differential amplifier with low output impedance, a termination network is needed. Additionally, a passive DC bias circuit is needed in AC-coupled applications which is combined with the termination network.

7.3.1.2.1 Sampling Glitch Filter Design

The front end sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency; therefore, the following filter designs are recommended for different input frequency ranges as shown in 図 7-4 and 図 7-5 (assuming a 50Ω source impedance).

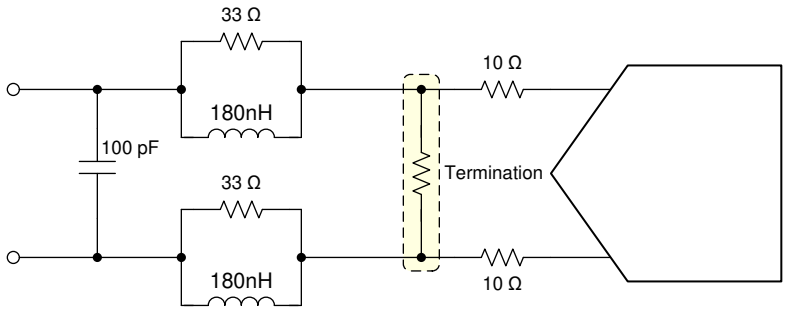


図 7-4. Sampling glitch filter example for input frequencies from DC to 30MHz

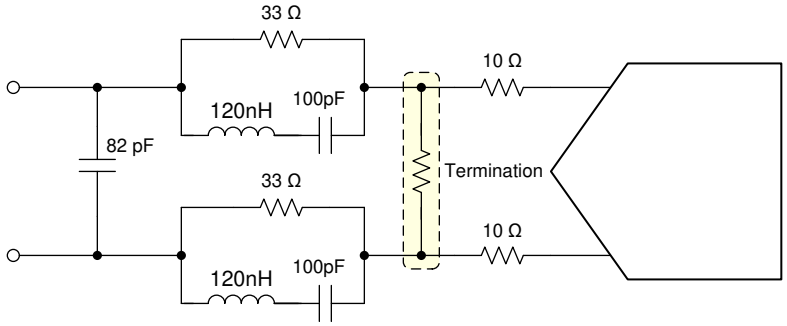


図 7-5. Sampling glitch filter example for input frequencies from 30 to 70MHz

7.3.1.2.2 Analog Input Termination and DC Bias

Depending on the input drive circuitry, a termination network and/or DC biasing needs to be provided.

7.3.1.2.2.1 AC-Coupling

The ADC3683-xEP requires external DC bias using the common mode output voltage (VCM) of the ADC together with the termination network as shown in 図 7-6. The termination is located within the glitch filter network. When using a balun on the input, the termination impedance has to be adjusted to account for the turns ratio of the transformer. When using an amplifier, the termination impedance is adjusted to optimize the amplifier performance.

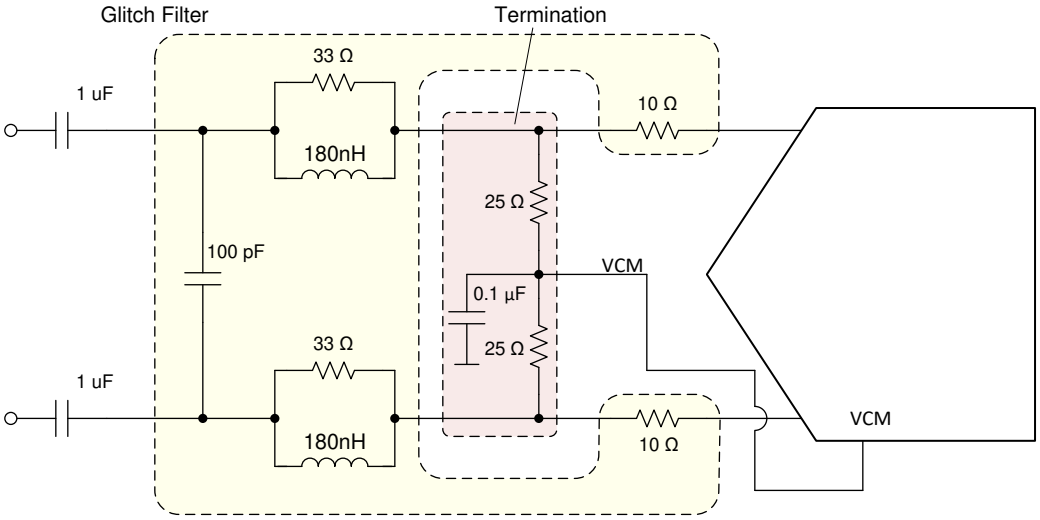


図 7-6. AC-Coupling: termination network provides DC bias (glitch filter example for DC - 30 MHz)

7.3.1.2.2.2 DC-Coupling

In DC coupled applications, the DC bias needs to be provided from the fully differential amplifier (FDA) using VCM output of the ADC as shown in 図 7-7. The glitch filter, in this case, is located between the anti-alias filter and the ADC. No termination is needed if the amplifier is located close to the ADC, or if the termination is part of the anti-alias filter.

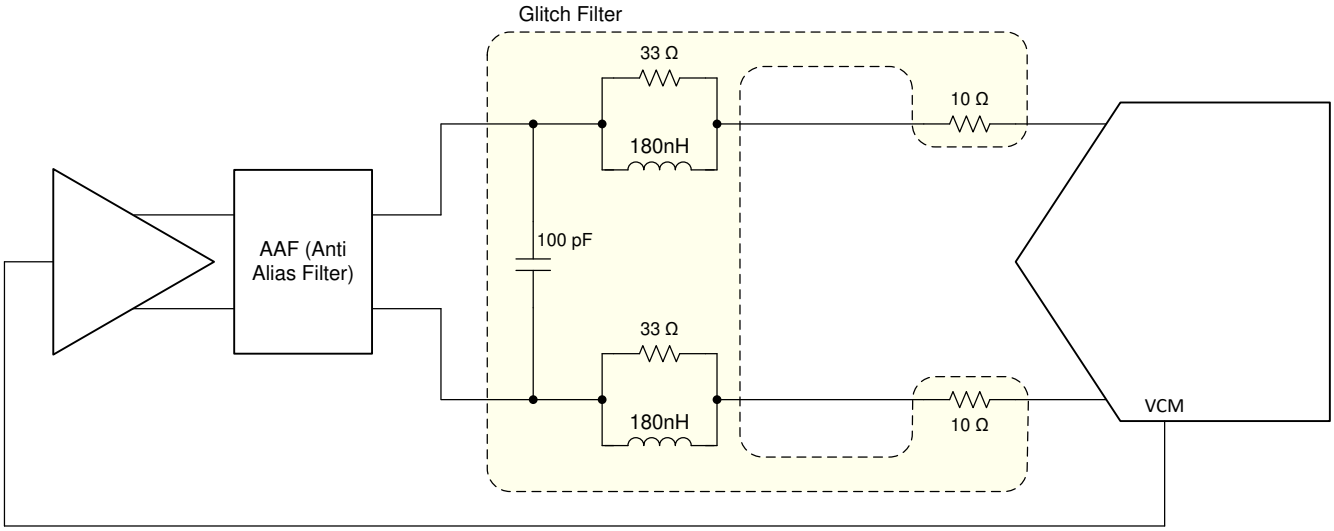


図 7-7. DC-Coupling: DC bias provided by FDA (glitch filter example for DC - 30MHz)

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7.3.1.3 Auto-Zero Feature

The ADC3683-xEP includes an internal auto-zero front end amplifier circuit which improves the 1/f flicker noise. The auto-zero feature is enabled using SPI register writes for the device (register 0x11, D0). The 4M point FFTs below shows the autozero feature enabled vs disabled.

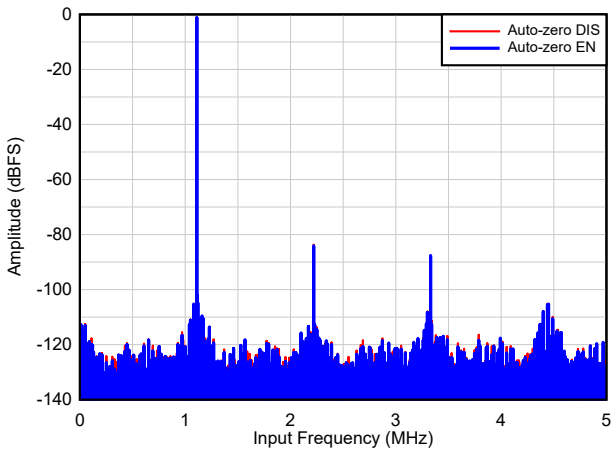


図 7-8. F_S = 10MSPS, F_{IN} = 1.1MHz

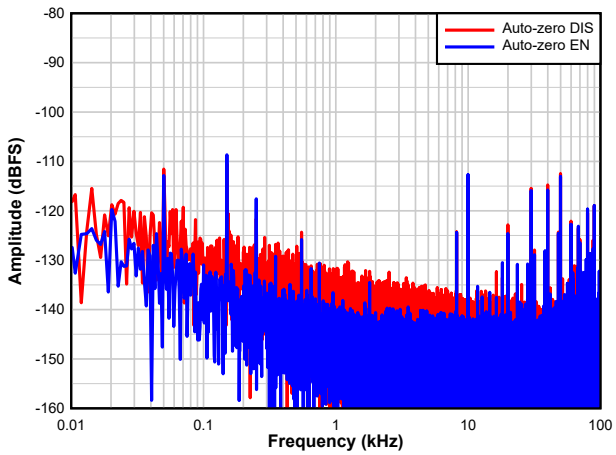


図 7-9. F_S = 10MSPS, F_{IN} = 1.1MHz

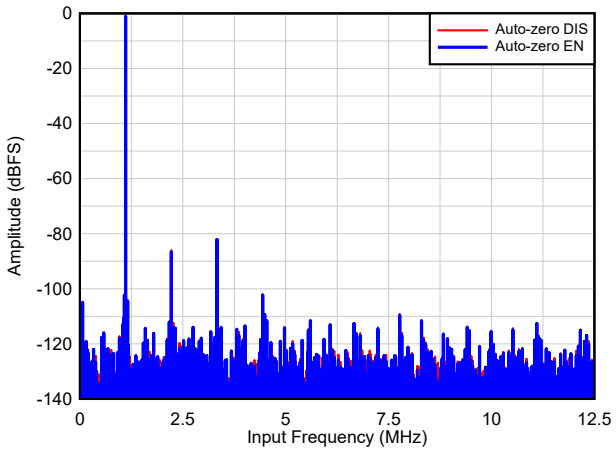


図 7-10. F_S = 25MSPS, F_{IN} = 1.1MHz

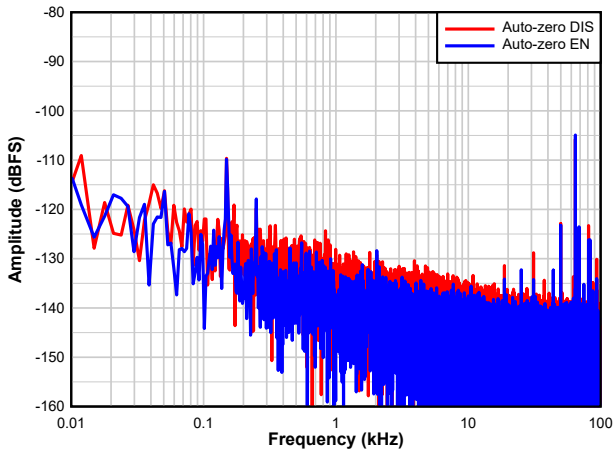


図 7-11. F_S = 25MSPS, F_{IN} = 1.1MHz

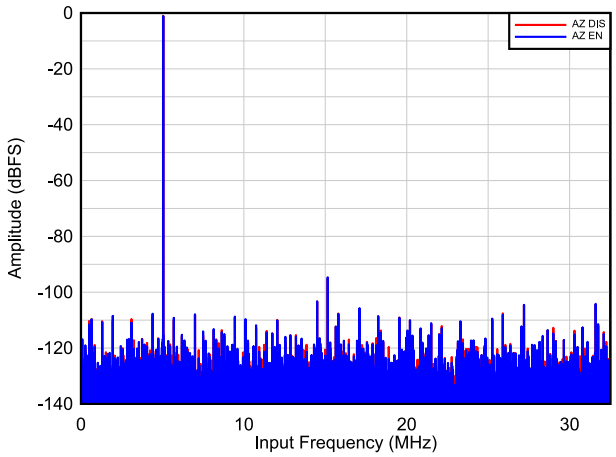


図 7-12. F_S = 65MSPS, F_{IN} = 5MHz

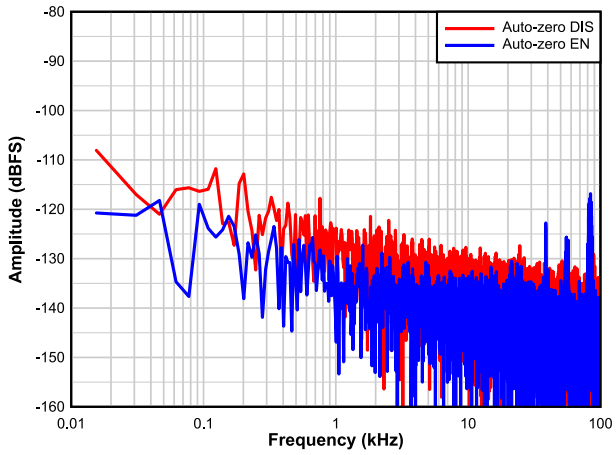


図 7-13. F_S = 65MSPS, F_{IN} = 5MHz

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7.3.2 Clock Input

To maximize the ADC SNR performance, the external sampling clock should be low jitter and differential signaling with a high slew rate. This is especially important in IF sampling applications (図 7-14 and 図 7-15). For less jitter sensitive applications, the device provides the option to operate with single ended signaling which saves additional power consumption.

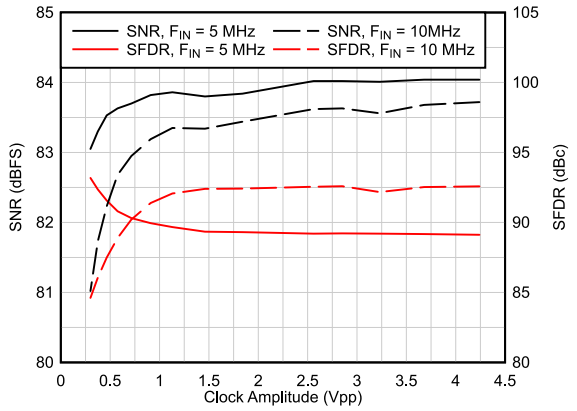


図 7-14. AC Performance vs Clock Amplitude (Differential Clock Input)

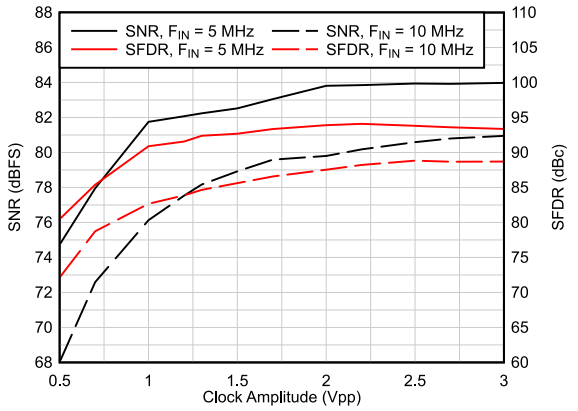


図 7-15. AC Performance vs Clock Amplitude (Single Ended Clock Input)

7.3.2.1 Single Ended vs Differential Clock Input

The ADC3683-xEP is operated using a differential or a single ended clock input where the single ended clock consumes less power consumption. However, clock amplitude impacts the ADC aperture jitter and consequently the SNR. For maximum SNR performance, a large clock signal with fast slew rates needs to be provided.

- Differential Clock Input: The clock input is AC coupled externally. The device provides internal bias.
- Single Ended Clock Input: This mode needs to be configured using SPI register (0x0E, D2 and D0) or with the REFBUF/CTRL pin. In this mode, there is no internal clock biasing and thus the clock input needs to be DC coupled around a 0.9V center. The unused input needs to be AC coupled to ground.

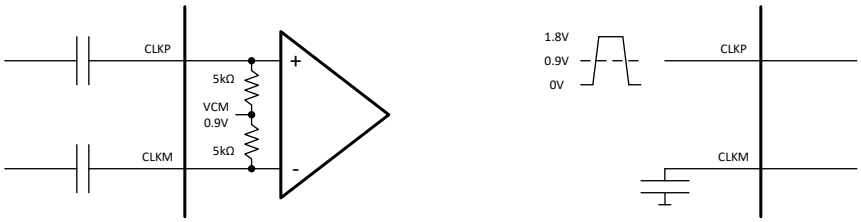


図 7-16. External and internal connection using differential (left) and single ended (right) clock input

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7.3.2.2 Signal Acquisition Time Adjust

The ADC3683-xEP includes a register (DLL PDN (0x11, D2) which increases the signal acquisition time window for clock rates below 40MSPS from 25% to 50% of the clock period. Increasing the sampling time provides a longer time for the driving amplifier to settle out the signal which can improve the SNR performance of the system. This register is only be used at or below 40MSPS. When powering down the DLL, the acquisition time tracks the clock duty cycle (50% is recommended).

表 7-1. Acquisition time vs DLL PDN setting

SAMPLING CLOCK F_S (MSPS)	DLL PDN (0x11, D2)	ACQUISITION TIME (t_{ACQ})
65	0	T_S / 4
≤ 40	1	T_S / 2

7.3.3 Voltage Reference

The ADC3683-xEP provides three different options for supplying the voltage reference to the ADC. Connect an external 1.6V reference is directly to the VREF input. A voltage 1.2V reference is connected to the REFBUF/CTRL input using the internal gain buffer or the internal 1.2V reference is enabled to generate a 1.6V reference voltage. For best performance, the reference noise should be filtered by connecting a 10µF and a 0.1µF ceramic bypass capacitor to the VREF pin. The internal reference circuitry of the ADC3683-xEP is shown in 図 7-17.

注

The voltage reference mode is selected using SPI writes or by using the REFBUF/CTRL pin (default) as a control pin (セクション 7.5.1). If the REFBUF/CTRL pin is not used for configuration, the pin must be connected to AVDD (even though the REFBUF/CTRL pin has a weak internal pullup to AVDD). The voltage reference option has to be selected using the SPI interface.

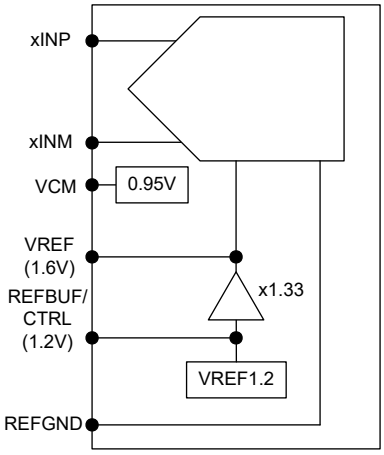


図 7-17. Different voltage reference options for ADC3683-xEP

7.3.3.1 Internal voltage reference

Generate the 1.6V reference for the ADC internal using the on-chip 1.2V bandgap reference along with the internal gain buffer. A 10µF and a 0.1µF ceramic bypass capacitor (C_{VREF}) is connected between the VREF and REFGND pins as close to the pins as possible.

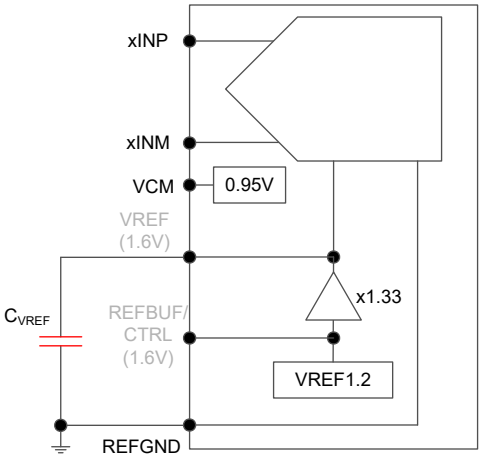


図 7-18. Internal reference

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7.3.3.2 External voltage reference (VREF)

For highest accuracy and lowest temperature drift, the VREF input is connected directly to an external 1.6V reference. A 10µF and a 0.1µF ceramic bypass capacitor (C_{VREF}) connected between the VREF and REFGND pins and placed as close to the pins as possible is recommended. The load current from the external reference is about 1mA.

注

The internal reference is also used for other functions inside the device; therefore, the reference amplifier should only be powered down in power down state but not during normal operation.

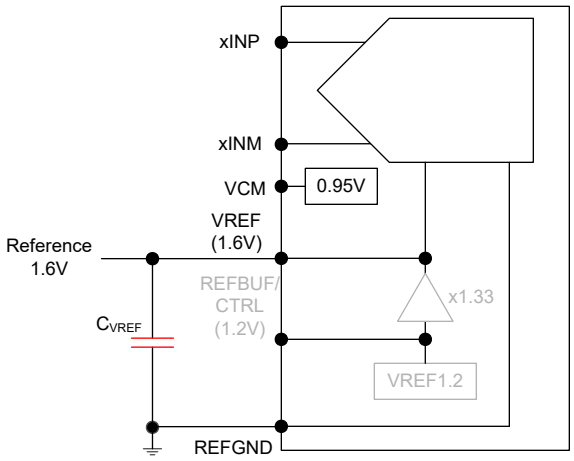


図 7-19. External 1.6V reference

7.3.3.3 External voltage reference with internal buffer (REFBUF/CTRL)

The ADC3683-xEP is equipped with an on-chip reference buffer that also includes gain to generate the 1.6V reference voltage from an external 1.2V reference. A 10µF and a 0.1µF ceramic bypass capacitor (C_{VREF}) between the VREF and REFGND pins and a 10µF and a 0.1µF ceramic bypass capacitor between the REFBUF/CTRL and REFGND pins are recommended. Both capacitors should be placed as close to the pins as possible. The load current from the external reference is less than 100µA.

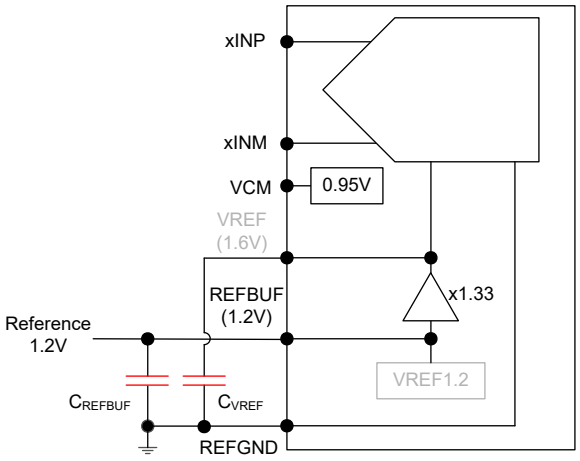


図 7-20. External 1.2V reference using internal reference buffer

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7.3.4 Digital Down Converter

The ADC3683-xEP includes an optional on-chip digital down conversion (DDC) decimation filter that is enabled via SPI register settings. Supporting complex decimation by 2, 4, 8, 16 and 32 using a digital mixer and a 32-bit numerically controlled oscillator (NCO) as shown in 図 7-21.

Supporting a mode with real decimation where the complex mixer is bypassed (NCO should be set to 0 for lowest power consumption) and the digital filter acts as a low pass filter.

Internally, the decimation filter calculations are performed with a 20-bit resolution to avoid any SNR degradation due to quantization noise limitation. The セクション 7.3.5.1 truncates to the selected resolution prior to outputting the data on the digital interface.

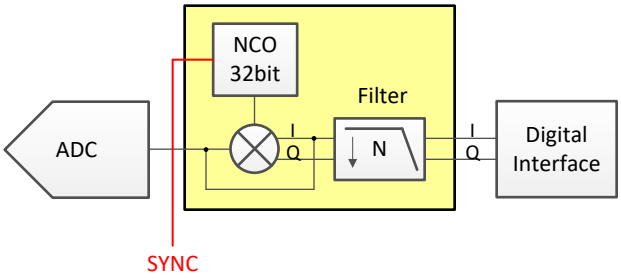


図 7-21. Internal digital decimation filter

7.3.4.1 DDC MUX

The ADC3683-xEP contains a MUX in front of the digital decimation filter which allows ADC ChA to be connected to DDC ChB. This feature is enabled and controlled using the SPI interface. Subsequently the output interface corresponds to the DDC channel A and B.

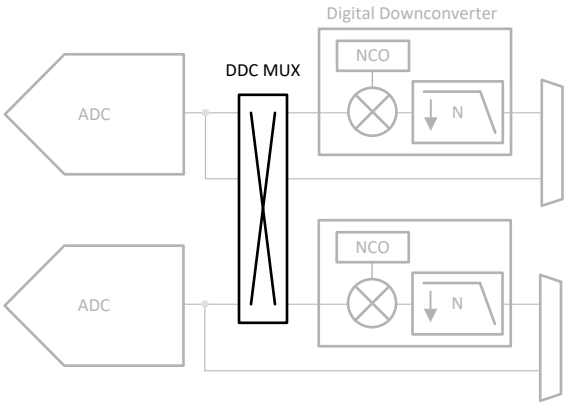


図 7-22. DDC MUX

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7.3.4.2 Digital Filter Operation

The complex decimation operation is illustrated with an example in 図 7-23. First the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left. Next a digital filter is applied (centered around 0 Hz) and the output data rate is decimated by 8 complex. In this example, the output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$. During the complex mixing the spectrum (signal and noise) is split into real and complex parts and thus the amplitude is reduced by 6dB. To compensate this loss, there is a 6dB digital gain option in the decimation filter block that is enabled via SPI write.

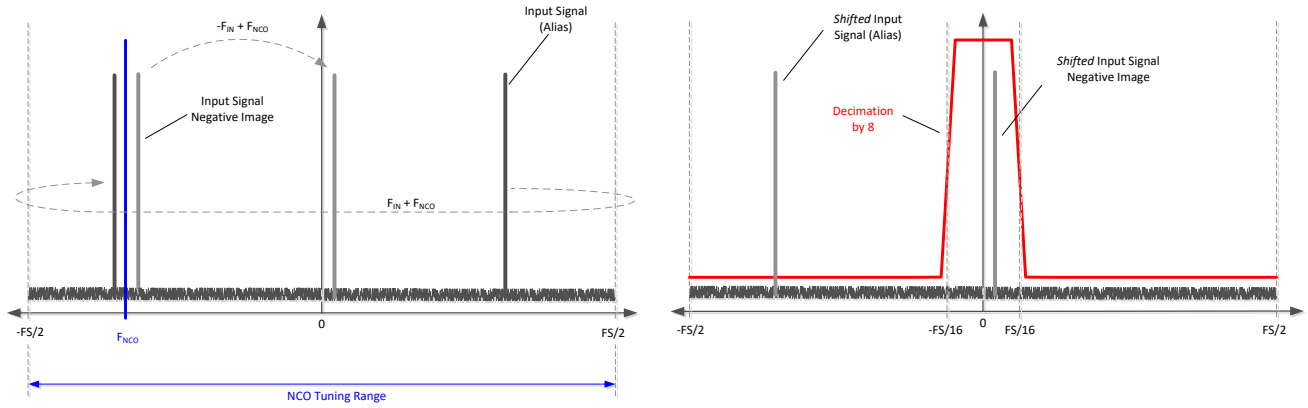


図 7-23. Complex decimation illustration

The real decimation operation is illustrated with an example in 図 7-24. There is no frequency shift happening and only the real portion of the complex digital filter is exercised. The output data rate is decimated - a decimation of 8 results in an output data rate $F_{S,OUT} = F_S/8$ with a Nyquist zone of $F_S/16$.

During the real mixing the spectrum (signal and noise) amplitude is reduced by 3dB. To compensate this loss, there is a 3dB digital gain option in the decimation filter block that is enabled via SPI write.

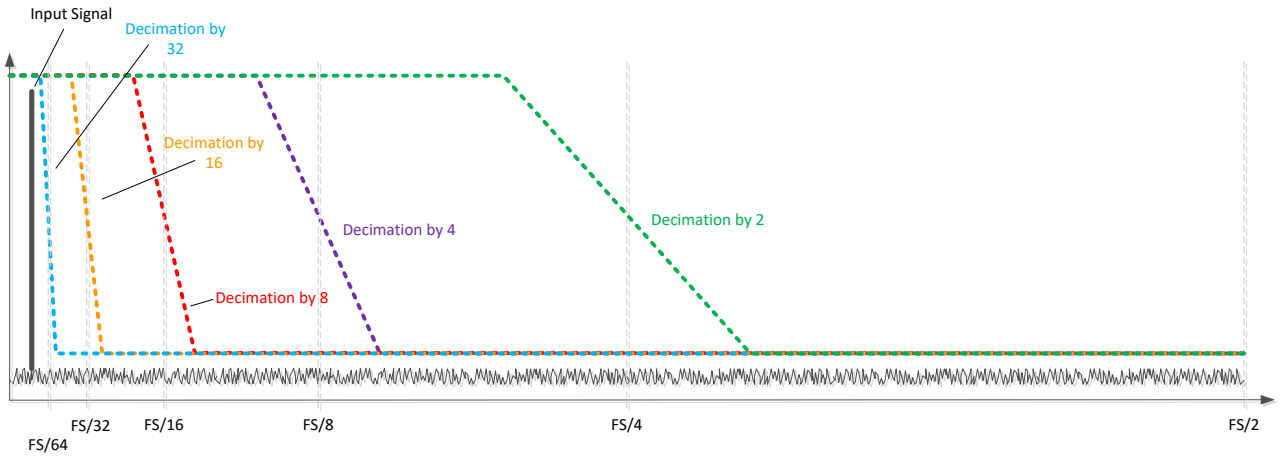


図 7-24. Real decimation illustration

7.3.4.3 FS/4 Mixing with Real Output

In this mode, the output after complex decimation gets mixed with FS/4 (FS = output data rate in this case). Instead of a complex output with the input signal centered around 0Hz, the output is transmitted as a real output at twice the data rate and the signal is centered around FS/4 (Fout/4) as illustrated in 図 7-25.

In this example, complex decimation by 8 is used. The output data is transmitted as a real output with an output rate of Fout = FS'/4 (FS' = ADC sampling rate). The input signal is now centered around FS/4 (Fout/4) or FS'/16.

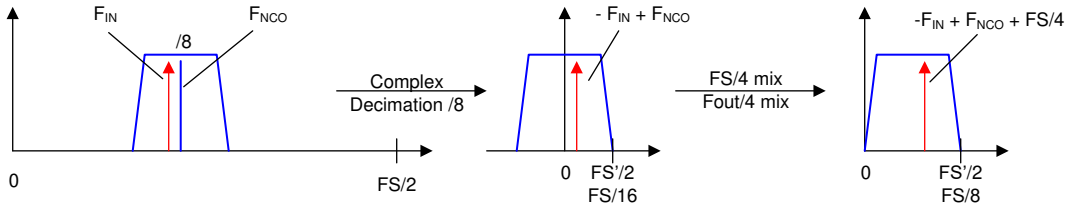


図 7-25. FS/4 Mixing with real output

7.3.4.4 Numerically Controlled Oscillator (NCO) and Digital Mixer

The decimation block is equipped with a 32-bit NCO and a digital mixer to fine tune the frequency placement prior to the digital filtering. The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \quad (1)$$

where: frequency (ω) is specified as a signed number by the 32-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$. The NCO frequency is tuned from $–F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, the MIXER RESTART register bit or SYNC pin has to be toggled for the new frequency to get active. Additionally, the ADC3683-xEP provides the option via SPI to invert the mixer phase.

The NCO frequency setting is set by the 32-bit register value given and calculated as:

$$\text{NCO frequency} = 0 \text{ to } + F_S/2\text{: NCO} = f_{NCO} \times 2^{32} / F_S \quad (2)$$

$$\text{NCO frequency} = -F_S/2 \text{ to } 0\text{: NCO} = (f_{NCO} + F_S) \times 2^{32} / F_S \quad (3)$$

where:

- NCO = NCO register setting (decimal value)
- f_{NCO} = Desired NCO frequency (MHz)
- F_S = ADC sampling rate (MSPS)

The NCO programming is further illustrated with this example:

- ADC sampling rate F_S = 65MSPS
- Input signal f_{IN} = 10MHz
- Desired output frequency f_{OUT} = 0MHz

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For this example, there are actually four ways to program the NCO and achieve the desired output frequency as shown in 表 7-2.

表 7-2. NCO value calculations example

Alias or negative image	f_{NCO}	NCO Value	Mixer Phase	Frequency translation for f_{OUT}
f_{IN} = –10MHz	f_{NCO} = 10MHz	660764199	as is	$f_{OUT} = f_{IN} + f_{NCO}$ = –10MHz +10MHz = 0MHz
f_{IN} = 10MHz	f_{NCO} = –10MHz	3634203097		$f_{OUT} = f_{IN} + f_{NCO}$ = 10MHz + (–10MHz) = 0MHz
f_{IN} = 10MHz	f_{NCO} = 10MHz	660764199	inverted	$f_{OUT} = f_{IN} – f_{NCO}$ = 10MHz – 10MHz = 0MHz
f_{IN} = –10MHz	f_{NCO} = –10MHz	3634203097		$f_{OUT} = f_{IN} – f_{NCO}$ = –10MHz – (–10MHz) = 0MHz

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7.3.4.5 Decimation Filter

The ADC3683-xEP supports complex decimation by 2, 4, 8, 16 and 32 with a stopband rejection of at least 85dB and a pass-band bandwidth of approximately 80%. 表 7-3 gives an overview of the pass-band bandwidth of the different decimation settings with respect to ADC sampling rate F_S. In real decimation mode, the output bandwidth is half of the complex bandwidth.

表 7-3. Decimation Filter Summary and Maximum Available Output Bandwidth

REAL/COMPLEX DECIMATION	DECIMATION SETTING N	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F_S = 65 MSPS)	OUTPUT BANDWIDTH (F_S = 65 MSPS)
Complex	2	F_S / 2 complex	0.8 × F_S / 2	32.5MSPS complex	26MHz
	4	F_S / 4 complex	0.8 × F_S / 4	16.25MSPS complex	13MHz
	8	F_S / 8 complex	0.8 × F_S / 8	8.125MSPS complex	6.5MHz
	16	F_S / 16 complex	0.8 × F_S / 16	4.0625MSPS complex	3.25MHz
	32	F_S / 32 complex	0.8 × F_S / 32	2.03125MSPS complex	1.625MHz
Real	2	F_S / 2 real	0.4 × F_S / 2	32.5MSPS	13MHz
	4	F_S / 4 real	0.4 × F_S / 4	16.25MSPS	6.5MHz
	8	F_S / 8 real	0.4 × F_S / 8	8.125MSPS	3.25MHz
	16	F_S / 16 real	0.4 × F_S / 16	4.0625MSPS	1.625MHz
	32	F_S / 32 real	0.4 × F_S / 32	2.03125MSPS	0.8125MHz

The decimation filter responses are normalized to the ADC sampling clock frequency F_S and illustrated in 図 7-27 to 図 7-36. They are interpreted as follows:

Each figure contains the filter pass-band, transition band(s) and alias or stop-band(s) as shown in 図 7-26. The x-axis shows the offset frequency (after the NCO frequency shift) normalized to the ADC sampling rate F_S.

For example, in the divide-by-4 complex setup, the output data rate is F_S / 4 complex with a Nyquist zone of F_S / 8 or 0.125 × F_S. The transition band (colored in blue) is centered around 0.125 × F_S and the alias transition band is centered at 0.375 × F_S. The stop-bands (colored in red), which alias on top of the pass-band, are centered at 0.25 × F_S and 0.5 × F_S. The stop-band attenuation is greater than 85dB.

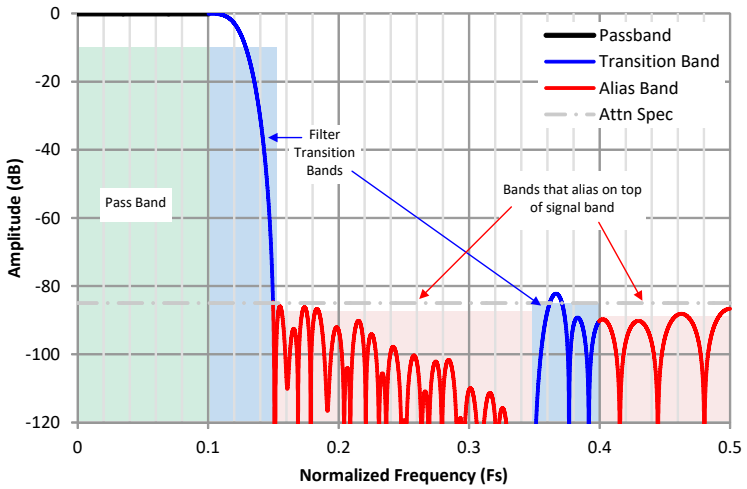


図 7-26. Interpretation of the Decimation Filter Plots

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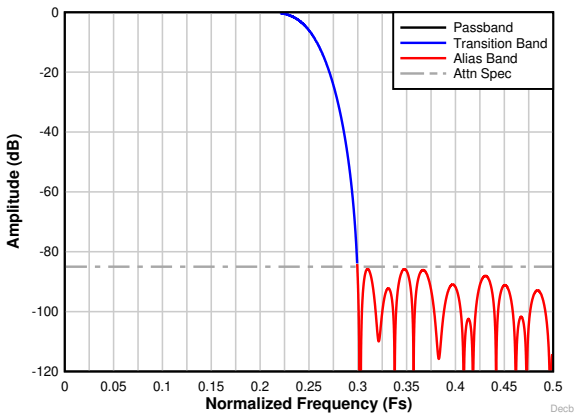


図 7-27. Decimation by 2 complex frequency response

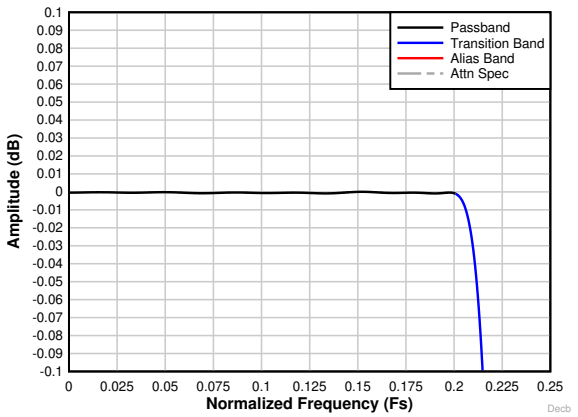


図 7-28. Decimation by 2 complex passband ripple response

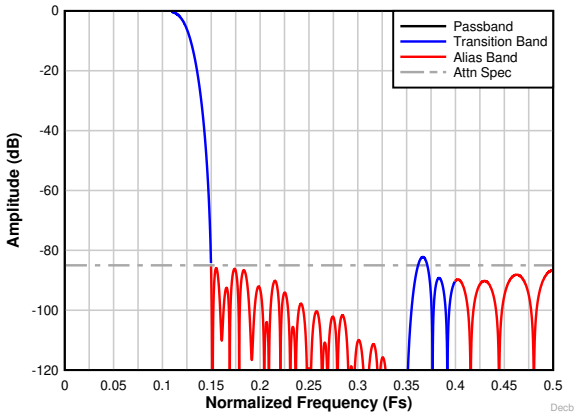


図 7-29. Decimation by 4complex frequency response

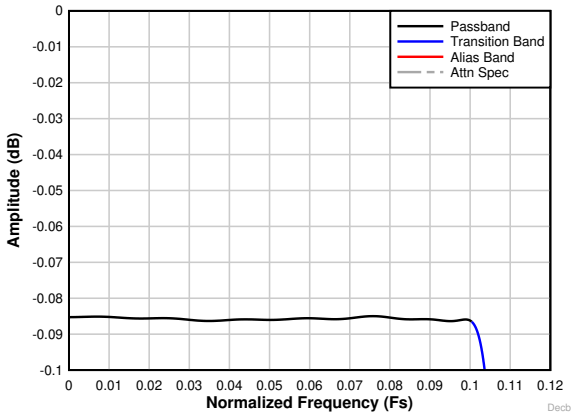


図 7-30. Decimation by 4 complex passband ripple response

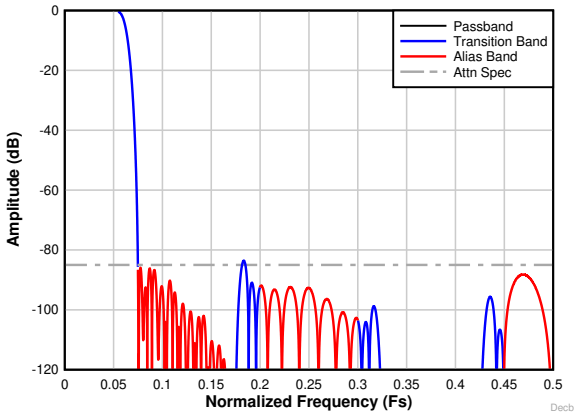


図 7-31. Decimation by 8 complex frequency response

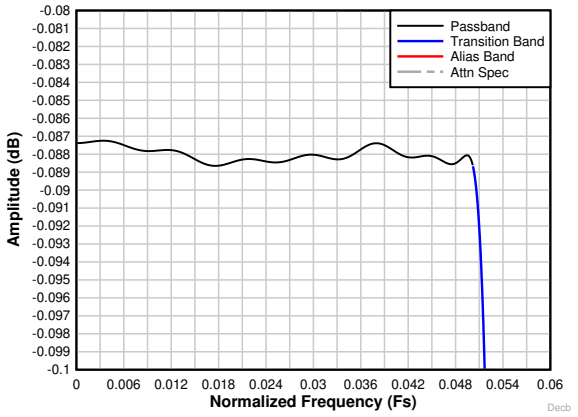


図 7-32. Decimation by 8 complex passband ripple response

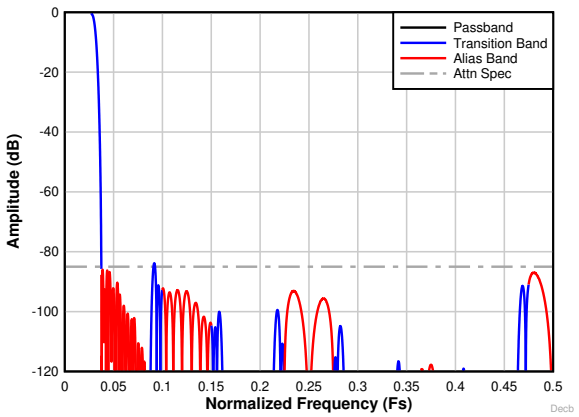


図 7-33. Decimation by 16 complex frequency response

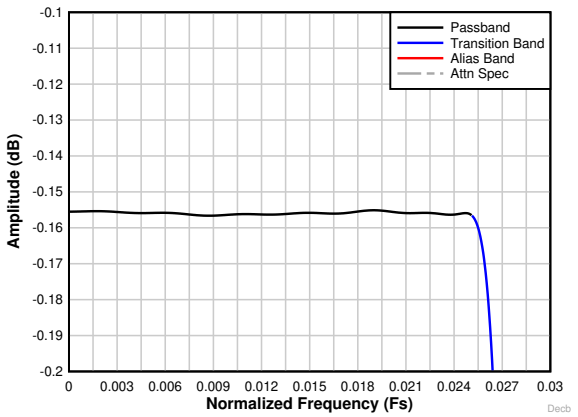


図 7-34. Decimation by 16 complex passband ripple response

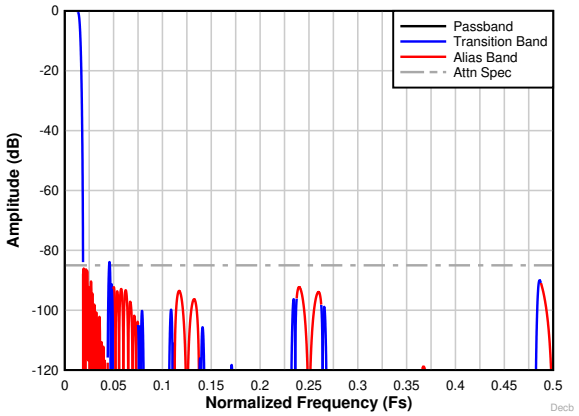


図 7-35. Decimation by 32 complex frequency response

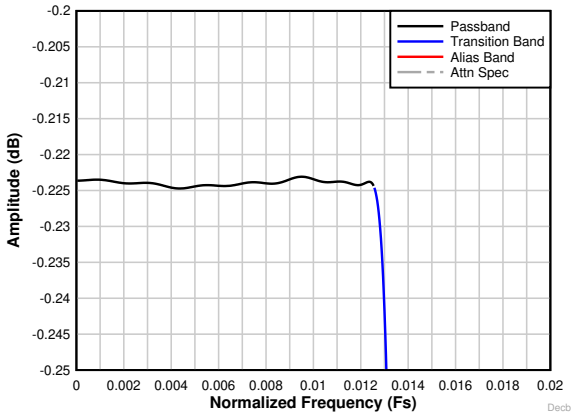


図 7-36. Decimation by 32 complex passband ripple response

7.3.4.6 SYNC

The PDN/SYNC pin is used to synchronize multiple devices using an external SYNC signal. The PDN/SYNC pin is configured through SPI (SYNC EN bit) from power down to synchronization functionality, and is latched in by the rising edge of the sampling clock as shown in 図 7-37.

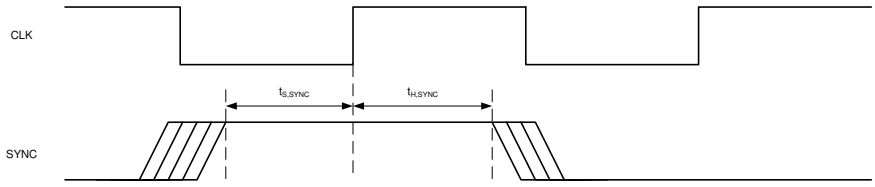


図 7-37. External SYNC timing diagram

The synchronization signal is only required when using the decimation filter - either using the SPI SYNC register or the PDN/SYNC pin. Resetting the internal clock dividers used in the decimation filter, and aligning the internal clocks as well as I and Q data within the same sample. If no SYNC signal is given, the internal clock dividers is not be synchronized, which can lead to a fractional delay across different devices. The SYNC signal also resets the NCO phase and loads the new NCO frequency (same as the MIXER RESTART bit).

When trying to resynchronize during operation, the SYNC toggle occurs at 64*K clock cycles, where K is an integer. This provides the phase continuity of the clock divider.

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7.3.4.7 Output Formatting with Decimation

When using decimation, the digital output data is formatted as shown in 図 7-38 (complex decimation) and 図 7-39 (real decimation).The output format is illustrated for 18-bit output resolution.

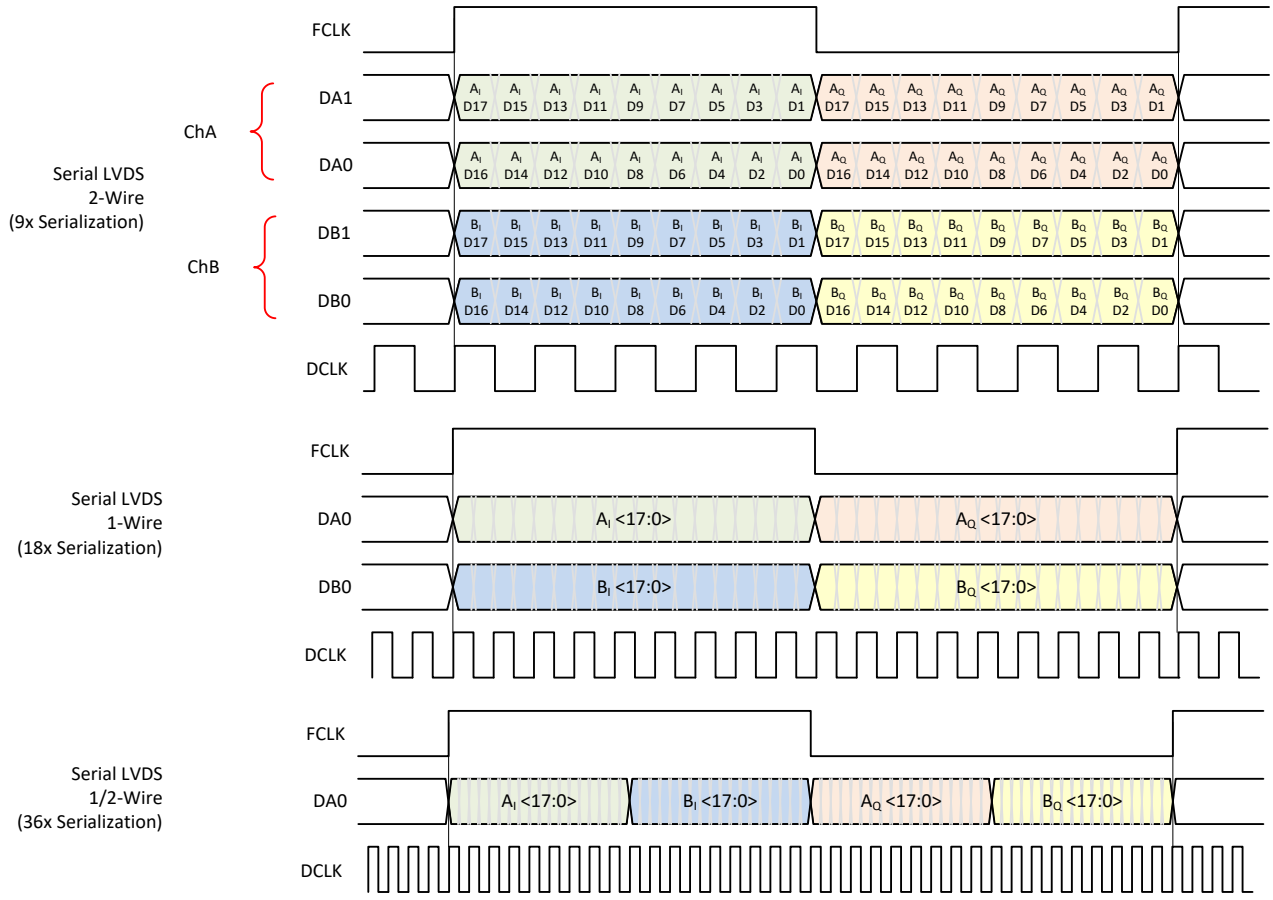


図 7-38. Output Data Format in Complex Decimation (18-bit Output Resolution)

表 7-4 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and complex decimation setting (N).

Tthe table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 18-bit output resolution and complex decimation by 4.

表 7-4. Serial LVDS Lane Rate Examples with Complex Decimation and 18-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DA/B0,1
N	F_S	R	L	F_S / N	[DA/B0,1] / 2	F_S x 2 x R / L / N
4	65MSPS	18	2	16.25MHz	146.25 MHz	292.5 MHz
			1		292.5 MHz	585 MHz
	55MSPS		1/2	13.75MHz	495 MHz	990 MHz

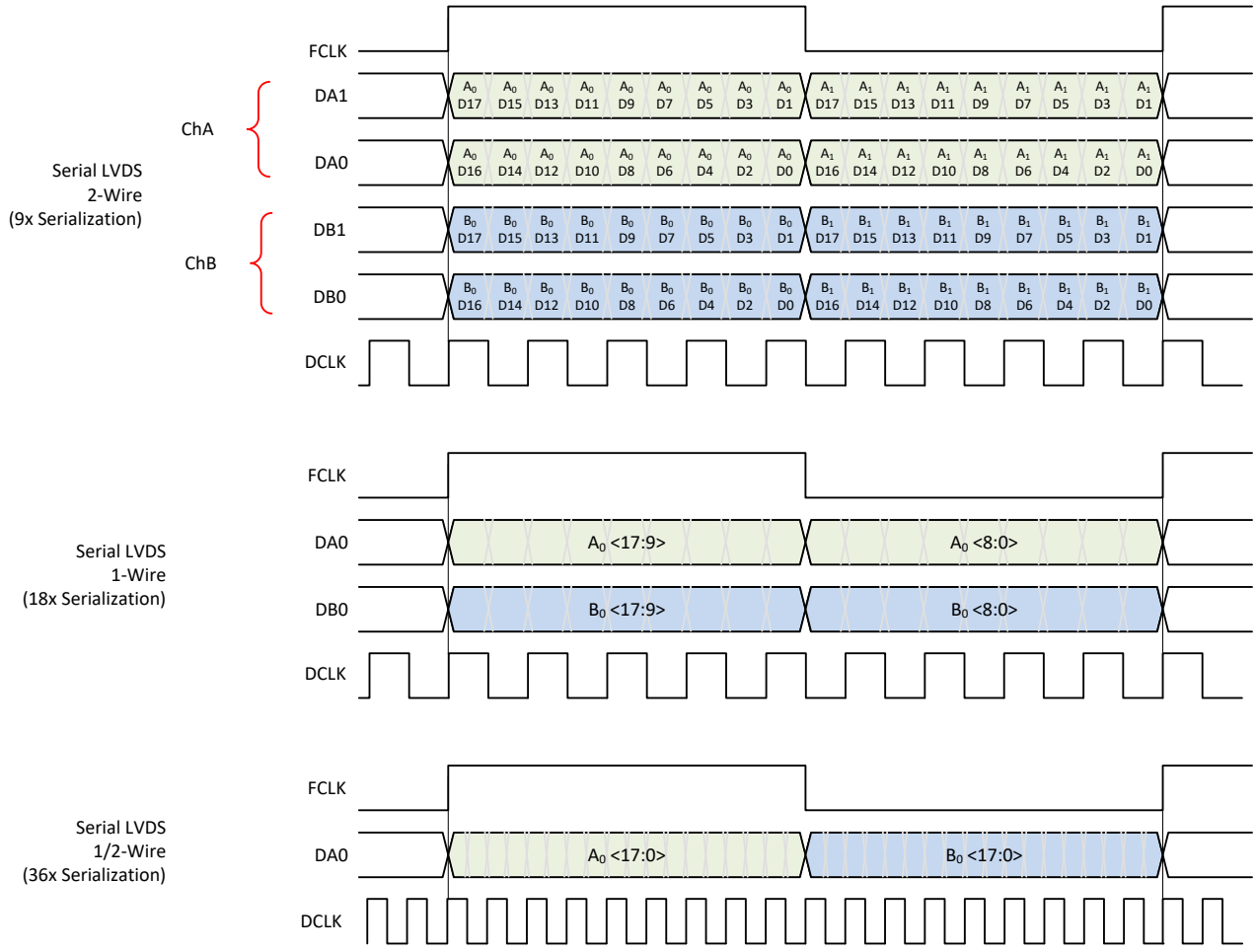


図 7-39. Output Data Format in Real Decimation (18-bit Output Resolution)

表 7-5 illustrates the output interface data rate along with the corresponding DCLK/DCLKIN and FCLK frequencies based on output resolution (R), number of SLVDS lanes (L) and real decimation setting (M).

The table shows an actual lane rate example for the 2-, 1- and 1/2-wire interface, 18-bit output resolution and real decimation by 4.

表 7-5. Serial LVDS Lane Rate Examples with Real Decimation and 18-bit Output Resolution

DECIMATION SETTING	ADC SAMPLING RATE	OUTPUT RESOLUTION	# of WIRES	FCLK	DCLKIN, DCLK	DA/B0,1
M	F_S	R	L	F_S / M / 2 (L = 2) F_S / M (L = 1, 1/2)	[DA/B0,1] / 2	F_S x R / L / M
4	65MSPS	18	2	8.125MHz	73.125 MHz	146.25 MHz
			1	16.25MHz	146.25 MHz	292.5 MHz
			1/2		292.5 MHz	585 MHz

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7.3.5 Digital Data Path and Interface

The ADC3683-xEP uses a serial LVDS (SLVDS) interface to output the ADC data which minimizes the number of digital interconnects. The SLVDS interface is configured to one of the following modes: two LVDS lanes per channel (2-wire), one LVDS lane per channel (1-wire), or a half-lane mode (1/2-wire) option where both channels are multiplexed on a single LVDS lane. The device supports configurable output resolutions from 14-bit to 20-bit.

The ADC3683-xEP requires an external interface clock (DCLKIN). A delayed version of DCLKIN is used as the interface output clock (DCLK).

7.3.5.1 Data Path Overview

The ADC3683-xEP offers a flexible set of digital features (図 7-40) where all, or a subset of the features are used. The core ADC provides an 18-bit output which is passed to the digital down converter (DDC), or directly provided to the digital interface through the resolution selector and bit mapper. Since the ADC core offers low latency, the digital blocks must be bypassed (D2 of 0x24) for the lowest latency. The final data path goes through a resolution selection block and an output bit mapper. The resolution selector offers selection of a 14-bit, 16-bit, 18-bit, or 20-bit output. For 14-bit and 16-bit output resolutions, the LSBs are truncated during the reformatting. With 20-bit output, in bypass mode, two 0s are added. Two LSBs are added for 20-bit mode in decimation modes. Lastly, the output bit mapper maps the bit transmit order on the active lanes. The output serialization factor is internally adjusted based the 2-, 1-, and 1/2-wire interface modes and resolution; however, the maximum SLVDS interface output data rate of 1Gbps can not be exceeded regardless of the interface settings.

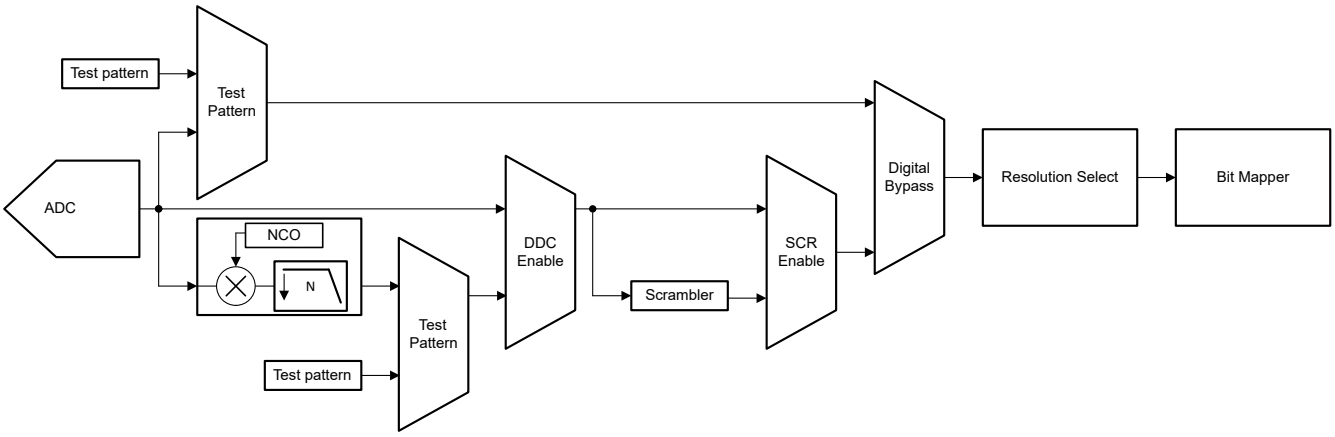


図 7-40. Digital Data Path Overview

7.3.5.2 Output Scrambler

The ADC3683-xEP includes an optional output scrambler feature in 2-wire mode only. The scrambler can enabled by enabling the DSP features (D2 of 0x24) and enabling scrambling (D6 of 0x22). When enabled, each sample is split into two halves. Each half of the samples stream is scrambled independently. For example, if the samples stream is at an 18-bit resolution, the stream is divided into two halves consisting of bits D17-D9 & D8-D0. The two halves are fed into independent scrambling blocks where each input bit (x[k]) of each scrambler is XOR-ed with 2 previous bits (y[k-14] and y[k-15]) as shown in 図 7-41. Since this is a self-synchronizing scrambler, the start up state of the scrambler is ignored.

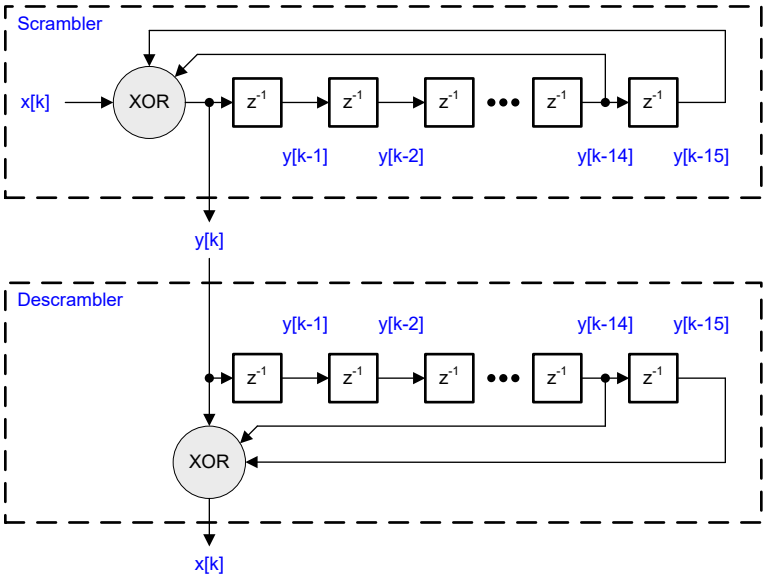


図 7-41. Scrambler and Descrambler Operation

注

The sample streams fed into each scrambler are fed to the scrambler LSB first. Therefore, in the previous example, the sample stream half consisting of D8-D0 is provided to the scrambler with D0 first as x[k] followed by D1 as x[k+1] and so on.

For proper descrambling, the sample stream halves are descrambled independently, then the descrambled data is used to reconstruct the samples. On the receiver side, the incoming serial data stream is descrambled by XOR-ing each incoming bit (y[k]) with 2 previous bits (y[k-14] and y[k-15]).

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注

Since the scramblers are looking at the two halves of the sample stream, the output bit mapper needs to be configured such that each lane contains only one of the sample halves.

For example, in 2-wire and 18-bit mode, by default (図 6-1), one lane carries the odd bits (D17, D15, D13, etc.) and one lane carries the even bits (D16, D14, D12, and so on). When scrambling is enabled, the bit mapper needs to be configured so that one lane carries bits D9-D17 and the other lane carries D0-D8 (LSB first for each lane). An example data flow diagram of scrambling an 18-bit sample stream is shown in 図 7-42, where D17:D0 is the sample provided by the ADC after the resolution select block, the sample is split into D0-D8 and D9-D17 and fed into each scrambler (LSB first) and S0-S17 are the resultant scrambled bits.

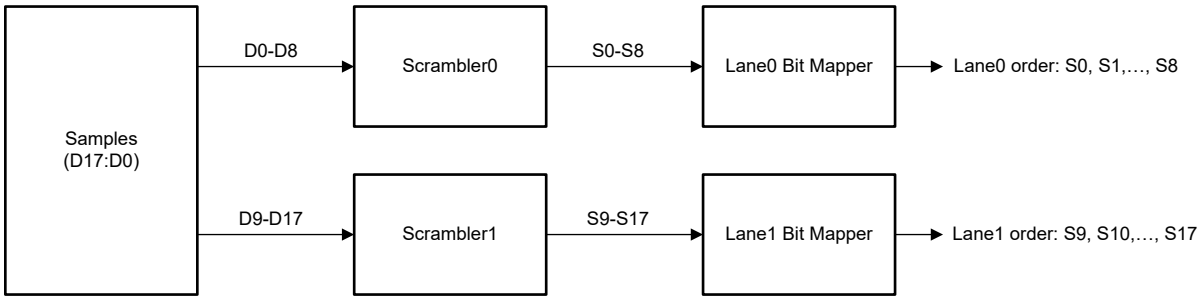


図 7-42. 18-bit Scrambling Example

7.3.5.3 Output Bit Mapper

The output bit mapper sits right before the physical output interface and dictates the transmitted bit order on each active lane. Each sample bit is uniquely identifiable by a value as shown in 表 7-6. Similarly, each bit position in each lane is also uniquely identifiable with each bit position having an independent register address. To map a specific bit to a specific bit position (and a specific lane), the value for the bit from the 表 7-6 needs to be written to the address corresponding to the desired bit position in the desired lane.

The ADC3683-xEP supports a maximum output resolution of 20-bit; therefore, there are 20-bits that are uniquely identifiable per channel. In 2-wire mode, two samples are considered part of the same frame; therefore, there are two sets of 20-bits each, one for the previous sample and another for the current sample. セクション 7.3.5.3.1, セクション 7.3.5.3.2, and セクション 7.3.5.3.3 provide the register addresses that correspond to each bit position in each lane for 2-wire, 1-wire, and 1/2-wire, respectively.

表 7-6. Unique Bit Identifiers

BIT_ID	Channel A		Channel B	
	Previous sample (2w only)	Current sample	Previous sample (2w only)	Current sample
D19 (MSB)	0x2D	0x6D	0x29	0x69
D18	0x2C	0x6C	0x28	0x68
D17	0x27	0x67	0x23	0x63
D16	0x26	0x66	0x22	0x62
D15	0x25	0x65	0x21	0x61
D14	0x24	0x64	0x20	0x60
D13	0x1F	0x5F	0x1B	0x5B
D12	0x1E	0x5E	0x1A	0x5A
D11	0x1D	0x5D	0x19	0x59
D10	0x1C	0x5C	0x18	0x58
D9	0x17	0x57	0x13	0x53
D8	0x16	0x56	0x12	0x52
D7	0x15	0x55	0x11	0x51
D6	0x14	0x54	0x10	0x50
D5	0x0F	0x4F	0x0B	0x4B
D4	0x0E	0x4E	0x0A	0x4A
D3	0x0D	0x4D	0x09	0x49
D2	0x0C	0x4C	0x08	0x48
D1	0x07	0x47	0x03	0x43
D0 (LSB)	0x06	0x46	0x02	0x42

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7.3.5.3.1 2-Wire Mode

In this mode, both the current and the previous sample have to be used in the address space as shown in 図 7-43. The address order is different for 14/18-bit and 16/20-bit.

注

There are unused addresses between samples for resolution less than 20-bit (gray back ground), which is skipped if not used.

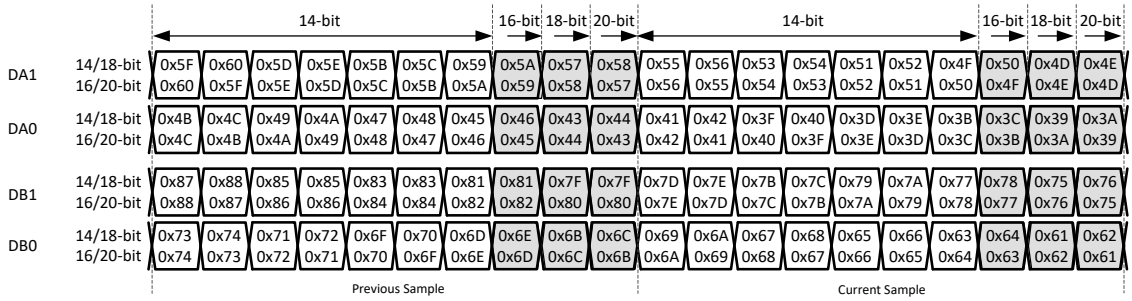


図 7-43. 2-wire output bit mapper

In the following example (図 7-44), the 16-bit 2-wire serial output is reordered to where lane DA1/DB1 carries the 8 MSB and lane DA0/DB0 carries 8 LSBs.

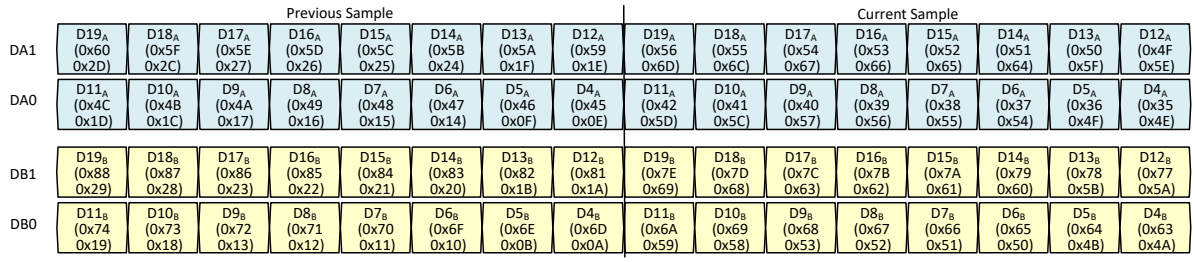


図 7-44. Example: 2-wire output bit mapping

7.3.5.3.2 1-Wire Mode

Only the *current sample* needs to programmed in the address space. If desired, the current sample is duplicated on DA1/DB1 as well (using addresses shown below) to have a redundant output. In this case, lane DA1/DB1 needs to be powered up.

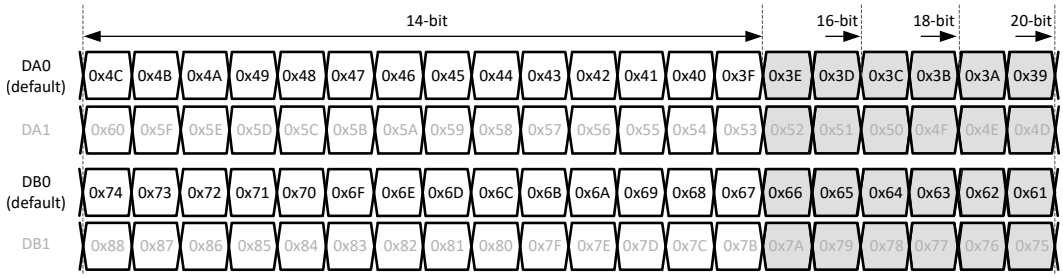


図 7-45. 1-wire output bit mapping

7.3.5.3.3 ½-Wire Mode

The output is only lane DA0 and the sample order is programmed into the 40 addresses of chA (from 0x39 to 0x60). Covering 2 samples (one for chA, one for chB) as shown below. To have a redundant output, duplicate on DB0 (using addresses shown in 図 7-46). In that case, Lane DB0 needs to be powered up.

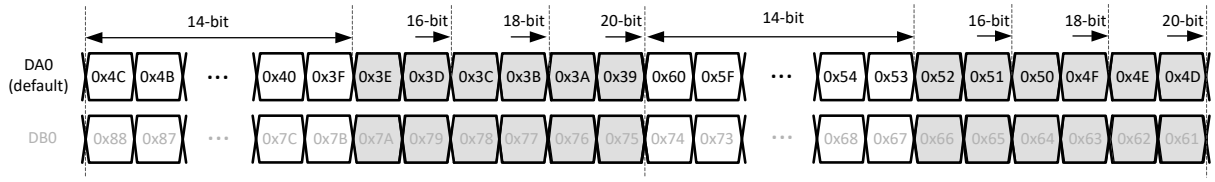


図 7-46. 1/2-wire output bit mapping

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7.3.5.4 Device Configuration Steps

The following sequence summarizes all the relevant registers for changing the ADC3683-xEP modes including DDC and output interface. Steps 1 and 2 must come first since the E-Fuse load resets some of the device registers, the remaining steps can come in any order.

表 7-7. Configuration steps for changing interface or decimation

<table>
<tr><th>STEP</th><th>FEATURE</th><th>ADDRESS</th><th colspan="6">DESCRIPTION</th></tr>
<tr><td rowspan="6">1</td><td rowspan="19">Output Interface</td><td rowspan="6">0x07</td><td colspan="6">Select the output interface bit mapping depending on resolution and output interface.</td></tr>
<tr><td colspan="2">Output Resolution</td><td>2-wire</td><td>1-wire</td><td>1/2-wire</td></tr>
<tr><td colspan="2">14-bit</td><td>0x2B</td><td rowspan="4">0x6C</td><td rowspan="4">0x8D</td></tr>
<tr><td colspan="2">16-bit</td><td>0x4B</td></tr>
<tr><td colspan="2">18-bit</td><td>0x2B</td></tr>
<tr><td colspan="2">20-bit</td><td>0x4B</td></tr>
<tr><td>2</td><td>0x13</td><td colspan="6">Load the output interface bit mapping using the E-fuse loader (0x13, D0). Program register 0x13 to 0x01, wait ~ 1ms so that bit mapping is loaded properly followed by 0x13 0x00.</td></tr>
<tr><td rowspan="8">3</td><td rowspan="8">0x19</td><td colspan="6">Configure the FCLK frequency based on bypass/decimation and number of lanes used.</td></tr>
<tr><td>Bypass/Dec</td><td>SLVDS</td><td>FCLK SRC (D7)</td><td>FCLK DIV (D4)</td><td>TOG FCLK (D0)</td></tr>
<tr><td rowspan="3">Bypass/ Real Decimation</td><td>2-wire</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1-wire</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1/2-wire</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="3">Complex Decimation</td><td>2-wire</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1-wire</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1/2-wire</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>0x1B</td><td colspan="6">Select the output interface resolution using the bit mapper (D5-D3).</td></tr>
<tr><td rowspan="9">5</td><td rowspan="9">0x20
0x21
0x22</td><td colspan="6">Select the FCLK pattern based on decimation mode for the proper duty cycle output of the frame clock.</td></tr>
<tr><td></td><td>Output Resolution</td><td>2-wire</td><td>1-wire</td><td>1/2-wire</td></tr>
<tr><td rowspan="4">Real Decimation</td><td>14-bit</td><td rowspan="8">use default</td><td>0xFE000</td><td rowspan="4">use default</td></tr>
<tr><td>16-bit</td><td>0xFF000</td></tr>
<tr><td>18-bit</td><td>0xFF800</td></tr>
<tr><td>20-bit</td><td>0xFFC00</td></tr>
<tr><td rowspan="4">Complex Decimation</td><td>14-bit</td><td rowspan="4">0xFFFFF</td><td rowspan="4">0xFFFFF</td></tr>
<tr><td>16-bit</td></tr>
<tr><td>18-bit</td></tr>
<tr><td>20-bit</td></tr>
<tr><td>6</td><td>0x39..0x60
0x61..0x88</td><td colspan="6">Change output bit mapping from the default as needed (e.g., if enabling the scrambler).</td></tr>
<tr><td>7</td><td>0x24
0x22</td><td colspan="6">Optionally, enable scrambling.</td></tr>
</table>

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表 7-7. Configuration steps for changing interface or decimation (続き)

STEP	FEATURE	ADDRESS	DESCRIPTION		
8	Decimation Filter	0x24	Enable the decimation filter		
9		0x25	Configure the decimation filter		
10		0x2A/B/C/D 0x31/2/3/4	Program the NCO frequency for complex decimation (skipped for real decimation)		
11		0x27 0x2E	Configure the complex output data stream (set both bits to 0 for real decimation)		
			SLVDS	OP-Order (D4)	Q-Delay (D3)
			2-wire	1	0
			1-wire	0	1
			1/2-wire	1	1
12		0x26	Set the mixer gain and toggle the mixer reset bit to update the NCO frequency.		

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7.3.5.4.1 Configuration Example

The following is a step by step programming example to configure the ADC3683-xEP to complex decimation by 8 with 1-wire SLVDS and 16-bit output.

1. 0x07 (address) 0x6C (load bit mapper configuration for 16-bit output with 1-wire SLVDS)
2. 0x13 0x01, wait 1 ms, 0x13 0x00 (load e-fuse)
3. 0x19 0x80 (configure FCLK)
4. 0x1B 0x88 (select 16-bit output resolution)
5. 0x20 0xFF, 0x21 0xFF, 0x22 0x0F (configure FCLK pattern)
6. 0x24 0x06 (enable decimation filter)
7. 0x25 0x30 (configure complex decimation by 8)
8. 0x2A/B/C/D and 0x31/32/33/34 (program NCO frequency)
9. 0x27/0x2E 0x08 (configure Q-delay register bit)
10. 0x26 0xAA, 0x26 0x88 (set digital mixer gain to 6dB and toggle the mixer update)

7.3.5.5 Output Data Format

The ADC3683-xEP samples are configured for either two's complement format (default) or offset binary via SPI (D2 of 0x8F and 0x92). 表 7-8 provides an overview for minimum and maximum output codes for the two formatting options based on resolution.

表 7-8. Minimum and Maximum ADC Codes

	Two's Complement (default)				Offset Binary			
RESOLUTION (BIT)	**14**	**16**	**18**	**20**	**14**	**16**	**18**	**20**
$V_{IN,MAX}$	0x1FFF	0x7FFF	0x1FFFF	0x7FFFF	0x3FFF	0xFFFF	0x3FFFF	0xFFFFF
0	0x0000		0x00000		0x2000	0x8000	0x20000	0x80000
$V_{IN,MIN}$	0x2000	0x8000	0x20000	0x80000	0x0000		0x00000	

7.3.6 Test Pattern

図 7-40 shows the location of the test pattern blocks within the device. When the digital signal processing (DSP) features are disabled (D2 of 0x24), a test pattern block is enabled to replace the ADC data. Similarly, when using the DDC, a test pattern is available to replace the DDC data.

注

No test pattern block is available when the DSP features are enabled and the DDC is not used.

Each test pattern block has the capability to generate one of the following outputs:

- Ramp pattern with programmable step size set by PAT_DATA.
- Constant pattern with a programmable custom pattern set by PAT_DATA.

図 7-40 shows there are two test pattern blocks, test pattern 0 and test pattern 1. There are two test pattern blocks, test pattern 0 and test pattern 1. The test pattern mode for each block is configured via D7:D5 and D4:D2 of 0x16. A shared set of data bits (PAT_DATA) is given to the test pattern blocks and this data is used as ramp pattern step size and/or the constant pattern. The PAT_DATA is an 18-bit value located across three different registers: D17:D16 in 0x16, D15:D8 in 0x15, and D7:D0 in 0x14. The PAT_DATA is MSB aligned. For example, if the device is configured for 14-bit resolution and constant pattern, only the top 14-bits of the PAT_DATA are used for the constant pattern. Additionally, in ramp mode, the test pattern counter operates at a 18-bit resolution; therefore, the ramp pattern step size must be configured based on the desired resolution and the step size at that resolution.

- The test pattern data must be configured to the following for a step size of one at each resolution:
  - 0x00001: 18-bit output resolution
  - 0x00004: 16-bit output resolution
  - 0x00010: 14-bit output resolution

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7.4 Device Functional Modes

7.4.1 Normal Operation

In normal operating mode, the entire ADC full-scale range gets converted to a digital output with 18-bit resolution.

7.4.2 Power Down Options

A global power down mode is enabled via SPI as well as using the power down pin (PDN/SYNC). There is an internal pull-down 21kΩ resistor on the PDN/SYNC input pin and the pin is active high, so the pin must be pulled high externally to enter global power down mode.

The SPI register map provides the capability to enable/disable individual blocks directly or via PDN pin mask to trade off power consumption vs wake up time as shown in 表 7-9.

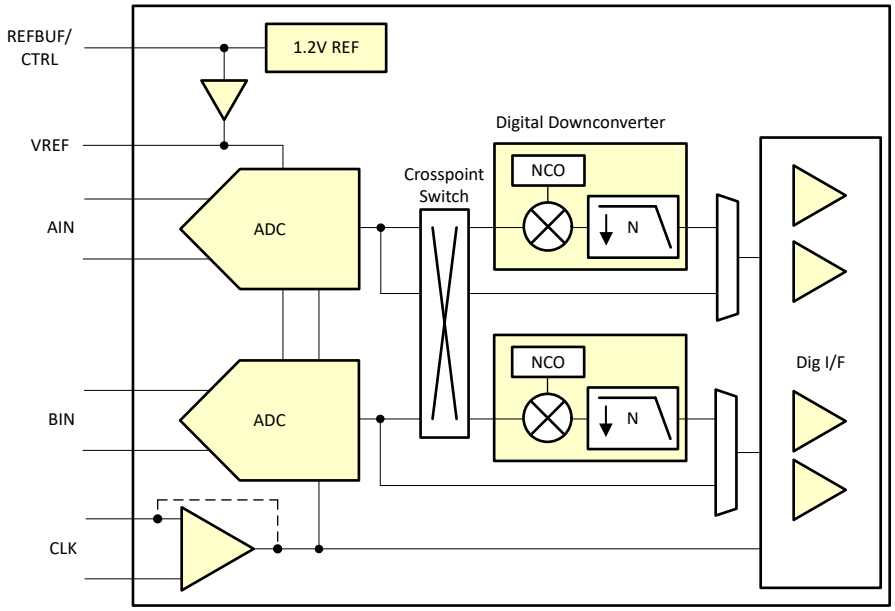


図 7-47. Power Down Configurations

表 7-9. Overview of Power Down Options

Function/ Register	PDN via SPI	Mask for Global PDN	Feature - Default	Power Impact	Wake-up time	Comment
ADC	Yes	-	Enabled			Both ADC channels are included in Global PDN automatically
Reference gain amplifier	Yes	Yes	Enabled	~ 0.4mA	~3us	Should only be powered down in power down state.
Internal 1.2V reference	Yes		External ref	~ 1-3.5mA	~3ms	Internal/external reference selection is available through SPI and REFBUF/CTRL pin.
Clock buffer	Yes		Differential clock	~ 1mA	n/a	Single ended clock input saves ~ 1mA compared to differential. Some programmability is available through the REFBUF/CTRL pin.
Output interface drivers	Yes	-	Enabled	varies	n/a	Depending on output interface mode, unused output drivers is powered down for maximum power savings
Decimation filter	Yes	-	Disabled	see Electrical table	n/a	

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7.4.3 Digital Channel Averaging

The ADC3683-xEP includes a digital channel averaging feature which enables improvement of the ADC dynamic range (see 図 7-48). The same input signal is given to both ADC inputs externally and the output of the two ADCs is averaged internally. By averaging, uncorrelated noise (that is, ADC thermal noise) improves 3dB while correlated noise (that is, jitter in the clock path, reference noise) is unaffected. Therefore, the averaging gives close to 3dB improvement at low input frequencies but less at high input frequencies where clock jitter dominates the SNR.

The output from the digital averaging block is given out on the digital outputs of channel A or alternatively is routed to the digital decimation filters using the digital mux.

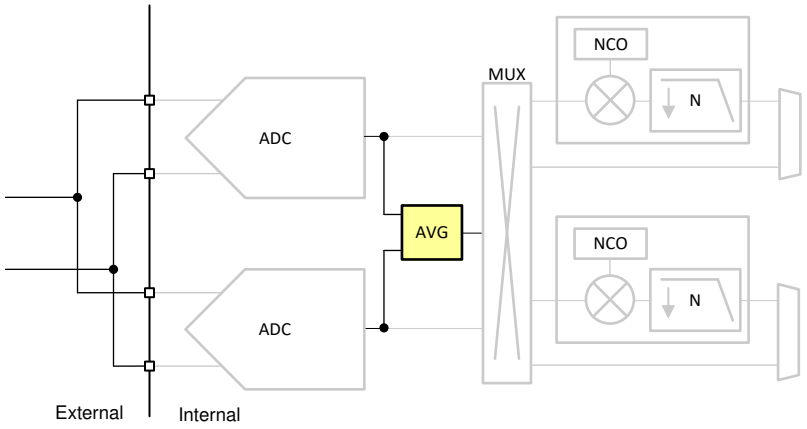


図 7-48. Digital Channel Averaging Diagram

7.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI); however, the device can operate in a default configuration without requiring the SPI interface. Also, the power down function and internal or external reference configuration is possible via pin control (PDN/SYNC and REFBUF/CTRL pin).

注

The power down command (via PIN or SPI) only goes in effect with the ADC sampling clock present.

After initial power up, the default operating configuration for each device is shown in 表 7-10.

表 7-10. Default device configuration after power up

FEATURE	ADC3683-xEP
Signal Input	Differential
Auto-zero	Disabled
Clock Input	Differential
Reference	External
Decimation	DDC bypass
Interface	2-wire
Output Format	2s complement

7.5.1 Configuration using PINs only

The ADC voltage reference is selected using the REFBUF/CTRL pin. Even though there is an internal 100kΩ pull-up resistor to AVDD, the REFBUF/CTRL pin should be set to a voltage externally and not left floating. When using a voltage divider to set the REFBUF/CTRL voltage (R1 and R2 in 図 7-49), resistor values < 5kΩ are used.

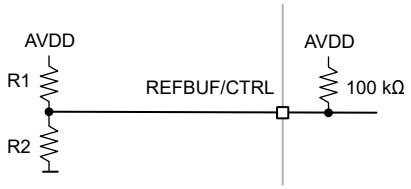


図 7-49. Configuration of external voltage on REFBUF/CTRL pin

表 7-11. REFBUF/CTRL voltage levels control voltage reference selection

REFBUF/CTRL VOLTAGE	VOLTAGE REFERENCE OPTION	CLOCKING OPTION
> 1.7V (Default)	External reference	Differential clock input
1.2V (1.15-1.25V)	External 1.2V input on REFBUF/CTRL pin using internal gain buffer	Differential clock input
0.5 - 0.7V	Internal reference	Differential clock input
< 0.1V	Internal reference	Single ended clock input

7.5.2 Configuration using the SPI interface

The device has a set of internal registers that are accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data is loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 12MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

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7.5.2.1 Register Write

The internal registers are programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

図 7-50 shows the timing requirements for the serial register write operation.

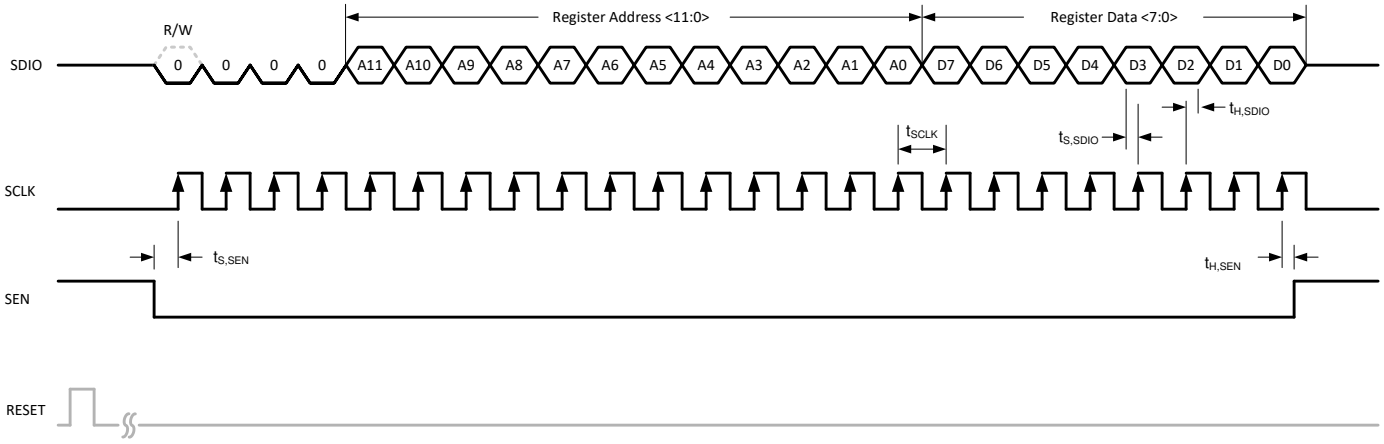


図 7-50. Serial Register Write Timing Diagram

7.5.2.2 Register Read

The device includes a mode where the contents of the internal registers are read back using the SDIO pin. This readback mode is useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content is read
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge
5. The external controller can capture the contents on the SCLK rising edge

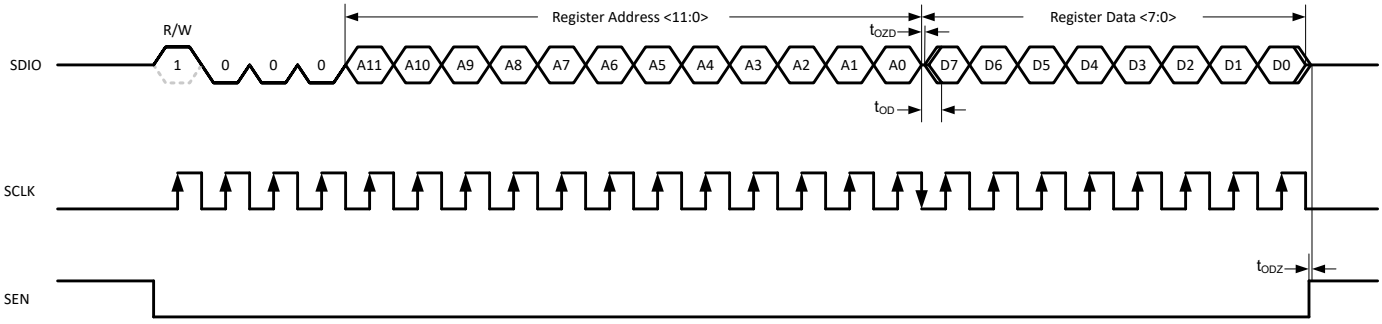


図 7-51. Serial Register Read Timing Diagram

8 Application Information Disclaimer

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A spectrum analyzer is a typical frequency domain application for the ADC3683-xEP and the front end circuitry is similar to several other systems such as software defined radio (SDR), sonar, radar or communications. Some applications require frequency coverage including DC or near DC (such as, sonar), which is included in this example.

(4)

8.2 Typical Application

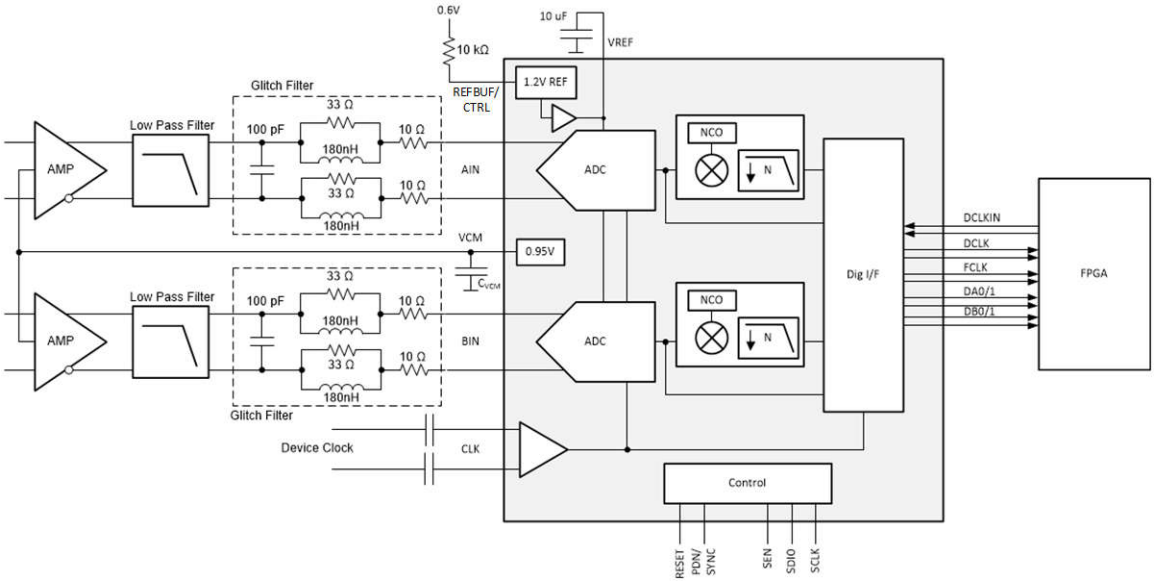


図 8-1. Typical configuration for a spectrum analyzer with DC support

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8.2.1 Design Requirements

Frequency domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone to under sampling in higher Nyquist zones. If low input frequency is supported, then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA). If low frequency support is not needed, then AC coupling and use of a balun is more suitable.

The internal reference is used since DC precision is not needed. However, the ADC AC performance is dependent on the quality of the external clock source. If in-band interferes are present, then the ADC SFDR performance is a key care about. A higher ADC sampling rate is desirable to relax the external anti-aliasing filter. An internal decimation filter is used to reduce the digital output rate afterwards.

表 8-1. Design key care-abouts

FEATURE	DESCRIPTION
Signal Bandwidth	DC to 20MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	External clock with low jitter

When designing the amplifier or filter driving circuit, the ADC input full-scale voltage needs to be considered. For example, the ADC3683-xEP input full-scale is 3.2Vpp. When factoring in approximately 1dB for insertion loss of the filter, then the amplifier needs to deliver close to 3.6Vpp. The amplifier distortion performance degrades with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The ADC3683-xEP provides an output common mode voltage of 0.95V and the THS4541 for example can only swing within 250mV of the negative supply. A unipolar 3.3V amplifier power supply limits the maximum voltage swing to approximately 2.8Vpp. If a larger output swing is required (factoring in filter insertion loss), then a negative supply for the amplifier is needed to eliminate that limitation. Additionally, input voltage protection diodes are needed to protect the ADC from over-voltage events.

表 8-2. Output voltage swing of THS4541 vs power supply

DEVICE	MIN OUTPUT VOLTAGE	MAX SWING WITH 3.3V/ 0V SUPPLY	MAX SWING WITH 3.3V/ -1.V SUPPLY
THS4541	VS- + 250mV	2.8Vpp	6.8Vpp

8.2.2 Detailed Design Procedure

8.2.2.1 Input Signal Path

Depending on desired input signal frequency range the THS4551 and THS4541 provide good low power options to drive the ADC inputs. 表 8-3 provides a comparison between the THS4551 and THS4541 and the power consumption vs usable frequency trade off.

表 8-3. Fully Differential Amplifier Options

DEVICE	CURRENT (IQ) PER CHANNEL	USABLE FREQUENCY RANGE
THS4561	0.8mA	< 3MHz
THS4551	1.4mA	< 10MHz
THS4541	10mA	< 70MHz

The low pass filter design (topology, filter order) is driven by the application itself. However, when designing the low pass filter, the optimum load impedance for the amplifier is taken into consideration as well. Between the low pass filter and the ADC input, the sampling glitch filter needs to be added as shown in セクション 7.3.1.2.1. In this example, the DC - 30MHz glitch filter is selected.

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8.2.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (that is, square wave vs sine wave). 表 8-4 provides an overview of the estimated SNR performance of the ADC3683-xEP based on different amounts of jitter of the external clock source. The SNR is estimated based on ADC3683-xEP thermal noise of 84.2dBFS and input signal at −1dBFS.

Termination of the clock input should be considered for long clock traces.

表 8-4. ADC SNR performance across vs input frequency for different amounts of external clock jitter

INPUT FREQUENCY	$T_{J,EXT}$ = 100fs	$T_{J,EXT}$ = 250fs	$T_{J,EXT}$ = 500fs	$T_{J,EXT}$ = 1ps
5 MHz	84.2	84.1	83.9	83.4
10 MHz	84.0	83.9	83.3	81.5
20 MHz	83.6	83.0	81.3	77.8

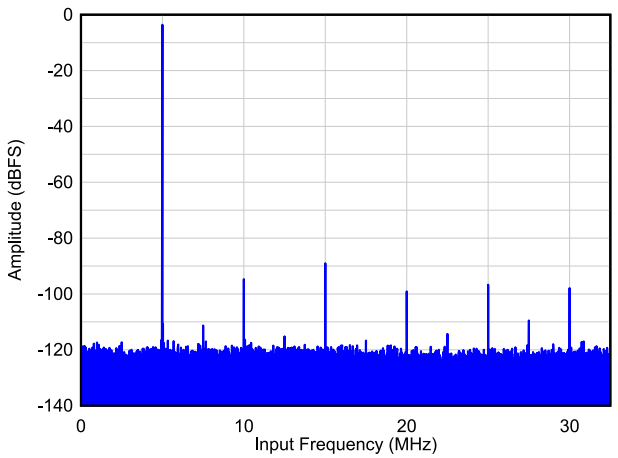
8.2.2.3 Voltage Reference

The ADC3683-xEP is configured to internal reference operation by applying 0.6V to the REFBUF/CTRL pin.

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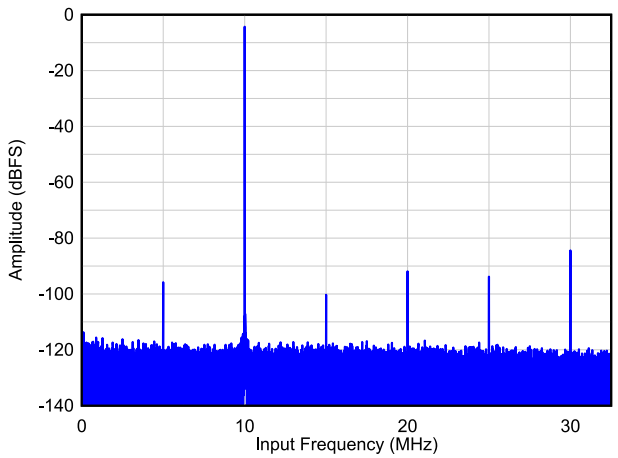
8.2.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3683-xEP operated at 65MSPS with a full-scale input at −1dBFS and input frequencies of 5, 10 and 20MHz.



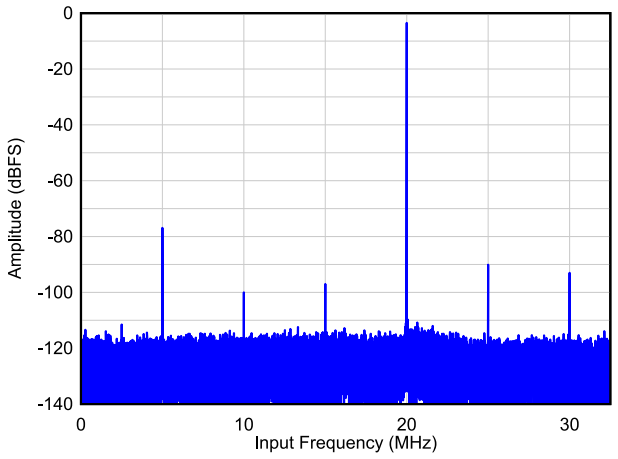
SNR = 81.5dBFS, SFDR = 88dBc, Non HD23 = 95dBFS

図 8-2. Single Tone FFT at F_{IN} = 5MHz



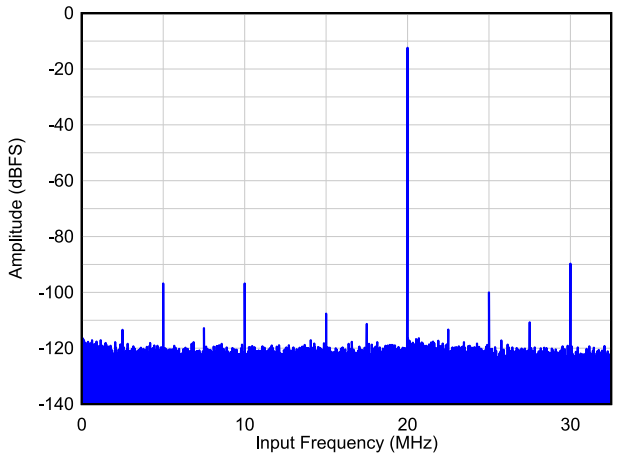
SNR = 80.9dBFS, SFDR = 91dBc, Non HD23 = 83dBFS

図 8-3. Single Tone FFT at F_{IN} = 10MHz



SNR = 77.6dBFS, SFDR = 76dBc, Non HD23 = 93dBFS

図 8-4. Single Tone FFT at F_{IN} = 20MHz



A_{IN} = -10dBFS, SNR = 81.3dBFS, SFDR = 87dBc, Non HD23 = 90dBFS

図 8-5. Single Tone FFT at F_{IN} = 20MHz

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8.3 Initialization Set Up

After power-up, the internal registers must be initialized to the default values through a hardware reset by applying a high pulse on the RESET pin, as shown in 図 8-6.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied, the internal bandgap reference powers up and settles out in approximately 2ms.
2. Configure REFBUF/CTRL pin (pull high or low even if configured through SPI later on) and apply the sampling clock.
3. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up capacitor calibration is initiated. The calibration takes approximately 200000 clock cycles.
4. Begin programming using the SPI interface.

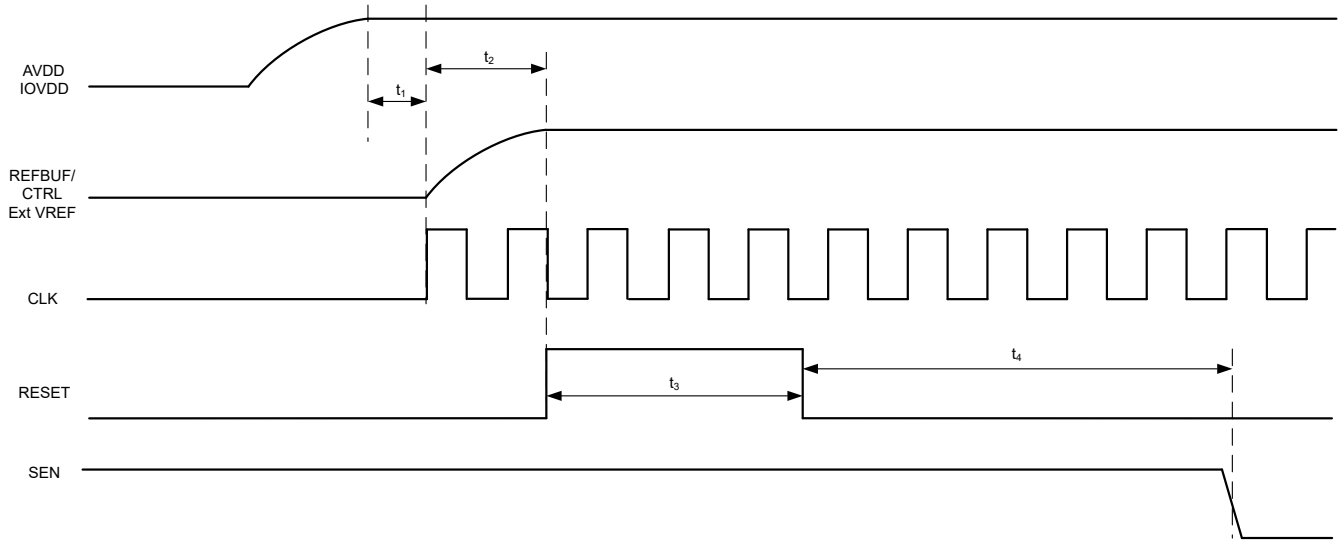


図 8-6. Initialization of serial registers after power up

表 8-5. Power-up timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay: delay from power up to logic level of REFBUF/CTRL pin	2			ms
t_2	Delay from REFBUF/CTRL pin logic level to RESET rising edge	100			ns
t_3	RESET pulse width	1			us
t_4	Delay from RESET disable to SEN active	~ 200000			clock cycles

8.3.1 Register Initialization During Operation

If required, the serial interface registers are cleared and reset to default settings during operation either:

- through a hardware reset or
- by applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 0x00) high. This setting initializes the internal registers to the default values, and then self-resets the RESET bit low. The RESET pin is kept low.

After hardware or software reset, the wait time is approximately 200000 clock cycles before the SPI registers are programmed.

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8.4 Power Supply Recommendations

The ADC3683-xEP requires two different power-supplies. The AVDD rail provides power for the internal analog circuits and the ADC itself while the IOVDD rail powers the digital interface and the internal digital circuits like decimation filter or output interface mapper. Power sequencing is not required.

The AVDD power supply must be low noise to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply needs to be considered as well. The ADC is designed for good PSRR which aides with the power supply filter design.

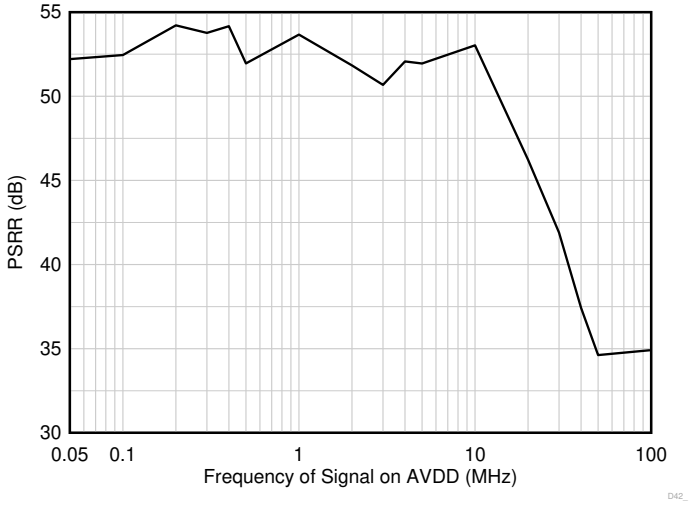


図 8-7. Power supply rejection ratio (PSRR) vs frequency

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to make sure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer are used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS7H4010-SEP, and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS73801-SE, TPS7H1111-SEP, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. 図 8-8 and 図 8-9 illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.

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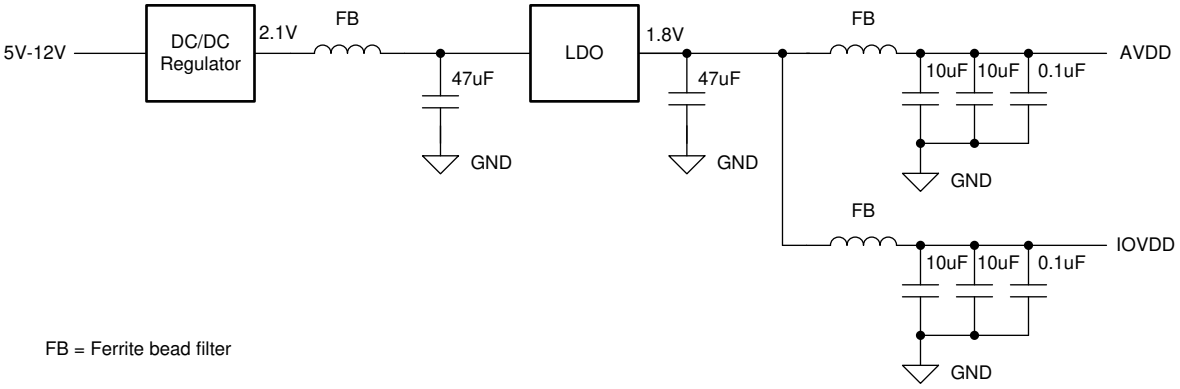


図 8-8. Example: LDO Linear Regulator Approach

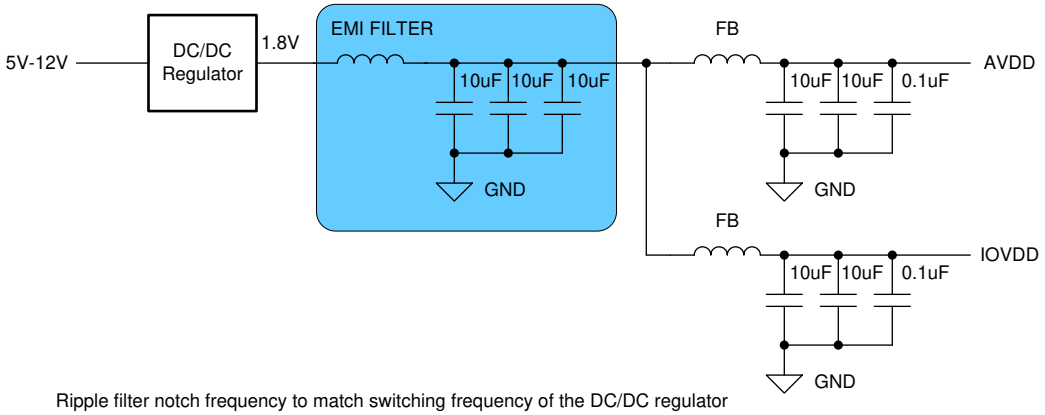


図 8-9. Example Switcher-Only Approach

8.5 Layout

8.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100Ω differential traces.
   - Differential trace lengths are matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital output interface
   - Traces are routed using tightly coupled 100Ω differential traces.
3. Voltage reference
   - The bypass capacitor is placed as close to the device pins as possible, and connected between VREF and REFGND on top layer avoiding vias.
   - Depending on configuration, an additional bypass capacitor between REFBUF/CTRL and REFGND is recommended, and is placed as close to pins as possible on the top layer.
4. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.

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- Use a signal, ground, or power circuit board stack up to maximize coupling between the ground and power plane.

8.5.2 Layout Example

The following screen shot shows the top layer of the ADC3683EVM.

- Signal and clock inputs are routed as differential signals on the top layer avoiding vias.
- SLVDS output interface lanes are routed differential and length matched
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

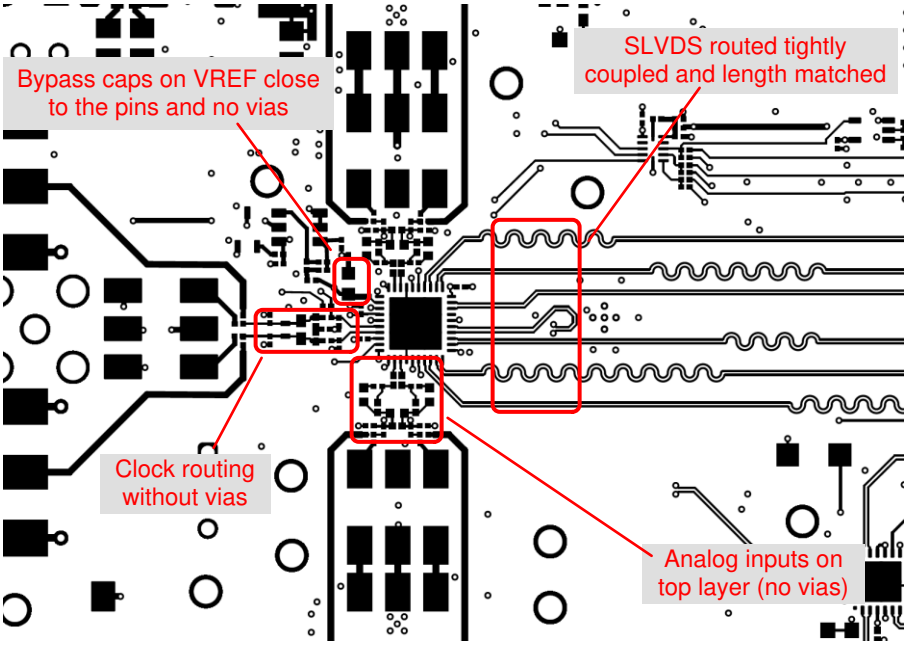


図 8-10. Layout example: top layer of ADC3683EVM

9 Register Map

表 9-1. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	0	0	0	0	0	0	0	RESET
0x07	OP IF MAPPER			0	OP IF EN	OP IF SEL		
0x08	0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	PDN B	PDN GLOBAL
0x09	0	0	PDN FCLKOUT	PDN DCLKOUT	PDN DA1	PDN DA0	PDN DB1	PDN DB0
0x0D	0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
0x0E	SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTRL	REF SEL		SE CLK EN
0x11	0	0	0	0	0	DLL PDN	0	AZ EN
0x13	0	0	0	0	0	0	0	E-FUSE LD
0x14	CUSTOM PAT [7:0]							
0x15	CUSTOM PAT [15:8]							
0x16	TEST PAT B			TEST PAT A			CUSTOM PAT [17:16]	
0x19	FCLK SRC	0	0	FCLK DIV	0	0	0	TOG FCLK
0x1A	0	LVDS ½ SWING	0	0	0	0	0	0
0x1B	MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
0x1E	0	0	0	0	LVDS DATA DEL		LVDS DCLK DEL	
0x20	FCLK PAT [7:0]							
0x21	FCLK PAT [15:8]							
0x22	0	SCR EN	0	0	FCLK PAT [19:16]			
0x24	0	0	CH AVG EN	DDC MUX		DIG BYP	DDC EN	0
0x25	DDC MUX EN	DECIMATION			REAL OUT	0	0	MIX PHASE
0x26	MIX GAIN A		MIX RES A	FS/4 MIX A	MIX GAIN B		MIX RES B	FS/4 MIX B
0x27	0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
0x2A	NCO A [7:0]							
0x2B	NCO A [15:8]							
0x2C	NCO A [23:16]							
0x2D	NCO A [31:24]							
0x2E	0	0	0	OP ORDER B	Q-DEL B	FS/4 MIX PH B	0	0
0x31	NCO B [7:0]							
0x32	NCO B [15:8]							
0x33	NCO B [23:16]							
0x34	NCO B [31:24]							
0x39..0x60	OUTPUT BIT MAPPER CHA							
0x61..0x88	OUTPUT BIT MAPPER CHB							
0x8F	0	0	0	0	0	0	FORMAT A	0
0x92	0	0	0	0	0	0	FORMAT B	0

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9.1 Detailed Register Description

図 9-1. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-2. Register 0x00 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

図 9-2. Register 0x07

7	6	5	4	3	2	1	0
OP IF MAPPER			0	OP IF EN	OP IF SEL		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-3. Register 0x07 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OP IF MAPPER	R/W	000	Output interface mapper. This register contains the proper output interface bit mapping for the different interfaces. The interface bit mapping is internally loaded from e-fuses and also requires a fuse load command to go into effect (0x13, D0). Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. After initial reset the default output interface variant is loaded automatically from fuse internally. However, when reading back this register reads 000 until a value is written using SPI. 001: 2-wire, 18 and 14-bit 010: 2-wire, 16-bit 011: 1-wire 100: 0.5-wire others: not used
4	0	R/W	0	Must write 0
3	OP IF EN	R/W	0	Enables changing the default output interface mode (D2-D0).
2-0	OP IF SEL	R/W	000	Selection of the output interface mode. OP IF EN (D3) needs to be enabled also. After initial reset the default output interface is loaded automatically from fuse internally. However, when reading back this register reads 000 until a value is written using SPI. 011: 2-wire 100: 1-wire 101: 0.5-wire others: not used

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図 9-3. Register 0x08

7	6	5	4	3	2	1	0
0	0	PDN CLKBUF	PDN REFAMP	0	PDN A	PDN B	PDN GLOBAL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-4. Register 0x08 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	PDN CLKBUF	R/W	0	Powers down sampling clock buffer 0: Clock buffer enabled 1: Clock buffer powered down
4	PDN REFAMP	R/W	0	Powers down internal reference gain amplifier 0: REFAMP enabled 1: REFAMP powered down
3	0	R/W	0	Must write 0
2	PDN A	R/W	0	Powers down ADC channel A 0: ADC channel A enabled 1: ADC channel A powered down
1	PDN B	R/W	0	Powers down ADC channel B 0: ADC channel B enabled 1: ADC channel B powered down
0	PDN GLOBAL	R/W	0	Global power down via SPI 0: Global power disabled 1: Global power down enabled. Power down mask (register 0x0D) determines which internal blocks are powered down.

図 9-4. Register 0x09

7	6	5	4	3	2	1	0
0	0	PDN FCLKOUT	PDN DCLKOUT	PDN DA1	PDN DA0	PDN DB1	PDN DB0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-5. Register 0x09 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	PDN FCLKOUT	R/W	0	Powers down frame clock (FCLK) LVDS output buffer 0: FCLK output buffer enabled 1: FCLK output buffer powered down
4	PDN DCLKOUT	R/W	0	Powers down DCLK LVDS output buffer 0: DCLK output buffer enabled 1: DCLK output buffer powered down
3	PDN DA1	R/W	0	Powers down LVDS output buffer for channel A, lane 1. NOT powered down automatically in 1-wire and 1/2-wire mode. 0: DA1 LVDS output buffer enabled 1: DA1 LVDS output buffer powered down
2	PDN DA0	R/W	0	Powers down LVDS output buffer for channel A, lane 0. 0: DA0 LVDS output buffer enabled 1: DA0 LVDS output buffer powered down
1	PDN DB1	R/W	0	Powers down LVDS output buffer for channel B, lane 1. NOT powered down automatically in 1-wire and 1/2-wire mode. 0: DB1 LVDS output buffer enabled 1: DB1 LVDS output buffer powered down
0	PDN DB0	R/W	0	Powers down LVDS output buffer for channel B, lane 0. NOT powered down automatically in 1/2-wire mode. 0: DB0 LVDS output buffer enabled 1: DB0 LVDS output buffer powered down

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図 9-5. Register 0x0D (PDN GLOBAL MASK)

7	6	5	4	3	2	1	0
0	0	0	0	MASK CLKBUF	MASK REFAMP	MASK BG DIS	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-6. Register 0x0D Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3	MASK CLKBUF	R/W	0	Global power down mask control for sampling clock input buffer. 0: Clock buffer will get powered down when global power down is exercised. 1: Clock buffer will NOT get powered down when global power down is exercised.
2	MASK REFAMP	R/W	0	Global power down mask control for reference amplifier. 0: Reference amplifier will get powered down when global power down is exercised. 1: Reference amplifier will NOT get powered down when global power down is exercised.
1	MASK BG DIS	R/W	0	Global power down mask control for internal 1.2V bandgap voltage reference. Setting this bit reduces power consumption in global power down mode but increases the wake up time. See the power down option overview. 0: Internal 1.2V bandgap voltage reference will NOT get powered down when global power down is exercised. 1: Internal 1.2V bandgap voltage reference will get powered down when global power down is exercised.
0	0	R/W	0	Must write 0

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図 9-6. Register 0x0E

7	6	5	4	3	2	1	0
SYNC PIN EN	SPI SYNC	SPI SYNC EN	0	REF CTL	REF SEL		SE CLK EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-7. Register 0x0E Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC PIN EN	R/W	0	This bit controls the functionality of the SYNC/PDN pin. 0: SYNC/PDN pin exercises global power down mode when pin is pulled high. 1: SYNC/PDN pin issues the SYNC command when pin is pulled high.
6	SPI SYNC	R/W	0	Toggling this bit issues the SYNC command using the SPI register write. SYNC using SPI must be enabled as well (D5). This bit doesn't self reset to 0. 0: Normal operation 1: SYNC command issued.
5	SPI SYNC EN	R/W	0	This bit enables synchronization using SPI instead of the SYNC/PDN pin. 0: Synchronization using SPI register bit disabled. 1: Synchronization using SPI register bit enabled.
4	0	R/W	0	Must write 0
3	REF CTL	R/W	0	This bit determines if the REFBUF/CTRL pin controls the voltage reference selection or the SPI register (D2-D1). 0: The REFBUF/CTRL pin selects the voltage reference option. 1: Voltage reference is selected using SPI (D2-D1) and single ended clock using D0.
2-1	REF SEL	R/W	00	Selects of the voltage reference option. REF CTRL (D3) must be set to 1. 00: Internal reference 01: External voltage reference (1.2V) using internal reference buffer (REFBUF/CTRL) 10: External voltage reference 11: not used
0	SE CLK EN	R/W	0	Selects single ended clock input and powers down the differential sampling clock input buffer. REF CRTL (D3) must be set to 1. 0: Differential clock input 1: Single ended clock input

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図 9-7. Register 0x11

7	6	5	4	3	2	1	0
0	0	0	0	0	DLL PDN	0	AZ EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-8. Register 0x11 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0
2	DLL PDN	R/W	0	This register applies ONLY to the ADC3683. It powers down the internal DLL, which is used to adjust the sampling time. This register must only be enabled when operating at sampling rates below 40 MSPS. When DLL PDN bit is enabled the sampling time is directly dependent on sampling clock duty cycle (with a 50/50 duty the sampling time is T_S/2). 0: Sampling time is T_S/ 4 1: Sampling time is T_S/2 (only for sampling rates below 40 MSPS).
1	0	R/W	0	Must write 0
0	AZ EN	R/W	0	This bit enables the internal auto-zero circuitry. It is disabled by default for the ADC3683-xEP. 0: Auto-zero disabled 1: Auto-zero enabled

図 9-8. Register 0x13

7	6	5	4	3	2	1	0
0	0	0	0	0	0		E-FUSE LD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-9. Register 0x13 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0
0	E-FUSE LD	R/W	0	This register bit loads the internal bit mapping for different interfaces. After setting the interface in register 0x07, this E-FUSE LD bit needs to be set to 1 and reset to 0 for loading to go into effect. Register 0x07 along with the E-Fuse Load (0x13, D0) needs to be loaded first in the programming sequence since the E-Fuse load resets the SPI writes. 0: E-FUSE LOAD set 1: E-FUSE LOAD reset

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図 9-9. Register 0x14/15/16

7	6	5	4	3	2	1	0
CUSTOM PAT [7:0]							
CUSTOM PAT [15:8]							
TEST PAT B			TEST PAT A			CUSTOM PAT [17:16]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-10. Register 0x14/15/16 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PAT [17:0]	R/W	00000000	This register is used for two purposes: • It sets the constant custom pattern starting from MSB • It sets the RAMP pattern increment step size. 00001: Ramp pattern for 18-bit ADC 00100: Ramp pattern for 16-bit ADC 10000: Ramp pattern for 14-bit ADC
7-5	TEST PAT B	R/W	000	Enables test pattern output mode for channel B (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format.
				000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used
4-2	TEST PAT A	R/W	000	Enables test pattern output mode for channel A (NOTE: The test pattern is set prior to the bit mapper and is based on native resolution of the ADC starting from the MSB). These work in either output format.
				000: Normal output mode (test pattern output disabled) 010: Ramp pattern: need to set proper increment using CUSTOM PAT register 011: Constant Pattern using CUSTOM PAT [17:0] in register 0x14/15/16. others: not used

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図 9-10. Register 0x19

7	6	5	4	3	2	1	0
FCLK SRC	0	0	FCLK DIV	0	0	0	TOG FCLK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-11. Register 0x19 Field Descriptions

Bit	Field	Type	Reset	Description
7	FCLK SRC	R/W	0	User has to select if FCLK signal comes from ADC or from DDC block. Here real decimation is treated same as bypass mode 0: FCLK generated from ADC. FCLK SRC set to 0 for DDC bypass, real decimation mode and 1/2-w complex decimation mode. 1: FCLK generated from DDC block. In complex decimation mode only this bit needs to be set for 2-w and 1-w output interface mode but NOT for 1/2-w mode.
6-5	0	R/W	0	Must write 0
4	FCLK DIV	R/W	0	This bit needs to be set to 1 for 2-w output mode in bypass/real decimation mode only . 0: All output interface modes except 2-w decimation bypass and real decimation mode. 1: 2-w output interface mode for decimation bypass and real decimation.
3-1	0	R/W	0	Must write 0
0	TOG FCLK	R/W	0	This bit adjusts the FCLK signal appropriately for 1/2-wire mode where FCLK is stretched to cover channel A and channel B. This bit ONLY needs to be set in 1/2-wire mode with complex decimation mode. 0: all other modes. 1: FCLK for 1/2-wire complex decimation mode.

表 9-12. Configuration of FCLK SRC and FCLK DIV Register Bits vs Serial Interface

BYPASS/DECIMATION	SERIAL INTERFACE	FCLK SRC	FCLK DIV	TOG FCLK
Decimation Bypass/ Real Decimation	2-wire	0	1	0
	1-wire	0	0	0
	1/2-wire	0	0	0
Complex Decimation	2-wire	1	0	0
	1-wire	1	0	0
	1/2-wire	0	0	1

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図 9-11. Register 0x1A

7	6	5	4	3	2	1	0
0	LVDS ½ SWING	0	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-13. Register 0x1A Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0
6	LVDS ½ SWING	R/W	0	This bit reduces the LVDS output current from 3.5mA to 1.75mA which reduces power consumption.
5-0	0	R/W	0	Must write 0

図 9-12. Register 0x1B

7	6	5	4	3	2	1	0
MAPPER EN	20B EN	BIT MAPPER RES			0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-14. Register 0x1B Field Descriptions

Bit	Field	Type	Reset	Description
7	MAPPER EN	R/W	0	This bit enables changing the resolution of the output (including output serialization factor) in bypass mode only. This bit is not needed for 20-bit resolution output. 0: Output bit mapper disabled. 1: Output bit mapper enabled.
6	20B EN	R/W	0	This bit enables 20-bit output resolution which can be useful for very high decimation settings so that quantization noise doesn't impact the ADC performance. 0: 20-bit output resolution disabled. 1: 20-bit output resolution enabled.
5-3	BIT MAPPER RES	R/W	000	Sets the output resolution using the bit mapper. MAPPER EN bit (D6) needs to be enabled when operating in bypass mode.. 000: 18 bit 001: 16 bit 010: 14 bit all others, n/a
2-0	0	R/W	0	Must write 0

表 9-15. Register Settings for Output Bit Mapper vs Operating Mode

BYPASS/DECIMATION	OUTPUT RESOLUTION	MAPPER EN (D7)	BIT MAPPER RES (D5-D3)
Decimation Bypass	Resolution Change	1	000: 18-bit 001: 16-bit 010: 14-bit
Real Decimation	Resolution Change (default 18-bit)	0	
Complex Decimation		0	

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図 9-13. Register 0x1E

7	6	5	4	3	2	1	0
0	0	0	0	LVDS DATA DEL		LVDS DCLK DEL	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-16. Register 0x1E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3-2	LVDS DATA DEL	R/W	00	These bits adjust the output timing of the SLVDS output data. 00: no delay 01: Data advanced by 50 ps 10: Data delayed by 50 ps 11: Data delayed by 100 ps
1-0	LVDS DCLK DEL	R/W	00	These bits adjust the output timing of the SLVDS DCLK output. 00: no delay 01: DCLK advanced by 50 ps 10: DCLK delayed by 50 ps 11: DCLK delayed by 100 ps

図 9-14. Register 0x20/21/22

7	6	5	4	3	2	1	0
FCLK PAT [7:0]							
FCLK PAT [15:8]							
0	SCR EN	0	0	FCLK PAT [19:16]			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-17. Register 0x20/21/22 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FCLK PAT [19:0]	R/W	0xFFC00	These bits can adjust the duty cycle of the FCLK. In decimation bypass mode the FCLK pattern gets adjusted automatically for the different output resolutions. 表 9-18 shows the proper FCLK pattern values for 1-wire and 1/2-wire in real/complex decimation.
6	SCR EN	R/W	0	This bit enables the output data scrambler. Digital bypass (0x24, D2) needs to be set as well. 0: Output scrambling disabled 1: Output scrambling enabled

表 9-18. FCLK Pattern for different resolution based on interface

DECIMATION	OUTPUT RESOLUTION	2-WIRE	1-WIRE	1/2-WIRE
REAL DECIMATION	14-bit	Use Default	0xFE000	Use Default
	16-bit		0xFF000	
	18-bit		0xFF800	
	20-bit		0xFFC00	
COMPLEX DECIMATION	14-bit		0xFFFFF	0xFFFFF
	16-bit			
	18-bit			
	20-bit			

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図 9-15. Register 0x24

7	6	5	4	3	2	1	0
0	0	CH AVG EN	DDC MUX		DIG BYP	DDC EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-19. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0
5	CH AVG EN	R/W	0	Averages the output of ADC channel A and channel B together. The DDC MUX has to be enabled and set to '11'. The decimation filter needs to be enabled and set to bypass (fullrate output) or decimation and DIG BYP set to 1. 0: Channel averaging feature disabled 1: Output of channel A and channel B are averaged: (A+B)/2.
4-3	DDC MUX	R/W	0	Configures DDC MUX in front of the decimation filter. 00: ADC channel A connected to DDC A; ADC Channel B connected to DDC B 01: ADC channel A connected to DDC A and DDC B. 10: ADC channel B connected to DDC A and DDC B. 11: Output of ADC averaging block (see CH AVG EN) given to DDC A and DDC B.
2	DIG BYP	R/W	0	This bit needs to be set to enable digital features block which includes decimation and scrambling. 0: Digital feature block bypassed - lowest latency 1: Data path includes digital features
1	DDC EN	R/W	0	Enables internal decimation filter for both channels 0: DDC disabled. 1: DDC enabled.
0	0	R/W	0	Must write 0

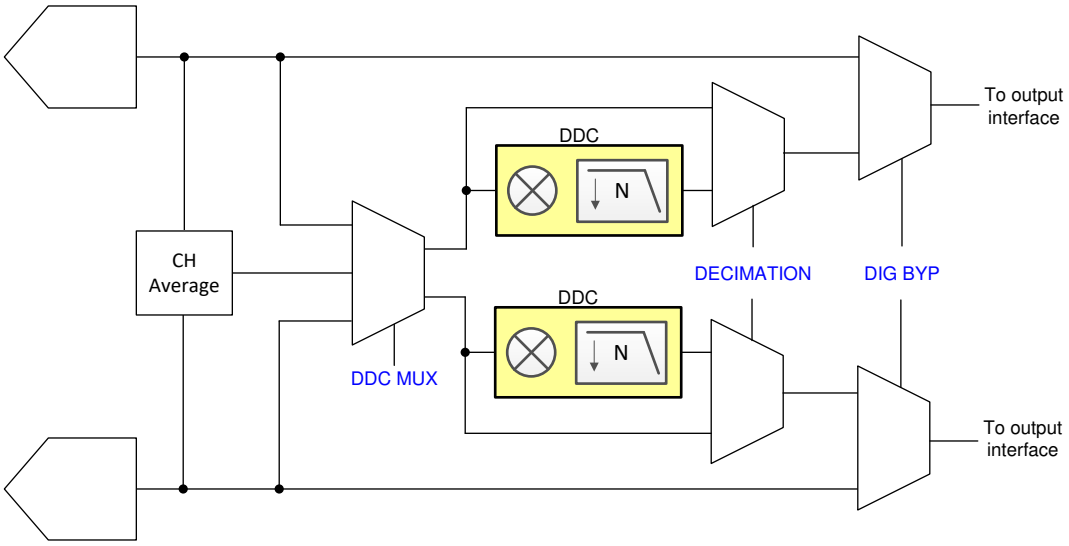


図 9-16. Register control for digital features

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図 9-17. Register 0x25

7	6	5	4	3	2	1	0
DDC MUX EN	DECIMATION			REAL OUT	0	0	MIX PHASE
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-20. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7	DDC MUX EN	R/W	0	Enables the digital mux between ADCs and decimation filters. This bit is required for DDC mux settings in register 0x24 (D4, D3) to go into effect. 0: DDC mux disabled 1: DDC mux enabled
6-4	DECIMATION	R/W	000	Complex decimation setting. This applies to both channels.
				000: Bypass mode (no decimation) 001: Decimation by 2 010: Decimation by 4 011: Decimation by 8 100: Decimation by 16 101: Decimation by 32 others: not used
3	REAL OUT	R/W	0	This bit selects real output decimation. This mode applies to both channels. In this mode, the decimation filter is a low pass filter and no complex mixing is performed to reduce power consumption. For maximum power savings the NCO in this case should be set to 0. 0: Complex decimation 1: Real decimation
2-1	0	R/W	0	Must write 0
0	MIX PHASE	R/W	0	This bit used to invert the NCO phase 0: NCO phase as is. 1: NCO phase inverted.

図 9-18. Register 0x26

7	6	5	4	3	2	1	0
MIX GAIN A		MIX RES A	FS/4 MIX A	MIX GAIN B		MIX RES B	FS/4 MIX B
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-21. Register 0x26 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	MIX GAIN A	R/W	00	This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel A. 00: no digital gain added 01: 3-dB digital gain added (should be enabled with real decimation) 10: 6-dB digital gain added (should be enabled with complex decimation) 11: not used
5	MIX RES A	R/W	0	Toggling this bit resets the NCO phase of channel A and loads the new NCO frequency. This bit does not self reset.
4	FS/4 MIX A	R/W	0	Enables FS/4 mixing for DDC A (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled.
3-2	MIX GAIN B	R/W	00	This bit applies a 0, 3 or 6-dB digital gain to the output of digital mixer to compensate for the mixing loss for channel B. 00: no digital gain added 01: 3-dB digital gain added (should be enabled with real decimation) 10: 6-dB digital gain added (should be enabled with complex decimation) 11: not used

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表 9-21. Register 0x26 Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	MIX RES B	R/W	0	Toggling this bit resets the NCO phase of channel B and loads the new NCO frequency. This bit does not self reset.
0	FS/4 MIX B	R/W	0	Enables FS/4 mixing for DDC B (complex decimation only). 0: FS/4 mixing disabled. 1: FS/4 mixing enabled.

図 9-19. Register 0x27

7	6	5	4	3	2	1	0
0	0	0	OP ORDER A	Q-DEL A	FS/4 MIX PH A	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-22. Register 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	OP ORDER A	R/W	0	Swaps the I and Q output order for channel A. See 表 9-23 for recommended settings. Only used with complex decimation. Set to 0 with real decimation. 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n]
3	Q-DEL A	R/W	0	This delays the Q-sample output of channel A by one. See 表 9-23 for recommended settings. Only used with complex decimation. Set to 0 with real decimation. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2]
2	FS/4 MIX PH A	R/W	0	Inverts the mixer phase for channel A when using FS/4 mixer. 0: Mixer phase is non-inverted 1: Mixer phase is inverted
1-0	0	R/W	0	Must write 0

表 9-23. OP-ORDER and Q-DELAY Register Settings for Complex Decimation

SLVDS INTERFACE	OP-ORDER	Q-DELAY
2-wire	1	0
1-wire	0	1
1/2-wire	1	1

図 9-20. Register 0x2A/B/C/D

7	6	5	4	3	2	1	0
NCO A [7:0]							
NCO A [15:8]							
NCO A [23:16]							
NCO A [31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-24. Register 0x2A/2B/2C/2D Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO A [31:0]	R/W	0	Sets the 32 bit NCO value for decimation filter channel A. The NCO value is $f_{NCO} \times 2^{32} / F_S$. In real decimation mode these registers are automatically set to 0.

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図 9-21. Register 0x2E

7	6	5	4	3	2	1	0
0	0	0	OP ORDER B	Q-DEL B	FS/4 MIX PH B	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-25. Register 0x2E Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	OP ORDER B	R/W	0	Swaps the I and Q output order for channel B. See 表 9-23 for recommended settings. Only used with complex decimation. Set to 0 with real decimation. 0: Output order is I[n], Q[n] 1: Output order is swapped: Q[n], I[n]
3	Q-DEL B	R/W	0	This delays the Q-sample output of channel B by one. See 表 9-23 for recommended settings. Only used with complex decimation. Set to 0 with real decimation. 0: Output order is I[n], Q[n] 1: Q-sample is delayed by 1 sample: I[n], Q[n+1], I[n+1], Q[n+2]
2	FS/4 MIX PH B	R/W	0	Inverts the mixer phase for channel B when using FS/4 mixer. 0: Mixer phase is non-inverted 1: Mixer phase is inverted
1-0	0	R/W	0	Must write 0

図 9-22. Register 0x31/32/33/34

7	6	5	4	3	2	1	0
NCO B [7:0]							
NCO B [15:8]							
NCO B [23:16]							
NCO B [31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-26. Register 0x31/32/33/34 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	NCO B [31:0]	R/W	0	Sets the 32 bit NCO value for decimation filter channel B. The NCO value is $f_{NCO} \times 2^{32} / F_S$. In real decimation mode these registers are automatically set to 0.

図 9-23. Register 0x39..0x60

7	6	5	4	3	2	1	0
OUTPUT BIT MAPPER CHA							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-27. Register 0x39..0x60 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTPUT BIT MAPPER CHA	R/W	0	These registers are used to reorder the output data bus. See the セクション 7.3.5.3 on how to program it.

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図 9-24. Register 0x61..0x88

7	6	5	4	3	2	1	0
OUTPUT BIT MAPPER CHB							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-28. Register 0x61..0x88 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OUTPUT BIT MAPPER CHB	R/W	0	These registers are used to reorder the output data bus. See the セクション 7.3.5.3 on how to program it.

図 9-25. Register 0x8F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT A	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-29. Register 0x8F Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT A	R/W	0	This bit sets the output data format for channel A. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary
0	0	R/W	0	Must write 0

図 9-26. Register 0x92

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT B	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 9-30. Register 0x92 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT B	R/W	0	This bit sets the output data format for channel B. Digital bypass register bit (0x24, D2) needs to be enabled as well. 0: 2s complement 1: Offset binary
0	0	R/W	0	Must write 0

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10 Device and Documentation Support

10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.2 サポート・リソース

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
February 2025	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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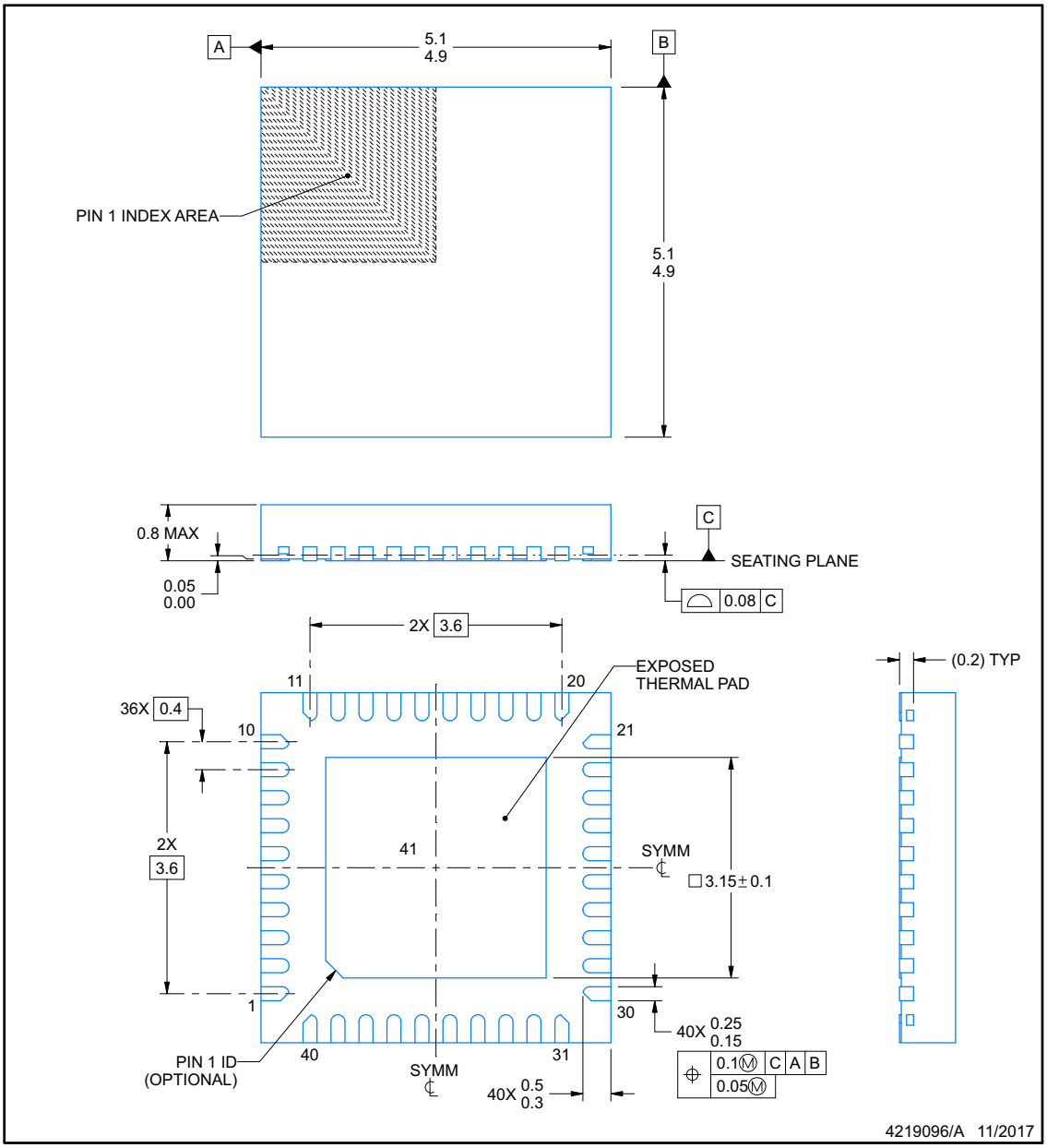
12.1 Mechanical Data

RSB0040E

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

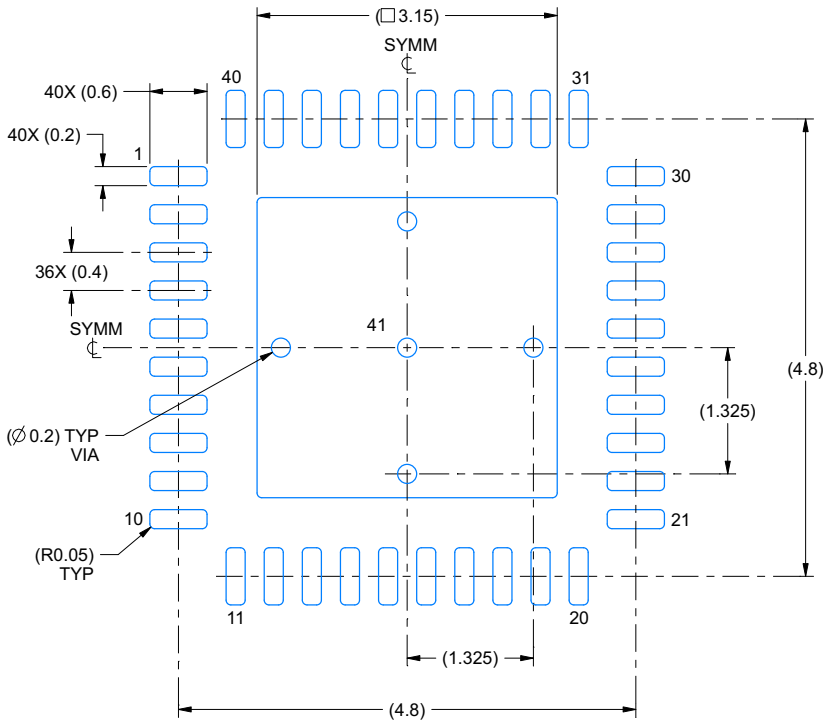
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EXAMPLE BOARD LAYOUT

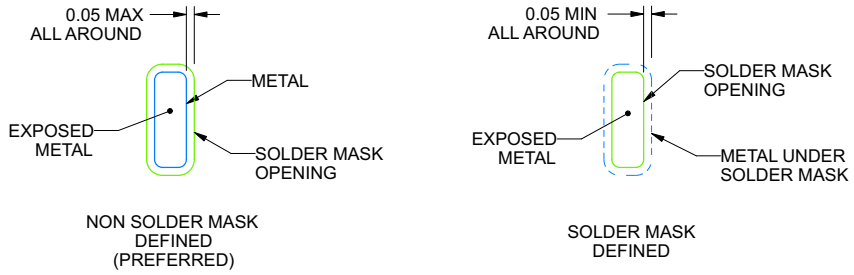
RSB0040E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219096/A 11/2017

NOTES: (continued)

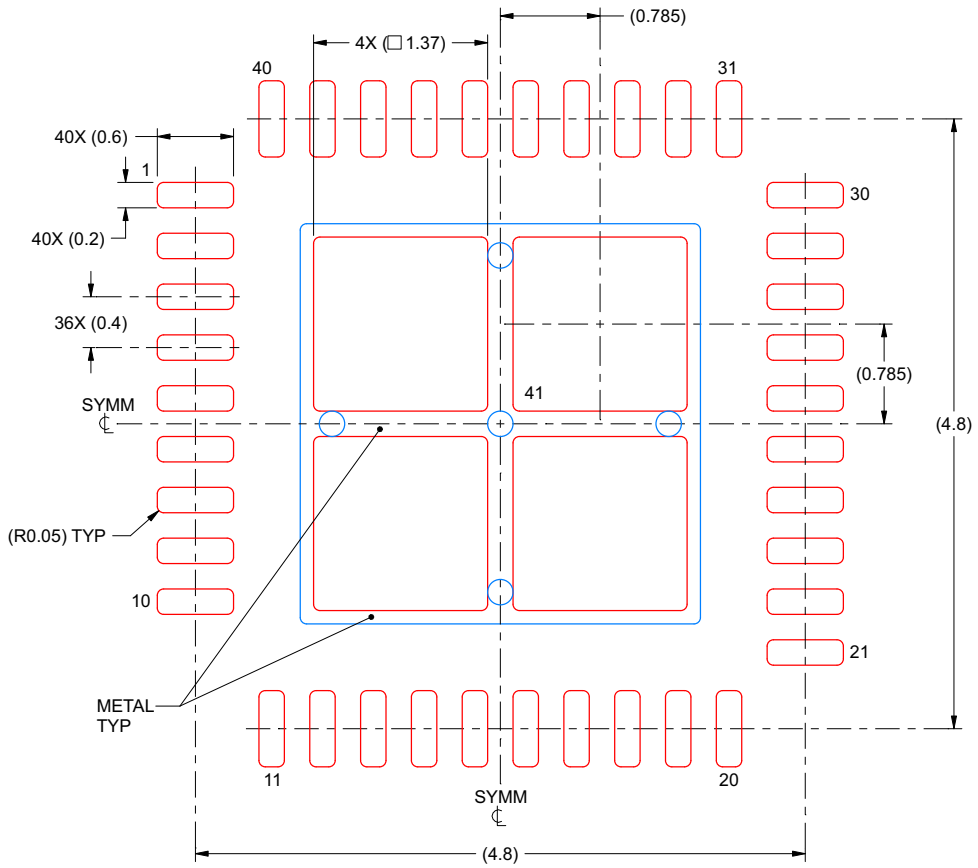
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

RSB0040E — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 41
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219096/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC3683RSBTEP	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 105	ADC3683 EP
ADC3683RSBTSEP	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 105	ADC3683 SEP
ADC3683RSBTSEP.A	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See ADC3683RSBTSEP	ADC3683 SEP
V62/24602-01XE	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See ADC3683RSBTEP	ADC3683 EP
V62/24602-02XE	Active	Production	WQFN (RSB) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See ADC3683RSBTSEP	ADC3683 SEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADC3683-EP, ADC3683-SEP :

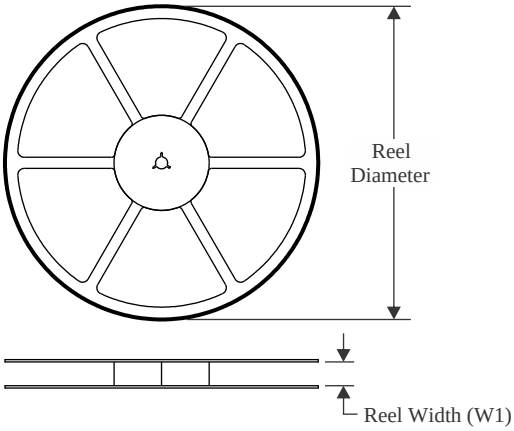
- Catalog : ADC3683
- Enhanced Product : ADC3683-EP
- Space : ADC3683-SP, ADC3683-SP

NOTE: Qualified Version Definitions:

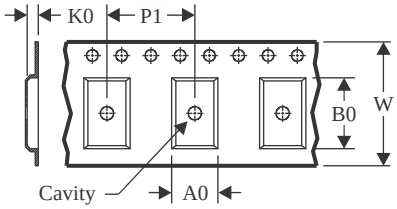
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

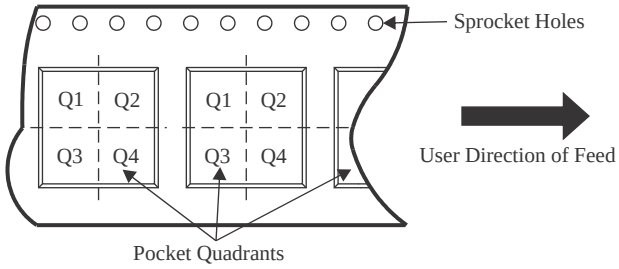


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

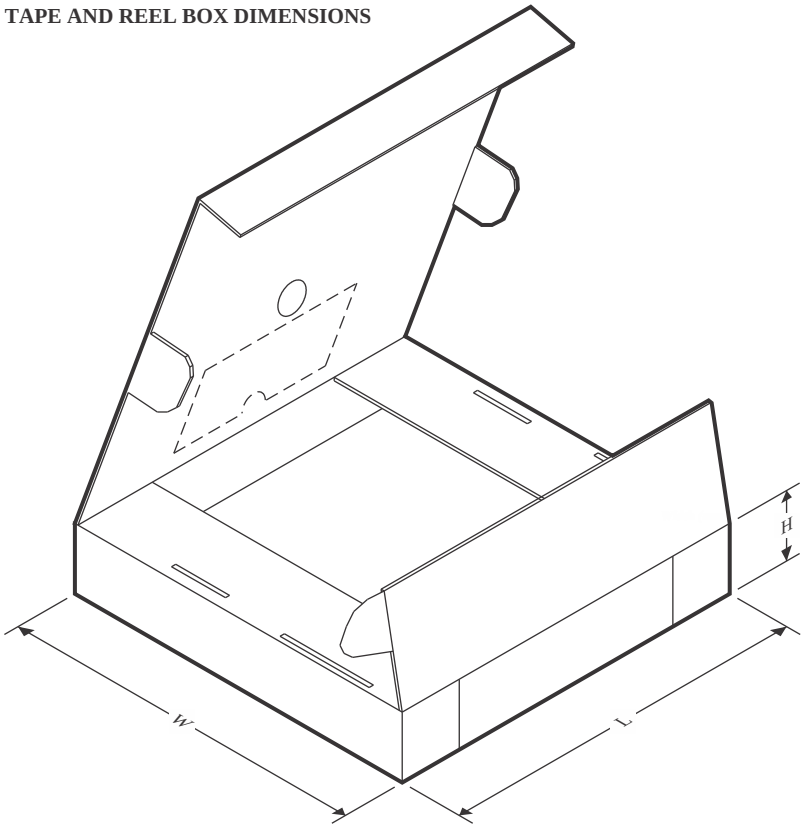
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC3683RSBTEP	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADC3683RSBTSEP	WQFN	RSB	40	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC3683RSBTEP	WQFN	RSB	40	250	210.0	185.0	35.0
ADC3683RSBTSEP	WQFN	RSB	40	250	210.0	185.0	35.0

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