ADS122C04 24ビット、4チャネル、2kSPS、I²Cインターフェイス搭載のデルタ-シグマADC

1 特長

- 315µA (標準値)の低消費電流
- 広い電源電圧範囲：2.3V～5.5V
- プログラマブル・ゲイン：1～128
- プログラマブル・データ・レート：最大2kSPS
- 最大20ビットの有効分解能
- シングル・サイクル安定化デジタル・フィルタによる50Hzおよび60Hzの同時リジェクション (20SPS)
- 2つの差動入力または4つのシングルエンド入力
- デュアル・マッチのプログラム可能電流源：10µA～1.5mA
- 内部リファレンス：2.048V、ドリフト(標準値)：5ppm/℃
- 内部オシレータ：精度2%
- 内部温度センサ：精度0.5℃(標準値)
- I²C互換インターフェイス
- サポートされるI²Cバス速度モード: Standard-Mode、Fast-Mode、Fast-Mode Plus
- 16のI²Cアドレスをピンで設定可能
- パッケージ：3.0mm × 3.0mm × 0.75mm WQFN

2 アプリケーション

- フィールド・トランスミッタ: 温度、圧力、張力、フロー
- PLCおよびDCSアナログ入力モジュール
- 温度コントローラ
- 熱メータ
- 患者モニタリング・システム：体温、血圧

3 概要

ADS122C04は、高精度の24ビット、アナログ/デジタル・コンバータ(ADC)で、小信号を測定するセンサ・アプリケーションのシステム・コストと部品点数を削減する多数の機能を統合しています。このデバイスは、柔軟な入力マルチプレクサ(MUX)を介した2つの差動入力または4つのシングルエンド入力、低ノイズのプログラマブル・ゲイン・アンプ(PGA)、2つのプログラマブル励起電流源、基準電圧、オシレータ、高精度温度センサを備えています。

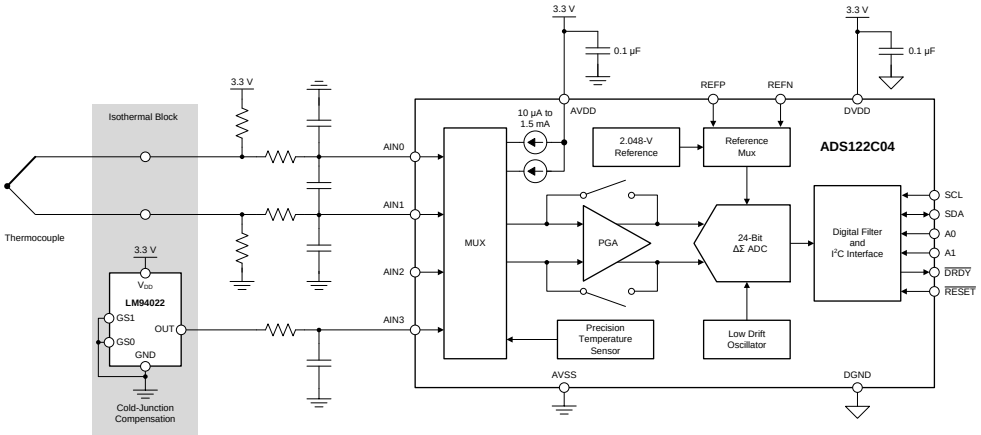
このデバイスはシングル・サイクル安定化により、最大2000サンプル/秒(SPS)のデータ・レートで変換を実行します。デジタル・フィルタはノイズの大きい工業用アプリケーションに対して、20SPSで50Hzおよび60Hzの同時リジェクションを提供します。内部PGAは最大128のゲインを提供します。このPGAを備えたADS122C04は、測温抵抗体(RTD)、熱電対、サーミスタ、抵抗性ブリッジ・センサなどの小信号を測定するセンサ・アプリケーションに最適です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS122C04	WQFN (16)	3.00mm×3.00mm
	TSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

Kタイプ熱電対温度の測定



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2018) から **Revision B** に変更 **Page**

- Changed Internal Voltage Reference, *Accuracy* parameter: added *TSSOP package* to test conditions of first row and added second row for the WQFN package ... 6
- 追加 *TSSOP package* to conditions of *Internal Reference Voltage Histogram* figure ... 14
- 変更 *Digital Supply Current vs Temperature* figure ... 17
- 削除 last sentence from first paragraph of *Pseudo Code Example* section ... 50
- 変更 *(MUX[3:1] = 1110)* to *(MUX[3:0] = 1110)* in *Pseudo Code Example* section ... 50

2017年10月発行のものから更新 **Page**

- 量産用にリリース ... 1

5 概要（続き）

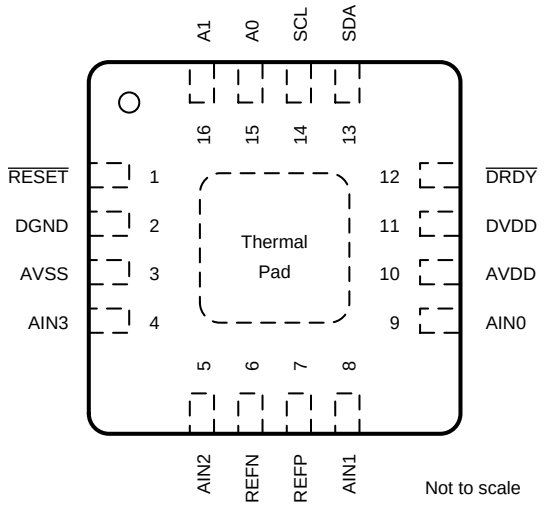
ADS122C04には2線式のI²C互換インターフェイスが搭載され、最高1MbpsのI²Cバス速度に対応します。2本のアドレス・ピンにより、16の異なるデバイスI²Cアドレスを選択できます。

ADS122C04は、16ピンのリードレスWQFNパッケージ、または16ピンTSSOPパッケージで提供されており、温度範囲-40℃～+125℃で動作が規定されています。

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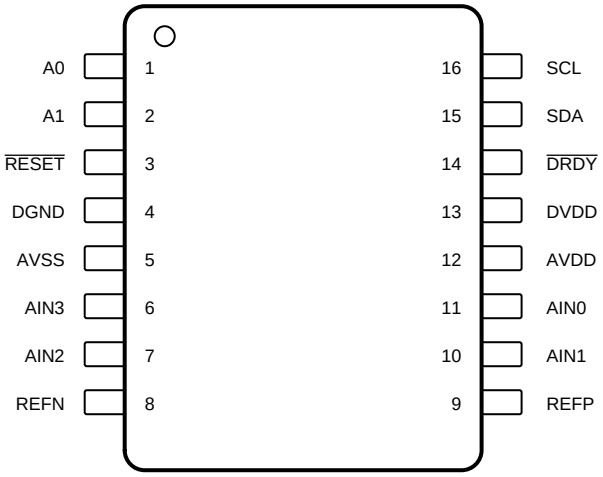
6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Not to scale

PW Package
16-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN			ANALOG OR DIGITAL INPUT/OUTPUT	DESCRIPTION(1)
NAME	NO. RTE	NO. PW		
A0	15	1	Digital input	I²C slave address select pin 0. See the *I²C Address* section for details.
A1	16	2	Digital input	I²C slave address select pin 1. See the *I²C Address* section for details.
AIN0	9	11	Analog input	Analog input 0
AIN1	8	10	Analog input	Analog input 1
AIN2	5	7	Analog input	Analog input 2
AIN3	4	6	Analog input	Analog input 3
AVDD	10	12	Analog supply	Positive analog power supply. Connect a 100-nF (or larger) capacitor to AVSS.
AVSS	3	5	Analog supply	Negative analog power supply
DGND	2	4	Digital supply	Digital ground
$\overline{\text{DRDY}}$	12	14	Digital output	Data ready, active low. Connect to DVDD using a pullup resistor.
DVDD	11	13	Digital supply	Positive digital power supply. Connect a 100-nF (or larger) capacitor to DGND.
REFN	6	8	Analog input	Negative reference input
REFP	7	9	Analog input	Positive reference input
$\overline{\text{RESET}}$	1	3	Digital input	Reset, active low
SCL	14	16	Digital input	Serial clock input. Connect to DVDD using a pullup resistor.
SDA	13	15	Digital input/output	Serial data input and output. Connect to DVDD using a pullup resistor.
Thermal pad	Pad	—	—	Thermal power pad. Connect to AVSS.

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	7	V
	DVDD to DGND	–0.3	7	
	AVSS to DGND	–2.8	0.3	
Analog input voltage	AIN0, AIN1, AIN2, AIN3, REFP, REFN	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	SCL, SDA, A0, A1, $\overline{DRDY}$, $\overline{RESET}$	DGND – 0.3	7	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Unipolar analog power supply	AVDD to AVSS	2.3		5.5	V
		AVSS to DGND	–0.1	0	0.1	
	Bipolar analog power supply	AVDD to DGND	2.3	2.5	2.75	V
		AVSS to DGND	–2.75	–2.5	–2.3	
	Digital power supply	DVDD to DGND	2.3		5.5	V
ANALOG INPUTS(1)						
$V_{(AINx)}$	Absolute input voltage(2)	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 4	AVSS + 0.2		AVDD – 0.2	
		PGA enabled, gain = 8 to 128	AVSS + 0.2 + $\lvert V_{INMAX}\rvert$·(Gain – 4) / 8		AVDD – 0.2 – $\lvert V_{INMAX}\rvert$·(Gain – 4) / 8	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINP} – V_{AINN}$(3)	$–V_{REF}$ / Gain		V_{REF} / Gain	V
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference input voltage	$V_{REF} = V_{(REFP)} – V_{(REFN)}$	0.75	2.5	AVDD – AVSS	V
$V_{(REFN)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFP)}$ – 0.75	V
$V_{(REFP)}$	Absolute positive reference voltage		$V_{(REFN)}$ + 0.75		AVDD + 0.1	V
DIGITAL INPUTS						
	Input voltage	SCL, SDA, A0, A1, $\overline{DRDY}$, 2.3 V ≤ DVDD < 3.0 V	DGND		DVDD + 0.5	V
		SCL, SDA, A0, A1, $\overline{DRDY}$, 3.0 V ≤ DVDD ≤ 5.5 V	DGND		5.5	
		$\overline{RESET}$	DGND		DVDD	
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. AINx denotes one of the four available analog inputs. *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case. See the *Low-Noise Programmable Gain Stage* section for more information.
(2) V_{INMAX} denotes the maximum differential input voltage, V_{IN}, that is expected in the application. $\lvert V_{INMAX}\rvert$ can be smaller than V_{REF} / Gain.
(3) Excluding the effects of offset and gain error.

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7.4 Thermal Information

THERMAL METRIC[1]		ADS122C04		UNIT
		WQFN (RTE)	TSSOP (PW)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	57.7	90.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.0	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	41.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.8	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.3 V to 5.5 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, all data rates, and internal reference enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current	PGA disabled, gain = 1 to 4, normal mode, V_{IN} = 0 V		±5		nA
		PGA disabled, gain = 1 to 4, turbo mode, V_{IN} = 0 V		±10		
		Gain = 1 to 128, V_{IN} = 0 V		±1		
	Absolute input current drift	PGA disabled, gain = 1 to 4, V_{IN} = 0 V		10		pA/°C
		Gain = 1 to 128, V_{IN} = 0 V		5		
	Differential input current	PGA disabled, gain = 1 to 4, normal mode, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		±5		nA
		PGA disabled, gain = 1 to 4, turbo mode, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		±10		
		Gain = 1 to 128, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		±1		
	Differential input current drift	PGA disabled, gain = 1 to 4, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		10		pA/°C
		Gain = 1 to 128, V_{CM} = AVDD / 2, $-V_{REF}$ / Gain ≤ V_{IN} ≤ V_{REF} / Gain		2		
SYSTEM PERFORMANCE						
	Resolution (no missing codes)			24		Bits
DR	Data rate	Normal mode		20, 45, 90, 175, 330, 600, 1000		SPS
		Turbo mode		40, 90, 180, 350, 660, 1200, 2000		
	Noise (input-referred)[1]	Normal mode, gain = 128, DR = 20 SPS		110		nV_{RMS}
INL	Integral nonlinearity	AVDD = 3.3 V, gain = 1 to 128, V_{CM} = AVDD / 2, external V_{REF}, normal mode, best fit	–15	±6	15	ppm_{FSR}
V_{IO}	Input offset voltage	PGA disabled, gain = 1 to 4, differential inputs		±4		µV
		Gain = 1, differential inputs, T_A = 25°C	–150	±5	150	
		Gain = 2 to 128, differential inputs		±4		
	Offset drift vs temperature	PGA disabled, gain = 1 to 4		0.02		µV/°C
		Gain = 1 to 128		0.1	0.6	
	Gain error[2]	PGA disabled, gain = 1 to 4		±0.01%		
		Gain = 1 to 32, T_A = 25°C	–0.05%	±0.01%	0.05%	
		Gain = 64 to 128, T_A = 25°C	–0.1%	±0.015%	0.1%	
	Gain drift vs temperature[2]	PGA disabled, gain = 1 to 4		0.5		ppm/°C
		Gain = 1 to 32		0.5	2	
		Gain = 64 to 128		1	4	

(1) See the *Noise Performance* section for more information.
(2) Excluding error of voltage reference.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.3 V to 5.5 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, all data rates, and internal reference enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE (continued)						
NMRR	Normal-mode rejection ratio	50 Hz ±1 Hz, DR = 20 SPS	78	88		dB
		60 Hz ±1 Hz, DR = 20 SPS	80	88		
CMRR	Common-mode rejection ratio	At dc, gain = 1, AVDD = 3.3 V	90	105		dB
		f_{CM} = 50 Hz or 60 Hz, DR = 20 SPS, AVDD = 3.3 V	105	115		
		f_{CM} = 50 Hz or 60 Hz, DR = 2 kSPS, AVDD = 3.3 V	95	110		
PSRR	Power-supply rejection ratio	AVDD at dc, V_{CM} = AVDD / 2	85	105		dB
		DVDD at dc, V_{CM} = AVDD / 2	95	115		
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Reference voltage			2.048		V
	Accuracy	T_A = 25°C, TSSOP package	–0.15%	±0.01%	0.15%	
		T_A = 25°C, WQFN package	–0.25%	±0.04%	0.25%	
	Temperature drift			5	30	ppm/°C
	Long-term drift	1000 hours		110		ppm
VOLTAGE REFERENCE INPUTS						
	Reference input current	REFP = V_{REF}, REFN = AVSS, AVDD = 3.3 V		±10		nA
INTERNAL OSCILLATOR						
f_{CLK}	Frequency	Normal mode		1.024		MHz
		Turbo mode		2.048		
	Accuracy	Normal mode	–2%	±1%	2%	
		Turbo mode	–4%	±2%	4%	
EXCITATION CURRENT SOURCES (IDACs) (AVDD = 3.3 V to 5.5 V)						
	Current settings			10, 50, 100, 250, 500, 1000, 1500		µA
	Compliance voltage	All IDAC settings			AVDD – 0.9	V
	Accuracy (each IDAC)	IDAC = 50 µA to 1.5 mA	–6%	±1%	6%	
	Current matching between IDACs	IDAC = 50 µA to 1.5 mA, T_A = 25°C		0.3%	2%	
	Temperature drift (each IDAC)	IDAC = 50 µA to 1.5 mA		50		ppm/°C
	Temperature drift matching between IDACs	IDAC = 50 µA to 1.5 mA		8	40	ppm/°C
BURN-OUT CURRENT SOURCES (BOCS)						
	Magnitude	Sink and source		10		µA
	Accuracy			±5%		
TEMPERATURE SENSOR						
	Conversion resolution			14		Bits
	Temperature resolution			0.03125		°C
	Accuracy	T_A = 0°C to +85°C	–1	±0.25	1	°C
		T_A = –40°C to +125°C	–1.5	±0.5	1.5	
	Accuracy vs analog supply voltage			0.0625	0.25	°C/V

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD = 2.3 V to 5.5 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, all data rates, and internal reference enabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.3 DVDD	V
V_{IH}	Logic input level, high	2.3 V ≤ DVDD < 3.0 V, SCL, SDA, A0, A1, $\overline{DRDY}$	0.7 DVDD		DVDD + 0.5	V
		3.0 V ≤ DVDD ≤ 5.5 V, SCL, SDA, A0, A1, $\overline{DRDY}$	0.7 DVDD		5.5	
		$\overline{RESET}$	0.7 DVDD		DVDD	
V_{hys}	Hysteresis of Schmitt-trigger inputs	Fast-mode, fast-mode plus	0.05 DVDD			V
V_{OL}	Logic output level, low	I_{OL} = 3 mA	DGND	0.15	0.4	V
I_{OL}	Low-level output current	V_{OL} = 0.4 V, standard-mode, fast-mode	3			mA
		V_{OL} = 0.4 V, fast-mode plus	20			
		V_{OL} = 0.6 V, fast-mode	6			
I_i	Input current	DGND + 0.1 V < $V_{Digital\ Input}$ < DVDD – 0.1 V	–10		10	µA
C_i	Capacitance	Each pin			10	pF
ANALOG SUPPLY CURRENT (AVDD = 3.3 V, V_{IN} = 0 V, IDACs Turned Off)						
I_{AVDD}	Analog supply current	Power-down mode		0.1	3	µA
		Normal mode, PGA disabled, gain = 1 to 4		250		
		Normal mode, gain = 1 to 16		360	510	
		Normal mode, gain = 32		455		
		Normal mode, gain = 64, 128		550		
		Turbo mode, PGA disabled, gain = 1 to 4		370		
		Turbo mode, gain = 1 to 16		580		
		Turbo mode, gain = 32		765		
		Turbo mode, gain = 64, 128		955		
ADDITIONAL ANALOG SUPPLY CURRENTS PER FUNCTION (AVDD = 3.3 V)						
I_{AVDD}	Analog supply current	External reference selected		60		µA
		IDAC overhead (excludes the actual IDAC current)		195		
DIGITAL SUPPLY CURRENT (DVDD = 3.3 V, All Data Rates, I^2C Not Active)						
I_{DVDD}	Digital supply current	Power-down mode		0.3	5	µA
		Normal mode		65	100	
		Turbo mode		100		
POWER DISSIPATION (AVDD = DVDD = 3.3 V, All Data Rates, V_{IN} = 0 V, I^2C Not Active)						
P_D	Power dissipation	Normal mode, gain = 1 to 16		1.4		mW
		Turbo mode, gain = 1 to 16		2.2		

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7.6 I²C Timing Requirements

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

			MIN	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency		0	100	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		4		µs
t_{LOW}	Pulse duration, SCL low		4.7		µs
t_{HIGH}	Pulse duration, SCL high		4.0		µs
$t_{SU;STA}$	Setup time, repeated START condition		4.7		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		250		ns
t_r	Rise time, SCL, SDA			1000	ns
t_f	Fall time, SCL, SDA			250	ns
$t_{SU;STO}$	Setup time, STOP condition		4.0		µs
t_{BUF}	Bus free time, between STOP and START condition		4.7		µs
$t_{VD;DAT}$	Valid time, data			3.45	µs
$t_{VD;ACK}$	Valid time, acknowledge			3.45	µs
FAST-MODE					
f_{SCL}	SCL clock frequency		0	400	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		0.6		µs
t_{LOW}	Pulse duration, SCL low		1.3		µs
t_{HIGH}	Pulse duration, SCL high		0.6		µs
$t_{SU;STA}$	Setup time, repeated START condition		0.6		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		100		ns
t_r	Rise time, SCL, SDA		20	300	ns
t_f	Fall time, SCL, SDA		20 · (DVDD / 5.5 V)	250	ns
$t_{SU;STO}$	Setup time, STOP condition		0.6		µs
t_{BUF}	Bus free time, between STOP and START condition		1.3		µs
$t_{VD;DAT}$	Valid time, data			0.9	µs
$t_{VD;ACK}$	Valid time, acknowledge			0.9	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency		0	1000	kHz
$t_{HD;STA}$	Hold time, (repeated) START condition. After this period, the first clock pulse is generated.		0.26		µs
t_{LOW}	Pulse duration, SCL low		0.5		µs
t_{HIGH}	Pulse duration, SCL high		0.26		µs
$t_{SU;STA}$	Setup time, repeated START condition		0.26		µs
$t_{HD;DAT}$	Hold time, data		0		µs
$t_{SU;DAT}$	Setup time, data		50		ns
t_r	Rise time, SCL, SDA			120	ns
t_f	Fall time, SCL, SDA	Pullup resistor = 350 Ω	20 · (DVDD / 5.5 V)	120	ns
$t_{SU;STO}$	Setup time, STOP condition		0.26		µs
t_{BUF}	Bus free time, between STOP and START condition		0.5		µs
$t_{VD;DAT}$	Valid time, data			0.45	µs
$t_{VD;ACK}$	Valid time, acknowledge			0.45	µs
t_{SP}	Pulse duration of spikes that must be suppressed by the input filter		0	50	ns

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I²C Timing Requirements (continued)

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

			MIN	MAX	UNIT
$\overline{\text{RESET}}$ PIN					
$t_{w(RSL)}$	Pulse duration, $\overline{\text{RESET}}$ low		250		ns
$t_{d(RSSTA)}$	Delay time, START condition after $\overline{\text{RESET}}$ rising edge(1)		100		ns
$\overline{\text{DRDY}}$ PIN					
$t_{d(DRSTA)}$	Delay time, START condition after $\overline{\text{DRDY}}$ falling edge		0		ns
TIMEOUT					
	Timeout(2)	Normal mode	14000		t_{MOD}
		Turbo mode	28000		

(1) No delay time is required when using the RESET command as long as all I²C timing requirements for the (repeated) START and STOP conditions are met.
(2) See the *Timeout* section for more information.
t_{MOD} = 1 / f_{MOD}. Modulator frequency f_{MOD} = 256 kHz (normal mode) and 512 kHz (turbo mode).

7.7 I²C Switching Characteristics

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V, bus capacitance = 10 pF to 400 pF, and pullup resistor = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(DRH)}$	Pulse duration, $\overline{\text{DRDY}}$ high(1)		2			t_{MOD}
$t_{p(RDDR)}$	Propagation delay time, RDATA command latched to $\overline{\text{DRDY}}$ rising edge			2		t_{MOD}

(1) t_{MOD} = 1 / f_{MOD}. Modulator frequency f_{MOD} = 256 kHz (normal mode) and 512 kHz (turbo mode).

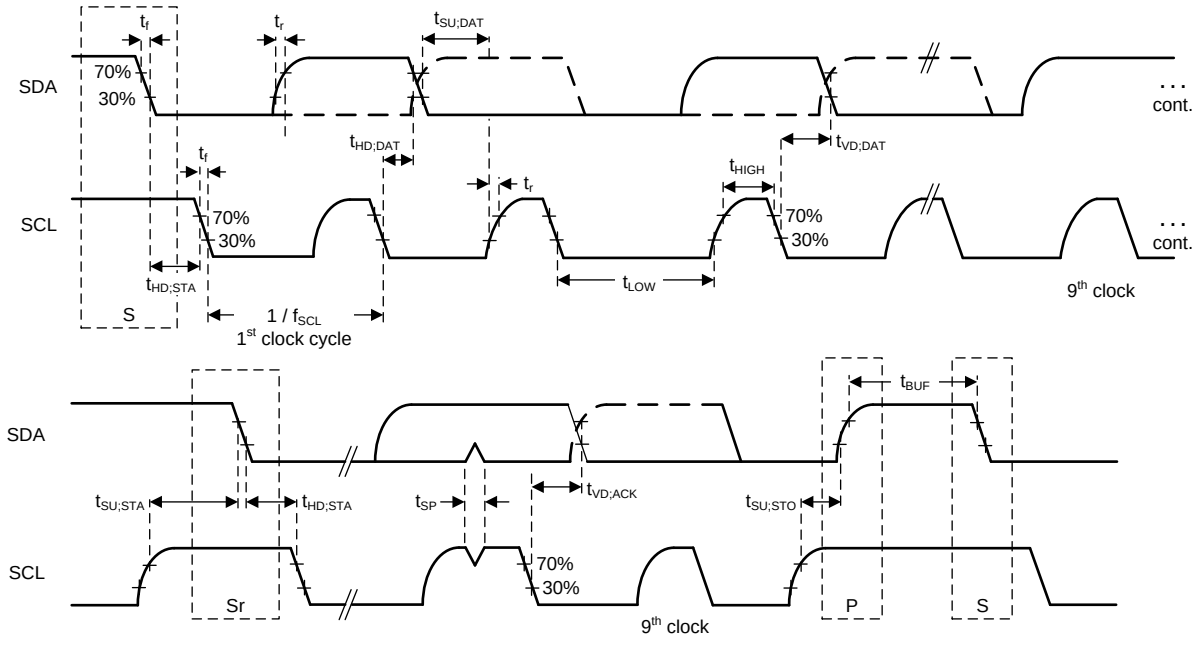


図 1. I²C Timing Requirements

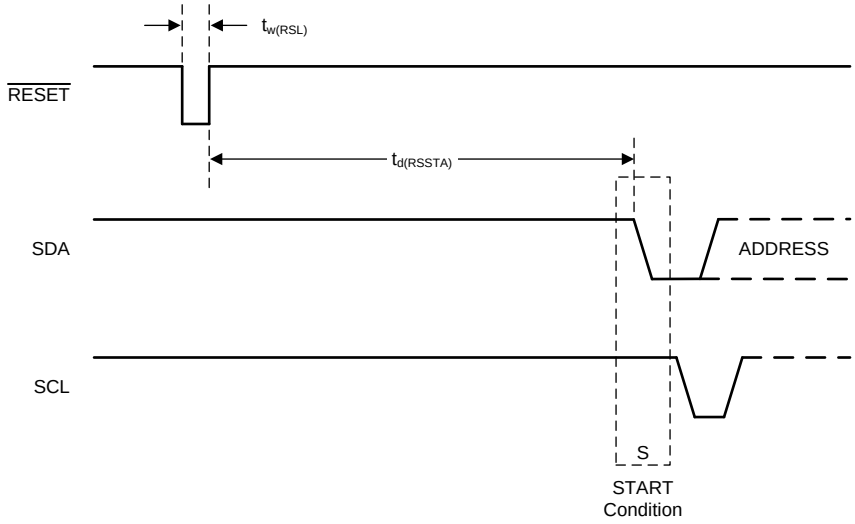


図 2. RESET Pin Timing Requirements

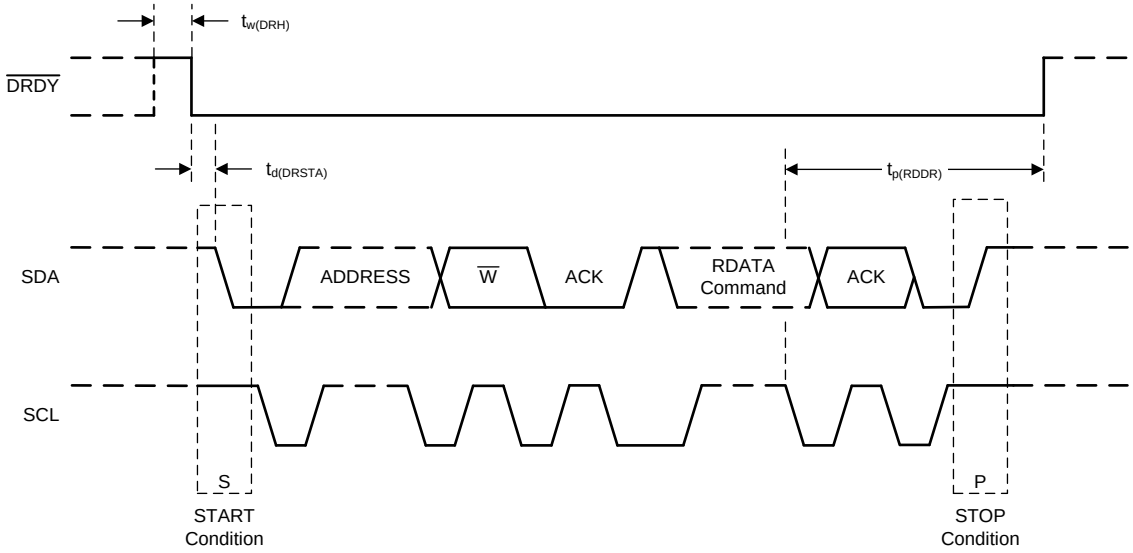
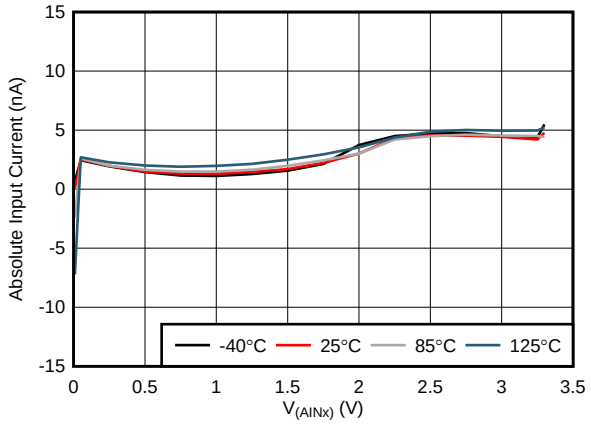


図 3. DRDY Pin Timing Requirements and Switching Characteristics

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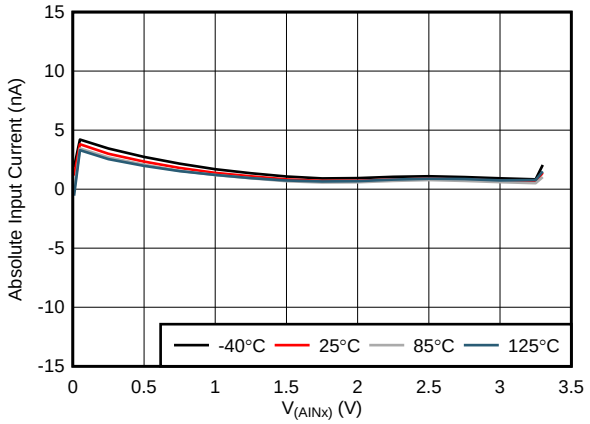
7.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)



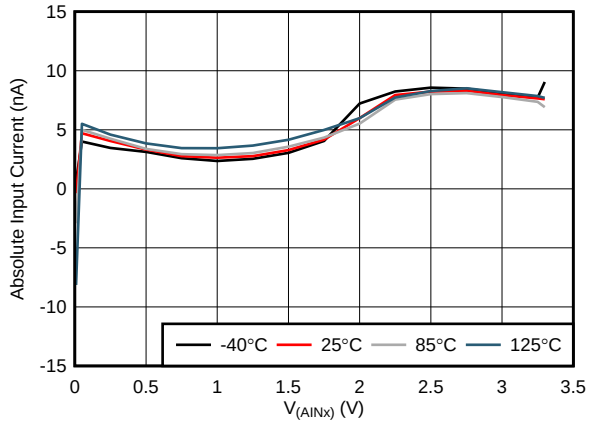
Normal mode, PGA disabled, V_{IN} = 0 V

図 4. Absolute Input current vs Absolute Input Voltage



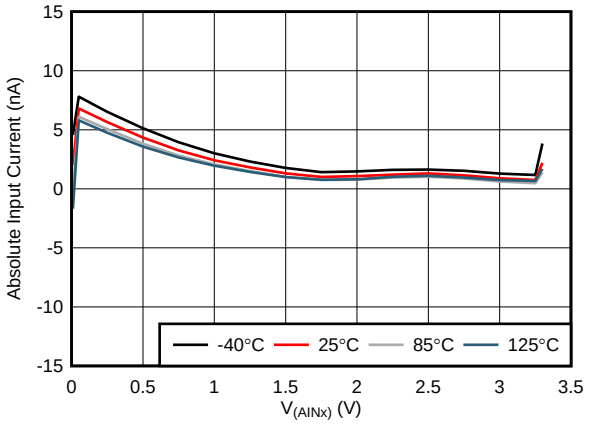
Normal mode, PGA enabled, V_{IN} = 0 V

図 5. Absolute Input Current vs Absolute Input Voltage



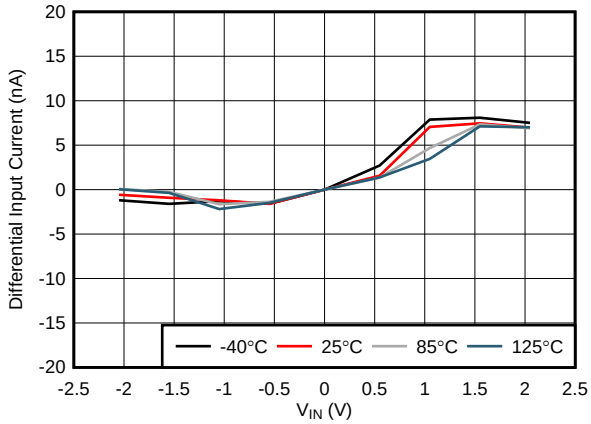
Turbo mode, PGA disabled, V_{IN} = 0 V

図 6. Absolute Input Current vs Absolute Input Voltage



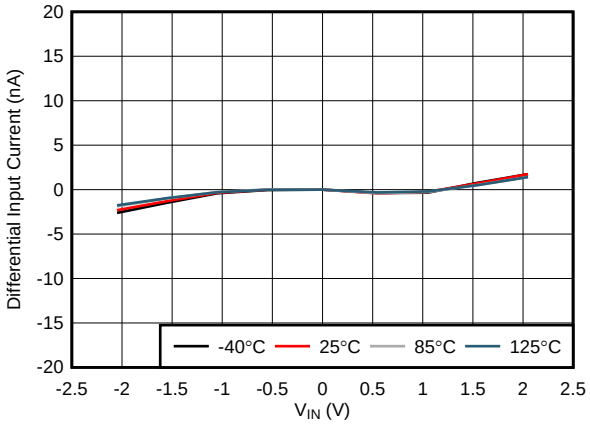
Turbo mode, PGA enabled, V_{IN} = 0 V

図 7. Absolute Input Current vs Absolute Input Voltage



Normal mode, PGA disabled, V_{CM} = 1.65 V

図 8. Differential Input Current vs Differential Input Voltage



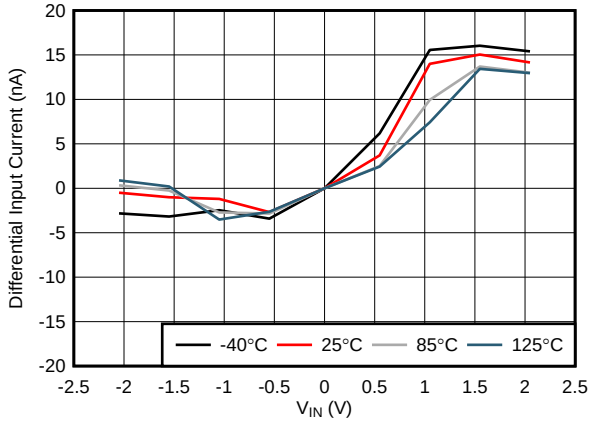
Normal mode, PGA enabled, V_{CM} = 1.65 V

図 9. Differential Input Current vs Differential Input Voltage

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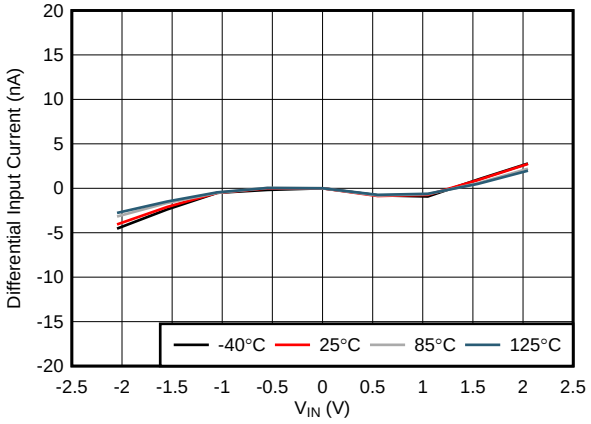
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)



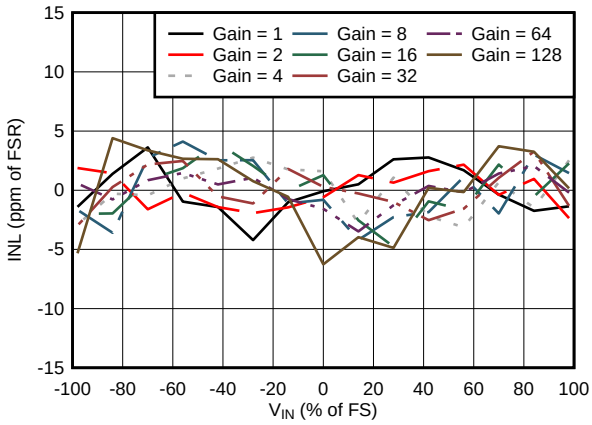
Turbo mode, PGA disabled, V_{CM} = 1.65 V

図 10. Differential Input Current vs Differential Input Voltage



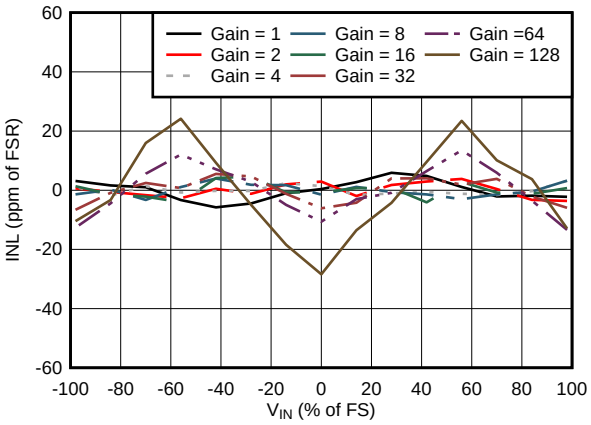
Turbo mode, PGA enabled, V_{CM} = 1.65 V

図 11. Differential Input Current vs Differential Input Voltage



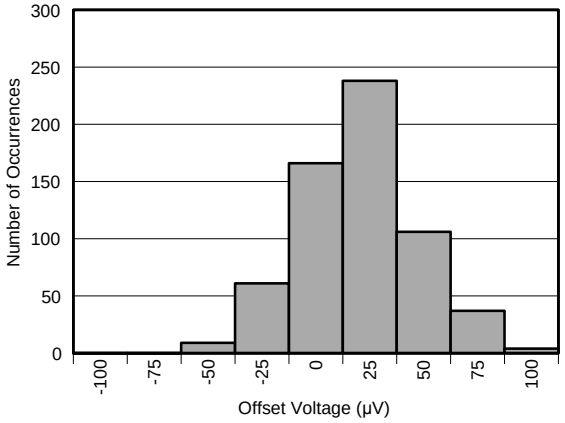
PGA enabled, external reference, best fit

図 12. INL vs Differential Input Voltage



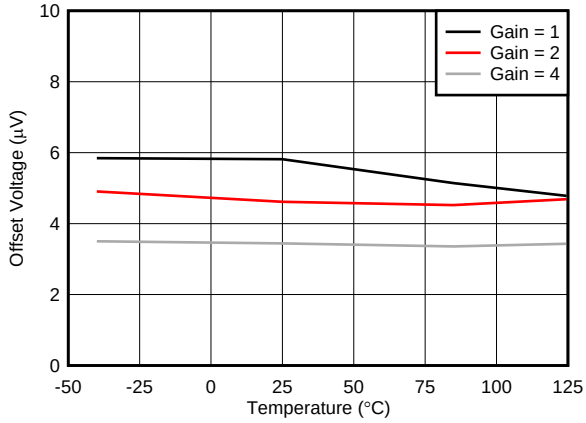
PGA enabled, internal reference, best fit

図 13. INL vs Differential Input Voltage



PGA enabled, gain = 1, 620 samples

図 14. Offset Voltage Histogram



PGA disabled

図 15. Input Offset Voltage vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)

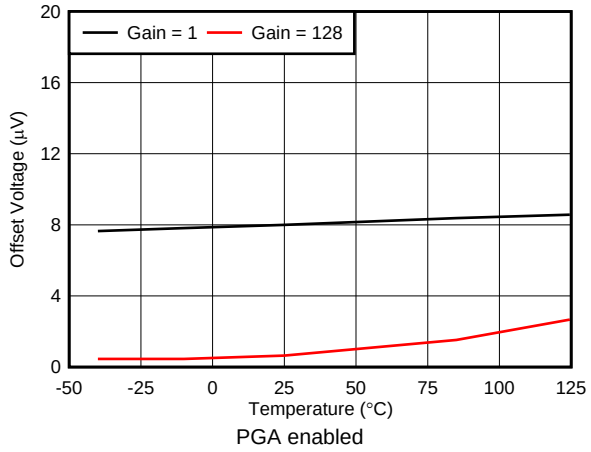


図 16. Input Offset Voltage vs Temperature

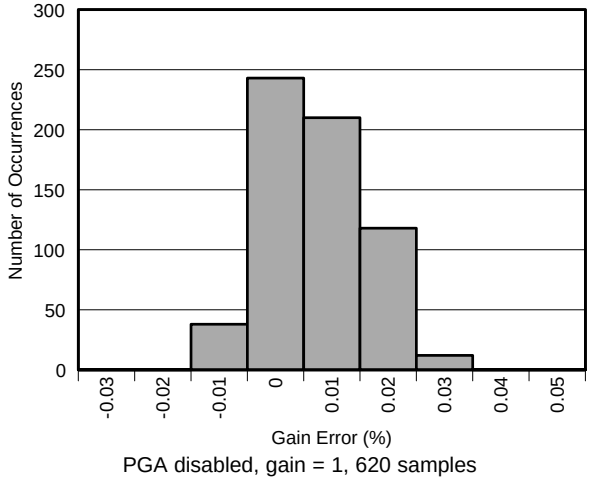


図 17. Gain Error Histogram

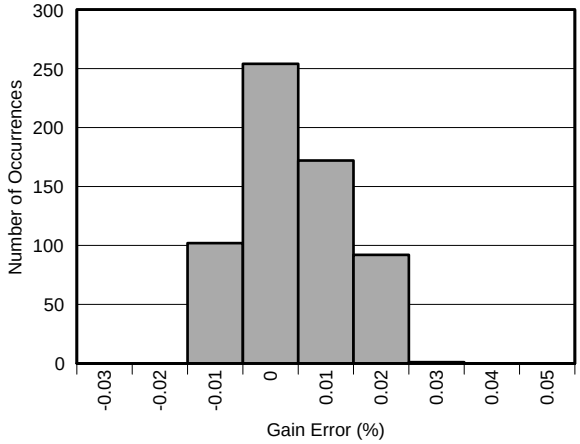


図 18. Gain Error Histogram

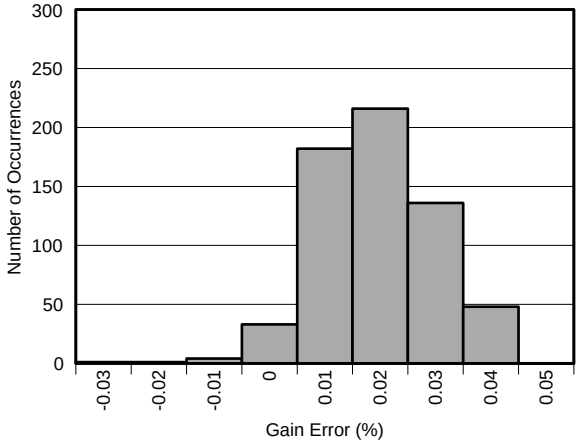


図 19. Gain Error Histogram

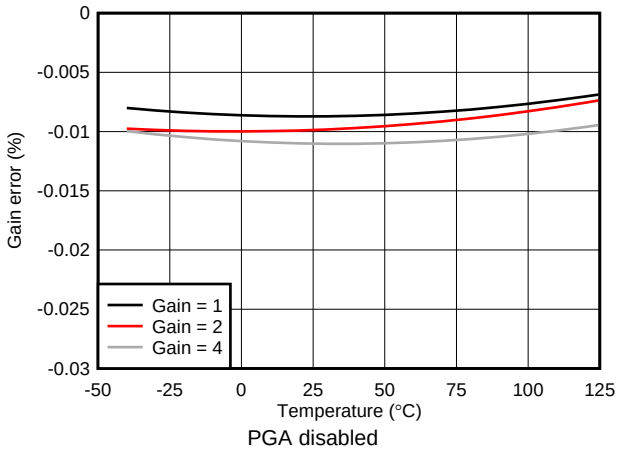


図 20. Gain Error vs Temperature

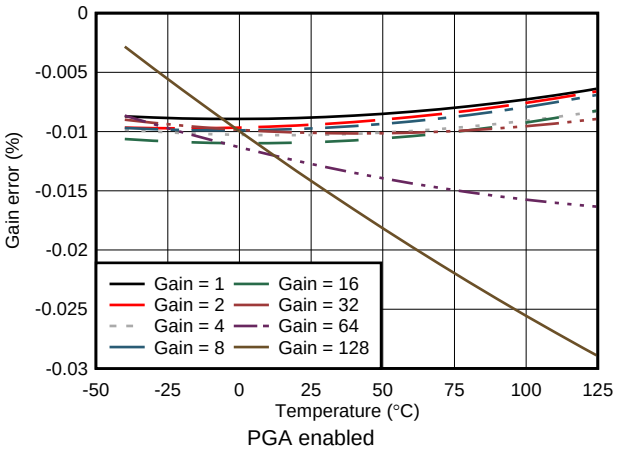


図 21. Gain Error vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)

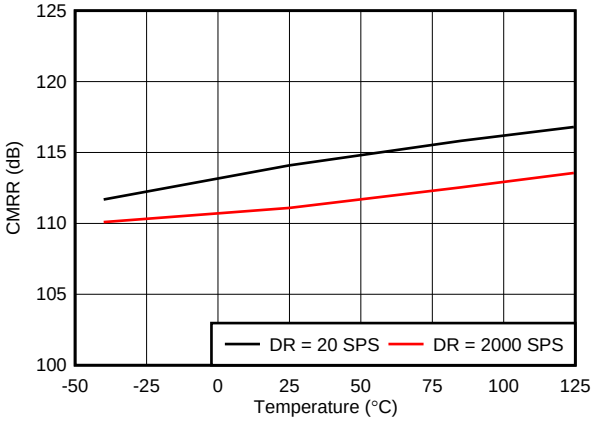


図 22. DC CMRR vs Temperature

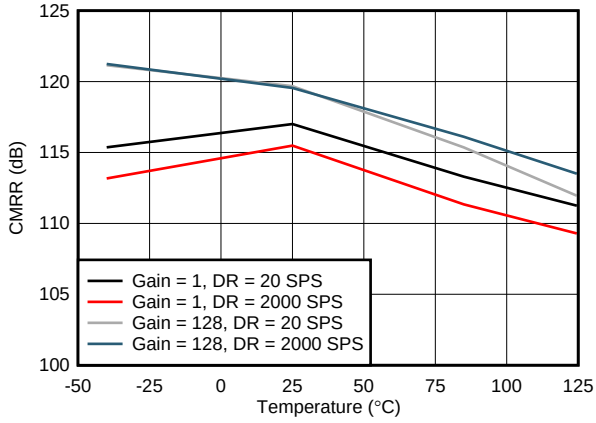


図 23. DC CMRR vs Temperature

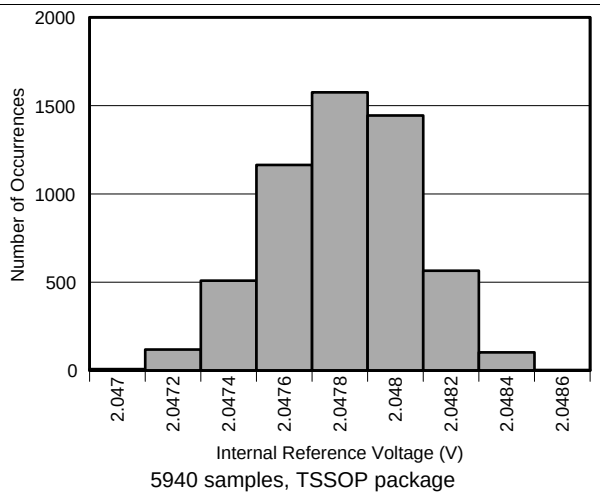


図 24. Internal Reference Voltage Histogram

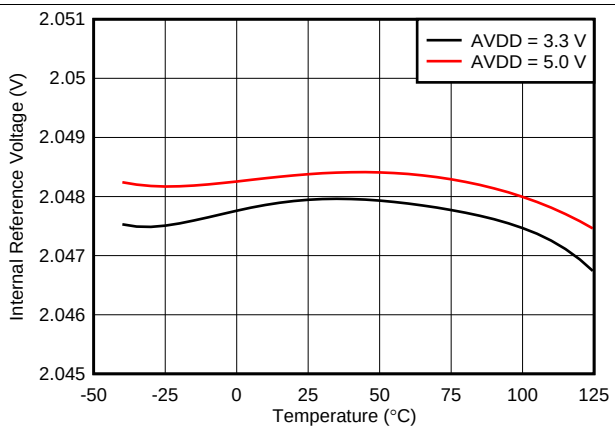


図 25. Internal Reference Voltage vs Temperature

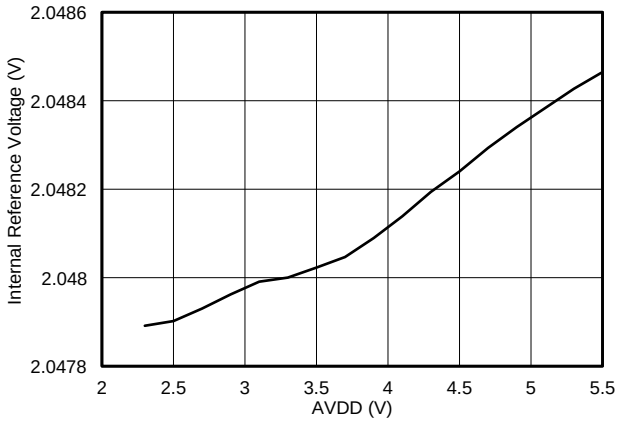


図 26. Internal Reference Voltage vs AVDD

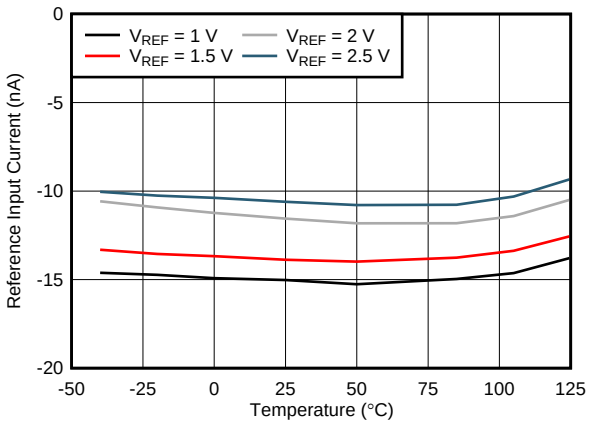


図 27. External Reference Input Current vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)

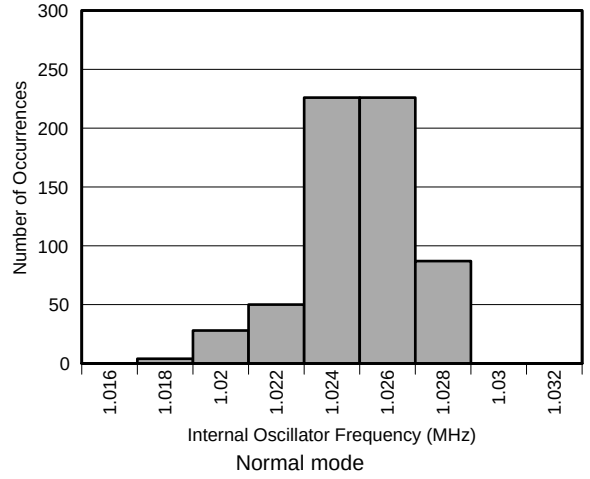


図 28. Internal Oscillator Frequency Histogram

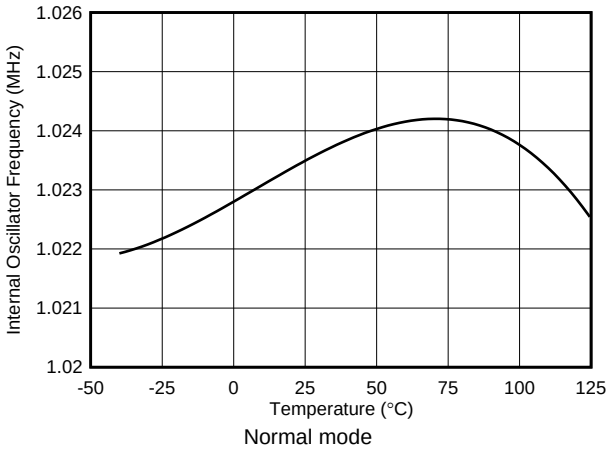


図 29. Internal Oscillator Frequency vs Temperature

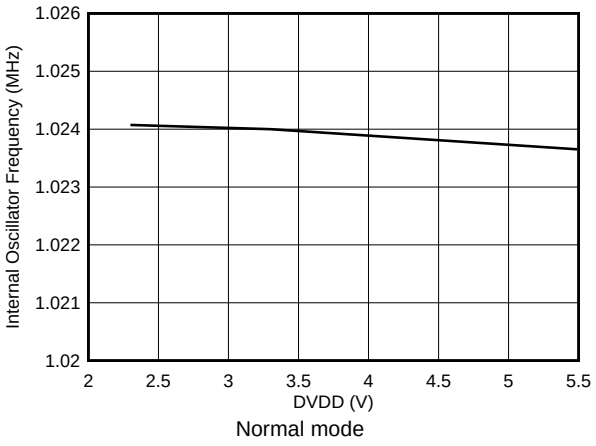


図 30. Internal Oscillator Frequency vs DVDD

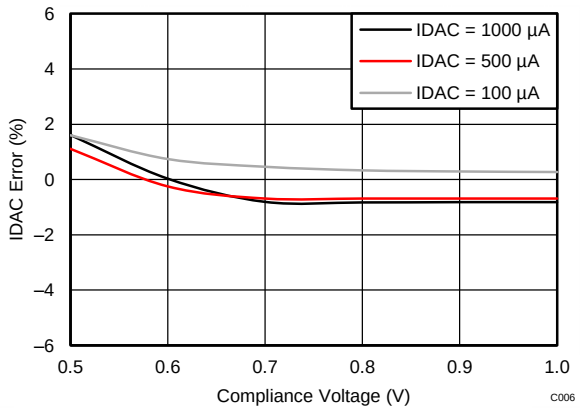


図 31. IDAC Accuracy vs Compliance Voltage

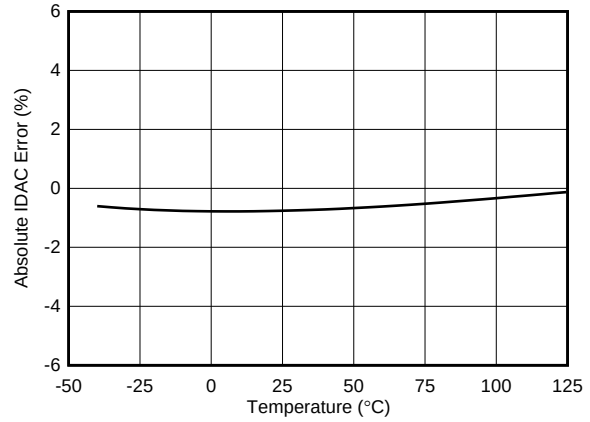


図 32. IDAC Accuracy vs Temperature

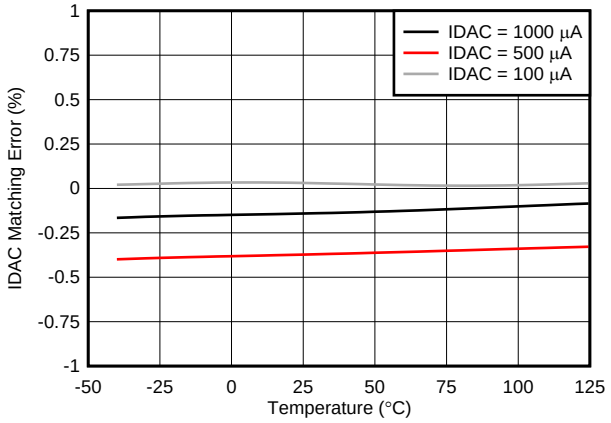


図 33. IDAC Matching vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)

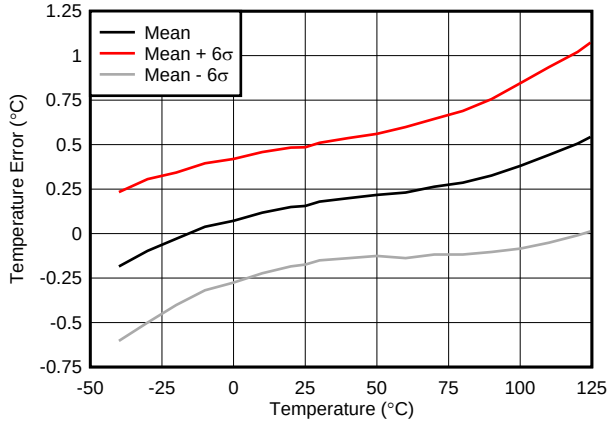


図 34. Internal Temperature Sensor Accuracy vs Temperature

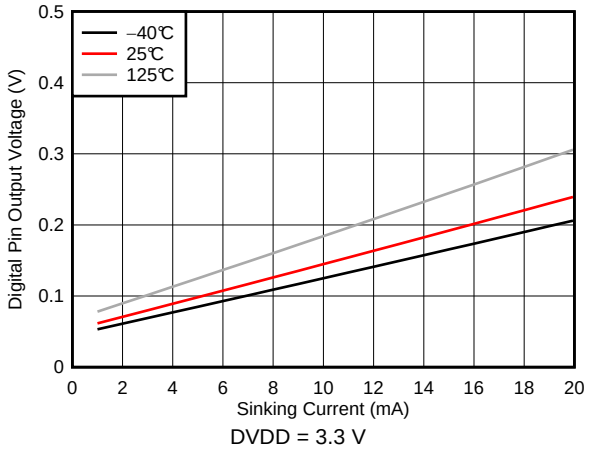


図 35. Digital Pin Output Voltage vs Sinking Current

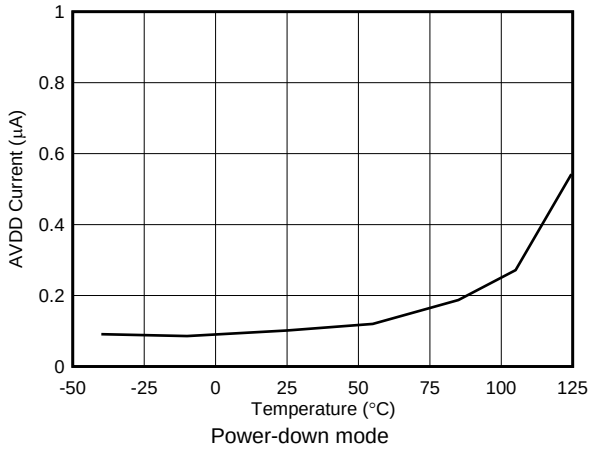


図 36. Analog Supply Current vs Temperature

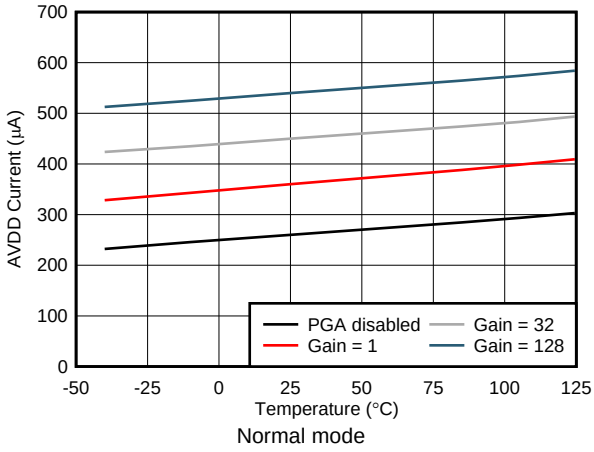


図 37. Analog Supply Current vs Temperature

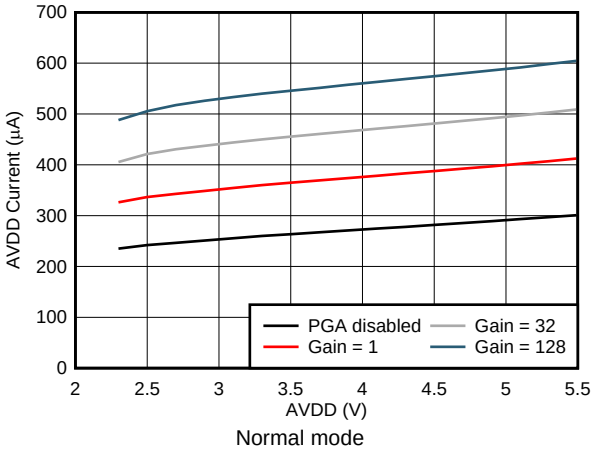


図 38. Analog Supply Current vs AVDD

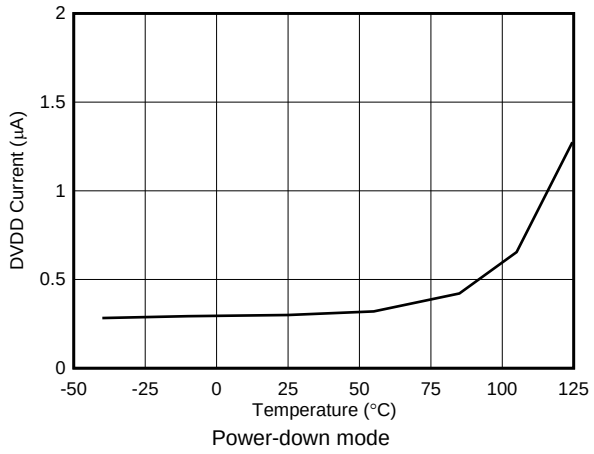


図 39. Digital Supply Current vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, and AVSS = 0 V using internal V_{REF} = 2.048 V (unless otherwise noted)

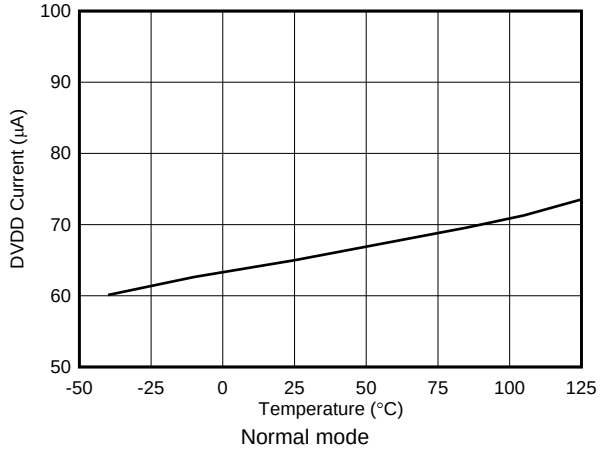


図 40. Digital Supply Current vs Temperature

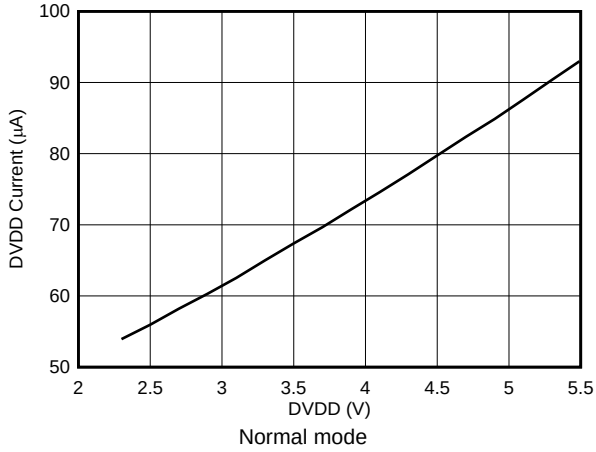


図 41. Digital Supply Current vs DVDD

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8 Parameter Measurement Information

8.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

表 1 to 表 8 summarize the device noise performance. Data are representative of typical noise performance at T_A = 25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together. 表 1, 表 3, 表 5, and 表 7 list the input-referred noise in units of μV_{RMS} for the conditions shown. Values in μV_{PP} are shown in parenthesis. 表 2, 表 4, 表 6, and 表 8 list the corresponding data in effective resolution calculated from μV_{RMS} values using 式 1. Noise-free resolution calculated from peak-to-peak noise values using 式 2 are shown in parenthesis.

The input-referred noise (表 1, 表 3, 表 5, and 表 7) only changes marginally when using an external low-noise reference, such as the REF5020. Use 式 1 and 式 2 to calculate effective resolution numbers and noise-free resolution when using a reference voltage other than 2.048 V:

$$\text{Effective Resolution} = \ln\left[2 \cdot V_{REF} / (\text{Gain} \cdot V_{RMS\text{-}Noise})\right] / \ln(2) \quad (1)$$

$$\text{Noise-Free Resolution} = \ln\left[2 \cdot V_{REF} / (\text{Gain} \cdot V_{PP\text{-}Noise})\right] / \ln(2) \quad (2)$$

表 1. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	5.10 (21.69)	2.49 (10.71)	1.25 (5.74)	0.64 (2.92)	0.41 (1.52)	0.24 (0.98)	0.14 (0.54)	0.11 (0.46)
45	6.53 (29.99)	3.02 (14.47)	1.67 (6.80)	0.93 (4.00)	0.52 (2.43)	0.28 (1.39)	0.17 (0.71)	0.13 (0.57)
90	9.01 (41.61)	4.67 (24.36)	2.41 (10.95)	1.24 (6.54)	0.73 (3.46)	0.41 (2.06)	0.25 (1.20)	0.19 (0.91)
175	12.78 (63.79)	6.75 (37.30)	3.26 (17.00)	1.92 (9.81)	1.02 (5.27)	0.60 (3.32)	0.35 (1.93)	0.25 (1.49)
330	17.75 (107.88)	8.75 (48.95)	4.72 (28.25)	2.62 (14.47)	1.42 (8.06)	0.85 (4.64)	0.50 (2.93)	0.37 (1.91)
600	24.73 (153.77)	12.89 (76.01)	6.81 (38.94)	3.84 (22.30)	2.02 (12.07)	1.18 (6.69)	0.70 (4.49)	0.51 (3.14)
1000	36.90 (228.90)	18.07 (108.90)	9.48 (58.24)	5.49 (31.55)	2.86 (17.41)	1.65 (10.23)	1.04 (6.21)	0.73 (4.69)

表 2. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Enabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	19.62 (17.53)	19.65 (17.54)	19.64 (17.44)	19.61 (17.22)	19.25 (17.36)	19.02 (16.99)	18.80 (16.85)	18.15 (16.09)
45	19.26 (17.06)	19.37 (17.11)	19.23 (17.20)	19.07 (16.94)	18.91 (16.68)	18.80 (16.49)	18.52 (16.46)	17.91 (15.78)
90	18.79 (16.59)	18.74 (16.36)	18.70 (16.51)	18.66 (16.23)	18.42 (16.18)	18.25 (15.92)	17.97 (15.70)	17.36 (15.10)
175	18.29 (15.97)	18.21 (15.74)	18.26 (15.88)	18.02 (15.48)	17.94 (15.57)	17.70 (15.23)	17.48 (15.02)	16.97 (14.39)
330	17.82 (15.21)	17.84 (15.35)	17.73 (15.12)	17.58 (15.15)	17.46 (14.96)	17.20 (14.75)	16.97 (14.41)	16.40 (14.03)
600	17.34 (14.70)	17.28 (14.72)	17.20 (14.68)	17.02 (14.70)	16.95 (14.37)	16.73 (14.22)	16.46 (13.80)	15.94 (13.32)
1000	16.76 (14.13)	16.79 (14.20)	16.72 (14.10)	16.51 (13.99)	16.45 (13.99)	16.24 (13.61)	15.91 (13.33)	15.42 (12.74)

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表 3. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Disabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Disabled)		
	1	2	4
20	5.04 (19.71)	2.53 (10.06)	1.57 (5.68)
45	6.57 (33.34)	3.43 (14.00)	1.60 (6.98)
90	8.75 (42.59)	4.35 (22.83)	2.13 (10.52)
175	12.64 (65.71)	6.27 (35.00)	3.40 (16.83)
330	18.58 (106.06)	9.33 (52.59)	4.54 (26.30)
600	25.74 (150.81)	12.57 (79.15)	6.47 (36.87)
1000	36.98 (221.61)	18.67 (111.61)	9.27 (55.07)

表 4. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Normal Mode, PGA Disabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Disabled)		
	1	2	4
20	19.63 (17.66)	19.63 (17.64)	19.32 (17.46)
45	19.25 (16.91)	19.19 (17.16)	19.29 (17.16)
90	18.84 (16.55)	18.84 (16.45)	18.87 (16.57)
175	18.31 (15.93)	18.32 (15.84)	18.20 (15.89)
330	17.75 (15.24)	17.74 (15.25)	17.78 (15.25)
600	17.28 (14.73)	17.31 (14.66)	17.27 (14.76)
1000	16.76 (14.17)	16.74 (14.16)	16.75 (14.18)

表 5. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, Turbo Mode, PGA Enabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
40	4.41 (19.43)	2.25 (10.62)	1.12 (5.32)	0.63 (2.74)	0.36 (1.64)	0.22 (1.10)	0.13 (0.63)	0.10 (0.51)
90	5.76 (30.73)	2.98 (14.16)	1.62 (7.84)	0.92 (4.43)	0.52 (2.59)	0.31 (1.59)	0.18 (0.97)	0.15 (0.76)
180	8.49 (44.61)	4.48 (22.25)	2.29 (13.23)	1.34 (6.83)	0.71 (4.11)	0.43 (2.49)	0.28 (1.51)	0.22 (1.05)
350	12.77 (71.04)	6.33 (37.00)	3.33 (19.17)	1.89 (10.76)	1.04 (5.91)	0.61 (3.54)	0.41 (2.13)	0.29 (1.64)
660	17.10 (105.64)	9.04 (54.97)	4.51 (27.74)	2.84 (16.98)	1.42 (8.45)	0.86 (5.07)	0.57 (3.32)	0.41 (2.38)
1200	25.26 (153.74)	12.51 (78.75)	6.58 (39.68)	3.90 (23.84)	2.11 (13.19)	1.23 (7.46)	0.81 (5.17)	0.58 (3.50)
2000	35.35 (226.39)	17.82 (112.98)	9.40 (59.37)	5.37 (32.97)	3.02 (18.73)	1.76 (11.12)	1.12 (7.06)	0.83 (5.41)

表 6. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Turbo Mode, PGA Enabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
40	19.83 (17.69)	19.80 (17.56)	19.80 (17.55)	19.63 (17.51)	19.44 (17.25)	19.15 (16.83)	18.91 (16.63)	18.29 (15.94)
90	19.44 (17.02)	19.39 (17.14)	19.27 (16.99)	19.09 (16.82)	18.91 (16.59)	18.66 (16.30)	18.44 (16.01)	17.70 (15.36)
180	18.88 (16.49)	18.80 (16.49)	18.77 (16.24)	18.54 (16.19)	18.46 (15.93)	18.18 (15.65)	17.80 (15.37)	17.15 (14.90)
350	18.29 (15.82)	18.30 (15.76)	18.23 (15.71)	18.05 (15.55)	17.91 (15.40)	17.68 (15.14)	17.25 (14.87)	16.75 (14.25)
660	17.87 (15.24)	17.79 (15.19)	17.79 (15.17)	17.46 (14.88)	17.46 (14.89)	17.18 (14.62)	16.78 (14.23)	16.25 (13.71)
1200	17.31 (14.70)	17.32 (14.67)	17.25 (14.66)	17.00 (14.39)	16.89 (14.24)	16.67 (14.07)	16.27 (13.60)	15.75 (13.16)
2000	16.82 (14.14)	16.81 (14.15)	16.73 (14.07)	16.54 (13.92)	16.37 (13.74)	16.15 (13.49)	15.80 (13.15)	15.23 (12.53)

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表 7. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, Turbo Mode, PGA Disabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Disabled)		
	1	2	4
40	4.30 (18.73)	2.18 (9.84)	1.10 (5.38)
90	6.19 (32.78)	3.14 (13.53)	1.42 (7.19)
180	9.08 (47.57)	4.49 (25.48)	2.18 (10.96)
350	12.40 (72.79)	5.89 (33.34)	3.07 (18.31)
660	17.59 (103.97)	9.05 (51.15)	4.39 (24.69)
1200	24.67 (149.07)	12.56 (76.35)	6.31 (37.48)
2000	34.54 (224.19)	17.76 (113.98)	8.85 (56.87)

表 8. Effective Resolution From RMS Noise (Noise-Free Resolution From Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, Turbo Mode, PGA Disabled, and Internal V_{REF} = 2.048 V

DATA RATE (SPS)	GAIN (PGA Disabled)		
	1	2	4
40	19.86 (17.74)	19.84 (17.67)	19.83 (17.54)
90	19.34 (16.93)	19.32 (17.21)	19.46 (17.12)
180	18.78 (16.39)	18.80 (16.29)	18.84 (16.51)
350	18.33 (15.78)	18.41 (15.91)	18.34 (15.77)
660	17.83 (15.27)	17.79 (15.29)	17.83 (15.34)
1200	17.34 (14.75)	17.32 (14.71)	17.31 (14.74)
2000	16.86 (14.16)	16.82 (14.13)	16.82 (14.14)

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9 Detailed Description

9.1 Overview

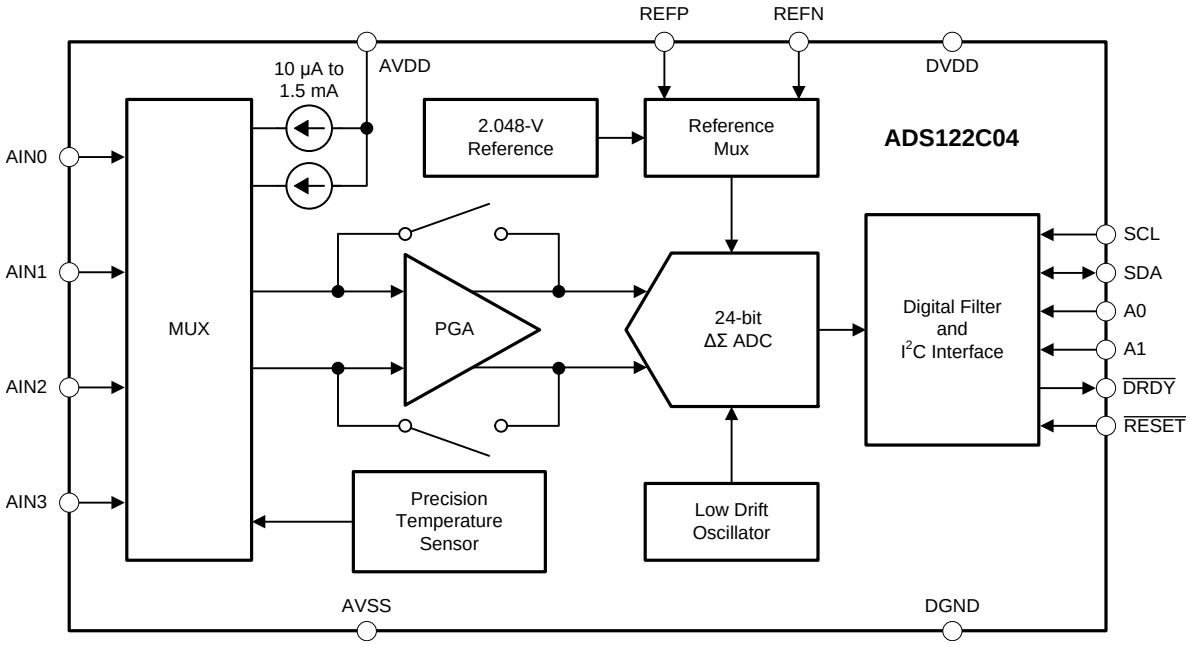
The ADS122C04 is a small, low-power, 24-bit, ΔΣ ADC that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals.

In addition to the ΔΣ ADC core and single-cycle settling digital filter, the device offers a low-noise, high input impedance, programmable gain amplifier (PGA), an internal 2.048-V voltage reference, and a clock oscillator. The device also integrates a highly linear and accurate temperature sensor as well as two matched programmable current sources (IDACs) for sensor excitation. All of these features are intended to reduce the required external circuitry in typical sensor applications and improve overall system performance. The device is fully configured through four registers and controlled by six commands through an I^2C-compatible interface. The *Functional Block Diagram* section shows the device functional block diagram.

The ADS122C04 ADC measures a differential signal, V_{IN}, which is the difference in voltage between nodes AIN_P and AIN_N. The converter core consists of a differential, switched-capacitor, ΔΣ modulator followed by a digital filter. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. This architecture results in a very strong attenuation of any common-mode signal.

The device has two available conversion modes: single-shot conversion and continuous conversion mode. In single-shot conversion mode, the ADC performs one conversion of the input signal upon request and stores the value in an internal data buffer. The device then enters a low-power state to save power. Single-shot conversion mode is intended to provide significant power savings in systems that require only periodic conversions, or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. New data are available at the programmed data rate. Data can be read at any time without concern of data corruption and always reflect the most recently completed conversion.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Multiplexer

図 42 shows the flexible input multiplexer of the device. Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The multiplexer is configured by four bits (MUX[3:0]) in the configuration register. When single-ended signals are measured, the negative ADC input (AIN_N) is internally connected to AVSS by a switch within the multiplexer. For system-monitoring purposes, the analog supply [(AVDD – AVSS) / 4] or the currently selected external reference voltage [(V_{REFP} – V_{REFN}) / 4] can be selected as inputs to the ADC. The multiplexer also offers the possibility to route any of the two programmable current sources to any analog input (AINx) or to the dedicated reference pins (REFP, REFN).

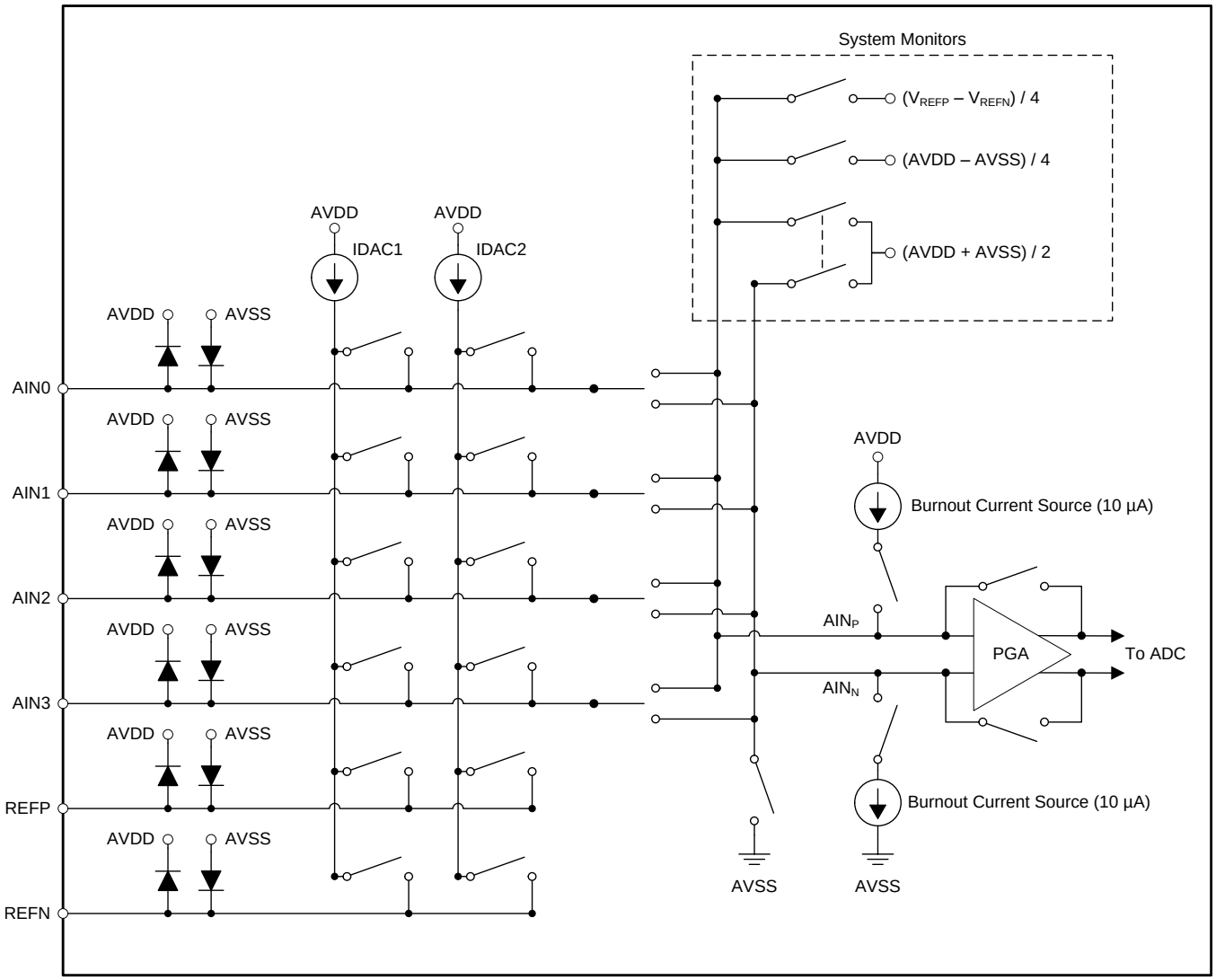


図 42. Analog Input Multiplexer

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. The absolute voltage on any input must stay within the range provided by 式 3 to prevent the ESD diodes from turning on:

$$AVSS - 0.3\ V < V_{(AINx)} < AVDD + 0.3\ V \quad (3)$$

If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unused input on the device can affect conversions taking place on other input pins.

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Feature Description (continued)

9.3.2 Low-Noise Programmable Gain Stage

The device features programmable gains of 1, 2, 4, 8, 16, 32, 64, and 128. Three bits (GAIN[2:0]) in the configuration register are used to configure the gain. Gains are achieved in two stages. The first stage is a low-noise, low-drift, high input impedance, programmable gain amplifier (PGA). The second gain stage is implemented by a switched-capacitor circuit at the input to the ΔΣ modulator. 表 9 shows how each gain is implemented.

表 9. Gain Implementation

GAIN SETTING	PGA GAIN	SWITCHED-CAPACITOR GAIN
1	1	1
2	1	2
4	1	4
8	2	4
16	4	4
32	8	4
64	16	4
128	32	4

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The input is equipped with an electromagnetic interference (EMI) filter. 図 43 shows a simplified diagram of the PGA.

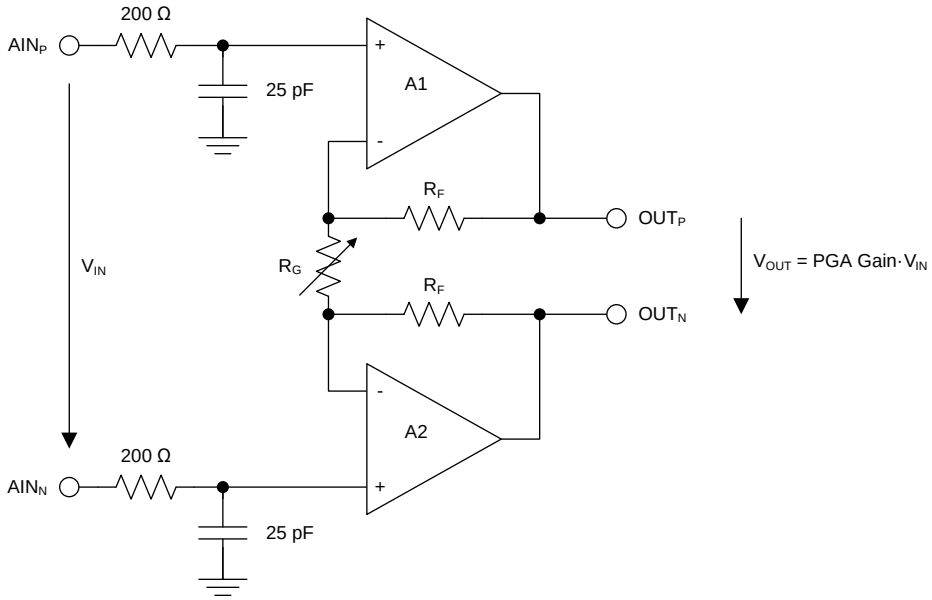


図 43. Simplified PGA Diagram

V_{IN} denotes the differential input voltage $V_{IN} = V_{AINP} – V_{AINN}$. Use 式 4 to calculate the gain of the PGA. Gain is changed inside the device using a variable resistor, R_G.

$$\text{PGA Gain} = 1 + 2 \cdot R_F / R_G \quad (4)$$

The switched-capacitor gain is changed using variable capacitors at the input to the ΔΣ modulator. Gains 1, 2, and 4 are implemented by using only the switched-capacitor circuit, which allows these gains to be used even when the PGA is bypassed; see the *Bypassing the PGA* section for more information about bypassing the PGA.

式 5 shows that the differential full-scale input voltage range (FSR) of the device is defined by the gain setting and the reference voltage used:

$$\text{FSR} = \pm V_{REF} / \text{Gain} \quad (5)$$

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表 10 shows the corresponding full-scale ranges when using the internal 2.048-V reference.

表 10. Full-Scale Range

GAIN SETTING	FSR
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

9.3.2.1 PGA Input Voltage Requirements

As with many amplifiers, the PGA has an absolute input voltage range requirement that cannot be exceeded. The maximum and minimum absolute input voltages are limited by the voltage swing capability of the PGA output. The specified minimum and maximum absolute input voltages (V_{AINP} and V_{AINN}) depend on the PGA gain, the maximum differential input voltage (V_{INMAX}), and the tolerance of the analog power-supply voltages (AVDD and AVSS). Because gain on the ADS122C04 is implemented by both the PGA and a switched-capacitor gain circuit, there are two formulas that define the absolute input voltages. Use 式 6 when the device gain is configured to less than or equal to 4. Use 式 7 when the device gain is greater than 4. Use the maximum differential input voltage expected in the application for V_{INMAX}.

$$AVSS + 0.2\ V \le V_{AINP}, V_{AINN} \le AVDD - 0.2\ V \quad (6)$$

$$AVSS + 0.2\ V + |V_{INMAX}| \cdot (Gain - 4) / 8 \le V_{AINP}, V_{AINN} \le AVDD - 0.2\ V - |V_{INMAX}| \cdot (Gain - 4) / 8 \quad (7)$$

図 44 graphically shows the relationship between the PGA input voltages to the PGA output voltages for gains larger than 4. The PGA output voltages (V_{OUTP}, V_{OUTN}) depend on the PGA gain and the differential input voltage magnitudes. For linear operation, the PGA output voltages must not exceed AVDD – 0.2 V or AVSS + 0.2 V. 図 44 depicts an example of a positive differential input voltage that results in a positive differential output voltage.

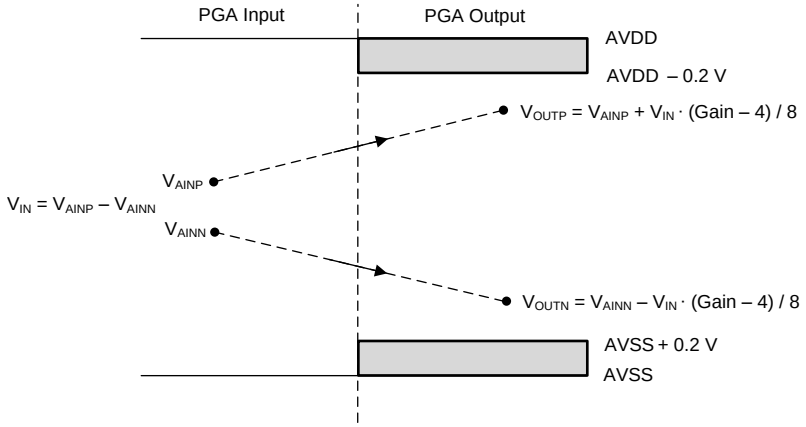


図 44. PGA Input/Output Voltage Relationship

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9.3.2.2 Bypassing the PGA

At gains of 1, 2, and 4, the device can be configured to disable and bypass the low-noise PGA by setting the PGA_BYPASS bit in the configuration register. Disabling the PGA lowers the overall power consumption and also removes the restrictions of 式 6 and 式 7 for the absolute input voltage range. The usable absolute input voltage range is (AVSS – 0.1 V ≤ V_{AINP}, V_{AINN} ≤ AVDD + 0.1 V) when the PGA is disabled.

In order to measure single-ended signals that are referenced to AVSS (AIN_P = V_{IN}, AIN_N = AVSS), the PGA must be bypassed. Configure the device for single-ended measurements by either connecting one of the analog inputs to AVSS externally or by using the internal AVSS connection of the multiplexer (MUX[3:0] settings 1000 through 1011). When configuring the internal multiplexer for settings where AIN_N = AVSS (MUX[3:0] = 1000 through 1011), the PGA is automatically bypassed and disabled irrespective of the PGA_BYPASS setting and gain is limited to 1, 2, and 4. In case gain is set to greater than 4, the device limits gain to 4.

When the PGA is disabled, the device uses a buffered switched-capacitor stage to obtain gains 1, 2, and 4. An internal buffer in front of the switched-capacitor stage ensures that the effect on the input loading resulting from the capacitor charging and discharging is minimal. See the *Electrical Characteristics* section for the typical values of absolute input currents (current flowing into or out of each input) and differential input currents (difference in absolute current between the positive and negative input) when the PGA is disabled.

For signal sources with high output impedance, external buffering may still be necessary. Active buffers can introduce noise as well as offset and gain errors. Consider all of these factors in high-accuracy applications.

9.3.3 Voltage Reference

The device offers an integrated, low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers a differential reference input pair (REFP and REFN). In addition, the analog supply (AVDD – AVSS) can be used as a reference.

The reference source is selected by two bits (VREF[1:0]) in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 µs to fully settle after power-up, when coming out of power-down mode, or when switching from an external reference source to the internal reference.

The differential reference input allows freedom in the reference common-mode voltage. The reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. When used in ratiometric applications, the reference inputs do not load the external circuitry; however, the analog supply current increases when using an external reference because the reference buffers are enabled.

In most cases the conversion result is directly proportional to the stability of the reference source. Any noise and drift of the voltage reference is reflected in the conversion result.

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9.3.4 Modulator and Internal Oscillator

A ΔΣ modulator is used in the ADS122C04 to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 4$, where f_{CLK} is provided by the internal oscillator. The oscillator frequency, and therefore also the modulator frequency, depend on the selected operating mode. 表 11 shows the oscillator and modulator frequencies for the different operating modes.

表 11. Oscillator and Modulator Clock Frequencies for Different Operating Modes

OPERATING MODE	f_{CLK}	f_{MOD}
Normal mode	1.024 MHz	256 kHz
Turbo mode	2.048 MHz	512 kHz

9.3.5 Digital Filter

The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. The frequency responses of the digital filter are illustrated in 図 45 to 図 53 for different output data rates. The filter notches and output data rate scale proportionally with the clock frequency. The internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate or conversion time, respectively, and consequently also the filter notches vary proportionally.

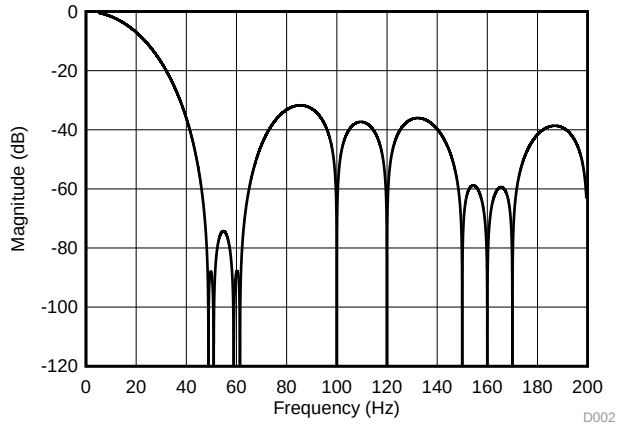


図 45. Filter Response (Normal Mode, DR = 20 SPS)

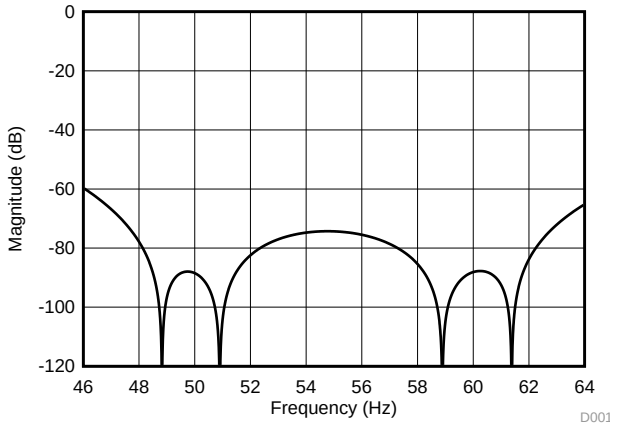


図 46. Detailed View of the Filter Response (Normal Mode, DR = 20 SPS)

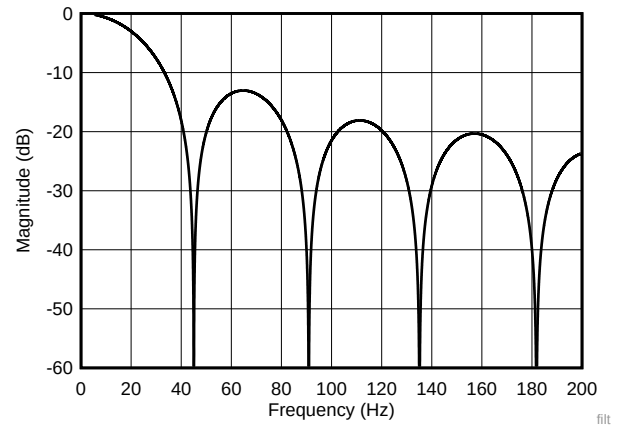


図 47. Filter Response (Normal Mode, DR = 45 SPS)

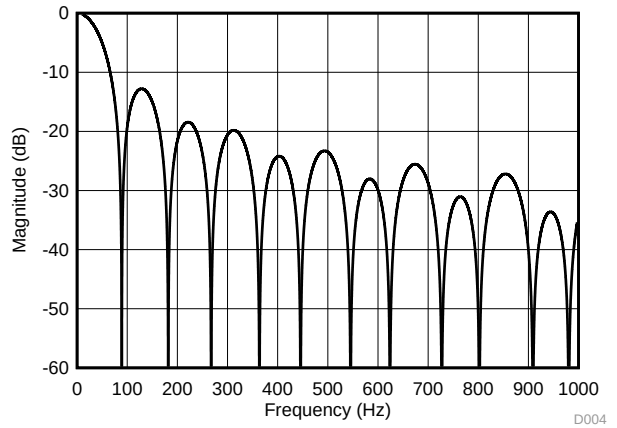


図 48. Filter Response (Normal Mode, DR = 90 SPS)

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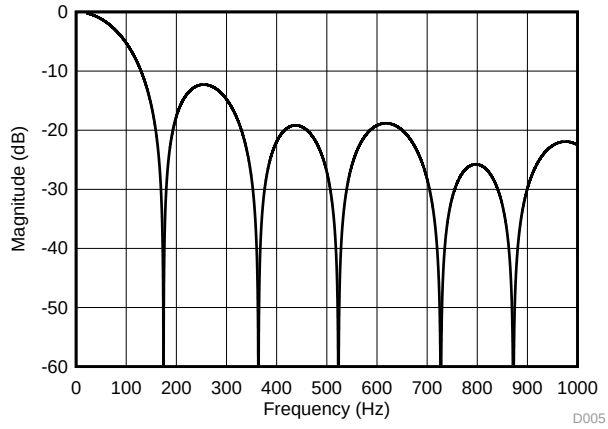


図 49. Filter Response (Normal Mode, DR = 175 SPS)

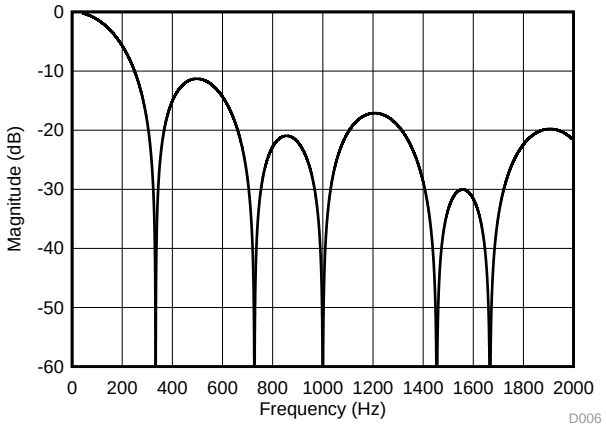


図 50. Filter Response (Normal Mode, DR = 330 SPS)

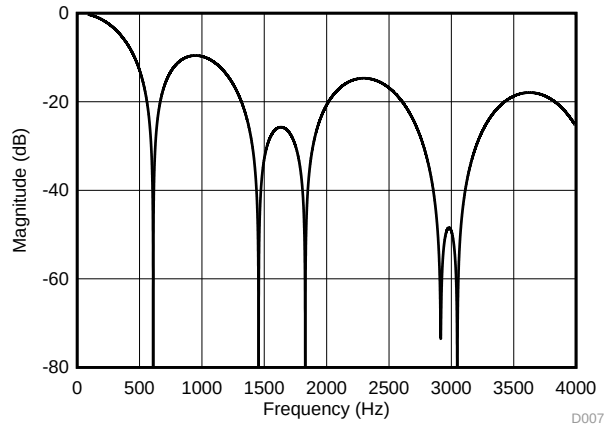


図 51. Filter Response (Normal Mode, DR = 600 SPS)

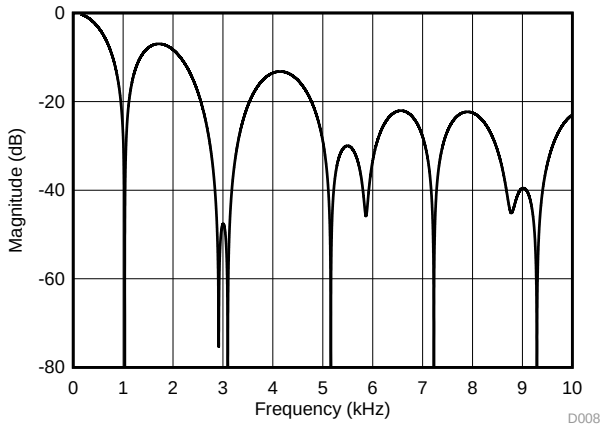


図 52. Filter Response (Normal Mode, DR = 1 kSPS)

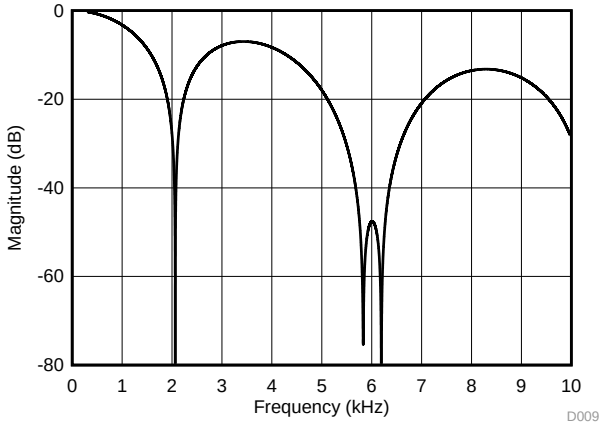


図 53. Filter Response (Turbo Mode, DR = 2 kSPS)

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9.3.6 Conversion Times

表 12 shows the actual conversion times for each data rate setting. The values provided are in terms of t_{CLK} cycles and in milliseconds.

Continuous conversion mode data rates are timed from one $\overline{DRDY}$ falling edge to the next $\overline{DRDY}$ falling edge. The first conversion starts 28.5 · t_{CLK} (normal mode) or 105 · t_{CLK} (turbo mode) after the START/SYNC command is latched.

Single-shot conversion mode data rates are timed from when the START/SYNC command is latched to the $\overline{DRDY}$ falling edge and rounded to the next t_{CLK}.

Commands are latched on the eighth falling edge of SCL in the command byte.

表 12. Conversion Times

NOMINAL DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	CONTINUOUS CONVERSION MODE(1)		SINGLE-SHOT CONVERSION MODE	
		ACTUAL CONVERSION TIME (t_{CLK})(2)	ACTUAL CONVERSION TIME (ms)	ACTUAL CONVERSION TIME (t_{CLK})(2)	ACTUAL CONVERSION TIME (ms)
NORMAL MODE					
20	13.1	51192	49.99	51213	50.01
45	20.0	22780	22.5	22805	22.27
90	39.6	11532	11.26	11557	11.29
175	77.8	5916	5.78	5941	5.80
330	150.1	3116	3.04	3141	3.07
600	279.0	1724	1.68	1749	1.71
1000	483.8	1036	1.01	1061	1.04
TURBO MODE					
40	17.1	51192	25.00	51217	25.01
90	39.9	22780	11.12	22809	11.14
180	79.2	11532	5.63	11561	5.65
350	155.6	5916	2.89	5945	2.90
660	300.3	3116	1.52	3145	1.54
1200	558.1	1724	0.84	1753	0.86
2000	967.6	1036	0.51	1065	0.52

(1) The first conversion starts 28.5 · t_{CLK} (normal mode) or 105 · t_{CLK} (turbo mode) after the START/SYNC command is latched. The times listed in this table do not include that time.
(2) t_{CLK} = 1 / f_{CLK}. f_{CLK} = 1.024 MHz in normal mode and 2.048 MHz in turbo mode.

Although the conversion time at the 20-SPS setting is not exactly 1 / 20 Hz = 50 ms, this discrepancy does not affect the 50-Hz or 60-Hz rejection. The conversion time and filter notches vary by the amount specified in the *Electrical Characteristics* table for oscillator accuracy.

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9.3.7 Excitation Current Sources

The device provides two matched programmable excitation current sources (IDACs) for resistance temperature detector (RTD) applications. The output current of the current sources can be programmed to 10 µA, 50 µA, 100 µA, 250 µA, 500 µA, 1000 µA, or 1500 µA using the respective bits (IDAC[2:0]) in the configuration register. Each current source can be connected to any of the analog inputs (AINx) as well as to the dedicated reference inputs (REFP and REFN). Both current sources can also be connected to the same pin. Routing of the IDACs is configured by bits (I1MUX[2:0], I2MUX[2:0]) in the configuration register. Care must be taken not to exceed the compliance voltage of the IDACs. In other words, limit the voltage on the pin where the IDAC is routed to ≤ (AVDD – 0.9 V), otherwise the specified accuracy of the IDAC current is not met. For three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *3-Wire RTD Measurement* section for more details).

The IDACs require up to 200 µs to start up after the IDAC current is programmed to the respective value using the IDAC[2:0] bits. Set the IDAC current to the respective value using the IDAC[2:0] bits and then select the routing for each IDAC (I1MUX[2:0], I2MUX[2:0]) thereafter.

In single-shot conversion mode, the IDACs remain active between any two conversions if the IDAC[2:0] bits are set to a value other than 000. However, the IDACs are powered down whenever the POWERDOWN command is issued.

Keep in mind that the analog supply current increases when enabling the IDACs (that is, when the IDAC[2:0] bits are set to a value other than 000). The IDAC circuit needs this bias current to operate even when the IDACs are not routed to any pin (I1MUX[2:0] = I2MUX[2:0] = 000). In addition, the selected output current is drawn from the analog supply when I1MUX[2:0] or I2MUX[2:0] are set to a value other than 000.

9.3.8 Sensor Detection

To help detect a possible sensor malfunction, the device provides internal 10-µA, burn-out current sources. When enabled by setting the respective bit (BCS) in the configuration register, one current source provides current to the positive analog input (AIN_P) currently selected and the other current source sinks current from the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading can indicate a shorted sensor. The absolute value of the burn-out current sources typically varies by ±5% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

Keep in mind that ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled. Disable the burn-out current sources when preforming the precision measurement, and only enable these sources to test for sensor fault conditions.

9.3.9 System Monitor

The device provides some means for monitoring the analog power supply and the external voltage reference. To select a monitoring voltage, the internal multiplexer (MUX[3:0]) must be configured accordingly in the configuration register. The device automatically bypasses the PGA and sets the gain to 1, irrespective of the configuration register settings when the monitoring feature is used. The system monitor function only provides a coarse result and is not meant to be a precision measurement.

When measuring the analog power supply (MUX[3:0] = 1101), the resulting conversion is approximately (AVDD – AVSS) / 4. The device uses the internal 2.048-V reference for the measurement regardless of what reference source is selected in the configuration register (VREF[1:0]).

When monitoring the external reference voltage source (MUX[3:0] = 1100), the result is approximately ($V_{(REFP)}$ – $V_{(REFN)}$) / 4. The device automatically uses the internal reference for the measurement.

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9.3.10 Temperature Sensor

The ADS122C04 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting the TS bit = 1 in the configuration register. When in temperature sensor mode, the settings of configuration register 0 have no effect and the device uses the internal reference for measurement, regardless of the selected voltage reference source. Temperature readings follow the same process as the analog inputs for starting and reading conversion results. Temperature data are represented as a 14-bit effective result that is left-justified within the 24-bit conversion result. When reading the three data bytes, the first 14 bits (MSBs) are used to indicate the temperature measurement result. The LSBs of the data output do not indicate temperature. Only the 14 MSBs are relevant. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary two's complement format. 表 13 shows the mapping between temperature and digital codes.

表 13. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–40	11 1011 0000 0000	3B00

9.3.10.1 Converting From Temperature to Digital Codes

9.3.10.1.1 For Positive Temperatures (For Example, 50°C):

Two's complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left-justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.03125°C per count) = 1600 = 0640h = 00 0110 0100 0000

9.3.10.1.2 For Negative Temperatures (For Example, –25°C):

Generate the two's complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.03125°C per count) = 800 = 0320h = 00 0011 0010 0000

Two's complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

9.3.10.2 Converting From Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB is a 1, subtract 1 from the result and complement all bits. Then, multiply the result by –0.03125°C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h · 0.03125°C = 2400 · 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Subtract 1 and complement the result: 3CE0h → 0320h

0320h · (–0.03125°C) = 800 · (–0.03125°C) = –25°C

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9.3.11 Offset Calibration

The internal multiplexer offers the option to short both PGA inputs (AIN_P and AIN_N) to mid-supply (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. Take multiple readings with the inputs shorted and average the result to reduce the effect of noise.

9.3.12 Conversion Data Counter

The ADS122C04 offers an optional data counter word to help the host determine if the conversion data are new. The DCNT bit in the configuration register enables the conversion data counter. The data counter appears as an 8-bit word that precedes the conversion data each time a conversion result is read. The reset value of the counter is 00h. The word increments each time the ADC completes a conversion. The counter rolls over to 00h after reaching FFh.

When the host reads a conversion result, the host can determine if the data being read are new by comparing the counter value with the counter value obtained with the last data read. If the counter values are the same, then this result indicates that no new conversion data are available from the ADC. The counter can also help the host determine if a conversion result was missed.

Reset the conversion data counter by clearing the DCNT bit to 0 and then setting DCNT back to 1. A device reset also resets the conversion data counter.

9.3.13 Data Integrity Features

There are two methods for ensuring data integrity for data output on the ADS122C04. Output data can be register contents or conversion results. The optional data counter word that precedes conversion data is covered by both data integrity options. The data integrity modes are configured using the CRC[1:0] bits in the configuration register. When CRC[1:0] = 01, a bitwise-inverted version of the data is output immediately following the most significant byte (MSB) of the data.

When CRC[1:0] = 10, a 16-bit CRC word is output immediately following the MSB of the data. In CRC mode, the checksum bytes are the 16-bit remainder of the bitwise exclusive-OR (XOR) of the data bytes with a CRC polynomial. The CRC is based on the CRC-16-CCITT polynomial: $x^{16} + x^{12} + x^5 + 1$ with an initial value of FFFFh.

The 17 binary coefficients of the polynomial are: 1 0001 0000 0010 0001. To calculate the CRC, divide (XOR operation) the data bytes (excluding the CRC) with the polynomial and compare the calculated CRC values to the ADC CRC value. If the values do not match, a data transmission error has occurred. In the event of a data transmission error, read the data again.

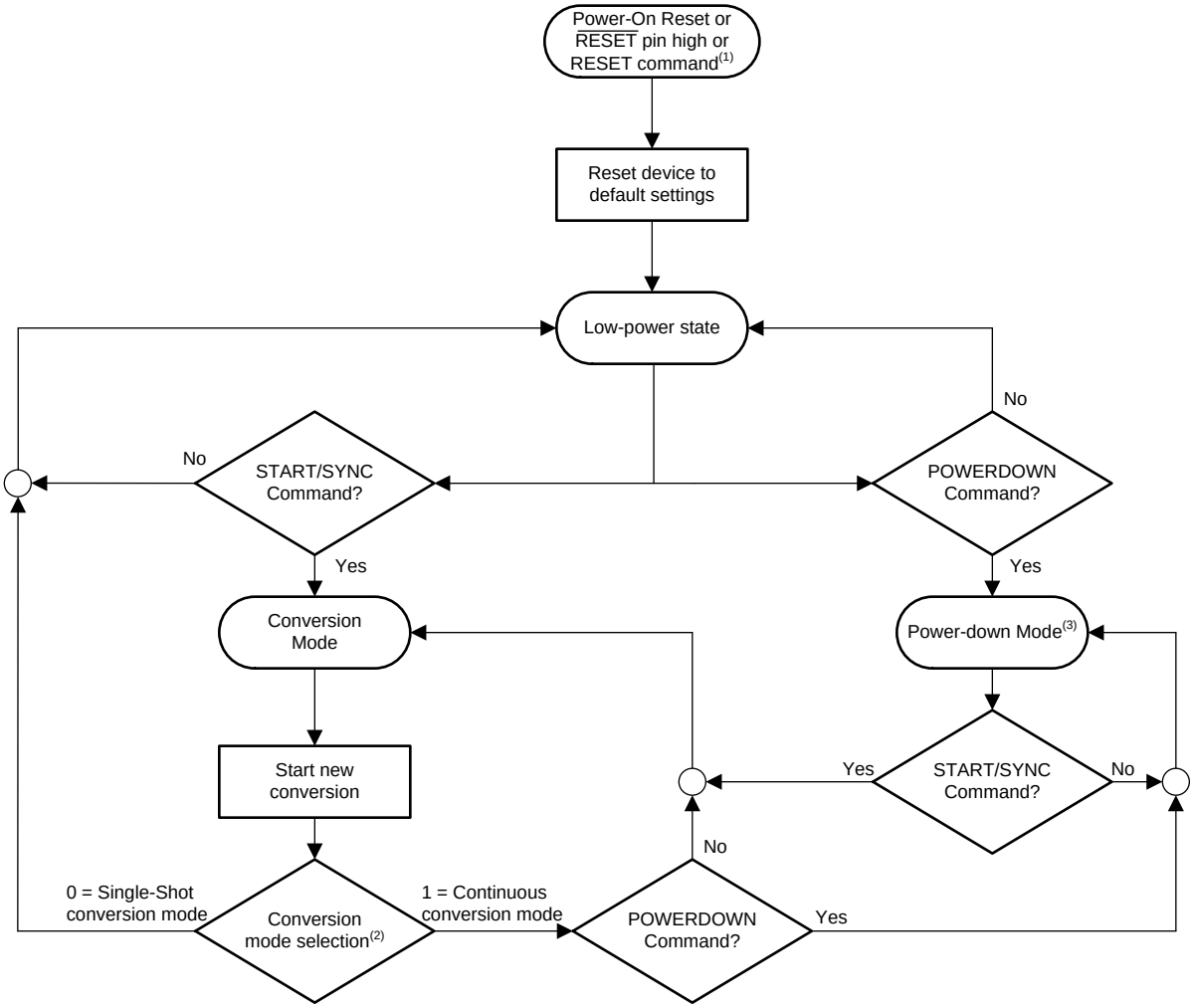
The following list shows a general procedure to compute the CRC value:

1. Left-shift the initial data value by 16 bits, with zeros padded to the right.
2. Align the MSB of the CRC polynomial to the left-most, logic-one value of the data.
3. Perform an XOR operation on the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter-length value. The bits of the data values that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result.
4. When the XOR result is less than 1 0000 0000 0000 0000, the procedure ends, yielding the 16-bit CRC value. Otherwise, continue with the XOR operation shown in step 2 using the current data value. The number of loop iterations depends on the value of the initial data.

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9.4 Device Functional Modes

図 54 shows a flow chart of the different operating modes and how the device transitions from one mode to another.



(1) Any reset (power-on, command, or pin) immediately resets the device.

(2) The conversion mode is selected with the CM bit in the configuration register.

(3) The POWERDOWN command allows any ongoing conversion to complete before placing the device in power-down mode.

図 54. Operating Flow Chart

9.4.1 Power-Up and Reset

The ADS122C04 is reset in one of three ways: either by a power-on reset, by the $\overline{\text{RESET}}$ pin, or by a RESET command.

When a reset occurs, the configuration registers reset to the default values and the device enters a low-power state. The device then waits for the START/SYNC command to enter conversion mode; see the *I^2C Timing Requirements* table for reset timing information.

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Device Functional Modes (continued)

9.4.1.1 Power-On Reset

During power up, the device is held in reset. The power-on reset releases approximately 500 µs after both supplies have exceeded their respective power-up reset thresholds. After this time all internal circuitry (including the voltage reference) are stable and communication with the device is possible. As part of the power-on reset process, the device sets all bits in the configuration registers to the respective default settings. After power-up, the device enters a low-power state. This power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up.

9.4.1.2 $\overline{\text{RESET}}$ Pin

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low for a minimum of $t_{w(RSL)}$ and then returning the pin high. After the rising edge of the $\overline{\text{RESET}}$ pin, a delay time of $t_{d(RSSTA)}$ is required before communicating with the device; see the *I^2C Timing Requirements* section for reset timing information.

9.4.1.3 Reset by Command

Reset the ADC by using the RESET command (06h or 07h). No delay time is required after the RESET command is latched before starting to communicate with the device as long as the timing requirements (see the *I^2C Timing Requirements* table) for the (repeated) START and STOP conditions are met. Alternatively, the device also responds to the I^2C general-call software reset.

9.4.2 Conversion Modes

The device operates in one of two conversion modes that are selected by the CM bit in the configuration register. These conversion modes are single-shot conversion and continuous conversion mode. A START/SYNC command must be issued each time the CM bit is changed.

9.4.2.1 Single-Shot Conversion Mode

In single-shot conversion mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry (except for the excitation current sources) are turned off while the device waits in this low-power state until the next conversion is started. Writing to any configuration register when a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to the final value before the conversion starts) because the device digital filter settles within a single cycle.

9.4.2.2 Continuous Conversion Mode

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion.

In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts $28.5 \cdot t_{CLK}$ (normal mode) or $105 \cdot t_{CLK}$ (turbo mode) after the START/SYNC command is latched. Writing to any configuration register during an ongoing conversion restarts the current conversion. Send a START/SYNC command immediately after the CM bit is set to 1.

Stop continuous conversions by sending the POWERDOWN command.

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Device Functional Modes (continued)

9.4.3 Operating Modes

In addition to the different conversion modes, the device can also be operated in different operating modes that can be selected to trade-off power consumption, noise performance, and output data rate. These modes are: normal mode, turbo mode, and power-down mode.

9.4.3.1 Normal Mode

Normal mode is the default mode of operation after power-up. In this mode, the internal modulator of the ΔΣ ADC runs at a modulator clock frequency of $f_{MOD} = f_{CLK} / 4 = 256$ kHz, where the system clock (f_{CLK}) is provided by the internal oscillator. Normal mode offers output data rate options ranging from 20 SPS to 1 kSPS. The data rate is selected by the DR[2:0] bits in the configuration register.

9.4.3.2 Turbo Mode

Applications that require higher data rates up to 2 kSPS can operate the device in turbo mode. In this mode, the internal modulator runs at a higher frequency of $f_{MOD} = f_{CLK} / 4 = 512$ kHz. Compared to normal mode, the device power consumption increases because the modulator runs at a higher frequency. Running the ADS122C04 in turbo mode at a comparable output data rate as in normal mode yields better noise performance. For example, the input-referred noise at 90 SPS in turbo mode is lower than the input-referred noise at 90 SPS in normal mode.

9.4.3.3 Power-Down Mode

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference and both IDACs) are powered down and the device typically only uses 400 nA of current. When in power-down mode, the device holds the configuration register settings and responds to commands, but does not perform any data conversions.

Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit.

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9.5 Programming

9.5.1 I²C Interface

The ADS122C04 uses an I²C-compatible (inter-integrated circuit) interface for serial communication. I²C is a 2-wire communication interface that allows communication of a master device with multiple slave devices on the same bus through the use of device addressing. Each slave device on an I²C bus must have a unique address. Communication on the I²C bus always takes place between two devices: one acting as the master and the other as the slave. Both the master and slave can receive and transmit data, but the slave can only read or write under the direction of the master. The ADS122C04 always acts as an I²C slave device.

An I²C bus consists of two lines: SDA and SCL. SDA carries data and SCL provides the clock. Devices on the I²C bus drive the bus lines low by connecting the lines to ground; the devices never drive the bus lines high. Instead, the bus wires are pulled high by pullup resistors; thus, the bus wires are always high when a device is not driving the lines low. As a result of this configuration, two devices do not conflict. If two devices drive the bus simultaneously, there is no driver contention.

See the *I²C-Bus Specification and User Manual* from NXP Semiconductors™ for more details.

9.5.1.1 I²C Address

The ADS122C04 has two address pins: A0 and A1. Each address pin can be tied to either DGND, DVDD, SDA, or SCL, providing 16 possible unique addresses. This configuration allows up to 16 different ADS122C04 devices to be present on the same I²C bus. 表 14 shows the truth table for the I²C addresses for the possible address pin connections.

At the start of every transaction, that is between the START condition (first falling edge of SDA) and the first falling SCL edge of the address byte, the ADS122C04 decodes its address configuration again.

表 14. I²C Address Truth Table

A1	A0	I²C ADDRESS
DGND	DGND	100 0000
DGND	DVDD	100 0001
DGND	SDA	100 0010
DGND	SCL	100 0011
DVDD	DGND	100 0100
DVDD	DVDD	100 0101
DVDD	SDA	100 0110
DVDD	SCL	100 0111
SDA	DGND	100 1000
SDA	DVDD	100 1001
SDA	SDA	100 1010
SDA	SCL	100 1011
SCL	DGND	100 1100
SCL	DVDD	100 1101
SCL	SDA	100 1110
SCL	SCL	100 1111

9.5.1.2 Serial Clock (SCL) and Serial Data (SDA)

The serial clock (SCL) line is used to clock data in and out of the device. The master always drives the clock line. The ADS122C04 cannot act as a master and as a result can never drive SCL.

The serial data (SDA) line allows for bidirectional communication between the host (the master) and the ADS122C04 (the slave). When the master reads from a ADS122C04, the ADS122C04 drives the data line; when the master writes to a ADS122C04, the master drives the data line.

Data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the SCL line is low. One clock pulse is generated for each data bit transferred. When in an idle state, the master should hold SCL high.

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9.5.1.3 Data Ready (DRDY)

DRDY is an open-drain output pin that indicates when a new conversion result is ready for retrieval. When DRDY falls low, new conversion data are ready. DRDY transitions back high when the conversion result is latched for output transmission. In case a conversion result in continuous conversion mode is not read, DRDY releases high for $t_{w(DRH)}$ before the next conversion completes. See the *I²C Timing Requirements* table for more details.

9.5.1.4 Interface Speed

The ADS122C04 supports I²C interface speeds up to 1 Mbps. Standard-mode (Sm) with bit rates up to 100 kbps, fast-mode (Fm) with bit rates up to 400 kbps, and fast-mode plus (Fm+) with bit rates up to 1 Mbps are supported. High-speed mode (Hs-mode) is not supported.

9.5.1.5 Data Transfer Protocol

図 55 shows the format of the data transfer. The master initiates all transactions with the ADS122C04 by generating a START (S) condition. A high-to-low transition on the SDA line while SCL is high defines a START condition. The bus is considered to be busy after the START condition.

Following the START condition, the master sends the 7-bit slave address corresponding to the address of the ADS122C04 that the master wants to communicate with. The master then sends an eighth bit that is a data direction bit (R/W). An R/W bit of 0 indicates a write operation, and an R/W bit of 1 indicates a read operation. After the R/W bit, the master generates a ninth SCLK pulse and releases the SDA line to allow the ADS122C04 to acknowledge (ACK) the reception of the slave address by pulling SDA low. In case the device does not recognize the slave address, the ADS122C04 holds SDA high to indicate a not acknowledge (NACK) signal.

Next follows the data transmission. If the transaction is a read (R/W = 1), the ADS122C04 outputs data on SDA. If the transaction is a write (R/W = 0), the host outputs data on SDA. Data are transferred byte-wise, most significant bit (MSB) first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be acknowledged (via the ACK bit) by the receiver. If the transaction is a read, the master issues the ACK. If the transaction is a write, the ADS122C04 issues the ACK.

The master terminates all transactions by generating a STOP (P) condition. A low-to-high transition on the SDA line while SCL is high defines a STOP condition. The bus is considered free again t_{BUF} (bus-free time) after the STOP condition.

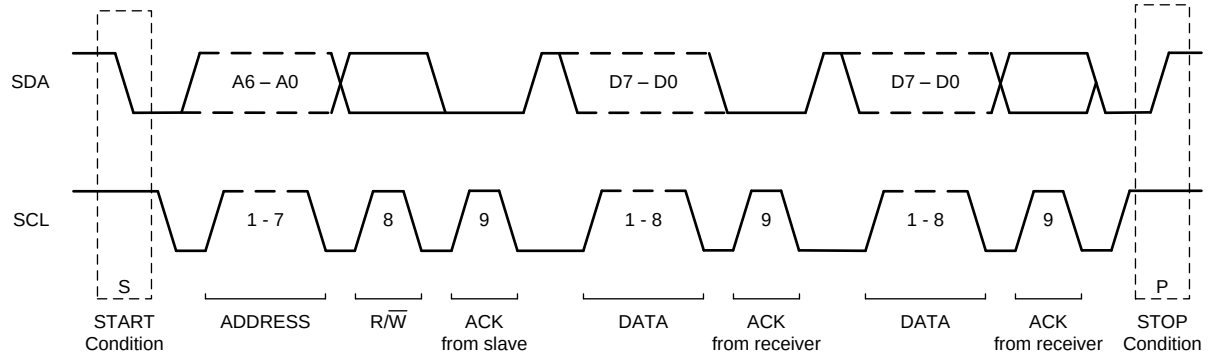


図 55. I²C Data Transfer Format

9.5.1.6 I²C General Call (Software Reset)

The ADS122C04 responds to the I²C general-call address (0000 000) if the R/W bit is 0. The device acknowledges the general-call address and, if the next byte is 06h, performs a reset. The general-call software reset has the same effect as the RESET command.

9.5.1.7 Timeout

The ADS122C04 offers a I²C timeout feature that can be used to recover communication when a serial interface transmission is interrupted. If the host initiates contact with the ADS122C04 but subsequently remains idle for $14000 \cdot t_{MOD}$ in normal mode and $28000 \cdot t_{MOD}$ in turbo mode before completing a command, the ADS122C04 interface is reset. If the ADS122C04 interface resets because of a timeout condition, the host must abort the transaction and restart the communication again by issuing a new START condition.

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9.5.2 Data Format

The device provides 24 bits of data in binary two's complement format. Use 式 8 to calculate the size of one code (LSB).

$$1\ \text{LSB} = (2 \cdot V_{REF} / \text{Gain}) / 2^{24} = +\text{FS} / 2^{23} \quad (8)$$

A positive full-scale input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFFFh and a negative full scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 800000h. The output clips at these codes for signals that exceed full-scale.

表 15 summarizes the ideal output codes for different input signals.

表 15. Ideal Output Code versus Input Signal

INPUT SIGNAL, $V_{IN} = V_{AINP} - V_{AINN}$	IDEAL OUTPUT CODE(1)
$\geq \text{FS}\ (2^{23} - 1) / 2^{23}$	7FFFFFh
$\text{FS} / 2^{23}$	000001h
0	000000h
$-\text{FS} / 2^{23}$	FFFFFFh
$\leq -\text{FS}$	800000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

図 56 shows the mapping of the analog input signal to the output codes.

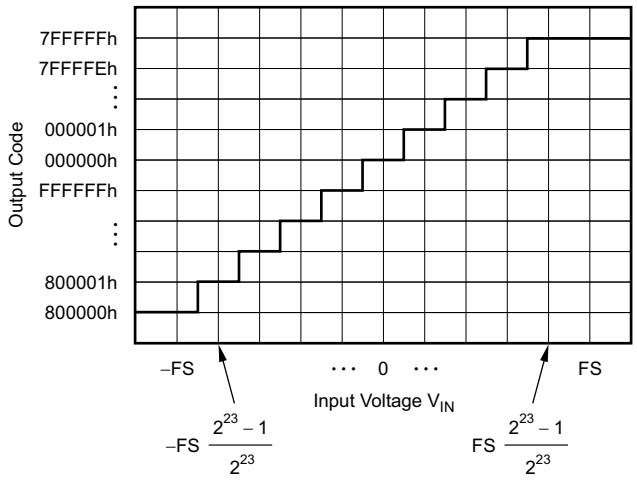


図 56. Code Transition Diagram

注

Single-ended signal measurements, where V_{AINN} = 0 V and V_{AINP} = 0 V to +FS, only use the positive code range from 000000h to 7FFFFFh. However, because of device offset, the ADS122C04 can still output negative codes when V_{AINP} is close to 0 V.

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9.5.3 Commands

As 表 16 shows, the device offers six different commands to control device operation. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction.

表 16. Command Definitions

COMMAND	DESCRIPTION	COMMAND BYTE (1)
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read register at address *rr*	0010 *rrxx*
WREG	Write register at address *rr*	0100 *rrxx*

(1) Operands: rr = register address (00 to 11), x = don't care.

9.5.3.1 Command Latching

Commands are not processed until latched by the ADS122C04. Commands are latched on the eighth falling edge of SCL in the command byte.

注

The legend for 図 57 to 図 63:

From master to slave

From slave to master

S = START condition
Sr = Repeated START condition
P = STOP condition
A = acknowledge (SDA low)
$\overline{A}$ = not acknowledge (SDA high)

9.5.3.2 RESET (0000 011x)

This command resets the device to the default states. No delay time is required after the RESET command is latched before starting to communicate with the device as long as the timing requirements (see the *I^2C Timing Requirements* table) for the (repeated) START and STOP conditions are met.

9.5.3.3 START/SYNC (0000 100x)

In single-shot conversion mode, the START/SYNC command is used to start a single conversion, or (when sent during an ongoing conversion) to reset the digital filter and then restart a single new conversion. When the device is set to continuous conversion mode, the START/SYNC command must be issued one time to start converting continuously. Sending the START/SYNC command when converting in continuous conversion mode resets the digital filter and restarts continuous conversions.

9.5.3.4 POWERDOWN (0000 001x)

The POWERDOWN command places the device into power-down mode. This command shuts down all internal analog components and turns off both IDACs, but holds all register values. In case the POWERDOWN command is issued when a conversion is ongoing, the conversion completes before the ADS122C04 enters power-down mode. As soon as a START/SYNC command is issued, all analog components return to their previous states.

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9.5.3.5 RDATA (0001 xxxx)

The RDATA command loads the output shift register with the most recent conversion result. Reading conversion data must be performed as shown in 図 57 by using two I²C communication frames. The first frame is an I²C write operation where the R/$\overline{W}$ bit at the end of the address byte is 0 to indicate a write. In this frame, the host sends the RDATA command to the ADS122C04. The second frame is an I²C read operation where the R/$\overline{W}$ bit at the end of the address byte is 1 to indicate a read. The ADS122C04 reports the latest ADC conversion data in this second I²C frame. If a conversion finishes in the middle of the RDATA command byte, the state of the $\overline{DRDY}$ pin at the end of the read operation signals whether the old or the new result is loaded. If the old result is loaded, $\overline{DRDY}$ stays low, indicating that the new result is not read out. The new conversion result loads when $\overline{DRDY}$ is high.

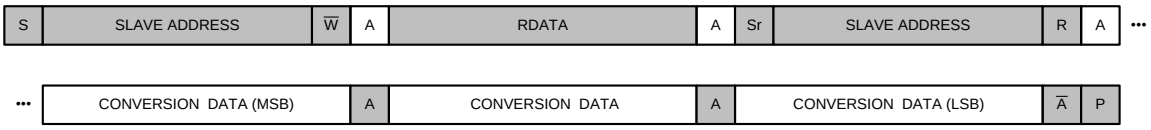


図 57. Read Conversion Data Sequence

9.5.3.6 RREG (0010 rrxx)

The RREG command reads the value of the register at address rr. Reading a register must be performed as shown in 図 58 by using two I²C communication frames. The first frame is an I²C write operation where the R/$\overline{W}$ bit at the end of the address byte is 0 to indicate a write. In this frame, the host sends the RREG command including the register address to the ADS122C04. The second frame is an I²C read operation where the R/$\overline{W}$ bit at the end of the address byte is 1 to indicate a read. The ADS122C04 reports the contents of the requested register in this second I²C frame.

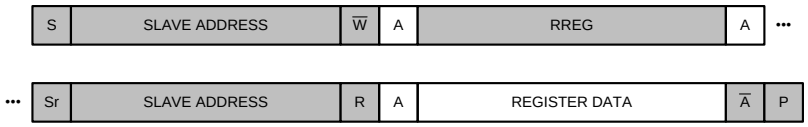


図 58. Read Register Sequence

9.5.3.7 WREG (0100 rrxx dddd dddd)

The WREG command writes dddd dddd to the register at address rr. Multiple registers can be written within the same I²C frame by simply issuing another WREG command without providing a STOP condition following the previous register write. 図 59 shows the sequence for writing an arbitrary number of registers. The R/$\overline{W}$ bit at the end of the address byte is 0 to indicate a write. The WREG command forces the digital filter to reset and any ongoing ADC conversion to restart.

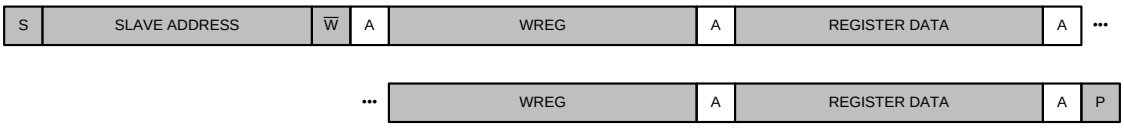


図 59. Write Register Sequence

9.5.4 Reading Data and Monitoring for New Conversion Results

Conversion data are read by issuing the RDATA command. The ADS122C04 responds to the RDATA command with the latest conversion result. There are three ways to monitor for new conversion data.

One way is to monitor for the falling edge of the $\overline{DRDY}$ signal. When $\overline{DRDY}$ falls low, a new conversion result is available for retrieval using the RDATA command. 図 60 illustrates the timing diagram for collecting data using the $\overline{DRDY}$ signal to indicate new data.

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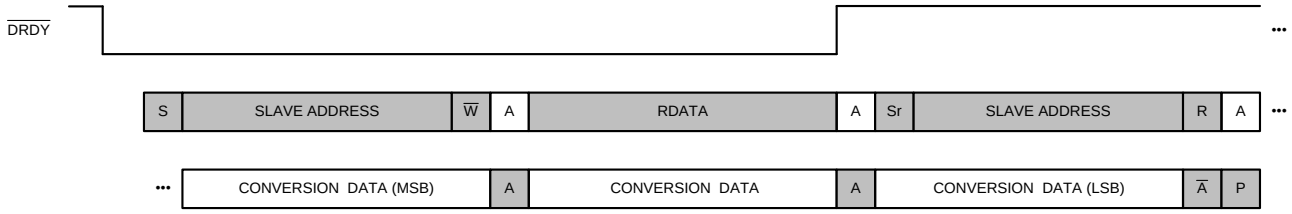


図 60. Using the DRDY Pin to Check for New Conversion Data

Another way to monitor for a new conversion result is to periodically read the DRDY bit in the configuration register. If set, the DRDY bit indicates that a new conversion result is ready for retrieval. The host can subsequently issue an RDATA command to retrieve the data. The rate at which the host polls the ADS122C04 for new data must be at least as fast as the data rate in continuous conversion mode to prevent the host from missing a conversion result.

If a new conversion result becomes ready during an I^2C transmission, the transmission is not corrupted. The new data are loaded into the output shift register upon the following RDATA command.

図 61 shows the timing diagram for collecting data using the DRDY bit in the configuration register to indicate new data.

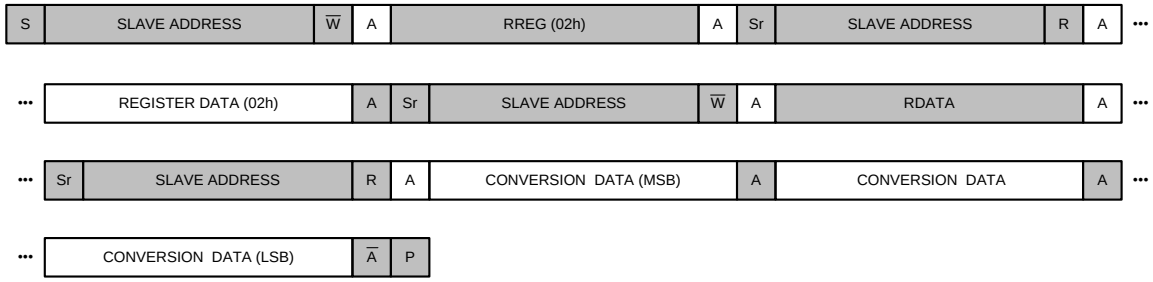


図 61. Using the DRDY Bit to Check for New Conversion Data

The last way to detect if new conversion data are available is through the use of the conversion data counter word. In this mode, the host periodically requests data from the device using the RDATA command and checks the conversion data counter word against the conversion data counter word read for the previous data received. If the counter values are the same, the host can disregard the data because that data has already been gathered. If the counter has incremented, the host records the data. The rate at which the host polls the ADS122C04 for new data must be at least as fast as the data rate in continuous conversion mode to prevent the host from missing a conversion result.

If a new conversion result becomes ready during an I^2C transmission, the transmission is not corrupted. The new data are loaded into the output shift register after the following RDATA command.

図 62 shows the timing diagram for collecting data using the conversion data counter word to indicate new data.

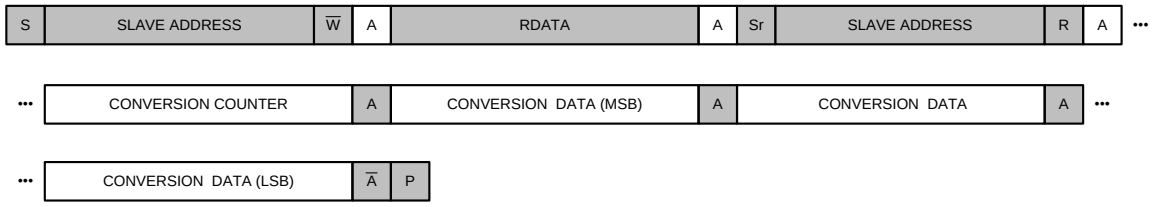


図 62. Using the Conversion Counter to Check for New Conversion Data

The conversion data counter can be used in conjunction with the previously discussed methods of detecting new data to ensure that the host did not miss a conversion result.

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9.5.5 Data Integrity

The optional data integrity checks can be configured using the CRC[1:0] bits in the configuration register. When one of the data integrity options is enabled, the data integrity check is output on the SDA pin immediately following the conversion or register data; see the *Data Integrity Features* section for a detailed description of the data integrity functionality. Additional words are always two bytes when CRC16 is enabled. The number of additional words in the inverted data mode when reading conversion data varies from three to four, depending on whether the conversion data counter is enabled. 図 63 shows data retrieval when either inverted data output or CRC are enabled.

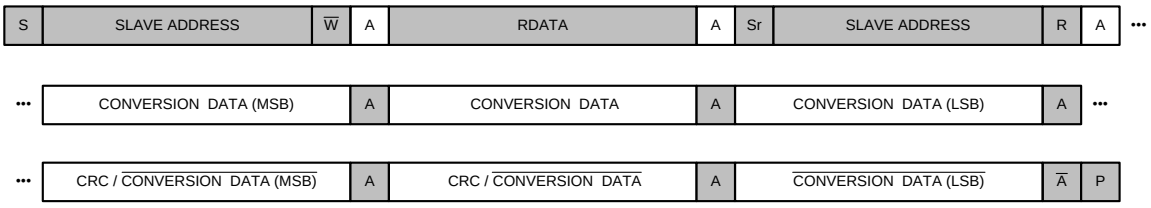


図 63. Conversion Data Output With CRC or Inverted Data Output Enabled

9.6 Register Map

9.6.1 Configuration Registers

The device has four 8-bit configuration registers that are accessible through the I^2C interface using the RREG and WREG commands. After power-up or reset, all registers are set to the default values (which are all 0). All register values are retained during power-down mode. 表 17 shows the register map of the configuration registers.

表 17. Configuration Register Map

REGISTER (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
01h	DR[2:0]			MODE	CM	VREF[1:0]		TS
02h	DRDY	DCNT	CRC[1:0]		BCS	IDAC[2:0]		
03h	I1MUX[2:0]			I2MUX[2:0]			0	0

9.6.2 Register Descriptions

表 18 lists the access codes for the ADS122C04 registers.

表 18. Register Access Type Codes

Access Type	Code	Description
R	R	Read
R/W	R/W	Read-Write
W	W	Write
-n		Value after reset or the default value

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9.6.2.1 Configuration Register 0 (address = 00h) [reset = 00h]

図 64. Configuration Register 0

7	6	5	4	3	2	1	0
MUX[3:0]				GAIN[2:0]			PGA_BYPASS
R/W-0h				R/W-0h			R/W-0h

表 19. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUX[3:0]	R/W	0h	**Input multiplexer configuration.** These bits configure the input multiplexer. For settings where AIN_N = AVSS, the PGA must be disabled (PGA_BYPASS = 1) and only gains 1, 2, and 4 can be used. 0000 : AIN_P = AIN0, AIN_N = AIN1 (default) 0001 : AIN_P = AIN0, AIN_N = AIN2 0010 : AIN_P = AIN0, AIN_N = AIN3 0011 : AIN_P = AIN1, AIN_N = AIN0 0100 : AIN_P = AIN1, AIN_N = AIN2 0101 : AIN_P = AIN1, AIN_N = AIN3 0110 : AIN_P = AIN2, AIN_N = AIN3 0111 : AIN_P = AIN3, AIN_N = AIN2 1000 : AIN_P = AIN0, AIN_N = AVSS 1001 : AIN_P = AIN1, AIN_N = AVSS 1010 : AIN_P = AIN2, AIN_N = AVSS 1011 : AIN_P = AIN3, AIN_N = AVSS 1100 : $(V_{(REFP)} – V_{(REFN)})$ / 4 monitor (PGA bypassed) 1101 : (AVDD – AVSS) / 4 monitor (PGA bypassed) 1110 : AIN_P and AIN_N shorted to (AVDD + AVSS) / 2 1111 : Reserved
3:1	GAIN[2:0]	R/W	0h	**Gain configuration.** These bits configure the device gain. Gains 1, 2, and 4 can be used without the PGA. In this case, gain is obtained by a switched-capacitor structure. 000 : Gain = 1 (default) 001 : Gain = 2 010 : Gain = 4 011 : Gain = 8 100 : Gain = 16 101 : Gain = 32 110 : Gain = 64 111 : Gain = 128
0	PGA_BYPASS	R/W	0h	**Disables and bypasses the internal low-noise PGA.** Disabling the PGA reduces overall power consumption and allows the absolute input voltage range to span from AVSS – 0.1 V to AVDD + 0.1 V. The PGA can only be disabled for gains 1, 2, and 4. The PGA is always enabled for gain settings 8 to 128, regardless of the PGA_BYPASS setting. 0 : PGA enabled (default) 1 : PGA disabled and bypassed

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9.6.2.2 Configuration Register 1 (address = 01h) [reset = 00h]

図 65. Configuration Register 1

7	6	5	4	3	2	1	0
DR[2:0]			MODE	CM	VREF[1:0]		TS
R/W-0h			R/W-0h	R/W-0h	R/W-0h		R/W-0h

表 20. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DR[2:0]	R/W	0h	**Data rate.** These bits control the data rate setting depending on the selected operating mode. 表 21 lists the bit settings for normal and turbo mode.
4	MODE	R/W	0h	**Operating mode.** These bits control the operating mode that the device operates in. 0 : Normal mode (256-kHz modulator clock, default) 1 : Turbo mode (512-kHz modulator clock)
3	CM	R/W	0h	**Conversion mode.** This bit sets the conversion mode for the device. 0 : Single-shot conversion mode (default) 1 : Continuous conversion mode
2:1	VREF[1:0]	R/W	0h	**Voltage reference selection.** These bits select the voltage reference source that is used for the conversion. 00 : Internal 2.048-V reference selected (default) 01 : External reference selected using the REFP and REFN inputs 10 : Analog supply (AVDD – AVSS) used as reference 11 : Analog supply (AVDD – AVSS) used as reference
0	TS	R/W	0h	**Temperature sensor mode.** This bit enables the internal temperature sensor and puts the device in temperature sensor mode. The settings of configuration register 0 have no effect and the device uses the internal reference for measurement when temperature sensor mode is enabled. 0 : Temperature sensor mode disabled (default) 1 : Temperature sensor mode enabled

表 21. DR Bit Settings

NORMAL MODE	TURBO MODE
000 = 20 SPS	000 = 40 SPS
001 = 45 SPS	001 = 90 SPS
010 = 90 SPS	010 = 180 SPS
011 = 175 SPS	011 = 350 SPS
100 = 330 SPS	100 = 660 SPS
101 = 600 SPS	101 = 1200 SPS
110 = 1000 SPS	110 = 2000 SPS
111 = Reserved	111 = Reserved

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9.6.2.3 Configuration Register 2 (address = 02h) [reset = 00h]

図 66. Configuration Register 2

7	6	5	4	3	2	1	0
DRDY	DCNT	CRC[1:0]		BCS	IDAC[2:0]		
R-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h		

表 22. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	DRDY	R	0h	**Conversion result ready flag.** This bit flags if a new conversion result is ready. This bit is reset when conversion data are read. 0 : No new conversion result available (default) 1 : New conversion result ready
6	DCNT	R/W	0h	**Data counter enable.** The bit enables the conversion data counter. 0 : Conversion counter disabled (default) 1 : Conversion counter enabled
5:4	CRC[1:0]	R/W	0h	**Data integrity check enable.** These bits enable and select the data integrity checks. 00 : Disabled (default) 01 : Inverted data output enabled 10 : CRC16 enabled 11 : Reserved
3	BCS	R/W	0h	**Burn-out current sources.** This bit controls the 10-µA, burn-out current sources. The burn-out current sources can be used to detect sensor faults such as wire breaks and shorted sensors. 0 : Current sources off (default) 1 : Current sources on
2:0	IDAC[2:0]	R/W	0h	**IDAC current setting.** These bits set the current for both IDAC1 and IDAC2 excitation current sources. 000 : Off (default) 001 : 10 µA 010 : 50 µA 011 : 100 µA 100 : 250 µA 101 : 500 µA 110 : 1000 µA 111 : 1500 µA

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9.6.2.4 Configuration Register 3 (address = 03h) [reset = 00h]

図 67. Configuration Register 3

7	6	5	4	3	2	1	0
I1MUX[2:0]			I2MUX[2:0]			0	0
R/W-0h			R/W-0h			R-0h	R-0h

表 23. Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	I1MUX[2:0]	R/W	0h	**IDAC1 routing configuration.** These bits select the channel that IDAC1 is routed to. 000 : IDAC1 disabled (default) 001 : IDAC1 connected to AIN0 010 : IDAC1 connected to AIN1 011 : IDAC1 connected to AIN2 100 : IDAC1 connected to AIN3 101 : IDAC1 connected to REFP 110 : IDAC1 connected to REFN 111 : Reserved
4:2	I2MUX[2:0]	R/W	0h	**IDAC2 routing configuration.** These bits select the channel that IDAC2 is routed to. 000 : IDAC2 disabled (default) 001 : IDAC2 connected to AIN0 010 : IDAC2 connected to AIN1 011 : IDAC2 connected to AIN2 100 : IDAC2 connected to AIN3 101 : IDAC2 connected to REFP 110 : IDAC2 connected to REFN 111 : Reserved
1:0	RESERVED	R	0h	**Reserved.** Always write 0

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10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS122C04 is a precision, 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) that offers many integrated features to ease the measurement of the most common sensor types, including various types of temperature and bridge sensors. Primary considerations when designing an application with the ADS122C04 include analog input filtering, establishing an appropriate external reference for ratiometric measurements, and setting the absolute input voltage range for the internal PGA. Connecting and configuring the interface appropriately is another concern. These considerations are discussed in the following sections.

10.1.1 Interface Connections

図 68 shows the principle interface connections for the ADS122C04.

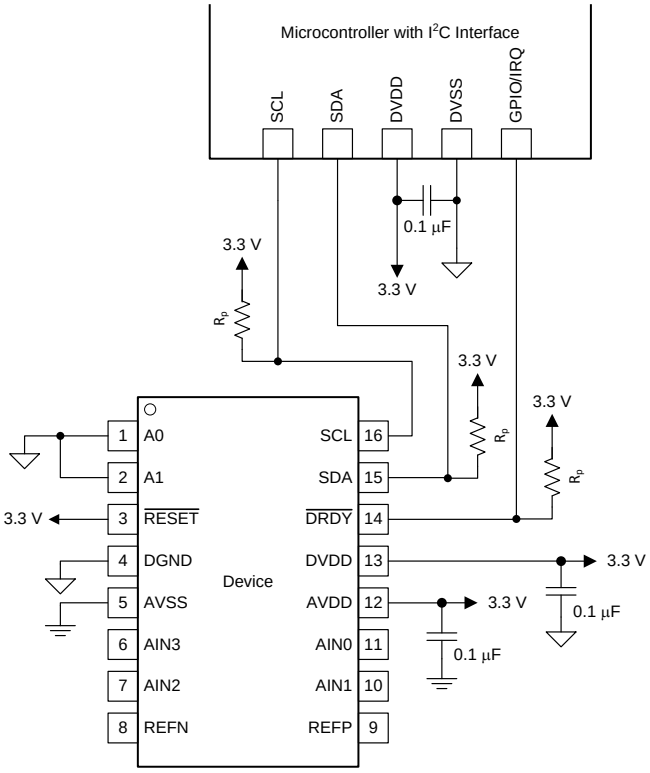


図 68. Interface Connections

The ADS122C04 interfaces directly to standard-mode, fast-mode, or fast-mode plus I^2C controllers. Any microcontroller I^2C peripheral, including master-only and single-master I^2C peripherals, operates with the ADS122C04. Details of the I^2C communication protocol of the device can be found in the *Programming* section. The ADS122C04 does not perform clock-stretching (that is, the device never pulls the clock line low), so this function does not need to be provided for unless other clock-stretching devices are present on the same I^2C bus.

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Application Information (continued)

Pullup resistors are required on both the SDA and SCL lines, as well as on the open-drain $\overline{\text{DRDY}}$ output. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors yield lower power consumption when the bus lines are pulled low, but increase the transition times on the bus, which limits the bus speed. Lower-value resistors allow higher interface speeds, but at the expense of higher power consumption when the bus lines are pulled low. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. Do not use resistors that are too small because the bus drivers may be unable to pull the bus lines low. See the *I²C-Bus Specification and User Manual* for details on pullup resistor sizing.

10.1.2 Connecting Multiple Devices on the Same I²C Bus

Up to 16 ADS122C04 devices can be connected to a single I²C bus by using different address pin configurations for each device. Use the address pins, A0 and A1, to set the ADS122C04 to one of 16 different I²C addresses. 図 69 shows an example with three ADS122C04 devices on the same I²C bus. One set of pullup resistors is required per bus line. If needed, decrease the pullup resistor values to compensate for the additional bus capacitance presented by multiple devices and increased line length.

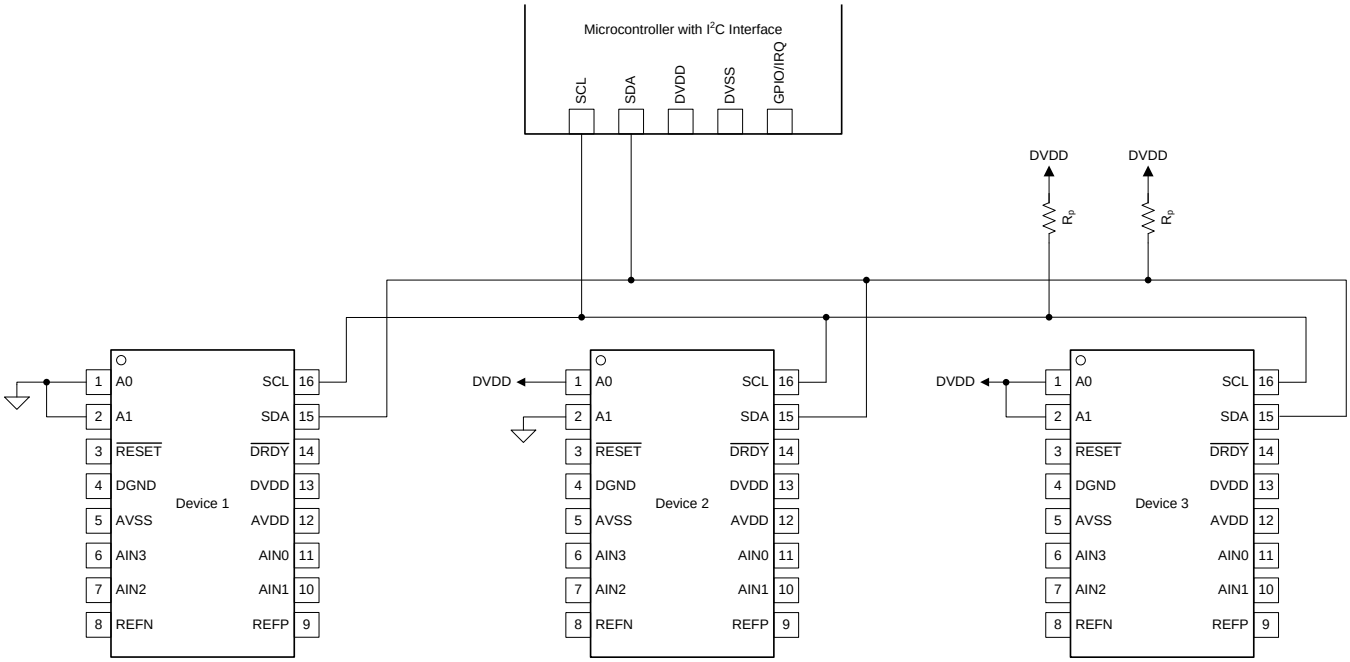


図 69. Connecting Multiple ADS122C04 Devices on the Same I²C Bus

10.1.3 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog and reference inputs floating, or connect the inputs to mid-supply or to AVDD. Connecting unused analog or reference inputs to AVSS is possible as well, but can yield higher leakage currents on other analog inputs than the previously mentioned options.

Do not float unused digital inputs; excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND, even when in power-down mode. Connections for unused digital pins are:

- Tie the $\overline{\text{RESET}}$ pin to DVDD if the $\overline{\text{RESET}}$ pin is not used
- If the $\overline{\text{DRDY}}$ output is not used, leave the $\overline{\text{DRDY}}$ pin unconnected or tie the $\overline{\text{DRDY}}$ pin to DVDD using a weak pullup resistor

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Application Information (continued)

10.1.4 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process, and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Inside a ΔΣ ADC, the input signal is sampled at the modulator frequency f_{MOD} and not at the output data rate. 図 70 shows that the filter response of the digital filter repeats at multiples of the sampling frequency (f_{MOD}). Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

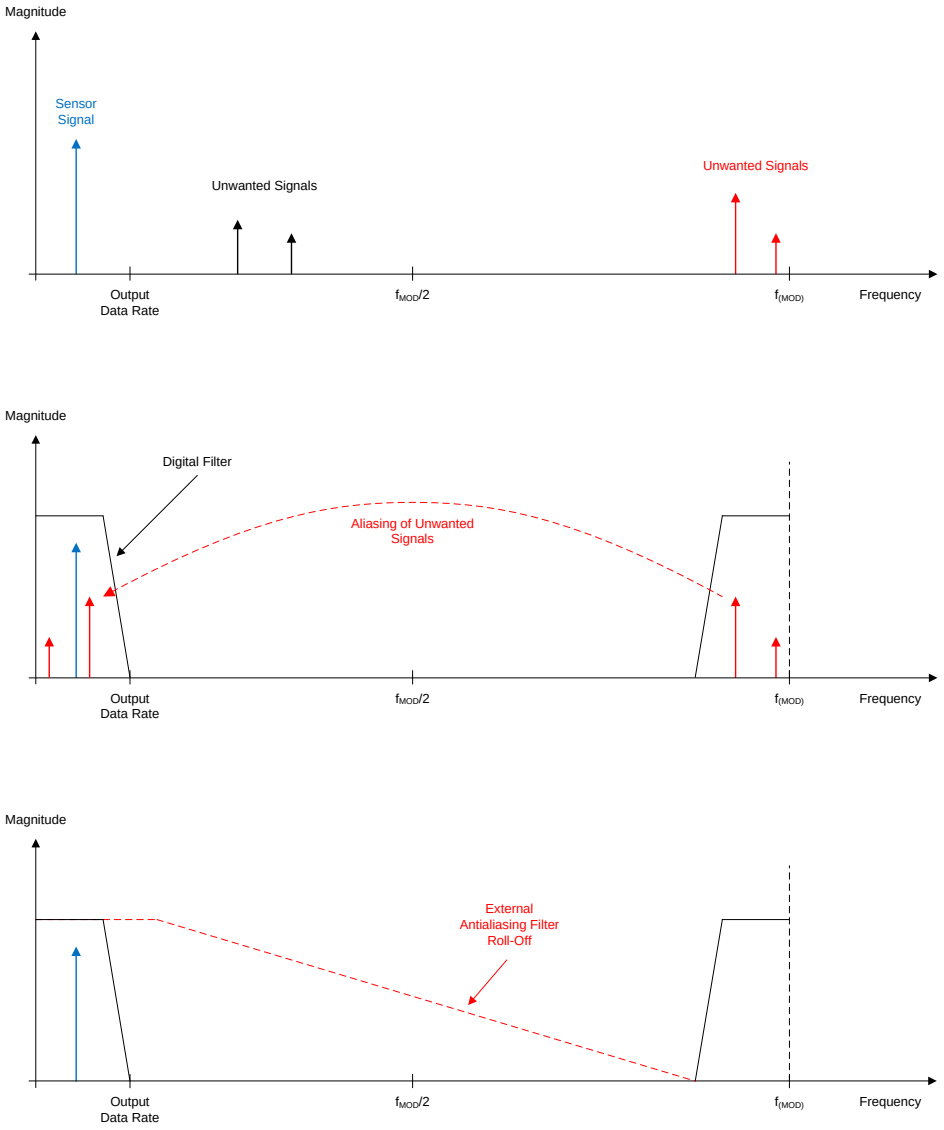


図 70. Effect of Aliasing

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Application Information (continued)

Many sensor signals are inherently band limited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass band. Power-line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS122C04 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; see 図 43. The cutoff frequency of this filter is approximately 31.8 MHz, which helps reject high-frequency interferences.

10.1.5 External Reference and Ratiometric Measurements

The full-scale range (FSR) of the ADS122C04 is defined by the reference voltage and the PGA gain (FSR = $\pm V_{REF}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system needs. An external reference must be used if V_{IN} is greater than 2.048 V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. These components cancel out in the ADC transfer function because current noise and drift are common to both the sensor measurement and the reference. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

10.1.6 Establishing Proper Limits on the Absolute Input Voltage

The ADS122C04 can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully differential signals (which can be either unipolar or bipolar). However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground (V_{AINN} = 0 V) are commonly called *single-ended signals*. If the PGA is disabled and bypassed, the absolute input voltages of the ADS122C04 can be as low as 100 mV below AVSS and as large as 100 mV above AVDD. Therefore, the PGA_BYPASS bit must be set in order to measure single-ended signals when a unipolar analog supply is used (AVSS = 0 V). Gains of 1, 2, and 4 are still possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100 Ω referenced to GND is a typical example. The ADS122C04 can directly measure the signal across the load resistor using a unipolar supply, the internal 2.048-V reference, and gain = 1 when the PGA is bypassed.

If gains larger than 4 are needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS122C04 to meet the absolute input voltage requirement of the PGA.

Signals where the negative analog input (AIN_N) is fixed at a voltage other the 0 V are referred to as *pseudo-differential signals*.

Fully differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

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Application Information (continued)

The ADS122C04 can measure pseudo-differential and fully differential signals with the PGA enabled or bypassed. However, the PGA must be enabled in order to use gains greater than 4. The absolute input voltages of the input signal must meet the absolute input voltage restrictions of the PGA (as explained in the *PGA Input Voltage Requirements* section) when the PGA is enabled. Setting the common-mode voltage at or near (AVSS + AVDD) / 2 in most cases satisfies the PGA absolute input voltage requirements.

Signals where both the positive and negative inputs are always ≥ 0 V are called *unipolar signals*. These signals can in general be measured with the ADS122C04 using a unipolar analog supply (AVSS = 0 V). As mentioned previously, the PGA must be bypassed in order to measure single-ended, unipolar signals when using a unipolar supply.

A signal is called *bipolar* when either the positive or negative input can swing below 0 V. A bipolar analog supply (such as AVDD = 2.5 V, AVSS = –2.5 V) is required in order to measure bipolar signals with the ADS122C04. A typical application task is measuring a single-ended, bipolar, ±10-V signal where AIN_N is fixed at 0 V and AIN_P swings between –10 V and 10 V. The ADS122C04 cannot directly measure this signal because the 10 V exceeds the analog power-supply limits. However, one possible solution is to use a bipolar analog supply (AVDD = 2.5 V, AVSS = –2.5 V), gain = 1, and a resistor divider in front of the ADS122C04. The resistor divider must divide the voltage down to ≤ ±2.048 V in order to measure the voltage using the internal 2.048-V reference.

10.1.7 Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS122C04 in continuous conversion mode. The $\overline{DRDY}$ pin is used to indicate availability of new conversion data. The default configuration register settings are changed to gain = 16, continuous conversion mode.

```
Power-up;
Delay to allow power supplies to settle and power-on reset to complete; minimum of 500 µs;
Configure the I2C interface of the microcontroller;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;

Send the RESET command (06h) to make sure the device is properly reset after power-up;


Write the respective register configurations with the WREG command (40h, 08h, 42h, 08h);
As an optional sanity check, read back all configuration registers with the RREG command (2xh);

Send the START/SYNC command (08h) to start converting in continuous conversion mode;

Loop
{
    Wait for DRDY to transition low;
    Send the RDATA command (10h) to read 3 bytes of conversion data;
}

Send the POWERDOWN command (02h) to stop conversions and put the device in power-down mode;
```

TI recommends running an offset calibration before performing any measurements or when changing the gain of the PGA. The internal offset of the device can, for example, be measured by shorting the inputs to mid-supply (MUX[3:0] = 1110). The microcontroller then takes multiple readings from the device with the inputs shorted and stores the average value in the microcontroller memory. When measuring the sensor signal, the microcontroller then subtracts the stored offset value from each device reading to obtain an offset compensated result; the offset can be either positive or negative in value.

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10.2 Typical Applications

10.2.1 K-Type Thermocouple Measurement (–200°C to +1250°C)

図 71 shows the basic connections of a thermocouple measurement system when using an external high-precision temperature sensor for cold-junction compensation. Apart from the thermocouple itself, the only external circuitry required are two biasing resistors, a simple low-pass, antialiasing filter, and the power-supply decoupling capacitors.

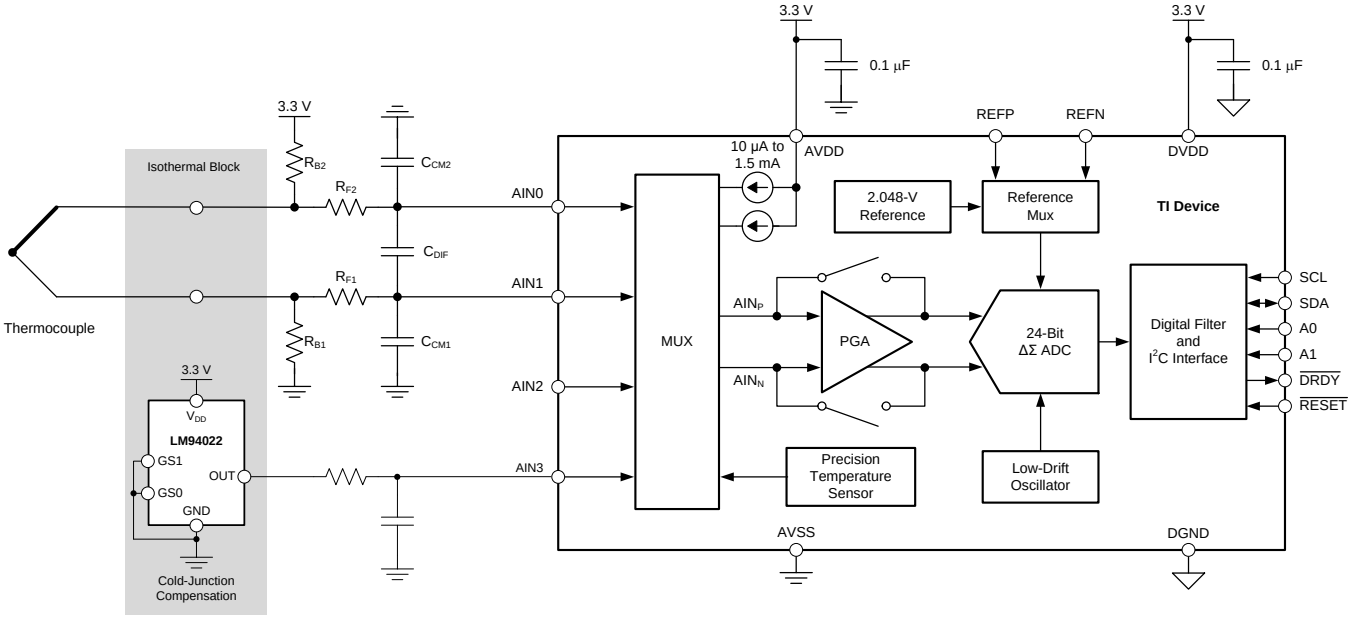


図 71. Thermocouple Measurement

10.2.1.1 Design Requirements

表 24. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Reference voltage	Internal 2.048-V reference
Update rate	≥10 readings per second
Thermocouple type	K
Temperature measurement range	–200°C to +1250°C
Measurement accuracy at T_A = 25°C (1)	±0.2°C

(1) Not accounting for the error of the thermocouple and cold-junction temperature measurement; offset calibration at $T_{(TC)} = T_{(CJ)}$ = 25°C; no gain calibration.

10.2.1.2 Detailed Design Procedure

The biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple such that the input voltages do not exceed the absolute input voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, either a bipolar supply (for example, AVDD = 2.5 V and AVSS = –2.5 V) must be used for the device to meet the absolute input voltage requirement of the PGA, or the PGA must be bypassed. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

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In addition to biasing the thermocouple, R_{B1} and R_{B2} are also useful for detecting an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs (AIN0 and AIN1) to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

Although the device digital filter attenuates high-frequency components of noise, performance can be further improved by providing a first-order, passive RC filter at the inputs. 式 9 calculates the cutoff frequency that is created by the differential RC filter formed by R_{F1}, R_{F2}, and the differential capacitor C_{DIF}.

$$f_C = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot C_{DIF}] \quad (9)$$

Two common-mode filter capacitors (C_{M1} and C_{M2}) are also added to offer attenuation of high-frequency, common-mode noise components. Choose a differential capacitor C_{DIF} that is at least an order of magnitude (10 times) larger than the common-mode capacitors (C_{M1} and C_{M2}) because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The filter resistors R_{F1} and R_{F2} also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels if an overvoltage on the inputs occur. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI therefore recommends limiting the filter resistor values to below 1 kΩ.

The filter component values used in this design are: $R_{F1} = R_{F2} = 1$ kΩ, $C_{DIF} = 100$ nF, and $C_{CM1} = C_{CM2} = 10$ nF.

The highest measurement resolution is achieved when matching the largest potential input signal to the FSR of the ADC by choosing the highest possible gain. From the design requirement, the maximum thermocouple voltage occurs at $T_{(TC)} = 1250$°C and is $V_{(TC)} = 50.644$ mV as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature of $T_{(CJ)} = 0$°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at $T_{(TC)} = 1250$°C produces an output voltage of $V_{(TC)} = 50.644$ mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of $T_{(CJ)} = –40$°C. The maximum gain that can be applied when using the internal 2.048-V reference is then calculated as (2.048 V / 52.171 mV) = 39.3. The next smaller PGA gain setting that the device offers is 32.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. To measure the internal temperature of the ADS122C04, the device must be set to internal temperature sensor mode by setting the TS bit to 1 in the configuration register. For best performance, careful board layout is critical to achieve good thermal conductivity between the cold junction and the device package.

However, the device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. An algorithm similar to the following must be implemented on the microcontroller to compensate for the cold-junction temperature:

1. Measure the thermocouple voltage, $V_{(TC)}$, between AIN0 and AIN1
2. Measure the temperature of the cold junction, $T_{(CJ)}$, using the temperature sensor mode of the ADS122C04
3. Convert the cold-junction temperature into an equivalent thermoelectric voltage, $V_{(CJ)}$, using the tables or equations provided by NIST
4. Add $V_{(TC)}$ and $V_{(CJ)}$ and translate the summation back into a thermocouple temperature using the NIST tables or equations again

In some applications, the integrated temperature sensor of the ADS122C04 cannot be used (for example, if the accuracy is not high enough or if the device cannot be placed close enough to the cold junction). The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor, RTD, or an analog temperature sensor. 図 71 illustrates the LM94022 temperature sensor being used for cold-junction compensation.

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As shown in 式 10, the rms noise of the ADS122C04 at gain = 32 and DR = 20 SPS (0.24 μV_{rms}) is divided by the average sensitivity of a K-type thermocouple (41 µV/°C) to obtain an approximation of the achievable temperature resolution.

Temperature Resolution = 0.24 µV / 41 µV/°C = 0.006°C (10)

表 25 shows the register settings for this design.

表 25. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	0Ah	AIN_P = AIN0, AIN_N = AIN1, gain = 32, PGA enabled(1)
01h	08h	DR = 20 SPS, normal mode, continuous conversion mode, internal reference
02h	00h	Conversion data counter disabled, data integrity disabled, burnout current sources disabled, IDACs off
03h	00h	No IDACs used

(1) To measure the cold junction temperature using the LM90422, change register 00h to B1h (AIN_P = AIN3, AIN_N = AVSS, gain = 1, PGA disabled).

10.2.1.3 Application Curves

図 72 and 図 73 show the measurement results. The measurements are taken at $T_A = T_{(CJ)}$ = 25°C. A system offset calibration is performed at $T_{(TC)}$ = 25°C, which translates to a $V_{(TC)}$ = 0 V when $T_{(CJ)}$ = 25°C. No gain calibration is implemented. The data in 図 72 are taken using a precision voltage source as the input signal instead of a thermocouple. The respective temperature measurement error in 図 73 is calculated from the data in 図 72 using the NIST tables.

The design meets the required temperature measurement accuracy given in 表 24. The measurement error shown in 図 73 does not include the error of the thermocouple itself nor the measurement error of the cold-junction temperature. Those two error sources are in general larger than 0.2°C and therefore, in many cases, dominate the overall system measurement accuracy.

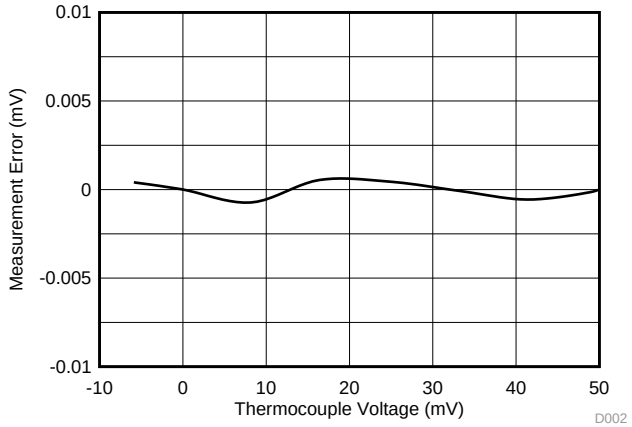


図 72. Voltage Measurement Error vs $V_{(TC)}$

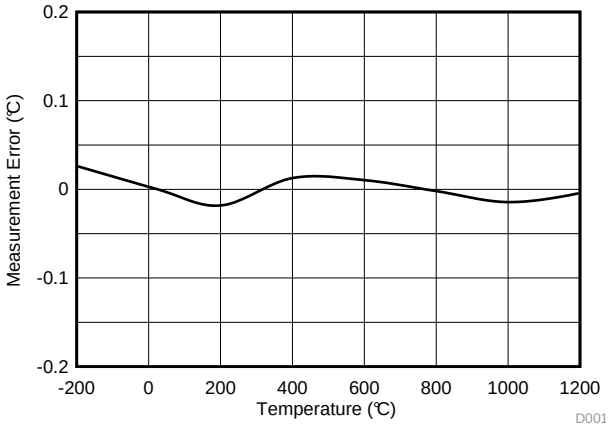


図 73. Temperature Measurement Error vs $T_{(TC)}$

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10.2.2 3-Wire RTD Measurement (–200°C to +850°C)

The ADS122C04 integrates all necessary features (such as dual-matched programmable current sources, buffered reference inputs, and a PGA) to ease the implementation of ratiometric 2-, 3-, and 4-wire RTD measurements. 図 74 shows a typical implementation of a ratiometric 3-wire RTD measurement using the excitation current sources integrated in the device to excite the RTD as well as to implement automatic RTD lead-resistance compensation.

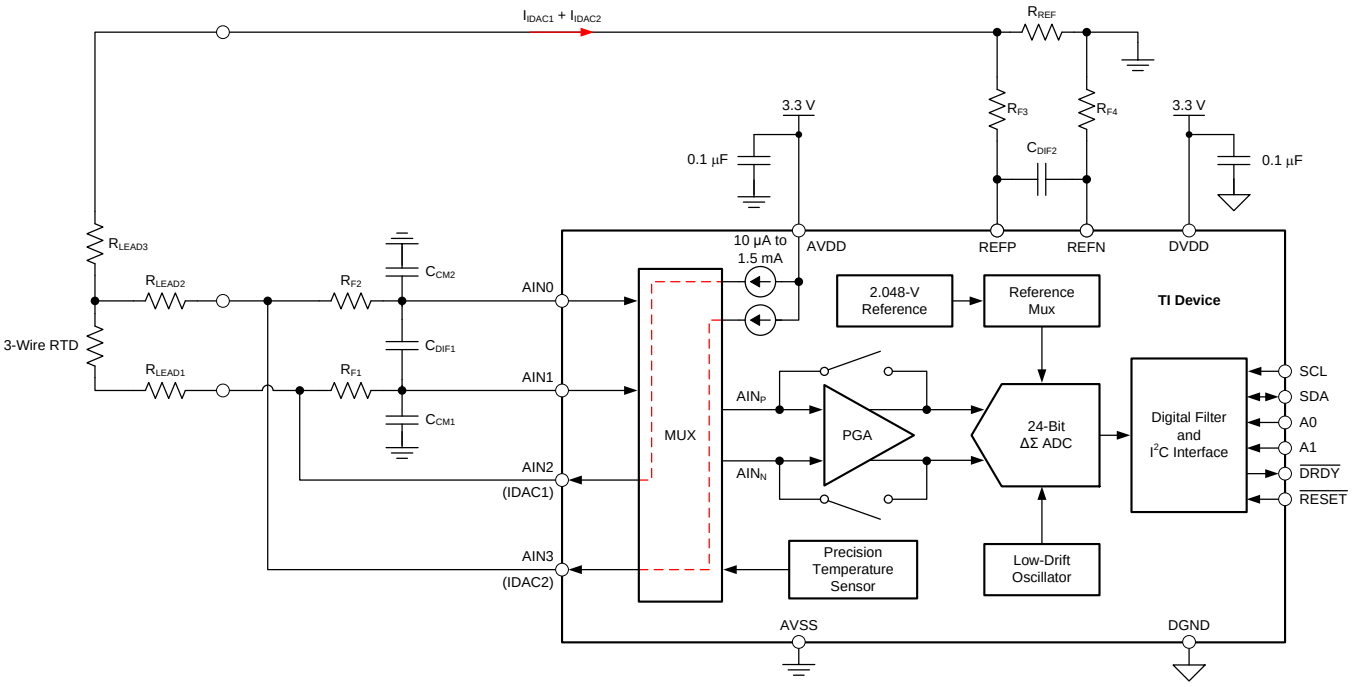


図 74. 3-Wire RTD Measurement

10.2.2.1 Design Requirements

表 26. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Update rate	20 readings per second
RTD type	3-wire Pt100
Maximum RTD lead resistance	15 Ω
RTD excitation current	500 µA
Temperature measurement range	–200°C to +850°C
Measurement accuracy at T_A = 25°C (1)	±0.2°C

(1) Not accounting for the error of RTD; offset calibration is performed with R_{RTD} = 100 Ω; no gain calibration.

10.2.2.2 Detailed Design Procedure

The circuit in 図 74 employs a ratiometric measurement approach. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise of the excitation source cancel out because these errors are common to both the sensor signal and the reference.

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In order to implement a ratiometric 3-wire RTD measurement using the device, IDAC1 is routed to one of the leads of the RTD and IDAC2 is routed to the second RTD lead. Both currents have the same value, which is programmable by the IDAC[2:0] bits in the configuration register. The design of the device ensures that both IDAC values are closely matched, even across temperature. The sum of both currents flows through a precision, low-drift reference resistor, R_{REF}. The voltage, V_{REF}, generated across the reference resistor (as shown in 式 11) is used as the ADC reference voltage. 式 11 reduces to 式 12 because $I_{IDAC1} = I_{IDAC2}$.

$$V_{REF} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (11)$$

$$V_{REF} = 2 \cdot I_{IDAC1} \cdot R_{REF} \quad (12)$$

To simplify the following discussion, the individual lead resistance values of the RTD (R_{LEADx}) are set to zero. As 式 13 shows, only IDAC1 excites the RTD to produce a voltage (V_{RTD}) proportional to the temperature-dependent RTD value and the IDAC1 value.

$$V_{RTD} = R_{RTD\ (at\ temperature)} \cdot I_{IDAC1} \quad (13)$$

The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code proportional to 式 14 through 式 16:

$$Code \propto V_{RTD} \cdot Gain / V_{REF} \quad (14)$$

$$Code \propto (R_{RTD\ (at\ temperature)} \cdot I_{IDAC1} \cdot Gain) / (2 \cdot I_{IDAC1} \cdot R_{REF}) \quad (15)$$

$$Code \propto (R_{RTD\ (at\ temperature)} \cdot Gain) / (2 \cdot R_{REF}) \quad (16)$$

As shown in 式 16, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly affects the measurement result, choosing a reference resistor with a very low temperature coefficient is important to limit errors introduced by the temperature drift of R_{REF}.

The second IDAC2 is used to compensate for errors introduced by the voltage drop across the lead resistance of the RTD. All three leads of a 3-wire RTD typically have the same length and, thus, the same lead resistance. Also, IDAC1 and IDAC2 have the same value. Taking the lead resistance into account, use 式 17 to calculate the differential voltage (V_{IN}) across the ADC inputs (AIN0 and AIN1):

$$V_{IN} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \quad (17)$$

式 17 reduces to 式 18 when $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$:

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \quad (18)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated, as long as the lead resistance values and the IDAC values are well matched.

A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs, as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}). The same guidelines for designing the input filter apply as described in the *K-Type Thermocouple Measurement* section. Match the corner frequencies of the input and reference filter for best performance. For more detailed information on matching the input and reference filter, see the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248* application report.

The reference resistor R_{REF} not only serves to generate the reference voltage for the device, but also sets the voltages at the leads of the RTD to within the specified absolute input voltage range of the PGA.

When designing the circuit, care must also be taken to meet the compliance voltage requirement of the IDACs. The IDACs require that the maximum voltage drop developed across the current path to AVSS be equal to or less than AVDD – 0.9 V in order to operate accurately. This requirement means that 式 19 must be met at all times.

$$AVSS + I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{REF}) \leq AVDD - 0.9\ V \quad (19)$$

The device also offers the possibility to route the IDACs to the same inputs used for measurement. If the filter resistor values R_{F1} and R_{F2} in 図 74 are small enough and well matched, then IDAC1 can be routed to AIN1 and IDAC2 to AIN0. In this manner, even two 3-wire RTDs sharing the same reference resistor can be measured with a single device.

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As stated in 表 26, this design example discusses the implementation of a 3-wire Pt100 measurement to be used to measure temperatures ranging from –200°C to +850°C. The excitation current for the Pt100 is chosen as I_{IDAC1} = 500 µA, which means a combined current of 1 mA is flowing through the reference resistor, R_{REF}. As mentioned previously, besides creating the reference voltage for the ADS122C04, the voltage across R_{REF} also sets the absolute input voltages for the RTD measurement. In general, choose the largest reference voltage possible that maintains the compliance voltage of the IDACs and meets the absolute input voltage requirement of the PGA. Setting the common-mode voltage at or near half the analog supply (in this case 3.3 V / 2 = 1.65 V) in most cases satisfies the absolute input voltage requirements of the PGA. 式 20 is then used to calculate the value for R_{REF}:

$$R_{REF} = V_{REF} / (I_{IDAC1} + I_{IDAC2}) = 1.65\ V / 1\ mA = 1.65\ k\Omega \quad (20)$$

The stability of R_{REF} is critical to achieve good measurement accuracy over temperature and time. Choosing a reference resistor with a temperature coefficient of ±10 ppm/°C or better is advisable. If a 1.65-kΩ value is not readily available, another value near 1.65 kΩ (such as 1.62 kΩ or 1.69 kΩ) can certainly be used as well.

As a last step, the PGA gain must be selected in order to match the maximum input signal to the FSR of the ADC. The resistance of a Pt100 increases with temperature. Therefore, the maximum voltage to be measured (V_{INMAX}) occurs at the positive temperature extreme. At 850°C, a Pt100 has an equivalent resistance of approximately 391 Ω as per the NIST tables. The voltage across the Pt100 equates to 式 21:

$$V_{INMAX} = V_{RTD\ (at\ 850°C)} = R_{RTD\ (at\ 850°C)} \cdot I_{IDAC1} = 391\ \Omega \cdot 500\ \mu A = 195.5\ mV \quad (21)$$

The maximum gain that can be applied when using a 1.65-V reference is then calculated as (1.65 V / 195.5 mV) = 8.4. The next smaller PGA gain setting available in the ADS122C04 is 8. At a gain of 8, the ADS122C04 offers a FSR value as described in 式 22:

$$FSR = \pm V_{REF} / Gain = \pm 1.65\ V / 8 = \pm 206.25\ mV \quad (22)$$

This range allows for margin with respect to initial accuracy and drift of the IDACs and reference resistor.

After selecting the values for the IDACs, R_{REF}, and PGA gain, make sure to double check that the settings meet the absolute input voltage requirements of the PGA and the compliance voltage of the IDACs. To determine the true absolute input voltages at the ADC inputs (AIN0 and AIN1), the lead resistance must be taken into account as well.

The smallest absolute input voltage occurs on AIN0 at the lowest measurement temperature (–200°C) with R_{LEADx} = 0 Ω, and is equal to V_{REF} = 1.65 V.

The minimum absolute input voltage must not exceed the limit set in 式 7 to meet 式 23:

$$V_{AIN0\ (MIN)} \geq AVSS + 0.2\ V + |V_{INMAX}| \cdot (Gain - 4) / 8 = 0\ V + 0.2\ V + 97.75\ mV = 297.75\ mV \quad (23)$$

The restriction is satisfied with V_{AIN0} = 1.65 V.

The largest absolute input voltage (calculated using 式 24 and 式 25) occurs on AIN1 at the highest measurement temperature (850°C).

$$V_{AIN1\ (MAX)} = V_{REF} + (I_{IDAC1} + I_{IDAC2}) \cdot R_{LEAD3} + I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD\ (at\ 850°C)}) \quad (24)$$

$$V_{AIN1\ (MAX)} = 1.65\ V + 1\ mA \cdot 15\ \Omega + 500\ \mu A \cdot (15\ \Omega + 391\ \Omega) = 1.868\ V \quad (25)$$

$V_{AIN1\ (MAX)}$ meets the requirement given by 式 7 and equates to 式 26 in this design:

$$V_{AINP\ (MAX)} \leq AVDD - 0.2\ V - |V_{INMAX}| \cdot (Gain - 4) / 8 = 3.3\ V - 0.2\ V - 97.75\ mV = 3.002\ V \quad (26)$$

The restriction on the compliance voltage (AVDD – 0.9 V = 3.3 V – 0.9 V = 2.4 V) of IDAC1 is met as well.

表 27 shows the register settings for this design.

表 27. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	36h	AIN_P = AIN1, AIN_N = AIN0, gain = 8, PGA enabled
01h	0Ah	DR = 20 SPS, normal mode, continuous conversion mode, external reference
02h	55h	Conversion data counter disabled, data integrity disabled, burnout current sources disabled, IDAC = 500 µA
03h	70h	IDAC1 = AIN2, IDAC2 = AIN3

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10.2.2.2.1 Design Variations for 2-Wire and 4-Wire RTD Measurements

Implementing a 2- or 4-wire RTD measurement is very similar to the 3-wire RTD measurement illustrated in 図 74, except that only one IDAC is required.

図 75 shows a typical circuit implementation of a 2-wire RTD measurement. The main difference compared to a 3-wire RTD measurement is with respect to the lead resistance compensation. The voltage drop across the lead resistors, R_{LEAD1} and R_{LEAD2}, in this configuration is directly part of the measurement (as shown in 式 27) because there is no means to compensate the lead resistance by use of the second current source. Any compensation must be done by calibration.

$$V_{IN} = I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD} + R_{LEAD2}) \quad (27)$$

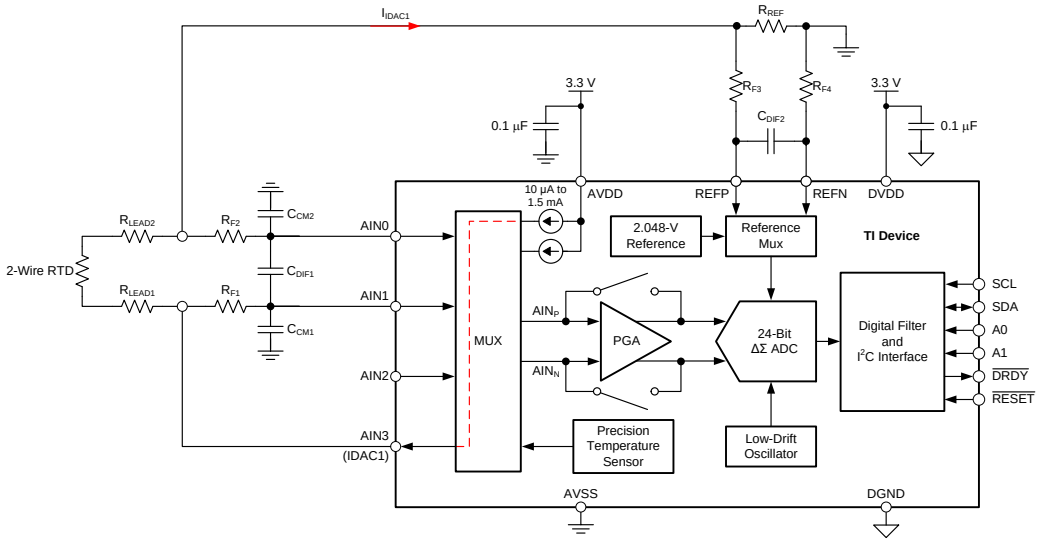


図 75. 2-Wire RTD Measurement

図 76 shows a typical circuit implementation of a 4-wire RTD measurement. Similar to the 2-wire RTD measurement, only one IDAC is required for exciting and measuring a 4-wire RTD in a ratiometric manner. The main benefit of using a 4-wire RTD is that the ADC inputs are connected to the RTD in the form of a Kelvin connection. Apart from the input leakage currents of the ADC, there is no current flow through the lead resistors R_{LEAD2} and R_{LEAD3} and therefore no voltage drop is created across them. The voltage at the ADC inputs consequently equals the voltage across the RTD and the lead resistance is of no concern.

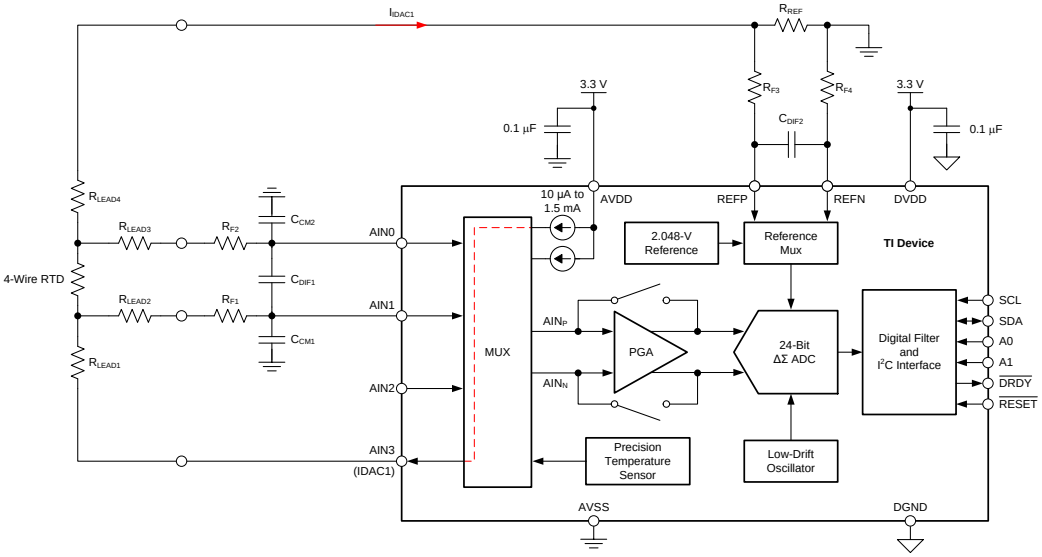


図 76. 4-Wire RTD Measurement

As shown in 式 28, the transfer function of a 2- and 4-wire RTD measurement differs compared to the one of a 3-wire RTD measurement by a factor of 2 because only one IDAC is used and only one IDAC flows through the reference resistor, R_{REF}.

$$\text{Code} \propto (R_{RTD\ (at\ Temperature)} \cdot \text{Gain}) / R_{REF} \quad (28)$$

In addition, the input common-mode voltage and reference voltage is reduced compared to the 3-wire RTD configuration. Therefore, some further modifications may be required in case the 3-wire RTD design is used to measure 2- and 4-wire RTDs as well. If the decreased absolute input voltages does not meet the minimum absolute voltage requirements of the PGA anymore, either increase the value of R_{REF} by switching in a larger resistor or, alternatively, increase the excitation current and decrease the gain at the same time.

10.2.2.3 Application Curves

図 77 and 図 78 show the measurement results. The measurements are taken at T_A = 25°C. A system offset calibration is performed using a reference resistor of 100 Ω. No gain calibration is implemented. The data in 図 77 are taken using precision resistors instead of a 3-wire Pt100. The respective temperature measurement error in 図 78 is calculated from the data in 図 77 using the NIST tables.

The design meets the required temperature measurement accuracy given in 表 26. However, the measurement error shown in 図 78 does not include the error of the RTD itself.

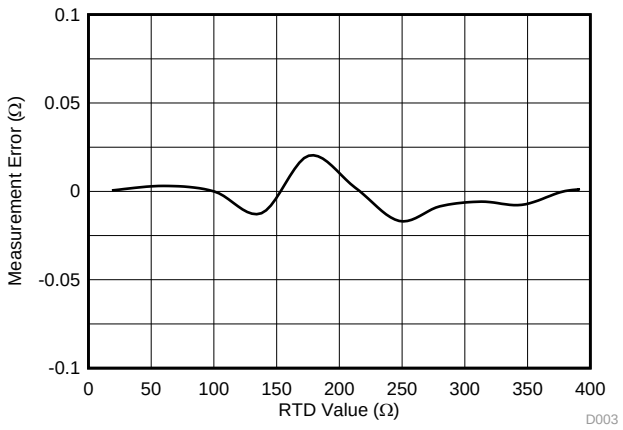


図 77. Resistance Measurement Error vs R_{RTD}

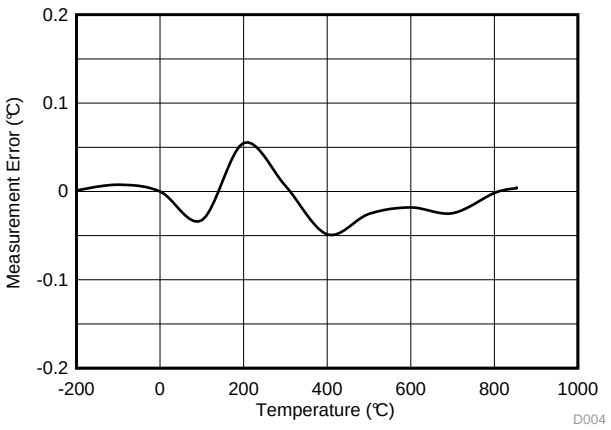
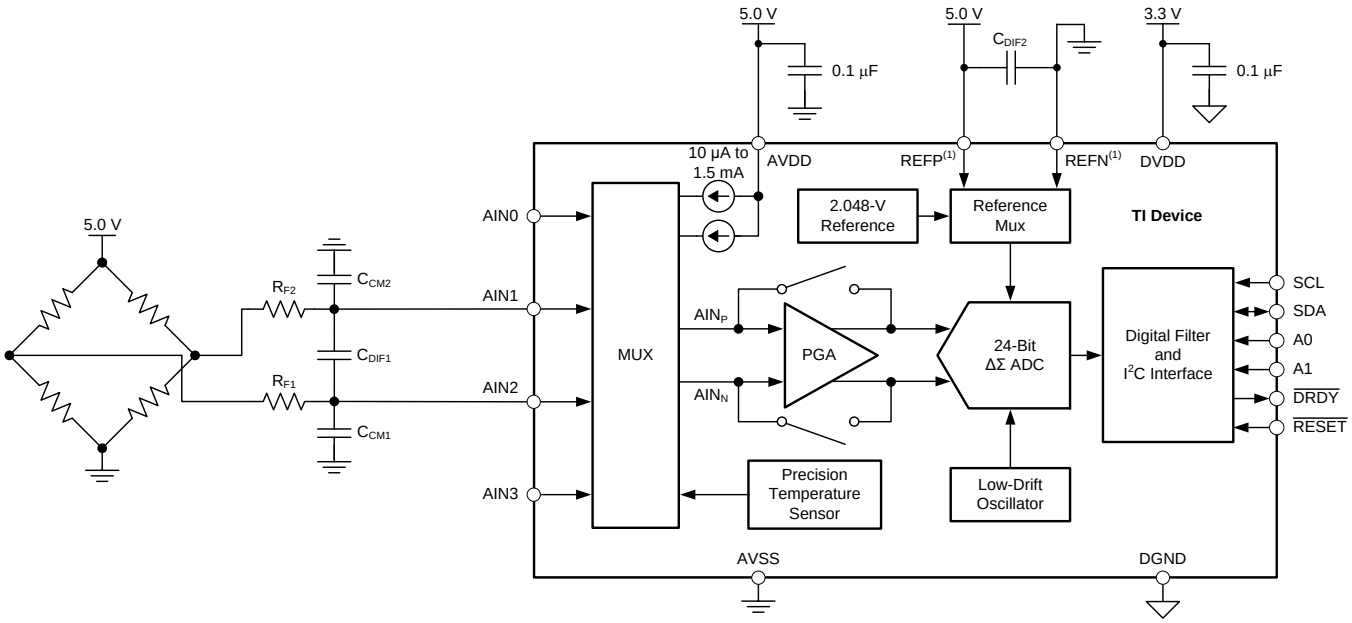


図 78. Temperature Measurement Error vs $T_{(RTD)}$

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10.2.3 Resistive Bridge Measurement

The device offers several features to ease the implementation of ratiometric bridge measurements (such as a PGA with gains up to 128, buffered, and differential reference inputs).



(1) Connect reference inputs directly to the bridge excitation voltage through Kelvin connections.

図 79. Resistive Bridge Measurement

10.2.3.1 Design Requirements

表 28. Design Requirements

DESIGN PARAMETER	VALUE
Analog supply voltage	5.0 V
Digital supply voltage	3.3 V
Load cell type	4-wire load cell
Load cell maximum capacity	1 kg
Load cell sensitivity	3 mV/V
Excitation voltage	5 V
Repeatability	50 mg

10.2.3.2 Detailed Design Procedure

As shown in 図 79, the bridge excitation voltage is simultaneously used as the reference voltage for the ADC to implement a ratiometric bridge measurement. With this configuration, any drift in excitation voltage also shows up on the reference voltage, consequently canceling out drift error. Either the dedicated reference inputs can be used, or the analog supply can be used as the reference if the supply is used to excite the bridge.

The PGA offers gains up to 128, which helps amplify the small differential bridge output signal to make optimal use of the ADC full-scale range. Using a symmetrical bridge with the excitation voltage equal to the supply voltage of the device ensures that the output signal of the bridge meets the absolute input voltage requirement of the PGA.

Using a 3-mV/V load cell with a 5-V excitation yields a maximum differential voltage at the ADC inputs of V_{INMAX} = 15 mV at maximum load. 式 29 then calculates the maximum gain that can be used.

$$\text{Gain} \le V_{REF} / V_{INMAX} = 5\ V / 15\ mV = 333.3 \quad (29)$$

Accordingly, gain = 128 is used in this example.

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A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs. The reference has an additional capacitor C_{DIF2} to limit reference noise. Care must be taken to maintain a limited amount of filtering or the measurement is no longer ratiometric.

To find the repeatability of the readings, perform the following calculation. The load cell produces an output voltage of 15 mV at the maximum load of 1 kg. At a gain = 128 and DR = 20 SPS the ADS122C04 offers a noise-free resolution of 0.46 μV_{PP}. 式 30 then calculates the repeatability.

$$\text{Repeatability} = (1\ \text{kg} / 15\ \text{mV}) \cdot 0.46\ \mu\text{V} = 31\ \text{mg} \quad (30)$$

表 29 shows the register settings for this design.

表 29. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	4Eh	AIN_P = AIN1, AIN_N = AIN2, gain = 128, PGA enabled
01h	0Ah	DR = 20 SPS, normal mode, continuous conversion mode, external reference
02h	98h	Conversion data counter disabled, data integrity disabled, burnout current sources disabled, IDACs off
03h	00h	No IDACs used

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11 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels.

11.1 Power-Supply Sequencing

The power supplies can be sequenced in any order, but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage and current limits. Wait approximately 500 µs after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. As shown in 図 80 and 図 81, AVDD, AVSS (when using a bipolar supply), and DVDD must be decoupled with at least a 0.1-µF capacitor. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital grounds together as close to the device as possible.

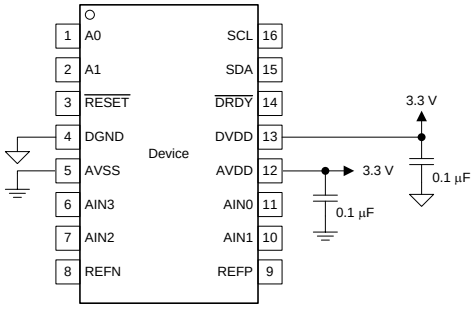


図 80. Unipolar Analog Power Supply

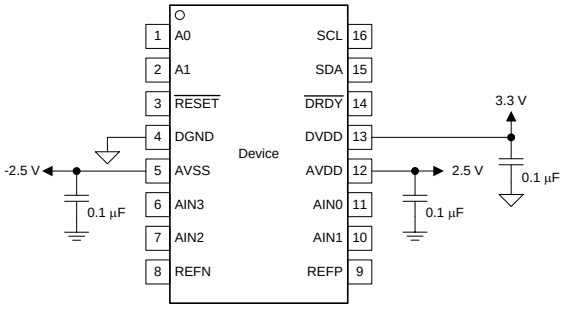


図 81. Bipolar Analog Power Supply

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12 Layout

12.1 Layout Guidelines

Employing best design practices is recommended when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. 図 82 shows an example of good component placement. Although 図 82 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

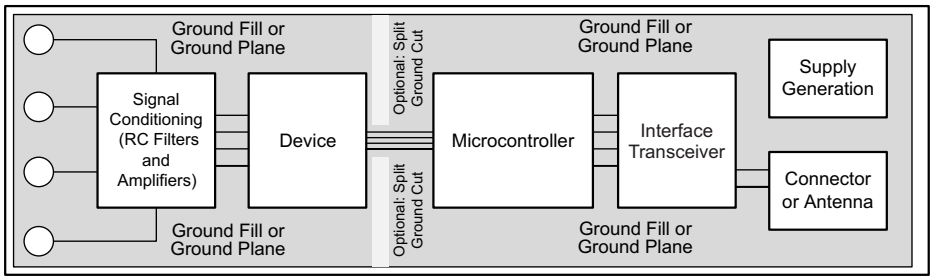


図 82. System Component Placement

The following basic recommendations for layout of the ADS122C04 help achieve the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Routing digital lines away from analog lines prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If forced into a larger path, the chance that the signal radiates increases. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduces the high-frequency impedance at the input of the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic thermocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines (such as AIN0, AIN1 and AIN2, AIN3). The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO) that have stable properties and low noise characteristics.

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12.2 Layout Example

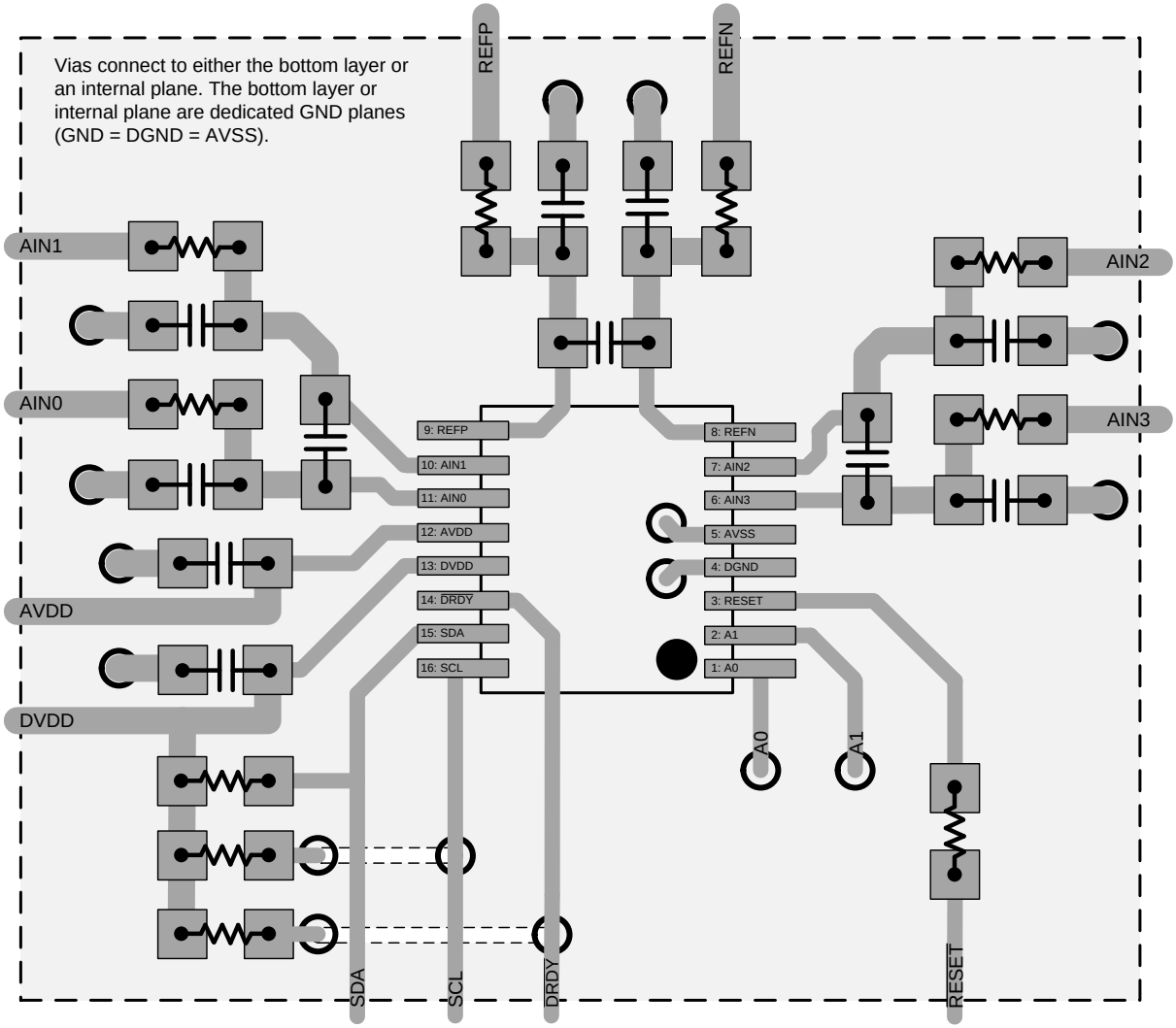


図 83. Layout Example

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13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

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13.2 ドキュメントのサポート

13.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『REF50xx 低ノイズ、超低ドリフト、高精度基準電圧』データシート*
- テキサス・インスツルメンツ、*『LM94022/-Q1 1.5V、SC70 パッケージ、マルチゲイン選択可、クラス AB 出力段内蔵アナログ温度センサ』データシート*
- テキサス・インスツルメンツ、*『ADS1148およびADS1248を使用したRTDレシオメトリック測定およびフィルタリング』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『高精度デルタ-シグマADCを使用する低コスト、シングルチップの差動温度測定ソリューション』*Tech Note

13.3 ドキュメントの更新通知を受け取る方法

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13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS122C04IPW	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IPW.B	Active	Production	TSSOP (PW) | 16	90 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IPWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IPWRG4.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS122C
ADS122C04IRTER	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	122C
ADS122C04IRTER.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	122C
ADS122C04IRTERG4	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	122C
ADS122C04IRTERG4.B	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	122C
ADS122C04IRTET	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(122C, 122C4)
ADS122C04IRTET.B	Active	Production	WQFN (RTE) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(122C, 122C4)

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(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

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(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

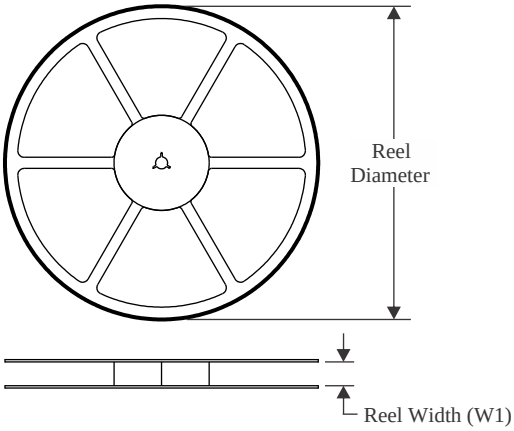
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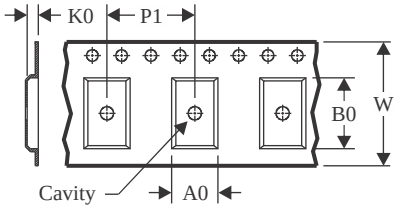
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

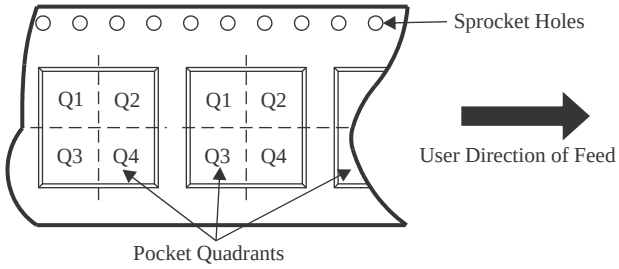


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

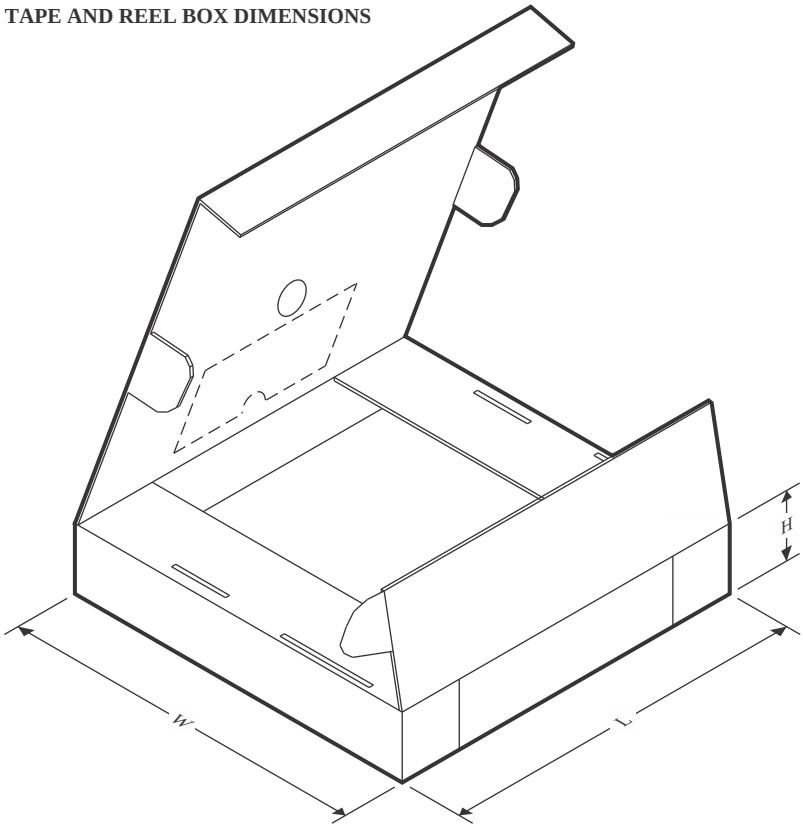
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS122C04IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS122C04IPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS122C04IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
ADS122C04IRTERG4	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
ADS122C04IRTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

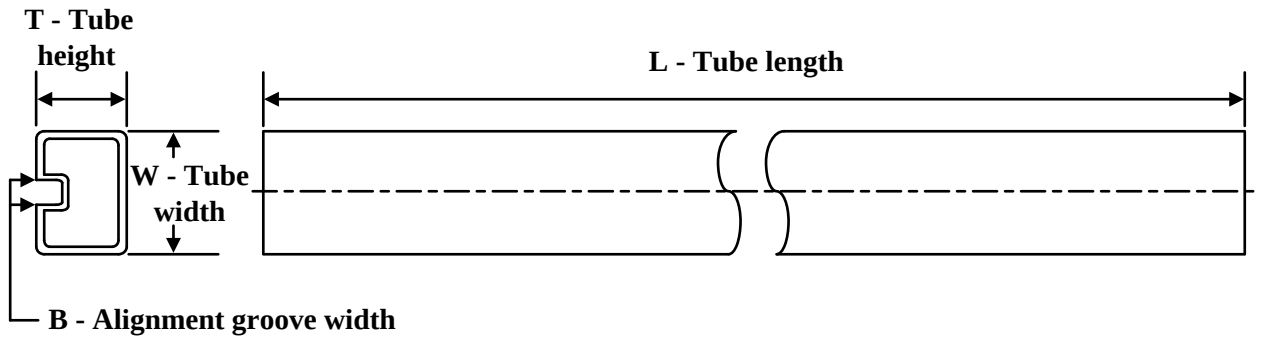
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS122C04IPWR	TSSOP	PW	16	2000	353.0	353.0	32.0
ADS122C04IPWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
ADS122C04IRTER	WQFN	RTE	16	3000	367.0	367.0	38.0
ADS122C04IRTERG4	WQFN	RTE	16	3000	367.0	367.0	38.0
ADS122C04IRTET	WQFN	RTE	16	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

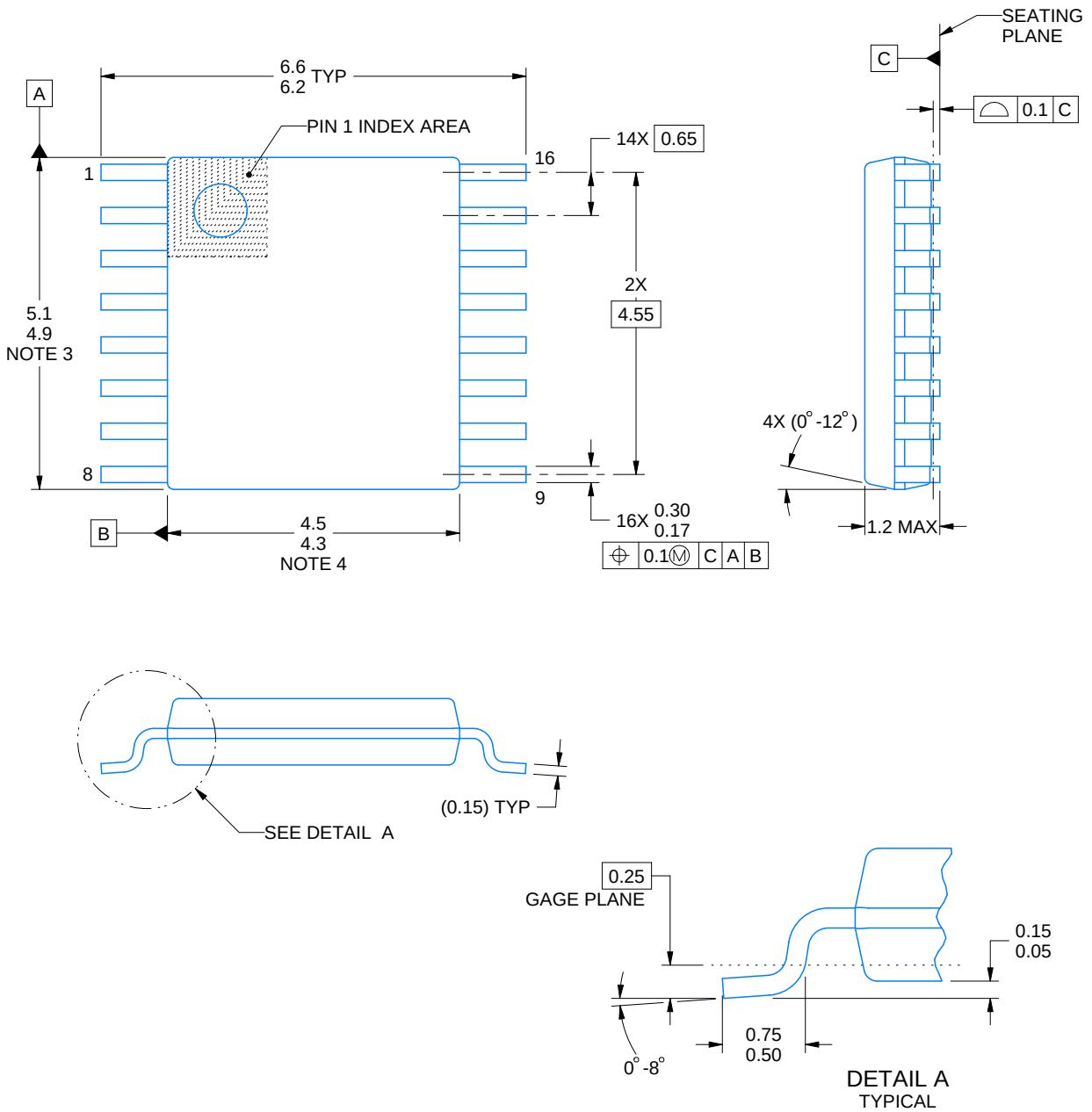
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS122C04IPW	PW	TSSOP	16	90	530	10.2	3600	3.5
ADS122C04IPW.B	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

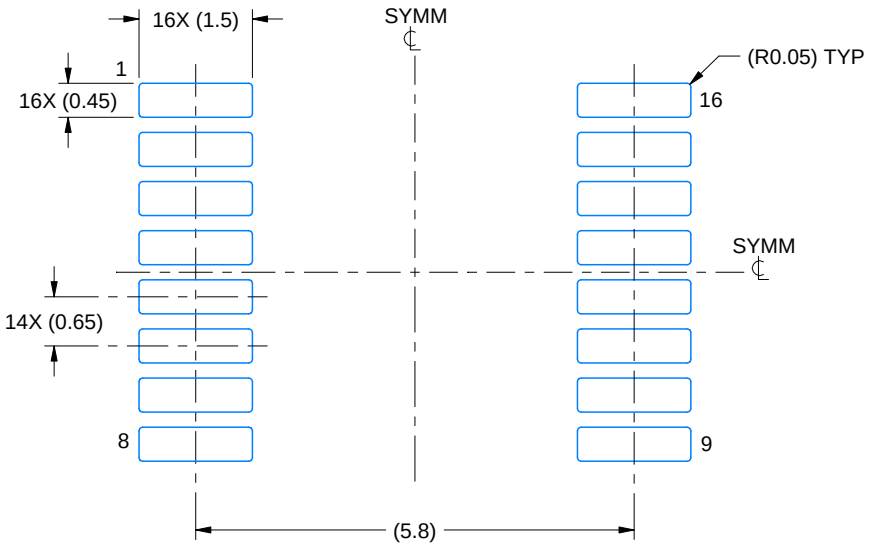
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

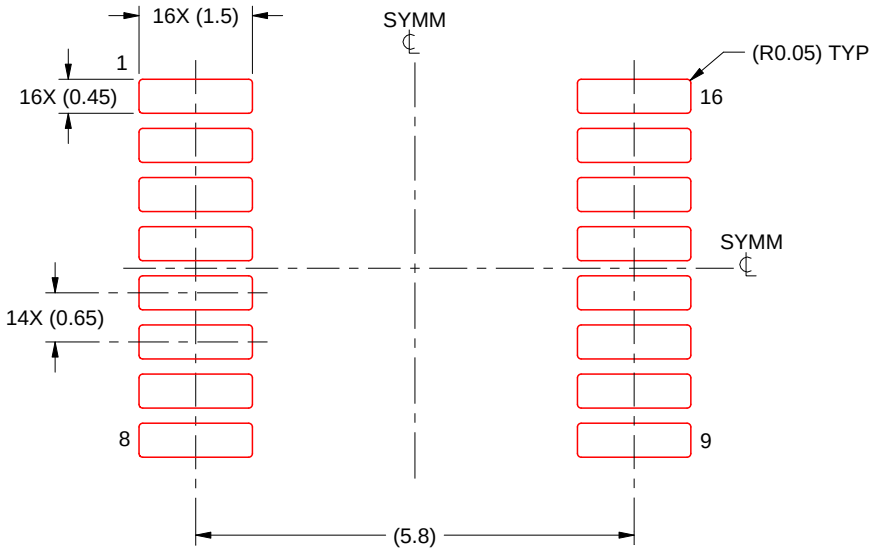


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

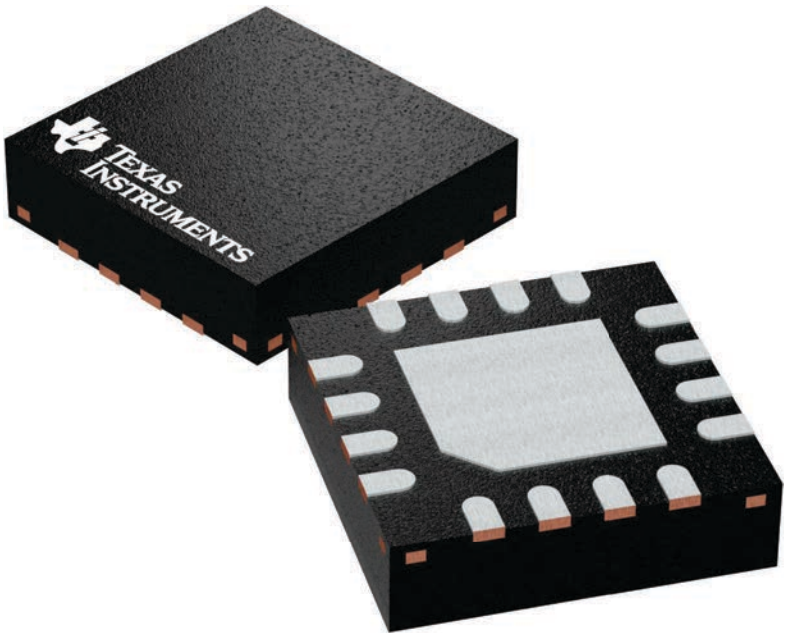
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

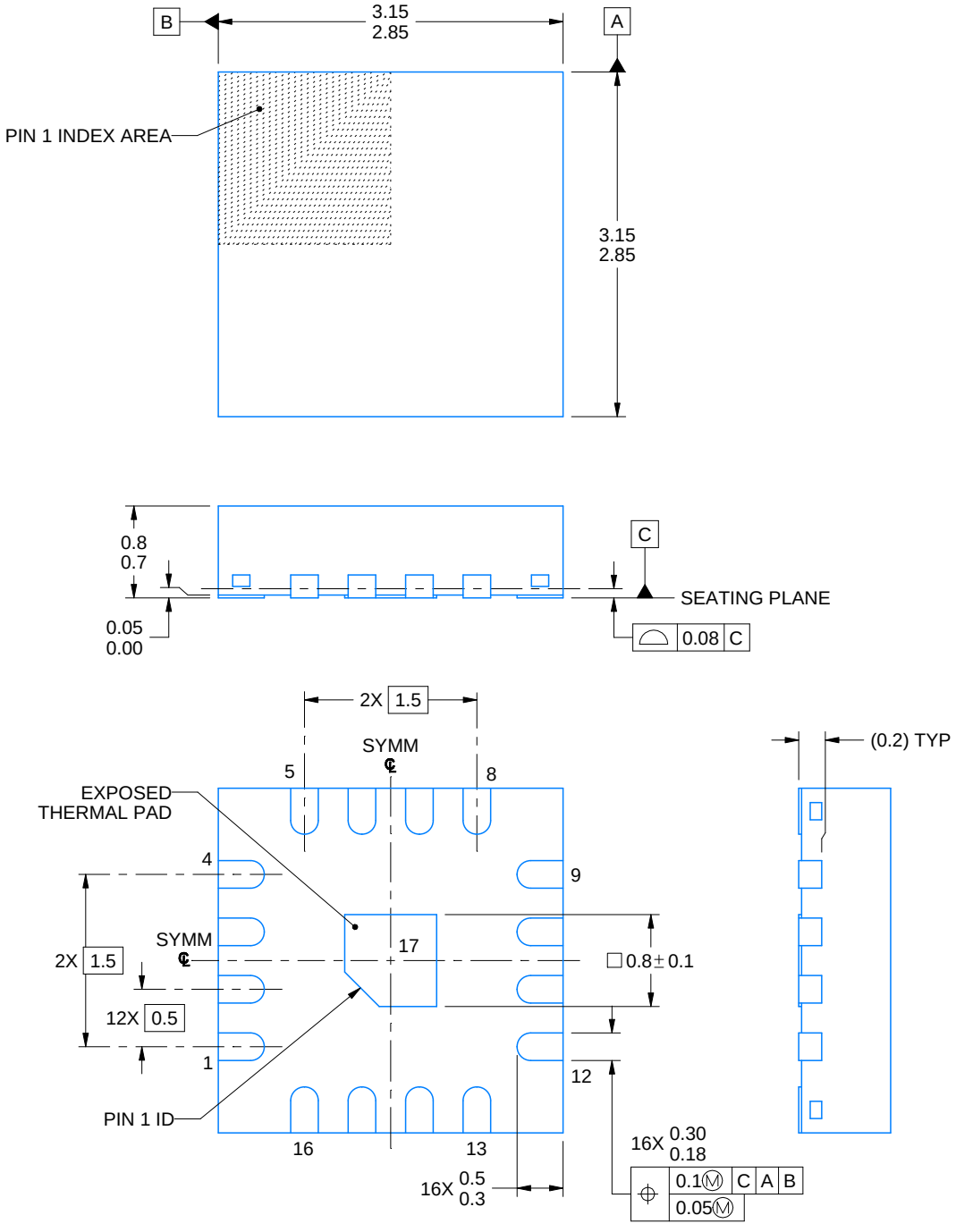


PACKAGE OUTLINE

RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

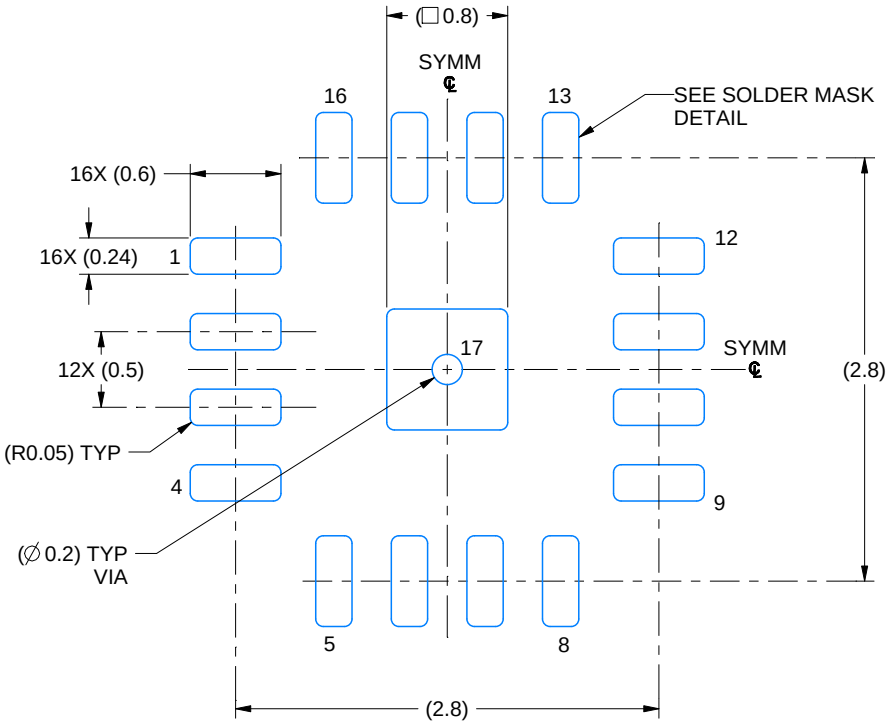
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

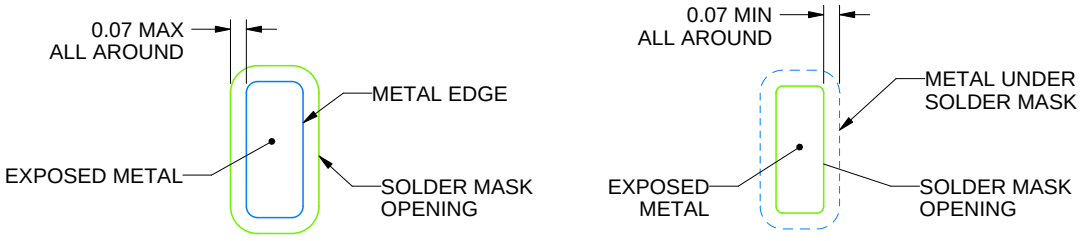
RTE0016D

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

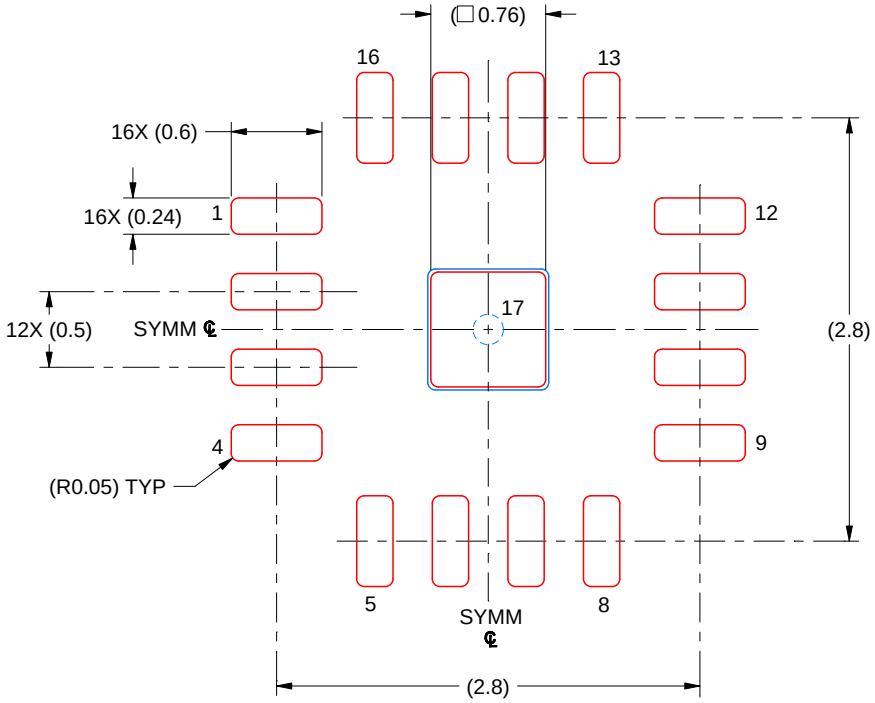


SOLDER MASK DETAILS

4219118/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219118/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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