ADS127L11 400kSPS、広帯域、24 ビット、デルタ・シグマ ADC

1 特長

- データ・レートをプログラム可能:
  - 最大 400kSPS (広帯域フィルタ)
  - 最大 1.067MSPS (低レイテンシ・フィルタ)
- デジタル・フィルタを選択可能:
  - 広帯域または低レイテンシ
- AC 精度および DC 精度:
  - ダイナミック・レンジ:111.5dB (200kSPS)
  - THD:-120dB
  - INL:0.9ppm FS
  - オフセット・ドリフト:50nV/℃
  - ゲイン・ドリフト:0.6ppm/℃
- 消費電力の拡張性が高いアーキテクチャ:
  - 高速モード:400kSPS、18.6mW
  - 低速モード:50kSPS、3.3mW
- 入力および基準電圧プリチャージ・バッファ
- 内部または外部クロック
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能

2 アプリケーション

- 試験および測定機器:
  - データ・アクイジション (DAQ)
  - 衝撃および振動計測器
  - 音響および動的歪みゲージ
- ファクトリ・オートメーション / 制御:
  - 状況監視
- 航空宇宙 / 防衛:
  - ソナー
- 医療:
  - 脳波 (EEG)
- グリッド・インフラ:
  - 電力品質分析器

3 概要

ADS127L11 は 24 ビットのデルタ・シグマ (ΔΣ) A/D コンバータ (ADC) で、データ・レートは広帯域フィルタ使用時に最大 400kSPS、低レイテンシ・フィルタ使用時に最大 1067kSPS です。本デバイスは、低消費電力 (高速モードで 18.6mW) で優れた AC 性能と DC 精度を備えています。

このデバイスには、入力バッファと基準電圧バッファが内蔵されており、信号負荷を減らすことができます。低ドリフトの変調器は、優れた DC 精度を備えており、小さい帯域内ノイズで AC 性能を向上しています。アーキテクチャは、消費電力に関する拡張性が高く、データ・レート、分解能、消費電力を最適化するために、2 つの速度モードを備えています。

デジタル・フィルタは広帯域または低レイテンシの動作に構成できるため、1 つのデバイスを広帯域の AC 特性か、DC 信号のデータ・スループットのどちらかに最適化できます。

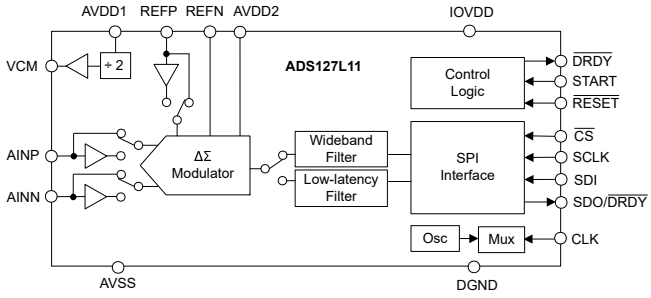
絶縁バリア越しの SPI I/O を簡素化するため、シリアル・インターフェイスはデイジー・チェーン機能を備えています。通信の信頼性を高めるため、入出力データは巡回冗長検査 (CRC) で検証されます。

小型の 3mm × 3mm WQFN パッケージと 6.5mm × 4.4mm TSSOP パッケージは省スペースのアプリケーションに適しています。本デバイスは、-40℃～+125℃の温度範囲について完全に動作が規定されています。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
ADS127L11	RUK (WQFN、20)	3.00mm × 3.00mm
	PW (TSSOP、20)	6.50mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2022) to Revision C (September 2022)	Page
• RUK (WQFN) パッケージをプレビューから量産データに変更	1
• Changed AVDD1 to DGND specification in *Recommended Operating Conditions* section	5
• Changed high-speed mode analog input precharge buffers off current drift specifications in *Electrical Characterisics* section	6
• Changed REFP input precharge buffer on current drift specification in *Electrical Characterisics* section	6
• Added *Long-Term Offset Drift* and *Long-Term Gain Drift* plots to *Typical Characteristics* section	13
• Added second paragraph to *Internal Oscillator* section	34
• Added footnote to *Wideband Filter Characteristics* table in *Wideband Filter* section	35
• Added footnote to *Sinc4 Filter Characteristics* table in *Sinc4 Filter* section	38
• Added footnote to *Sinc4 + Sinc1 Filter Characteristics* table in *Sinc4 + Sinc1 Filter* section	39
• Changed *Digital Supply Threshold* and *Analog Supply Threshold* figures in *Power-On Reset* section	43

Changes from Revision A (October 2021) to Revision B (April 2022)	Page
• Changed INL specification in *Electrical Characteristics* section	6
• Changed *SPI CRC* section	50

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5 Pin Configuration and Functions

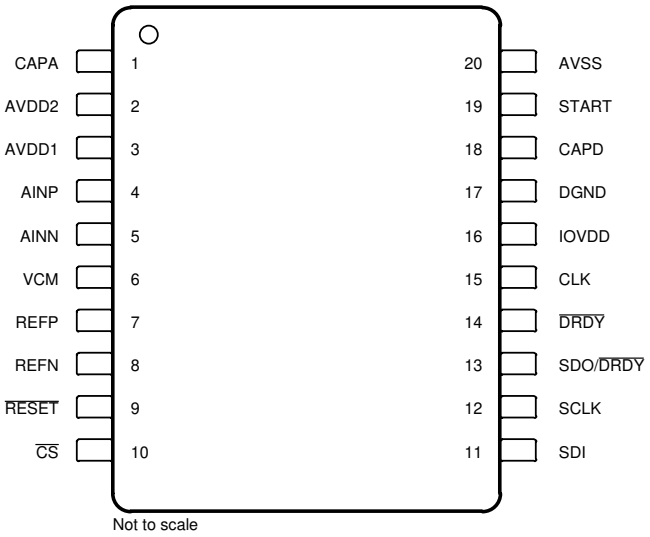

図 5-1. PW Package, 20-Pin TSSOP (Top View)

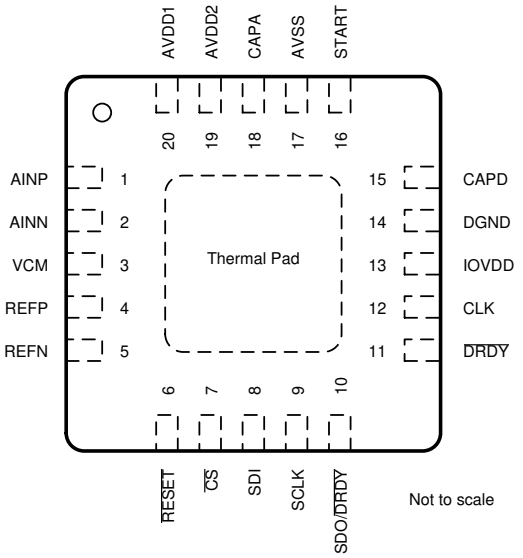

図 5-2. RUK Package, 20-Pin WQFN (Top View)

表 5-1. Pin Functions

NAME	PIN NO.		I/O	DESCRIPTION
	TSSOP	WQFN		
AINN	5	2	Analog input	Negative analog input; see the *Analog Input* section for details
AINP	4	1	Analog input	Positive analog input; see the *Analog Input* section for details
AVDD1	3	20	Analog Supply	Positive analog supply 1; see the *Power Supplies* section for details
AVDD2	2	19	Analog Supply	Positive analog supply 2; see the *Power Supplies* section for details
AVSS	20	17	Analog Supply	Negative analog supply; see the *Power Supplies* section for details
CAPA	1	18	Analog output	Analog voltage regulator output capacitor bypass
CAPD	18	15	Analog output	Digital voltage regulator output capacitor bypass
CLK	15	12	Digital input	Clock input; see the *Clock Operation* section for details
$\overline{CS}$	10	7	Digital input	Chip select, active low; see the *Chip Select* section for details
DGND	17	14	Ground	Digital ground
$\overline{DRDY}$	14	11	Digital output	Data ready, active low; see the *Data Ready* section for details
IOVDD	16	13	Digital Supply	I/O supply voltage; see the *Power Supplies* section for details
REFN	8	5	Analog input	Negative reference input; see the *Reference Voltage* section for details
REFP	7	4	Analog input	Positive reference input; see the *Reference Voltage* section for details
$\overline{RESET}$	9	6	Digital input	Reset, active low; see the *Reset* section for details
SCLK	12	9	Digital input	Serial data clock; see the *Serial Clock* section for details
SDI	11	8	Digital input	Serial data input; see the *Serial Data Input* section for details
SDO/$\overline{DRDY}$	13	10	Digital output	Serial data output and data ready (optional); see the *SDO/DRDY* section for details
START	19	16	Digital input	Conversion start; see the *Synchronization* section for details
VCM	6	3	Analog output	Common-mode voltage buffered output; see the *VCM Output Voltage* section for details
Thermal Pad	—	Pad	—	Thermal power pad; connect to AVSS

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power supply voltage	AVDD1 to AVSS	–0.3	6.5	V
	AVDD2 to AVSS	–0.3	6.5	
	AVSS to DGND	–3	0.3	
	IOVDD to DGND	–0.3	6.5	
	IOVDD to AVSS		8.5	
Analog input voltage	AINP, AINN, REFP, REFN	AVSS – 0.3	AVDD1 + 0.3	V
Analog output voltage	CAPA	AVSS	1.65	V
	CAPD	DGND	1.65	
	VCM	AVSS	AVDD1	
Digital input/output voltage	SDO/$\overline{\text{DRDY}}$, $\overline{\text{DRDY}}$, START	DGND – 0.3	IOVDD + 0.3	V
	$\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{RESET}}$, CLK	DGND – 0.3	6.5	
Input current	Continuous, any pin except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Analog input pins AINP, AINN, REFP, and REFN are diode-clamped to AVDD1 and AVSS. Limit the input current to 10 mA in the event the analog input voltage exceeds AVDD1 + 0.3 V or AVSS – 0.3 V. Digital input pin START and digital output pins SDO/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$ are diode-clamped to IOVDD and DGND. Digital input pins $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{RESET}}$ and CLK are diode-clamped to DGND. Limit the input current to 10 mA in the event the digital input voltage exceeds IOVDD + 0.3 V (for effected pins) or exceeds DGND – 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD1 to AVSS, high-speed mode	4.5		5.5	V
		AVDD1 to AVSS, low-speed mode	2.85		5.5	
		AVDD1 to DGND	1.65			
		Absolute ratio of AVSS / AVDD1 to DGND			1.2	V/V
		AVDD2 to AVSS	1.74		5.5	V
		AVSS to DGND	–2.75		0	
	Digital power supply	IOVDD to DGND	1.65		5.5	V
ANALOG INPUTS						
V_{AINP}, V_{AINN}	Absolute input voltage	Precharge buffer off	AVSS – 0.05		AVDD1 + 0.05	V
		Precharge buffer on	AVSS + 0.1		AVDD1 – 0.1	
V_{IN}	Differential input voltage $V_{IN} = V_{AINP} – V_{AINN}$	1x input range	$–V_{REF}$		V_{REF}	V
		2x input range	$–2·V_{REF}$		$2·V_{REF}$	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference voltage $V_{REF} = V_{REFP} – V_{REFN}$	Low-reference range	0.5	2.5	2.75	V
		High-reference range	1	4.096	AVDD1 – AVSS	
V_{REFN}	Negative reference voltage		AVSS – 0.05			V
V_{REFP}	Positive reference voltage	REFP precharge buffer off			AVDD1 + 0.05	V
		REFP precharge buffer on			AVDD1 – 0.7	
EXTERNAL CLOCK SOURCE						
f_{CLK}	Clock frequency	High-speed mode	0.5	25.6	26.2	MHz
		Low-speed mode	0.5	3.2	3.28	
DIGITAL INPUTS						
V_{IL}	Logic input voltage, low		DGND		0.3·IOVDD	V
V_{IH}	Logic input voltage, high		0.7·IOVDD		IOVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–45		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		ADS127L11		UNIT
		WQFN (RUK)	TSSOP (PW)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.0	92.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	32.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	44.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	2.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.9	43.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS, HIGH-SPEED MODE							
	Input current, differential input voltage	Precharge buffers off			95		µA/V
		Precharge buffers off, 2x input range			47		
		Precharge buffers on			±3		µA
	Input current drift, differential input voltage	Precharge buffers off			3		nA/V/°C
		Precharge buffers off, 2x input range			1.5		
		Precharge buffers on			5		nA/°C
	Input current, common-mode input voltage	Precharge buffers off			5		µA/V
		Precharge buffers off, 2x input range			2.5		
		Precharge buffers on			±3		µA
ANALOG INPUTS, LOW-SPEED MODE							
	Input current, differential input voltage	Precharge buffers off			12		µA/V
		Precharge buffers off, 2x input range			6		
		Precharge buffers on			±0.4		µA
	Input current drift, differential input voltage	Precharge buffers off			1		nA/V/°C
		Precharge buffers off, 2x input range			0.5		
		Precharge buffers on			0.2		nA/°C
	Input current, common-mode input voltage	Precharge buffers off			0.6		µA/V
		Precharge buffers off, 2x input range			0.3		
		Precharge buffers on			±0.4		µA
DC PERFORMANCE							
	Resolution	OSR ≥ 64			24		Bits
	Noise			See *Noise Performance* for details			
f_{DATA}	Output data rate	High-speed mode, low-latency filter		0.08		1067	kSPS
		High-speed mode, wideband filter		3.125		400	
		Low-speed mode, low-latency filter		0.01		133	
		Low-speed mode, wideband filter		0.390625		50	
INL	Integral nonlinearity	Best-fit method			0.9	5.5	ppm of FSR
			T_A = 25°C to 85°C			4	
	Offset error	T_A = 25°C		–250	±30	250	µV
	Offset drift				50	200	nV/°C
	Gain error	T_A = 25°C		–2000	±200	2000	ppm of FSR
	Gain drift				0.6	1.9	ppm of FSR/°C
NMRR	Normal-mode rejection ratio	f_{IN} = 50 Hz (±1 Hz), f_{DATA} = 50 SPS		100			dB
		f_{IN} = 60 Hz (±1 Hz), f_{DATA} = 60 SPS		100			
CMRR	Common-mode rejection ratio	At dc		110	130		dB
		Up to 10 kHz			115		
		At dc, 2x input range			95		
PSRR	Power-supply rejection ratio	AVDD1, dc		100	120		dB
		AVDD2, dc		115	130		
		IOVDD, dc		115	130		

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6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE, HIGH-SPEED MODE							
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 200 kSPS	Wideband filter	109	111.5		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108.5		
			Low-latency filter	112	114		
			Low-latency filter, V_{REF} = 2.5 V		110.5		
			Low-latency filter, V_{REF} = 2.5 V, 2x input range		111		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 200 kSPS, 9 harmonics	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		107		
			Low-latency filter		112		
			Low-latency filter, V_{REF} = 2.5 V		108.5		
			Low-latency filter, V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 200 kSPS, 9 harmonics	Wideband filter		–120		dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			120		dB
AC PERFORMANCE, LOW-SPEED MODE							
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 25 kSPS	Wideband filter	109	112		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108.5		
			Low-latency filter	111.5	114.5		
			Low-latency filter, V_{REF} = 2.5 V		110.5		
			Low-latency filter, V_{REF} = 2.5 V, 2x input range		111.5		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 25 kSPS	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108		
			Low-latency filter		112		
			Low-latency filter, V_{REF} = 2.5 V		108		
			Low-latency filter, V_{REF} = 2.5 V, 2x input range		110		

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6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 25 kSPS, 9 harmonics	Wideband filter		–125		dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			120		dB
WIDEBAND FILTER CHARACTERISTICS							
	Pass-band frequency	Within envelope of pass-band ripple			0.4 · f_{DATA}		Hz
		–0.1-dB frequency			0.4125 · f_{DATA}		
		–3-dB frequency			0.4374 · f_{DATA}		
	Pass-band ripple			–0.0004		0.0004	dB
	Stop-band frequency	At stop-band attenuation			0.5 · f_{DATA}		Hz
	Stop-band attenuation(1)				106		dB
	Group delay				34 / f_{DATA}		s
	Settling time				68 / f_{DATA}		s
VOLTAGE REFERENCE INPUTS							
	REFP and REFN input current, differential reference voltage	REFP precharge buffer off, high-speed mode			190		µA/V
		REFP precharge buffer off, low-speed mode			80		
	REFP input current, differential reference voltage	REFP precharge buffer on			±2		µA
	REFP and REFN input current drift	REFP precharge buffer off, high-speed mode			10		nA/°C
		REFP precharge buffer off, low-speed mode			10		
	REFP input current drift	REFP precharge buffer on			10		
INTERNAL OSCILLATOR							
	Frequency	High-speed mode		25.4	25.6	25.8	MHz
		Low-speed mode		3.17	3.2	3.23	
VCM OUTPUT VOLTAGE							
	Output voltage				(AVDD1 + AVSS) / 2		V
	Accuracy			–1%	±0.1%	1%	
	Voltage noise	1-kHz bandwidth			25		$µV_{RMS}$
	Start-up time	C_L = 100 nF			1		ms
	Capacitive load					100	nF
	Resistive load			2			kΩ
	Short-circuit current limit				10		mA
DIGITAL INPUTS/OUTPUTS							
V_{OL}	Logic-low output level	OUT_DRV = 0b, I_{OL} = 2 mA				0.2 · IOVDD	V
		OUT_DRV = 1b, I_{OL} = 1 mA				0.2 · IOVDD	
V_{OH}	Logic-high output level	OUT_DRV = 0b, I_{OH} = –2 mA		0.8 · IOVDD			V
		OUT_DRV = 1b, I_{OH} = –1 mA		0.8 · IOVDD			
	Input hysteresis				150		mV
	Input current	Excluding $\overline{\text{RESET}}$ pin		–1		1	µA
	$\overline{\text{RESET}}$ pin pullup resistor				20		kΩ

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6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, f_{CLK} = 25.6 MHz (high-speed mode), f_{CLK} = 3.2 MHz (low-speed mode), input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SUPPLY CURRENT							
I_{AVDD1}, I_{AVSS}	AVDD1 and AVSS current (All buffers off)	High-speed mode			1.7	1.85	mA
		Low-speed mode			0.25	0.3	
		Standby mode			35		µA
		Power-down mode			5		
	AVDD1 and AVSS additional current (per buffer function)	AINx precharge buffer, high-speed mode			1.35	1.9	mA
		AINx precharge buffer, low-speed mode			0.2	0.3	
		REFP precharge buffer, high-speed mode			1.5	1.6	
		REFP precharge buffer, low-speed mode			0.4	0.45	
		VCM buffer			0.1		
I_{AVDD2}, I_{AVSS}	AVDD2 and AVSS current	High-speed mode			3.5	3.8	mA
		Low-speed mode			0.85	0.95	
		Standby mode			60		µA
		Power-down mode			1		
DIGITAL SUPPLY CURRENT							
I_{IOVDD}	IOVDD current	High-speed mode, wideband filter, OSR = 32			2.1	2.7	mA
		High-speed mode, low-latency filter, OSR = 32			0.6	1	
		Low-speed mode, wideband filter, OSR = 32			0.3	0.4	
		Low-speed mode, low-latency filter, OSR = 32			0.1	0.2	
		Standby mode, external clock			10		µA
		Standby mode, internal oscillator			40		
		Power-down mode			10		
POWER DISSIPATION							
P_D	Power dissipation	AVDD2 = 1.8 V, precharge buffers off	High-speed mode, wideband filter		18.6		mW
			High-speed mode, low-latency filter		15.9		
			Low-speed mode, wideband filter		3.3		
			Low-speed mode, low-latency filter		3.0		

(1) Stop-band attenuation as provided by the digital filter. Input frequencies in the stop band intermodulate with the chop frequency beginning at f_{MOD} / 32, which results in stop-band attenuation exceeding 106 dB. See the wideband filter stop-band attenuation figure for details.

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6.6 Timing Requirements (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, high-speed mode	38.2	2000	ns
	CLK period, low-speed mode, CLK_DIV = 1b	38.2	2000	
	CLK period, low-speed mode, CLK_DIV = 0b	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low	17		ns
	Pulse duration, CLK low, low-speed mode, CLK_DIV = 0b	128		
$t_{w(CLKH)}$	Pulse duration, CLK high	17		ns
	Pulse duration, CLK high, low-speed mode, CLK_DIV = 0b	128		
SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	25	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	10		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	10		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, communication start after $\overline{RESET}$ rising edge or after SPI RESET pattern	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START high before CLK rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START high after CLK rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) START rising edge should not be applied between the setup and hold time period at the rising edge of CLK

6.7 Switching Characteristics (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven state				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				20	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				23	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ return high	Synchronized and start/stop control modes			5	t_{CLK}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b			50	ns

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6.8 Timing Requirements (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, high-speed mode	38.2	2000	ns
	CLK period, low-speed mode, CLK_DIV = 1b	38.2	2000	
	CLK period, low-speed mode, CLK_DIV = 0b	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low	17		ns
	Pulse duration, CLK low, low-speed mode	128		
$t_{w(CLKH)}$	Pulse duration, CLK high	17		ns
	Pulse duration, CLK high, low-speed mode	128		
SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	20	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	8		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	8		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t
$t_{d(RSSC)}$	Delay time, communication start after $\overline{RESET}$ rising edge or after SPI RESET pattern	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START high before CLKIN rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START high after CLKIN rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) START rising edge should not be applied between the setup and hold time period at the rising edge of CLK

6.9 Switching Characteristics (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven				17	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				17	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				19	ns
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ return high	Synchronized and start/stop control modes			5	t_{CLK}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	SDO_DRDY = 1b			50	ns

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6.10 Timing Diagrams

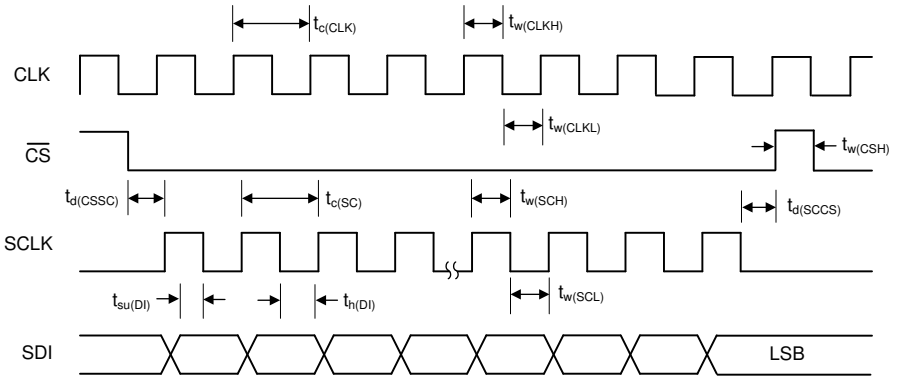

図 6-1. Clock and Serial Interface Timing Requirements

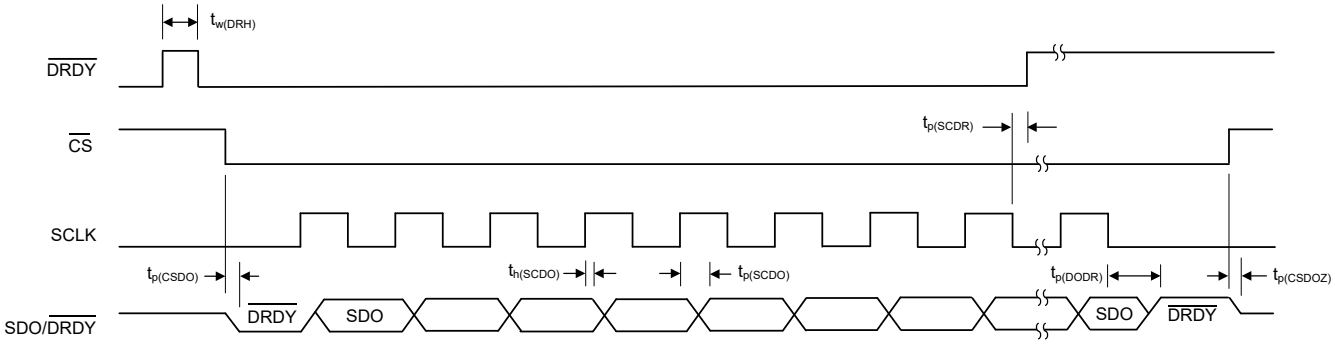

図 6-2. Serial Interface Switching Characteristics

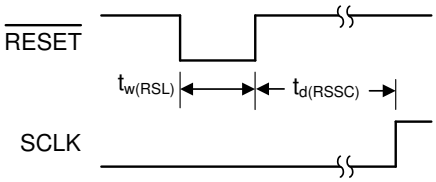

図 6-3. $\overline{RESET}$ Pin Timing

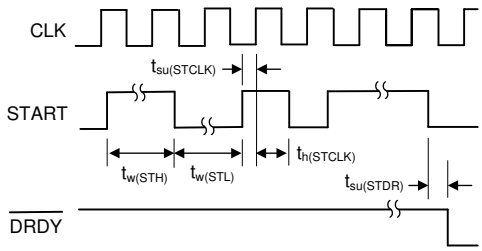

図 6-4. START Pin Timing

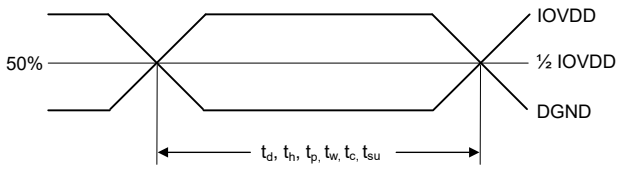

図 6-5. Timing Reference

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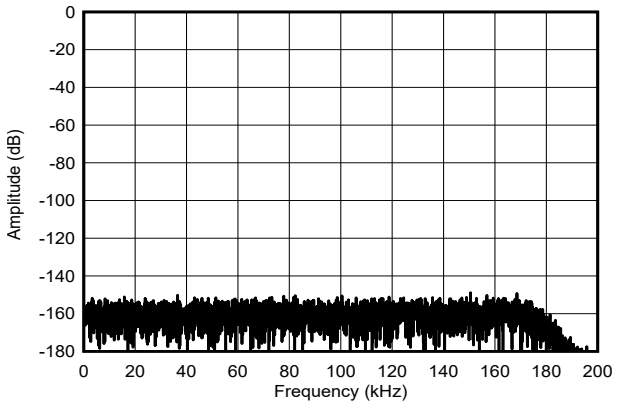
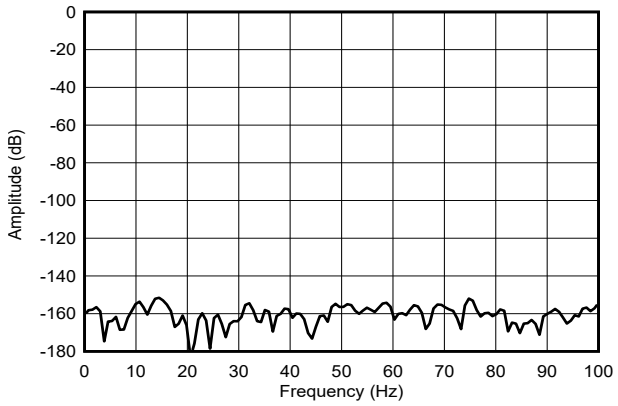
6.11 Typical Characteristics

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



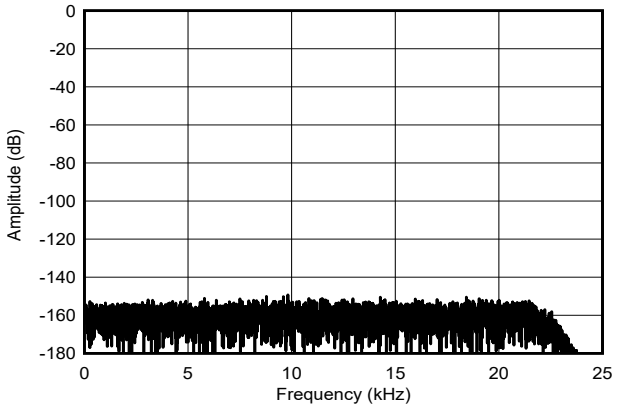
Wideband filter, OSR = 32, high-speed mode, 524,288 samples

図 6-6. Shorted Input FFT



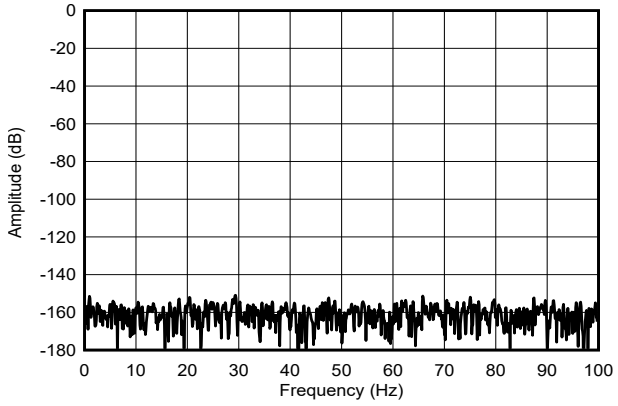
Wideband filter, OSR = 32, high-speed mode, 524,288 samples

図 6-7. Shorted Input FFT



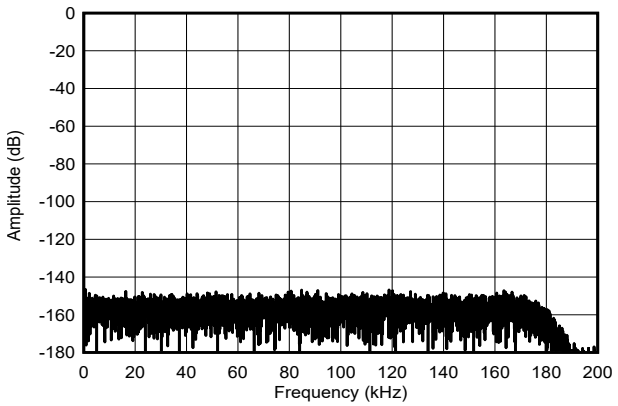
Wideband filter, OSR = 32, low-speed mode, 524,288 samples

図 6-8. Shorted Input FFT



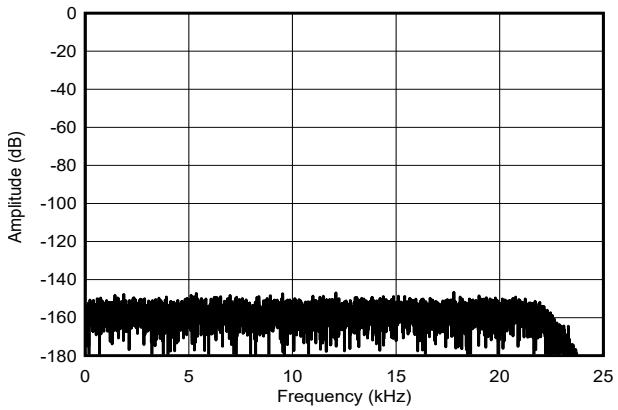
Wideband filter, OSR = 32, low-speed mode, 524,288 samples

図 6-9. Shorted Input FFT



2x input range, V_{REF} = 2.5 V, wideband filter, OSR = 32, high-speed mode, 524,288 samples

図 6-10. Shorted Input FFT



2x input range, V_{REF} = 2.5 V, wideband filter, OSR = 32, low-speed mode, 524,288 samples

図 6-11. Shorted Input FFT

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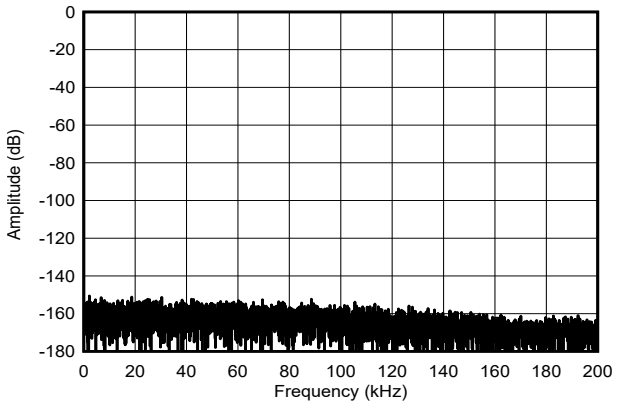
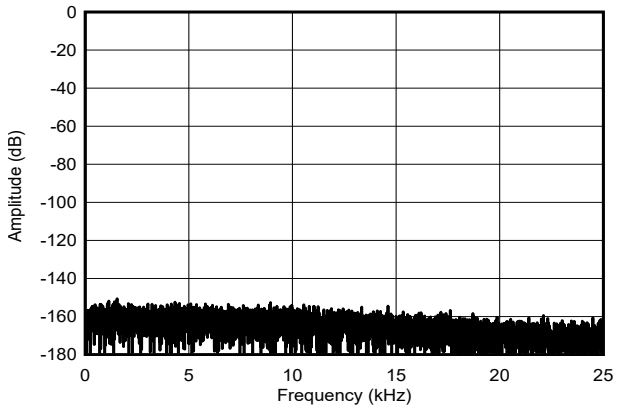
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



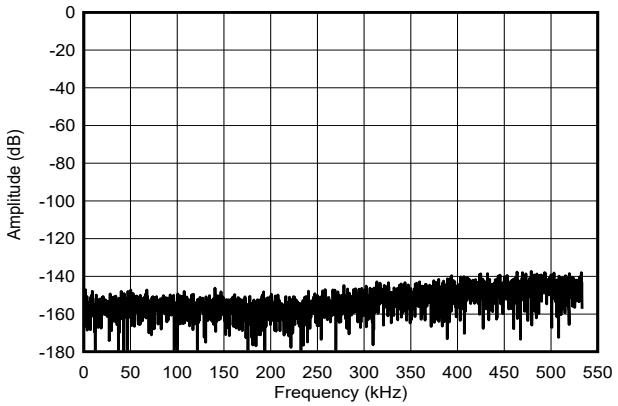
Sinc4 filter, OSR = 32, high-speed mode, 524,288 samples

図 6-12. Shorted Input FFT



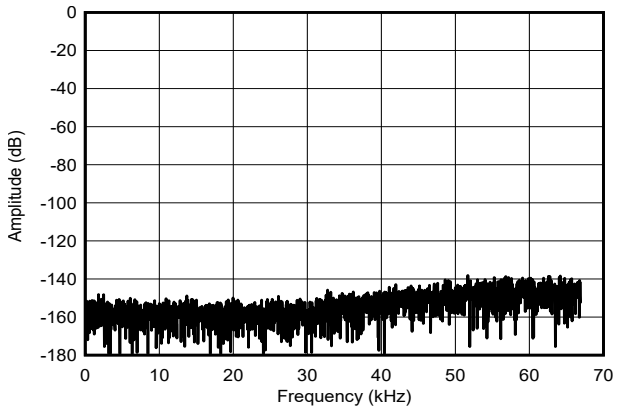
Sinc4 filter, OSR = 32, low-speed mode, 524,288 samples

図 6-13. Shorted Input FFT



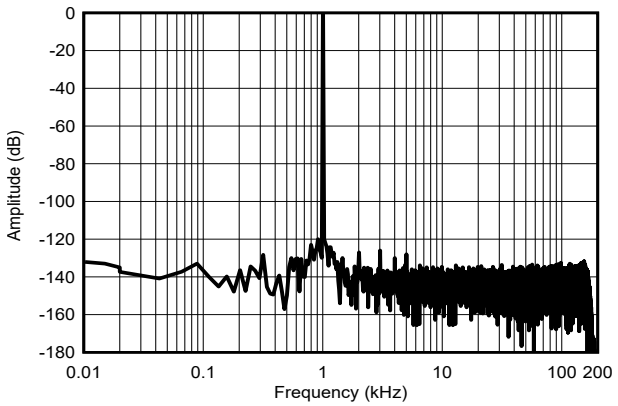
Sinc4 filter, OSR = 12, high-speed mode, 524,288 samples

図 6-14. Shorted Input FFT



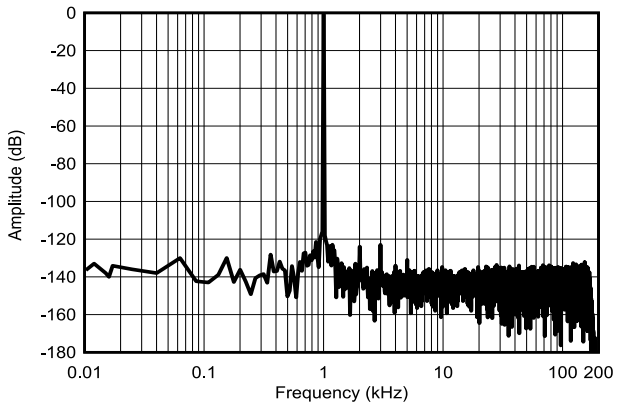
Sinc4 filter, OSR = 12, low-speed mode, 524,288 samples

図 6-15. Shorted Input FFT



Input precharge buffers on, wideband filter, OSR = 32, high-speed mode, V_{IN} = –0.2 dBFS, 65,536 samples

図 6-16. Full-Scale Input FFT



Input precharge buffers off, wideband filter, OSR = 32, high-speed mode, V_{IN} = –0.2 dBFS, 65,536 samples

図 6-17. Full-Scale Input FFT

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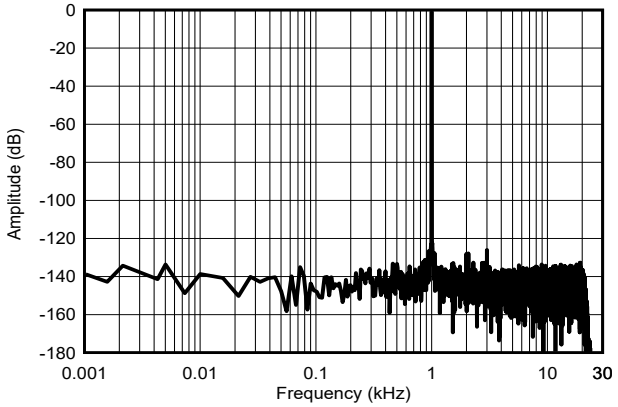
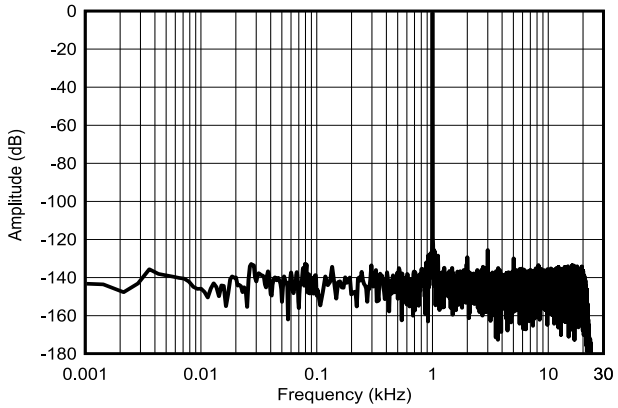
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



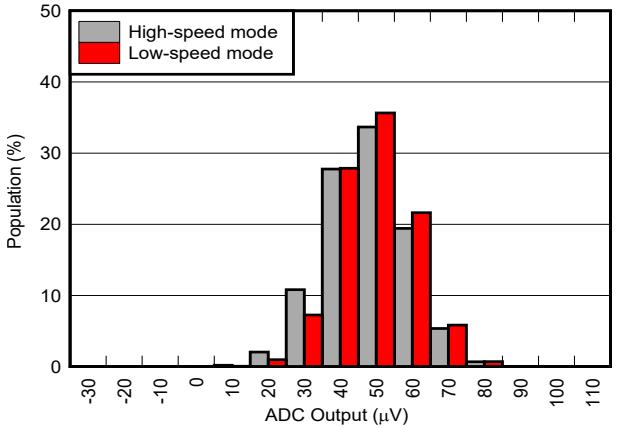
Input precharge buffers on, wideband filter, OSR = 32, low-speed mode, V_{IN} = –0.2 dBFS, 65,536 samples

図 6-18. Full-Scale Input FFT



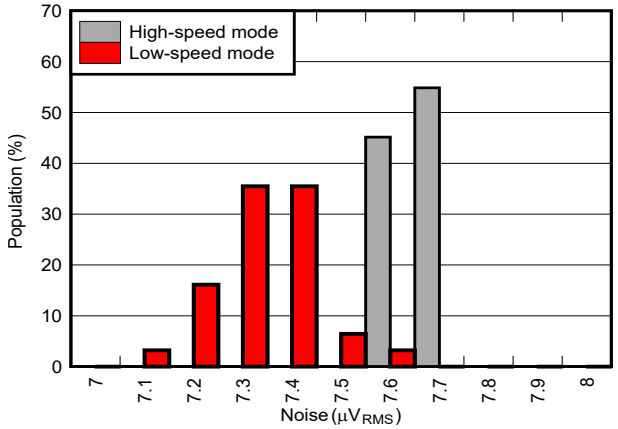
Input precharge buffers off, wideband filter, OSR = 32, low-speed mode, V_{IN} = –0.2 dBFS, 65,536 samples

図 6-19. Full-Scale Input FFT



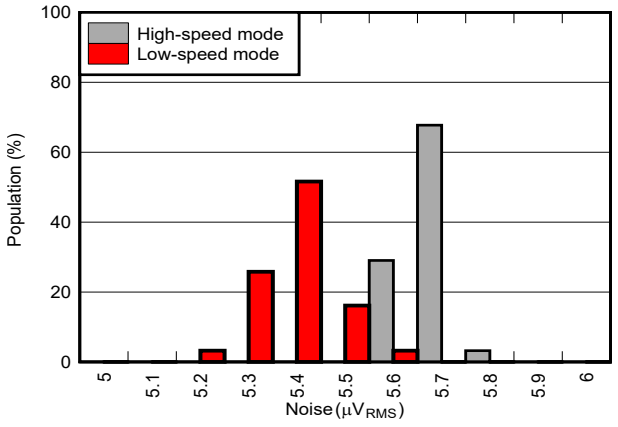
Shorted input, wideband filter, OSR = 32

図 6-20. Output Data Distributions



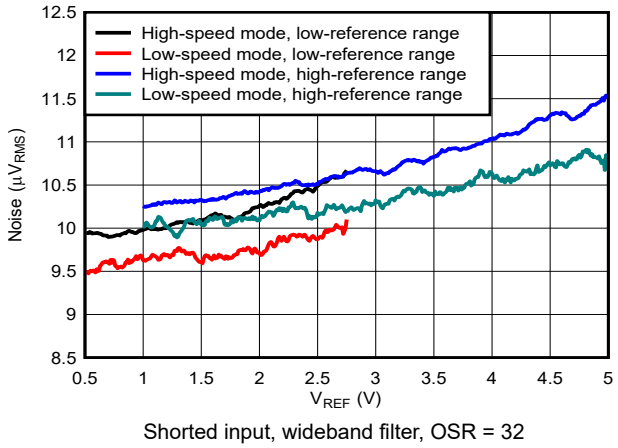
Shorted input, wideband filter, OSR = 64, N = 30

図 6-21. Total Noise Performance Distributions



Shorted input, sinc4 filter, OSR = 64, N = 30

図 6-22. Total Noise Performance Distributions



Shorted input, wideband filter, OSR = 32

図 6-23. Total Noise Performance vs Reference Voltage

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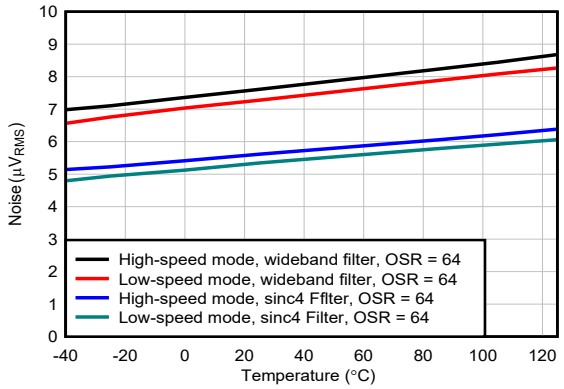
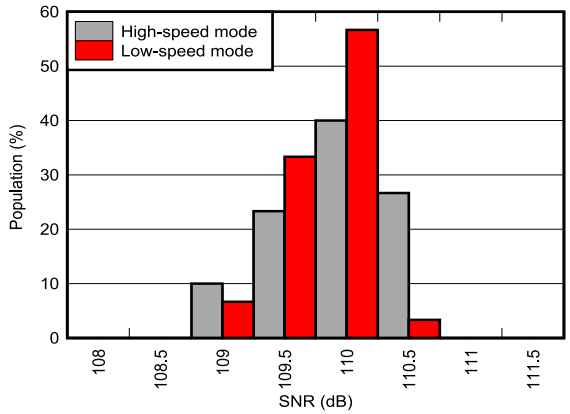
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



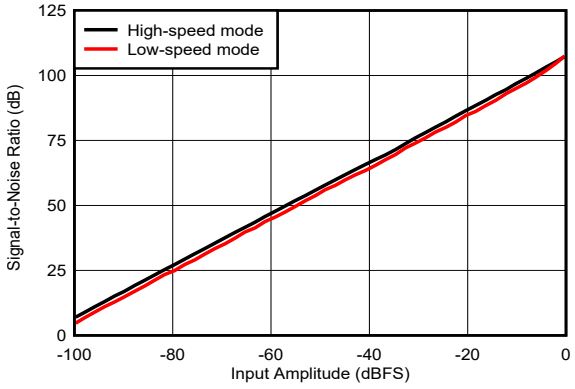
Shorted input

図 6-24. Total Noise Performance vs Temperature



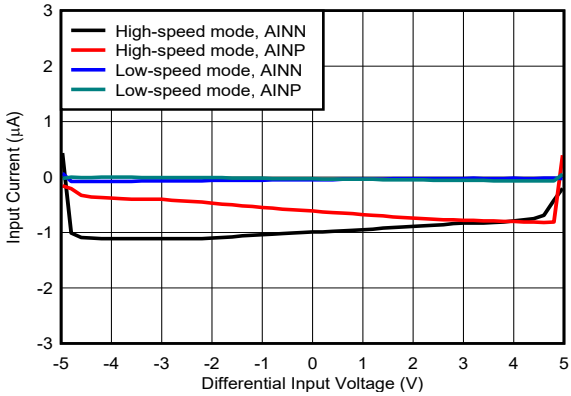
Wideband filter, OSR = 64, N = 30

図 6-25. SNR Distributions



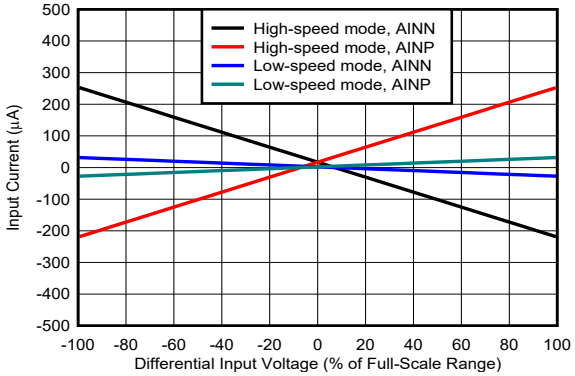
Wideband filter, OSR = 64

図 6-26. SNR vs Signal Amplitude



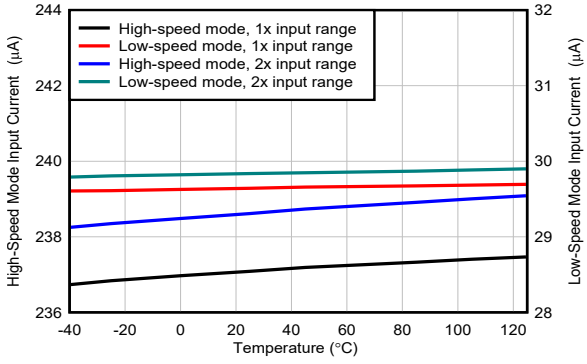
Precharge buffers on, 2x input range,
V_{REF} = 2.5 V, V_{CM} = 2.5 V

図 6-27. Input Current vs Differential Input Voltage



Precharge buffers off, 1x and 2x input range,
V_{REF} = 2.5 V, V_{CM} = 2.5 V

図 6-28. Input Current vs Differential Input Voltage



V_{IN} = full scale, V_{CM} = 2.5 V, precharge buffers off

図 6-29. Input Current vs Temperature

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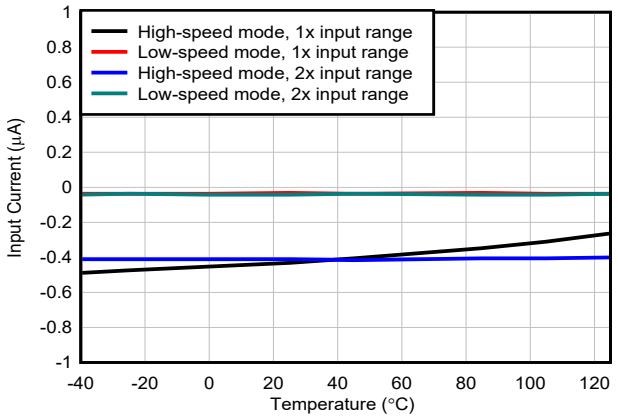
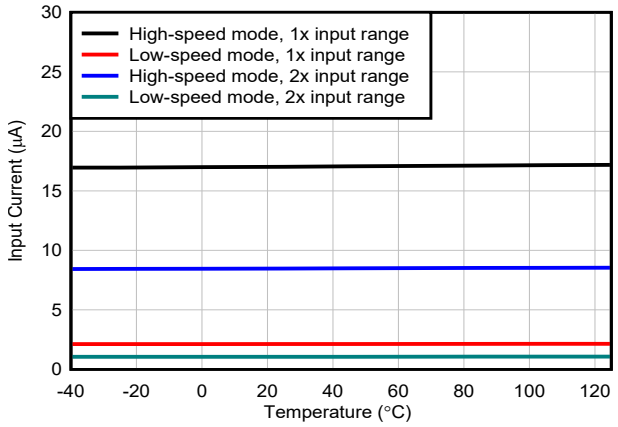
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



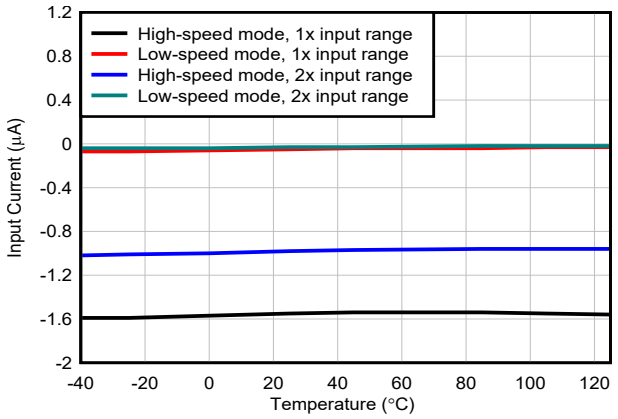
V_{IN} = full scale, V_{CM} = 2.5 V, precharge buffers on

図 6-30. Input Current vs Temperature



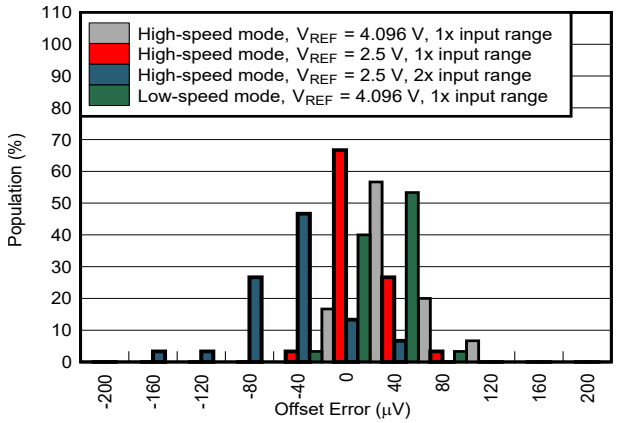
V_{IN} = 0 V, V_{CM} = 2.5 V, precharge buffers off

図 6-31. Input Current vs Temperature



V_{IN} = 0 V, V_{CM} = 2.5 V, precharge buffers on

図 6-32. Analog Input Current vs Temperature



N = 30

図 6-33. Offset Error Distribution

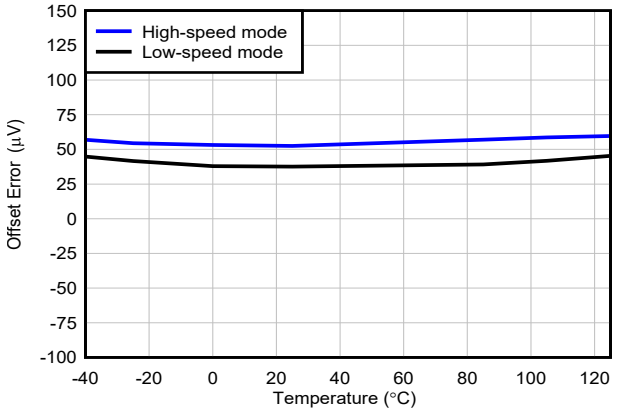
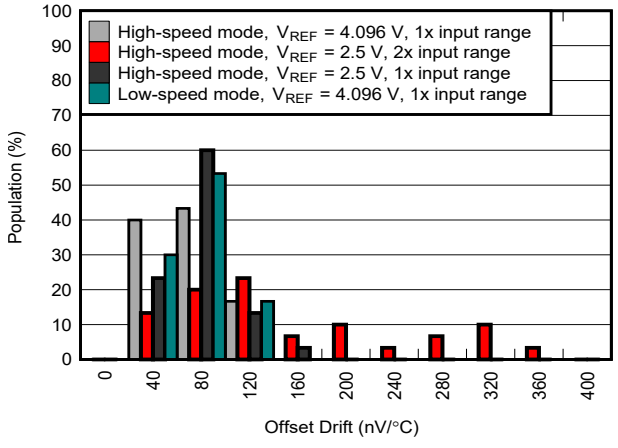


図 6-34. Offset Error vs Temperature



N = 30

図 6-35. Offset Drift Distribution

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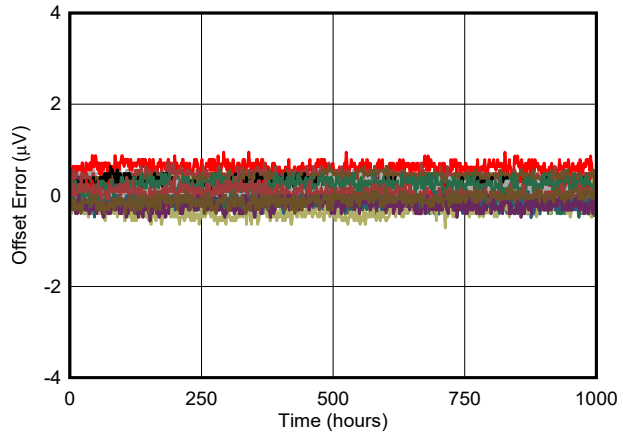
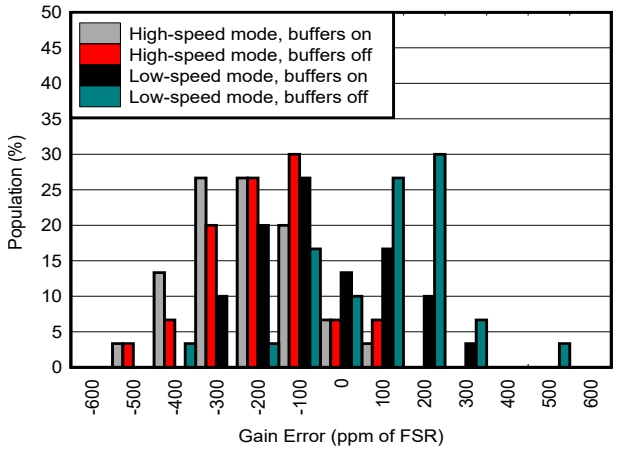
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



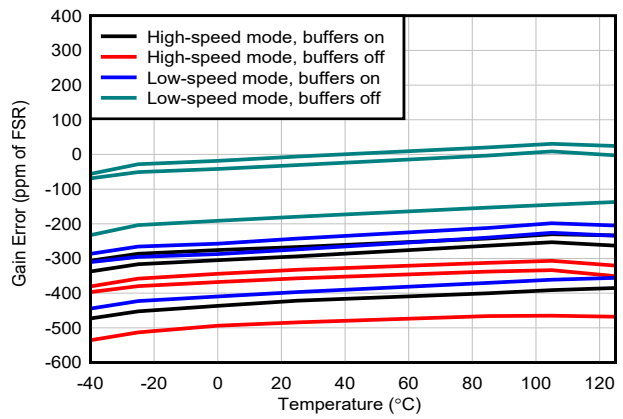
N = 30, offset error calibrated at t = 0

図 6-36. Long-Term Offset Drift



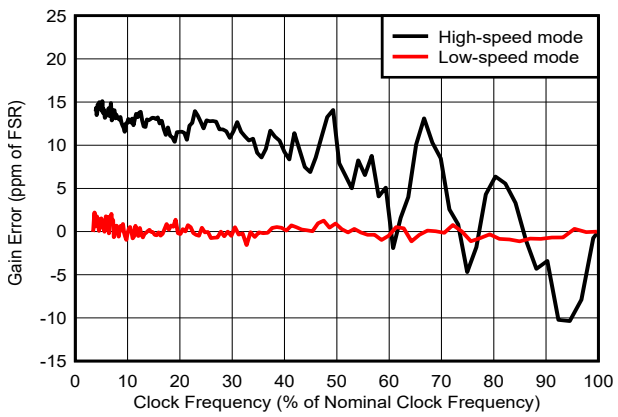
N = 30

図 6-37. Gain Error Distribution



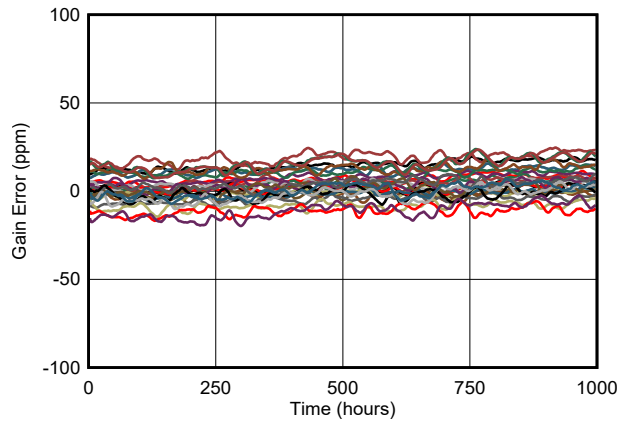
N = 3

図 6-38. Gain Error vs Temperature



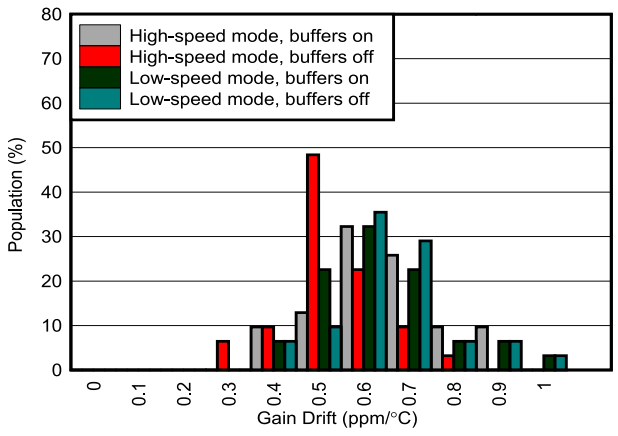
Gain error calibrated at nominal clock frequency

図 6-39. Gain Error vs Clock Frequency



N = 30, gain error calibrated at t = 0

図 6-40. Long-Term Gain Drift



N = 30

図 6-41. Gain Drift Distributions

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6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

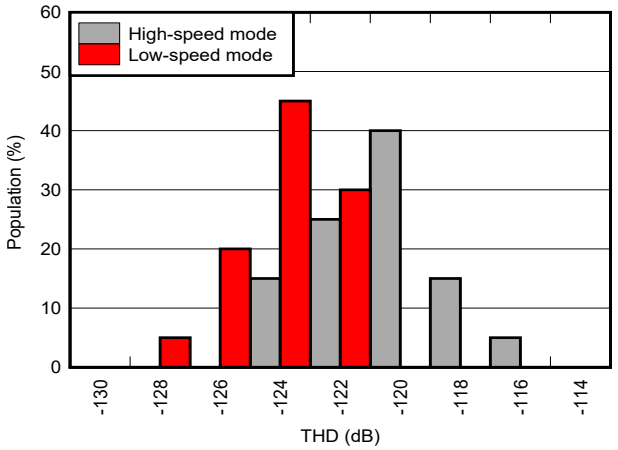

図 6-42. THD Distribution

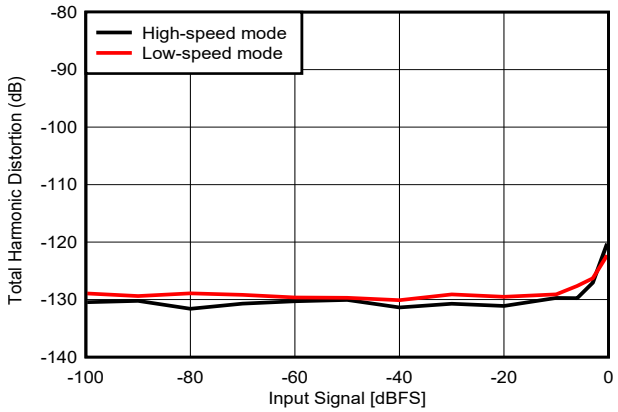

図 6-43. THD vs Input Signal Amplitude

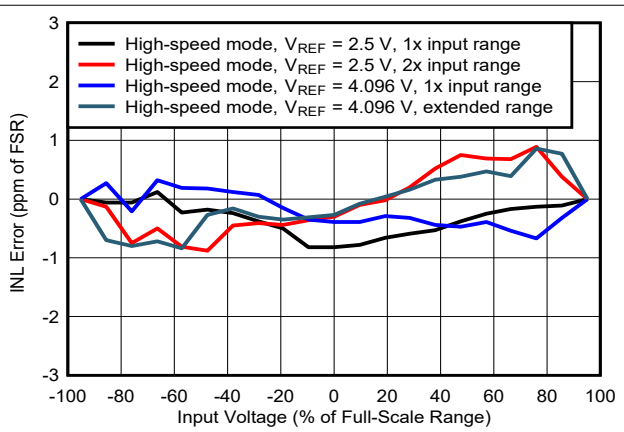

図 6-44. INL Error vs Input Voltage

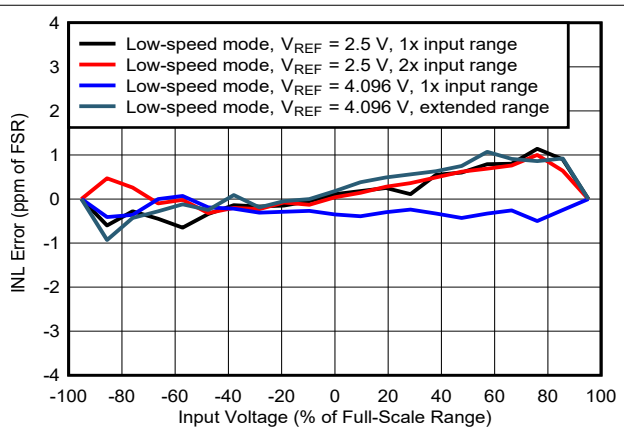

図 6-45. INL Error vs Input Voltage

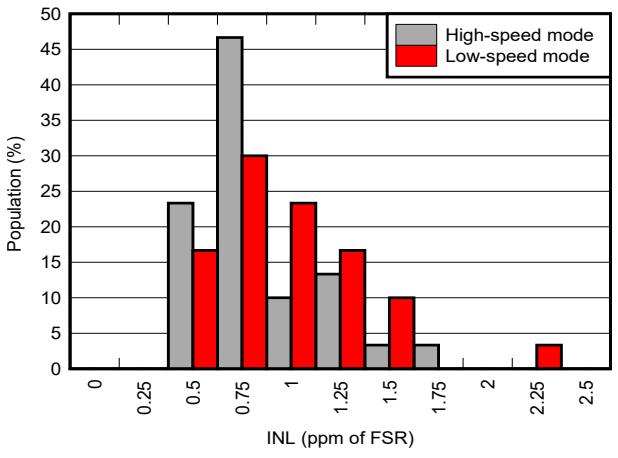

図 6-46. INL Distributions

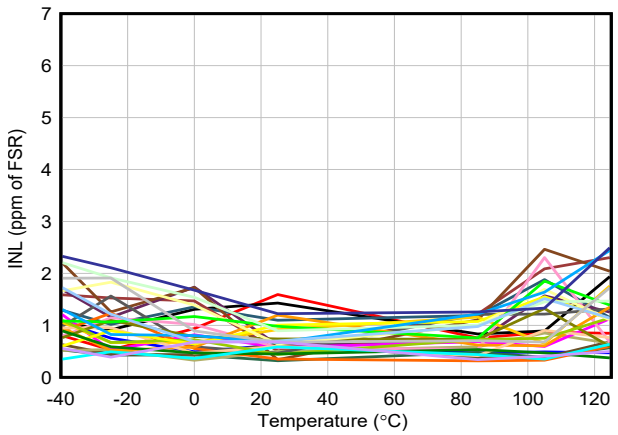

図 6-47. INL vs Temperature

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6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

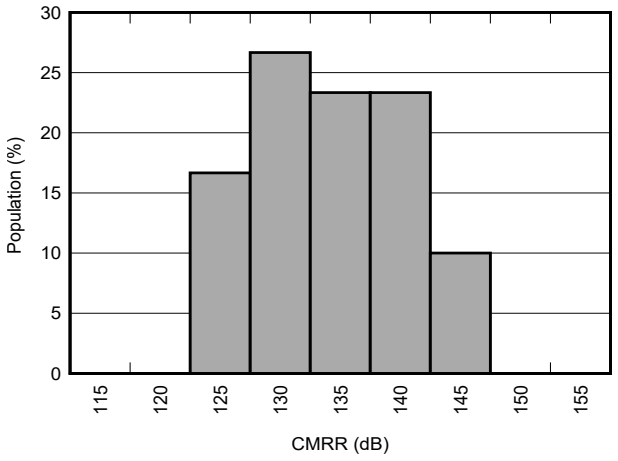

図 6-48. DC CMRR Distribution

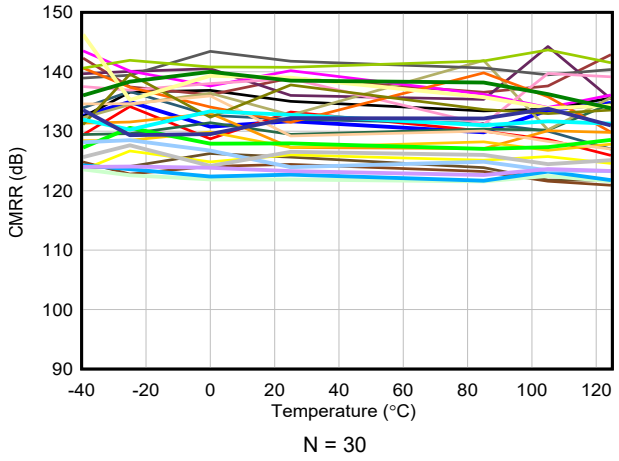

図 6-49. DC CMRR vs Temperature

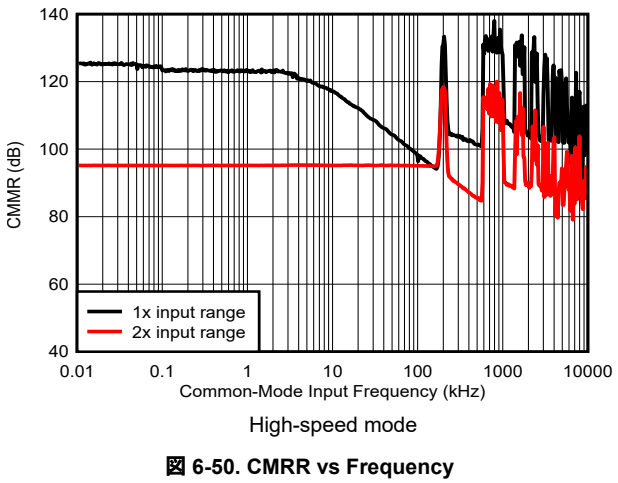

図 6-50. CMRR vs Frequency

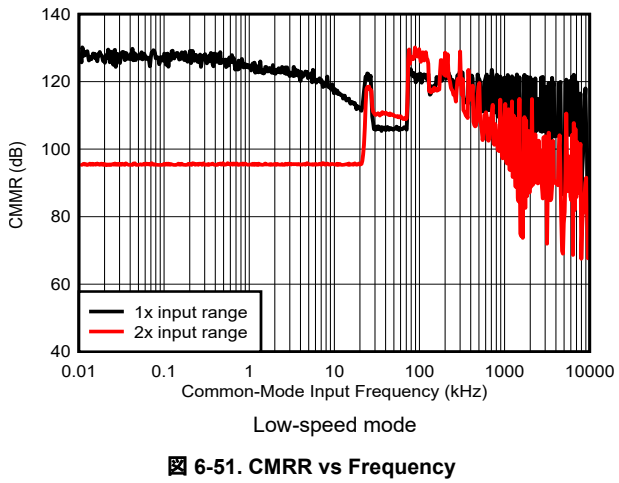

図 6-51. CMRR vs Frequency

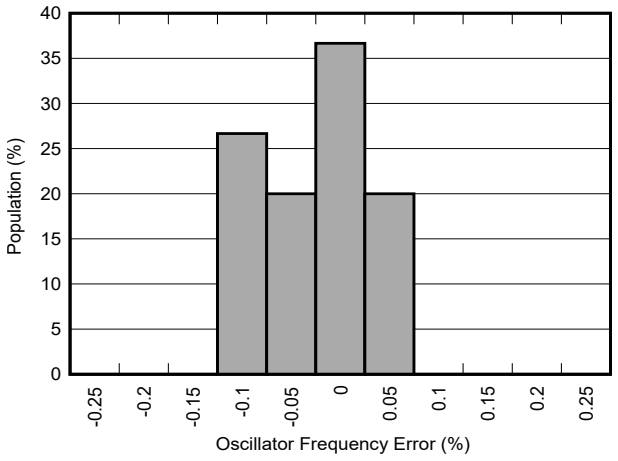

図 6-52. Oscillator Frequency Distribution

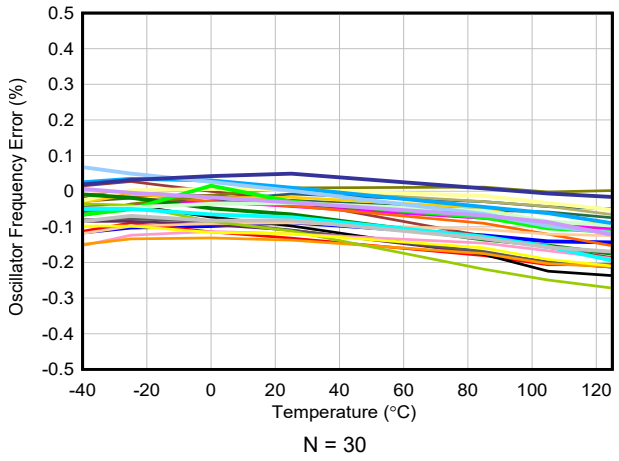

図 6-53. Oscillator Frequency vs Temperature

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6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

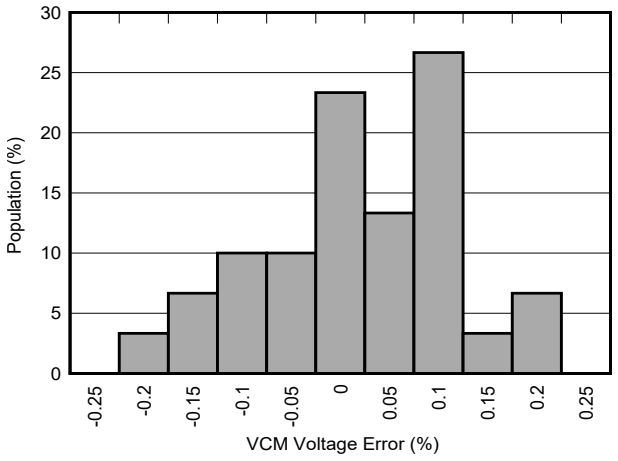

図 6-54. VCM Voltage Distribution

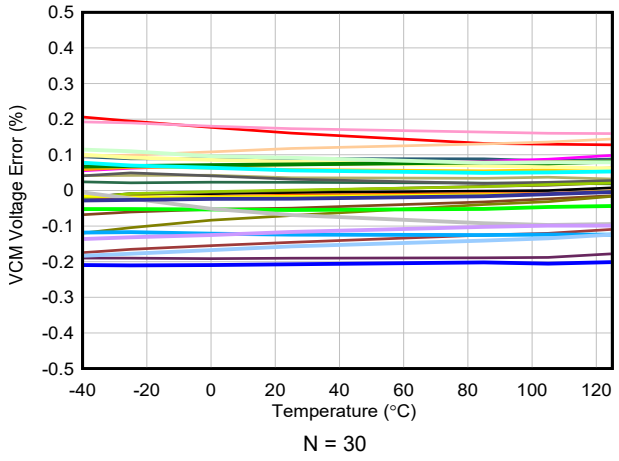

図 6-55. VCM Voltage vs Temperature

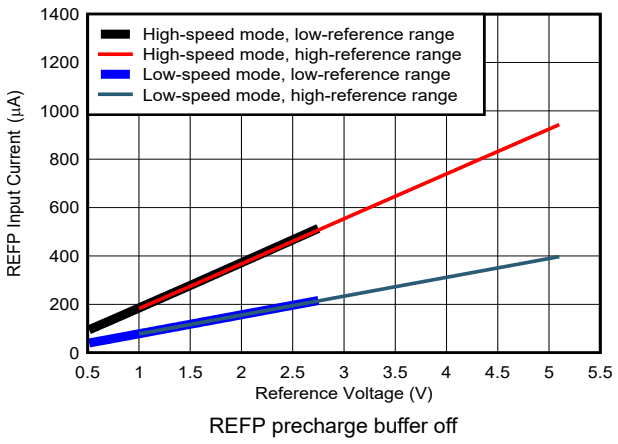

図 6-56. Reference Input Current vs Reference Voltage

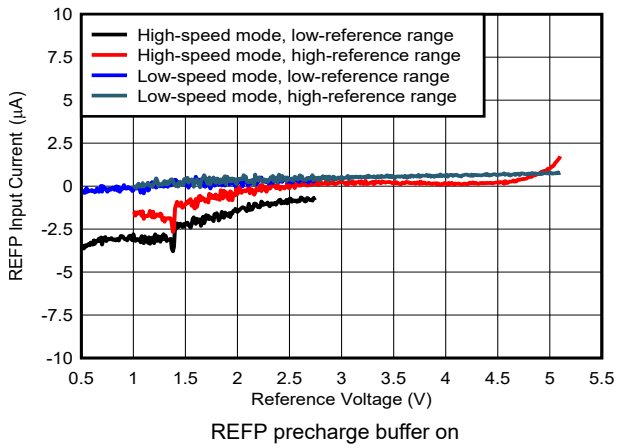

図 6-57. REFP Input Current vs Reference Voltage

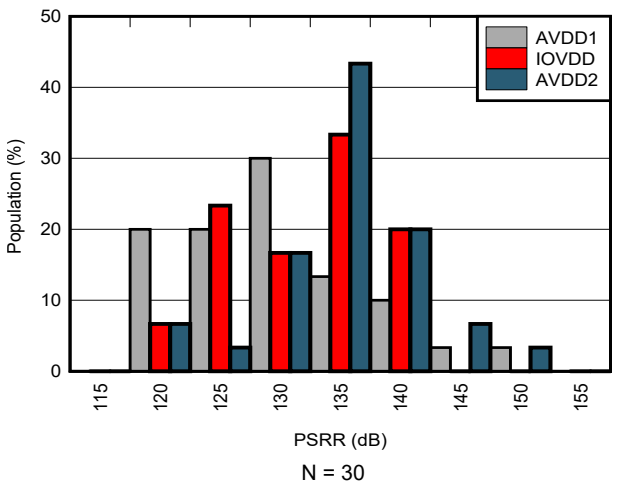

図 6-58. DC PSRR Distribution

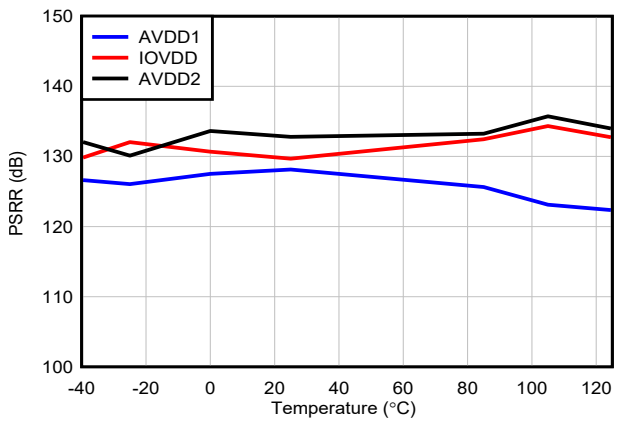

図 6-59. DC PSRR vs Temperature

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6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

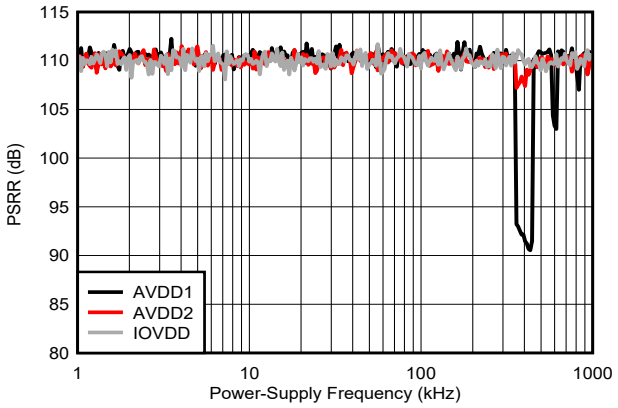

図 6-60. PSRR vs Power-Supply Frequency

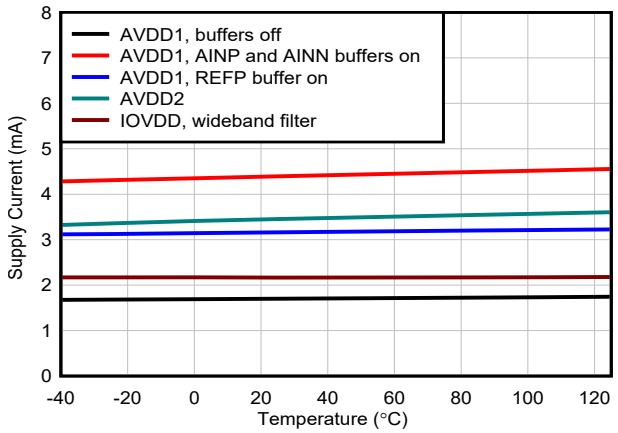

図 6-61. Power-Supply Current vs Temperature

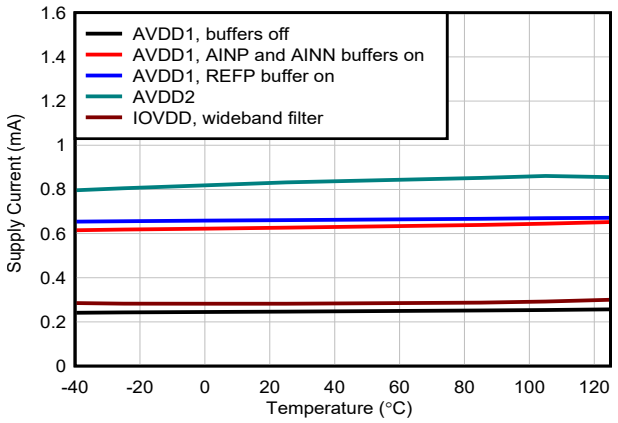

図 6-62. Power-Supply Current vs Temperature

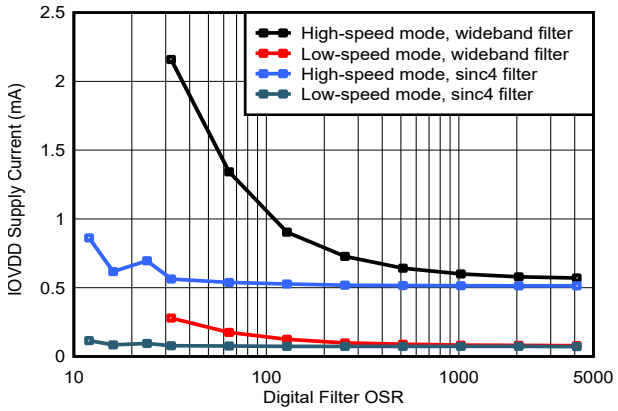

図 6-63. Power-Supply Current vs Oversampling Ratio

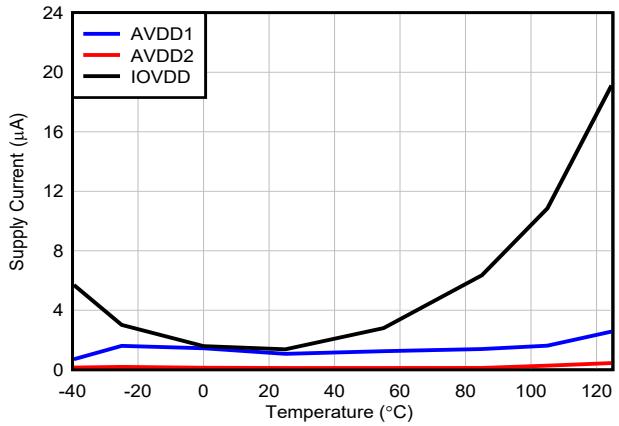

図 6-64. Power-Down Mode Supply Current vs Temperature

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7 Parameter Measurement Information

7.1 Offset Error Measurement

Offset error is measured with the ADC inputs externally shorted together. The input common-mode voltage is fixed to the mid-point of the AVDD1 and AVSS power-supply range. Offset error is specified at T_A = 25°C.

7.2 Offset Drift Measurement

Offset drift is defined as the change in offset voltage measured at multiple points over the specified temperature range. Offset drift is calculated using the *box method* in which a box is formed over the maximum and minimum offset voltages and over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test.

式 1 shows the offset drift calculation using the box method:

$$\text{Offset Drift (nV/°C)} = 10^9 \cdot (V_{OFSMAX} - V_{OFSMIN}) / (T_{MAX} - T_{MIN}) \quad (1)$$

where:

- V_{OFSMAX} and V_{OFSMIN} = Maximum and minimum offset voltages over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

7.3 Gain Error Measurement

Gain error is defined as the difference between the actual and the ideal slopes of the ADC transfer function. Gain error is measured by applying dc test voltages at –95% and 95% of FSR. The error is calculated by subtracting the difference of the dc test voltages (ideal slope) from the difference in the ADC output voltages (actual slope). The difference in the slopes is divided by the ideal slope and multiplied by 10^6 to convert the error to ppm of FSR. Error resulting from the ADC reference voltage is excluded from the gain error measurement. The gain error is specified at T_A = 25°C. 式 2 shows the calculation of gain error:

$$\text{Gain Error (ppm of FSR)} = 10^6 \cdot (\Delta V_{OUT} - \Delta V_{IN}) / \Delta V_{IN} \quad (2)$$

where:

- ΔV_{OUT} = Difference of two ADC output voltages
- ΔV_{IN} = Difference of two input test voltages

7.4 Gain Drift Measurement

Gain drift is defined as the change of gain error measured at multiple points over the specified temperature range. The box method is used in which a box is formed over the maximum and minimum gain errors over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. 式 3 describes gain drift using the box method.

$$\text{Gain Drift (ppm/°C)} = (GE_{MAX} - GE_{MIN}) / (T_{MAX} - T_{MIN}) \quad (3)$$

where:

- GE_{MAX} and GE_{MIN} = Maximum and minimum gain errors over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

7.5 NMRR Measurement

Normal-mode rejection ratio (NMRR) specifies the ability of the ADC to reject normal-mode input signals at specific frequencies, usually expressed at 50-Hz and 60-Hz input frequencies. Normal-mode rejection is uniquely determined by the frequency response of the digital filter. In this case, the nulls in the frequency response of the low-latency sinc3 filter option located at 50 Hz and 60 Hz provide rejection at these frequencies.

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7.6 CMRR Measurement

Common-mode rejection ratio (CMRR) specifies the ability of the ADC to reject common-mode input signals. CMRR is expressed as dc and ac parameters. For measurement of CMRR (dc), three common-mode test voltages equal to AVSS + 50 mV, (AVDD1 + AVSS) / 2, and AVDD1 – 50 mV are applied with the inputs externally shorted together. The maximum change of the ADC offset voltage is recorded versus the change in common-mode test voltage. 式 4 shows how CMRR (dc) is computed.

$$\text{CMRR (dc) (dB)} = 20 \cdot \log(\Delta V_{CM} / \Delta V_{OS}) \quad (4)$$

where:

- ΔV_{CM} = Change of dc common-mode test voltage
- ΔV_{OS} = Change of corresponding offset voltage

For the measurement of CMRR (ac), an ac common-mode signal is applied at various test frequencies at 95% full-scale range. An FFT is computed from the ADC data with the common-mode signal applied. As shown in 式 5, the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers and related to the amplitude of the common-mode test signal.

$$\text{PSRR (ac) (dB)} = 20 \cdot \log(V_{CM} / V_O) \quad (5)$$

where:

- V_{CM} (RMS) = Common-mode input signal amplitude
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

7.7 PSRR Measurement

Power-supply rejection ratio (PSRR) specifies the ability of the ADC to reject power-supply interference. PSRR is expressed as ac and dc parameters. For measurement of PSRR (dc), the power-supply voltage is changed over the range of minimum, nominal, and maximum specified voltages with the inputs externally shorted together. The maximum change of ADC offset voltage is recorded versus the change in power-supply voltage. PSRR (dc) is computed as shown in 式 6 as the ratio of change of the power-supply voltage step to the change of offset voltage.

$$\text{PSRR (dc) (dB)} = 20 \cdot \log(\Delta V_{PS} / \Delta V_{OS}) \quad (6)$$

where:

- ΔV_{PS} = Change of power-supply voltage
- ΔV_{OS} = Change of offset voltage

For the measurement of PSRR (ac), the power-supply voltage is modulated by a 100-mVpp (35 mV_{RMS}) signal at various test frequencies. An FFT of the ADC data with power-supply modulation is performed. As shown in 式 7, the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers and related to the amplitude of the power-supply modulation signal.

$$\text{PSRR (ac) (dB)} = 20 \cdot \log(V_{PS} / V_O) \quad (7)$$

where:

- V_{PS} (RMS) = 100 mV ac power-supply modulation signal
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

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7.8 SNR Measurement

Signal-to-noise ratio (SNR) is a measure of noise performance with a full-scale ac input signal. For the SNR measurement, a –0.2-dBFS, 1-kHz test signal is used with V_{CM} equal to the mid-supply voltage. As shown in 式 8, SNR is the ratio of the rms value of the input signal to the root-sum-square of all other frequency components derived from the FFT result of the ADC output samples. DC and harmonics of the original signal are excluded from the SNR calculation. In a test case where an FFT window function is used because of non-coherent sampling, the spectral leakage of adjacent frequency bins surrounding dc, the original signal and signal harmonics are removed to calculate SNR.

$$\text{SNR (dB)} = 20 \cdot \log(V_{IN} / e_n) \tag{8}$$

where:

- V_{IN} = Input test signal
- e_n = Root-sum-square of frequency components excluding dc and signal harmonics

7.9 INL Error Measurement

Integral nonlinearity (INL) error specifies the linearity of the ADC dc transfer function. INL is measured by applying a series of dc test voltages along a straight line computed from the slope and offset transfer function of the ADC. INL is the difference between a set of dc test voltages [$V_{IN(N)}$] to the corresponding set of output voltages [$V_{OUT(N)}$]. 式 9 shows the *end-point method* of calculating INL error.

$$\text{INL (ppm of FSR)} = \text{maximum absolute value of INL test series } [10^6 \cdot (V_{IN(N)} – V_{OUT(N)}) / \text{FSR}] \tag{9}$$

where:

- N = Index of dc test voltage
- [$V_{IN(N)}$] = Set of test voltages over the range –95% to 95% of FSR
- [$V_{OUT(N)}$] = Set of corresponding ADC output voltages
- FSR (full-scale range) = $2 \cdot V_{REF}$ (1x input range) or $4 \cdot V_{REF}$ (2x input range)

The INL *best-fit method* uses a least-squared error (LSE) calculation to determine a new straight line to minimize the root-sum-square of the INL errors above and below the original end-point line.

7.10 THD Measurement

Total harmonic distortion (THD) specifies the dynamic linearity of the ADC with an ac input signal. For the THD measurement, a –0.2-dBFS, 1-kHz differential input signal with V_{CM} equal to the mid-supply voltage is applied. A sufficient number of data points are collected to yield an FFT result with frequency bin widths of 5 Hz or less. The 5-Hz bin width reduces the noise in the harmonic bins for consistent THD measurements. As shown in 式 10, THD is calculated as the ratio of the root-sum-square amplitude of harmonics to the input signal amplitude.

$$\text{THD (dB)} = 20 \cdot \log(V_H / V_{IN}) \tag{10}$$

where:

- V_H = Root-sum-square of harmonics: $\sqrt{(V_2{}^2 + V_3{}^2 + \ldots V_n{}^2)}$, where V_n = Ninth harmonic voltage
- V_{IN} = Input signal fundamental

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7.11 SFDR Measurement

Spurious-free dynamic range (SFDR) is the ratio of the rms value of a single-tone ac input to the highest spurious signal in the ADC frequency spectrum. SFDR measurement includes harmonics of the original signal. For the SFDR measurement, a –0.2-dBFS, 1-kHz input signal with V_{CM} equal to the mid-supply voltage is applied. As shown in 式 11, SFDR is the ratio of the rms values of the input signal to the single highest spurious signal, including harmonics of the original signal.

$$\text{SFDR (dB)} = 20 \cdot \log(V_{IN} / V_{SPUR}) \quad (11)$$

where:

- V_{IN} = Input test signal
- V_{SPUR} = Single highest spurious level

7.12 Noise Performance

The ADC provides two operational speed modes (high speed and low speed) that allow trade-offs between ADC resolution, power consumption, and signal bandwidth. Low-speed mode operates the modulator at 1/8th speed for decreased device power consumption and, as a result, the output data rates are reduced by 1/8th. The programmable oversampling ratio (OSR) determines the output data rate and associated signal bandwidth, and therefore also determines the total noise performance. Increasing the OSR lowers the signal bandwidth and total noise by averaging more samples from the modulator to yield one conversion result.

The wideband filter provides data rates up to 400 kSPS in high-speed mode and 50 kSPS in low-speed mode. The low-latency sinc4 filter provides data rates up to 1.067 MSPS in high-speed mode and up to 133 kSPS in low-speed mode. The low-latency filter provides the options of sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1 configurations.

表 7-1 through 表 7-5 summarize the noise performance and signal bandwidth of the various filter modes. Noise performance is shown with 1x input range and a 4.096-V reference voltage. In comparison, decreasing the reference voltage to 2.5 V decreases dynamic range by 4 dB (typical). Operation in 2x input range and a 2.5-V reference voltage decreases dynamic range by 3 dB (typical) compared to 1x input range and 4.096-V reference voltage operation.

The noise data are the result of the standard deviation (rms) of the conversion data with inputs shorted and biased to the mid-supply voltage and are representative of typical performance at T_A = 25°C. A minimum of 1,000 or 10 seconds of consecutive conversions (whichever occurs first) are used to measure RMS noise (e_n). Because of the statistical nature of noise, repeated noise measurements can yield higher or lower noise results.

式 12 converts RMS noise to dynamic range (dB) and 式 13 converts RMS noise to effective resolution (bits).

$$\text{Dynamic Range (dB)} = 20 \cdot \log[\text{FSR} / (2 \cdot \sqrt{2} \cdot e_n)] \quad (12)$$

$$\text{Effective Resolution (bits)} = \log_2(\text{FSR} / e_n) \quad (13)$$

where:

- FSR = 2 · V_{REF} (1x input range)
- FSR = 4 · V_{REF} (2x input range)
- e_n = Noise voltage (RMS)

When evaluating ADC noise performance, consider the effect of external buffer and amplifier noise to the total noise performance. The noise performance of the ADC can be evaluated in isolation by selecting the input short test connection of the input multiplexer.

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表 7-1. Wideband Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
32	400	165.000	10.6	108.7	19.5
64	200	82.500	7.47	111.8	20.1
128	100	41.250	5.20	114.9	20.6
256	50	20.625	3.66	118.0	21.1
512	25	10.312	2.58	121.0	21.6
1024	12.5	5.156	1.83	124.0	22.1
2048	6.25	2.578	1.29	127.0	22.6
4096	3.125	1.289	0.92	130.0	23.1
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
32	50	20.625	10.6	108.7	19.5
64	25	10.312	7.47	111.8	20.1
128	12.5	5.156	5.20	114.9	20.6
256	6.25	2.578	3.66	118.0	21.1
512	3.125	1.289	2.58	121.0	21.6
1024	1.5625	0.645	1.83	124.0	22.1
2048	0.78125	0.322	1.29	127.0	22.6
4096	0.390625	0.161	0.92	130.0	23.1

表 7-2. Sinc4 Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
12	1066.666	242.666	76.3	91.6	16.7
16	800	182.000	27.3	100.5	18.2
24	533.333	121.333	10.4	108.9	19.6
32	400	91.000	7.96	111.2	20.0
64	200	45.500	5.57	114.3	20.5
128	100	22.750	3.90	117.4	21.0
256	50	11.375	2.80	120.3	21.5
512	25	5.687	1.98	123.3	22.0
1024	12.5	2.844	1.40	126.3	22.5
2048	6.25	1.422	0.99	129.3	23.0
4096	3.125	0.711	0.70	132.3	23.5
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
12	133.333	30.333	76.3	91.6	16.7
16	100	22.750	27.3	100.5	18.2
24	66.666	15.166	10.4	108.9	19.6
32	50	11.375	7.96	111.2	20.0
64	25	5.687	5.57	114.3	20.5
128	12.5	2.844	3.90	117.4	21.0
256	6.25	1.422	2.80	120.3	21.5
512	3.125	0.711	1.98	123.3	22.0
1024	1.5625	0.355	1.40	126.3	22.5
2048	0.78125	0.177	0.99	129.3	23.0
4096	0.390625	0.089	0.70	132.3	23.5

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表 7-3. Sinc4 + Sinc1 Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

SINC4 OSR	SINC1 OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	NOISE (e_n) (μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32	2	200	68.35	5.63	114.2	20.5
32	4	100	40.97	3.98	117.2	21.0
32	10	40	17.47	2.81	120.3	21.5
32	20	20	8.814	1.99	123.3	22.0
32	40	10	4.420	1.41	126.3	22.5
32	100	4	1.770	0.99	129.3	23.0
32	200	2	0.885	0.70	132.3	23.5
32	400	1	0.442	0.52	134.9	23.9
32	1000	0.4	0.177	0.39	137.4	24.3
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32	2	25	8.544	5.63	114.2	20.5
32	4	12.5	5.121	3.98	117.2	21.0
32	10	5	2.184	2.81	120.3	21.5
32	20	2.5	1.102	1.99	123.3	22.0
32	40	1.25	0.552	1.41	126.3	22.5
32	100	0.5	0.221	0.99	129.3	23.0
32	200	0.25	0.111	0.70	132.3	23.5
32	400	0.125	0.055	0.52	134.9	23.9
32	1000	0.05	0.022	0.39	137.4	24.3

表 7-4. Sinc3 Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	NOISE (e_n) (μV_{RMS}) (1)	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
26667	480	126	0.29	140.0	24.7
32000	400	105	0.27	140.6	24.8
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
26667	60	16	0.29	140.0	24.7
32000	50	13	0.27	140.6	24.8

(1) The noise measurement may vary resulting from the effects of 24-bit quantization levels: 4.096 V / 2^{23} = 0.488 µV / code.

表 7-5. Sinc3 + Sinc1 Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

SINC3 OSR	SINC1 OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	NOISE (e_n) (μV_{RMS}) (1)	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32000	3	133.3	54	0.19	143.7	25.3
32000	5	80	34	0.15	145.7	25.7
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32000	3	16.6	6.7	0.19	143.7	25.3
32000	5	10	4.3	0.15	145.7	25.7

(1) The noise measurement may vary resulting from the effects of 24-bit quantization levels: 4.096 V / 2^{23} = 0.488 µV / code.

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8 Detailed Description

8.1 Overview

The ADS127L11 is a high performance, 24-bit delta-sigma (ΔΣ) analog-to-digital converter (ADC) offering an excellent combination of dc accuracy and ac precision. The device is optimized to provide high resolution with low power consumption. Integrated input and reference precharge buffers simplify the driver requirements. The digital filter consists of two programmable modes: low-latency mode (typically used for measurement of dc signals) and wideband mode (typically used for measurement of ac signals).

The delta-sigma modulator produces low-resolution, high-frequency data proportional to the signal magnitude. Noise shaping within the modulator shifts the quantization noise of the low-resolution data to an out-of-band frequency range where the noise is removed by the digital filter. The noise remaining within the pass band is white, which is reduced by the digital filter. The digital filter simultaneously decimates and filters the modulator data to provide the high-resolution final output data.

The *Functional Block Diagram* shows the features of the ADS127L11. The modulator is a third-order, multibit delta-sigma design that measures the differential input signal, $V_{IN} = (V_{AINP} - V_{AINN})$, against the differential reference, $V_{REF} = (V_{REFP} - V_{REFN})$. Input and positive reference precharge buffers reduce the bandwidth and driving requirements of the external input driver. The VCM output provides a buffered mid-supply voltage to drive the common-mode voltage of an external driver stage.

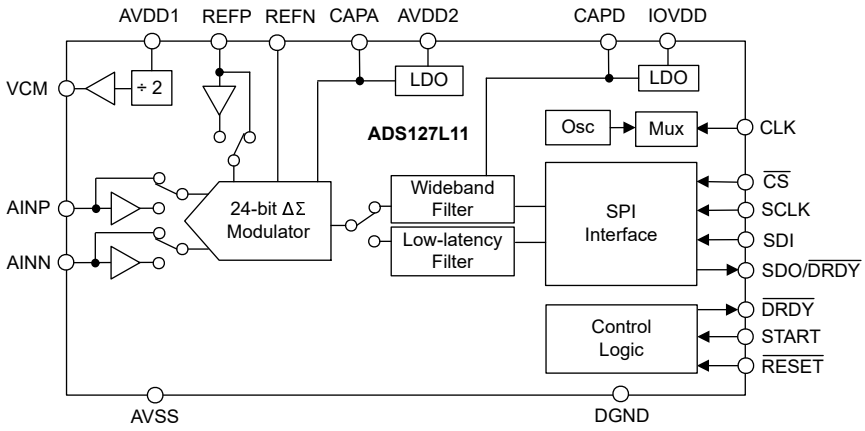
The digital filter offers two modes of operation: the low-latency filter and the wideband filter. The low-latency filter is programmable to sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1 modes, allowing optimization between noise performance and latency. The sinc3 + sinc1 filter provides rejection at 400 Hz, 60 Hz, 50 Hz, and 16.6 Hz. The wideband filter is a multi-tap finite impulse response (FIR) design providing outstanding frequency response with low pass-band ripple, steep transition-band, and high stop-band attenuation. Programmable oversampling ratio (OSR) and two speed modes allow optimized choices of bandwidth, resolution, and device power consumption.

The SPI-compatible serial interface is used to configure the device and read conversion data. The interface features daisy-chaining capability for convenient connection of multichannel, simultaneous-sampled systems. Integrated cyclic redundancy check (CRC) error monitoring improves system-level reliability. $\overline{\text{DRDY}}$ is the conversion data-ready output signal.

The device supports external clock operation for ac or dc applications, and internal oscillator operation for dc applications. The START pin synchronizes the digital filter process. The $\overline{\text{RESET}}$ pin resets the ADC.

Supply voltage AVDD1 powers the precharge buffers and the input sampling switches. AVDD2 powers the modulator via an internal regulator (CAPA). Supply voltage IOVDD is the digital I/O voltage that also powers the digital core via an internal regulator (CAPD). The internal regulators minimize overall power consumption and provide consistent levels of performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input (AINP, AINN)

The analog input of the ADC is differential, with the input defined as a difference voltage: $V_{IN} = V_{AINP} – V_{AINN}$. For best performance, drive the input with a differential signal with the common-mode voltage centered to mid-supply (AVDD1 + AVSS) / 2.

The ADC can accept either unipolar or bipolar input signals by configuring AVDD1 and AVSS accordingly. 図 8-1 shows an example of a differential signal with the supplies configured to unipolar operation. Symmetric input voltage headroom is available when the common-mode voltage is at mid-supply (AVDD1 / 2). Use AVDD1 = 5 V and AVSS = 0 V for unipolar operation (AVDD1 can be reduced to 3 V in low-speed mode). The VCM output provides a buffered common-mode voltage to level-shift the output voltage in the external driver stage. 図 8-2 shows an example of a differential signal configured for bipolar operation. The common-mode voltage of the signal is normally at 0 V. Use AVDD1 and AVSS = ±2.5 V for bipolar operation (AVDD and AVSS can be reduced to ±1.5 V in low-speed mode).

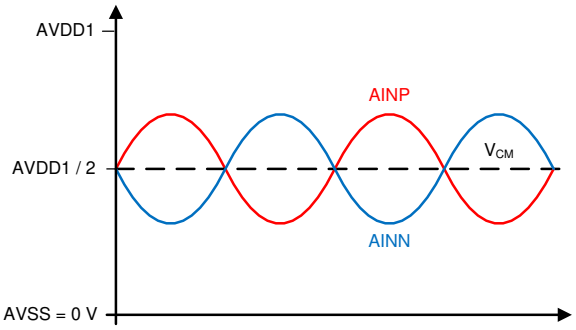


図 8-1. Unipolar Differential Input Signal

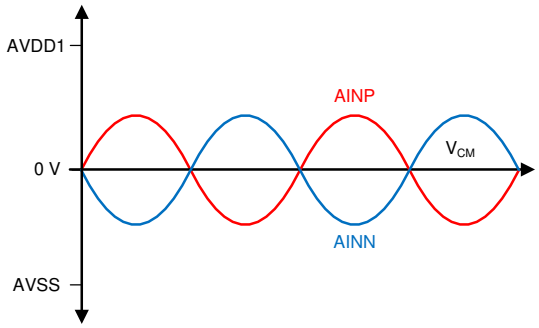


図 8-2. Bipolar Differential Input Signal

In both bipolar and unipolar power-supply configurations, the ADC can accept single-ended input signals by tying the AINN input to AVSS or ground, or to mid-supply. However, because AINN is now a fixed voltage, the voltage range of the ADC is limited by the input swing range of AINP (±2.5 V or 0 V to 5 V for a 5-V supply).

The simplified circuit of 図 8-3 represents the analog input structure.

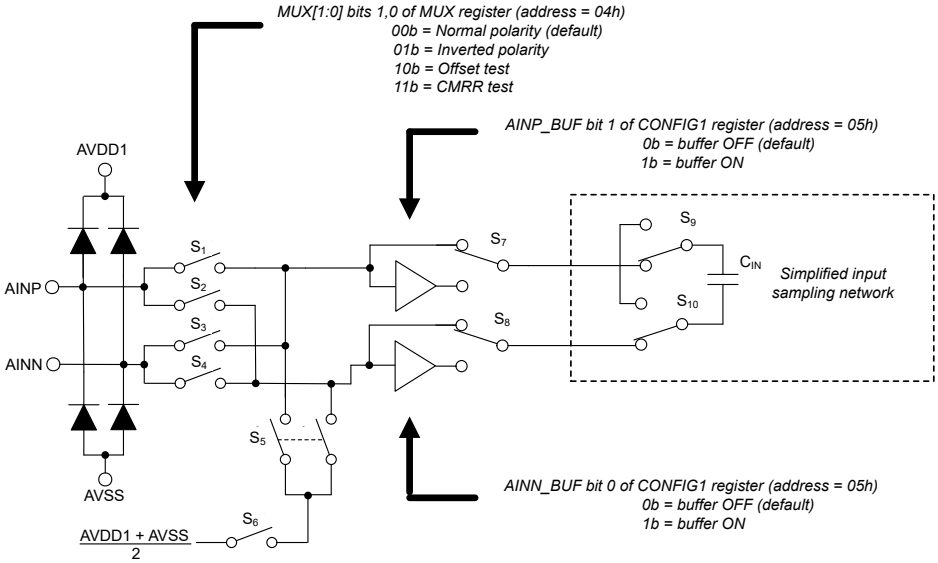


図 8-3. Analog Input Circuit

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Diodes protect the ADC inputs from electrostatic discharge (ESD) events that occur during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. If the inputs are driven below AVSS – 0.3 V, or above AVDD1 + 0.3 V, the protection diodes may conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

The input multiplexer offers the option of normal or reverse input signal polarities. The multiplexer also provides two internal test modes to help verify ADC performance. The offset test mode is used to verify noise and offset error by providing a short to the ADC inputs. The resulting noise and offset voltage data are evaluated by the user. CMRR performance is tested using the CMRR test mode by applying a CMRR test signal to the AINP input. The resulting CMRR test data are also evaluated by the user. 表 8-1 shows the switch configurations of the input multiplexer circuit of 図 8-3.

表 8-1. Input Multiplexer Configurations

MUX[1:0] BITS	SWITCHES	DESCRIPTION
00b	S_1, S_4	Normal polarity input
01b	S_2, S_3	Reverse polarity input
10b	S_5, S_6	Internal noise and offset error test
11b	S_1, S_5	CMRR test using a signal applied to AINP

The device has optional input precharge buffers to reduce the charge required by capacitor C_{IN} during the input sampling phase. When the capacitor is near full charge, the precharge buffers are bypassed (S_7 and S_8 of 図 8-3 in up positions). The external signal driver then provides the fine charge to the capacitor. At the completion of the sample phase, the sampling capacitor is discharged by the modulator to complete the cycle, at which time the sample process repeats. The buffers reduce the transient input current required to charge C_{IN}, therefore reducing the settling time requirement of the signal. Incomplete settling of the input signal can lead to degraded ADC performance. The input buffers are enabled by the AINP_BUF and AINN_BUF bits of the CONFIG1 register. In many cases, if AINN is tied to ground or to a low-impedance fixed potential, the AINN buffer can be disabled to reduce power consumption.

With the input precharge buffers disabled, the charge required by the input sampling capacitor can be modeled as an average input current flowing into the ADC inputs. As shown in 式 14 and 式 15, the input current is comprised of differential and absolute components.

$$\text{Input Current (Differential Input Voltage)} = f_{MOD} \cdot C_{IN} \cdot 10^6 \text{ (µA/V)} \quad (14)$$

where:

- $f_{MOD} = f_{CLK} / 2$ = 12.8 MHz (high-speed mode), 1.6 MHz (low-speed mode)
- C_{IN} = 7.4 pF (1x input range), 3.6 pF (2x input range)

$$\text{Input Current (Absolute Input Voltage)} = f_{MOD} \cdot C_{CM} \cdot 10^6 \text{ (µA/V)} \quad (15)$$

where:

- $f_{MOD} = f_{CLK} / 2$ = 12.8 MHz (high-speed mode), 1.6 MHz (low-speed mode)
- C_{CM} = 0.35 pF (1x input range), 0.17 pF (2x input range)

For f_{MOD} = 12.8 MHz, C_{IN} = 7.4 pF, and C_{CM} = 0.35 pF, the input current resulting from differential voltage is 95 µA/V and the input current resulting from the absolute voltage is 4.5 µA/V. For example, if AINP = 4.5 V and AINN = 0.5 V, then V_{IN} = 4 V. The total AINP input current = (4 V · 95 µA/V) + (4.5 V · 4.5 µA/V) = 400 µA, and the total AINN current is (–4 V · 95 µA/V) + (0.5 V · 4.5 µA/V) = –378 µA.

The charge demand of the input sampling capacitor requires the signal to settle within a half cycle at the modulator frequency $t = 1 / (2 \cdot f_{MOD})$. To satisfy this requirement, the driver bandwidth is typically required to be much larger than the original signal frequency. The bandwidth of the driver can be determined to be sufficient when the THD and SNR data sheet performance are achieved. In the low-speed mode of operation, the modulator sampling is eight times slower, therefore more time is available for driver settling.

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8.3.1.1 Input Range

The ADC has two programmable input ranges: 1x and 2x, where the 1x range is defined by $V_{IN} = \pm V_{REF}$ and the 2x range is defined by $V_{IN} = \pm 2 \cdot V_{REF}$. The 2x input range doubles the available range when using a reference voltage = 2.5 V or less. The 2x input range typically improves SNR by +1 dB, but this requires driving the inputs to the 5-V supply rails to achieve full SNR when using a 2.5-V reference voltage. The best available SNR performance (4 dB improvement typical) is by using a 4.096-V or 5-V reference voltage (be sure to program the ADC to the high-reference range mode). The 2x range operation is internally forced to the 1x range mode when the high-reference range is selected. See the CONFIG1 register to program the input range. 表 8-2 summarizes the ADC input range options.

表 8-2. ADC Input Range

INP_RNG BIT(1)	INPUT RANGE (V)
0	$\pm V_{REF}$
1	$\pm 2 \cdot V_{REF}$

(1) The input range is forced to 1x when the high-reference range is selected.

In some cases, the full available input range is limited by the power supply voltage. For example, the input range exceeds the power supply voltage when using a 3-V power supply with a 2.5-V reference voltage in the 2x range mode.

The ADC also provides the option of extending the input range beyond standard full-scale range. In this mode, the input range is extended by 25% to provide signal headroom before clipping of the signal occurs. Output data are scaled such that the positive and negative full-scale output codes (7FFFFFh and 800000h) are at $\pm 1.25 \cdot k \cdot V_{REF}$, where k is the 1x or 2x input range option.

The SNR performance degrades when the signal exceeds 110% standard full-scale range because of modulator saturation. The modulator MOD_FLAG bit of the STATUS register indicates when modulator saturation occurs. 図 8-4 shows SNR performance when operating in the extended range. See the CONFIG2 register to program the extended range mode.

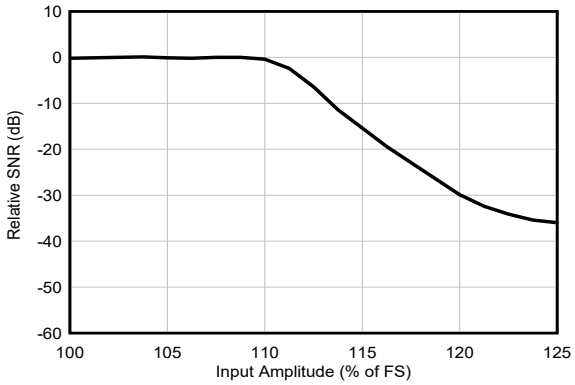

図 8-4. Extended Range SNR Performance

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8.3.2 Reference Voltage (REFP, REFN)

A reference voltage is required for operation. The reference voltage input is differential, defined as: $V_{REF} = V_{REFP} – V_{REFN}$, and applied to the REFP and REFN inputs. See the *Reference Voltage Range* section for details of the reference voltage operating range.

As shown in 図 8-5, the reference inputs have an input structure similar to the analog inputs. ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 0.3 V, or above AVDD1 by 0.3 V. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

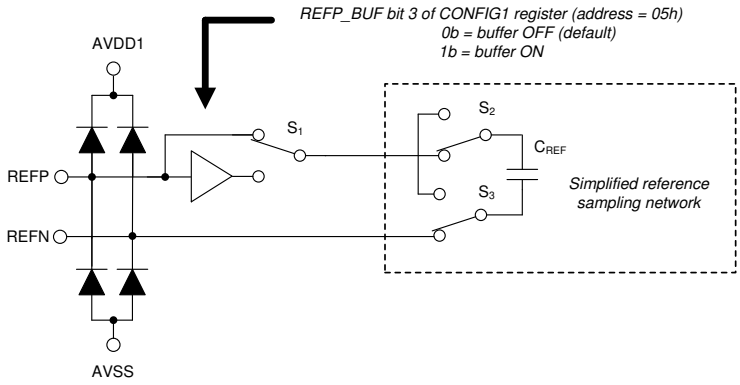

図 8-5. Reference Input Circuit

The reference voltage is sampled by a sampling capacitor C_{REF}. In unbuffered mode, current flows through the reference inputs to charge the sampling capacitor. The current consists of a dc component and an ac component that varies with the frequency of the modulator sampling clock. See the *Electrical Characteristics* table for the reference input current specification.

The effect of charging the reference sampling capacitor requires the external reference driver to settle at the end of the sample phase $t = 1 / (2 \cdot f_{MOD})$. Incomplete settling of the reference voltage can lead to excessive gain error and gain error drift. Operation in low-speed mode reduces the modulator sampling clock frequency by 1/8th, therefore allowing more time for the reference driver to settle.

The ADC provides a precharge buffer option for the REFP input to reduce the charge drawn by the sampling capacitor. The precharge buffer provides the coarse charge for the reference sampling capacitor C_{REF}. Halfway through the sample phase, the precharge buffer is bypassed (S_1 is in an up position as demonstrated in 図 8-5), at which time the external driver provides the fine charge to the sampling capacitor. Because the buffer reduces the charge demand of the sampling capacitor, the bandwidth requirement of the external driver is greatly reduced.

Many applications either ground REFN, or connect REFN to AVSS. A precharge buffer for REFN is not necessary for these cases. For applications when REFN is not a low impedance source, consider buffering the REFN input.

8.3.2.1 Reference Voltage Range

The operation of the ADC is optimized by separating the reference voltage into two operating ranges: low-reference range and high-reference range. The reference voltage range must be programmed to match the applied reference voltage, such as 2.5 V or 4.096 V. The low-reference operating range is 0.5 V to 2.75 V, and the high-reference operating range is 1 V up to the AVDD1 – AVSS power supplies. For best performance where the ranges overlap, such as reference voltage = 2.5 V, use the low-reference range. Program the REF_RNG bit of the CONFIG1 register to the appropriate reference range to match the applied reference voltage. When the high-reference range is selected, the input range is internally forced to 1x.

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8.3.3 Clock Operation

図 8-6 shows the block diagram of the internal clock circuit. The ADC can be operated by an external clock or the internal oscillator. The nominal value of f_{CLK} is 25.6 MHz in high-speed mode and 3.2 MHz in low-speed mode. A divide-by-eight option is available at the CLK input to divide the high-speed mode clock frequency to provide the low-speed mode clock frequency. The clock frequency is divided by two to derive the modulator sampling clock (f_{MOD}).

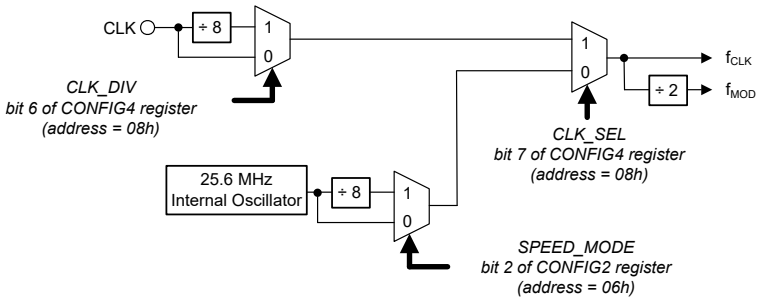

図 8-6. Clock Block Diagram

8.3.3.1 Internal Oscillator

At power-up and after reset, the ADC defaults to internal oscillator mode (CLK_SEL bit = 0b). The frequency of the internal oscillator automatically scales to high-speed or low-speed operation. Because of the clock jitter associated with the internal oscillator, the internal oscillator is only recommended for dc signal measurements. AC signal measurements are not recommended when using the internal oscillator.

When changing the clock mode from an external clock to the internal oscillator, maintain the external clock for at least four cycles after completing the SPI register write command used to change the clock mode. After the clock mode changes, the ADC ignores control inputs (the START and $\overline{\text{RESET}}$ pins) for a period of 150 µs to allow time for the internal oscillator to stabilize.

8.3.3.2 External Clock

To operate the ADC with an external clock, apply the clock signal to the CLK pin, then program the CLK_SEL bit to 1b. A divide-by-eight option is available to operate the ADC in low-speed mode using the high-speed mode clock frequency (set the CLK_DIV bit = 1b). The clock can be decreased from nominal to yield specific data rates between the integer OSR values. However, the conversion noise when operating at the reduced clock frequency is the same as the higher clock frequency. Reducing the conversion noise is only possible by increasing the OSR value or changing the filter mode.

Clock jitter results in timing variations in the modulator sampling that leads to degraded SNR performance. A low-jitter clock is essential to meet data sheet SNR performance. For example, with a 200-kHz signal frequency, an external clock with < 10-ps (rms) jitter is required. For lower signal frequencies, the clock jitter requirement can be relaxed by –20 dB per decade of signal frequency. For example, with f_{IN} = 20 kHz, a clock with 100-ps jitter can be used. Many types of RC oscillators exhibit high levels of jitter and should be avoided for ac signal measurement. Instead, use a crystal-based clock oscillator as the clock source. Avoid ringing on the clock input. A series resistor placed at the output of the clock buffer often helps reduce ringing.

8.3.4 Modulator

The ADS127L11 uses a switched-capacitor, third-order, singe-loop modulator with a 5-bit internal quantizer. This modulator topology achieves excellent noise and linearity performance while consuming very low power. As with most high-order modulators driven by high amplitude out-of-band signals, modulator saturation can occur. When saturated, the in-band signal still converts, however the noise floor increases. 図 8-7 illustrates the amplitude limit of out-of-band signals to avoid modulator saturation. The limit of dc and in-band signal amplitudes are 1 dB above standard full scale.

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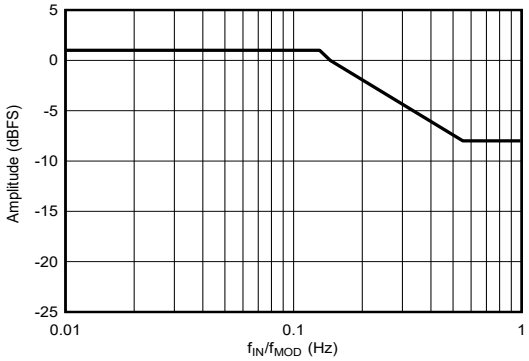

図 8-7. Amplitude Limit to Avoid Modulator Saturation

Modulator saturation is indicated by the MOD_FLAG bit of the STATUS register. The modulator saturation status is latched during the conversion period and is refreshed at completion of the next conversion. Modulator saturation resulting from out-of-band signals can be avoided by using an antialias filter at the ADC inputs. The *Typical Application* section describes an example of a fourth-order antialias filter, however a low-order filter can be used with equal effect provided the amplitude is below the saturation limit.

8.3.5 Digital Filter

The digital filter low-pass filters and decimates the low-resolution, high-speed data from the modulator to produce high-resolution, low-speed output data. The programmable oversampling ratio (OSR) determines the amount of filtering that affects signal bandwidth and conversion noise, and the final data rate through decimation. The output data rate is defined by: $f_{DATA} = f_{MOD} / OSR$.

The ADC offers the choice of two filter modes: wideband and low latency. The filter mode selection optimizes either the frequency response characteristics (wideband filter mode) or the time domain characteristics (low-latency filter mode).

8.3.5.1 Wideband Filter

The wideband filter is a multistage FIR filter design featuring linear phase response, low pass-band ripple, narrow transition band, and high stop-band attenuation. Because of the superior frequency response characteristics, the filter is well suited for measuring ac signals. The ADC provides eight programmable oversampling ratios (OSR) and two speed modes, offering a range of data rate and resolution to select from.

図 8-8 through 図 8-12 illustrate the frequency response of the wideband filter. 図 8-8 shows the pass-band ripple. 図 8-9 shows the detailed frequency response at the transition band.

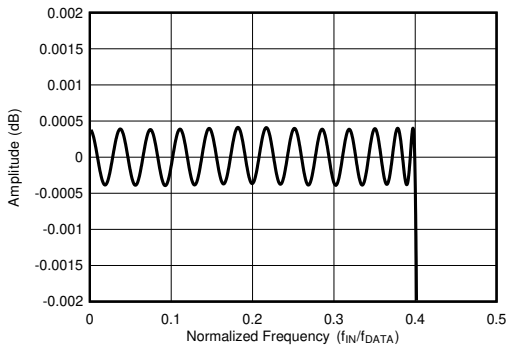

図 8-8. Wideband Filter Pass-Band Ripple

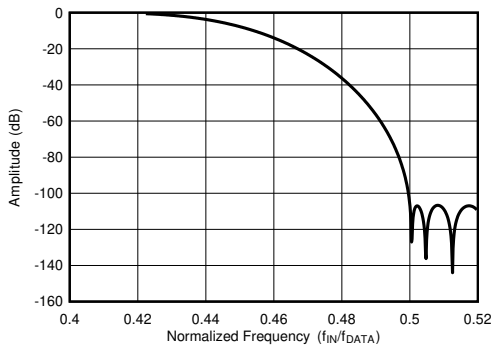

図 8-9. Wideband Filter Transition Band

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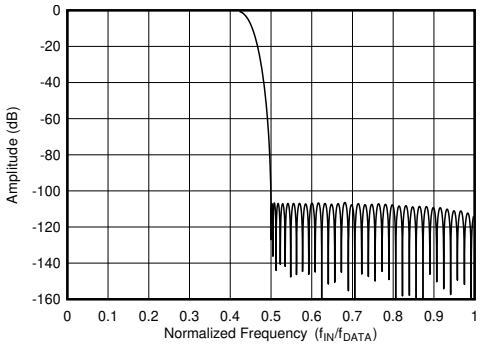
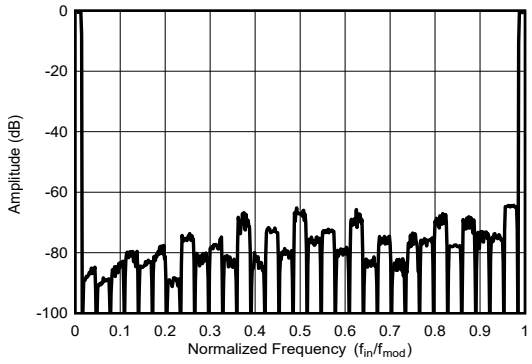
図 8-10 shows the frequency response to f_{DATA} for OSR ≥ 64. The stop band begins at f_{DATA} / 2 to prevent aliasing at the Nyquist frequency. 図 8-11 shows the stop-band attenuation to f_{MOD} for OSR = 32. In the stop-band region, out-of-band input frequencies intermodulate with multiples of the chop frequency at f_{MOD} / 32, creating a pattern of response peaks that exceed the stop-band attenuation of the digital filter. The width of the response peaks is twice the filter bandwidth. Stop-band attenuation is improved when used in conjunction with an antialias filter at the ADC input. See the *Typical Application* section for details of a fourth-order antialias filter.



OSR ≥ 64

図 8-10. Wideband Filter Frequency Response



OSR = 32

図 8-11. Wideband Filter Stop-Band Attenuation

図 8-12 shows the filter response centered around f_{MOD}. As shown, the filter response repeats at f_{MOD}. If not removed by an antialiasing filter, input frequencies at f_{MOD} appear as aliased frequencies in the pass band. Aliasing also occurs with input frequencies occurring at multiples of f_{MOD}. These frequency bands are defined by:

$$\text{Alias frequency bands: } (N \cdot f_{MOD}) \pm f_{BW} \tag{16}$$

where:

- *N* = 1, 2, 3, and so on
- f_{MOD} = Modulator sampling frequency
- f_{BW} = Filter bandwidth

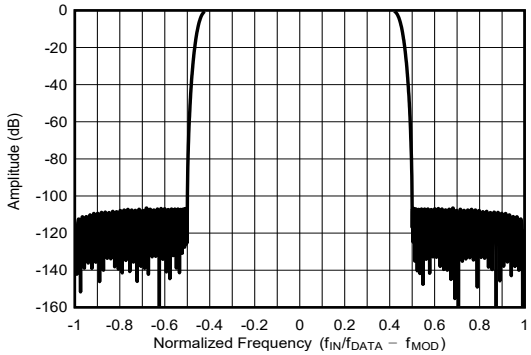


図 8-12. Wideband Filter Frequency Response Centered at f_{MOD}

The group delay of the filter is the time for an input signal to propagate from the input to the output of the filter. Because the filter is a linear-phase design, the envelope of a complex input signal is undistorted by the filter. The group delay (expressed in units of time) is constant versus frequency equal to the value = 34 / f_{DATA}. After a step input is applied, fully settled data occur at 68 data periods later. 図 8-13 illustrates the filter group delay (34 / f_{DATA}) and the settling time to a step input (68 / f_{DATA}).

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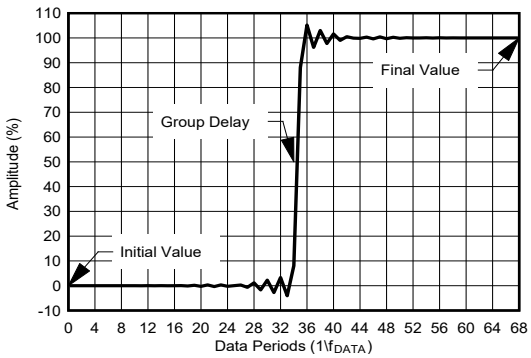

図 8-13. Wideband Filter Step Response

The digital filter is restarted when the ADC is synchronized. The ADC suppresses the first 68 conversion periods until the filter is fully settled. There is no need to discard data after synchronization. The time of data suppression is the conversion latency time as listed in the *latency time* column of 表 8-3. A 0.4-µs fixed overhead time is incurred for all data rates. If a step input occurs asynchronous to the conversion period without synchronizing, then the next 69 conversions are partially settled data.

表 8-3. Wideband Filter Characteristics

OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)				
32	400	165	174.96	170.6
64	200	82.5	87.48	340.6
128	100	41.25	43.74	680.6
256	50	20.625	21.87	1360.6
512	25	10.312	10.935	2720.6
1024	12.5	5.156	5.467	5440.6
2014	6.25	2.578	2.734	10880.6
4096	3.125	1.289	1.367	21760.6
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)				
32	50	20.625	21.87	1364.8
64	25	10.312	10.935	2724.8
128	12.5	5.156	5.467	5444.8
256	6.25	2.578	2.734	10884.8
512	3.125	1.289	1.367	21764.8
1024	1.5625	0.645	0.683	43524.8
2048	0.78125	0.322	0.342	87044.8
4096	0.390625	0.161	0.171	174084.8

(1) Latency time increases 8 / f_{CLK} (µs) when analog input buffers are enabled.

8.3.5.2 Low-Latency Filter (Sinc)

The low-latency filter is a cascaded-integrator-comb (CIC) topology that minimizes the delay (latency) as the conversion data propagates through the filter. The CIC filter is otherwise known as a sinc filter because of the characteristic sinx/x (sinc) frequency response. The latency time is shorter compared to the wideband filter, making the filter suitable for fast acquisition of dc signals. The device offers the choice of four sinc filter configurations: sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1 to provide trade-offs of acquisition time, noise performance, and line-cycle rejection.

Latency is defined as the time from synchronization to the falling edge of $\overline{\text{DRDY}}$, at which time, fully settled data are available. There is no need to discard data because the unsettled data are suppressed by the ADC. Detailed latency data for each sinc filter mode are given in 表 8-5 through 表 8-8.

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If the input is changed without synchronization, then the next conversion data are partially settled. The number of conversions required for fully settled data in this case is found by rounding the latency time value to the next whole number of conversion periods.

式 17 is the general expression of the sinc-filter frequency response. For single-stage sinc filter options (for example, the single-stage sinc3 or sinc4 filter), the second stage is not used.

$$\left|H_{(f)}\right| = \left| \frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A\sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^{n} \cdot \left| \frac{\sin\left[\frac{AB\pi f}{f_{MOD}}\right]}{B\sin\left[\frac{A\pi f}{f_{MOD}}\right]} \right| \quad (17)$$

where:

- f = Signal frequency
- A = Stage 1 OSR
- B = Stage 2 OSR
- $f_{MOD} = f_{CLK} / 2$ = 12.8 MHz (high-speed mode), 1.6 MHz (low-speed mode)
- n = Order of the stage 1 filter (3 or 4)

8.3.5.2.1 Sinc4 Filter

The sinc4 filter averages and decimates the high-speed modulator data to yield data rates from 1066.6 kSPS to 3.125 kSPS in high-speed mode, and data rates from 133.333 kSPS to 0.390625 kSPS in low-speed mode. Increasing the OSR value decreases the data rate and simultaneously reduces signal bandwidth and total noise resulting from increased decimation and data averaging.

Because of the reduced amount of data averaging performed in the filtering process for OSR values = 12, 16 and 24, the output resolution of the corresponding data rates is reduced. 表 8-4 summarizes the output data resolution for these OSR values.

表 8-4. Sinc4 Data Resolution

OSR	DATA RATE (kSPS)	RESOLUTION (bits)
12	1066.666	19
16	800	20.5
24	533.333	23
≥32	≤400	24

表 8-5 lists the sinc4 filter characteristics.

表 8-5. Sinc4 Filter Characteristics

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)			
12	1066.666	242.666	4.38
16	800	182	5.63
24	533.333	121.333	8.13
32	400	91.0	10.63
64	200	45.5	20.63
128	100	22.75	40.63
256	50	11.375	80.63
512	25	5.687	160.63
1024	12.5	2.844	320.63
2048	6.25	1.422	640.63
4096	3.125	0.711	1280.63

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表 8-5. Sinc4 Filter Characteristics (continued)

OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)			
12	133.333	30.333	35.04
16	100	22.75	45.04
24	66.666	15.166	65.04
32	50	11.375	85.04
64	25	5.687	165.04
128	12.5	2.844	325.04
256	6.25	1.422	645.04
512	3.125	0.711	1285.04
1024	1.5625	0.355	2565.04
2048	0.78125	0.177	5125.04
4096	0.390625	0.089	10245.04

(1) Latency time increases 8 / f_{CLK} (µs) when analog input buffers are enabled.

図 8-14 and 図 8-15 show the sinc4 filter frequency response at OSR = 32. The frequency response consists of a series of response nulls occurring at discrete frequencies. The null frequencies occur at multiples of f_{DATA}. At the null frequencies, the filter has zero gain. A folded image of the overall frequency response appears at multiples of f_{MOD}, as illustrated in the f_{MOD} frequency plot of 図 8-15. No attenuation is provided by the filter at input frequencies near n · f_{MOD} (n = 1, 2, 3, and so on), and if present, alias into the pass band.

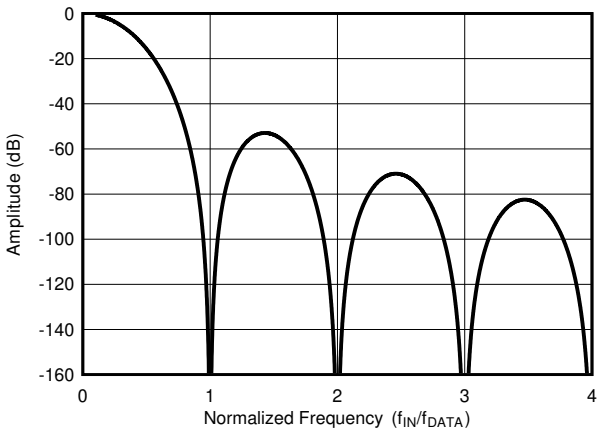

図 8-14. Sinc4 Frequency Response (OSR = 32)

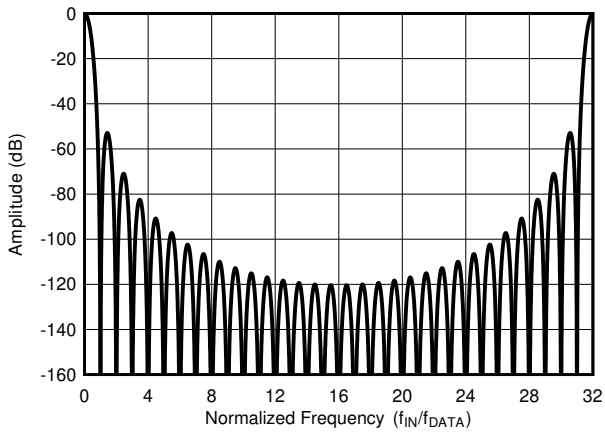

図 8-15. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

8.3.5.2.2 Sinc4 + Sinc1 Filter

The sinc4 + sinc1 filter is the cascade of two filter sections: sinc4 and sinc1. The OSR of the sinc4 stage is a constant value (32) and the programmable OSR of the sinc1 stage determines the output data rate. The sinc4 + sinc1 filter mode has comparably less latency time than that of the single-stage sinc4 filter. 表 8-6 summarizes the sinc4 + sinc1 filter characteristics.

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表 8-6. Sinc4 + Sinc1 Filter Characteristics

SINC4 OSR	SINC1 OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)	LATENCY TIME (µs)(1)
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)				
32	2	200	68.35	13.13
32	4	100	40.97	18.13
32	10	40	17.47	33.13
32	20	20	8.814	58.13
32	40	10	4.420	108.13
32	100	4	1.770	258.13
32	200	2	0.885	508.13
32	400	1	0.442	1008.13
32	1000	0.4	0.177	2508.13
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)				
32	2	25	8.544	105.04
32	4	12.5	5.121	145.04
32	10	5	2.184	265.04
32	20	2.5	1.102	465.04
32	40	1.25	0.552	865.04
32	100	0.5	0.221	2065.04
32	200	0.25	0.111	4065.04
32	400	0.125	0.055	8065.04
32	1000	0.05	0.022	20065.04

(1) Latency time increases 8 / f_{CLK} (µs) when analog input buffers are enabled.

図 8-16 shows the frequency response of the sinc4 + sinc1 filter for three values of OSR. The combined frequency response is the overlay of the sinc1 filter with the sinc4 filter. For low values of OSR, the response profile is dominated by the rolloff of the sinc4 filter. Nulls in the frequency response occur at n · f_{DATA}, n = 1, 2, 3, and so on. At the null frequencies, the filter has zero gain.

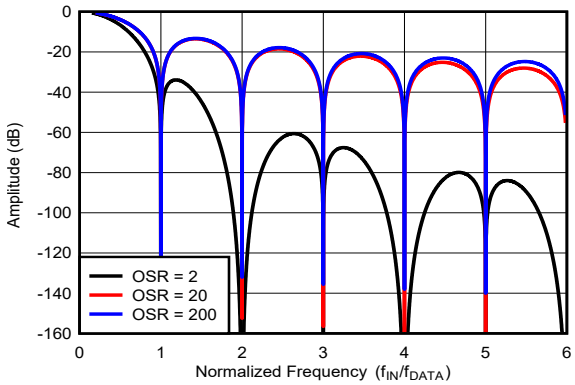

図 8-16. Sinc4 + Sinc1 Frequency Response

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8.3.5.2.3 Sinc3 Filter

The sinc3 filter mode is a single-stage filter. Relatively high values of OSR provide line-cycle rejection with data rates = 480 SPS, 400 SPS, 60 SPS, and 50 SPS. Because of the large width of the frequency response notch, excellent line-frequency NMRR and CMRR can be achieved with this filter. 表 8-7 summarizes the characteristics of the sinc3 filter.

表 8-7. Sinc3 Filter Characteristics

OSR	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	LATENCY (ms)	REJECTION OF FIRST NULL (dB)	
				2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)					
26667	480	126	6.25	100	71
32000	400	105	7.50	100	71
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)					
26667	60	15.7	50.01	100	71
32000	50	13.1	60.01	100	71

図 8-17 shows the frequency response of the sinc3 filter (OSR = 32000). 図 8-18 shows the detailed response in the region of 0.9 to 1.1 · f_{IN} / f_{DATA}.

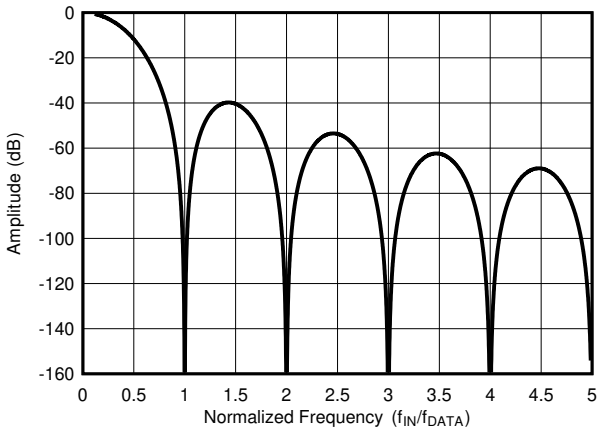

図 8-17. Sinc3 Frequency Response (OSR = 32000)

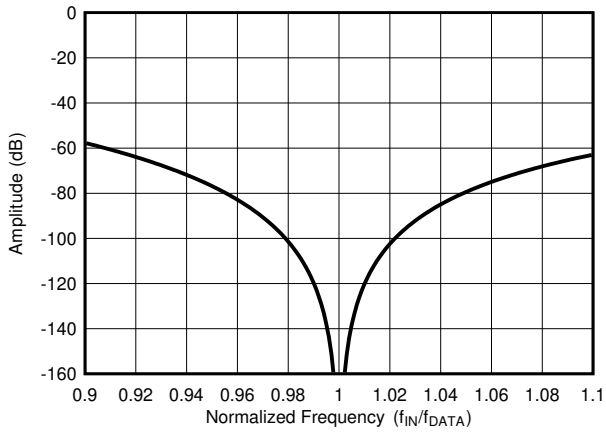

図 8-18. Detail Sinc3 Frequency Response (OSR = 32000)

8.3.5.2.4 Sinc3 + Sinc1 Filter

The sinc3 + sinc1 filter mode is the cascade of the sinc3 and the sinc1 filter. The OSR of the sinc3 stage is fixed (32000) and the OSR of the sinc1 stage is programmable to 3 and 5. 表 8-8 summarizes the characteristics of the sinc3 + sinc1 filter.

表 8-8. Sinc3 + Sinc1 Filter Characteristics

SINC3 OSR	SINC1 OSR	DATA RATE (SPS)	–3-dB FREQUENCY (HZ)	LATENCY (ms)	REJECTION OF FIRST NULL (dB)	
					2% CLOCK TOLERANCE	6% CLOCK TOLERANCE
HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)						
32000	3	133.3	54	12.5	37	26
32000	5	80	34	17.5	37	26
LOW-SPEED MODE (f_{CLK} = 3.2 MHz)						
32000	3	16.7	6.7	100.1	34	26
32000	5	10	4.2	140.01	34	26

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図 8-19 shows the frequency response of the sinc3 + sinc1 filter. The frequency response exhibits the characteristic sinc filter response lobes and nulls. The nulls occur at f_{DATA} and at multiples thereof. 図 8-20 shows the detailed response in the region of 0.9 to 1.1 · f_{IN} / f_{DATA}.

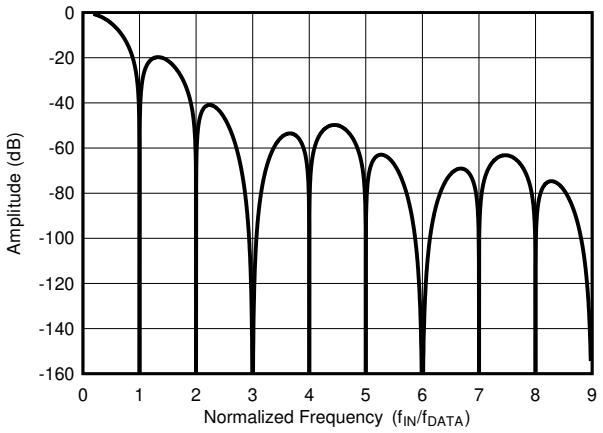

図 8-19. Sinc3 + Sinc1 Frequency Response

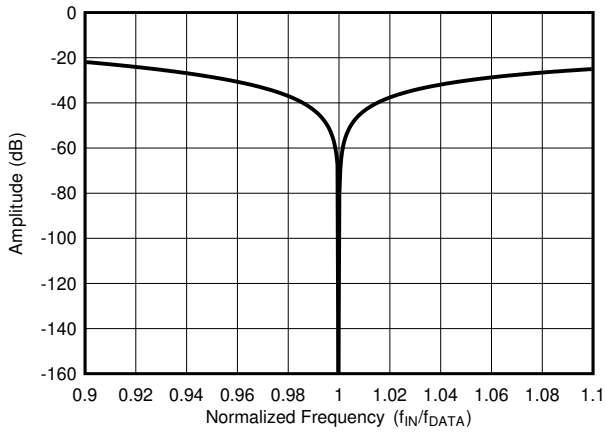

図 8-20. Detail Sinc3 + Sinc1 Frequency Response

8.3.6 Power Supplies

The device has three analog power-supply pins (AVDD1, AVSS, and AVDD2) and one digital power-supply pin (IOVDD). The power supplies can be sequenced in any order and are tolerant of slow or fast power-supply voltage ramp rates. However, in no case must any analog or digital input exceed the respective AVDD1 and AVSS (analog) or IOVDD (digital) power supply.

8.3.6.1 AVDD1 and AVSS

AVDD1 and AVSS power the precharge buffers and the internal sampling switches. The ADC can be configured either for bipolar input operation (such as using ±2.5-V power supplies), or for unipolar input operation (such as AVDD1 = 5 V and AVSS = DGND). Use a parallel combination of 1-µF and 0.1-µF bypass capacitors across the AVDD1 supply voltage and the AVSS pin, with a 3-Ω series resistor placed in series between the capacitors and the AVDD1 pin. Place the resistor and capacitors as close as possible to the AVDD1 pin.

8.3.6.2 AVDD2

AVDD2 is with respect to AVSS and powers the modulator core. AVDD2 can be connected to AVDD1 to simplify the required supply voltages, or AVDD2 can be operated by a lower supply voltage to minimize device power consumption. Use a combination of 1-µF and 0.1-µF bypass capacitors across the AVDD2 to AVSS supply pins.

表 8-9 shows examples of AVDD1, AVSS, and AVDD2 power-supply configurations.

表 8-9. AVDD1, AVSS, and AVDD2 Power-Supply Voltages (All Voltages with Respect to DGND)

SUPPLY CONFIGURATION	HIGH-SPEED MODE			LOW-SPEED MODE		
	AVDD1	AVSS	AVDD2	AVDD1	AVSS	AVDD2
Unipolar	5 V	0 V	1.8 V to 5 V	3 V to 5 V	0 V	1.8 V to 5 V
Bipolar	2.5 V	–2.5 V	0 V to 2.5 V	1.5 V to 2.5 V	–1.5 V to –2.5 V	0.3 V to 2.5 V

8.3.6.3 IOVDD

IOVDD is the digital I/O supply voltage pin for the device. IOVDD is internally regulated to 1.25 V to supply power to the digital core. Bypass IOVDD to DGND with a parallel combination of 1-µF and 0.1-µF capacitors. The voltage level of IOVDD is independent of the analog supply configuration.

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8.3.6.4 Power-On Reset (POR)

The ADC uses power-supply monitors to detect power-up and supply brownout events. Power-up or power-cycling of the IOVDD digital supply results in device reset. Power-up or power-cycling of the analog power supplies does not reset the ADC.

図 8-21 shows the digital power-on thresholds of the IOVDD and the internal CAPD voltages. When the voltages are above their respective thresholds, the ADC is released from reset. $\overline{DRDY}$ later transitions high when the SPI is ready for communication. If the START pin is high, the ADC immediately begins conversions with the $\overline{DRDY}$ pin pulsing for each conversion. However, valid conversion data only occur after the power supplies and reference voltage are stabilized. The POR_FLAG bit of the STATUS register indicates the device POR. Write 1b to clear the bit in order to detect the next POR event.

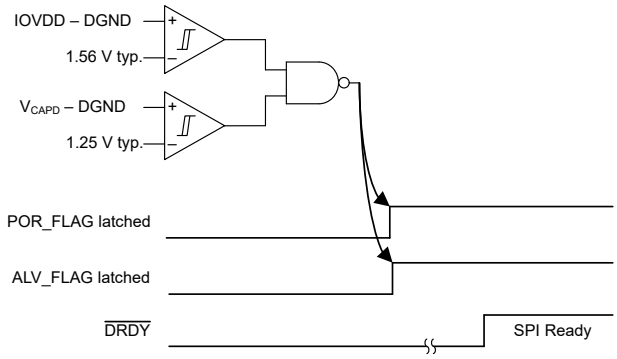

図 8-21. Digital Supply Threshold

図 8-22 shows the power-on thresholds of the analog power supplies. Four monitors are used for four analog supply voltage conditions (AVDD1 – DGND), (AVDD1 – AVSS), (AVDD2 – AVSS), and (CAPA – AVSS). Valid conversion data are available after all power supplies and the reference voltage are stabilized after power-on. The ALV_FLAG bit of the STATUS register sets when any analog power voltage falls below the respective threshold. Write 1b to clear the bit to detect the next analog supply low-voltage condition. Power cycling the analog power supplies does not reset the ADC. Because a low voltage on the IOVDD supply also resets the internal analog LDO (CAPA), the analog low-voltage flag (ALV_FLAG) is also set.

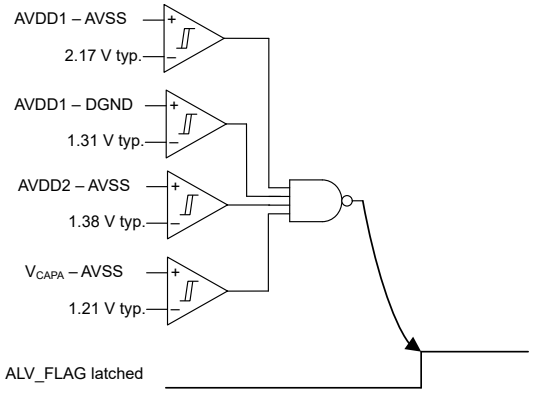

図 8-22. Analog Supply Threshold

8.3.6.5 CAPA and CAPD

CAPA and CAPD are the output voltages of the internal analog and digital voltage regulators. The regulators are used to reduce the supply voltage to operate internal sub-circuits and are not designed to drive external loads. CAPA is the analog regulator voltage output and is powered from AVDD2. The output voltage is 1.6 V with respect to AVSS. Bypass CAPA with a 1-µF capacitor to AVSS. CAPD is the digital regulator voltage output, powered from IOVDD. The regulator output is 1.25 V with respect to DGND. Bypass CAPD with a 1-µF capacitor to DGND.

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8.3.7 VCM Output Voltage

The VCM pin provides a buffered output voltage at the mid-point of the AVDD1 – AVSS power supply. The VCM voltage is intended to drive the output common-mode control input of a fully differential amplifier (FDA) to establish the common-mode voltage for the ADC input signal. With many types of FDAs, the same common-mode voltage is provided when the common-mode control input of these devices are floated when using the same power supply. If VCM is not used, the pin can be left unconnected. The VCM output is enabled by the VCM bit of the CONFIG1 register.

8.4 Device Functional Modes

8.4.1 Power-Scalable Speed Modes

The ADC offers two power-scalable speed modes that determine the range of conversion data rates and power consumed by the ADC. The modes allow optimization of signal bandwidth, data rate, and power consumption. High-speed mode provides maximum data rate and signal bandwidth, and low-speed mode minimizes power consumption for applications that do not require large signal bandwidths. The ADC clock frequency must be adapted to the operating mode. For high-speed mode the clock frequency is 25.6 MHz, and for low-speed mode the clock frequency is 3.2 MHz (see the *Clock Operation* section for the internal clock divider option). The speed mode is programmed by the SPEED_MODE bit of the CONFIG2 register.

8.4.2 Idle Mode

When conversions are stopped, the ADC can be programmed to remain in a full-powered idle mode or enter a low-power standby mode. In idle mode, the analog circuit remains fully operational, including sampling of the signal and voltage reference inputs. Only the digital filter is forced inactive. When conversions are restarted, the digital filter is reactivated to begin the conversion process. Idle mode (default) is programmed by the STBY_MODE bit of the CONFIG2 register.

8.4.3 Standby Mode

The ADC has the option of engaging the standby mode when conversions are stopped. Standby mode is an automatic power-down mode enabled by the STBY_MODE bit of the CONFIG2 register. Standby is entered and exited when conversions stop and start, respectively. During standby, sampling of the signal and reference voltage are stopped. When conversions are restarted, sampling of the signal and reference voltages resume. Exiting standby mode requires an additional 24 clock cycles to the normal conversion latency time.

8.4.4 Power-Down Mode

Power-down mode is engaged by setting the PWDN bit of the CONFIG2 register. In power-down mode, the analog and digital sections are powered off, except for a small bias current required to maintain SPI operation needed to exit power-down mode by clearing the register bit. The digital LDO also remains active to maintain user register settings. The sampling of the signal and voltage reference are stopped during power-down mode. Exit power-down mode by writing 0b to the PWDN bit or by resetting the device.

8.4.5 Reset

The ADC performs an automatic reset at power-on and can also be manually reset by the $\overline{\text{RESET}}$ pin or SPI operation. At reset the control logic, digital filter, and SPI restart and the user registers reset to the default values. See 図 6-3 for details when the ADC is available for operation after reset.

8.4.5.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is an active low input. The ADC is reset by taking $\overline{\text{RESET}}$ low then back high. Because the $\overline{\text{RESET}}$ pin has an internal 20-kΩ pullup resistor, $\overline{\text{RESET}}$ can be left unconnected if not used. The $\overline{\text{RESET}}$ pin is a Schmitt-triggered input designed to reduce noise sensitivity. See 図 6-3 for $\overline{\text{RESET}}$ pin timing and for the start of SPI communications after reset. Because the ADC performs an automatic reset at power-on, a reset is not required after device power-on.

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8.4.5.2 Reset by SPI Register Write

The device is reset through SPI operation by writing 01011000b to the CONTROL register. Writing any other value to this register does not result in reset. In 4-wire SPI mode, reset takes effect at the end of the frame at the time $\overline{CS}$ is taken high. In 3-wire SPI mode, reset takes effect on the last falling edge of SCLK of the register write operation. Reset in 3-wire SPI mode requires that the SPI is synchronized to the SPI host. If SPI synchronization is not assured, use the pattern described in the *Reset by SPI Input Pattern* section to reset the device. Reset can be validated by checking the POR_FLAG of the STATUS register.

8.4.5.3 Reset by SPI Input Pattern

The device is also reset through SPI operation by inputting a special bit pattern. The input pattern does not follow the input command format. There are two input patterns in which to reset the ADC. Pattern 1 consists of a *minimum* 1023 consecutive ones followed by one zero. The device resets on the falling edge of SCLK when the final zero is shifted in. This pattern can be used for either 3- or 4-wire SPI modes. 図 8-23 shows a pattern 1 reset example.

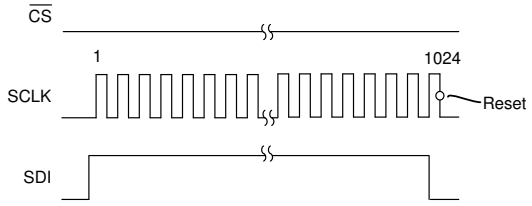

図 8-23. Reset Pattern 1 (3-Wire or 4-Wire SPI Mode)

Reset pattern 2 is only for use with the 4-wire SPI mode. To reset, input a *minimum* of 1024 consecutive ones (no ending zero value), followed by taking $\overline{CS}$ high at which time reset occurs. Use pattern 2 when the devices are connected in daisy-chain mode. 図 8-24 shows a pattern 2 reset example.

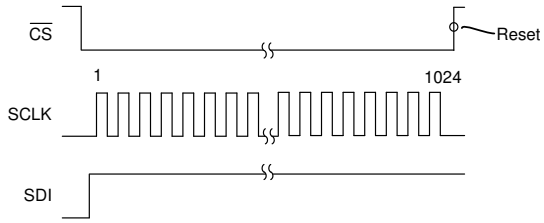

図 8-24. Reset Pattern 2 (4-Wire SPI Mode)

8.4.6 Synchronization

Conversions are synchronized and controlled by the START pin or, optionally, through SPI operation. If controlling conversions through SPI operation, keep the START pin low to avoid contention with the pin. Writing to any register from 04h through 0Eh causes the conversion to restart, thus resulting in loss of synchronization. Resynchronization of the ADC may be necessary in this case.

The ADC has three modes to synchronize and control conversions: synchronized, start/stop, and one-shot modes, each with specific functionalities. Program the selected mode of synchronization by the START_MODE[1:0] bits of the CONFIG2 register. Only the start/stop and one-shot control modes can be controlled through SPI operation.

After the ADC is synchronized, the first conversion is fully settled data but incurs a delay (latency time) compared to the normal data period. This latency is needed to account for full settling of the digital filter. The latency time depends on the data rate and the filter mode (see the *Digital Filter* section for filter latency details).

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8.4.6.1 Synchronized Control Mode

In synchronized control mode, the ADC converts continuously regardless if START is high or low. The ADC is synchronized on the rising edge of START. When synchronized, the first $\overline{\text{DRDY}}$ falling edge is delayed to account for the filter settling time (latency time). Both a single-pulse input and a continuous-clock input can be applied to the START pin in this mode.

The ADC synchronizes at the rising edge of START. If the time to the next rising edge of START is an *n* multiple of the conversion period, within a ±1 / f_{CLK} window, the ADC does not resynchronize (*n* = 1, 2, 3, and so on). Synchronization does not occur because the ADC conversion period is already synchronized to the period of the START signal. If the period of the START signal is *not* an *n* multiple of the conversion period, the ADC resynchronizes. As a result of the propagation delay of the digital filter, a phase difference exists between the START signal and the $\overline{\text{DRDY}}$ output. 図 8-25 shows synchronization to the START signal when the period of START pulses is not equal to an *n* multiple of the conversion period.

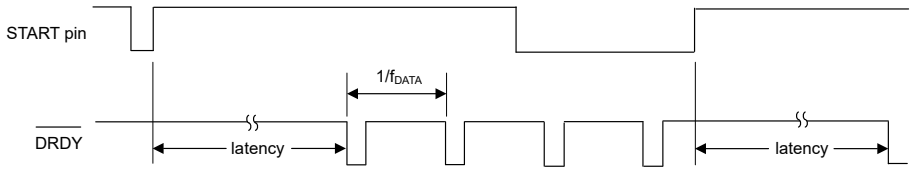

図 8-25. Synchronized Control Mode

8.4.6.2 Start/Stop Control Mode

Start/stop control mode is a gate-control mode used to start and stop conversions. Conversions are started by taking the START pin high or, if conversions are controlled through SPI operation, by writing 1b to the START bit of the CONTROL register. Preclear the CONTROL register by writing 00h before setting the START bit. Conversions continue until stopped by taking the START pin low, or by writing 1b to the STOP bit through SPI operation. $\overline{\text{DRDY}}$ is driven high at conversion start and is driven low when each conversion data are ready. If START is taken low or 1b is written to the STOP bit while conversions are in progress, the ongoing conversion finishes as normal and then stops. (See 図 6-4 for detailed START timing).

To restart an ongoing conversion, pulse START low to high, or write 1b to the START bit a second time. 図 8-26 shows the START and $\overline{\text{DRDY}}$ operation. If conversions are stopped in standby mode, $\overline{\text{DRDY}}$ returns high three clock cycles after falling low, otherwise $\overline{\text{DRDY}}$ remains low until being forced high at the eighth SCLK edge during conversion data readout. If data are not read, $\overline{\text{DRDY}}$ remains low and pulses high just before the next $\overline{\text{DRDY}}$ falling edge.

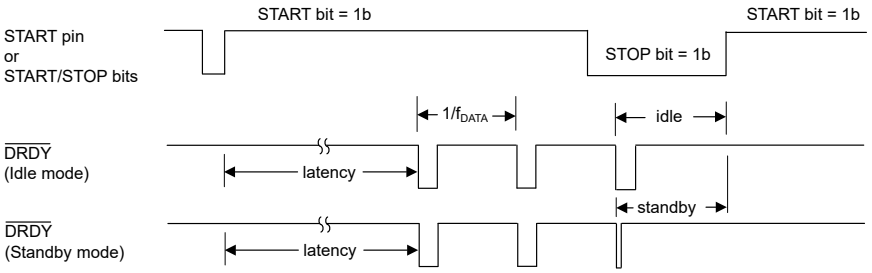

図 8-26. Start/Stop Control Mode

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8.4.6.3 One-Shot Control Mode

One-shot control mode initiates a single conversion when START is taken high or, through SPI operation, when the START bit of the CONTROL register is set to 1b. $\overline{\text{DRDY}}$ drives high to indicate the conversion is started and drives low when the conversion is complete. Data are available for readback at that time.

Taking START low, or writing 1b to the STOP bit, does not interrupt the ongoing conversion. The STOP bit has no effect. To restart the conversion, pulse START low to high, or write 1b to the START bit a second time. 図 8-27 shows the one-shot control mode operation. In standby mode, $\overline{\text{DRDY}}$ returns high three clock cycles after transitioning low, otherwise $\overline{\text{DRDY}}$ remains low until forced high at the next rising edge of START.

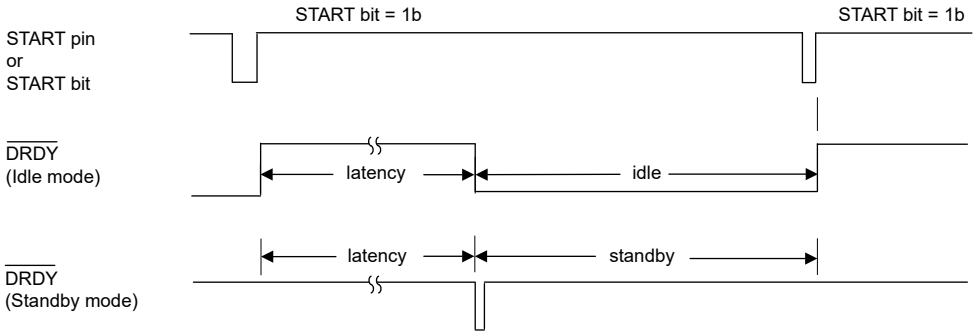

図 8-27. One-Shot Control Mode

8.4.7 Conversion-Start Delay Time

A programmable delay time is provided to delay the start of the conversion cycle after the START pin or START bit is asserted. This delay time allows for settling of external components, such as the voltage reference after exiting standby mode, or for additional settling time when switching the signal through an external multiplexer. After the initial delay time, subsequent conversions are not delayed. The programmed value of this delay time adds to the value of the conversion latency time of the digital filter. See the DELAY[2:0] bits of the CONFIG3 register for programming details.

8.4.8 Calibration

The ADS127L11 provides the ability to calibrate offset and gain errors by using user-programmable offset and gain correction registers. As shown in 図 8-28, the 24-bit offset correction value is subtracted from the conversion data before being multiplied by the 24-bit gain correction value. Output data are rounded to the final resolution (16- or 24-bit) and clipped to +FS and –FS code values after the scaling operation.

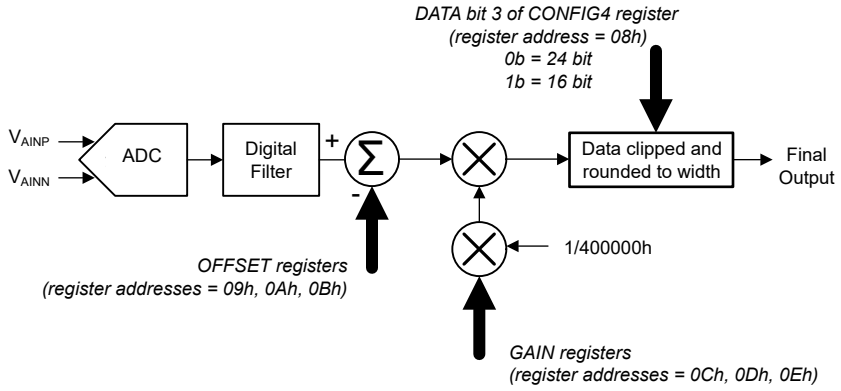

図 8-28. Calibration Block Diagram

式 18 shows how conversion data are calibrated:

$$\text{Final Output Data} = (\text{Data} - \text{OFFSET}) \times \text{GAIN} / 400000\text{h} \quad (18)$$

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8.4.8.1 OFFSET2, OFFSET1, OFFSET0 Calibration Registers (Addresses 9h, Ah, Bh)

The offset calibration value is a 24-bit value consisting of three 8-bit registers coded in 2's-complement format. The offset value is subtracted from the conversion data. Register 09h is the most-significant byte, register 0Ah is the middle byte, and register 0Bh is the least-significant byte. If the ADC is programmed to provide 16-bit resolution, the least-significant offset byte provides sub-LSB offset accuracy. 表 8-10 shows example offset calibration values.

表 8-10. Offset Calibration Values

OFFSET CALIBRATION VALUE	OFFSET APPLIED
000010h	–16 LSB
000001h	–1 LSB
FFFFFFh	1 LSB
FFFFF0h	16 LSB

8.4.8.2 GAIN2, GAIN1, GAIN0 Calibration Registers (Addresses 0Ch, 0Dh, 0Eh)

The gain calibration value is a 24-bit value consisting of three 8-bit registers coded in straight binary format and normalized to unity gain at 400000h. Register 0Ch is the most-significant byte, register 0Dh is the middle byte, and register 0Eh is the least-significant byte. For example, to correct a gain error greater than 1, the calculated gain calibration value is less than 400000h. 表 8-11 shows example gain calibration values.

表 8-11. Gain Calibration Values

GAIN CALIBRATION VALUE	GAIN APPLIED
433333h	1.05
400000h	1
3CCCCCh	0.95

8.4.8.3 Calibration Procedure

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to 000000h and 400000h, respectively.
2. Perform offset calibration by shorting the ADC inputs, or short the inputs at the system level to include the offset error of the external amplifier stages. Acquire conversion data and write the average value of the data to the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform gain calibration by applying a calibration signal to the ADC input or at the system level to include the gain error of the external buffer stages. For the standard input range mode, choose the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 3.9-V calibration signal with V_{REF} = 4.096 V. When operating in the extended range mode, the calibration signal can be equal to V_{REF} without causing clipped output codes. Acquire conversion data and average the results. Use 式 19 to calculate the gain calibration value.

$$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \cdot 400000\text{h} \quad (19)$$

For example, the expected output code of a 3.9-V calibration voltage using a 4.096-V reference voltage is: (3.9 V / 4.096 V) · 7FFFFFh = 79E000h.

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8.5 Programming

8.5.1 Serial Interface (SPI)

The serial interface is used to read conversion data, configure device registers, and control ADC conversions. The optional CRC mode is used to validate error-free data transmission between the host and ADC. A separate CRC based on the register map is used to detect register map changes after the initial register data are loaded.

The serial interface consists of four lines: $\overline{CS}$, SCLK, SDI, and SDO/$\overline{DRDY}$. The interface operates in the peripheral mode (passive) where SCLK is driven by the host. The interface is compatible to SPI mode 1 (CPOL = 0 and CPHA = 1). In SPI mode 1, SCLK idles low, and data are updated on SCLK rising edges and read on SCLK falling edges. The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously. The interface also supports daisy-chain connection of multiple ADCs to simplify the SPI connection.

8.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the interface for communication. The communication frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends the frame by interpreting the last 16-bits of input data (24 bits in CRC mode) regardless of the total number of bits shifted in. When $\overline{CS}$ is high, the SPI interface resets, commands are blocked, and SDO/$\overline{DRDY}$ enters a high-impedance state. $\overline{DRDY}$ is an active output regardless of the state of $\overline{CS}$. $\overline{CS}$ can be tied low to operate the interface in 3-wire SPI mode.

8.5.1.2 Serial Clock (SCLK)

SCLK is the serial clock input used to shift data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series termination resistor at the SCLK driver can often reduce ringing.

8.5.1.3 Serial Data Input (SDI)

SDI is the serial interface data input. SDI is used to input data to the device. Input data are latched on the falling edge of SCLK. SDI can be idled high or low when not active.

8.5.1.4 Serial Data Output/Data Ready (SDO/$\overline{DRDY}$)

SDO/$\overline{DRDY}$ is a dual-function output pin. This pin is programmable to provide output data only, or to provide output data and the data-ready indication. The dual-function mode multiplexes output data and data-ready operations on a single pin. Output data are updated on the rising edge of SCLK. The SDO/$\overline{DRDY}$ pin is in a high-Z state when $\overline{CS}$ is high. See the *SDO/$\overline{DRDY}$* section for details of dual-function operation. The SDO_MODE bit of the CONFIG2 register programs the mode.

8.5.2 SPI Frame

Communication through the serial interface is based on the concept of frames. A frame consists of a prescribed number of SCLKs required to shift in or shift out data. A frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device interprets the last 16 bits (or 24 bits in CRC mode) of input data regardless of the amount of data shifted into the device. In typical use, the input frame is sized to match the output frame by padding the frame with leading zeros if needed. However, if not transmitting and receiving data in full-duplex mode, the input data frame can be the minimum size of 16 bits (or 24 bits in CRC mode). The output frame size, as given in 表 8-12, depends on the programmed data resolution (16 or 24 bits) and optional STATUS header and CRC bytes. After the ADC is powered up or reset, the default output frame size is 24 bits. In 3-wire SPI mode, the input frame must match the size of the output frame for the SPI to remain synchronized.

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表 8-12. Output Frame Size

RESOLUTION	STATUS BYTE	CRC BYTE	FRAME SIZE
24 bit	No	No	24 bit
24 bit	No	Yes	32 bit
24 bit	Yes	No	32 bit
24 bit	Yes	Yes	40 bit
16 bit	No	No	16 bit
16 bit	No	Yes	24 bit
16 bit	Yes	No	24 bit
16 bit	Yes	Yes	32 bit

8.5.3 SPI CRC

The SPI cyclic redundancy check (CRC) is an SPI check code used to detect transmission errors to and from the host controller. A CRC byte is transmitted with the ADC input data by the host and a CRC byte is transmitted with the output data by the ADC. The SPI CRC error check is enabled by the SPI_CRC bit of the CONFIG4 register.

The CRC code is calculated by the host on the two command bytes. Any input bytes padded to the start of the frame are not included in the CRC calculation. The ADC checks the input command CRC code against an internal code calculated over the two input command bytes. If the CRC codes do not match, the command is not executed and the SPI_ERR bit is set in the STATUS byte. Register write operations are blocked except to the STATUS register to allow clearing the SPI CRC error by writing 1b to the SPI_ERR bit. Register read operations are not blocked unless an SPI_CRC error is detected in the immediately preceding register-read command frame.

The number of bytes used to calculate the output CRC code depends on the amount of data bytes transmitted in the frame. All data bytes that precede the output CRC code are used in the CRC calculation. 表 8-13 shows the number of bytes used for the output CRC calculation.

表 8-13. Byte Count of Output CRC Code

BYTE COUNT	BYTE FIELD DESCRIPTION
2	16 bits of conversion data
2	One byte of register data + 00h pad byte
3	16 bits of conversion data + STATUS byte
3	24 bits of conversion data
3	One byte of register data + two 00h pad bytes
4	24 bits of conversion data + STATUS byte
4	One byte of register data + three 00h pad bytes

The CRC code calculation is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the variable-length argument with the CRC polynomial. The CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 100000111. The input argument is XORed with FFh allowing error detection in the event that SDI or SDO/$\overline{\text{DRDY}}$ fail low.

The following procedure is used to compute the CRC code value:

1. Left shift the initial data value by eight bits by appending 0s in the LSB, creating a new data value.
2. XOR the MSB of the new data value from step 1 with FFh.
3. Align the MSB of the CRC polynomial (100000111) to the left-most, logic 1 of the data.
4. The bits of the data value that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result. XOR the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter-length value.

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5. If the XOR result is less than 100h, the procedure ends, yielding the 8-bit CRC code result. Otherwise, continue with the XOR operation at step 3 using the current XOR result. The number of loop iterations depend on the value of the initial data.

8.5.4 Register Map CRC

The register map CRC is used to check the register map contents for unintended changes. Write a new register map CRC code to the CRC register whenever the registers are changed. The CRC code is calculated over the 00h to 0Eh register addresses, skipping the 02h and 03h addresses (STATUS and CONTROL registers). The ADC continuously compares the CRC code written to the CRC register to an internal value. If the values do not match, the REG_ERR bit in the STATUS register is set. If set, correct the register values or update the CRC code then write 1b to the bit to clear the error flag. No other action is taken by the ADC in the event of a register map error. The register map CRC check is optional and is enabled by the REG_CRC bit of the CONFIG4 register.

Read the REV_ID register of the individual ADC when calculating the CRC code because the REV_ID can change during device production without notice. Set the REG_CRC bit to 1 (enabled) when calculating the CRC code because this bit must be set to enable the CRC check. The register map CRC code computation is the same as the one shown in the *SPI CRC* section.

8.5.5 Full-Duplex Operation

The serial interface supports full-duplex operation. Full-duplex operation allows the simultaneous transmission and reception of data in one frame. For example, the register read command for the next register can be input at the same time that data of the previously addressed register are output, which doubles the throughput when reading multiple registers. An example of full-duplex operation is illustrated in 図 8-30.

8.5.6 Device Commands

Commands are used to read and write register data. The register map of 表 8-16 consists of a series of one-byte registers, accessible by read and write operations. The minimum frame length of the input command sequence is two bytes (three bytes in CRC mode). If desired, the input command sequence can be padded with leading zeros to match the length of the output data frame. In CRC mode, the device interprets the two bytes immediately preceding the CRC byte at the end of the frame. 表 8-14 shows the ADS127L11 device commands.

表 8-14. SPI Commands

DESCRIPTION	BYTE1	BYTE2	BYTE 3 (Optional CRC Byte)
No operation	00h	00h	D7h
Read register command	40h + address [3:0]	don't care	CRC of byte 1 and byte 2
Write register command	80h + address [3:0]	register data	CRC of byte 1 and byte 2

There are special extended-length bit patterns that are longer than the standard command length. These patterns are used to reset the ADC and to reset the frame in three-wire SPI operation. The extended bit patterns are explained in the *Reset by SPI Input Pattern* and *3-Wire SPI Mode* sections.

8.5.6.1 No-Operation

The no-operation command bytes are 00h and 00h. Use this command if no input command is desired. If the SPI CRC check is enabled, the CRC byte is required (byte 3), which is always D7h for bytes 00h and 00h. SDI can be held low during data readback, but in CRC mode the SPI_ERR flag is set, which blocks future register write operations. The SPI_ERR flag can be ignored while reading conversion data until the next register write operation. At that point, the SPI_ERR flag of the STATUS register must be manually cleared by writing 1b.

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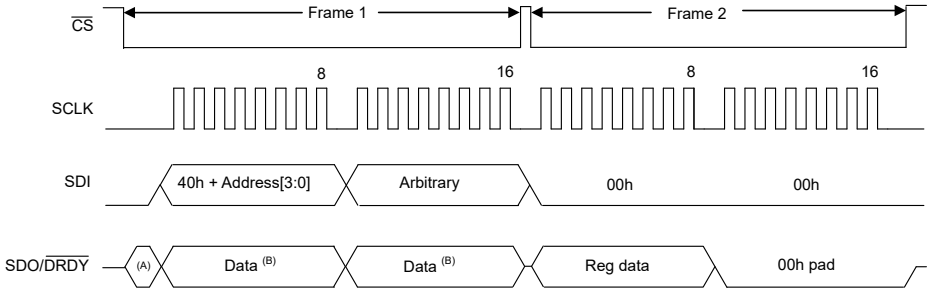
8.5.6.2 Read Register Command

The read register command is used to read register data. The command follows an off-frame protocol in which the read command is sent in one frame and the ADC responds with register data in the next frame. The first byte of the command is the base command value (40h) added to the 4-bit register address. The value of the second command byte is arbitrary, but is used together with the first byte for the CRC. The response to registers outside the valid address range is 00h. The register data format is most-significant-bit first.

図 8-29 shows an example of reading register data using the 16-bit output frame size. Frame 1 is the command frame and frame 2 is the data response frame. The frames are delimited by taking $\overline{CS}$ high. The data response frame is padded with 00h after the register data byte to fill the 16-bit frame. If desired, the data response frame can be shortened after the data byte by taking $\overline{CS}$ high.

If operating in full-duplex mode (such as a simultaneous read of 24-bit conversion data during the input of the register read command), pad the command frame with a leading 00h value to match the length of the data response frame. When configuring multiple registers, full-duplex operation can be used to double the throughput of the read register operations by inputting the next read register command during the data response frame of the previous register.



A. Previous state of SDO/$\overline{DRDY}$ before first SCLK.
B. Data are either 16 bits of conversion data, or if the read register command is sent in the prior frame, the data field is the register data byte + 00h.

図 8-29. Read Register Data, Minimum 16-Bit Frame Size

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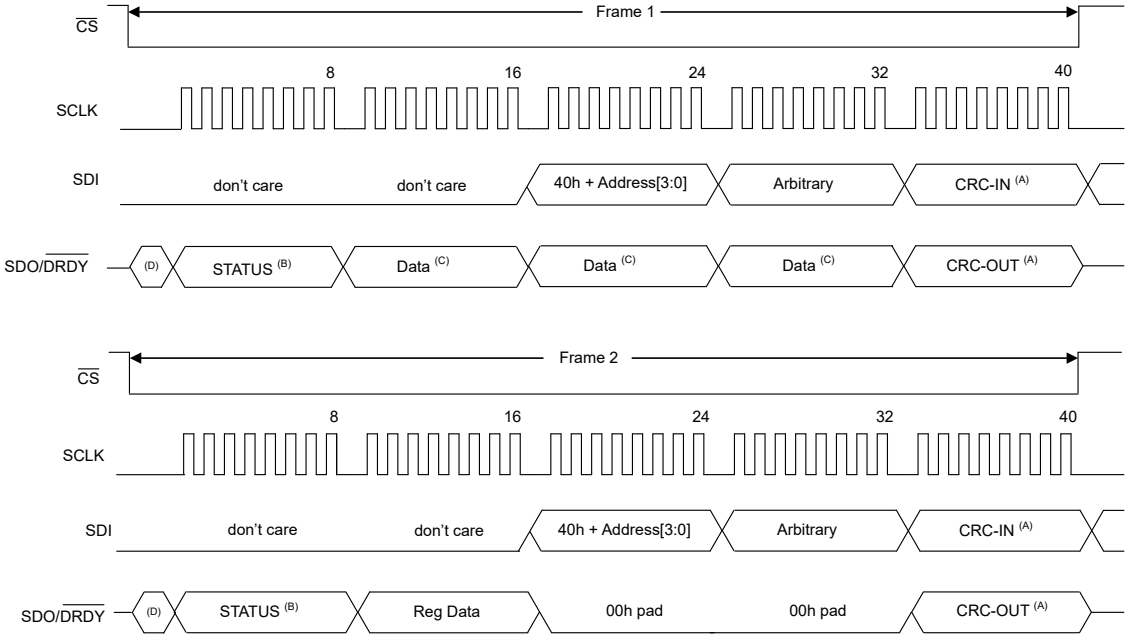
図 8-30 shows an example of the read register operation using the maximum 40-bit frame size in full-duplex operation. In frame 1, conversion data are output at the same time as the input of the read register command (if the previous frame was not a read register command). The input command is padded with two don't care bytes in order to match the length of the output data frame. The padded input bytes are excluded from the CRC-IN code calculation. Frame 2 shows the input of the next read register command concurrent with the output of the previous register data. Zeros are padded after the register data to place CRC-OUT in the same location as with a conversion data output frame. The CRC-OUT code includes all preceding bytes within the data output frame. The SPI_ERR bit of the STATUS header indicates if an SPI CRC error occurred and whether the read register command is accepted.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS byte. If STATUS is disabled, the frame shortens by one byte.
C. Depending on the previous operation, the data field is either conversion data or register data + two 00h pad bytes
D. Previous state of SDO/DRDY before the first SCLK.

図 8-30. Read Register Data, Maximum 40-Bit Frame Size

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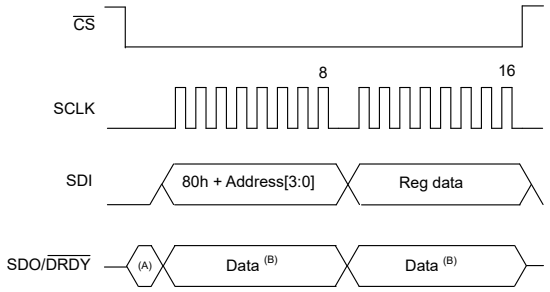
8.5.6.3 Write Register Command

The write register command is used to write register data. The write register operation is performed in a single frame. The first byte of the command is the base value (80h) added to the 4-bit register address. The second byte of the command is the register data. Writing to registers outside the valid address range is ignored.

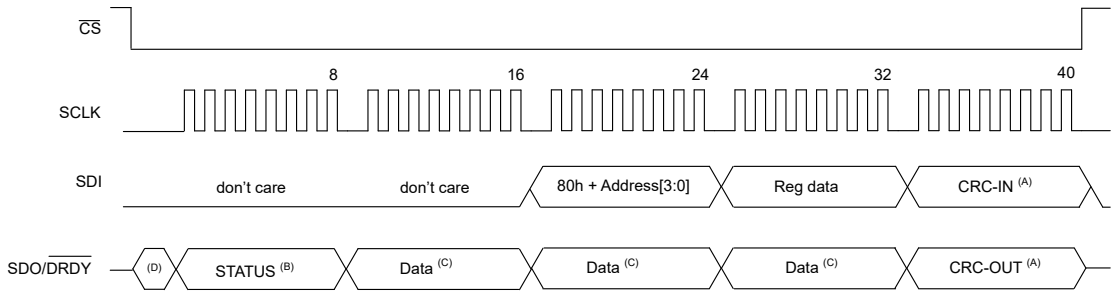
図 8-31 shows an example of a register write operation using the 16-bit frame size. If operating in full-duplex mode (simultaneous reading of 24-bit conversion data during the input of the register write command), include one or more leading pad bytes to the input data to match the length of the output frame. When configuring a series of registers (when conversion data can be ignored), the minimum 16-bit frame size can be used to improve throughput.



A. Previous state of SDO/DRDY before the first SCLK.
B. Data are either the conversion data, or if the read register command was sent in a prior frame, the data field is register data byte + one 00h pad byte.

図 8-31. Write Register Data, Minimum 16-Bit Frame Size

図 8-32 shows an example of a write register operation using the maximum 40-bit frame size. Full-duplex operation is also illustrated to show simultaneous input of the command and output of conversion data. The input frame is prefixed with two *don't care* bytes to match the output frame so all conversion data bytes are transmitted. Successful write operations are verified by reading back the register data, or by checking the SPI_ERR bit of the STATUS byte for input byte CRC errors. If an SPI CRC input error occurred, SPI_ERR is set and further register write operations are blocked (except for the STATUS register) until reset by writing 1b to the same SPI_ERR bit.



A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS byte. If STATUS is disabled, the frame shortens by one byte.
C. The data field is either 24-bits of conversion data, or if the read register command was sent in the prior frame, register data byte + two 00h pad bytes.
D. Previous state of SDO/DRDY before the first SCLK.

図 8-32. Write Register Data, Maximum 40-Bit Frame Size

8.5.7 Read Conversion Data

Conversion data are read by taking CS low and by applying SCLK to shift out the data directly (no command is used). Conversion data are buffered, which allows data to be read up to one f_{MOD} clock cycle before the next DRDY falling edge. Conversion data may be read multiple times until the next conversion data are ready. If the register read command was sent in the previous frame then register data replaces the conversion data.

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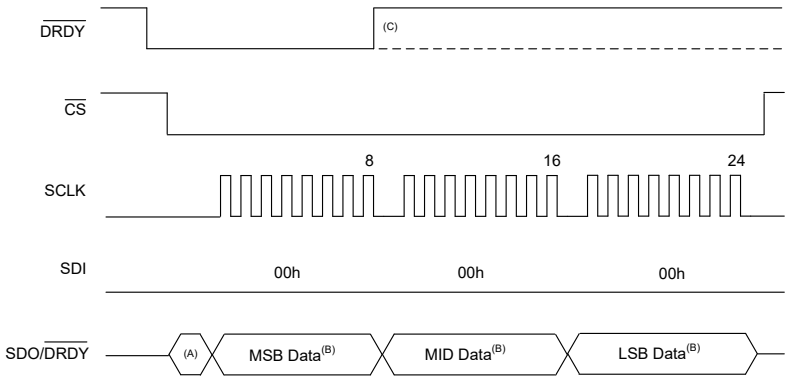
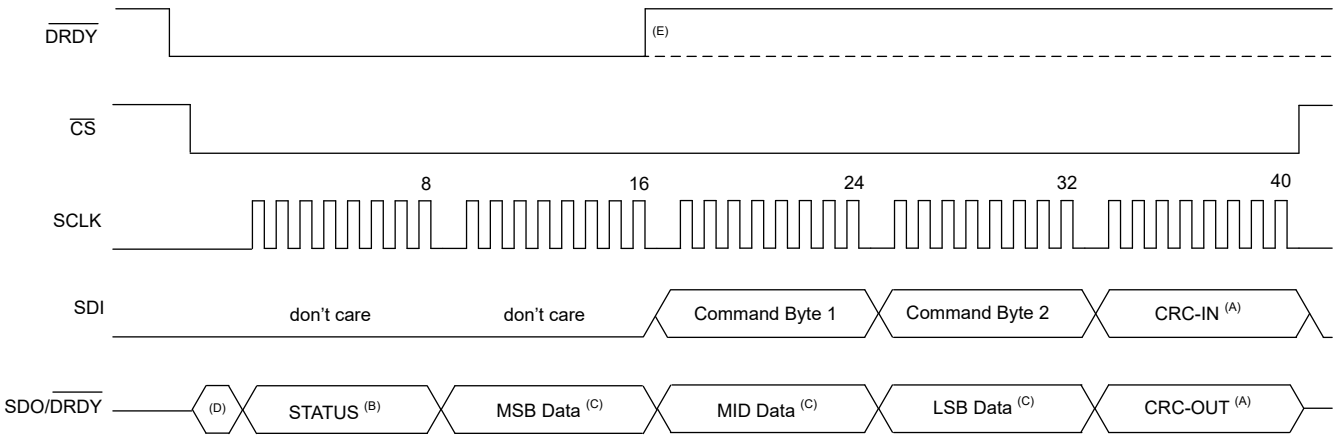
図 8-33 shows an example of reading 24-bit conversion data with the STATUS and CRC bytes disabled.



A. Before the first SCLK, SDO/DRDY is the previous state when SDO_MODE = 0b. Otherwise, SDO/DRDY follows DRDY.
B. The data field is two bytes (16-bit resolution) or three bytes (24-bit resolution).
C. In synchronized and start/stop control modes, DRDY returns high at the eighth SCLK falling edge. In one-shot control mode, DRDY remains low until a new conversion is started.

図 8-33. Conversion Data Read, Short Format

図 8-34 is an example of the long-format read data operation, which includes the STATUS header byte and the CRC byte. This example also shows the optional use of a full-duplex transmission when a register command is input at the same time the conversion data are output. If no input command is desired, the input bytes are 00h, 00h, and D7h. The output CRC (CRC-OUT) code computation includes the STATUS byte. If the conversion data readback is stopped after the eighth SCLK of the MSB data, DRDY returns high and the DRDY bit of the STATUS header goes low to indicate a data-read attempt.



A. Optional CRC byte. If the CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by one byte.
C. Data are two bytes (16-bit resolution) or three bytes (24-bit resolution).
D. If the SDO_MODE bit = 0, the previous state of SDO/DRDY remains until SCLK begins. Otherwise, SDO/DRDY follows DRDY.
E. In synchronized and start/stop control modes, DRDY returns high at the 16th SCLK falling edge (eighth bit of the MS data byte). In one-shot control mode, DRDY stays low until a new conversion is started.

図 8-34. Conversion Data Read, Long Format

Conversion data can be read asynchronous to DRDY. However, when conversion data are read close to the DRDY falling edge, there is uncertainty whether previous data or new data are output. If the SCLK shift operation starts at least one f_{MOD} clock cycle before the DRDY falling edge, then old data are provided. If the shift operation starts at least one f_{MOD} clock cycle *after* DRDY, then new data are output. The DRDY bit of the STATUS header indicates if the data are old (previously read data) or new.

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8.5.7.1 Conversion Data

Conversion data are coded in 2's-complement format, MSB first (sign bit), with resolution programmable to 24 bits or 16 bits. The resolution is programmed by the DATA bit of the CONFIG4 register. The SNR of 16-bit data is limited to 98.1 dB as a result of 16-bit quantization noise. 表 8-15 shows the output code for standard and extended input ranges shown for 24-bit resolution. The conversion data clips to positive and negative full-scale code values when the input signal exceeds the respective positive and negative full-scale values.

表 8-15. 24-Bit Output Data Format

DIFFERENTIAL INPUT VOLTAGE (V)(1)	24-BIT OUTPUT DATA(2)	
	STANDARD RANGE	EXTENDED RANGE
$1.25 \cdot k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	7FFFFFh
$k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	666666h
$k \cdot V_{REF} / 2^{23}$	000001h	000001h
0	000000h	000000h
$-k \cdot V_{REF} / 2^{23}$	FFFFFFh	FFFFFFh
$-k \cdot V_{REF}$	800000h	99999Ah
$-1.25 \cdot k \cdot V_{REF}$	800000h	800000h

(1) k = 1x or 2x input range option.
(2) Ideal output data, excluding offset, gain, linearity, and noise errors, and reduced data resolution with 12, 16, and 24 OSR values.

8.5.7.2 Data Ready

There are several methods available to determine when conversion data are ready for readback.

1. Hardware: Monitor the $\overline{\text{DRDY}}$ or the SDO/$\overline{\text{DRDY}}$ pin
2. Software: Monitor the DRDY bit of the STATUS header byte
3. Clock count: Count the number of ADC clocks to predict when data are ready

8.5.7.2.1 $\overline{\text{DRDY}}$

$\overline{\text{DRDY}}$ is the data-ready output signal. $\overline{\text{DRDY}}$ drives high when conversions are started or resynchronized, and drives low when conversion data are ready. $\overline{\text{DRDY}}$ is driven back high at the eighth SCLK during conversion data read. This behavior applies to the synchronized and the start/stop control modes. In one-shot control mode, $\overline{\text{DRDY}}$ stays low during conversion data read. If the ADC is programmed to enter standby mode (STBY_MODE bit = 1b), $\overline{\text{DRDY}}$ is driven back high three f_{CLK} cycles after transitioning low. If conversion data are not read, $\overline{\text{DRDY}}$ pulses high just prior to the next falling edge. See the *Synchronization* section for details of $\overline{\text{DRDY}}$ operation for each of the conversion control modes. $\overline{\text{DRDY}}$ is an active output whether $\overline{\text{CS}}$ is high or low.

8.5.7.2.2 SDO/$\overline{\text{DRDY}}$

SDO/$\overline{\text{DRDY}}$ is a dual-function output pin that can be programmed to automatically change modes from data ready, when not reading data, to data output mode, when reading data. This pin can replace the function of the $\overline{\text{DRDY}}$ pin to conserve the number of SPI I/O lines. When programmed to the dual-function mode (SDO_MODE bit = 1b) and when $\overline{\text{CS}}$ is low, SDO/$\overline{\text{DRDY}}$ mirrors $\overline{\text{DRDY}}$ until the first rising edge of SCLK, at which time the pin changes mode to provide data output. When the data read operation is complete (24th falling edge of SCLK, or 40th edge if the CRC and STATUS header bytes are included), the pin reverts back to mirroring $\overline{\text{DRDY}}$. 図 8-35 illustrates the operation of SDO/$\overline{\text{DRDY}}$.

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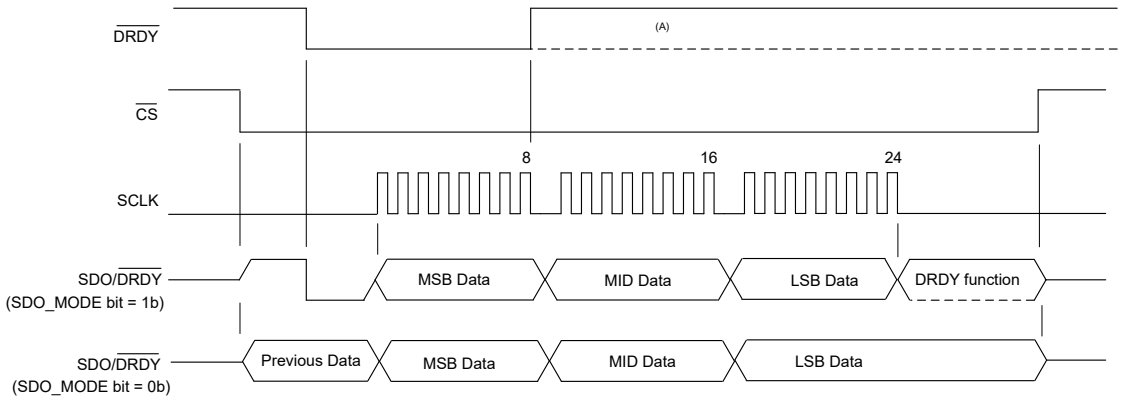

A. In synchronized and start/stop control modes, $\overline{\text{DRDY}}$ returns high at the eighth SCLK falling edge (eighth bit of MSB data). In one-shot control mode, $\overline{\text{DRDY}}$ stays low until a new conversion is started.

図 8-35. SDO/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$ Function

8.5.7.2.3 DRDY Bit

The software method of determining data ready is by polling the DRDY bit (bit 0 of the STATUS header). When DRDY = 1b, the data are new from the last data read operation, otherwise the data supplied are the previous data. After data are read, the bit stays cleared until the next conversion data are ready. To avoid missing data, poll the bit at least as often as the output data rate.

8.5.7.2.4 Clock Counting

Another method to determine when data are ready is to count clock cycles. This method is only possible using an external clock because the internal clock oscillator is not observable. After synchronization or conversion start, the number of clock cycles is larger compared to the normal conversion data period. The initial number of clock cycles is equal to the latency time of the digital filter as listed in the *Digital Filter* section.

8.5.7.3 STATUS Header

A STATUS header is an optional byte prefixed to the conversion data. See 表 8-20 for the STATUS header field descriptions. The STATUS header is enabled by setting the STATUS bit of the CONFIG4 register. The STATUS header byte sent with conversion data has the same content as the STATUS register.

8.5.8 Daisy-Chain Operation

In simultaneous-sampling systems using multiple ADCs, the devices can be connected in a daisy-chain string to reduce the number of SPI connections. A daisy-chain connection links together the SPI output of one device to the SPI input of the next device so the devices in the chain appear as a single logical device to the host controller. There is no special programming required for daisy-chain operation, simply apply additional shift clocks to access all devices in the chain. For simplified operation, program the same SPI frame size for each device (for example, when enabling the CRC option of all devices, thus producing a 32-bit frame size).

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図 8-36 shows four devices connected in a daisy-chain configuration. The SDI of ADS127L11 (1) connects to the host SPI data out, and SDO/$\overline{\text{DRDY}}$ of ADS127L11 (4) connects to the host SPI data input. The shift operation is simultaneous for all devices in the chain. After each ADC shifts out the conversion data, the data of SDI appears on SDO/$\overline{\text{DRDY}}$ to drive the SDI of the next device in the chain. The shift operation continues until the last device in the chain is reached. The SPI frame ends when $\overline{\text{CS}}$ is taken high, at which time the data shifted into each device is interpreted. The SDO/$\overline{\text{DRDY}}$ pin must be programmed to data output-only mode.

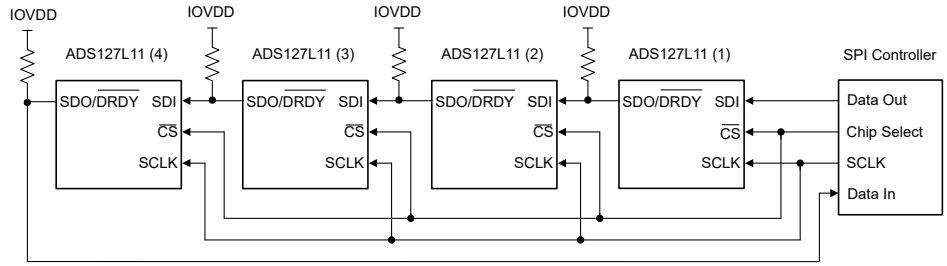


図 8-36. Daisy-Chain Connection

図 8-37 shows the 24-bit frame size of each device used at initial communication after device power up.

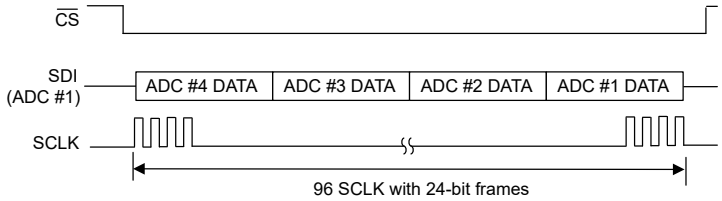
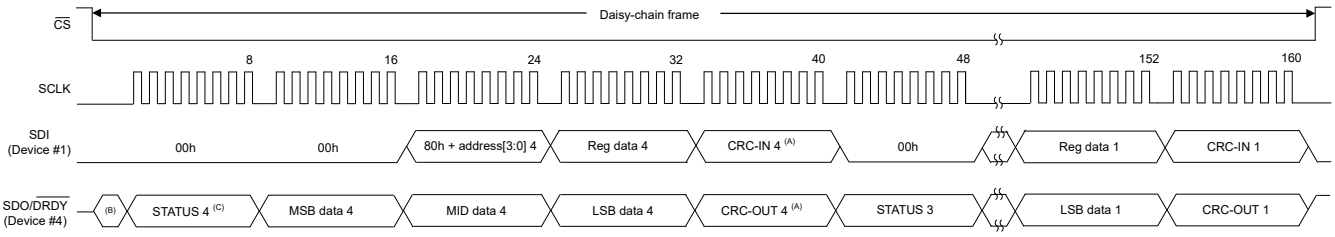


図 8-37. 24-Bit Data Input Sequence

To input data, the host first shifts in the data intended for the last device in the chain. The number of input bytes for each ADC is sized to match the output frame size. The default frame size is 24 bits, so initially each ADC requires three bytes by prefixing a pad byte in front of the two command bytes. The input data of ADC #4 is first, followed by the input data of ADC #3, and so forth.

図 8-38 shows the detailed input data sequence for the daisy-chain write register operation of 図 8-36. 40-bit frames for each ADC are shown (24-bits of data, with the STATUS and CRC bytes enabled). Command operations can be different for each ADC. The read register operation requires a second frame operation to read out the register data.



A. Optional CRC byte. If CRC is disabled, the individual frames shortens one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.
C. Optional STATUS header. If STATUS is disabled, the individual frames shorten one byte.

図 8-38. Write Register Data in Daisy-Chain Connection

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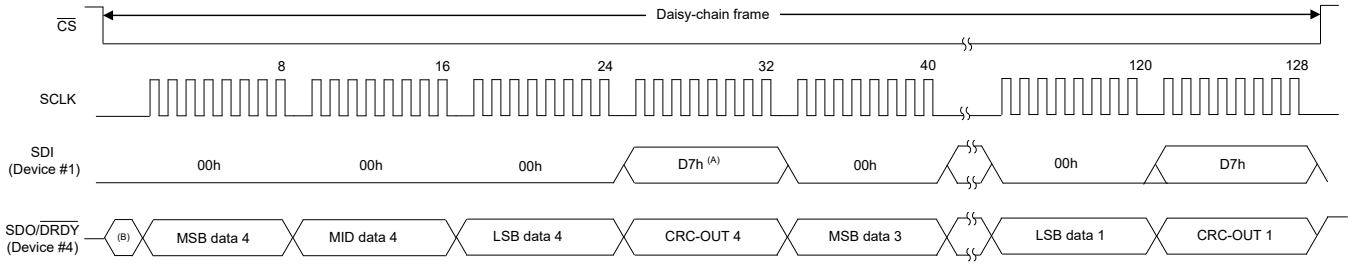
図 8-39 shows the clock sequence to read conversion data from the device connection provided in 図 8-36. This example illustrates a 32-bit output frame (24-bits of data, with the CRC byte enabled). The output data of ADC (4) is first in the sequence, followed by the data of ADC (3), and so on. The total number of clocks required to shift out the data is given by the number of bits per frame × the number of devices in the chain. In this example, 32-bit output frames × four devices result in 128 total clocks.



A. Optional CRC byte. If CRC is disabled, the individual frames shortens one byte.
B. Previous state of SDO/$\overline{\text{DRDY}}$ before SCLK is applied.

図 8-39. Read Conversion Data in Daisy-Chain Connection

As shown in 式 20, the maximum number of devices connected in daisy-chain configuration is limited by the SCLK signal frequency, data rate, and number of bits per frame. The same limitation applies to parallel-connected SPI because the data from each ADC is also read serially.

$$\text{Maximum devices in a chain} = \lfloor f_{SCLK} / (f_{DATA} \cdot \text{bits per frame}) \rfloor \quad (20)$$

For example, if f_{SCLK} = 20 MHz, f_{DATA} = 100 kSPS, and 32-bit frames are used, the maximum number of daisy-chain connected devices is the floor of: $\lfloor 20\ \text{MHz} / (100\ \text{kHz} \cdot 32) \rfloor = 6$.

8.5.9 3-Wire SPI Mode

The ADC has the option of 3-wire SPI operation by grounding $\overline{\text{CS}}$. 3-wire mode is detected by the ADC when $\overline{\text{CS}}$ is grounded at power up or after reset. 3-wire SPI mode is indicated by bit 7 (CS_MODE) of the STATUS register. The device changes to 4-wire SPI mode any time $\overline{\text{CS}}$ is taken high.

Because $\overline{\text{CS}}$ no longer controls frame timing in 3-wire SPI mode, SCLKs are counted by the ADC to determine the beginning and ending of a frame. The number of SCLK bits must be controlled by the host and must match the size of the output frame. The number of bits per frame depends on device configuration. The size of the output frame is shown in 表 8-12. Because frame timing is determined by the number of SCLKs, avoid inadvertent SCLK transitions, such as those possibly occurring at power up.

3-wire SPI mode supports the same command format and clocking as the 4-wire mode, except there is no $\overline{\text{CS}}$ toggling and therefore no wait time between frames.

8.5.9.1 3-Wire SPI Mode Frame Reset

In 3-wire SPI mode, an unintended SCLK can misalign the frame, resulting in loss of frame synchronization to the ADC. As shown in 図 8-40, the SPI is resynchronized without requiring an ADC reset by sending an SPI reset pattern. The reset pattern is a minimum of 63 consecutive 1s followed by one 0 at the 64th SCLK. The 65th SCLK starts a new SPI frame. Optionally, the ADC can be completely reset by toggling $\overline{\text{RESET}}$ or by the reset pattern shown in the *Reset by SPI Input Pattern* section.

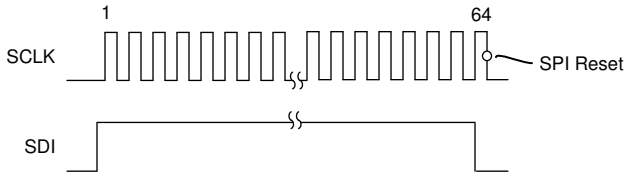


図 8-40. 3-Wire Mode SPI Reset Pattern

8.6 Registers

表 8-16 lists the register map of the ADS127L11. Register data are read or written one register at a time for each read or write operation in a frame. Writing to any register address 4h through Eh results in a conversion restart and loss of synchronization. If the ADC is idle (conversions are stopped), new conversions are not started.

表 8-16. ADS127L11 Register Map Overview

ADDRESS	REGISTER	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0h	DEV_ID	00h	DEV_ID[7:0]							
1h	REV_ID	xxh	REV_ID[7:0]							
2h	STATUS	x1100xxxb	CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	MOD_FLAG	DRDY
3h	CONTROL	00h	RESET[5:0]						START	STOP
4h	MUX	00h	RESERVED						MUX[1:0]	
5h	CONFIG1	00h	RESERVED	REF_RNG	INP_RNG	VCM	REFP_BUF	RESERVED	AINP_BUF	AINN_BUF
6h	CONFIG2	00h	EXT_RNG	RESERVED	SDO_MODE	START_MODE[1:0]		SPEED_MODE	STBY_MODE	PWDN
7h	CONFIG3	00h	DELAY[2:0]			FILTER[4:0]				
8h	CONFIG4	00h	CLK_SEL	CLK_DIV	OUT_DRV	RESERVED	DATA	SPI_CRC	REG_CRC	STATUS
9h	OFFSET2	00h	OFFSET[23:16]							
Ah	OFFSET1	00h	OFFSET[15:8]							
Bh	OFFSET0	00h	OFFSET[7:0]							
Ch	GAIN2	40h	GAIN[23:16]							
Dh	GAIN1	00h	GAIN[15:8]							
Eh	GAIN0	00h	GAIN[7:0]							
Fh	CRC	00h	CRC[7:0]							

表 8-17 lists the access codes of the registers.

表 8-17. Register Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1 DEV_ID Register (Address = 0h) [reset = 00h]

Return to the Register Map Overview.

図 8-41. DEV_ID Register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R-00h							

表 8-18. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID[7:0]	R	00h	Device ID. 00h = ADS127L11

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8.6.2 REV_ID Register (Address = 1h) [reset = xxh]

Return to the Register Map Overview.

図 8-42. REV_ID Register

7	6	5	4	3	2	1	0
REVID[7:0]							
R-xxxxxxxxb							

表 8-19. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Die revision ID The die revision ID can change during device production without notice.

8.6.3 STATUS Register (Address = 2h) [reset = x1100xxxb]

Return to the Register Map Overview.

図 8-43. STATUS Register

7	6	5	4	3	2	1	0
CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	REG_ERR	ADC_ERR	MOD_FLAG	DRDY
R-xb	R/W-1b	R/W-1b	R/W-0b	R/W-0b	R-xb	R-xb	R-xb

表 8-20. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CS_MODE	R	xb	$\overline{CS}$ mode. This bit indicates 4-wire or 3-wire SPI mode. The mode is determined by the state of $\overline{CS}$ at power up or after reset. 0b = 4-wire SPI operation ($\overline{CS}$ is active) 1b = 3-wire SPI operation ($\overline{CS}$ is tied low)
6	ALV_FLAG	R/W	1b	Analog supply low-voltage flag. This bit indicates a low-voltage condition occurred on the analog power supplies. Write 1b to clear the flag to detect the next low-voltage condition. 0b = No analog supply low-voltage condition from when flag last cleared 1b = Analog supply low-voltage condition detected
5	POR_FLAG	R/W	1b	Power-on reset (POR) flag. This bit indicates a reset from device power-on, by a brownout of the IOVDD supply, CAPD bypass output, or by a user-initiated reset. Write 1b to clear the flag to detect the next reset. 0b = No reset from when the flag last cleared 1b = Device reset occurred

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表 8-20. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	SPI_ERR	R/W	0b	SPI communication CRC error. This bit indicates an SPI CRC error. If set, register write operations are blocked, except for the STATUS register that allows clearing the error (write 1b to clear the error). Register read operations remain functional. The SPI CRC error detection is enabled by the SPI_CRC bit (CONFIG4 register). 0b = No error 1b = SPI CRC error
3	REG_ERR	R/W	0b	Register map CRC error. REG_ERR indicates if the written register map CRC (0Fh) value does not match the internal ADC calculated value. Write 1b to clear the register map CRC error or clear the REG_CRC bit. Set the REG_CRC bit (CONFIG4 register) to enable the register map error check. 0b = No error 1b = Register map CRC error
2	ADC_ERR	R	xb	Internal ADC error. ADC_ERR indicates an internal error. Perform a power cycle or reset the device. 0b = No ADC error 1b = ADC error detected
1	MOD_FLAG	R	xb	Modulator saturation flag. This bit indicates a transient or continuous modulator saturation occurred during the conversion cycle. The flag is updated at the completion of each conversion. 0b = Modulator not saturated 1b = Modulator saturation detected during the conversion cycle
0	DRDY	R	xb	Data-ready bit. DRDY indicates when new conversion data are ready. The DRDY bit is the inverse of the $\overline{\text{DRDY}}$ pin. Poll the bit to determine if conversion data are new or are repeated data from the last read operation. DRDY = 1 indicates data are new. In one-shot control mode, the bit remains at 1b until a new conversion is started. 0b = Data are not new 1b = Data are new

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8.6.4 CONTROL Register (Address = 3h) [reset = 00h]

Return to the Register Map Overview.

図 8-44. CONTROL Register

7	6	5	4	3	2	1	0
RESET[5:0]						START	STOP
W-000000b						W-0b	W-0b

表 8-21. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESET[5:0]	W	000000b	Device reset. Write 010110b to reset the ADC. The adjacent START and STOP bits must be set to 00b in the same write operation to reset the ADC. These bits always read 000000b.
1	START	W	0b	Start conversion. Conversions are started or restarted by writing 1b. Preclear the CONTROL register by writing 00h prior to writing the START bit. In one-shot control mode, one conversion is started. In start/stop control mode, conversions are started and continue until stopped by the STOP bit. Writing 1b to START while a conversion is ongoing restarts the conversion. This bit has no effect in synchronized control mode. Writing 1b to both the START and STOP bits has no effect. START is self-clearing and always reads 0b. 0b = No operation 1b = Start or restart conversion
0	STOP	W	0b	Stop conversion. This bit stops conversions after the current conversion completes. This bit has no effect in synchronized control mode. Writing 1b to both the START and STOP has no effect. STOP is self-clearing and always reads 0b. 0b = No operation 1b = Stop conversion after the current conversion completes

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8.6.5 MUX Register (Address = 4h) [reset = 00h]

Return to the Register Map Overview.

図 8-45. MUX Register

7	6	5	4	3	2	1	0
RESERVED						MUX[1:0]	
R-000000b						R/W-00b	

表 8-22. MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	000000b	Reserved
1:0	MUX[1:0]	R/W	00b	Input multiplexer selection. These bits select the polarity of the analog input and selects the test modes. See the *Analog Input* section for details. 00b = Normal input polarity 01b = Inverted input polarity 10b = Offset and noise test: AINP and AINN disconnected, ADC inputs internally shorted to (AVDD1 + AVSS) / 2 11b = Common-mode test: ADC inputs internally shorted and connected to AINP

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8.6.6 CONFIG1 Register (Address = 5h) [reset = 00h]

Return to the Register Map Overview.

図 8-46. CONFIG1 Register

7	6	5	4	3	2	1	0
RESERVED	REF_RNG	INP_RNG	VCM	REFP_BUF	RESERVED	AINP_BUF	AINN_BUF
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b

表 8-23. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6	REF_RNG	R/W	0b	Voltage reference range selection. Program this bit to select the low- or high-reference voltage range to match the applied reference voltage. See the *Recommended Operating Conditions* table for the range of reference voltages. When the high-reference range is selected, the INP_RNG bit is internally overridden to the 1x input range. 0b = Low-reference range 1b = High-reference range
5	INP_RNG	R/W	0b	Input range selection. This bit selects the 1x or 2x input range. See the *Input Range* section for more details. 0b = 1x input range 1b = 2x input range
4	VCM	R/W	0b	VCM output enable. This bit enables the VCM output voltage pin. The VCM voltage is (AVDD1 + AVSS) / 2. 0b = Disabled 1b = Enabled
3	REFP_BUF	R/W	0b	Reference positive buffer enable. This bit enables the REFP reference input precharge buffer. 0b = Disabled 1b = Enabled
2	RESERVED	R	0b	Reserved
1	AINP_BUF	R/W	0b	Analog input positive buffer enable. This bit enables the AINP analog input precharge buffer. 0b = Disabled 1b = Enabled
0	AINN_BUF	R/W	0b	Analog input negative buffer enable. This bit enables the AINN analog input precharge buffer. 0b = Disabled 1b = Enabled

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8.6.7 CONFIG2 Register (Address = 6h) [reset = 00h]

Return to the Register Map Overview.

図 8-47. CONFIG2 Register

7	6	5	4	3	2	1	0
EXT_RNG	RESERVED	SDO_MODE	START_MODE[1:0]		SPEED_MODE	STBY_MODE	PWDN
R/W-0b	R-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b

表 8-24. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EXT_RNG	R/W	0b	Extended input range selection. This bit extends the input range by 25%. See the *Input Range* section for more details. 0b = Standard input range 1b = 25% extended input range
6	RESERVED	R	0b	Reserved
5	SDO_MODE	R/W	0b	SDO/$\overline{\text{DRDY}}$ mode selection. This bit programs the mode of the SDO/$\overline{\text{DRDY}}$ pin to either data-output function only, or to dual-mode function of data output and data ready. For daisy-chain connection of ADCs, use the data-output function only mode. See the *SDO/$\overline{\text{DRDY}}$* section for more details. 0b = Data output only mode 1b = Dual mode: data output and data ready
4:3	START_MODE[1:0]	R/W	00b	START mode selection. These bits program the mode of the START pin. See the *Synchronization* section for more details. 00b = Start/stop control mode 01b = One-shot control mode 10b = Synchronized control mode 11b = Reserved
2	SPEED_MODE	R/W	0b	Speed mode selection. This bit programs the power-scalable speed mode of the device. The clock frequency corresponds to the mode. 0b = High-speed mode (f_{CLK} = 25.6 MHz) 1b = Low-speed mode (f_{CLK} = 3.2 MHz)
1	STBY_MODE	R/W	0b	Standby mode selection. This bit enables the auto engagement of the low-power standby mode after conversions are stopped. 0b = Idle mode; ADC remains fully powered when conversions are stopped. 1b = Standby mode; ADC powers down when conversions are stopped. Standby mode is exited when conversions restart.

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表 8-24. CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	PWDN	R/W	0b	Power-down mode selection. When set, the ADC is powered down. All functions are powered down except for SPI operation and the digital LDO to retain user register settings. 0b = Normal operation 1b = Power-down mode

8.6.8 CONFIG3 Register (Address = 7h) [reset = 00h]

Return to the Register Map Overview.

図 8-48. CONFIG3 Register

7	6	5	4	3	2	1	0
DELAY[2:0]			FILTER[4:0]				
R/W-000b			R/W-00000b				

表 8-25. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DELAY[2:0]	R/W	000b	Conversion-start delay time selection. Programmable delay time before the start of the *first* conversion when START is applied. Delay time is given in number of f_{MOD} clock cycles ($f_{MOD} = f_{CLK} / 2$). 000b = 0 001b = 4 010b = 8 011b = 16 100b = 32 101b = 128 110b = 512 111b = 1024

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表 8-25. CONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	FILTER[4:0]	R/W	00000b	Digital filter mode and oversampling ratio selection. These bits configure the digital filter. The digital filter has five modes: wideband, sinc4, sinc4 + sinc1, sinc3, and sinc3 + sinc1, each with a range of OSR values. See 表 7-1 through 表 7-5 for data rate and bandwidth information. 00000 = wideband, OSR = 32 00001 = wideband, OSR = 64 00010 = wideband, OSR = 128 00011 = wideband, OSR = 256 00100 = wideband, OSR = 512 00101 = wideband, OSR = 1024 00110 = wideband, OSR = 2048 00111 = wideband, OSR = 4096 01000 = sinc4, OSR = 12 01001 = sinc4, OSR = 16 01010 = sinc4, OSR = 24 01011 = sinc4, OSR = 32 01100 = sinc4, OSR = 64 01101 = sinc4, OSR = 128 01110 = sinc4, OSR = 256 01111 = sinc4, OSR = 512 10000 = sinc4, OSR = 1024 10001 = sinc4, OSR = 2048 10010 = sinc4, OSR = 4096 10011 = sinc4, OSR = 32 + sinc1, OSR = 2 10100 = sinc4, OSR = 32 + sinc1, OSR = 4 10101 = sinc4, OSR = 32 + sinc1, OSR = 10 10110 = sinc4, OSR = 32 + sinc1, OSR = 20 10111 = sinc4, OSR = 32 + sinc1, OSR = 40 11000 = sinc4, OSR = 32 + sinc1, OSR = 100 11001 = sinc4, OSR = 32 + sinc1, OSR = 200 11010 = sinc4, OSR = 32 + sinc1, OSR = 400 11011 = sinc4, OSR = 32 + sinc1, OSR = 1000 11100 = sinc3, OSR = 26667 11101 = sinc3, OSR = 32000 11110 = sinc3, OSR = 32000 + sinc1, OSR = 3 11111 = sinc3, OSR = 32000 + sinc1, OSR = 5

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8.6.9 CONFIG4 Register (Address = 8h) [reset = 00h]

Return to the Register Map Overview.

図 8-49. CONFIG4 Register

7	6	5	4	3	2	1	0
CLK_SEL	CLK_DIV	OUT_DRV	RESERVED	DATA	SPI_CRC	REG_CRC	STATUS
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 8-26. CONFIG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_SEL	R/W	0b	Clock selection. Selects internal or external clock operation. 0b = Internal clock operation 1b = External clock operation
6	CLK_DIV	R/W	0b	External clock divider selection. This bit is used to divide the external clock by 8. 0b = No clock division 1b = Clock division by 8
5	OUT_DRV	R/W	0b	Digital output drive selection. Select the drive strength of the digital outputs. 0b = Full-drive strength 1b = Half-drive strength
4	RESERVED	R	0b	Reserved
3	DATA	R/W	0b	Data resolution selection. This bit selects the output data resolution. 0b = 24-bit resolution 1b = 16-bit resolution
2	SPI_CRC	R/W	0b	SPI CRC enable. This bit enables the SPI CRC error check. When enabled, the device verifies the CRC input byte and appends a CRC output byte to the output data. The SPI_ERR bit of the STATUS byte sets if an input SPI CRC error is detected. Write 1b to the SPI_ERR bit to clear the error. 0b = SPI CRC function disabled 1b = SPI CRC function enabled
1	REG_CRC	R/W	0b	Register map CRC enable. This bit enables the register map CRC error check. Write the register map CRC value to the 0Fh register, calculated over registers 0h to 1h and 4h to Eh. An internal CRC value is compared to the value written to the register map CRC register. The REG_ERR bit of the STATUS byte sets if the CRC values do not match. 0b = Register map CRC function disabled 1b = Register map CRC function enabled

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表 8-26. CONFIG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STATUS	R/W	0b	STATUS byte output enable. Program this bit to prefix the STATUS byte to the conversion data output. 0b = Status byte not prefixed to the conversion data 1b = Status byte prefixed to the conversion data

8.6.10 OFFSET2, OFFSET1, OFFSET0 Registers (Addresses = 9h, Ah, Bh) [reset = 00h, 00h, 00h]

Return to the Register Map Overview.

図 8-50. OFFSET2, OFFSET1, OFFSET0 Registers

7	6	5	4	3	2	1	0
OFFSET[23:16]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[7:0]							
R/W-00000000b							

表 8-27. OFFSET Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFFSET[23:0]	R/W	000000h	User offset calibration value. Three registers form the 24-bit offset calibration word. OFFSET[23:0] is in 2's-complement representation and is subtracted from the conversion result. The offset operation precedes the gain operation.

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8.6.11 GAIN2, GAIN1, GAIN0 Registers (Addresses = Ch, Dh, Eh) [reset = 40h, 00h, 00h]

Return to the Register Map Overview.

図 8-51. GAIN2, GAIN1, GAIN0 Registers

7	6	5	4	3	2	1	0
GAIN[23:16]							
R/W-01000000b							
7	6	5	4	3	2	1	0
GAIN[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
GAIN[7:0]							
R/W-00000000b							

表 8-28. GAIN Registers Field Description

Bit	Field	Type	Reset	Description
23:0	GAIN[23:0]	R/W	400000h	User gain calibration value. Three registers form the 24-bit gain calibration word. GAIN[23:0] is in straight-binary representation and normalized to 400000h for gain = 1. The conversion data is multiplied by GAIN[23:0] / 400000h after the offset operation.

8.6.12 CRC Register (Address = Fh) [reset = 00h]

Return to the Register Map Overview.

図 8-52. CRC Register

7	6	5	4	3	2	1	0
CRC[7:0]							
R/W-00000000b							

表 8-29. CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CRC[7:0]	R/W	00h	Register map CRC value. The register map CRC is a user-computed value of registers 0h to 1h together with registers 4h through Eh. The value written to this register is compared to an internal CRC calculation. If the values do not match, the REG_ERR bit is set in the STATUS header byte and register. The register CRC check is enabled by the REG_CRC bit. If the register CRC function is disabled, this register is available for scratchpad purposes.

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9 Application and Implementation

注

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9.1 Application Information

The high-performance capability of the ADS127L11 is achievable when familiar with the requirements of the input driver, antialias filter, reference voltage, SPI clocking, and PCB layout. The following sections provide design guidelines.

9.1.1 SPI Operation

Although the ADC provides flexible clock options for the SPI interface and the range of IOVDD voltages, the following guidelines are recommended to achieve full data sheet performance.

1. Use an SCLK that is phase coherent to CLK; that is, ratios of 2:1, 1:1, 1:2, 1:4, and so on.
2. Minimize phase skew between SCLK and CLK (< 5 ns).
3. Operate IOVDD at the lowest voltage possible to reduce digital noise.
4. If IOVDD ≥ 3.3 V, consider operating SCLK continuously over the full conversion period to spread noise coupling over the full conversion period.
5. Keep the trace capacitance of SDO/$\overline{\text{DRDY}}$ ≤ 20 pF to reduce the peak currents associated with digital output transitions.

9.1.2 Input Driver

The ADC incorporates precharge buffers that reduce the settling and bandwidth requirement of the analog input driver. If a 10-MHz or less bandwidth driver is used, or if there is a long distance between the driver and the ADC inputs (such as a cable connection), enable the input precharge buffers. For higher gain-bandwidth drivers, the precharge buffers may be disabled to reduce power consumption, but in any case, full-rated THD and SNR data sheet performance is realized with the input precharge buffers active. In low-speed mode operation, the modulator sample rate is significantly reduced, therefore the driver has more time to settle between the input sampling pulses. Using a lower bandwidth input driver or disabling the precharge buffers can be practical options for low-speed operation.

9.1.3 Antialias Filter

Input signals occurring near f_{MOD} (12.8 MHz in high-speed mode and 1.6 MHz in low-speed mode) fold back (or alias) to the pass band, resulting in data errors. When aliased, the frequency errors cannot be removed by post processing. An analog antialias filter at the ADC inputs removes the frequencies from the input signal before they are aliased by the ADC. The required order of the antialias filter is dependent on the selected OSR and the target value of signal attenuation at f_{MOD}. A large value of OSR means more frequency range between the f_{DATA} Nyquist frequency and f_{MOD} for the filter to provide the desired roll off. For example, for OSR = 128, more than two decades of frequency separates f_{DATA} and f_{MOD}. With a corner frequency = f_{DATA}, a third-order, 60-dB per decade filter provides a 120-dB alias rejection at f_{MOD}.

9.1.4 Reference Voltage

For data sheet performance, the ADC requires a reference voltage with low noise and good drive strength to charge the sampled reference input. Because the modulator continuously samples the reference voltage whether conversions are ongoing or not (except in standby and power-down modes), the reference loading is constant, therefore incomplete settling of the reference voltage appears as a gain error to the system. The total system gain error can be calibrated. A 22-µF decoupling capacitor at the reference output and 1-µF and 0.1-µF capacitors directly across the reference input pins filters the reference input. The ADC also incorporates an optional reference precharge buffer for the positive input to buffer the reference voltage.

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9.1.5 Simultaneous-Sampling Systems

When using the ADC in a multichannel system, the same design principles apply with additional considerations for clock routing, synchronization, shared reference voltage and SPI clocking. See the *ADS127L11 in Simultaneous-Sampling Systems* application brief for details for use in simultaneous-sampling systems.

9.2 Typical Application

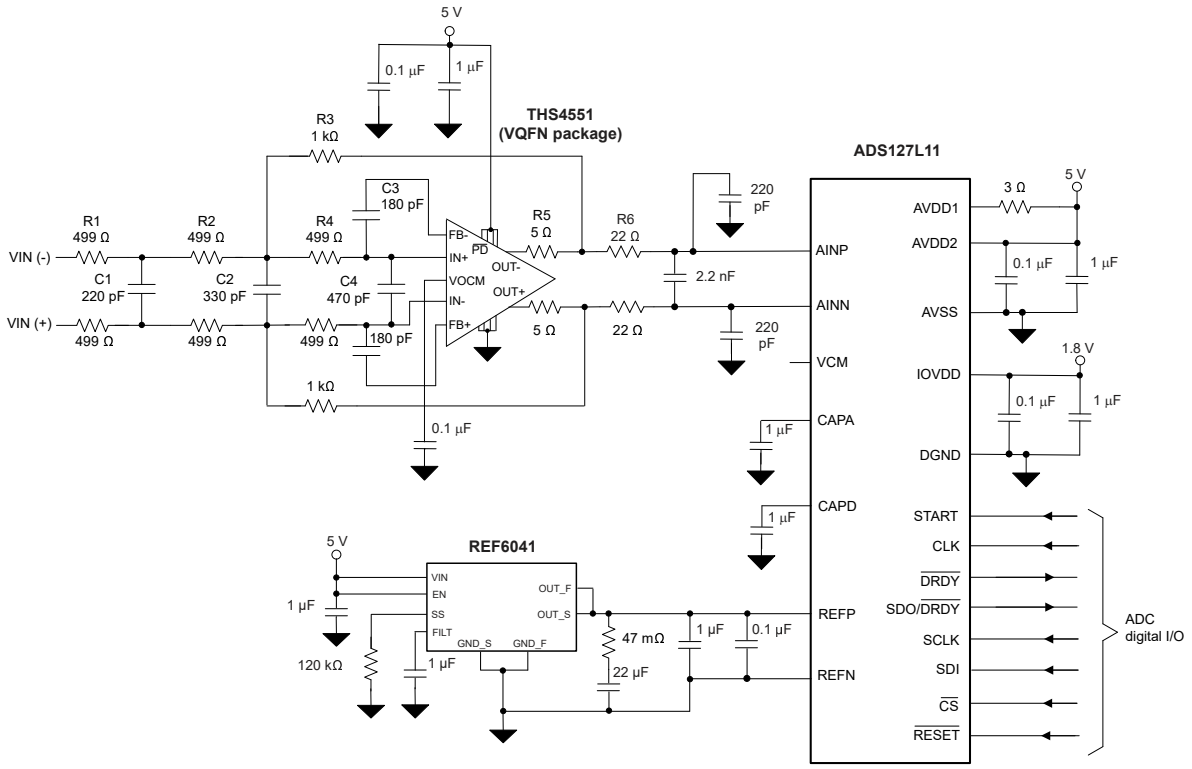

図 9-1. ADS127L11 Circuit Diagram

9.2.1 Design Requirements

図 9-1 shows an application of the ADS127L11 used in a precision data acquisition system. The goal of this design is an antialias filter at the ADC input to attenuate out-of-band signals at the modulator sample rate (f_{MOD}). The requirement of the antialias filter is 90-dB attenuation at the critical f_{MOD} frequency (12.8 MHz in high-speed mode) using the OSR = 32 setting in wideband filter mode. The filter is designed for a flat amplitude response and low group delay error within the pass band of the signal.

表 9-1 lists the target design values and the actual values in this design example.

表 9-1. Antialias Filter Design Requirements

FILTER PARAMETER	TARGET VALUE	ACTUAL VALUE
Voltage gain	0 dB	0 dB
Alias rejection at 12.8 MHz	90 dB	90 dB
–0.1-dB frequency	250 kHz	260 kHz
–3-dB frequency	500 kHz	550 kHz
Amplitude peaking	20 mdB	12 mdB
Group delay linearity	0.1 µs	0.017 µs
Total noise of filter and ADC (165-kHz bandwidth)	12 µV	11.8 µV

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9.2.2 Detailed Design Procedure

The antialias filter consists of a passive first-order input filter, an active second-order filter, and a passive first-order output filter. The filter is fourth-order overall. The filter design accommodates the worst-case wideband filter OSR value (32), which results in less than two decades of frequency range between the Nyquist frequency at f_{DATA} and the f_{MOD} frequency. The fourth-order filter provides 90-dB rolloff over this frequency range. The filter rolloff at f_{MOD} is the key function of the filter.

The THS4551 amplifier is selected for the active filter stage because of the 135-MHz gain-bandwidth product (GBP) and 50-ns settling time. The amplifier GBP is sufficient to maintain the filter rolloff at 12.8 MHz, even with the dc gain of 15 dB. For example, for applications where gain is desired, a 10-MHz amplifier has marginal GBP to fully support the required rolloff at the f_{MOD} frequency. The settling time specification of the THS4551 also makes the device a good choice for driving the ADC sampled inputs.

The design of the active filter section begins with an equal-R assumption to reduce the number of component values to select. The dc gain of the filter is R_3 / (R_1 + R_2). 1-kΩ resistors are selected to be low enough in value to keep resistor noise and amplifier input current noise from affecting the noise of the ADC.

The 1-kΩ input resistor is divided into two 499-Ω resistors (R_1 and R_2) to implement the first-order filter using C_1. The first-order filter is decoupled from the second-order active filter, but shares R_1 and R_2 to determine each filter stage corner frequency. The corner frequency is given by C_1 and the Thevenin resistance at the terminals of C_1 (R_{TH} = 2 × 250 Ω).

Given an arbitrary selection of R_4 (2 × 499 Ω in this case), the values of the 2 × 180 pF (C3) feedback capacitors and the single 330-pF differential capacitor (C2) are calculated by the filter design equations given in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The design inputs are filter f_O and filter Q for the multiple-feedback active filter topology. The differential capacitor (C_4) is not part of the filter design but is used to improve filter phase margin. The 5-Ω resistors (R_5) isolate the amplifier outputs from stray capacitance to further improve filter phase margin.

The final RC filter at the ADC inputs serves two purposes. First, the filter provides a fourth pole to the overall filter response, thereby increasing filter rolloff. The other purpose of the filter is a charge reservoir to filter the sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise can degrade because of incomplete amplifier settling. The input filter values are 2 × 22 Ω and 2.2 nF. The 22-Ω resistors are outside the THS4551 filter loop to isolate the amplifier outputs from the 2.2-nF capacitor to maintain phase margin.

Low voltage-coefficient C0G capacitors are used everywhere in the signal path for their low distortion properties. The amplifier gain resistors are 0.1% tolerance to provide best possible THD performance. The ADC VCM output connection to the amplifier VOCM input pin is optional because the same function is provided by the amplifier.

See the THS4551 data sheet for additional examples of active filter designs and application.

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9.2.3 Application Curves

The following figures are produced by the TINA-TI™, SPICE-based analog simulation program. The THS4551 SPICE model can be downloaded at the THS4551 product folder.

図 9-2 shows the frequency response of the antialias filter and the *total* response of the antialias filter and ADC. As shown in this image, the filter provides 90-dB stop-band attenuation from the Nyquist frequency to the 12.8-MHz f_{MOD} frequency.

図 9-3 shows the analog filter group delay. The 0.575-µs group delay is small in comparison to the 85-µs group delay of the ADC digital filter (34 / f_{DATA}). The analog filter group delay linearity is 0.017 µs, peaking at the edge of the 165-kHz pass band.

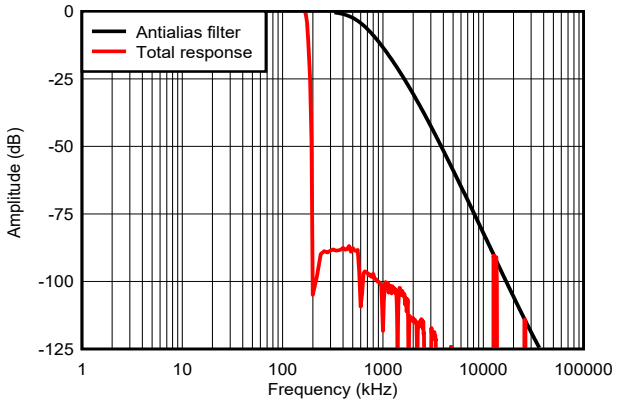

図 9-2. Antialias Filter Frequency Response

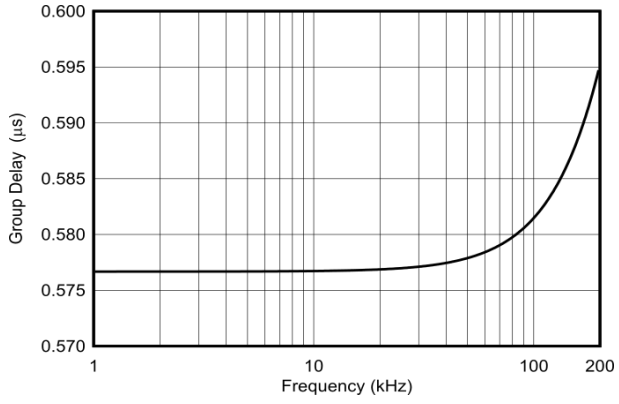

図 9-3. Antialias Filter Group Delay

図 9-4 shows the noise density of the antialias filter circuit, the noise density of the ADC, and the combined noise density of the filter and ADC. Noise density is the noise voltage per √Hz of bandwidth plotted versus frequency.

図 9-5 shows the total noise from the 1-Hz start frequency up to the ADC final bandwidth. Below 200 Hz, noise is dominated by 1 / f voltage and current noise of the THS4551 amplifier. Above 200 Hz, noise is dominated by ADC noise. The combined noise of the filter and ADC over the 165-kHz bandwidth is 11.8 µV, meeting the 12-µV target value.

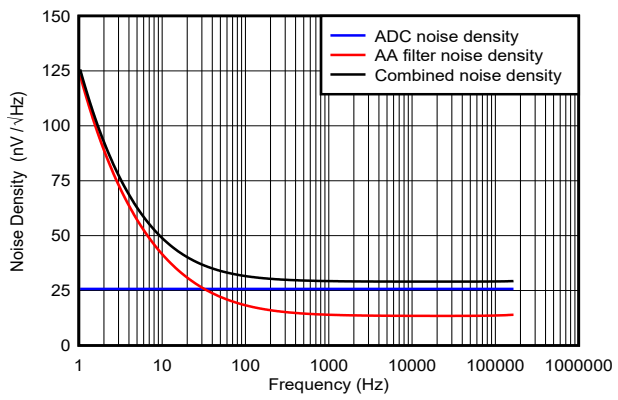

図 9-4. Noise Density

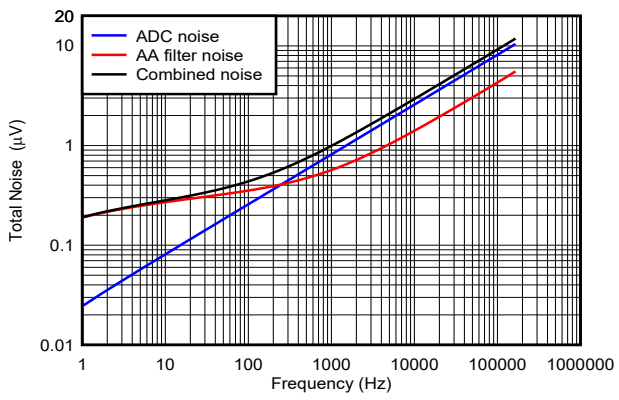

図 9-5. Total Noise

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9.3 Power Supply Recommendations

The ADC has three analog power supplies and one digital power supply. Power-supply voltages AVDD1 and AVSS establish the type of analog input signal range. Bipolar input signals are only possible using bipolar supply voltages, such as AVDD1 = 2.5 V and AVSS = –2.5 V, and only unipolar input signals are possible using unipolar supply voltages, such as AVDD1 = 5 V and AVSS = DGND.

The AVDD2 power-supply voltage is with respect to AVSS and the IOVDD power-supply voltage is with respect to DGND. The specified range of the power supplies are listed in the *Recommended Operating Conditions* table. The ADC can be operated using a single 5-V voltage for all supplies (or one 3-V voltage in low-speed mode) with AVSS = DGND. The ADC supply pins must always have separate bypass capacitors.

Power-supply bypassing at the device pins is essential to achieve data sheet performance. The ADC also requires capacitors for the CAPA and CAPD pins, and for the analog input and reference pins. Place the capacitors close to the device pins using short, direct traces with the smaller capacitor value placed closest to the device pins.

The recommended bypass components of the device pins are as follows:

1. AVDD1 to AVSS:
   a. Parallel combination of 1-µF and 0.1-µF capacitors across the AVDD1 power supply and AVSS
   b. A 3-Ω resistor placed in series between the bypass capacitors and the device AVDD1 pin
2. AVDD2 to AVSS: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
3. IOVDD to DGND: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
4. CAPA to AVSS: 1-µF capacitor placed across the pins
5. CAPD to DGND: 1-µF capacitor placed across the pins
6. REFP, REFN: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
7. AINP, AINN: 22-Ω resistors in series, followed by 2.2 nF across the pins, 220 pF from each pin to AVSS

図 9-6 shows the component placement for the device configured for unipolar power-supply operation.

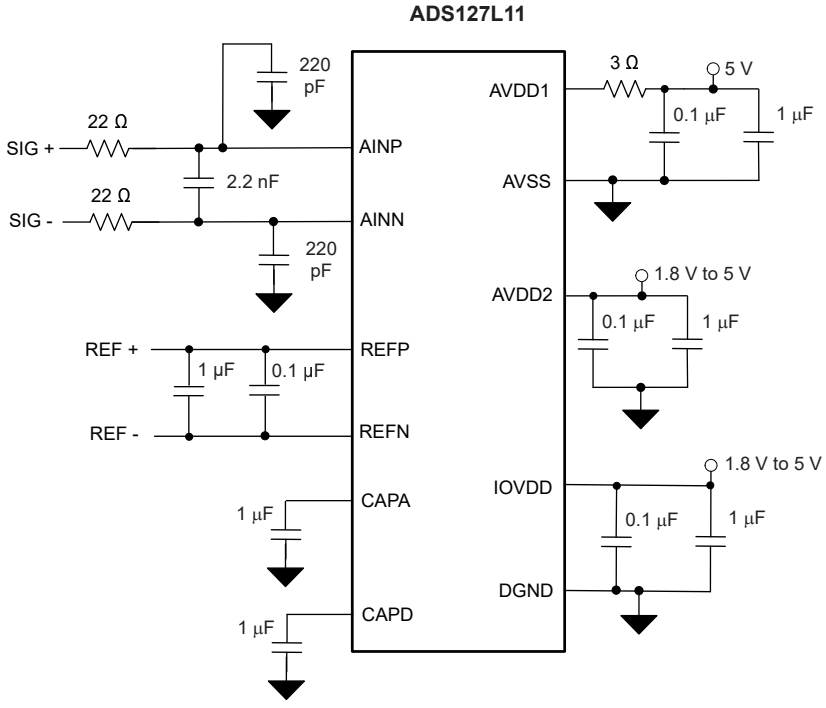

図 9-6. Device Bypass Recommendation

The power supplies do not require special sequencing and can be powered up in any order, but in no case must any analog or digital input exceed the respective AVDD1 and AVSS (analog) or IOVDD (digital) power-supply voltages. An internal reset is performed after the IOVDD power-supply voltage is applied.

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9.4 Layout

9.4.1 Layout Guidelines

To achieve data sheet performance, use a minimum four-layer PCB board with the inner layers dedicated to ground and power planes. Best performance is achieved by combining the analog and digital grounds on a single, unbroken ground plane. In some layout geometries, however, using separate analog and digital grounds may be necessary to help direct digital currents away from the analog ground (such as pulsing LED indicators, relays, and so on). In this case, consider separate ground return paths for these loads. When separate analog and digital grounds are used, join the grounds at the ADC.

Use the power plane layer to route the power supplies to the ADC.

The top and bottom layers route the analog and digital signals. Route the input signal as a matched differential pair throughout the signal chain to reduce differential noise coupling. Avoid crossing or adjacent placement of digital signals with the analog signals. This layout is especially true for high-frequency digital signals such as the clock input, and SPI signals, SCLK, and SDO/$\overline{\text{DRDY}}$. The pin placement of both ADC package options minimizes the need to cross digital and analog signals.

Place the voltage reference close to the ADC. Orient the reference such that the reference ground pin is close to the ADC REFN pin. Place the reference input bypass capacitors directly at the ADC pins. Use reference bypass capacitors for each ADC in multichannel systems and connect the reference ground pin to the ground plane (or to AVSS in some bipolar supply systems) at one point and route REFP and REFN as paired traces to each ADC.

9.4.2 Layout Example

図 9-7 is a layout example based on the circuit diagram of 図 9-1. The ADC is shown in the WQFN package option. A four-layer PCB is used, with the inner layers dedicated as ground and power planes. Cutouts are used on the plane layers under the amplifier input pins to reduce stray capacitance to increase amplifier phase margin. Thermal vias for the ADS127L11 and THS4551 WQFN package thermal pad are not used so that bypass capacitors can be placed on the bottom layer underneath the devices. Place the smaller of the parallel supply bypass capacitors closest to the device supply pins.

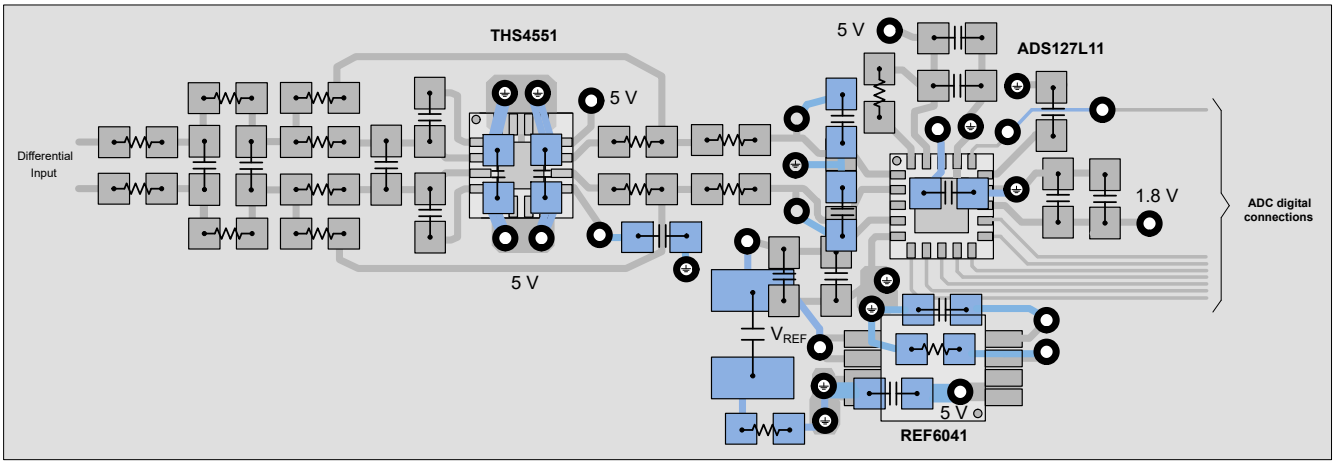

図 9-7. Layout Example of Typical Application Circuit

See the *QFN and SON PCB Attachment* application note for details of attaching the WQFN package to the printed circuit board.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *ADS127L11 in Simultaneous-Sampling Systems* application brief
- Texas Instruments, *ADS127L11 CRC Calculator*
- Texas Instruments, *IEPE Vibration Sensor Interface Reference Design for PLC Analog Input* design guide
- Texas Instruments, *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *REF60xx High-Precision Voltage Reference with Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications* application note
- Texas Instruments, *QFN and SON PCB Attachment* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS127L11IPWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IPWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IPWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IPWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IPWT	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IPWT.A	Active	Production	TSSOP (PW) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A127L11
ADS127L11IRUKR	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A27L11
ADS127L11IRUKR.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A27L11
ADS127L11IRUKRG4	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A27L11
ADS127L11IRUKRG4.A	Active	Production	WQFN (RUK) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A27L11
ADS127L11IRUKT	Active	Production	WQFN (RUK) | 20	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A27L11
ADS127L11IRUKT.A	Active	Production	WQFN (RUK) | 20	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	A27L11

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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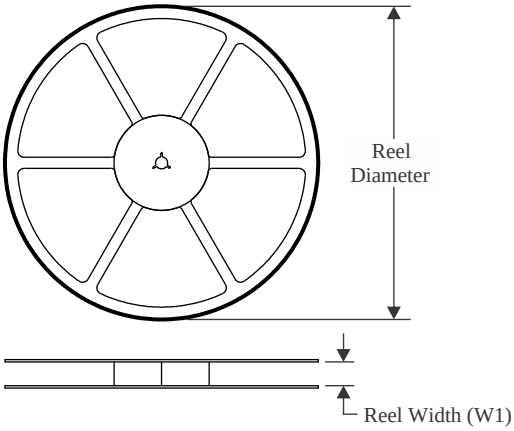
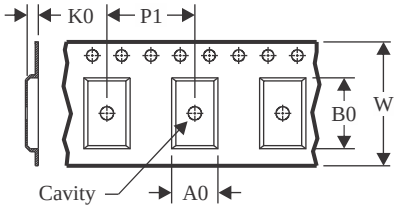
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

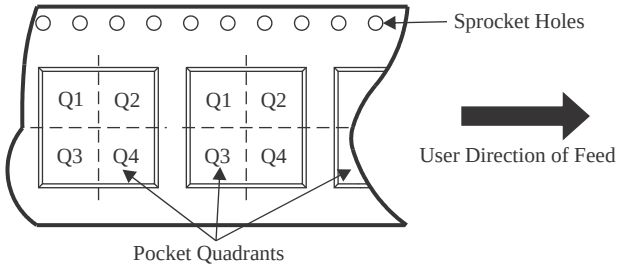


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

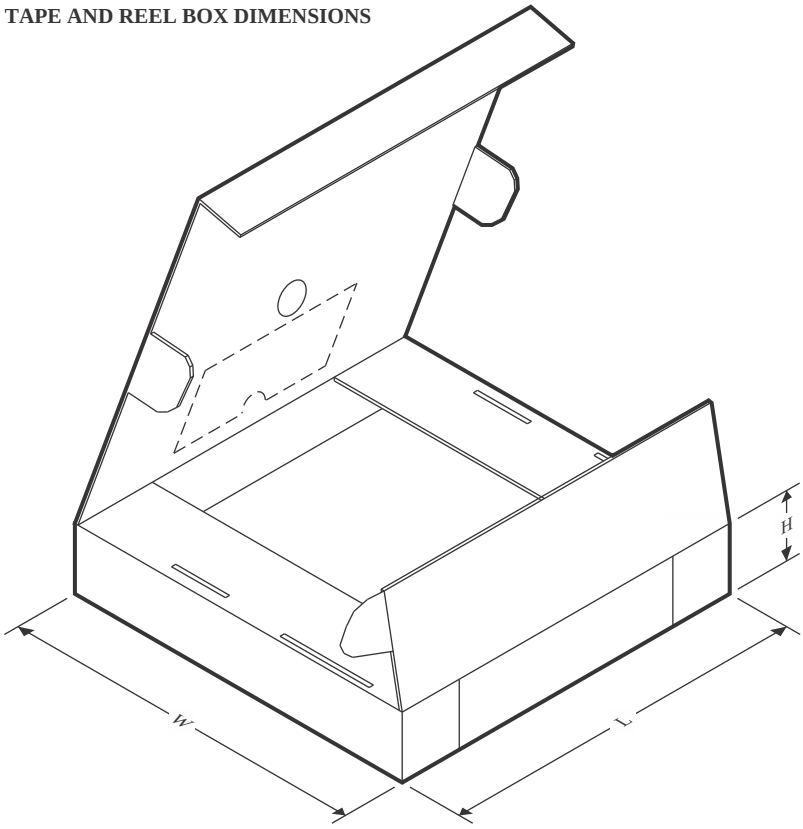
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS127L11IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
ADS127L11IPWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
ADS127L11IRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS127L11IRUKRG4	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS127L11IRUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

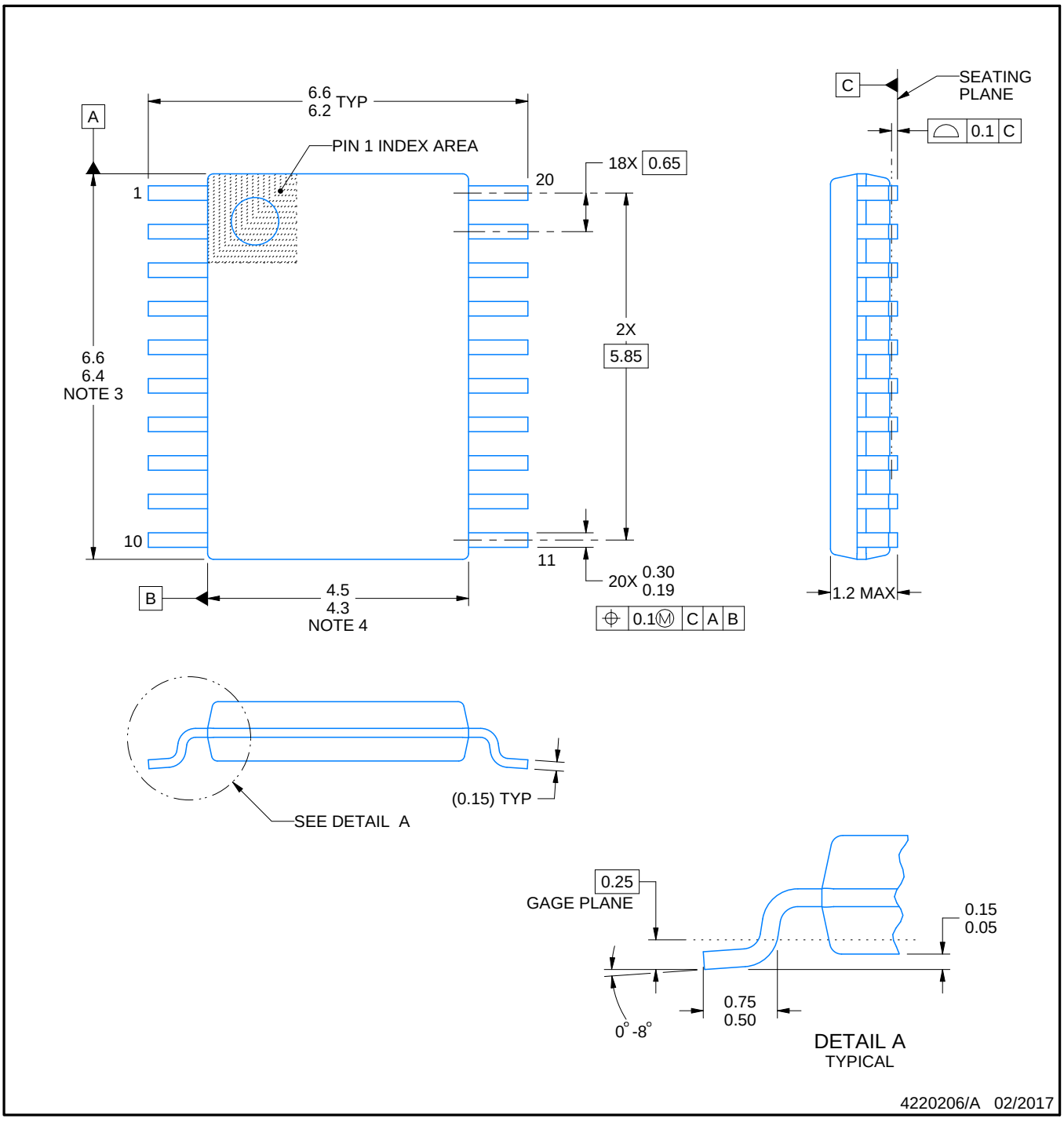
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS127L11IPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
ADS127L11IPWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
ADS127L11IRUKR	WQFN	RUK	20	3000	360.0	360.0	36.0
ADS127L11IRUKRG4	WQFN	RUK	20	3000	367.0	367.0	35.0
ADS127L11IRUKT	WQFN	RUK	20	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0020A

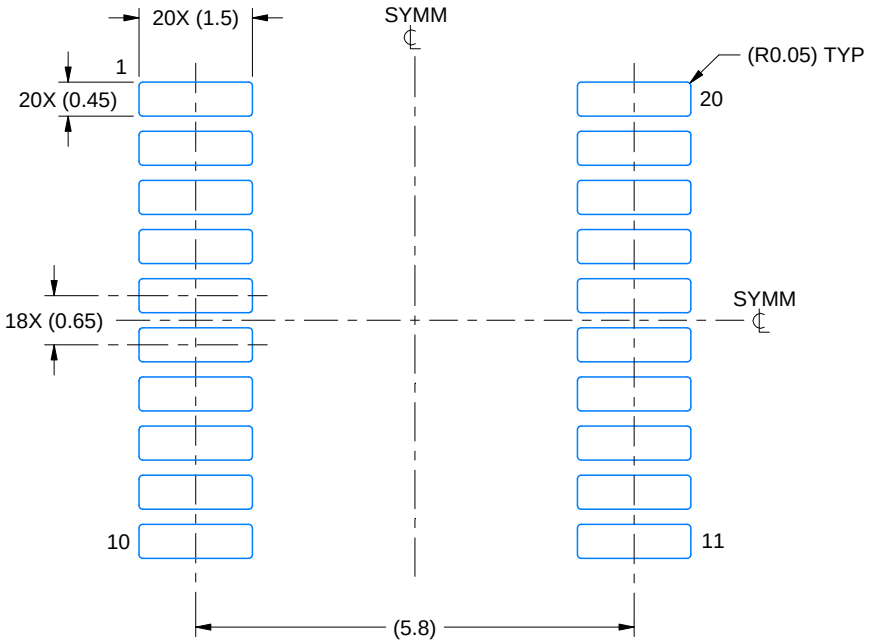
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

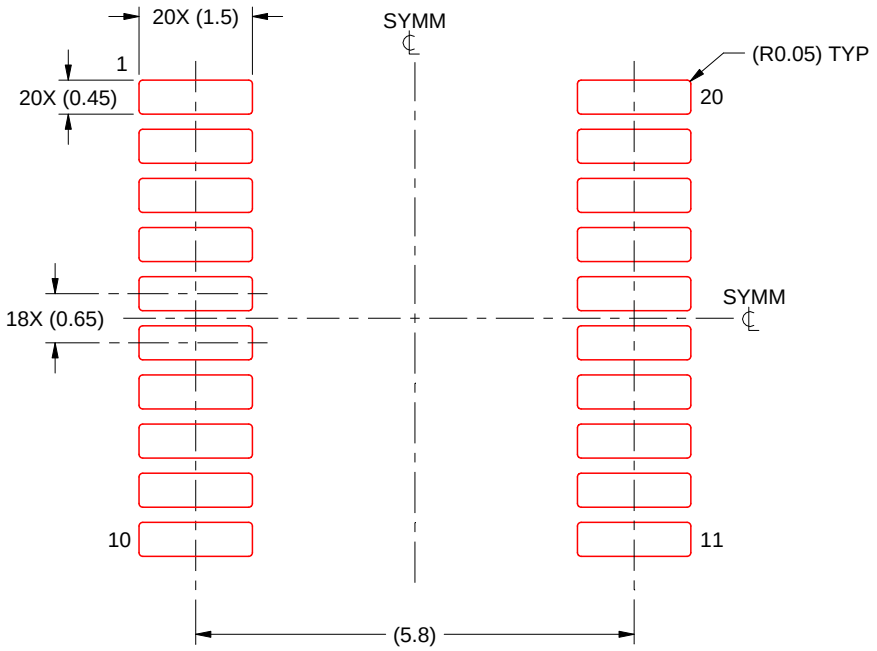
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

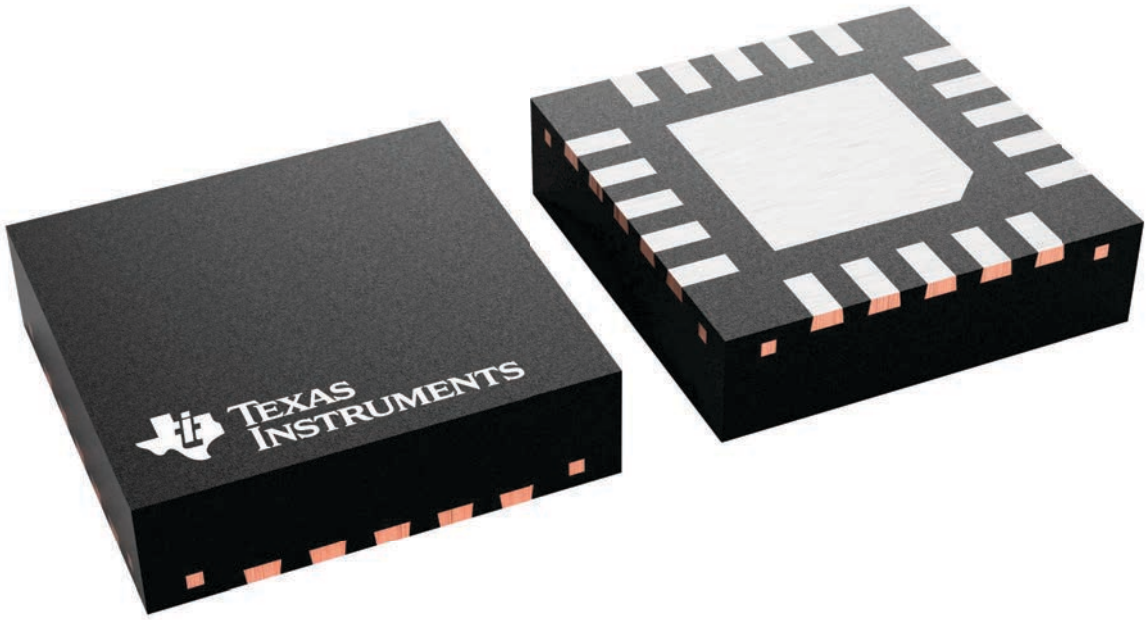
RUK 20

WQFN - 0.8 mm max height

3 x 3, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



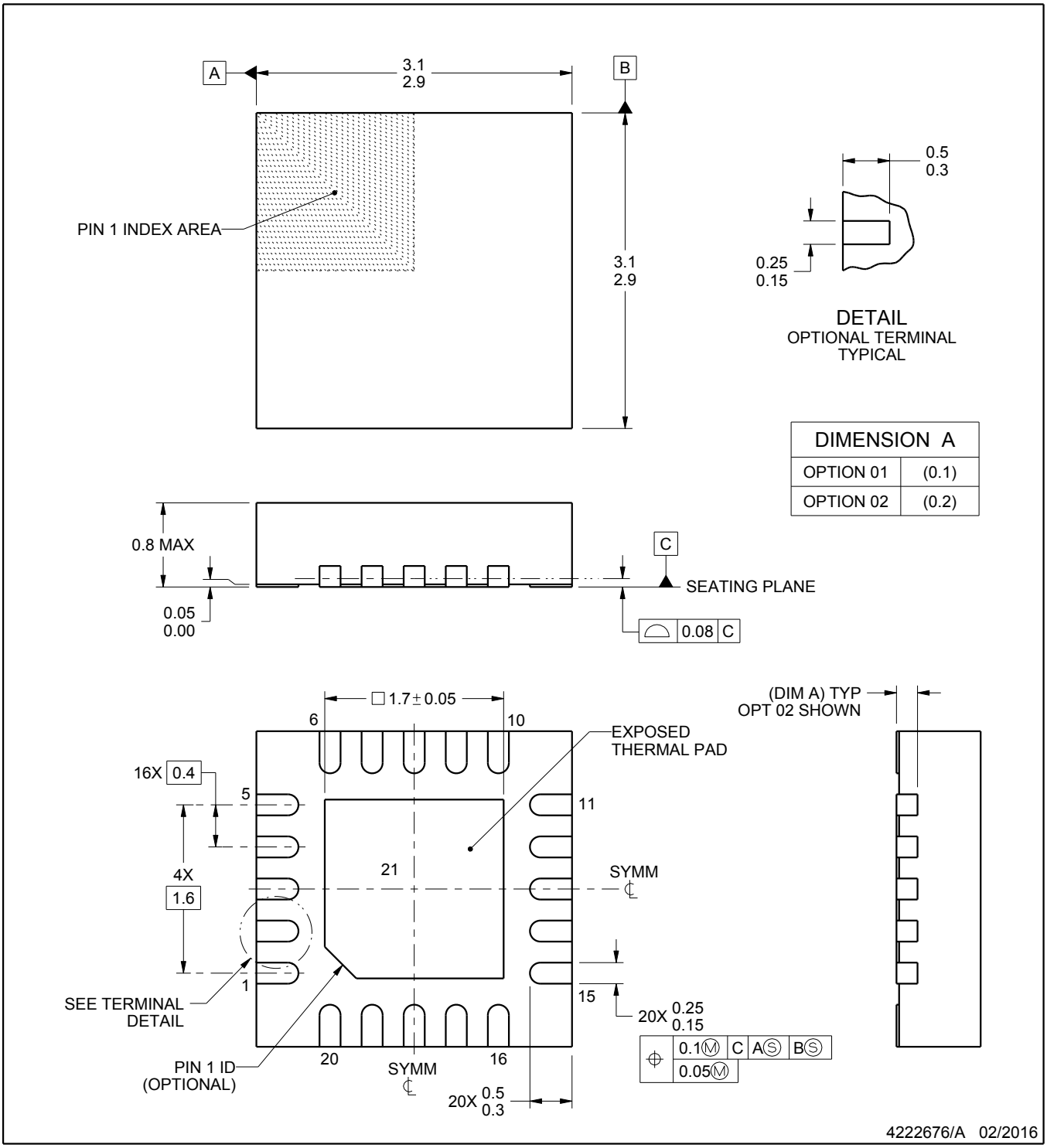
4229651/A

PACKAGE OUTLINE

RUK0020B

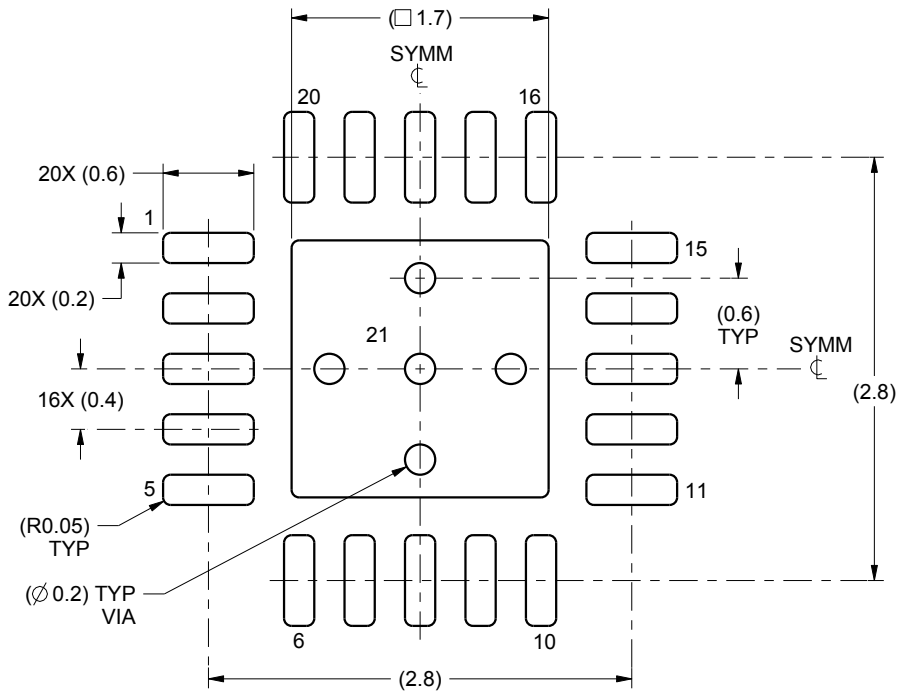
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

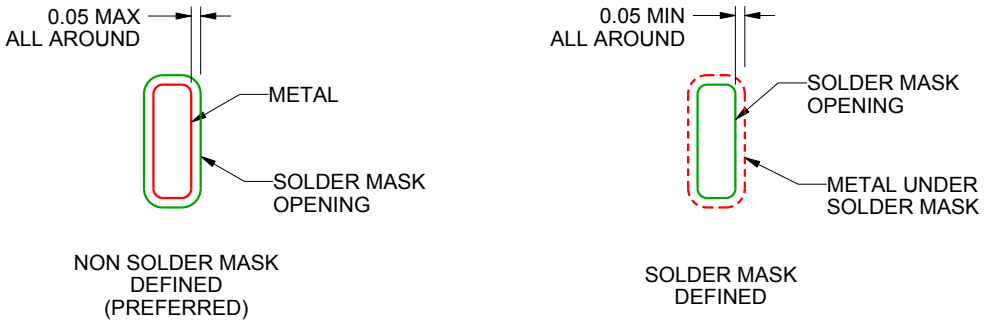


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

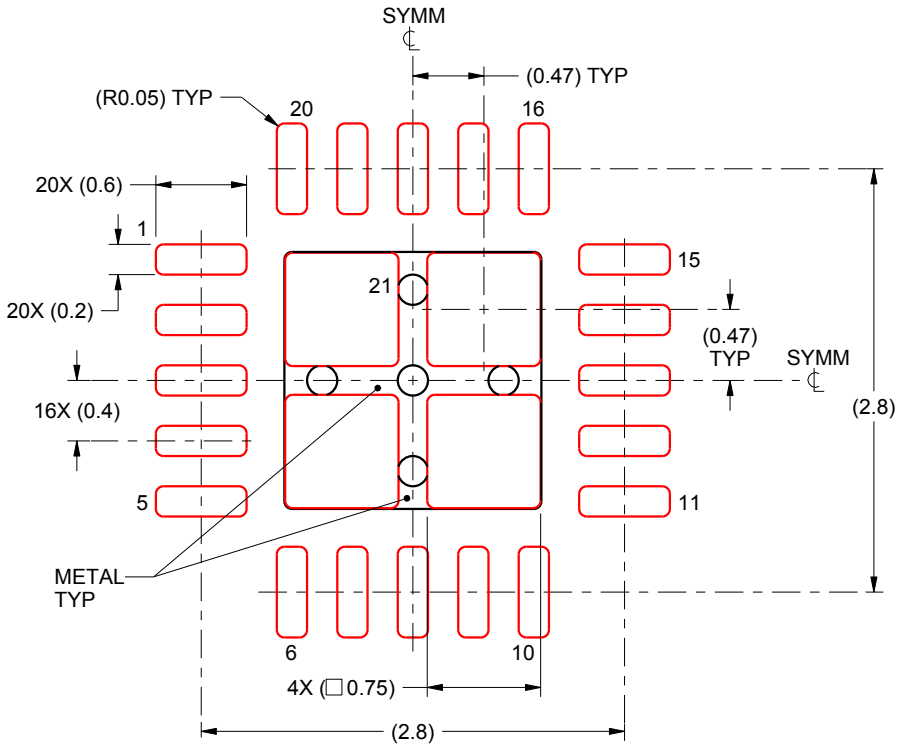


SOLDER MASK DETAILS

4222676/A 02/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222676/A 02/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月