ADS7138-Q1
JAJSJ11A – MAY 2020 – REVISED OCTOBER 2020

ADS7138-Q1 小型、8 チャネル、12 ビット ADC、I²C インターフェイス、GPIO、CRC 搭載

1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1：-40℃ ~ 125℃、T_A
- 小型のパッケージ
  - 3mm × 3mm WQFN
  - ウェッタブル・フランクによりハンダ接合部を目視検査可能
- 8 つのチャネルを次の任意の組み合わせに構成可能
  - 最大 8 つのアナログ入力、デジタル入力、またはデジタル出力
- GPIO による I/O の拡張
  - オープン・ドレイン、プッシュプル・デジタル出力
- 広い動作範囲：
  - AVDD：2.35V ~ 5.5V
  - DVDD：1.65V ~ 5.5V
  - 温度範囲：–40℃ ~ +125℃
- CRC を使用した読み取り / 書き込み動作：
  - データ読み取り / 書き込み時の CRC
  - 起動構成時の CRC
- I²C インターフェイス：
  - 最大 3.4MHz (高速モード)
  - 8 つの I²C アドレスを構成可能
- 平均化フィルタをプログラム可能：
  - 平均化のサンプル・サイズをプログラム可能
  - 内部変換による平均化
  - 平均出力の分解能：16 ビット
- 最大 3.2MSPS の速度のターボ・コンパレータ・モード

2 アプリケーション

- 処理機能なしのカメラ・モジュール
- 車載センター情報ディスプレイ
- 車載クラスタ・ディスプレイ

3 説明

ADS7138-Q1 は、使いやすい 8 チャネル、多重化、12 ビット、逐次比較型アナログ / デジタル・コンバータ (SAR ADC) です。8 つのチャネルは、アナログ入力、デジタル入力、デジタル出力のいずれかとして独立して構成可能です。このデバイスは、ADC 変換プロセス用の発振器を内蔵しています。

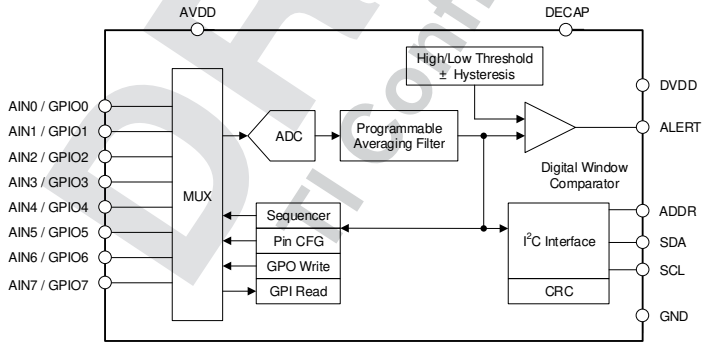
ADS7138-Q1 は I²C 互換のインターフェイスを使用して通信を行い、連続またはシングル・ショットの変換モードで動作します。ADS7138-Q1 は、プログラム可能な高および低スレッショルド、ヒステリシス、イベント・カウンタを備えたデジタル・ウィンドウ・コンパレータを使用して、チャネルごとのイベント・トリガ割り込みによるアナログ・ウォッチドッグ機能を実装しています。ADS7138-Q1 は、データの読み取り / 書き込み動作と起動構成のための巡回冗長性検査 (CRC) を内蔵しています。

製品情報 (1) (1 ページ)

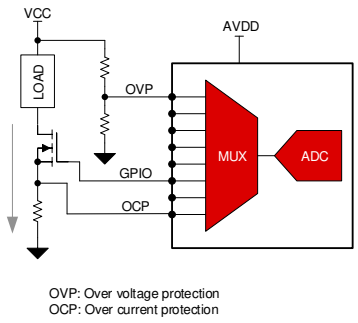
型番	パッケージ	本体サイズ (公称)
ADS7138-Q1	WQFN (16)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

Device Block Diagram



Example System Architecture



ADS7138-Q1 のブロック図とアプリケーション

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2020) to Revision A (October 2020)	Page
• ドキュメントのステータスを事前情報から量産データに変更	1

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5 Device Comparison Table

PART NUMBER	DESCRIPTION	CRC MODULE	ZERO-CROSSING-DETECT (ZCD) MODULE	ROOT-MEAN-SQUARE (RMS) MODULE
ADS7128	8-channel, 12-bit ADC with I^2C interface and GPIOs	Yes	Yes	Yes
ADS7138		Yes	No	No
ADS7138-Q1		Yes	No	No

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6 Pin Configuration and Functions

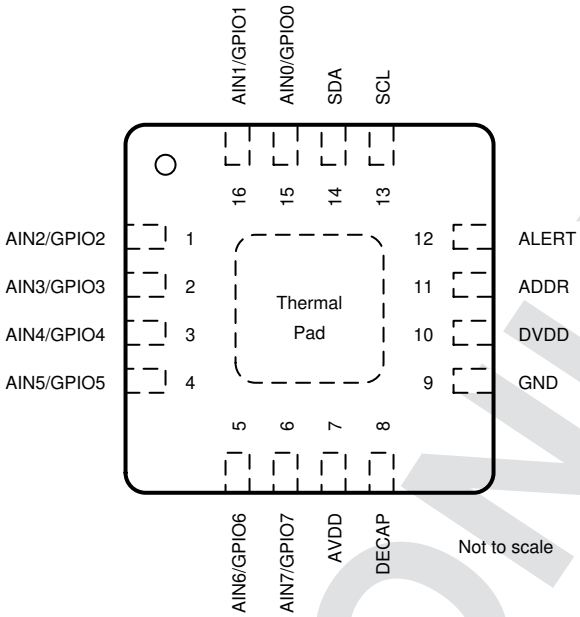


図 6-1. RTE Package, 16-Pin WQFN, Top View

表 6-1. Pin Functions

PIN		FUNCTION[1]	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; configurable as either an analog input (default) or a general-purpose input/output (GPIO).
AIN1/GPIO1	16	AI, DI, DO	Channel 1; configurable as either an analog input (default) or a GPIO.
AIN2/GPIO2	1	AI, DI, DO	Channel 2; configurable as either an analog input (default) or a GPIO.
AIN3/GPIO3	2	AI, DI, DO	Channel 3; configurable as either an analog input (default) or a GPIO.
AIN4/GPIO4	3	AI, DI, DO	Channel 4; configurable as either an analog input (default) or a GPIO.
AIN5/GPIO5	4	AI, DI, DO	Channel 5; configurable as either an analog input (default) or a GPIO.
AIN6/GPIO6	5	AI, DI, DO	Channel 6; configurable as either an analog input (default) or a GPIO.
AIN7/GPIO7	6	AI, DI, DO	Channel 7; configurable as either an analog input (default) or a GPIO.
ADDR	11	AI	Input for selecting the device I^2C address. Connect a resistor to this pin from DECAP pin or GND to select one of the eight addresses.
ALERT	12	Digital output	Open-drain (default) or push-pull output for the digital comparator.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND.
DECAP	8	Supply	Connect a1-µF decoupling capacitor between the DECAP and GND pins for the internal power supply.
DVDD	10	Supply	Digital I/O supply voltage; connect a 1-µF decoupling capacitor to GND.
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage.
SDA	14	DI, DO	Serial data input or output for the I^2C interface.
SCL	13	DI	Serial clock for the I^2C interface.
Thermal pad	—	Supply	Exposed thermal pad; connect to GND.

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Pin Functions

PIN		FUNCTION[1]	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; configurable as either an analog input (default) or a general-purpose input/output (GPIO).
AIN1/GPIO1	16	AI, DI, DO	Channel 1; configurable as either an analog input (default) or a GPIO.
AIN2/GPIO2	1	AI, DI, DO	Channel 2; configurable as either an analog input (default) or a GPIO.
AIN3/GPIO3	2	AI, DI, DO	Channel 3; configurable as either an analog input (default) or a GPIO.
AIN4/GPIO4	3	AI, DI, DO	Channel 4; configurable as either an analog input (default) or a GPIO.
AIN5/GPIO5	4	AI, DI, DO	Channel 5; configurable as either an analog input (default) or a GPIO.
AIN6/GPIO6	5	AI, DI, DO	Channel 6; configurable as either an analog input (default) or a GPIO.
AIN7/GPIO7	6	AI, DI, DO	Channel 7; configurable as either an analog input (default) or a GPIO.
ADDR	11	AI	Input for selecting the device I^2C address. Connect a resistor to this pin from DECAP pin or GND to select one of the eight addresses.
ALERT	12	Digital output	Open-drain (default) or push-pull output for the digital comparator.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND.
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SDA	14	DI, DO	Serial data input or output for the I^2C interface.
SCL	13	DI	Serial clock for the I^2C interface.
Thermal pad	—	Supply	Exposed thermal pad; connect to GND.

(1) AI = analog input, DI = digital input, and DO = digital output.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx/GPOx(3)	GND – 0.3	AVDD + 0.3	V
ADDR	GND – 0.3	2.1	V
Digital inputs	GND – 0.3	5.5	V
Current through any pin except supply pins, SCL, and SDA(2)	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pin current must be limited to 10mA or less.
(3) AINx/GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011; corner pins (1, 4, 5, 8, 9, 12, 13, 16)	±750	
		Charged-device model (CDM), per AEC Q100-011; all other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS						
FSR	Full-scale input range	AIN_X (1) - GND	0		AVDD	V
V_{IN}	Absolute input voltage	AIN_X - GND	–0.1		AVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	℃

(1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

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7.4 Thermal Information

THERMAL METRIC[1]		ADS7138-Q1	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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7.5 Electrical Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	Sampling capacitance			12		pF
DC PERFORMANCE						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity		–0.75	±0.2	0.75	LSB
INL	Integral nonlinearity		–1.5	±0.45	1.5	LSB
$V_{(OS)}$	Input offset error	Post offset calibration	–2	±0.4	2	LSB
	Input offset thermal drift	Post offset calibration		±1		ppm/°C
G_E	Gain error		–0.065	±0.025	0.065	%FSR
	Gain error thermal drift			±1		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f_{IN} = 2 kHz	70	72.8		dB
		AVDD = 3 V, f_{IN} = 2 kHz	69.8	72.4		
SNR	Signal-to-noise ratio	AVDD = 5 V, f_{IN} = 2 kHz	71.2	73		dB
		AVDD = 3 V, f_{IN} = 2 kHz	70.5	72.5		
THD	Total harmonic distortion	f_{IN} = 2 kHz		–85		dB
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		91		dB
	Crosstalk	100-kHz signal applied on any OFF channel and measured on ON the channel		–100		dB
DECAP Pin						
C_{DECAP}	Decoupling capacitor on DECAP pin		0.1	1	4.7	µF
	Voltage output on DECAP pin	C_{DECAP} = 1 µF		1.8		V
DIGITAL INPUT/OUTPUT (SCL, SDA)						
V_{IH}	Input high logic level	All I^2C modes	0.7 x DVDD		DVDD	V
V_{IL}	Input low logic level	All I^2C modes	–0.3		0.3 x DVDD	V
V_{OL}	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
I_{OL}	Low-level output current (sink)	V_{OL} = 0.4 V, standard and fast Mode			3	mA
		V_{OL} = 0.6 V, fast mode			6	
		V_{OL} = 0.4 V, fast mode plus			20	
GPIOs						
V_{IH}	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V_{IL}	Input low logic level		–0.3		0.3 x AVDD	V
	Input leakge current	GPIO configured as input		10	100	nA
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x AVDD		AVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x AVDD	V
I_{OH}	Output high source current	V_{OH} > 0.7 x AVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x AVDD			5	mA
DIGITAL OUTPUT (ALERT)						
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x DVDD		DVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x DVDD	V

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7.5 Electrical Characteristics (continued)

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OH}	Output high sink current	V_{OH} > 0.7 x DVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x DVDD			5	mA
POWER SUPPLY CURRENTS						
I_{AVDD}	Analog supply current	I^2C high-speed mode, AVDD = 5 V		130	210	µA
		I^2C fast mode plus, AVDD = 5 V		45	85	
		I^2C fast mode, AVDD = 5 V		25	46	
		I^2C standard mode, AVDD = 5 V		12	26	
		No conversion, AVDD = 5 V		7	20	

7.6 I^2C Timing Requirements

		MODE(2)				UNIT
		STANDARD, FAST, AND FAST MODE PLUS		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL clock frequency(1)		1		3.4	MHz
$t_{SU;STA}$	Setup time for a repeated START condition	260		160		ns
$t_{HD;STA}$	Hold time after repeated START condition. After this period, the first clock is generated.	260		160		ns
t_{LOW}	Low period of the SCL clock pin	500		160		ns
t_{HIGH}	High period for the SCL clock pin	260		60		ns
$t_{SU;DAT}$	Data in setup time	50		10		ns
$t_{HD;DAT}$	Data in hold time	0		0		ns
t_R	SCL rise time, standard mode		1000		1000	ns
	SCL rise time, fast mode		300		300	ns
	SCL rise time, fast mode plus		120		120	ns
	SCL rise time, high-speed mode		–		80	ns
t_F	SCL fall time, standard mode		300		300	ns
	SCL fall time, fast mode		300		300	ns
	SCL fall time, fast mode plus		120		120	ns
	SCL fall time, high-speed mode		–		80	ns
$t_{SU;STO}$	STOP condition hold time	260		60		ns
t_{BUF}	Bus free time before new transmission	500		300		ns

(1) Bus load (C_B) consideration; C_B ≤ 400 pF for f_{SCL} ≤ 1 MHz; C_B < 100 pF for f_{SCL} = 3.4 MHz.

(2) The device supports standard, full-speed, and fast modes by default on power-up. For selecting high-speed mode refer to the section on *Configuring the Device for High-Speed I2C Mode* .

7.7 Timing Requirements

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C ; typical values at T_A = 25°C.

		MIN	MAX	UNIT
t_{ACQ}	Acquisition time (CONV_MODE = 00b or 01b)	300		ns
	Acquisition time in turbo comparator mode (CONV_MODE = 10b)	90		

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7.8 I²C Switching Characteristics

		MODE				UNIT
		STANDARD, FAST, AND FAST MODE PLUS		HIGH-SPEED MODE		
		MIN	MAX	MIN	MAX	
t_F	Fall time for SDA		120		80	ns
$t_{VD;DATA}$	SCL low to SDA data out valid		450		200	ns
$t_{VD;DATA}$	SCL low to SDA data out valid		450		200	ns
$t_{VD;ACK}$	SCL low to SDA acknowledge time		450		200	ns
$t_{STRETCH}$	Clock stretch time (OSR[2:0] = 000b)		1400		1000	ns
t_{SP}	Noise supression time constant on SDA and SCL		50		10	ns

7.9 Switching Characteristics

at AVDD = 2.35 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C ; typical values at T_A = 25°C.

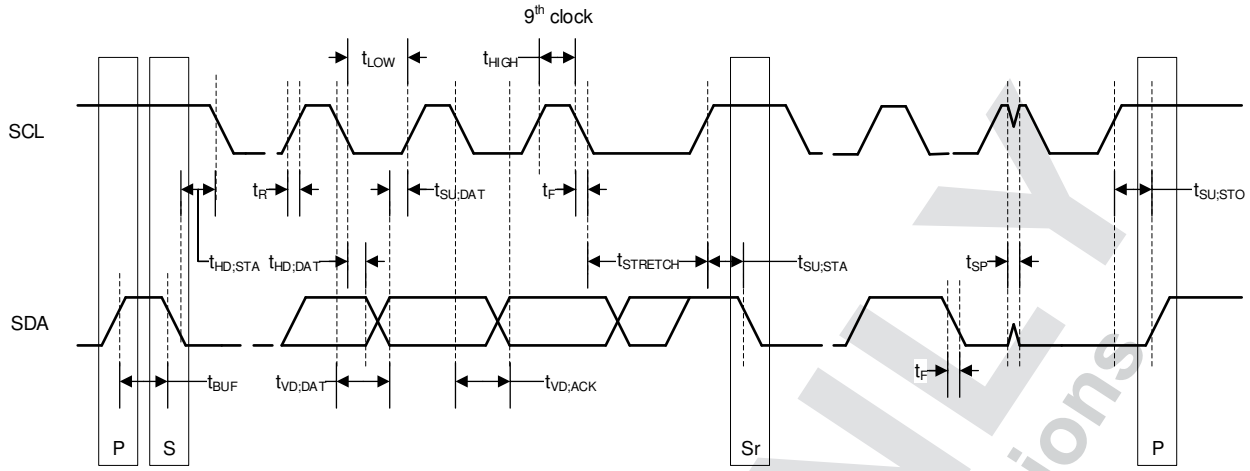
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time	*Manual Mode* and *Auto-Sequence Mode*		$t_{STRETCH}$	ns
		Autonomous Mode		600	
	ADC comparison time in turbo comparator mode	*Turbo Comparator Mode*		192	
RESET AND ALERT					
t_{PU}	Power-up time for device	AVDD ≥ 2.35 V		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete(1)			5	ms
t_{ALERT_HI}	ALERT high period	ALERT_LOGIC[1:0] = 1x	50	150	ns
t_{ALERT_LO}	ALERT low period	ALERT_LOGIC[1:0] = 1x	50	150	ns

(1) RST bit is automatically reset to 0b after t_{RST}.

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7.10 Timing Diagram



NOTE: S = Start, Sr = Repeated Start, and P = Stop.

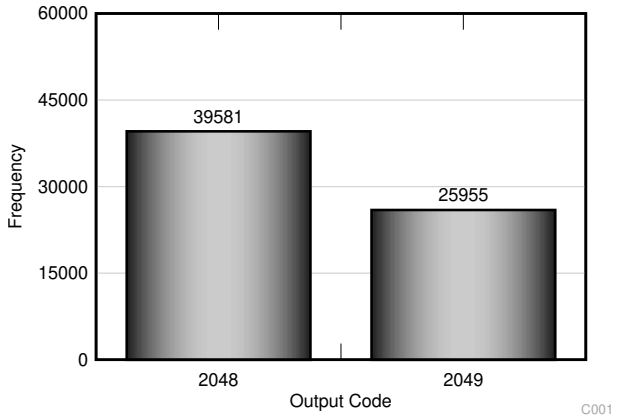
A. S = start, Sr = repeated start, and P = stop.

図 7-1. I²C Timing Diagram

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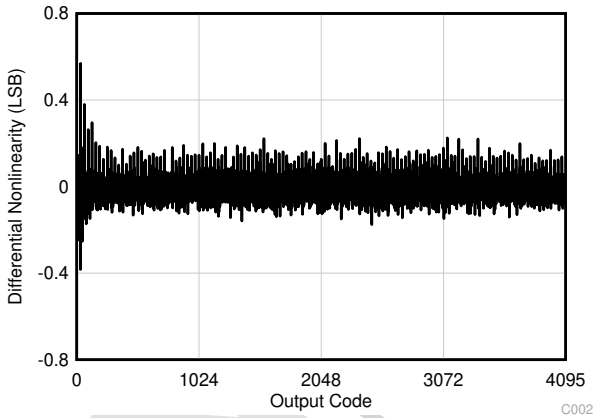
7.11 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)



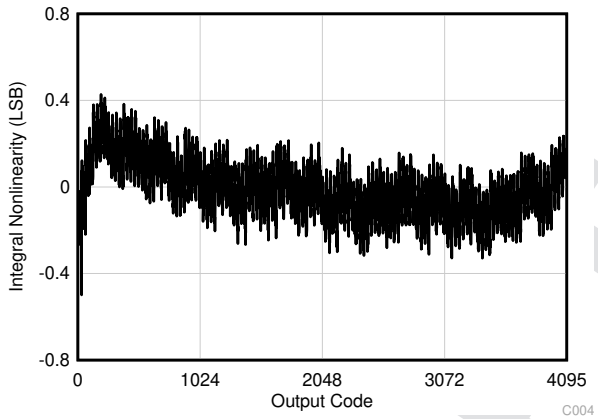
Standard deviation = 0.49 LSB

図 7-2. DC Input Histogram



Typical DNL = ±0.2 LSB

図 7-3. Typical DNL



Typical INL = ±0.5 LSB

図 7-4. Typical INL

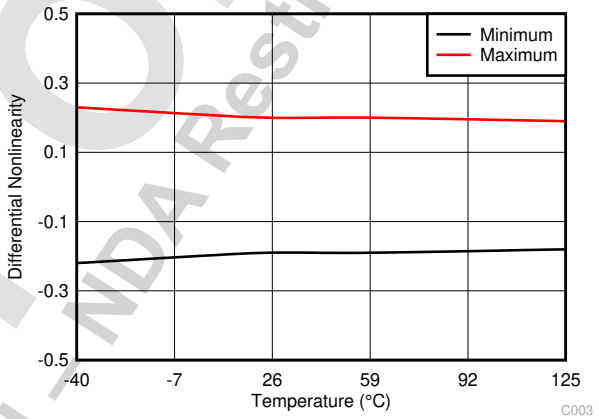


図 7-5. DNL vs Temperature

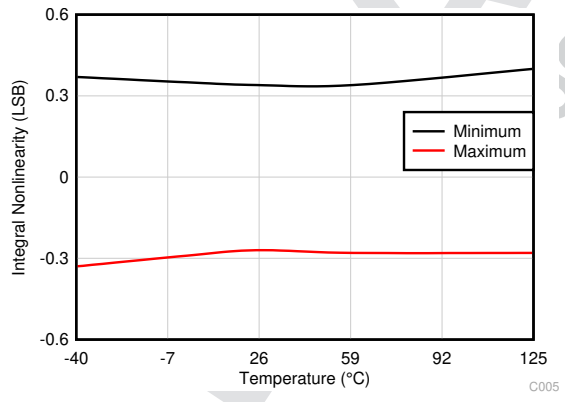


図 7-6. INL vs Temperature

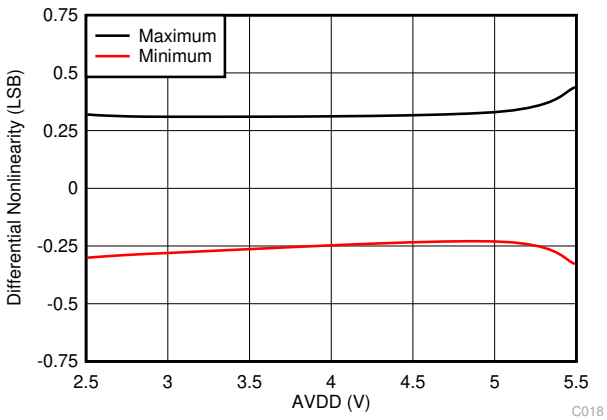


図 7-7. DNL vs AVDD

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7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

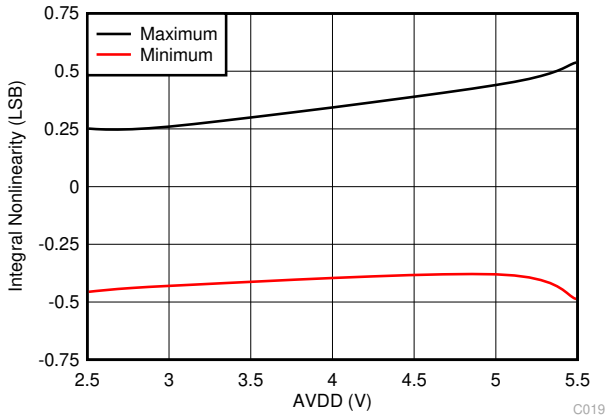


図 7-8. INL vs AVDD

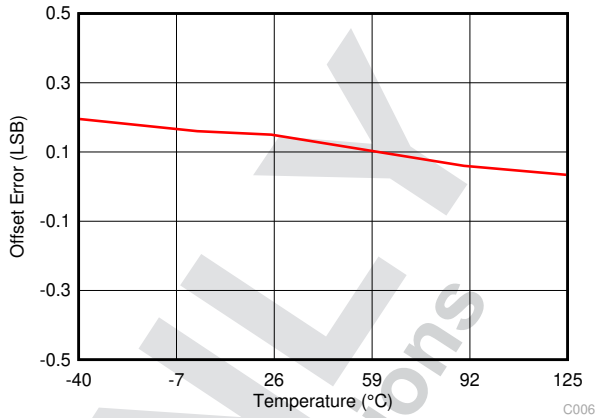


図 7-9. Offset Error vs Temperature

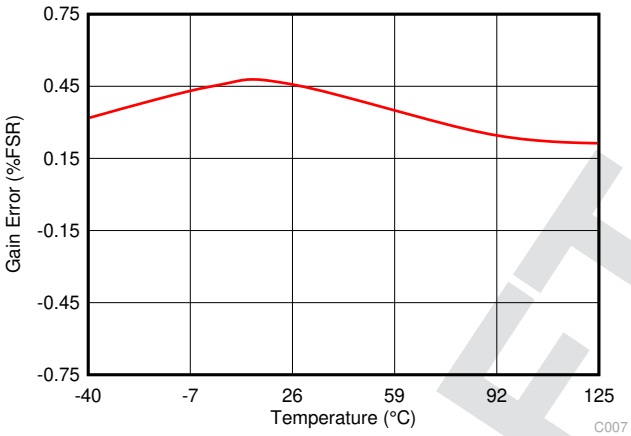


図 7-10. Gain Error vs Temperature

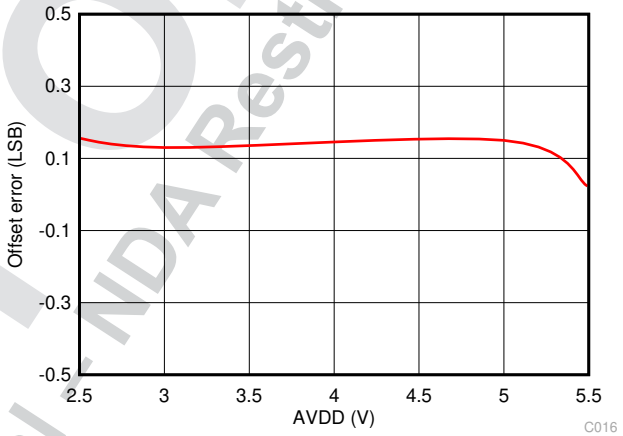


図 7-11. Offset Error vs AVDD

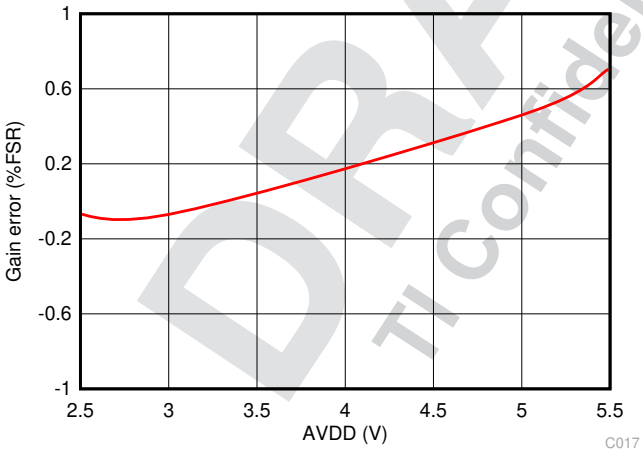
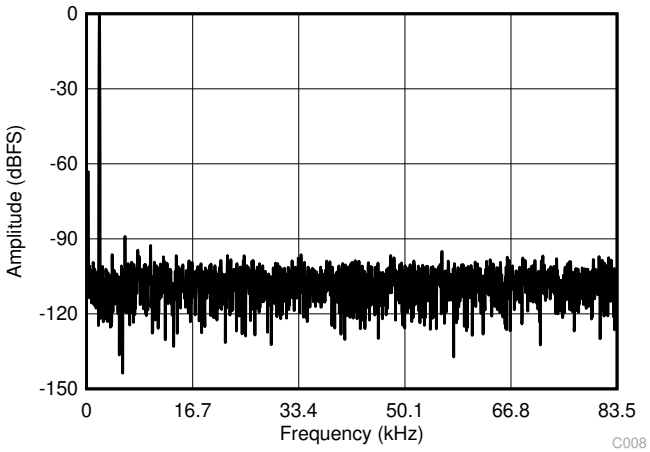


図 7-12. Gain Error vs AVDD



f_{IN} = 2 kHz, SNR = 73.2 dB, THD = 92.3 dB

図 7-13. Typical FFT

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7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

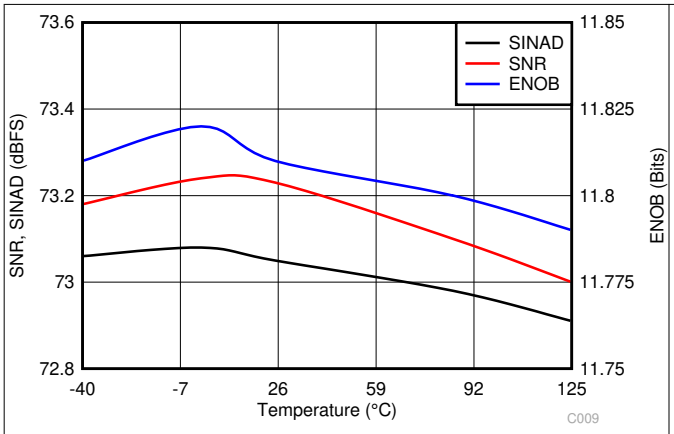


図 7-14. Noise Performance vs Temperature

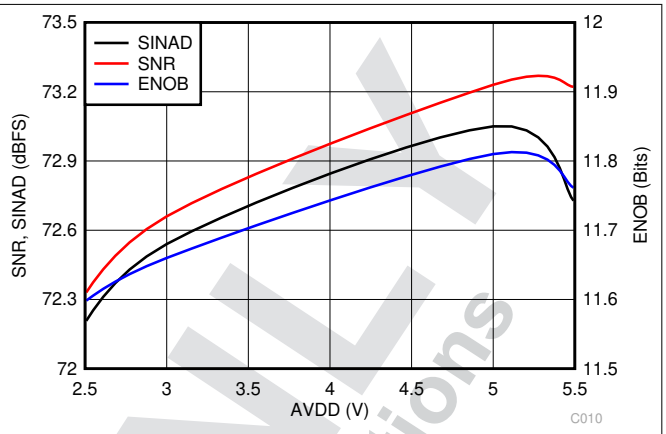


図 7-15. Noise Performance vs AVDD

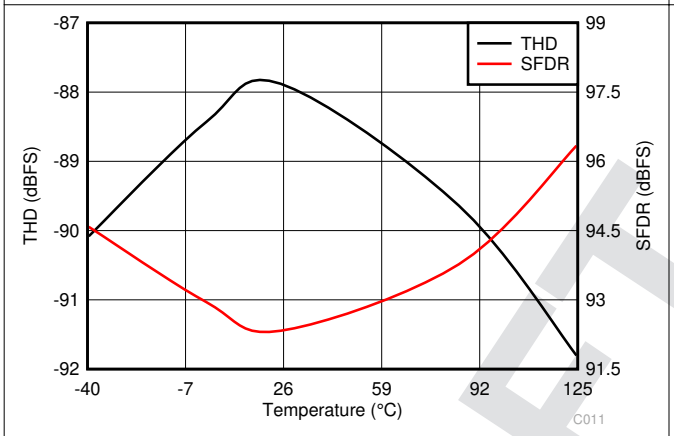


図 7-16. Distortion Performance vs Temperature

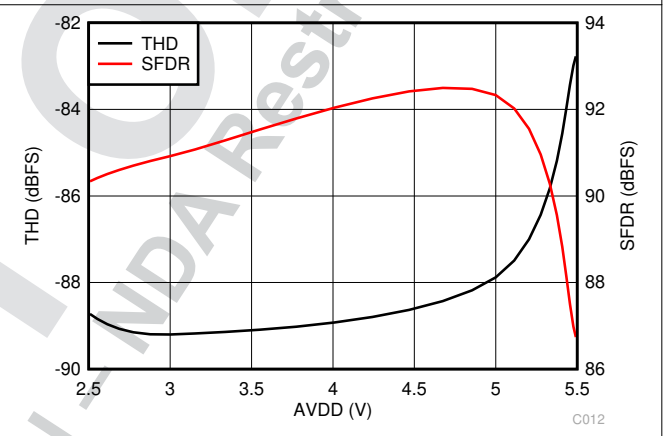


図 7-17. Distortion Performance vs AVDD

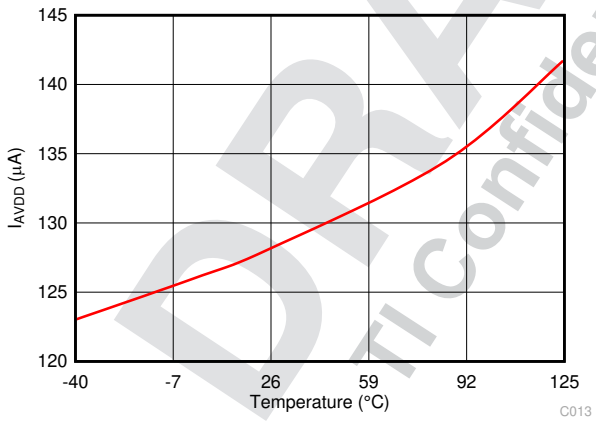


図 7-18. Analog Supply Current vs Temperature

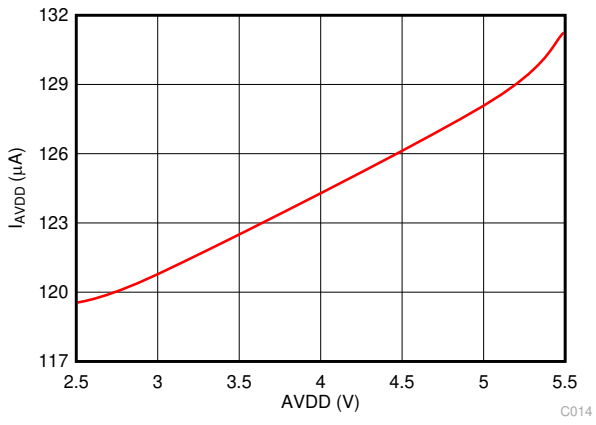


図 7-19. Analog Supply Current vs AVDD

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7.11 Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3.3 V, and maximum throughput (unless otherwise noted)

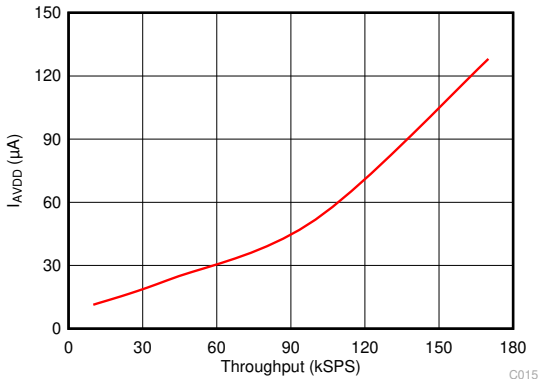


図 7-20. Analog Supply Current vs Throughput

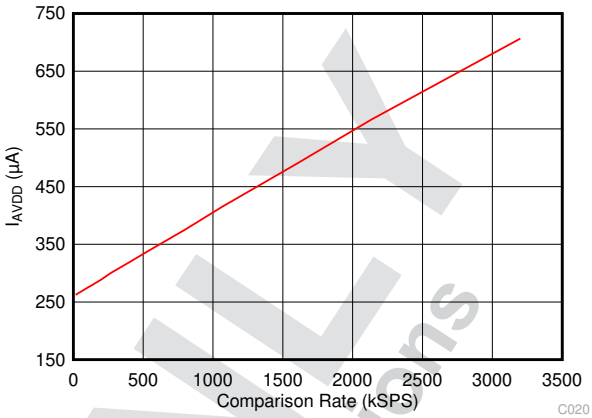


図 7-21. Analog Supply Current vs Comparison Rate (OSC_SEL = 0) in Turbo Comparator Mode

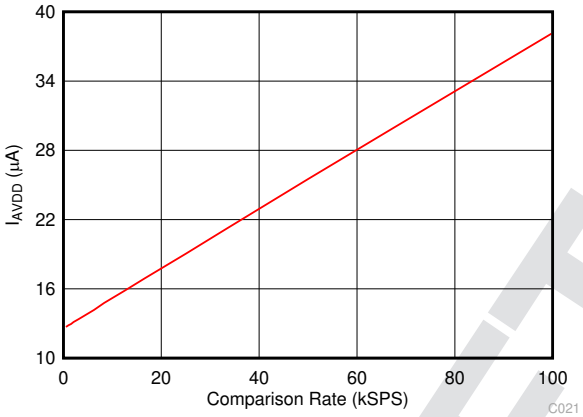


図 7-22. Analog Supply Current vs Comparison Rate (OSC_SEL = 1) in Turbo Comparator Mode

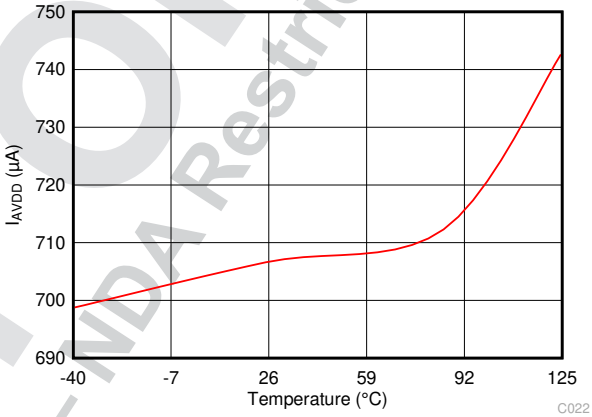


図 7-23. Analog Supply Current vs Temperature (OSC_SEL = 0, CLK_DIV = 0) in Turbo Comparator Mode

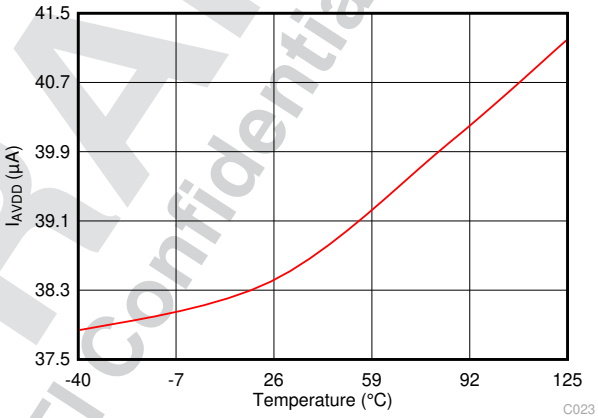


図 7-24. Analog Supply Current vs Temperature (OSC_SEL = 1, CLK_DIV = 0) in Turbo Comparator Mode

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8 Detailed Description

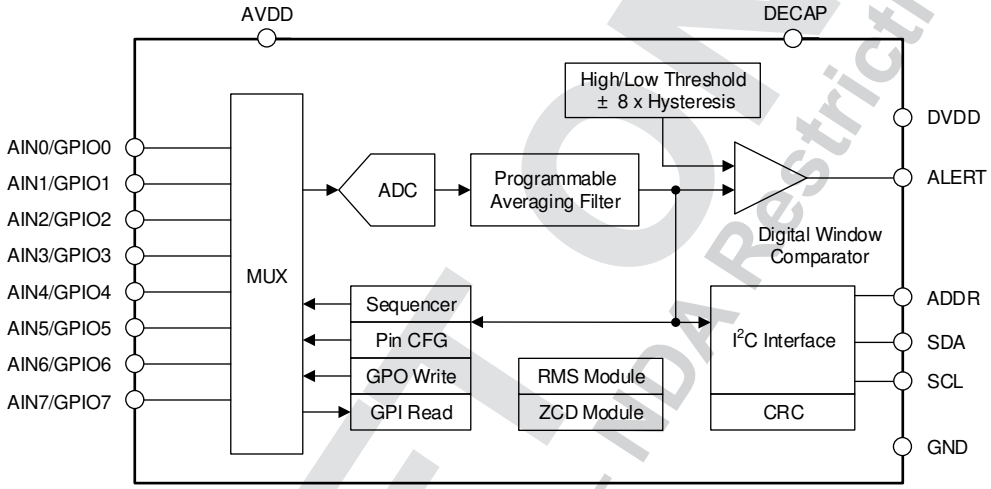
8.1 Overview

The ADS7138-Q1 is a small, eight-channel, multiplexed, 12-bit, analog-to-digital converter (ADC) with an I^2C-compatible serial interface. The eight channels of the ADS7138-Q1 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device includes a digital window comparator with a dedicated ALERT pin that can be used to alert the host when a programmed high or low threshold is crossed on any input channel. The device uses an internal oscillator for conversion. The ADC can be used in manual mode for reading ADC data over the I^2C interface or in autonomous and turbo comparator modes for monitoring the analog inputs without an active I^2C interface.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution.

The I^2C serial interface supports standard-mode, fast-mode, fast-mode plus, and high-speed mode. The device also features an 8-bit cyclic redundancy check (CRC) for the serial communication interface.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). As shown in 図 8-1 every AINx/GPIOx channel has ESD protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

図 8-1 shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with the resistor (R_{SW}, typically 150 Ω), and the sampling capacitor (C_{SH}).

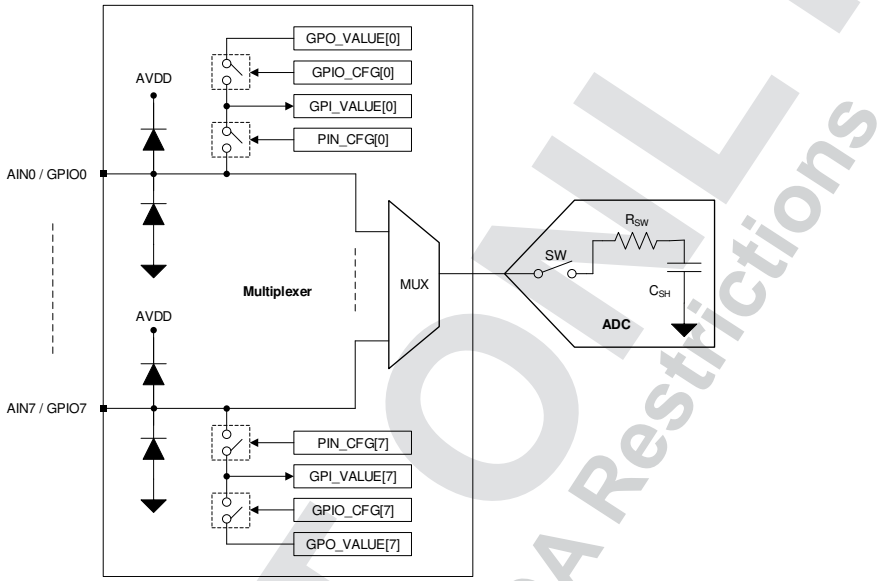


図 8-1. Analog Inputs, GPIOs, and ADC Connections

The SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor during acquisition time. The switch SW is opened to disconnect the sampling capacitor on the ninth falling edge of SCL.

The multiplexer channels can be configured as GPIOs using the PIN_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO_CFG register. The logic level on all device channels can be read from the GPI_VALUE register. The digital outputs can be configured by writing to the GPO_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO_DRIVE_CFG register.

8.3.2 Reference

The device uses the analog supply voltage (AVDD) as the reference for the analog-to-digital conversion process. TI recommends connecting a 1-µF, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

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8.3.3 ADC Transfer Function

The ADC output is in straight binary format. 式 1 computes the ADC resolution:

$$1\ LSB = V_{REF} / 2^N \quad (1)$$

where:

- V_{REF} = AVDD
- N = 12

図 8-2 and 表 8-1 detail the transfer characteristics for the device.

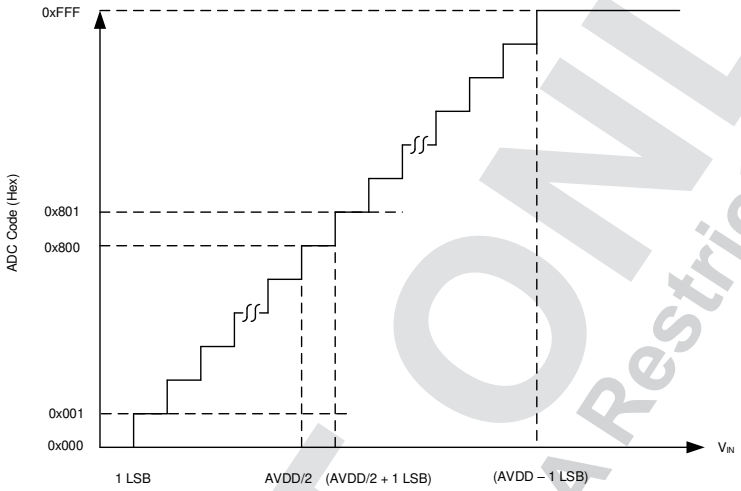


図 8-2. Ideal Transfer Characteristics

表 8-1. Transfer Characteristics

INPUT VOLTAGE	CODE	IDEAL OUTPUT CODE
≤1 LSB	Zero	000
1 LSB to 2 LSBs	Zero + 1	001
(AVDD / 2) to (AVDD / 2) + 1 LSB	Mid-scale code	800
(AVDD / 2) + 1 LSB to (AVDD / 2) + 2 LSB	Mid- scale code + 1	801
≥ AVDD – 1 LSB	Full-scale code	FFF

8.3.4 ADC Offset Calibration

The variation in the ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

Multiplexer sequencing must be stopped (SEQ_START = 0b) before initiating offset calibration.

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8.3.5 I²C Address Selector

The I²C address for the device is determined by connecting external resistors on the ADDR pin. The device address is determined at power-up based on the resistor values. The device retains this address until the next power-up event, until the next device reset, or until the device receives a command to program its own address . 図 8-3 shows a connection diagram for the ADDR pin and 表 8-2 lists the resistor values for selecting different addresses of the device.

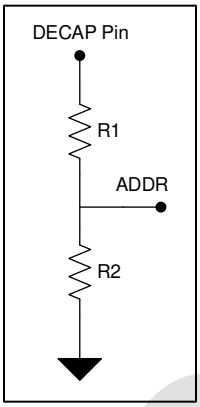


図 8-3. External Resistor Connection Diagram for the ADDR Pin

表 8-2. I²C Address Selection

RESISTORS		ADDRESS
R1(2)	R2(2)	
0 Ω	DNP(1)	001 0111b (17h)
11 kΩ	DNP	001 0110b (16h)
33 kΩ	DNP	001 0101b (15h)
100 kΩ	DNP	001 0100b (14h)
DNP	0 Ω or DNP	001 0000b (10h)
DNP	11 kΩ	001 0001b (11h)
DNP	33 kΩ	001 0010b (12h)
DNP	100 kΩ	001 0011b (13h)

(1) DNP = Do not populate.
(2) Tolerance for R1, R2 ≤ ±5%.

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8.3.6 Oscillator and Timing Control

The device uses an internal oscillator for conversions. The host initiates the first conversion and all subsequent conversions are generated internally by the device when using the averaging module. However, in the autonomous mode of operation, the start of the conversion signal is generated by the device. As described in 表 8-3, the sampling rate can be controlled by the OSC_SEL and CLK_DIV register fields when the device initiates conversions internally.

The conversion time of the device, given by t_{CONV} in the *Switching Characteristics* table, is independent of the OSC_SEL and CLK_DIV configuration.

表 8-3. Configuring Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE_OSR} (kSPS)	CYCLE TIME, t_{CYCLE_OSR} (µs)	SAMPLING FREQUENCY, f_{CYCLE_OSR} (kSPS)	CYCLE TIME, t_{CYCLE_OSR} (µs)
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072
1110b	7.8	128	0.24	4096
1111b	5.2	192	0.16	6144

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The comparison time in the *turbo comparator mode* can be controlled by the OSC_SEL and CLK_DIV register fields, as shown in 表 8-4.

表 8-4. Configuring Comparison Rate for Turbo Comparator Mode

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	COMPARISON RATE, $f_{COMPARISON}$ (kSPS)	CYCLE TIME, t_{CYCLE_COMP} (µs)	COMPARISON RATE, $f_{COMPARISON}$ (kSPS)	CYCLE TIME, t_{CYCLE_COMP} (µs)
0000b	3200	0.3125	100	10
0001b	2133.3	0.46875	66.7	15
0010b	1600	0.625	50	20
0011b	1066.7	0.9375	33.3	30
0100b	800	1.25	25	40
0101b	533.3	1.875	16.67	60
0110b	400	2.5	12.5	80
0111b	266.7	3.75	8.33	120
1000b	200	5	6.25	160
1001b	133.3	7.5	4.17	240
1010b	100	10	3.13	320
1011b	66.7	15	2.08	480
1100b	50	20	1.56	640
1101b	33.3	30	1.04	960
1110b	25	40	0.78	1280
1111b	16.67	60	0.52	1920

8.3.7 General-Purpose I/Os (GPIOs)

The eight channels of the ADS7138-Q1 can be independently configured as analog inputs, digital inputs, or digital outputs. The device channels, as described in 表 8-5, can be configured as analog inputs or GPIOs using the PIN_CFG and GPIO_CFG registers.

表 8-5. Configuring Channels as Analog Inputs or GPIOs

PIN_CFG[7:0]	GPIO_CFG[7:0]	GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x	x	Analog input (default)
1	0	x	Digital input
1	1	0	Digital output; open-drain driver
1	1	1	Digital output; push-pull driver

Digital outputs can be configured to logic 1 or 0 by writing to the GPO_VALUE register. Digital outputs can also be updated in response to event flags set by the digital window comparator (see the *Triggering Digital Outputs With a Digital Window Comparator* section for more details). Reading the GPI_VALUE register returns the logic level for all channels configured as analog inputs, digital inputs, and digital outputs.

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8.3.8 Programmable Averaging Filter

The ADS7138-Q1 features a built-in oversampling (OSR) module that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register. The averaging filter configuration is common to all analog input channels. As shown in 図 8-4, the averaging filter module output is 16 bits long. Only the first conversion for the selected analog input channel must be initiated by the host. Any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged; see the *Oscillator and Timing Control* section. The 16-bit result can be read out after the averaging operation completes. For more information about programmable averaging filters and performance results, see the *Resolution-Boosting ADS7138 Using Programmable Averaging Filter* appliction report.

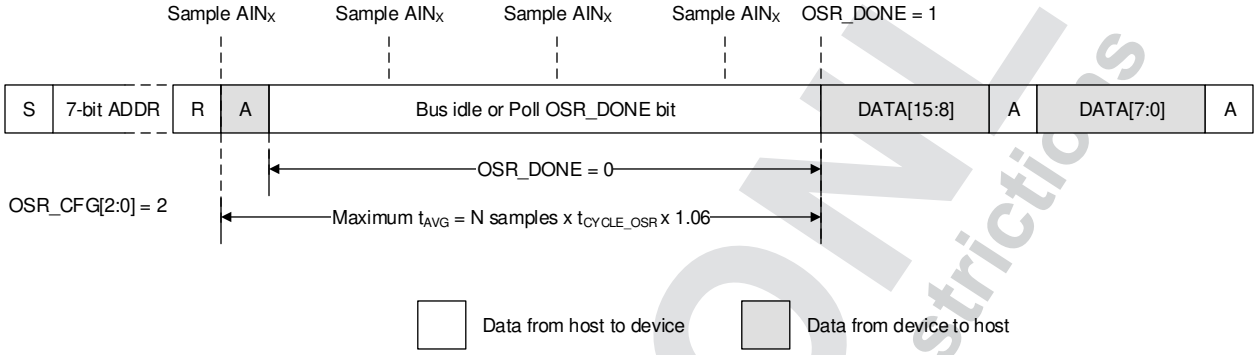


図 8-4. Averaging Example

As shown in 図 8-4, SCL is stretched by the device after the start of conversions until the averaging operation is complete.

If SCL stretching is not required during averaging, enable the statistics registers by setting STATS_EN to 1b and initiate conversions by writing 1b to the CNVST bit. The OSR_DONE bit in the SYSTEM_STATUS register can be polled to check the averaging completion status. When using the CNVST bit to initiate conversion, the result can be read in the RECENT_CHx_LSB and RECENT_CHx_MSB registers.

In the autonomous mode of operation, samples from the analog input channels that are enabled in the AUTO_SEQ_CH_SEL register are averaged sequentially; see the *Autonomous Mode* section. The digital window comparator compares the top 12 bits of the 16-bit average result with the thresholds.

式 2 provides the LSB value of the 16-bit average result.

$$1\ LSB = \frac{AVDD}{2^{16}} \tag{2}$$

8.3.9 CRC on Data Interface

The cyclic redundancy check (CRC) is an error checking code that detects errors in communication between the device and the host. The CRC module is optional and can be enabled by the CRC_EN bit in the GENERAL_CFG register.

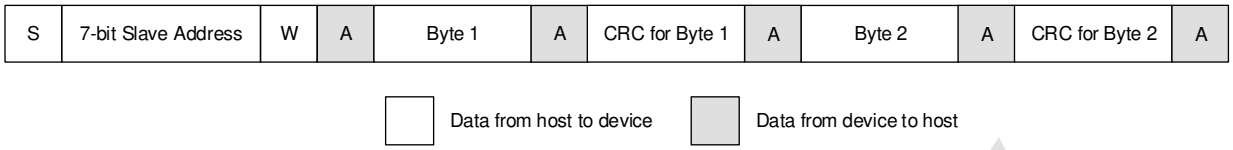
The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-CCITT: $X^8 + X^2 + X + 1$. The nine binary polynomial coefficients are 100000111. The CRC calculation is preset with 0 data values.

8.3.9.1 Input CRC (From Host To Device)

The host must compute the appropriate 8-bit CRC corresponding to the 8-bit I^2C data (see 図 8-5). The ADC also computes the expected 8-bit CRC corresponding to the 8-bit data received from the host and compares the calculated CRC code to the CRC received from the host. The host must not send a CRC byte corresponding to the I^2C frame containing the device address.

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NOTE: S = Start, Sr = Repeated Start, and P = Stop.

図 8-5. I²C Write With a CRC

If a CRC error is detected by the device, the command does not execute, and the CRCERR_IN flag is set to 1b. The ADC conversion data read and register read, with a valid CRC from the host, are still supported. The error condition can be detected, as listed in 表 8-6, by either status flags or by a register read. Further register writes to the device are blocked until the CRCERR_IN flag is cleared to 0b. Register write operations, with a valid CRC from the host, to the SYSTEM_STATUS and GENERAL_CFG registers are still supported.

The device can be configured to set all channels to analog inputs on detecting a CRC error by setting the CH_RST bit to 1b. This setting ensures channels configured as digital outputs are not driven by the device when a CRC error is detected. All channels are reset as per the configuration in the PIN_CFG and GPIO_CFG registers when the CRCERR_IN flag is cleared.

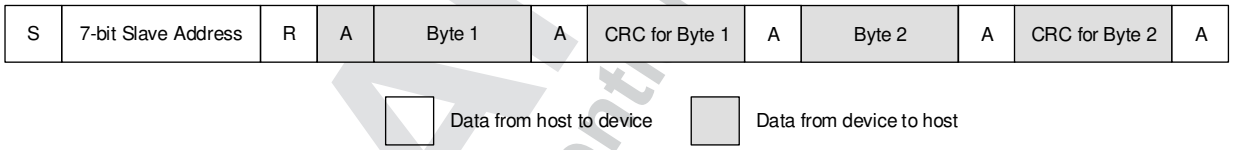
The device can be configured to abort further conversions in autonomous and turbo comparator modes (see the *Autonomous Mode* and *Turbo Comparator Mode* sections), on detecting a CRC error, by setting CONV_ON_ERR = 1b.

表 8-6. Configuring Notifications When a CRC Error is Detected

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
ALERT	ALERT_CRCIN = 1b	ALERT pin is asserted if a CRC error is detected.
Status flags	APPEND_STATUS = 10b	See the *Status Flags* section for details.
Register read	—	Read the CRCERR_IN bit to check if a CRC error was detected.

8.3.9.2 Output CRC (From Device to Host)

As shown in 図 8-6, the device sends an 8-bit CRC corresponding to every byte sent by the device over the I²C interface.



NOTE: S = Start, Sr = Repeated Start, and P = Stop.

図 8-6. I²C Read With CRC

8.3.10 Output Data Format

図 8-7 illustrates various I²C frames for reading data.

- Read the ADC conversion result: Two 8-bit I²C packets are required (frame A).
- Read the averaged conversion result: Two 8-bit I²C packets are required (frame B).
- Read data with the channel ID or status flags appended: The 4-bit channel ID or status flags can be appended to the 12-bit ADC result by configuring the APPEND_STATUS field in the GENERAL_CFG register. The status flags can be used to detect if a CRC error is detected and if an alert condition is detected by the digital window comparator. When the channel ID or status flags are appended to the 12-bit ADC data, two I²C packets are required (frame C). If the channel ID or status flags are appended to the 16-bit average result, three I²C frames are required (frame D).

When the CRC module is enabled, the device sends an 8-bit CRC for every 8-bit data byte sent over the I²C interface; see the *Output CRC (From Device to Host)* section for more details.

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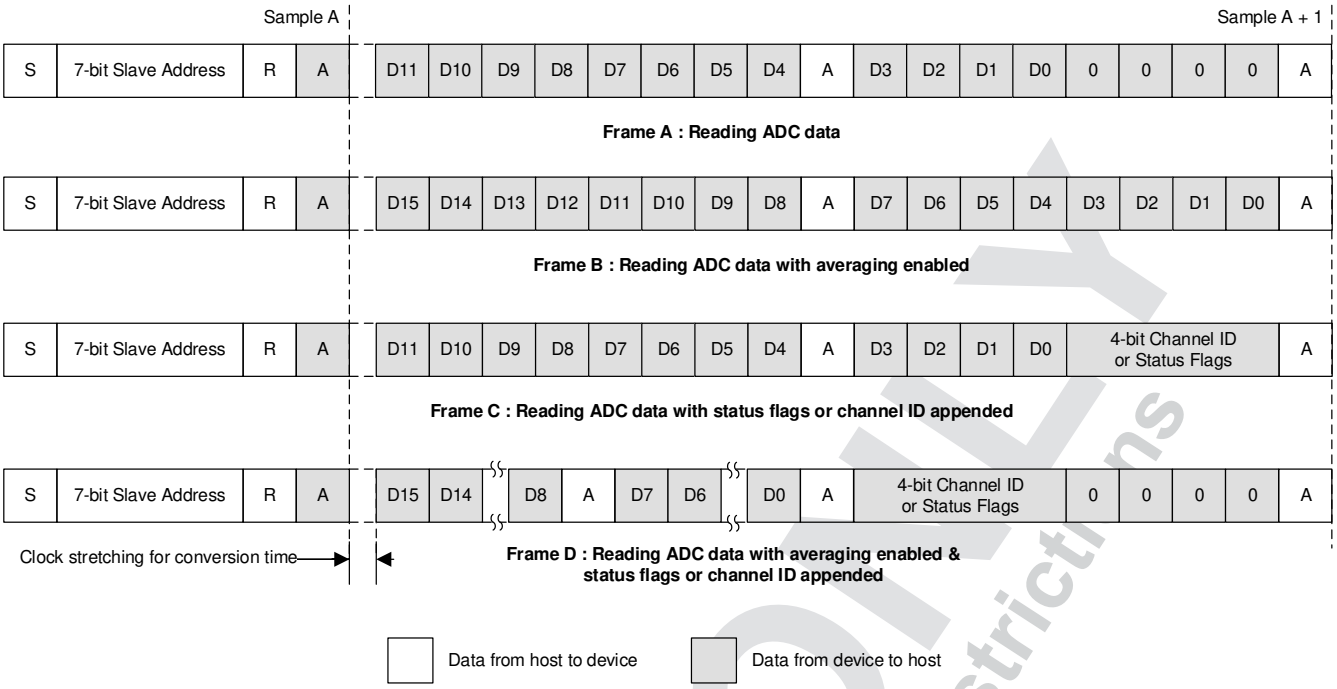


図 8-7. Data Frames for Reading Data

When status flags are enabled, APPEND_STATUS is set to 10b and four bits are appended to the ADC output. The device outputs status flags in this order: {1b, 0b, CRCERR_IN, ALERT}. The level transitions on the digital interface, resulting from the fixed 1b and 0b in the status flags, can be used to detect if the digital outputs are shorted to a fixed voltage in the system. The CRCERR_IN flag reflects the corresponding bit in the GENERAL_CFG register. The ALERT flag is the output of the logical OR of the bits in the EVENT_FLAG register.

8.3.10.1 Status Flags

Status flags can be enabled by setting APPEND_STATUS = 10b. As shown in 図 8-7, four additional bits are appended to the ADC output when status flags are enabled.

The device outputs status flags in this order: {1b, 0b, CRCERR_IN, ALERT}. The CRCERR_IN flag reflects the corresponding bit in the GENERAL_CFG register. The ALERT flag is the output of the logical OR of the bits in the EVENT_FLAG register.

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8.3.11 Digital Window Comparator

The digital window comparator (DWC) compares the conversion result for an analog input channel with programmable high and low thresholds with hysteresis. As shown in 図 8-8, the DWC sets the EVENT_HIGH_FLAG and EVENT_LOW_FLAG registers based on the comparison result sounds better. The logical OR of the EVENT_HIGH_FLAG and EVENT_LOW_FLAG registers is available in the EVENT_FLAG register. The ALERT pin is asserted when a bit in the EVENT_FLAG register is high and the corresponding bit in the ALERT_CH_SEL register is enabled.

The ALERT pin can be configured as open-drain (default) or push-pull output using the ALERT_DRIVE bit in the ALERT_PIN_CFG register.

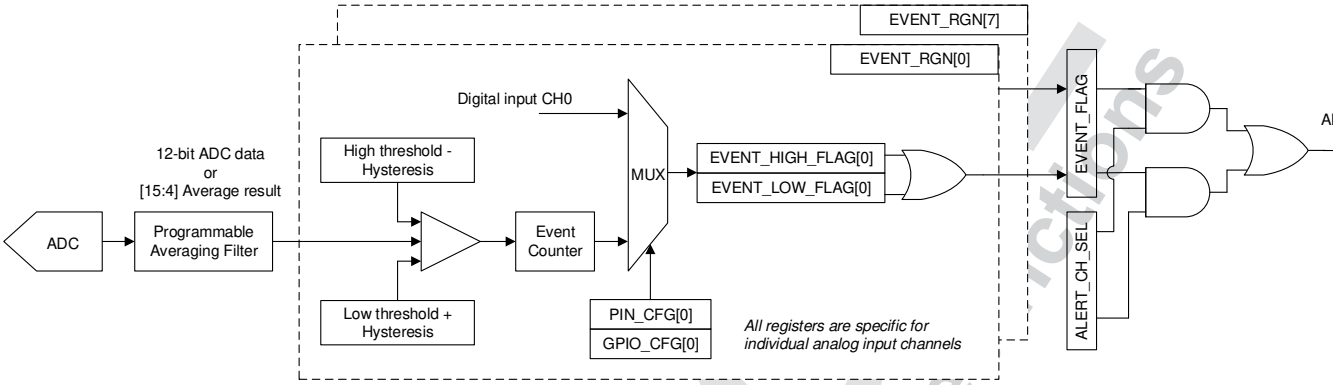


図 8-8. Digital Window Comparator Block Diagram

The low-side threshold, high-side threshold, event counter, and hysteresis parameters are independently programmable for each input channel. 図 8-9 shows the events that can be monitored for every analog input channel by the window comparator.

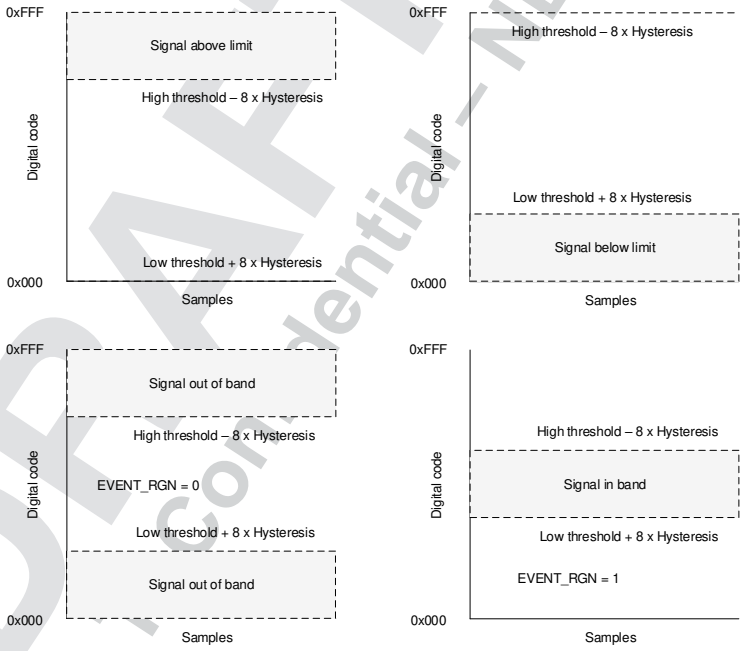


図 8-9. Event Monitoring With the Window Comparator

To enable the digital window comparator, set the DWC_EN bit in the GENERAL_CFG register. By default, hysteresis is 0, the high threshold is 0xFFF, and the low threshold is 0x000. Configure the EVENT_RGN register to detect when a signal is within a band defined by the high and low thresholds. In each of the cases shown in 図 8-9, either or both EVENT_HIGH_FLAG and EVENT_LOW_FLAG can be set.

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The device features a programmable event counter that counts consecutive threshold violations before either EVENT_HIGH_FLAG or EVENT_LOW_FLAG are set. An example is shown in 図 8-10 where the EVENT_HIGH_FLAG is not set until eight consecutive conversion results of the corresponding analog input channel exceed the threshold configuration. The event count can be set to a higher value to avoid transients in the input signal from setting the event flags.

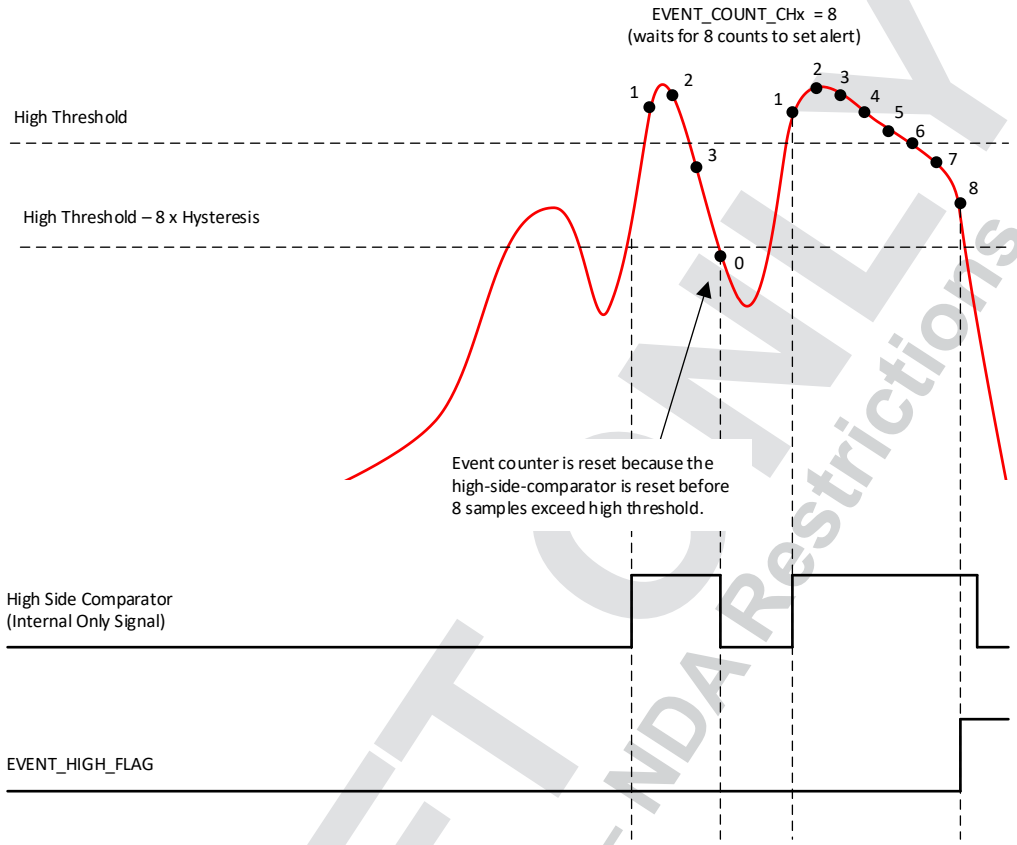


図 8-10. False Trigger Avoidance Using the Event Counter

In order to assert the ALERT pin when the alert flag is set for a particular analog input channel, set the corresponding bit in the ALERT_CH_SEL register.

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8.3.11.1 Interrupts From Digital Inputs

Rising edge or falling edge events can be detected on channels configured as digital inputs. As described in 表 8-7, configure the EVENT_RGN register to select either a rising edge or falling edge event.

表 8-7. Configuring Interrupts From Digital Inputs

PIN_CFG[7:0]	GPIO_CFG[7:0]	EVENT_RGN [7:0]	EVENT DESCRIPTION
1	0	0	A rising edge on the digital input sets the corresponding flag in the EVENT_HIGH_FLAG register.
1	0	1	A falling edge on the digital input sets the corresponding flag in the EVENT_LOW_FLAG register.

8.3.11.2 Triggering Digital Outputs With a Digital Window Comparator

As shown in 図 8-11, the output value of channels configured as digital outputs can be updated in response to one or more flags being set in the EVENT_FLAG register.

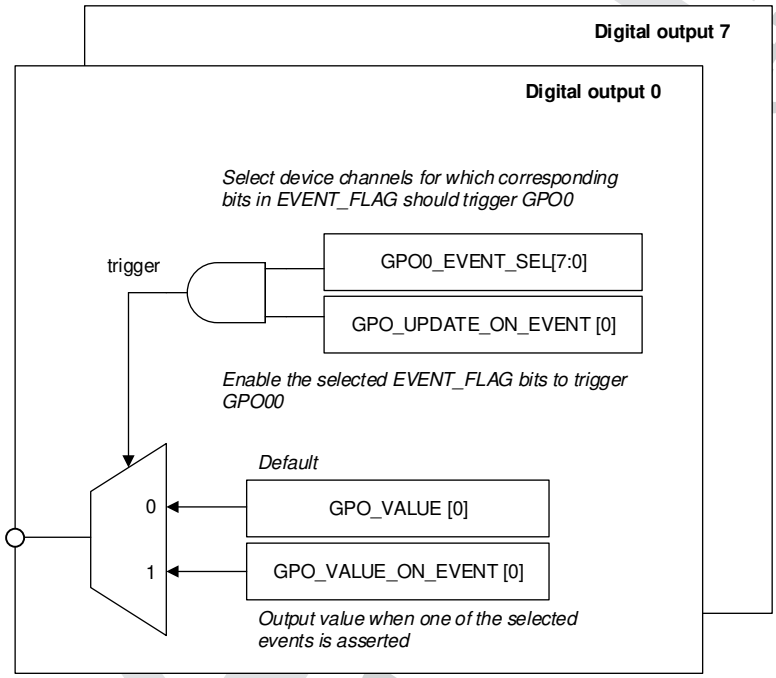


図 8-11. Block Diagram of the Digital Output Logic

The following procedure enables updating the output value of a digital output in response to event flags:

1. Configure the device channels as either analog inputs (default), digital inputs, or digital outputs.
2. Configure the digital outputs as either open-drain (default) or push-pull outputs.
3. Configure the digital window comparator for the input channels. The digital window comparator updates the flags in the EVENT_FLAG register corresponding to individual channels. See the *Digital Window Comparator* section for more details.
4. Select the bits corresponding to the input channels that are to be enabled for triggering the digital output in the GPOx_EVENT_SEL register (where x is the digital output channel number).
5. The default output value of the digital output, when no event flag is set, is configured in the GPO_VALUE register. The output value of the digital output, when event flags are set, is configured in the GPO_VALUE_ON_EVENT register.
6. Configure the GPO_UPDATE_ON_EVENT register to enable the logic to update the selected digital output in response to event flags.

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The configuration in GPO_VALUE sets the output value of a dgital output when either no event flags are set or when event flags are reset in the EVENT_FLAG register corresponding to channels selected in the GPOx_EVENT_SEL register.

8.3.12 Minimum, Maximum, and Latest Data Registers

The ADS7138-Q1 can record the minimum, maximum, and latest code (statistics registers) for every analog input channel. To enable or re-enable recording statistics, set the STATS_EN bit in the GENERAL_CFG register. Writing 1 to the STATS_EN bit reinitializes the statistics module. Previous values can be read from the statistics registers until a new conversion result is available. Set STATS_EN = 0b to prevent any updates to this block of registers before reading the statistics registers.

8.3.13 I^2C Protocol Features

8.3.13.1 General Call

On receiving a general call (00h), the device provides an acknowledge (ACK).

8.3.13.2 General Call With Software Reset

On receiving a general call (00h) followed by a software reset (06h), the device resets itself.

8.3.13.3 General Call With a Software Write to the Programmable Part of the Slave Address

On receiving a general call (00h) followed by 04h, the device reevaluates its own I^2C address configured by the ADDR pin. During this operation, the device does not respond to other I^2C commands except the general-call command.

8.3.13.4 Configuring the Device for High-Speed I^2C Mode

The device can be configured in high-speed I^2C mode by providing an I^2C frame with one of these codes: 0x09, 0x0B, 0x0D, or 0x0F.

After receiving one of these codes, the device sets the I^2C_SPEED bit in the SYSTEM_STATUS register and remains in high-speed I^2C mode until a STOP condition is received in an I^2C frame.

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8.4 Device Functional Modes

表 8-8 lists the functional modes supported by the ADS7138-Q1. The device powers up in manual mode (see the *Manual Mode* section) and can be configured into any mode listed in 表 8-8 by writing the configuration registers for the desired mode.

表 8-8. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	CONV_MODE[1:0]	SEQ_MODE[1:0]
Manual	9th falling edge of SCL (ACK)	Register write to MANUAL_CHID	00b	00b
Auto-sequence	9th falling edge of SCL (ACK)	Channel sequencer	00b	01b
Autonomous	Internal to the device	Channel sequencer	01b	01b
Turbo comparator	Internal to the device	Channel sequencer	10b	01b

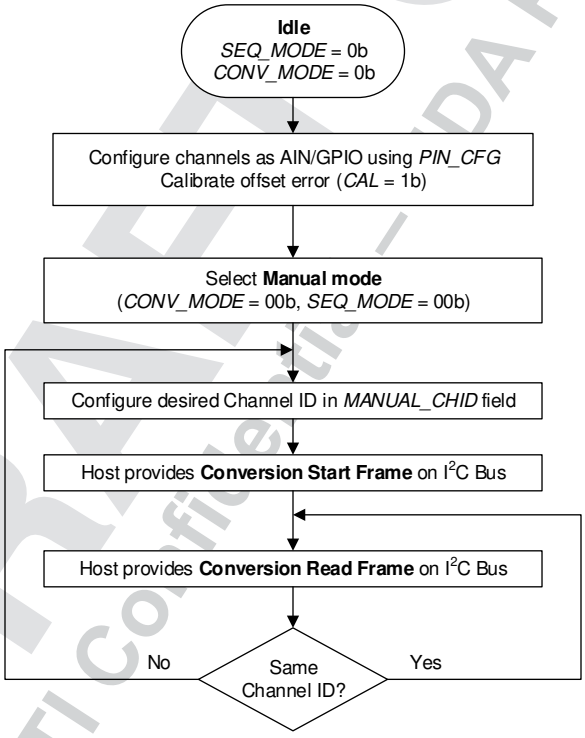
8.4.1 Device Power-Up and Reset

On power-up, the device calculates the address from the resistors connected on the ADDR pin and the BOR bit is set, thus indicating a power-cycle or reset event.

The device can be reset by an I^2C general call (00h) followed by a software reset (06h), by setting the RST bit, or by recycling the power on the AVDD pin.

8.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. 図 8-12 lists the steps for operating the device in manual mode.



Manual mode with channel selection using register write

図 8-12. Device Operation in Manual Mode

Provide an I^2C start or restart frame to initiate a conversion, as illustrated in the conversion start frame of 図 8-13, after configuring the device registers. ADC data can be read in subsequent I^2C frames. The number of I^2C frames required to read conversion data depends on the output data frame size; see the *Output Data Format*

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section for more details. A new conversion is initiated on the ninth falling edge of SCL (ACK bit) when the last byte of output data is read.

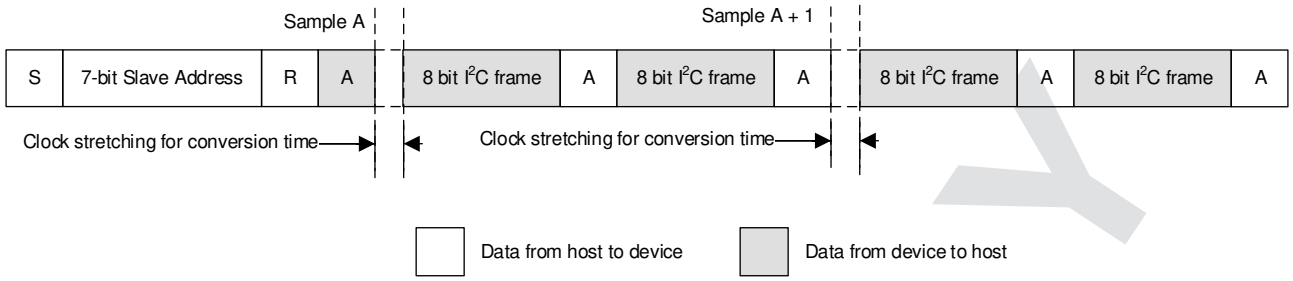


図 8-13. Starting a Conversion and Reading Data in Manual Mode

8.4.3 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CH_SEL register. To enable the channel sequencer, set SEQ_START to 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START to 0b. 図 8-14 lists the conversion start and read frames for auto-sequence mode.

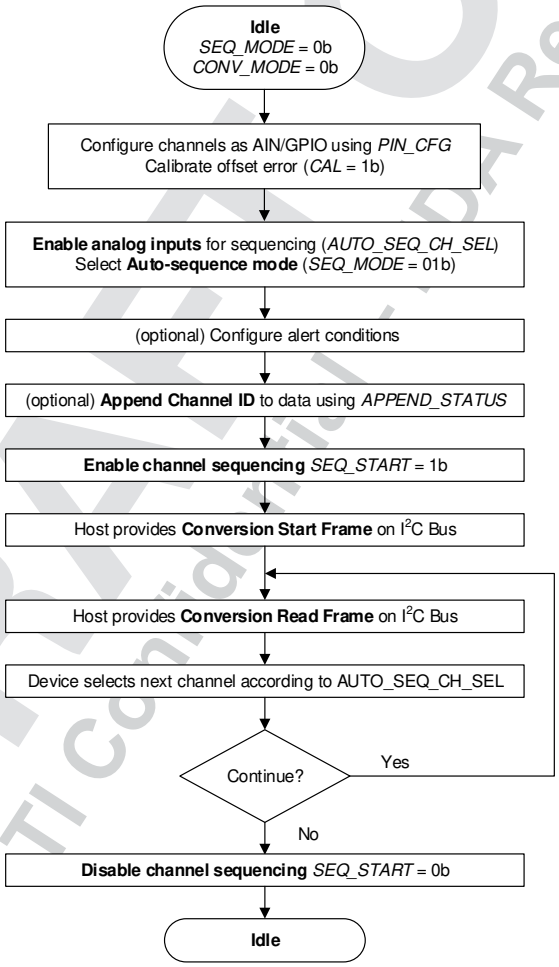


図 8-14. Device Operation in Auto-Sequence Mode

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8.4.4 Autonomous Mode

In autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate a signal on the ALERT pin when the programmable high or low threshold values are crossed. In this mode, the device generates the start of conversion using the internal oscillator. The first start of conversion must be provided by the host and the device then generates the subsequent start of conversions.

図 8-15 shows the steps for configuring the operation mode to autonomous mode. Abort the ongoing sequence by setting SEQ_START to 0b before changing the functional mode or device configuration.

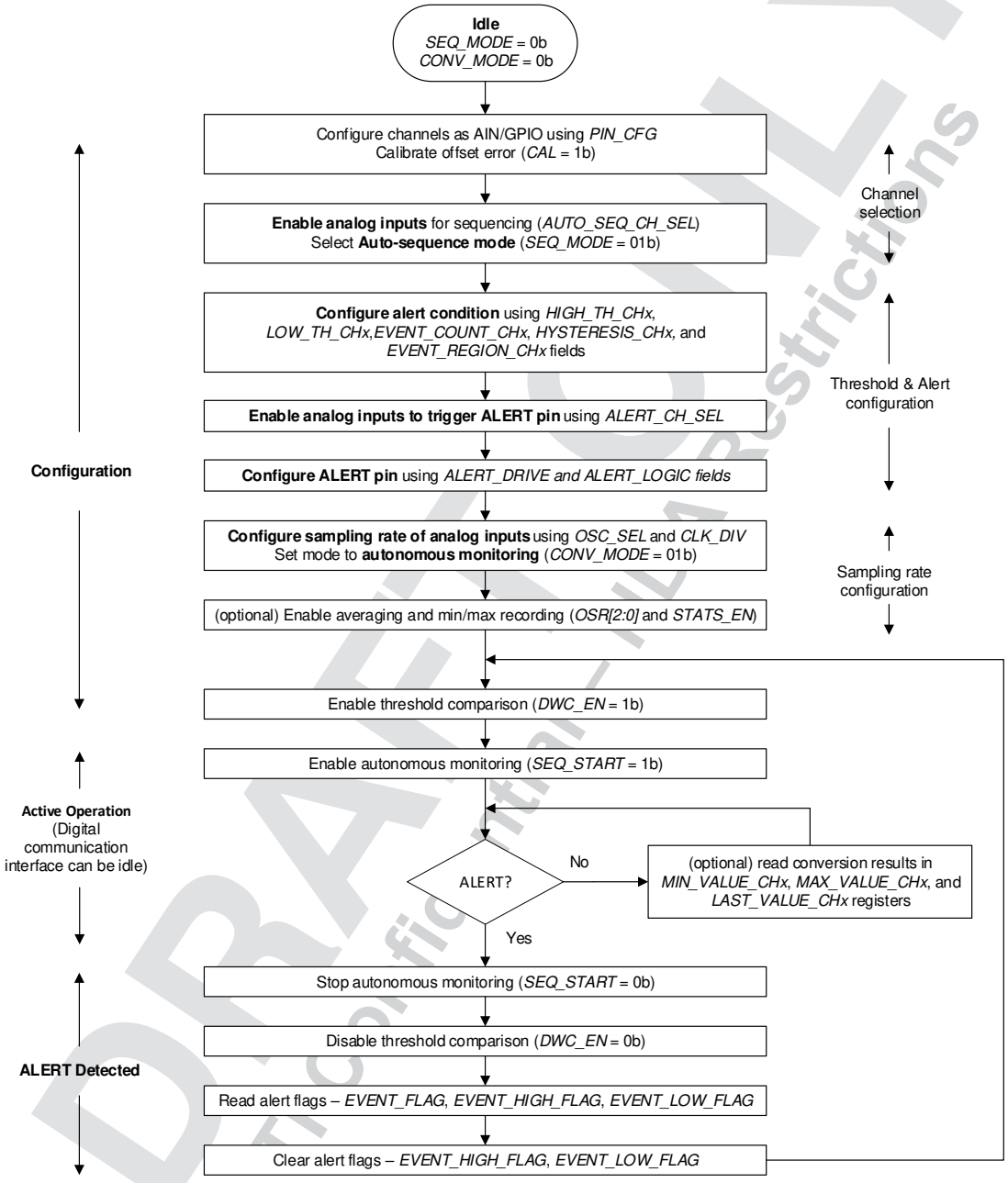


図 8-15. Configuring the Device in Autonomous Mode

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8.4.5 Turbo Comparator Mode

Turbo comparator mode allows fast comparison with high and low thresholds using the digital window comparator. ADC output data are not available in this mode.

図 8-16 lists the comparison start and read frames for turbo comparator mode. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CH_SEL register. To enable the channel sequencer, set SEQ_START to 1b. After every comparison, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START to 0b. See the *Oscillator and Timing Control* section for more details on configuring the speed in turbo comparator mode.

Abort the ongoing sequence by setting SEQ_START to 0b before changing the functional mode or device configuration.

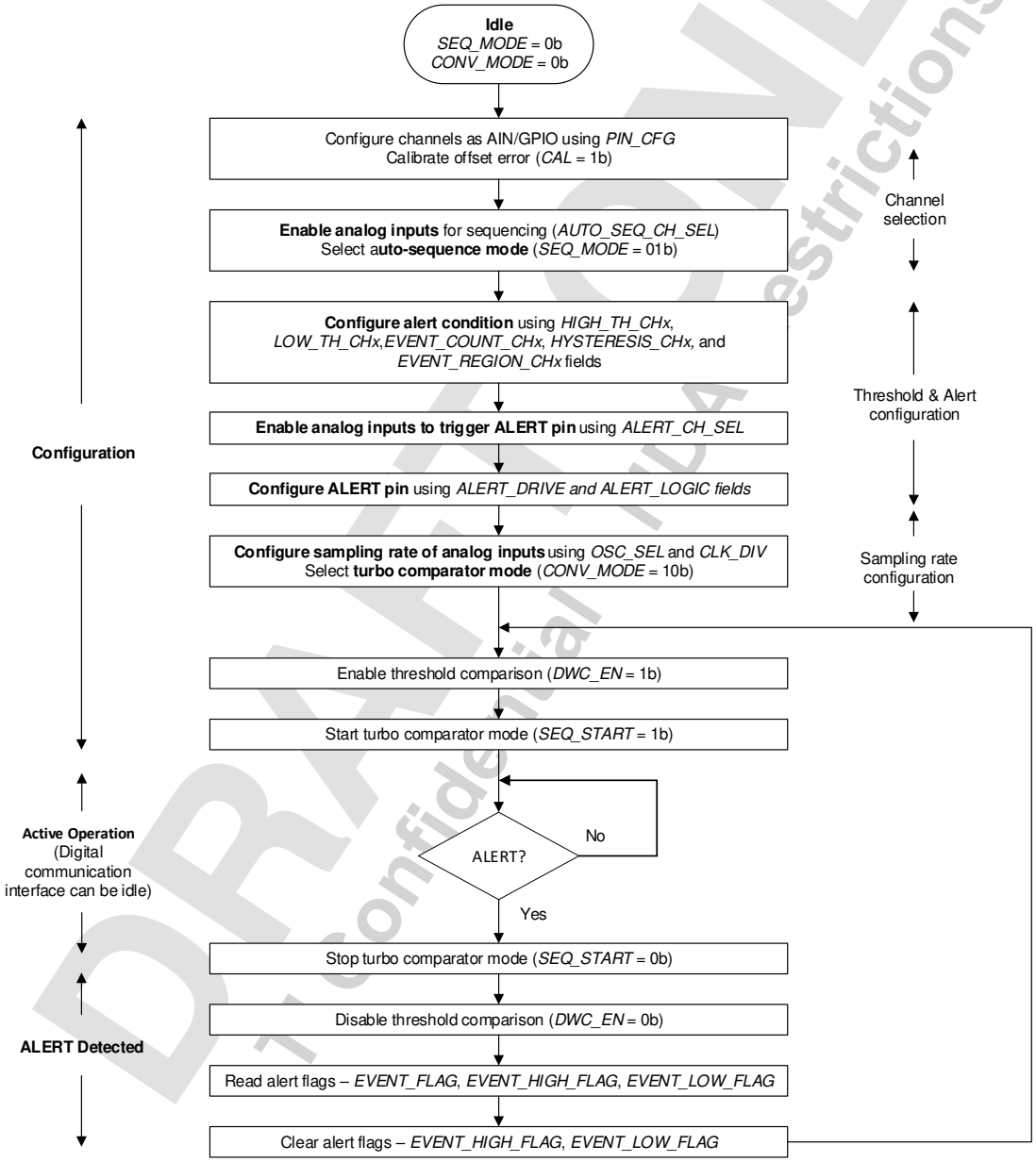


図 8-16. Device Operation in Turbo Comparator Mode

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8.5 Programming

表 8-9 provides the acronyms for different conditions in an I²C frame. 表 8-10 lists the various command opcodes.

表 8-9. I²C Frame Acronyms

SYMBOL	DESCRIPTION
S	Start condition for the I²C frame
Sr	Restart condition for the I²C frame
P	Stop condition for the I²C frame
A	ACK (low)
N	NACK (high)
R	Read bit (high)
W	Write bit (low)

表 8-10. Opcodes for Commands

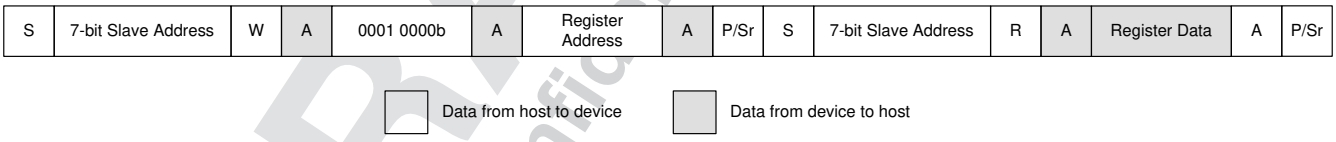
OPCODE	COMMAND DESCRIPTION
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit
0011 0000b	Reading a continuous block of registers
0010 1000b	Writing a continuous block of registers

8.5.1 Register Read

The I²C master can either read a single register or a continuous block registers from the device, as described in the *Single Register Read* and *Reading a Continuous Block of Registers* sections.

8.5.1.1 Single Register Read

To read a single register from the device, the I²C master must provide an I²C command with three frames to set the register address for reading data. The opcodes for commands supported by the device are listed in 表 8-10. After an I²C command is provided, the I²C master must provide another I²C frame (as shown in 図 8-17) containing the device address and the read bit. The device provides the register data in the next I²C frame. The device provides the same register data even if the host provides more I²C frames. To end the register read command, the master must provide a STOP or a RESTART condition in the I²C frame.



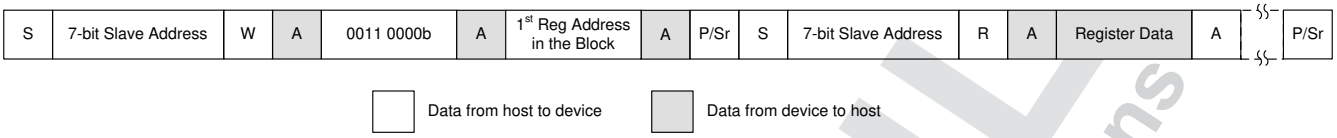
S = start, Sr = repeated start, and P = stop.

図 8-17. Single Register Read

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8.5.1.2 Reading a Continuous Block of Registers

To read a continuous block of registers, the I²C master must provide an I²C command to set the register address. The register address is the address of the first register in the block that must be read. After this command is provided, the I²C master must provide another I²C frame, as shown in 図 8-18, containing the device address and the read bit. After this frame, the device provides the register data. The device provides data for the next register when more clocks are provided. When data are read from addresses that do not exist in the register map of the device, the device returns zeros. If the device does not have any further registers to provide data on, the device provide zeros. To end the register read command, the master must provide a STOP or a RESTART condition in the I²C frame.



S = start, Sr = repeated start, and P = stop.

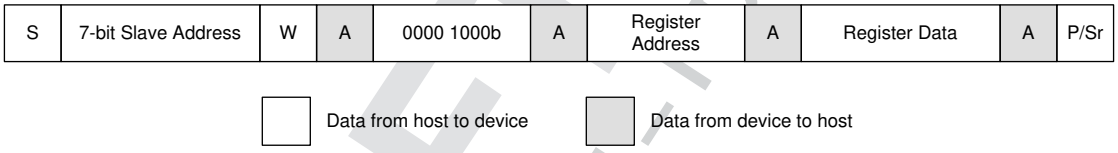
図 8-18. Reading a Continuous Block of Registers

8.5.2 Writing Registers

The I²C master can either write a single register or a continuous block of registers to the device, set a few bits in a register, or clear a few bits in a register.

8.5.2.1 Single Register Write

To write a single register from the device, as shown in 図 8-19, the I²C master must provide an I²C command with four frames. The register address is the address of the register that must be written and the register data is the value that must be written. 表 8-10 lists the opcodes for different commands. To end the register write command, the master must provide a STOP or a RESTART condition in the I²C frame.



S = start, Sr = repeated start, and P = stop.

図 8-19. Writing a Single Register

8.5.2.2 Set Bit

The I²C master must provide an I²C command with four frames, as shown in 図 8-19, to set bits in a register without changing the other bits. The register address is the address of the register that the bits must set and the register data is the value representing the bits that must be set. Bits with a value of 1 in the register data are set and bits with a value of 0 in the register data are not changed. 表 8-10 lists the opcodes for different commands. To end this command, the master must provide a STOP or RESTART condition in the I²C frame.

8.5.2.3 Clear Bit

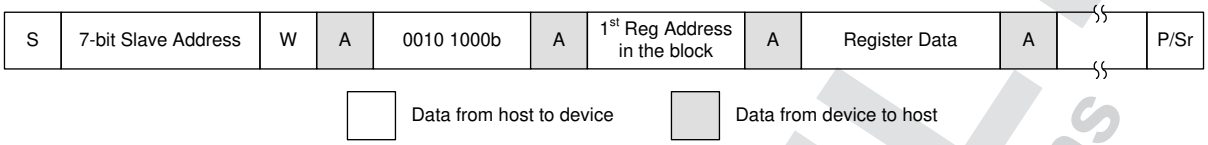
The I²C master must provide an I²C command with four frames, as shown in 図 8-19, to clear bits in a register without changing the other bits. The register address is the address of the register that the bits must clear and the register data is the value representing the bits that must be cleared. Bits with a value of 1 in the register data are cleared and bits with a value of 0 in the register data are not changed. 表 8-10 lists the opcodes for different commands. To end this command, the master must provide a STOP or a RESTART condition in the I²C frame.

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8.5.2.4 Writing a Continuous Block of Registers

The I²C master must provide an I²C command, as shown in 図 8-20, to write a continuous block of registers. The register address is the address of the first register in the block that must be written. The I²C master must provide data for registers in subsequent I²C frames in an ascending order of register addresses. Writing data to addresses that do not exist in the register map of the device have no effect. 表 8-10 lists the opcodes for different commands. If the data provided by the I²C master exceeds the address space of the device, the device ignores the data beyond the address space. To end the register write command, the master must provide a STOP or a RESTART condition in the I²C frame.



S = start, Sr = repeated start, and P = stop.

図 8-20. Writing a Continuous Block of Registers

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8.6 ADS7138-Q1 Registers

表 8-11 lists the memory-mapped registers for the ADS7138-Q1 registers. All register offset addresses not listed in 表 8-11 should be considered as reserved locations and the register contents should not be modified.

表 8-11. ADS7138-Q1 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		セクション 8.6.1
0x1	GENERAL_CFG		セクション 8.6.2
0x2	DATA_CFG		セクション 8.6.3
0x3	OSR_CFG		セクション 8.6.4
0x4	OPMODE_CFG		セクション 8.6.5
0x5	PIN_CFG		セクション 8.6.6
0x7	GPIO_CFG		セクション 8.6.7
0x9	GPO_DRIVE_CFG		セクション 8.6.8
0xB	GPO_VALUE		セクション 8.6.9
0xD	GPI_VALUE		セクション 8.6.10
0x10	SEQUENCE_CFG		セクション 8.6.11
0x11	MANUAL_CH_SEL		セクション 8.6.12
0x12	AUTO_SEQ_CH_SEL		セクション 8.6.13
0x14	ALERT_CH_SEL		セクション 8.6.14
0x16	ALERT_FUNC_SEL		セクション 8.6.15
0x17	ALERT_PIN_CFG		セクション 8.6.16
0x18	EVENT_FLAG		セクション 8.6.17
0x1A	EVENT_HIGH_FLAG		セクション 8.6.18
0x1C	EVENT_LOW_FLAG		セクション 8.6.19
0x1E	EVENT_RGN		セクション 8.6.20
0x20	HYSTERESIS_CH0		セクション 8.6.21
0x21	HIGH_TH_CH0		セクション 8.6.22
0x22	EVENT_COUNT_CH0		セクション 8.6.23
0x23	LOW_TH_CH0		セクション 8.6.24
0x24	HYSTERESIS_CH1		セクション 8.6.25
0x25	HIGH_TH_CH1		セクション 8.6.26
0x26	EVENT_COUNT_CH1		セクション 8.6.27
0x27	LOW_TH_CH1		セクション 8.6.28
0x28	HYSTERESIS_CH2		セクション 8.6.29
0x29	HIGH_TH_CH2		セクション 8.6.30
0x2A	EVENT_COUNT_CH2		セクション 8.6.31
0x2B	LOW_TH_CH2		セクション 8.6.32
0x2C	HYSTERESIS_CH3		セクション 8.6.33
0x2D	HIGH_TH_CH3		セクション 8.6.34
0x2E	EVENT_COUNT_CH3		セクション 8.6.35
0x2F	LOW_TH_CH3		セクション 8.6.36
0x30	HYSTERESIS_CH4		セクション 8.6.37
0x31	HIGH_TH_CH4		セクション 8.6.38
0x32	EVENT_COUNT_CH4		セクション 8.6.39
0x33	LOW_TH_CH4		セクション 8.6.40
0x34	HYSTERESIS_CH5		セクション 8.6.41
0x35	HIGH_TH_CH5		セクション 8.6.42

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表 8-11. ADS7138-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0x36	EVENT_COUNT_CH5		セクション 8.6.43
0x37	LOW_TH_CH5		セクション 8.6.44
0x38	HYSTERESIS_CH6		セクション 8.6.45
0x39	HIGH_TH_CH6		セクション 8.6.46
0x3A	EVENT_COUNT_CH6		セクション 8.6.47
0x3B	LOW_TH_CH6		セクション 8.6.48
0x3C	HYSTERESIS_CH7		セクション 8.6.49
0x3D	HIGH_TH_CH7		セクション 8.6.50
0x3E	EVENT_COUNT_CH7		セクション 8.6.51
0x3F	LOW_TH_CH7		セクション 8.6.52
0x60	MAX_CH0_LSB		セクション 8.6.53
0x61	MAX_CH0_MSB		セクション 8.6.54
0x62	MAX_CH1_LSB		セクション 8.6.55
0x63	MAX_CH1_MSB		セクション 8.6.56
0x64	MAX_CH2_LSB		セクション 8.6.57
0x65	MAX_CH2_MSB		セクション 8.6.58
0x66	MAX_CH3_LSB		セクション 8.6.59
0x67	MAX_CH3_MSB		セクション 8.6.60
0x68	MAX_CH4_LSB		セクション 8.6.61
0x69	MAX_CH4_MSB		セクション 8.6.62
0x6A	MAX_CH5_LSB		セクション 8.6.63
0x6B	MAX_CH5_MSB		セクション 8.6.64
0x6C	MAX_CH6_LSB		セクション 8.6.65
0x6D	MAX_CH6_MSB		セクション 8.6.66
0x6E	MAX_CH7_LSB		セクション 8.6.67
0x6F	MAX_CH7_MSB		セクション 8.6.68
0x80	MIN_CH0_LSB		セクション 8.6.69
0x81	MIN_CH0_MSB		セクション 8.6.70
0x82	MIN_CH1_LSB		セクション 8.6.71
0x83	MIN_CH1_MSB		セクション 8.6.72
0x84	MIN_CH2_LSB		セクション 8.6.73
0x85	MIN_CH2_MSB		セクション 8.6.74
0x86	MIN_CH3_LSB		セクション 8.6.75
0x87	MIN_CH3_MSB		セクション 8.6.76
0x88	MIN_CH4_LSB		セクション 8.6.77
0x89	MIN_CH4_MSB		セクション 8.6.78
0x8A	MIN_CH5_LSB		セクション 8.6.79
0x8B	MIN_CH5_MSB		セクション 8.6.80
0x8C	MIN_CH6_LSB		セクション 8.6.81
0x8D	MIN_CH6_MSB		セクション 8.6.82
0x8E	MIN_CH7_LSB		セクション 8.6.83
0x8F	MIN_CH7_MSB		セクション 8.6.84
0xA0	RECENT_CH0_LSB		セクション 8.6.85
0xA1	RECENT_CH0_MSB		セクション 8.6.86
0xA2	RECENT_CH1_LSB		セクション 8.6.87

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表 8-11. ADS7138-Q1 Registers (continued)

Address	Acronym	Register Name	Section
0xA3	RECENT_CH1_MSB		セクション 8.6.88
0xA4	RECENT_CH2_LSB		セクション 8.6.89
0xA5	RECENT_CH2_MSB		セクション 8.6.90
0xA6	RECENT_CH3_LSB		セクション 8.6.91
0xA7	RECENT_CH3_MSB		セクション 8.6.92
0xA8	RECENT_CH4_LSB		セクション 8.6.93
0xA9	RECENT_CH4_MSB		セクション 8.6.94
0xAA	RECENT_CH5_LSB		セクション 8.6.95
0xAB	RECENT_CH5_MSB		セクション 8.6.96
0xAC	RECENT_CH6_LSB		セクション 8.6.97
0xAD	RECENT_CH6_MSB		セクション 8.6.98
0xAE	RECENT_CH7_LSB		セクション 8.6.99
0xAF	RECENT_CH7_MSB		セクション 8.6.100
0xC3	GPO0_TRIG_EVENT_SEL		セクション 8.6.101
0xC5	GPO1_TRIG_EVENT_SEL		セクション 8.6.102
0xC7	GPO2_TRIG_EVENT_SEL		セクション 8.6.103
0xC9	GPO3_TRIG_EVENT_SEL		セクション 8.6.104
0xCB	GPO4_TRIG_EVENT_SEL		セクション 8.6.105
0xCD	GPO5_TRIG_EVENT_SEL		セクション 8.6.106
0xCF	GPO6_TRIG_EVENT_SEL		セクション 8.6.107
0xD1	GPO7_TRIG_EVENT_SEL		セクション 8.6.108
0xE9	GPO_TRIGGER_CFG		セクション 8.6.109
0xEB	GPO_VALUE_TRIG		セクション 8.6.110

Complex bit access types are encoded to fit into small table cells. 表 8-12 shows the codes that are used for access types in this section.

表 8-12. ADS7138-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.

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表 8-12. ADS7138-Q1 Access Type Codes (continued)

Access Type	Code	Description
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

8.6.1 SYSTEM_STATUS Register (Address = 0x0) [Reset = 0x81]

SYSTEM_STATUS is shown in 図 8-17 and described in 表 8-13.

Return to the 表 8-11.

図 8-17. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	I²C_SPEED	RESERVED	OSR_DONE	CRC_ERR_FUSE	CRC_ERR_IN	BOR
R-1b	R-0b	R-0b	R-0b	R/W-0b	R-0b	R/W-0b	R/W-1b

表 8-13. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5	I²C_SPEED	R	0b	I²C high-speed status. 0b = I²C bus is not in high-speed mode. 1b = I²C bus is in high-speed mode.
4	RESERVED	R	0b	Reserved Bit
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRC_ERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRC_ERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out condition detected from last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

8.6.2 GENERAL_CFG Register (Address = 0x1) [Reset = 0x0]

GENERAL_CFG is shown in 図 8-18 and described in 表 8-14.

Return to the 表 8-11.

図 8-18. GENERAL_CFG Register

7	6	5	4	3	2	1	0

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図 8-18. GENERAL_CFG Register (continued)

RESERVED	CRC_EN	STATS_EN	DWC_EN	CNVST	CH_RST	CAL	RST
R-0b	R/W-0b	R/W-0b	R/W-0b	W-0b	R/W-0b	R/W-0b	W-0b

表 8-14. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved Bit
6	CRC_EN	R/W	0b	Enable or disable the CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5	STATS_EN	R/W	0b	Enable or disable the statistics module to update minimu, maximum, and latest output code registers. 0b = Statistics registers are not updated. 1b = Clear statistics registers and conitnue updating with new conversion results.
4	DWC_EN	R/W	0b	Enable or disable the digital window comparator. 0b = Reset or disable the digital window comparator. 1b = Enable the digital window comparator.
3	CNVST	W	0b	Control start conversion on selected analog input. Readback of this bit returns 0b. 0b = Normal operation; conversions starts on the 9th falling edge of I^{2}C frame. Device stretches SCL until end of conversion or completion of averaging. 1b = Initiate start of conversion. Device does not stretch SCL until end of conversion or completion of averaging.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels are configured as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b by the device.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b by the device.

8.6.3 DATA_CFG Register (Address = 0x2) [Reset = 0x0]

DATA_CFG is shown in 図 8-19 and described in 表 8-15.

Return to the 表 8-11.

図 8-19. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED			
R/W-0b	R-0b	R/W-0b		R-0b			

表 8-15. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device will output fixed data bits, which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A repeatitively when reading data.
6	RESERVED	R	0b	Reserved Bit

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表 8-15. DATA_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-0	RESERVED	R	0b	Reserved Bit

8.6.4 OSR_CFG Register (Address = 0x3) [Reset = 0x0]

OSR_CFG is shown in 図 8-20 and described in 表 8-16.

Return to the 表 8-11.

図 8-20. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

表 8-16. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved Bit
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

8.6.5 OPMODE_CFG Register (Address = 0x4) [Reset = 0x0]

OPMODE_CFG is shown in 図 8-21 and described in 表 8-17.

Return to the 表 8-11.

図 8-21. OPMODE_CFG Register

7	6	5	4	3	2	1	0
CONV_ON_ERR	CONV_MODE[1:0]		OSC_SEL	CLK_DIV[3:0]			
R/W-0b	R/W-0b		R/W-0b	R/W-0b			

表 8-17. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CONV_ON_ERR	R/W	0b	Control continuation of autonomous and turbo comparator modes if CRC error is detected on communication interface. 0b = If CRC error is detected, device continues channel sequencing and pin configuration is retained. See the CRC_ERR_IN bit for more details. 1b = If CRC error is detected, device changes all channels to analog inputs and channel sequencing is paused until CRC_ERR_IN = 1b. After clearing CRC_ERR_IN flag, device resumes channel sequencing and pin confguration is restored.

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表 8-17. OPMODE_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-5	CONV_MODE[1:0]	R/W	0b	These bits set the mode of conversion of the ADC. 0b = Manual mode; conversions are initiated by host. 1b = Autonomous mode; conversions are initiated by internal state machine. 10b = Turbo mode; comparisons are initiated by internal state machine.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control. See the section on oscillator and timing control for details.

8.6.6 PIN_CFG Register (Address = 0x5) [Reset = 0x0]

PIN_CFG is shown in 図 8-22 and described in 表 8-18.

Return to the 表 8-11.

図 8-22. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

表 8-18. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN/GPIO[7:0] as analog inputs or GPIOs. 0b = Channel is configured as an analog input. 1b = Channel is configured as a GPIO.

8.6.7 GPIO_CFG Register (Address = 0x7) [Reset = 0x0]

GPIO_CFG is shown in 図 8-23 and described in 表 8-19.

Return to the 表 8-11.

図 8-23. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

表 8-19. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

8.6.8 GPO_DRIVE_CFG Register (Address = 0x9) [Reset = 0x0]

GPO_DRIVE_CFG is shown in 図 8-24 and described in 表 8-20.

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図 8-24. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

表 8-20. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as either open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

8.6.9 GPO_VALUE Register (Address = 0xB) [Reset = 0x0]

GPO_VALUE is shown in 図 8-25 and described in 表 8-21.

Return to the 表 8-11.

図 8-25. GPO_VALUE Register

7	6	5	4	3	2	1	0
GPO_VALUE[7:0]							
R/W-0b							

表 8-21. GPO_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output is set to logic 0. 1b = Digital output is set to logic 1.

8.6.10 GPI_VALUE Register (Address = 0xD) [Reset = 0x0]

GPI_VALUE is shown in 図 8-26 and described in 表 8-22.

Return to the 表 8-11.

図 8-26. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

表 8-22. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	This field returns the logical level of all channels including analog inputs, digital inputs, and digital outputs. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

8.6.11 SEQUENCE_CFG Register (Address = 0x10) [Reset = 0x0]

SEQUENCE_CFG is shown in 図 8-27 and described in 表 8-23.

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図 8-27. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

表 8-23. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved Bit
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved Bit
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by AUTO_SEQ_CH_SEL. 10b = Reserved. 11b = Reserved.

8.6.12 MANUAL_CH_SEL Register (Address = 0x11) [Reset = 0x0]

MANUAL_CH_SEL is shown in 図 8-28 and described in 表 8-24.

Return to the 表 8-11.

図 8-28. MANUAL_CH_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

表 8-24. MANUAL_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved Bit
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7 1000b = Reserved.

8.6.13 AUTO_SEQ_CH_SEL Register (Address = 0x12) [Reset = 0x0]

AUTO_SEQ_CH_SEL is shown in 図 8-29 and described in 表 8-25.

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図 8-29. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

表 8-25. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

8.6.14 ALERT_CH_SEL Register (Address = 0x14) [Reset = 0x0]

ALERT_CH_SEL is shown in 図 8-30 and described in 表 8-26.

Return to the 表 8-11.

図 8-30. ALERT_CH_SEL Register

7	6	5	4	3	2	1	0
ALERT_CH_SEL[7:0]							
R/W-0b							

表 8-26. ALERT_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ALERT_CH_SEL[7:0]	R/W	0b	Select channels for which the alert flags can assert the ALERT pin. 0b = Event flags for this channel do not assert the ALERT pin. 1b = Event flags for this channel assert the ALERT pin.

8.6.15 ALERT_FUNC_SEL Register (Address = 0x16) [Reset = 0x0]

ALERT_FUNC_SEL is shown in 図 8-31 and described in 表 8-27.

Return to the 表 8-11.

図 8-31. ALERT_FUNC_SEL Register

7	6	5	4	3	2	1	0
RESERVED							ALERT_CRCIN
R-0b							R/W-0b

表 8-27. ALERT_FUNC_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0b	Reserved Bit
0	ALERT_CRCIN	R/W	0b	Enable or disable the alert notification for CRC error on input data (CRCERR_IN = 1b). 0b = ALERT pin is not asserted when CRCERR_IN = 1b. 1b = ALERT pin is asserted when CRCERR_IN = 1b. Clear CRCERR_IN for deasserting the ALERT pin.

8.6.16 ALERT_PIN_CFG Register (Address = 0x17) [Reset = 0x0]

ALERT_PIN_CFG is shown in 図 8-32 and described in 表 8-28.

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図 8-32. ALERT_PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED					ALERT_DRIVE	ALERT_LOGIC[1:0]	
R-0b					R/W-0b	R/W-0b	

表 8-28. ALERT_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved Bit
2	ALERT_DRIVE	R/W	0b	Configure output drive of the ALERT pin. 0b = Open-drain output. Connect external pullup resistor. 1b = Push-pull output.
1-0	ALERT_LOGIC[1:0]	R/W	0b	Configure how ALERT pin is asserted. 0b = Active low. 1b = Active high. 10b = Pulsed low (one logic low pulse every time a bit in EVENT_FLAG is set to 1b). 11b = Pulsed high (one logic high pulse every time a bit in EVENT_FLAG is set to 1b).

8.6.17 EVENT_FLAG Register (Address = 0x18) [Reset = 0x0]

EVENT_FLAG is shown in 図 8-33 and described in 表 8-29.

Return to the 表 8-11.

図 8-33. EVENT_FLAG Register

7	6	5	4	3	2	1	0
EVENT_FLAG[7:0]							
R-0b							

表 8-29. EVENT_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_FLAG[7:0]	R	0b	Event flags indicating digital window comparator status for AIN/GPIO[7:0]. Clear individual bits of EVENT_HIGH_FLAG or EVENT_LOW_FLAG registers to clear the corresponding bit in this register. 0b = Event condition not detected. 1b = Event condition detected.

8.6.18 EVENT_HIGH_FLAG Register (Address = 0x1A) [Reset = 0x0]

EVENT_HIGH_FLAG is shown in 図 8-34 and described in 表 8-30.

Return to the 表 8-11.

図 8-34. EVENT_HIGH_FLAG Register

7	6	5	4	3	2	1	0
EVENT_HIGH_FLAG[7:0]							
R/W-0b							

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表 8-30. EVENT_HIGH_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_HIGH_FLAG[7:0]	R/W	0b	Event flag corresponding to high threshold of analog input or logic 1 on digital input on AIN/GPIO[7:0]. Write 1b to clear this flag. 0b = No alert condition detected. 1b = Either high threshold was exceeded (analog input) or logic 1 was detected (digital input).

8.6.19 EVENT_LOW_FLAG Register (Address = 0x1C) [Reset = 0x0]

EVENT_LOW_FLAG is shown in 図 8-35 and described in 表 8-31.

Return to the 表 8-11.

図 8-35. EVENT_LOW_FLAG Register

7	6	5	4	3	2	1	0
EVENT_LOW_FLAG[7:0]							
R/W-0b							

表 8-31. EVENT_LOW_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_LOW_FLAG[7:0]	R/W	0b	Event orresponding to low threshold of analog input or logic 0 on digital input on AIN/GPIO[7:0]. Write 1b to clear this flag. 0b = No Event condition detected. 1b = Either low threshold was exceeded (analog input) or logic 0 was detected (digital input).

8.6.20 EVENT_RGN Register (Address = 0x1E) [Reset = 0x0]

EVENT_RGN is shown in 図 8-36 and described in 表 8-32.

Return to the 表 8-11.

図 8-36. EVENT_RGN Register

7	6	5	4	3	2	1	0
EVENT_RGN[7:0]							
R/W-0b							

表 8-32. EVENT_RGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	EVENT_RGN[7:0]	R/W	0b	Choice of region used in monitoring analog and digital inputs AIN/GPIO[7:0]. 0b = Event flag is set if: (conversion result < low threshold) or (conversion result > high threshold). For digital inputs, logic 1 sets the alert flag. 1b = Event flag is set if: (low threshold > conversion result < high threshold). For digital inputs, logic 0 sets the eventt flag.

8.6.21 HYSTERESIS_CH0 Register (Address = 0x20) [Reset = 0xF0]

HYSTERESIS_CH0 is shown in 図 8-37 and described in 表 8-33.

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図 8-37. HYSTERESIS_CH0 Register

7	6	5	4	3	2	1	0

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図 8-37. HYSTERESIS_CH0 Register (continued)

HIGH_THRESHOLD_CH0_LSB[3:0]	HYSTERESIS_CH0[3:0]
R/W-1111b	R/W-0b

表 8-33. HYSTERESIS_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH0_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH0[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.22 HIGH_TH_CH0 Register (Address = 0x21) [Reset = 0xFF]

HIGH_TH_CH0 is shown in 図 8-38 and described in 表 8-34.

Return to the 表 8-11.

図 8-38. HIGH_TH_CH0 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH0_MSB[7:0]							
R/W-11111111b							

表 8-34. HIGH_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH0_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.23 EVENT_COUNT_CH0 Register (Address = 0x22) [Reset = 0x0]

EVENT_COUNT_CH0 is shown in 図 8-39 and described in 表 8-35.

Return to the 表 8-11.

図 8-39. EVENT_COUNT_CH0 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH0_LSB[3:0]				EVENT_COUNT_CH0[3:0]			
R/W-0b				R/W-0b			

表 8-35. EVENT_COUNT_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH0_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH0[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.24 LOW_TH_CH0 Register (Address = 0x23) [Reset = 0x0]

LOW_TH_CH0 is shown in 図 8-40 and described in 表 8-36.

Return to the 表 8-11.

図 8-40. LOW_TH_CH0 Register

7	6	5	4	3	2	1	0

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図 8-40. LOW_TH_CH0 Register (continued)

LOW_THRESHOLD_CH0_MSB[7:0]
R/W-0b

表 8-36. LOW_TH_CH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH0_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.25 HYSTERESIS_CH1 Register (Address = 0x24) [Reset = 0xF0]

HYSTERESIS_CH1 is shown in 図 8-41 and described in 表 8-37.

Return to the 表 8-11.

図 8-41. HYSTERESIS_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_LSB[3:0]				HYSTERESIS_CH1[3:0]			
R/W-1111b				R/W-0b			

表 8-37. HYSTERESIS_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH1_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH1[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.26 HIGH_TH_CH1 Register (Address = 0x25) [Reset = 0xFF]

HIGH_TH_CH1 is shown in 図 8-42 and described in 表 8-38.

Return to the 表 8-11.

図 8-42. HIGH_TH_CH1 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH1_MSB[7:0]							
R/W-11111111b							

表 8-38. HIGH_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH1_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.27 EVENT_COUNT_CH1 Register (Address = 0x26) [Reset = 0x0]

EVENT_COUNT_CH1 is shown in 図 8-43 and described in 表 8-39.

Return to the 表 8-11.

図 8-43. EVENT_COUNT_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_LSB[3:0]				EVENT_COUNT_CH1[3:0]			
R/W-0b				R/W-0b			

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図 8-43. EVENT_COUNT_CH1 Register (continued)

表 8-39. EVENT_COUNT_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH1_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH1[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.28 LOW_TH_CH1 Register (Address = 0x27) [Reset = 0x0]

LOW_TH_CH1 is shown in 図 8-44 and described in 表 8-40.

Return to the 表 8-11.

図 8-44. LOW_TH_CH1 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH1_MSB[7:0]							
R/W-0b							

表 8-40. LOW_TH_CH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH1_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.29 HYSTERESIS_CH2 Register (Address = 0x28) [Reset = 0xF0]

HYSTERESIS_CH2 is shown in 図 8-45 and described in 表 8-41.

Return to the 表 8-11.

図 8-45. HYSTERESIS_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_LSB[3:0]				HYSTERESIS_CH2[3:0]			
R/W-1111b				R/W-0b			

表 8-41. HYSTERESIS_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH2_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH2[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.30 HIGH_TH_CH2 Register (Address = 0x29) [Reset = 0xFF]

HIGH_TH_CH2 is shown in 図 8-46 and described in 表 8-42.

Return to the 表 8-11.

図 8-46. HIGH_TH_CH2 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH2_MSB[7:0]							
R/W-11111111b							

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図 8-46. HIGH_TH_CH2 Register (continued)

表 8-42. HIGH_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH2_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.31 EVENT_COUNT_CH2 Register (Address = 0x2A) [Reset = 0x0]

EVENT_COUNT_CH2 is shown in 図 8-47 and described in 表 8-43.

Return to the 表 8-11.

図 8-47. EVENT_COUNT_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_LSB[3:0]				EVENT_COUNT_CH2[3:0]			
R/W-0b				R/W-0b			

表 8-43. EVENT_COUNT_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH2_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH2[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.32 LOW_TH_CH2 Register (Address = 0x2B) [Reset = 0x0]

LOW_TH_CH2 is shown in 図 8-48 and described in 表 8-44.

Return to the 表 8-11.

図 8-48. LOW_TH_CH2 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH2_MSB[7:0]							
R/W-0b							

表 8-44. LOW_TH_CH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH2_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.33 HYSTERESIS_CH3 Register (Address = 0x2C) [Reset = 0xF0]

HYSTERESIS_CH3 is shown in 図 8-49 and described in 表 8-45.

Return to the 表 8-11.

図 8-49. HYSTERESIS_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_LSB[3:0]				HYSTERESIS_CH3[3:0]			
R/W-1111b				R/W-0b			

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表 8-45. HYSTERESIS_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH3_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH3[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.34 HIGH_TH_CH3 Register (Address = 0x2D) [Reset = 0xFF]

HIGH_TH_CH3 is shown in 図 8-50 and described in 表 8-46.

Return to the 表 8-11.

図 8-50. HIGH_TH_CH3 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH3_MSB[7:0]							
R/W-11111111b							

表 8-46. HIGH_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH3_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.35 EVENT_COUNT_CH3 Register (Address = 0x2E) [Reset = 0x0]

EVENT_COUNT_CH3 is shown in 図 8-51 and described in 表 8-47.

Return to the 表 8-11.

図 8-51. EVENT_COUNT_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_LSB[3:0]				EVENT_COUNT_CH3[3:0]			
R/W-0b				R/W-0b			

表 8-47. EVENT_COUNT_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH3_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH3[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.36 LOW_TH_CH3 Register (Address = 0x2F) [Reset = 0x0]

LOW_TH_CH3 is shown in 図 8-52 and described in 表 8-48.

Return to the 表 8-11.

図 8-52. LOW_TH_CH3 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH3_MSB[7:0]							
R/W-0b							

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表 8-48. LOW_TH_CH3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH3_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.37 HYSTERESIS_CH4 Register (Address = 0x30) [Reset = 0xF0]

HYSTERESIS_CH4 is shown in 図 8-53 and described in 表 8-49.

Return to the 表 8-11.

図 8-53. HYSTERESIS_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_LSB[3:0]				HYSTERESIS_CH4[3:0]			
R/W-1111b				R/W-0b			

表 8-49. HYSTERESIS_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH4_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH4[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.38 HIGH_TH_CH4 Register (Address = 0x31) [Reset = 0xFF]

HIGH_TH_CH4 is shown in 図 8-54 and described in 表 8-50.

Return to the 表 8-11.

図 8-54. HIGH_TH_CH4 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH4_MSB[7:0]							
R/W-11111111b							

表 8-50. HIGH_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH4_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.39 EVENT_COUNT_CH4 Register (Address = 0x32) [Reset = 0x0]

EVENT_COUNT_CH4 is shown in 図 8-55 and described in 表 8-51.

Return to the 表 8-11.

図 8-55. EVENT_COUNT_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_LSB[3:0]				EVENT_COUNT_CH4[3:0]			
R/W-0b				R/W-0b			

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表 8-51. EVENT_COUNT_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH4_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH4[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.40 LOW_TH_CH4 Register (Address = 0x33) [Reset = 0x0]

LOW_TH_CH4 is shown in 図 8-56 and described in 表 8-52.

Return to the 表 8-11.

図 8-56. LOW_TH_CH4 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH4_MSB[7:0]							
R/W-0b							

表 8-52. LOW_TH_CH4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH4_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.41 HYSTERESIS_CH5 Register (Address = 0x34) [Reset = 0xF0]

HYSTERESIS_CH5 is shown in 図 8-57 and described in 表 8-53.

Return to the 表 8-11.

図 8-57. HYSTERESIS_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_LSB[3:0]				HYSTERESIS_CH5[3:0]			
R/W-1111b				R/W-0b			

表 8-53. HYSTERESIS_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH5_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH5[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.42 HIGH_TH_CH5 Register (Address = 0x35) [Reset = 0xFF]

HIGH_TH_CH5 is shown in 図 8-58 and described in 表 8-54.

Return to the 表 8-11.

図 8-58. HIGH_TH_CH5 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH5_MSB[7:0]							
R/W-11111111b							

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表 8-54. HIGH_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH5_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.43 EVENT_COUNT_CH5 Register (Address = 0x36) [Reset = 0x0]

EVENT_COUNT_CH5 is shown in 図 8-59 and described in 表 8-55.

Return to the 表 8-11.

図 8-59. EVENT_COUNT_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_LSB[3:0]				EVENT_COUNT_CH5[3:0]			
R/W-0b				R/W-0b			

表 8-55. EVENT_COUNT_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH5_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH5[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.44 LOW_TH_CH5 Register (Address = 0x37) [Reset = 0x0]

LOW_TH_CH5 is shown in 図 8-60 and described in 表 8-56.

Return to the 表 8-11.

図 8-60. LOW_TH_CH5 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH5_MSB[7:0]							
R/W-0b							

表 8-56. LOW_TH_CH5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH5_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.45 HYSTERESIS_CH6 Register (Address = 0x38) [Reset = 0xF0]

HYSTERESIS_CH6 is shown in 図 8-61 and described in 表 8-57.

Return to the 表 8-11.

図 8-61. HYSTERESIS_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_LSB[3:0]				HYSTERESIS_CH6[3:0]			
R/W-1111b				R/W-0b			

表 8-57. HYSTERESIS_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH6_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.

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表 8-57. HYSTERESIS_CH6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-0	HYSTERESIS_CH6[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.46 HIGH_TH_CH6 Register (Address = 0x39) [Reset = 0xFF]

HIGH_TH_CH6 is shown in 図 8-62 and described in 表 8-58.

Return to the 表 8-11.

図 8-62. HIGH_TH_CH6 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH6_MSB[7:0]							
R/W-11111111b							

表 8-58. HIGH_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH6_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.47 EVENT_COUNT_CH6 Register (Address = 0x3A) [Reset = 0x0]

EVENT_COUNT_CH6 is shown in 図 8-63 and described in 表 8-59.

Return to the 表 8-11.

図 8-63. EVENT_COUNT_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_LSB[3:0]				EVENT_COUNT_CH6[3:0]			
R/W-0b				R/W-0b			

表 8-59. EVENT_COUNT_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH6_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH6[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.48 LOW_TH_CH6 Register (Address = 0x3B) [Reset = 0x0]

LOW_TH_CH6 is shown in 図 8-64 and described in 表 8-60.

Return to the 表 8-11.

図 8-64. LOW_TH_CH6 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH6_MSB[7:0]							
R/W-0b							

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表 8-60. LOW_TH_CH6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH6_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.49 HYSTERESIS_CH7 Register (Address = 0x3C) [Reset = 0xF0]

HYSTERESIS_CH7 is shown in 図 8-65 and described in 表 8-61.

Return to the 表 8-11.

図 8-65. HYSTERESIS_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_LSB[3:0]				HYSTERESIS_CH7[3:0]			
R/W-1111b				R/W-0b			

表 8-61. HYSTERESIS_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	HIGH_THRESHOLD_CH7_LSB[3:0]	R/W	1111b	Lower 4-bits of high threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	HYSTERESIS_CH7[3:0]	R/W	0b	4-bit hysteresis for high and low thresholds. This 4-bit hysteris is left shifted 3 times and applied on the lower 7-bits of the threshold. Total hysteresis = 7-bits [4-bits, 000b]

8.6.50 HIGH_TH_CH7 Register (Address = 0x3D) [Reset = 0xFF]

HIGH_TH_CH7 is shown in 図 8-66 and described in 表 8-62.

Return to the 表 8-11.

図 8-66. HIGH_TH_CH7 Register

7	6	5	4	3	2	1	0
HIGH_THRESHOLD_CH7_MSB[7:0]							
R/W-11111111b							

表 8-62. HIGH_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HIGH_THRESHOLD_CH7_MSB[7:0]	R/W	11111111b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.51 EVENT_COUNT_CH7 Register (Address = 0x3E) [Reset = 0x0]

EVENT_COUNT_CH7 is shown in 図 8-67 and described in 表 8-63.

Return to the 表 8-11.

図 8-67. EVENT_COUNT_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_LSB[3:0]				EVENT_COUNT_CH7[3:0]			
R/W-0b				R/W-0b			

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表 8-63. EVENT_COUNT_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	LOW_THRESHOLD_CH7_LSB[3:0]	R/W	0b	Lower 4-bits of low threshold for analog input. These bits are compared with bits 3:0 of ADC conversion result.
3-0	EVENT_COUNT_CH7[3:0]	R/W	0b	Configuration for checking 'n+1' consecutive samples above threshold before setting event flag.

8.6.52 LOW_TH_CH7 Register (Address = 0x3F) [Reset = 0x0]

LOW_TH_CH7 is shown in 図 8-68 and described in 表 8-64.

Return to the 表 8-11.

図 8-68. LOW_TH_CH7 Register

7	6	5	4	3	2	1	0
LOW_THRESHOLD_CH7_MSB[7:0]							
R/W-0b							

表 8-64. LOW_TH_CH7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LOW_THRESHOLD_CH7_MSB[7:0]	R/W	0b	MSB aligned high threshold for analog input. These bits are compared with top 8 bits of ADC conversion result.

8.6.53 MAX_CH0_LSB Register (Address = 0x60) [Reset = 0x0]

MAX_CH0_LSB is shown in 図 8-69 and described in 表 8-65.

Return to the 表 8-11.

図 8-69. MAX_CH0_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_LSB[7:0]							
R-0b							

表 8-65. MAX_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.54 MAX_CH0_MSB Register (Address = 0x61) [Reset = 0x0]

MAX_CH0_MSB is shown in 図 8-70 and described in 表 8-66.

Return to the 表 8-11.

図 8-70. MAX_CH0_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH0_MSB[7:0]							
R-0b							

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表 8-66. MAX_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH0_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.55 MAX_CH1_LSB Register (Address = 0x62) [Reset = 0x0]

MAX_CH1_LSB is shown in 図 8-71 and described in 表 8-67.

Return to the 表 8-11.

図 8-71. MAX_CH1_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_LSB[7:0]							
R-0b							

表 8-67. MAX_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.56 MAX_CH1_MSB Register (Address = 0x63) [Reset = 0x0]

MAX_CH1_MSB is shown in 図 8-72 and described in 表 8-68.

Return to the 表 8-11.

図 8-72. MAX_CH1_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH1_MSB[7:0]							
R-0b							

表 8-68. MAX_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH1_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.57 MAX_CH2_LSB Register (Address = 0x64) [Reset = 0x0]

MAX_CH2_LSB is shown in 図 8-73 and described in 表 8-69.

Return to the 表 8-11.

図 8-73. MAX_CH2_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_LSB[7:0]							
R-0b							

表 8-69. MAX_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

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8.6.58 MAX_CH2_MSB Register (Address = 0x65) [Reset = 0x0]

MAX_CH2_MSB is shown in 図 8-74 and described in 表 8-70.

Return to the 表 8-11.

図 8-74. MAX_CH2_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH2_MSB[7:0]							
R-0b							

表 8-70. MAX_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH2_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.59 MAX_CH3_LSB Register (Address = 0x66) [Reset = 0x0]

MAX_CH3_LSB is shown in 図 8-75 and described in 表 8-71.

Return to the 表 8-11.

図 8-75. MAX_CH3_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_LSB[7:0]							
R-0b							

表 8-71. MAX_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.60 MAX_CH3_MSB Register (Address = 0x67) [Reset = 0x0]

MAX_CH3_MSB is shown in 図 8-76 and described in 表 8-72.

Return to the 表 8-11.

図 8-76. MAX_CH3_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH3_MSB[7:0]							
R-0b							

表 8-72. MAX_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH3_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.61 MAX_CH4_LSB Register (Address = 0x68) [Reset = 0x0]

MAX_CH4_LSB is shown in 図 8-77 and described in 表 8-73.

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図 8-77. MAX_CH4_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_LSB[7:0]							
R-0b							

表 8-73. MAX_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.62 MAX_CH4_MSB Register (Address = 0x69) [Reset = 0x0]

MAX_CH4_MSB is shown in 図 8-78 and described in 表 8-74.

Return to the 表 8-11.

図 8-78. MAX_CH4_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH4_MSB[7:0]							
R-0b							

表 8-74. MAX_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH4_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.63 MAX_CH5_LSB Register (Address = 0x6A) [Reset = 0x0]

MAX_CH5_LSB is shown in 図 8-79 and described in 表 8-75.

Return to the 表 8-11.

図 8-79. MAX_CH5_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_LSB[7:0]							
R-0b							

表 8-75. MAX_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.64 MAX_CH5_MSB Register (Address = 0x6B) [Reset = 0x0]

MAX_CH5_MSB is shown in 図 8-80 and described in 表 8-76.

Return to the 表 8-11.

図 8-80. MAX_CH5_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH5_MSB[7:0]							
R-0b							

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表 8-76. MAX_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH5_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.65 MAX_CH6_LSB Register (Address = 0x6C) [Reset = 0x0]

MAX_CH6_LSB is shown in 図 8-81 and described in 表 8-77.

Return to the 表 8-11.

図 8-81. MAX_CH6_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_LSB[7:0]							
R-0b							

表 8-77. MAX_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.66 MAX_CH6_MSB Register (Address = 0x6D) [Reset = 0x0]

MAX_CH6_MSB is shown in 図 8-82 and described in 表 8-78.

Return to the 表 8-11.

図 8-82. MAX_CH6_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH6_MSB[7:0]							
R-0b							

表 8-78. MAX_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH6_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.67 MAX_CH7_LSB Register (Address = 0x6E) [Reset = 0x0]

MAX_CH7_LSB is shown in 図 8-83 and described in 表 8-79.

Return to the 表 8-11.

図 8-83. MAX_CH7_LSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_LSB[7:0]							
R-0b							

表 8-79. MAX_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_LSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

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8.6.68 MAX_CH7_MSB Register (Address = 0x6F) [Reset = 0x0]

MAX_CH7_MSB is shown in 図 8-84 and described in 表 8-80.

Return to the 表 8-11.

図 8-84. MAX_CH7_MSB Register

7	6	5	4	3	2	1	0
MAX_VALUE_CH7_MSB[7:0]							
R-0b							

表 8-80. MAX_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAX_VALUE_CH7_MSB[7:0]	R	0b	Maximum code recorded on analog input channel from the last time this register was read. Reading the register resets the value to 0.

8.6.69 MIN_CH0_LSB Register (Address = 0x80) [Reset = 0xFF]

MIN_CH0_LSB is shown in 図 8-85 and described in 表 8-81.

Return to the 表 8-11.

図 8-85. MIN_CH0_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_LSB[7:0]							
R-11111111b							

表 8-81. MIN_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.70 MIN_CH0_MSB Register (Address = 0x81) [Reset = 0xFF]

MIN_CH0_MSB is shown in 図 8-86 and described in 表 8-82.

Return to the 表 8-11.

図 8-86. MIN_CH0_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH0_MSB[7:0]							
R-11111111b							

表 8-82. MIN_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH0_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.71 MIN_CH1_LSB Register (Address = 0x82) [Reset = 0xFF]

MIN_CH1_LSB is shown in 図 8-87 and described in 表 8-83.

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図 8-87. MIN_CH1_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_LSB[7:0]							
R-11111111b							

表 8-83. MIN_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.72 MIN_CH1_MSB Register (Address = 0x83) [Reset = 0xFF]

MIN_CH1_MSB is shown in 図 8-88 and described in 表 8-84.

Return to the 表 8-11.

図 8-88. MIN_CH1_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH1_MSB[7:0]							
R-11111111b							

表 8-84. MIN_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH1_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.73 MIN_CH2_LSB Register (Address = 0x84) [Reset = 0xFF]

MIN_CH2_LSB is shown in 図 8-89 and described in 表 8-85.

Return to the 表 8-11.

図 8-89. MIN_CH2_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_LSB[7:0]							
R-11111111b							

表 8-85. MIN_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.74 MIN_CH2_MSB Register (Address = 0x85) [Reset = 0xFF]

MIN_CH2_MSB is shown in 図 8-90 and described in 表 8-86.

Return to the 表 8-11.

図 8-90. MIN_CH2_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH2_MSB[7:0]							

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図 8-90. MIN_CH2_MSB Register (continued)

R-11111111b

表 8-86. MIN_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH2_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.75 MIN_CH3_LSB Register (Address = 0x86) [Reset = 0xFF]

MIN_CH3_LSB is shown in 図 8-91 and described in 表 8-87.

Return to the 表 8-11.

図 8-91. MIN_CH3_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_LSB[7:0]							
R-11111111b							

表 8-87. MIN_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.76 MIN_CH3_MSB Register (Address = 0x87) [Reset = 0xFF]

MIN_CH3_MSB is shown in 図 8-92 and described in 表 8-88.

Return to the 表 8-11.

図 8-92. MIN_CH3_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH3_MSB[7:0]							
R-11111111b							

表 8-88. MIN_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH3_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.77 MIN_CH4_LSB Register (Address = 0x88) [Reset = 0xFF]

MIN_CH4_LSB is shown in 図 8-93 and described in 表 8-89.

Return to the 表 8-11.

図 8-93. MIN_CH4_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_LSB[7:0]							
R-11111111b							

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表 8-89. MIN_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.78 MIN_CH4_MSB Register (Address = 0x89) [Reset = 0xFF]

MIN_CH4_MSB is shown in 図 8-94 and described in 表 8-90.

Return to the 表 8-11.

図 8-94. MIN_CH4_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH4_MSB[7:0]							
R-11111111b							

表 8-90. MIN_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH4_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.79 MIN_CH5_LSB Register (Address = 0x8A) [Reset = 0xFF]

MIN_CH5_LSB is shown in 図 8-95 and described in 表 8-91.

Return to the 表 8-11.

図 8-95. MIN_CH5_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_LSB[7:0]							
R-11111111b							

表 8-91. MIN_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.80 MIN_CH5_MSB Register (Address = 0x8B) [Reset = 0xFF]

MIN_CH5_MSB is shown in 図 8-96 and described in 表 8-92.

Return to the 表 8-11.

図 8-96. MIN_CH5_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH5_MSB[7:0]							
R-11111111b							

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表 8-92. MIN_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH5_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.81 MIN_CH6_LSB Register (Address = 0x8C) [Reset = 0xFF]

MIN_CH6_LSB is shown in 図 8-97 and described in 表 8-93.

Return to the 表 8-11.

図 8-97. MIN_CH6_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_LSB[7:0]							
R-11111111b							

表 8-93. MIN_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.82 MIN_CH6_MSB Register (Address = 0x8D) [Reset = 0xFF]

MIN_CH6_MSB is shown in 図 8-98 and described in 表 8-94.

Return to the 表 8-11.

図 8-98. MIN_CH6_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH6_MSB[7:0]							
R-11111111b							

表 8-94. MIN_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH6_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.83 MIN_CH7_LSB Register (Address = 0x8E) [Reset = 0xFF]

MIN_CH7_LSB is shown in 図 8-99 and described in 表 8-95.

Return to the 表 8-11.

図 8-99. MIN_CH7_LSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_LSB[7:0]							
R-11111111b							

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表 8-95. MIN_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_LSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.84 MIN_CH7_MSB Register (Address = 0x8F) [Reset = 0xFF]

MIN_CH7_MSB is shown in 図 8-100 and described in 表 8-96.

Return to the 表 8-11.

図 8-100. MIN_CH7_MSB Register

7	6	5	4	3	2	1	0
MIN_VALUE_CH7_MSB[7:0]							
R-11111111b							

表 8-96. MIN_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MIN_VALUE_CH7_MSB[7:0]	R	11111111b	Minimum code recorded on the analog input channel from the last time this register was read. Reading the register resets the value to 0xFF.

8.6.85 RECENT_CH0_LSB Register (Address = 0xA0) [Reset = 0x0]

RECENT_CH0_LSB is shown in 図 8-101 and described in 表 8-97.

Return to the 表 8-11.

図 8-101. RECENT_CH0_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_LSB[7:0]							
R-0b							

表 8-97. RECENT_CH0_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.86 RECENT_CH0_MSB Register (Address = 0xA1) [Reset = 0x0]

RECENT_CH0_MSB is shown in 図 8-102 and described in 表 8-98.

Return to the 表 8-11.

図 8-102. RECENT_CH0_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH0_MSB[7:0]							
R-0b							

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表 8-98. RECENT_CH0_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH0_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.87 RECENT_CH1_LSB Register (Address = 0xA2) [Reset = 0x0]

RECENT_CH1_LSB is shown in 図 8-103 and described in 表 8-99.

Return to the 表 8-11.

図 8-103. RECENT_CH1_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_LSB[7:0]							
R-0b							

表 8-99. RECENT_CH1_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.88 RECENT_CH1_MSB Register (Address = 0xA3) [Reset = 0x0]

RECENT_CH1_MSB is shown in 図 8-104 and described in 表 8-100.

Return to the 表 8-11.

図 8-104. RECENT_CH1_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH1_MSB[7:0]							
R-0b							

表 8-100. RECENT_CH1_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH1_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.89 RECENT_CH2_LSB Register (Address = 0xA4) [Reset = 0x0]

RECENT_CH2_LSB is shown in 図 8-105 and described in 表 8-101.

Return to the 表 8-11.

図 8-105. RECENT_CH2_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_LSB[7:0]							
R-0b							

表 8-101. RECENT_CH2_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

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8.6.90 RECENT_CH2_MSB Register (Address = 0xA5) [Reset = 0x0]

RECENT_CH2_MSB is shown in 図 8-106 and described in 表 8-102.

Return to the 表 8-11.

図 8-106. RECENT_CH2_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH2_MSB[7:0]							
R-0b							

表 8-102. RECENT_CH2_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH2_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.91 RECENT_CH3_LSB Register (Address = 0xA6) [Reset = 0x0]

RECENT_CH3_LSB is shown in 図 8-107 and described in 表 8-103.

Return to the 表 8-11.

図 8-107. RECENT_CH3_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_LSB[7:0]							
R-0b							

表 8-103. RECENT_CH3_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.92 RECENT_CH3_MSB Register (Address = 0xA7) [Reset = 0x0]

RECENT_CH3_MSB is shown in 図 8-108 and described in 表 8-104.

Return to the 表 8-11.

図 8-108. RECENT_CH3_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH3_MSB[7:0]							
R-0b							

表 8-104. RECENT_CH3_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH3_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.93 RECENT_CH4_LSB Register (Address = 0xA8) [Reset = 0x0]

RECENT_CH4_LSB is shown in 図 8-109 and described in 表 8-105.

Return to the 表 8-11.

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図 8-109. RECENT_CH4_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_LSB[7:0]							
R-0b							

表 8-105. RECENT_CH4_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.94 RECENT_CH4_MSB Register (Address = 0xA9) [Reset = 0x0]

RECENT_CH4_MSB is shown in 図 8-110 and described in 表 8-106.

Return to the 表 8-11.

図 8-110. RECENT_CH4_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH4_MSB[7:0]							
R-0b							

表 8-106. RECENT_CH4_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH4_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.95 RECENT_CH5_LSB Register (Address = 0xAA) [Reset = 0x0]

RECENT_CH5_LSB is shown in 図 8-111 and described in 表 8-107.

Return to the 表 8-11.

図 8-111. RECENT_CH5_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_LSB[7:0]							
R-0b							

表 8-107. RECENT_CH5_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.96 RECENT_CH5_MSB Register (Address = 0xAB) [Reset = 0x0]

RECENT_CH5_MSB is shown in 図 8-112 and described in 表 8-108.

Return to the 表 8-11.

図 8-112. RECENT_CH5_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH5_MSB[7:0]							
R-0b							

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表 8-108. RECENT_CH5_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH5_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.97 RECENT_CH6_LSB Register (Address = 0xAC) [Reset = 0x0]

RECENT_CH6_LSB is shown in 図 8-113 and described in 表 8-109.

Return to the 表 8-11.

図 8-113. RECENT_CH6_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_LSB[7:0]							
R-0b							

表 8-109. RECENT_CH6_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

8.6.98 RECENT_CH6_MSB Register (Address = 0xAD) [Reset = 0x0]

RECENT_CH6_MSB is shown in 図 8-114 and described in 表 8-110.

Return to the 表 8-11.

図 8-114. RECENT_CH6_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH6_MSB[7:0]							
R-0b							

表 8-110. RECENT_CH6_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH6_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.99 RECENT_CH7_LSB Register (Address = 0xAE) [Reset = 0x0]

RECENT_CH7_LSB is shown in 図 8-115 and described in 表 8-111.

Return to the 表 8-11.

図 8-115. RECENT_CH7_LSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_LSB[7:0]							
R-0b							

表 8-111. RECENT_CH7_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_LSB[7:0]	R	0b	Next 8 bits of the last result for this analog input channel.

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8.6.100 RECENT_CH7_MSB Register (Address = 0xAF) [Reset = 0x0]

RECENT_CH7_MSB is shown in 図 8-116 and described in 表 8-112.

Return to the 表 8-11.

図 8-116. RECENT_CH7_MSB Register

7	6	5	4	3	2	1	0
LAST_VALUE_CH7_MSB[7:0]							
R-0b							

表 8-112. RECENT_CH7_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LAST_VALUE_CH7_MSB[7:0]	R	0b	MSB aligned first 8 bits of the last result for this analog input channel.

8.6.101 GPO0_TRIG_EVENT_SEL Register (Address = 0xC3) [Reset = 0x2]

GPO0_TRIG_EVENT_SEL is shown in 図 8-117 and described in 表 8-113.

Return to the 表 8-11.

図 8-117. GPO0_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-113. GPO0_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO0. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO0 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO0 output.

8.6.102 GPO1_TRIG_EVENT_SEL Register (Address = 0xC5) [Reset = 0x2]

GPO1_TRIG_EVENT_SEL is shown in 図 8-118 and described in 表 8-114.

Return to the 表 8-11.

図 8-118. GPO1_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO1_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-114. GPO1_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO1_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO1. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO1 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO1 output.

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8.6.103 GPO2_TRIG_EVENT_SEL Register (Address = 0xC7) [Reset = 0x2]

GPO2_TRIG_EVENT_SEL is shown in 図 8-119 and described in 表 8-115.

Return to the 表 8-11.

図 8-119. GPO2_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO2_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-115. GPO2_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO2_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO2. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO2 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO2 output.

8.6.104 GPO3_TRIG_EVENT_SEL Register (Address = 0xC9) [Reset = 0x2]

GPO3_TRIG_EVENT_SEL is shown in 図 8-120 and described in 表 8-116.

Return to the 表 8-11.

図 8-120. GPO3_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO3_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-116. GPO3_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO3_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO3. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO3 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO3 output.

8.6.105 GPO4_TRIG_EVENT_SEL Register (Address = 0xCB) [Reset = 0x2]

GPO4_TRIG_EVENT_SEL is shown in 図 8-121 and described in 表 8-117.

Return to the 表 8-11.

図 8-121. GPO4_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO4_TRIG_EVENT_SEL[7:0]							
R/W-10b							

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表 8-117. GPO4_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO4_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO4. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO4 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO4 output.

8.6.106 GPO5_TRIG_EVENT_SEL Register (Address = 0xCD) [Reset = 0x2]

GPO5_TRIG_EVENT_SEL is shown in 図 8-122 and described in 表 8-118.

Return to the 表 8-11.

図 8-122. GPO5_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO0_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-118. GPO5_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO0_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO5. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO5 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO5 output.

8.6.107 GPO6_TRIG_EVENT_SEL Register (Address = 0xCF) [Reset = 0x2]

GPO6_TRIG_EVENT_SEL is shown in 図 8-123 and described in 表 8-119.

Return to the 表 8-11.

図 8-123. GPO6_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0
GPO6_TRIG_EVENT_SEL[7:0]							
R/W-10b							

表 8-119. GPO6_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO6_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO6. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO6 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO6 output.

8.6.108 GPO7_TRIG_EVENT_SEL Register (Address = 0xD1) [Reset = 0x2]

GPO7_TRIG_EVENT_SEL is shown in 図 8-124 and described in 表 8-120.

Return to the 表 8-11.

図 8-124. GPO7_TRIG_EVENT_SEL Register

7	6	5	4	3	2	1	0

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図 8-124. GPO7_TRIG_EVENT_SEL Register (continued)

GPO7_TRIG_EVENT_SEL[7:0]
R/W-10b

表 8-120. GPO7_TRIG_EVENT_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO7_TRIG_EVENT_SEL[7:0]	R/W	10b	Select the inputs AIN/GPIO[7:0], analog or digital, which can trigger an event based update on GPO7. 0b = Alert flags for the AIN/GPIO corresponding to this bit do not trigger GPO7 output. 1b = Alert flags for the AIN/GPIO corresponding to this bit trigger GPO7 output.

8.6.109 GPO_TRIGGER_CFG Register (Address = 0xE9) [Reset = 0x0]

GPO_TRIGGER_CFG is shown in 図 8-125 and described in 表 8-121.

Return to the 表 8-11.

図 8-125. GPO_TRIGGER_CFG Register

7	6	5	4	3	2	1	0
GPO_TRIGGER_UPDATE_EN[7:0]							
R/W-0b							

表 8-121. GPO_TRIGGER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_TRIGGER_UPDATE_EN[7:0]	R/W	0b	Update digital outputs GPO[7:0] when corresponding trigger is set. 0b = Digital output is not updated in response to alert flags. 1b = Digital output is updated when corresponding alert flags are set. Configure GPOx_TRIG_EVENT_SEL register to select which alert flags can trigger an update on the desired GPO.

8.6.110 GPO_VALUE_TRIG Register (Address = 0xEB) [Reset = 0x0]

GPO_VALUE_TRIG is shown in 図 8-126 and described in 表 8-122.

Return to the 表 8-11.

図 8-126. GPO_VALUE_TRIG Register

7	6	5	4	3	2	1	0
GPO_VALUE_ON_TRIGGER[7:0]							
R/W-0b							

表 8-122. GPO_VALUE_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_VALUE_ON_TRIGGER[7:0]	R/W	0b	Value to be set on digital outputs GPO[7:0] when corresponding trigger occurs. GPO update on alert flags must be enabled in corresponding bit in GPO_TRIGGER_CFG register. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

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9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections give example circuits and suggestions for using the ADS7128-Q1 in various applications.

9.2 Typical Applications

9.2.1 Mixed-Channel Configuration

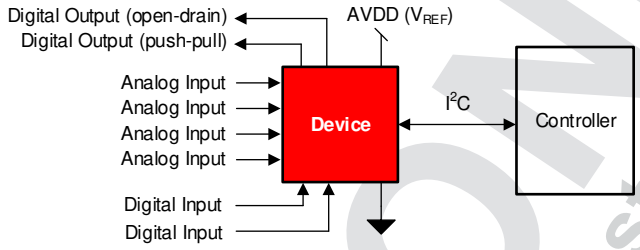


図 9-1. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of this application is to configure some channels of the ADS7138-Q1 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

9.2.1.2 Detailed Design Procedure

The ADS7138-Q1 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output though the PIN_CFG and GPIO_CFG registers; see 表 8-5.

9.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. 図 9-2 shows that the state of the digital input can be read from the GPI_VALUE register.

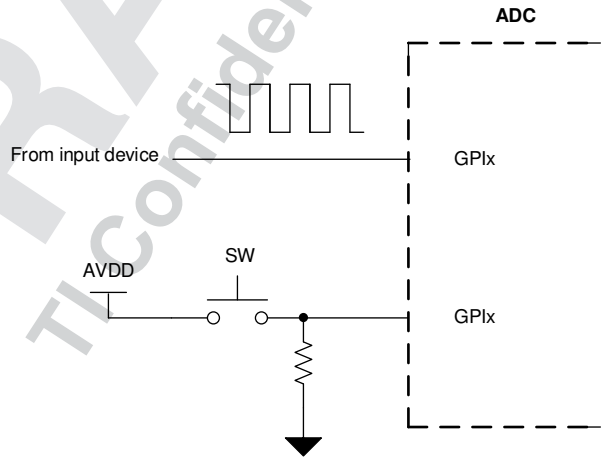


図 9-2. Digital Input

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9.2.1.2.2 Digital Open-Drain Output

The channels of the ADS7138-Q1 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in 図 9-3, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pullup resistor, R_{PULL_UP}, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pullup resistor to ground and bringing the node voltage at GPOx low.

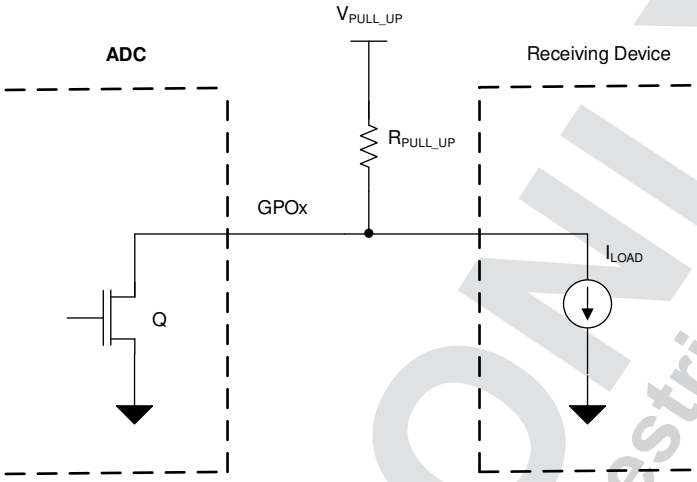


図 9-3. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in 式 3, is given by the ratio of V_{PULL_UP} and the maximum current supported by the device digital output (5 mA).

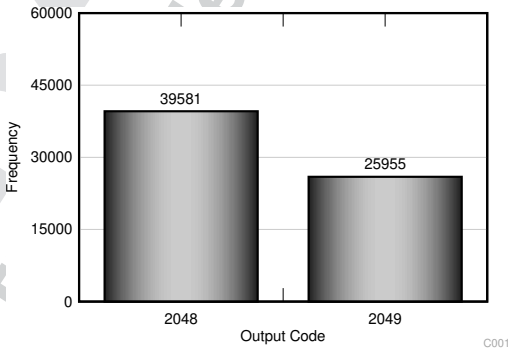
$$R_{MIN} = (V_{PULL_UP} / 5\ mA) \quad (3)$$

The maximum value of the pullup resistor, as calculated in 式 4, depends on the minimum input current requirement, I_{LOAD}, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL_UP} / I_{LOAD}) \quad (4)$$

Select R_{PULL_UP} such that $R_{MIN} < R_{PULL_UP} < R_{MAX}$.

9.2.1.3 Application Curve



Standard deviation = 0.49 LSB

図 9-4. DC Input Histogram

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9.2.2 Digital Push-Pull Output

The channels of the ADS7138-Q1 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in 図 9-5, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

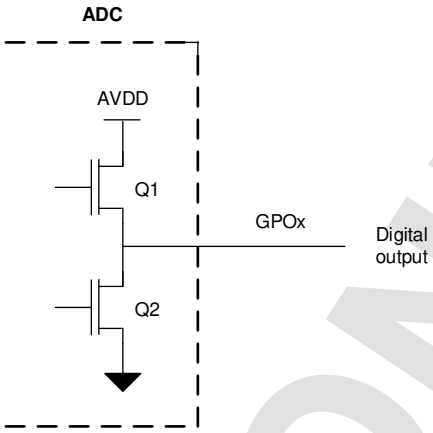


図 9-5. Digital Push-Pull Output

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The ADS7138-Q1 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in 図 10-1, with 1-µF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

Connect a 1-µF decoupling capacitor between the DECAP and GND pins for the internal power supply.

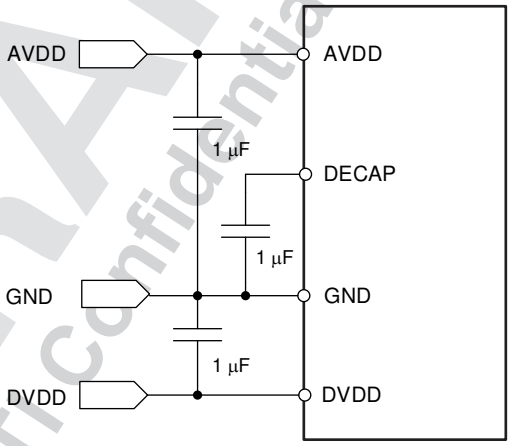


図 10-1. Power-Supply Decoupling

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11 Layout

11.1 Layout Guidelines

図 11-1 shows a board layout example for the ADS7138-Q1. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the ADS7138-Q1. Place the decoupling capacitor for AVDD close to the device AVDD and GND pins and connect the decoupling capacitor to the device pins with thick copper tracks.

11.2 Layout Example

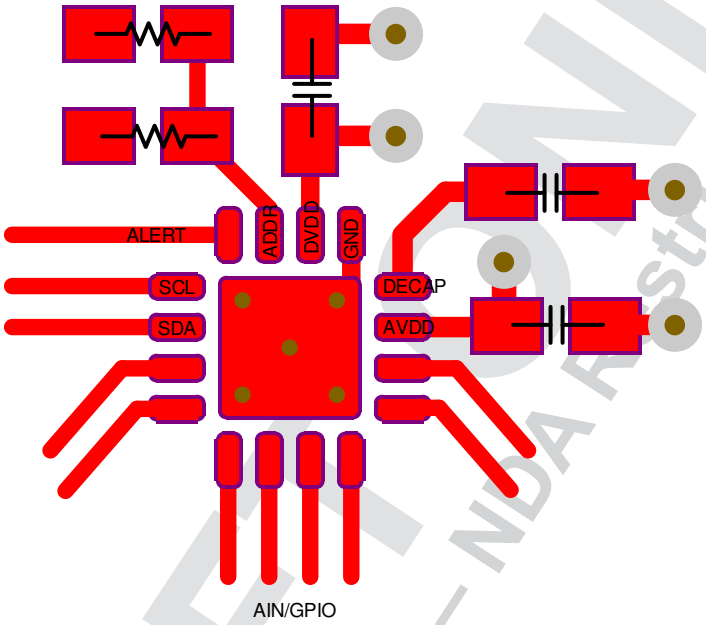


図 11-1. Example Layout

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

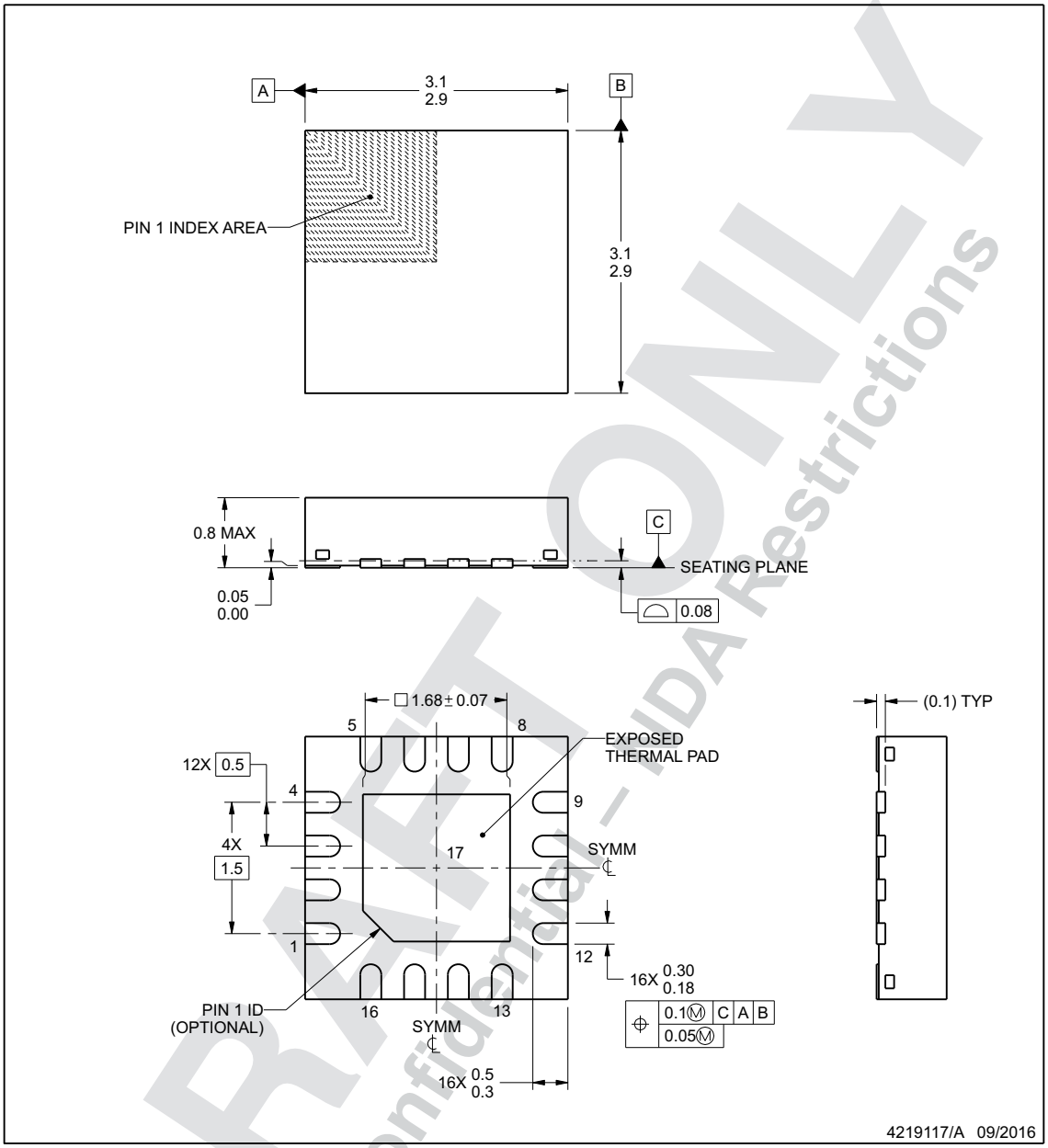
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PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

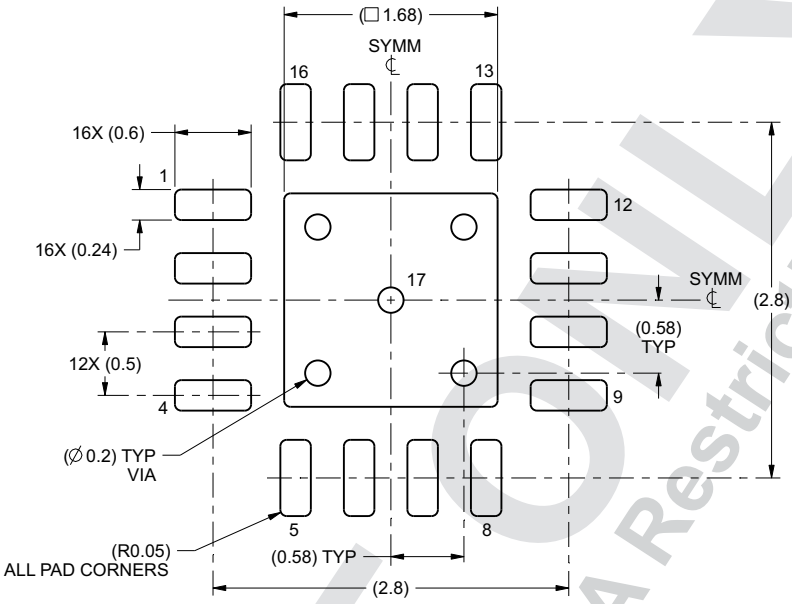
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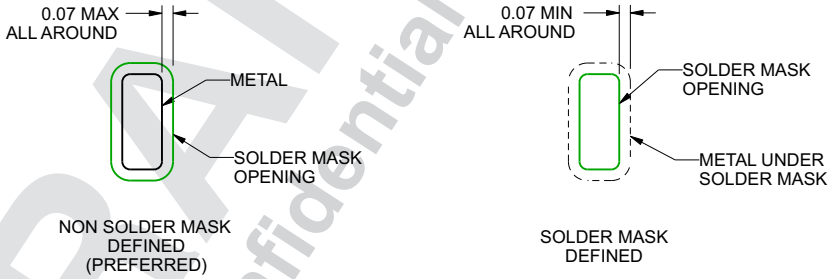
EXAMPLE BOARD LAYOUT

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219117/A 09/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

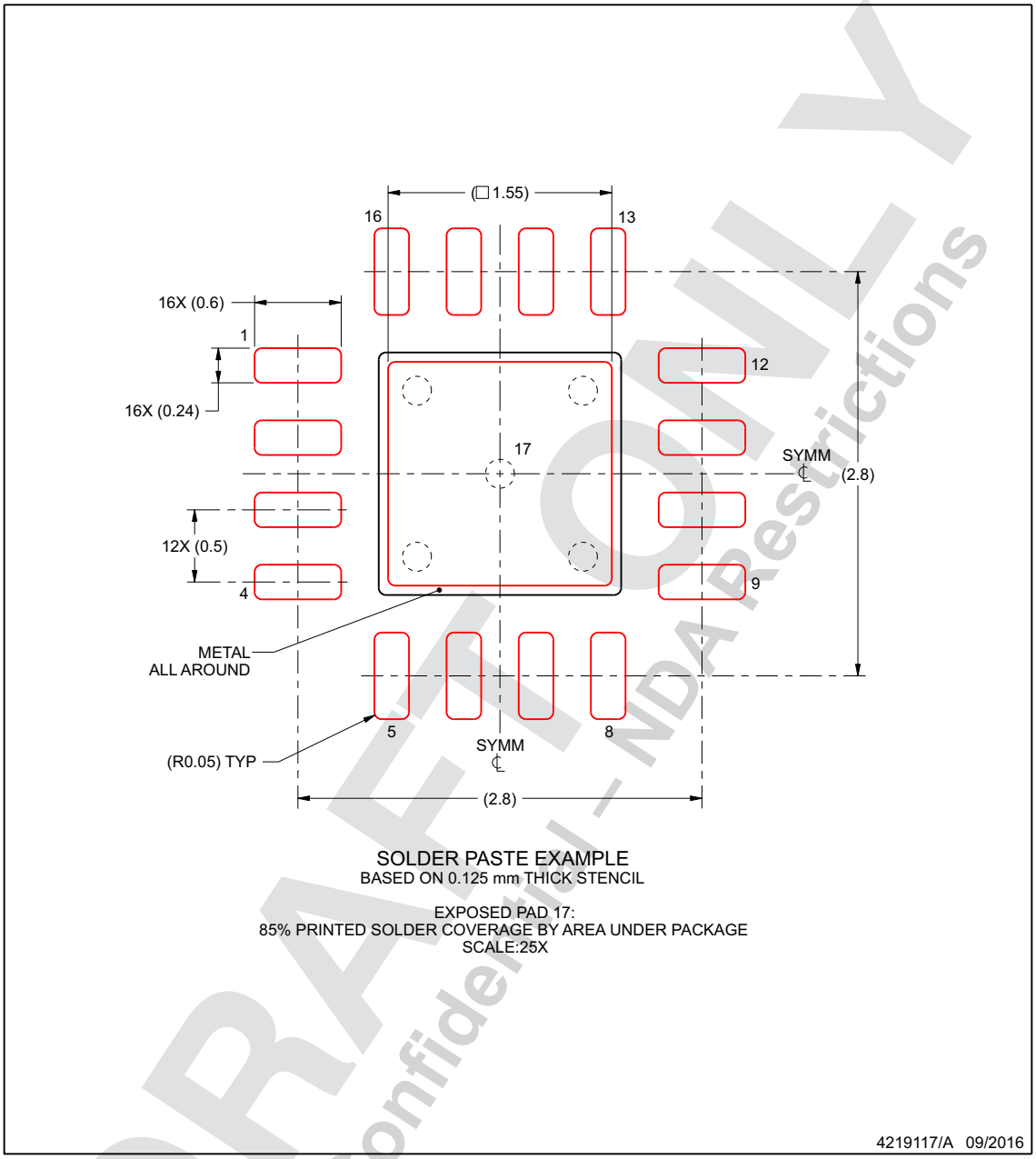
DRAFT ONLY
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EXAMPLE STENCIL DESIGN

RTE0016C — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

DRAFT ONLY
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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS7138QRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7138Q
ADS7138QRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7138Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS7138-Q1 :

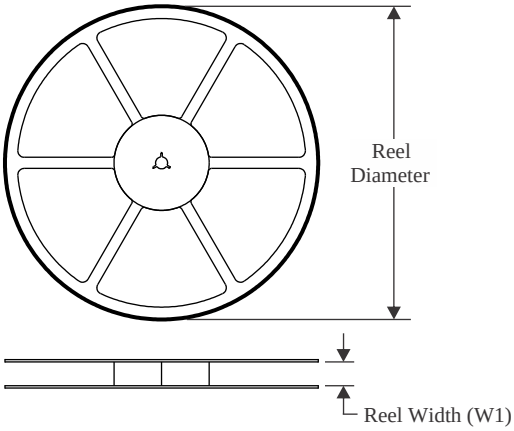
- Catalog : ADS7138

NOTE: Qualified Version Definitions:

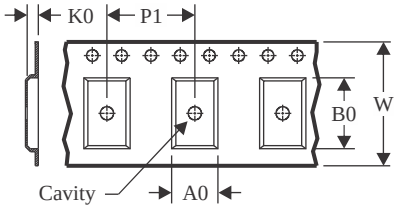
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

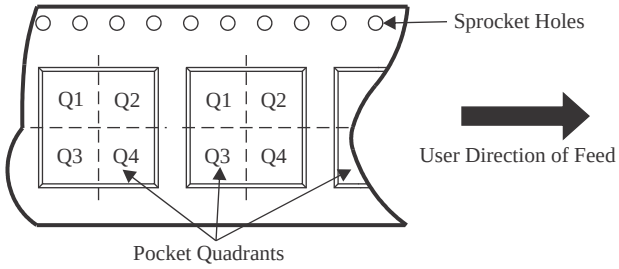


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

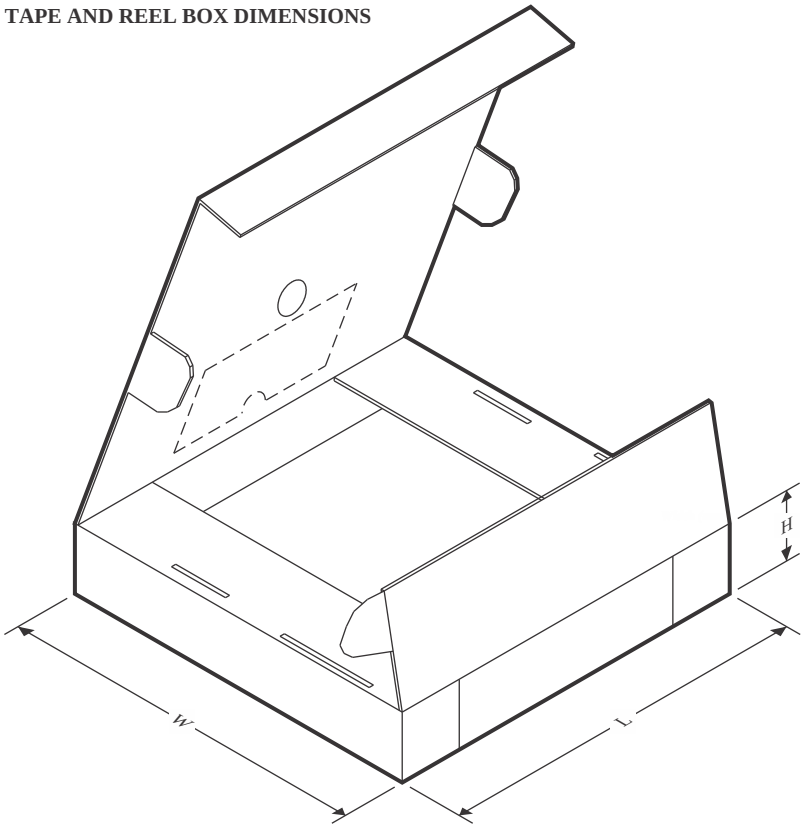
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7138QRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7138QRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

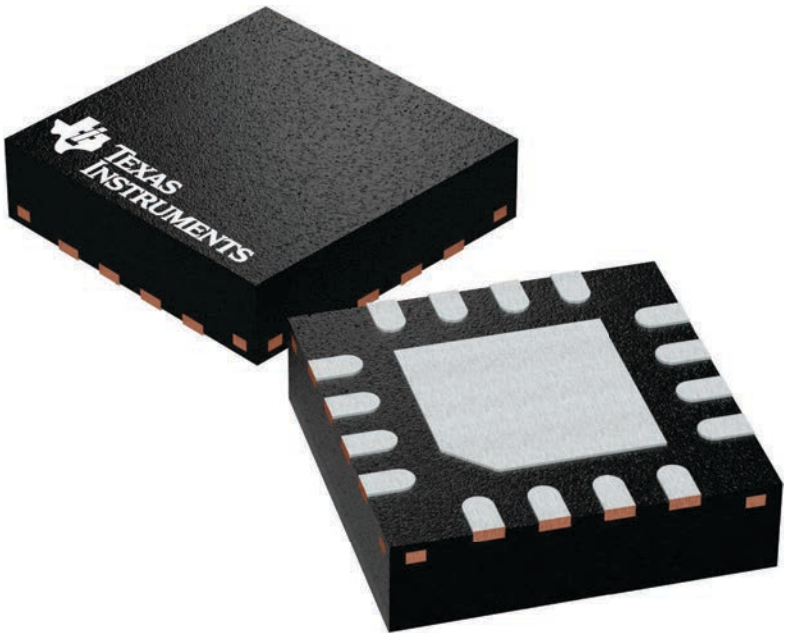
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

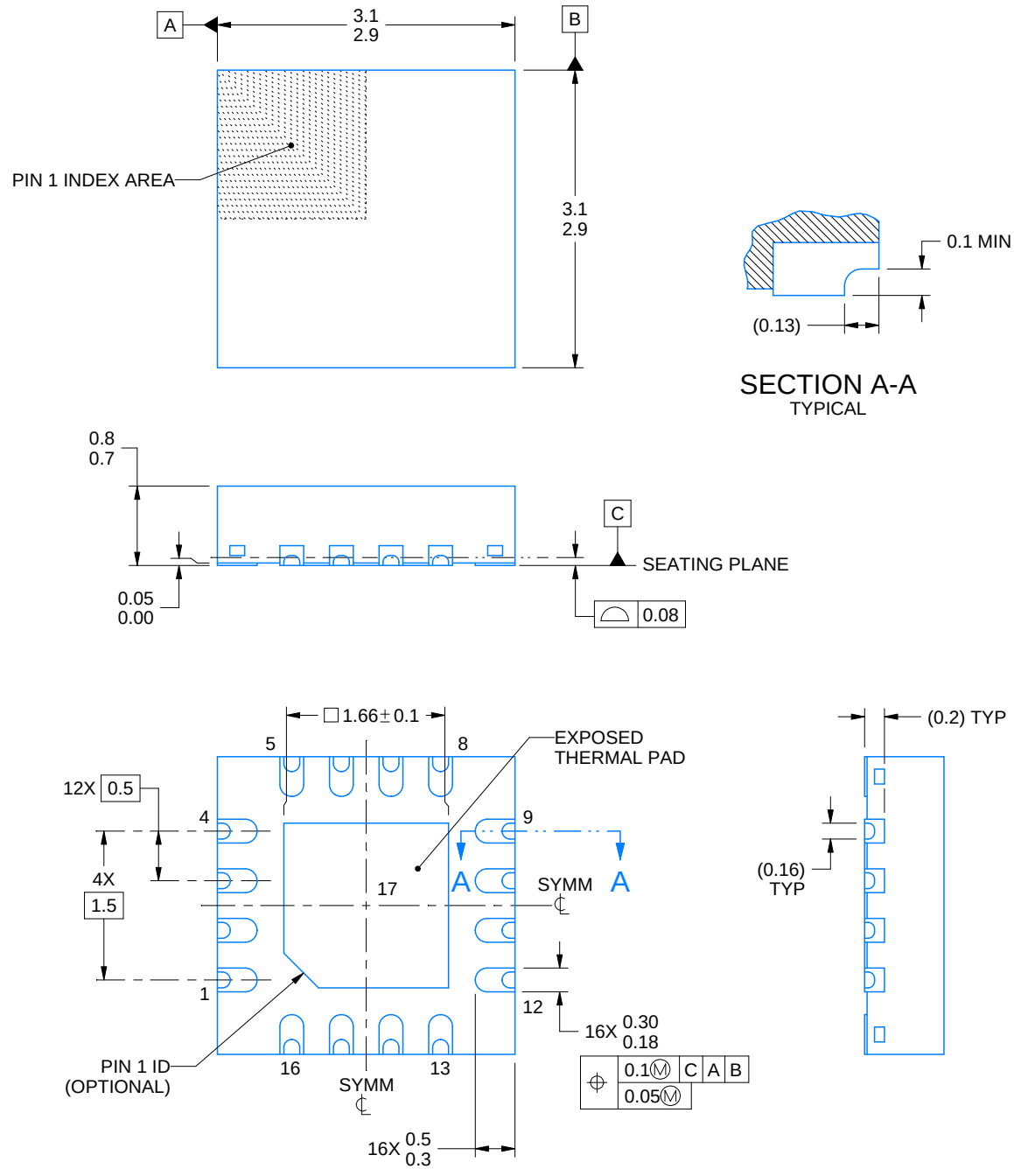


RTE0016K

PACKAGE OUTLINE

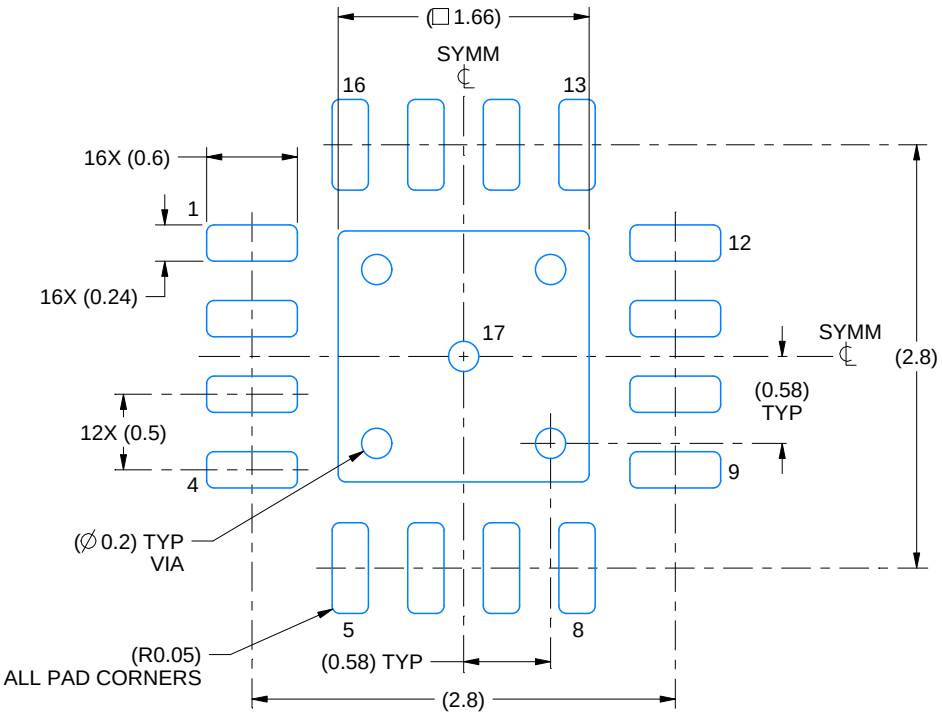
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

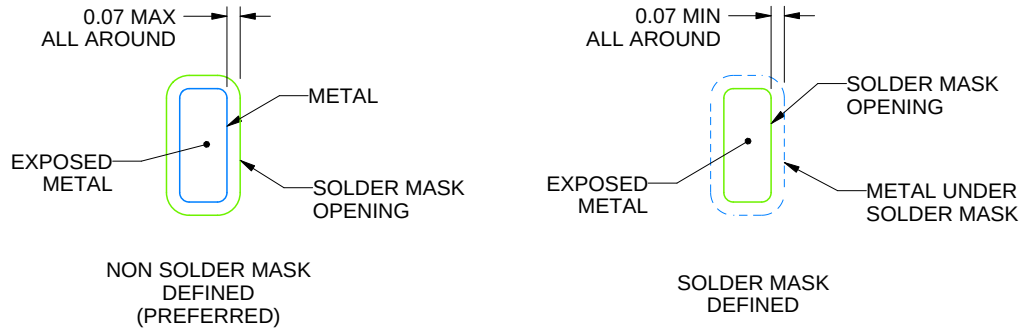


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

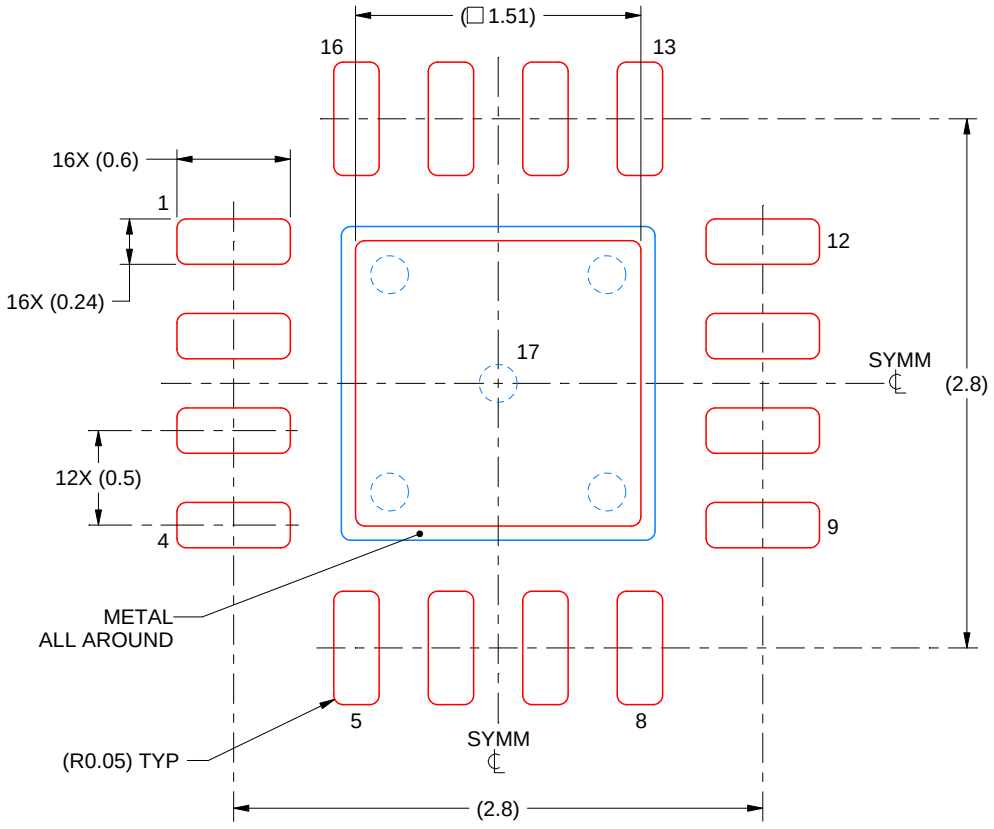


SOLDER MASK DETAILS

4224938/C 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月