ADS8586S 16ビット、高速、6チャネル同時サンプリングADC、単一電源によるバイポーラ入力

1 特長

- アナログ・フロントエンドが内蔵された16ビットADC
- 6チャネルを同時にサンプリング
- ピンでプログラム可能なバイポーラ入力: ±10Vおよび±5V
- 高い入力インピーダンス: 1MΩ
- 5Vアナログ電源: 2.3V～5Vのデジタル電源
- 7kV ESDの過電圧入力クランプ
- 低ドリフト係数のオンチップ基準電圧(2.5V)およびバッファ
- 優れた性能
  - チャネルごとに最大250kSPSのスループット
  - DNL: ±0.35LSB、INL: ±0.45LSB
  - SNR: 96.4dB、THD: −114dB
- 温度性能
  - 最大オフセット・ドリフト: 3ppm/℃
  - ゲイン・ドリフト: 6ppm/℃
- オンチップのデジタル・フィルタによるオーバーサンプリング
- 柔軟なパラレル、バイト、シリアル・インターフェイス
- 温度範囲: -40°C～+125°C
- パッケージ: 64ピンLQFP

2 アプリケーション

- 電力網の監視および制御
- 保護リレー
- マルチフェーズ・モータ制御
- 産業用自動化および制御
- マルチチャネル・データ収集システム

3 概要

ADS8586Sデバイスは 6チャネルの統合データ収集(DAQ)システムで、チャネルごとに最大250kSPSで動作する、同時サンプリング、16ビットの逐次比較型(SAR)アナログ/デジタル・コンバータ(ADC)を基礎としています。デバイスには、チャネルごとに完全なアナログ・フロントエンドが搭載されており、高い入力インピーダンス(1MΩ)を持つプログラム可能なゲイン・アンプ(PGA)、入力クランプ、ローパス・フィルタ、ADC入力ドライバが内蔵されています。デバイスには、低ドリフト係数の高精度基準電圧も内蔵され、ADCを駆動するためのバッファも搭載されています。柔軟なデジタル・インターフェイスはシリアル、パラレル、およびパラレル・バイト通信をサポートするため、デバイスを各種のホスト・コントローラとともに使用できます。

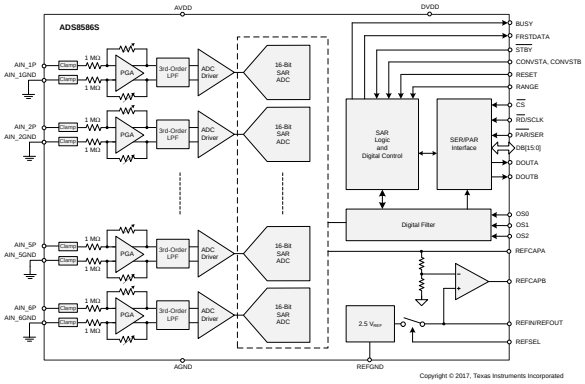
ADS8586Sは、単一の5V電源を使用して、±10Vまたは±5Vの真のバイポーラ入力を受け付けるように構成できます。入力インピーダンスが高いため、センサや変圧器と直接接続でき、外付けのドライバ回路が必要ありません。高い性能と精度に加え、レイテンシなしで変換が行われるため、ADS8586Sは多くの産業自動化および制御アプリケーションに優れた選択肢です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADS8586S	LQFP (64)	10.00mm×10.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

ブロック概略図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年4月発行のものから更新 **Page**

- ドキュメントをADS8588S (SBAS642)から分離、ドキュメントの状態を「事前情報」から「量産データ」へ 変更 ... 1
- Changed minimum specification from –96 to –64 in last row of external reference for E_G parameter ... 7

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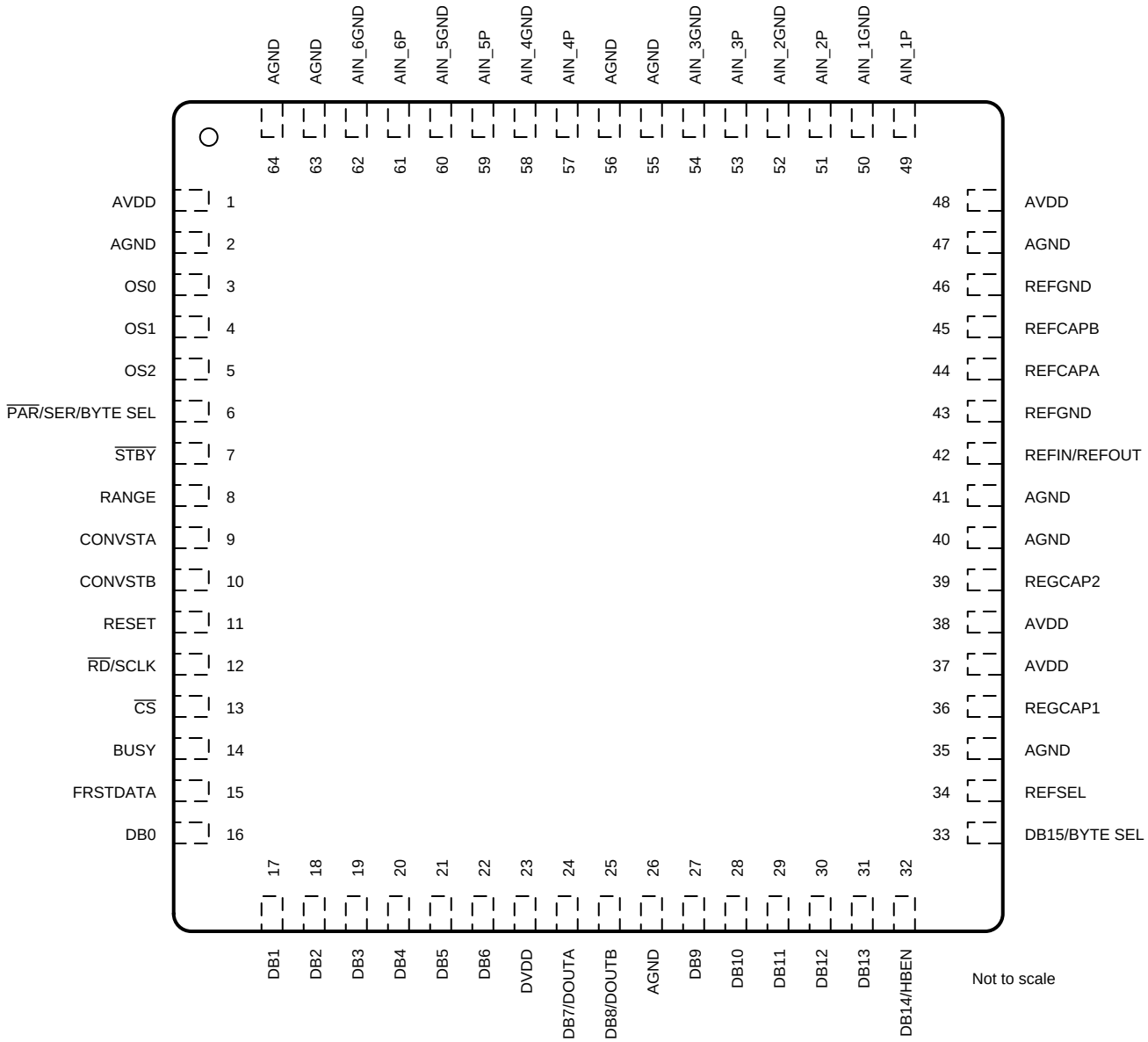
5 Device Family Comparison Table

PRODUCT	RESOLUTION (Bits)	CHANNELS	SAMPLE RATE (kSPS)
ADS8588S	16	8, single-ended	200
ADS8586S	16	6, single-ended	250
ADS8584S	16	4, single-ended	330
ADS8578S	14	8, single-ended	200

6 Pin Configuration and Functions

PM Package: ADS8586S
64-Pin LQFP
Top View



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Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	2, 26, 35, 40, 41, 47	P	Analog ground pins
AGND	55, 56, 63, 64	AI	Analog ground pins
AIN_1GND	50	AI	Analog input channel 1: negative input
AIN_1P	49	AI	Analog input channel 1: positive input
AIN_2GND	52	AI	Analog input channel 2: negative input
AIN_2P	51	AI	Analog input channel 2: positive input
AIN_3GND	54	AI	Analog input channel 3: negative input
AIN_3P	53	AI	Analog input channel 3: positive input
AIN_4GND	58	AI	Analog input channel 4: negative input
AIN_4P	57	AI	Analog input channel 4: positive input
AIN_5GND	60	AI	Analog input channel 5: negative input
AIN_5P	59	AI	Analog input channel 5: positive input
AIN_6GND	62	AI	Analog input channel 6: negative input
AIN_6P	61	AI	Analog input channel 6: positive input
AVDD	1, 37, 38, 48	P	Analog supply pins. Decouple these pins to the closest AGND pins (see the *Power Supply Recommendations* section)
BUSY	14	DO	Active high digital output indicating ongoing conversion (see the *BUSY (Output)* section)
CONVSTA	9	DI	Active high logic input to control start of conversion for first half count of device input channels (see the *CONVSTA, CONVSTB (Input)* section)
CONVSTB	10	DI	Active high logic input to control start of conversion for second half count of device input channels (see the *CONVSTA, CONVSTB (Input)* section)
$\overline{CS}$	13	DI	Active low logic input chip-select signal (see the *CS (Input)* section)
DB0	16	DO	Data output DB0 (LSB) in parallel interface mode (see the *DB[6:0]* section)
DB1	17	DO	Data output DB1 in parallel interface mode (see the *DB[6:0]* section)
DB2	18	DO	Data output DB2 in parallel interface mode (see the *DB[6:0]* section)
DB3	19	DO	Data output DB3 in parallel interface mode (see the *DB[6:0]* section)
DB4	20	DO	Data output DB4 in parallel interface mode (see the *DB[6:0]* section)
DB5	21	DO	Data output DB5 in parallel interface mode (see the *DB[6:0]* section)
DB6	22	DO	Data output DB6 in parallel interface mode (see the *DB[6:0]* section)
DB7/DOUTA	24	DO	Multi-function logic output pin (see the *DB7/DOUTA* section): this pin is data output DB7 in parallel and parallel byte interface mode; this pin is a data output pin in serial interface mode.
DB8/DOUTB	25	DO	Multi-function logic output pin (see the *DB8/DOUTB* section): this pin is data output DB8 in parallel interface mode; this pin is a data output pin in serial interface mode.
DB9	27	DO	Data output DB9 in parallel interface mode (see the *DB[13:9]* section)
DB10	28	DO	Data output DB10 in parallel interface mode (see the *DB[13:9]* section)
DB11	29	DO	Data output DB11 in parallel interface mode (see the *DB[13:9]* section)
DB12	30	DO	Data output DB12 in parallel interface mode (see the *DB[13:9]* section)
DB13	31	DO	Data output DB13 in parallel interface mode (see the *DB[13:9]* section)
DB14/HBEN	32	DIO	Multi-function logic input or output pin (see the *DB14/HBEN* section): this pin is data output DB14 in parallel interface mode; this pin is a control input pin for byte selection (high or low) in parallel byte interface mode
DB15/BYTE SEL	33	DIO	Multi-function logic input or output pin (see the *DB15/BYTE SEL* section): this pin is data output DB15 (MSB) in parallel interface mode; this pin is an active high control input pin to enable parallel byte interface mode.
DVDD	23	P	Digital supply pin; decouple with AGND on pin 26.
FRSTDATA	15	DO	Active high digital output indicating data read back from channel 1 of the device (see the *FRSTDATA (Output)* section)
OS0	3	DI	Oversampling mode control pin (see the *Oversampling Mode of Operation* section)
OS1	4	DI	Oversampling mode control pin (see the *Oversampling Mode of Operation* section)

(1) AI = analog input; AO = analog output; AIO = analog input/output; DI = digital input; DO = digital output; DIO = digital input/output; P = power supply; and NC = no connect.

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OS2	5	DI	Oversampling mode control pin (see the *Oversampling Mode of Operation* section)
$\overline{\text{PAR}}$/SER/BYTE SEL	6	DI	Logic input pin to select between parallel, serial, or parallel byte interface mode (see the *Data Read Operation* section)
RANGE	8	DI	Multi-function logic input pin (see the *RANGE (Input)* section): when $\overline{\text{STBY}}$ pin is high, this pin selects the input range of the device (±10 V or ±5 V); when $\overline{\text{STBY}}$ pin is low, this pin selects between the standby and shutdown modes.
$\overline{\text{RD}}$/SCLK	12	DI	Multi-function logic input pin (see the *RD/SCLK (Input)* section): this pin is an active-low ready input pin in parallel and parallel byte interface; this pin is a clock input pin in serial interface mode.
REFCAPA	44	AO	Reference amplifier output pins. This pin must be shorted to REFCAPB and decoupled to AGND using a low ESR, 10-µF ceramic capacitor.
REFCAPB	45	AO	Reference amplifier output pins. This pin must be shorted to REFCAPA and decoupled to AGND using a low ESR, 10-µF ceramic capacitor.
REFGND	43, 46	P	Reference GND pin. This pin must be shorted to the analog GND plane and decoupled with REFIN/REFOUT on pin 42 using a 10-µF capacitor.
REFIN/REFOUT	42	AIO	This pin acts as an internal reference output when REFSEL is high; this pin functions as input pin for the external reference when REFSEL is low; decouple with REFGND on pin 43 using a 10-µF capacitor.
REFSEL	34	DI	Active high logic input to enable the internal reference (see the *REFSEL (Input)* section)
REGCAP1	36	AO	Output pin 1 for the internal voltage regulator; decouple separately to AGND using a 1-µF capacitor.
REGCAP2	39	AO	Output pin 2 for the internal voltage regulator; decouple separately to AGND using a 1-µF capacitor.
RESET	11	DI	Active high logic input to reset the device digital logic (see the *RESET (Input)* section)
$\overline{\text{STBY}}$	7	DI	Active low logic input to enter the device into one of the two power-down modes: standby or shutdown (see the *Power-Down Modes* section)

7 Specifications

7.1 Absolute Maximum Ratings

at T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
AVDD to AGND		–0.3	7.0	V
DVDD to AGND		–0.3	7.0	V
Analog input voltage to AGND(2)		–15	15	V
Digital input to AGND		–0.3	DVDD + 0.3	V
REFIN to AGND		–0.3	AVDD + 0.3	V
Input current to any pin except supplies(2)		–10	10	mA
Temperature	Operating	–40	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient currents of up to 100 mA do not cause SCR latch-up.

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7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	All pins except analog inputs	±2000	V
			Analog input pins only	±7000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	All pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	4.75	5	5.25	V
DVDD	Digital supply voltage	2.3	3.3	AVDD	V

7.4 Thermal Information

THERMAL METRIC[1]		ADS8586S PM (LQFP) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Electrical Characteristics

minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.75 V to 5.25 V; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3 V, V_{REF} = 2.5 V (internal), and f_{SAMPLE} = 250 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	TEST LEVEL(1)
ANALOG INPUTS								
	Full-scale input span(2) (AIN_*n*P to AIN_*n*GND)	RANGE pin = 1		–10		10	V	A
		RANGE pin = 0		–5		5		A
AIN_*n*P	Operating input range, positive input	RANGE pin = 1		–10		10	V	A
		RANGE pin = 0		–5		5		A
AIN_*n*GND	Operating input range, negative input	All input ranges		–0.3	0	0.3	V	B
R_{IN}	Input impedance	At T_A = 25°C		0.85	1	1.15	MΩ	B
	Input impedance drift	All input ranges		–25	±7	25	ppm/°C	B
$I_{lkg(in)}$	Input leakage current	With voltage at AIN_*n*P = V_{IN}, all input ranges			(V_{IN} – 2) / R_{IN}		µA	A
SYSTEM PERFORMANCE								
	Resolution			16			Bits	A
NMC	No missing codes			16			Bits	A
DNL	Differential nonlinearity	All input ranges		–0.5	±0.35	0.5	LSB(3)	A
INL	Integral nonlinearity(4)	All input ranges		–1.5	±0.45	1.5	LSB	A
E_G	Gain error(5)	All input ranges, external reference	T_A = –40°C to +85°C	–64	±4	64	LSB	A
			T_A = –40°C to +125°C	–64	±4	96		A
		All input ranges, internal reference			±4			A
	Gain error matching (channel-to-channel)	Input range = ±10 V, external and internal reference			10	60	LSB	A
		Input range = ±5 V, external and internal reference			12	60		A
	Gain error temperature drift	All input ranges, external reference		–14	±6	14	ppm/°C	B
		All input ranges, internal reference			±10			B
E_O	Offset error	Input range = ±10 V		–1.8	±0.15	1.8	mV	B
		Input range = ±5 V		–1.8	±0.15	1.8		B
	Offset error matching (channel-to-channel)	All input ranges			0.3	2.4	mV	B
	Offset error temperature drift	All input ranges		–3	±0.3	3	ppm/°C	B
SAMPLING DYNAMICS								
t_{ACQ}	Acquisition time			1			µs	A
f_S	Maximum throughput rate per channel without latency	All six channels included				250	kSPS	A

(1) Test Levels: (**A**) Tested at final test. Overtemperature limits are set by characterization and simulation. (**B**) Limits set by characterization and simulation, across temperature range. (**C**) Typical value only for information, provided by design simulation.
(2) Ideal input span, does not include gain or offset error.
(3) LSB = least significant bit.
(4) This parameter is the endpoint INL, not best-fit INL.
(5) Gain error is calculated after adjusting for offset error, which implies that positive full-scale error = negative full-scale error = gain error ÷ 2.

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Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.75 V to 5.25 V; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3 V, V_{REF} = 2.5 V (internal), and f_{SAMPLE} = 250 kSPS (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
DYNAMIC CHARACTERISTICS								
SNR	Signal-to-noise ratio, no oversampling (V_{IN} – 0.5 dBFS at 1 kHz)		Input range = ±10 V	91	92.7		dB	A
			Input range = ±5 V	90.4	92.2			A
SNR_{OSR}	Signal-to-noise ratio, oversampling = 16x (V_{IN} – 0.5 dBFS at 130 Hz)		Input range = ±10 V	95.5	96.4		dB	A
			Input range = ±5 V	94.4	95.5			A
THD	Total harmonic distortion (6) (V_{IN} – 0.5 dBFS at 1 kHz)		All input ranges		–114	–95	dB	B
SINAD	Signal-to-noise + distortion ratio, no oversampling (V_{IN} – 0.5 dBFS at 1 kHz)		Input range = ±10 V	90.7	92.7		dB	A
			Input range = ±5 V	90.2	92.1			A
$SINAD_{OSR}$	Signal-to-noise + distortion ratio, oversampling = 16x (V_{IN} – 0.5 dBFS at 130 Hz)		Input range = ±10 V	95	96.4		dB	A
			Input range = ±5 V	94	95.4			A
SFDR	Spurious-free dynamic range (V_{IN} – 0.5 dBFS at 1 kHz)		All input ranges		–118		dB	B
	Crosstalk isolation (7)				–95		dB	A
$BW_{(–3\ dB)}$	Small-signal bandwidth	–3 dB	At T_A = 25°C, input range = ±10 V		24		kHz	B
			At T_A = 25°C, input range = ±5 V		16			B
$BW_{(–0.1\ dB)}$		–0.1 dB	At T_A = 25°C, input range = ±10 V		14		kHz	B
			At T_A = 25°C, input range = ±5 V		9.5			B
t_{GROUP}	Group delay		Input range = ±10 V		13		µs	C
			Input range = ±5 V		19			C
INTERNAL REFERENCE OUTPUT (REFSEL = 1)								
V_{REF} (8)	Voltage on the REFIN/REFOUT pin (configured as output)		At T_A = 25°C	2.4975	2.5	2.5025	V	A
	Internal reference temperature drift				7.5		ppm/°C	B
$C_{(REFIN_\ REFOUT)}$	Decoupling capacitor on REFIN/REFOUT (9)				10		µF	B
$V_{(REFCAP)}$	Reference voltage to the ADC (on the REFCAPA, REFCAPB pin)		At T_A = 25°C	3.996	4.0	4.004	V	A
	Reference buffer output impedance				0.5	1	Ω	C
	Reference buffer output temperature drift				5		ppm/°C	B
$C_{(REFCAP)}$	Decoupling capacitor on REFCAPA, REFCAPB				10		µF	B
	Turn-on time		$C_{(REFCAP)}$ = 10 µF, $C_{(REFIN_REFOUT)}$ = 10 µF		25		ms	B
EXTERNAL REFERENCE INPUT (REFSEL = 0)								
V_{REFIO_EXT}	External reference voltage on REFIO (configured as input)			2.475	2.5	2.525	V	B
	Reference input impedance				100		MΩ	C
	Reference input capacitance				10		pF	C

(6) Calculated on the first nine harmonics of the input frequency.
(7) Isolation crosstalk is measured by applying a full-scale sinusoidal signal up to 160 kHz to a channel, not selected in the multiplexing sequence, and measuring the effect on the output of any selected channel.
(8) Does not include the variation in voltage resulting from solder shift effects.
(9) Recommended to use an X7R-grade, 0603-size ceramic capacitor for optimum performance (see the *Layout Guidelines* section).

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Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.75 V to 5.25 V; typical specifications are at T_A = 25°C; AVDD = 5 V, DVDD = 3 V, V_{REF} = 2.5 V (internal), and f_{SAMPLE} = 250 kSPS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	TEST LEVEL (1)
POWER-SUPPLY REQUIREMENTS							
AVDD	Analog power-supply voltage	Analog supply	4.75	5	5.25	V	A
DVDD	Digital power-supply voltage	Digital supply range	2.3	3.3	AVDD	V	A
I_{AVDD_DYN}	Analog supply current (operational)	For ADS8586S, AVDD = 5 V, f_S = 250 kSPS, internal reference		14.6	19.8	mA	A
		For ADS8586S, AVDD = 5 V, f_S = 250 kSPS, external reference		14.1	19.1		A
I_{AVDD_STC}	Analog supply current (static)	For ADS8586S, AVDD = 5 V, internal reference, device not converting		10.6	14.5	mA	A
		For ADS8586S, AVDD = 5 V, external reference, device not converting		10.1	13.8		A
I_{AVDD_STDBY}	AVDD supply STANDBY current	At AVDD = 5 V, device in STDBY mode, internal reference		3.7	4.9	mA	A
		At AVDD = 5 V, device in STDBY mode, external reference		3.2	4.2		A
$I_{AVDD_PWR_DN}$	AVDD supply power-down current	At AVDD = 5 V, device in PWR_DN, internal or external reference, T_A = –40°C to +85°C		0.2	6	µA	A
I_{DVDD_DYN}	Digital supply current	For ADS8586S, DVDD = 3.3 V, f_S = 250 kSPS		0.15	0.3	mA	A
I_{DVDD_STDBY}	DVDD supply STANDBY current	At AVDD = 5 V, device in STDBY mode		0.05	1.5	µA	A
I_{DVDD_PWR-DN}	DVDD supply power-down current	At AVDD = 5 V, device in PWR_DN mode		0.05	1.5	µA	A
DIGITAL INPUTS (CMOS)							
V_{IH}	Digital high input voltage logic level	DVDD > 2.3 V	0.7 × DVDD		DVDD + 0.3	V	A
V_{IL}	Digital low input voltage logic level	DVDD > 2.3 V	–0.3		0.3 × DVDD	V	A
	Input leakage current			100		nA	A
	Input pin capacitance			5		pF	A
DIGITAL OUTPUTS (CMOS)							
V_{OH}	Digital high output voltage logic level	I_O = 100-µA source	0.8 × DVDD		DVDD	V	A
V_{OL}	Digital low output voltage logic level	I_O = 100-µA sink	0		0.2 × DVDD	V	A
	Floating state leakage current	Only for SDO		1		µA	A
	Internal pin capacitance			5		pF	A
TEMPERATURE RANGE							
T_A	Operating free-air temperature		–40		125	°C	A

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7.6 Timing Requirements: CONVST Control

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), BUSY load = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 1)

		MIN	NOM	MAX	UNIT
t_{ACQ}	Acquisition time: BUSY falling edge to rising edge of trailing CONVSTA or CONVSTB	1			µs
t_{PH_CN}	CONVSTA, CONVSTB pulse high time	25			ns
t_{PL_CN}	CONVSTA, CONVSTB pulse low time	25			ns
t_{SU_BSYCS}	Setup time: BUSY falling to $\overline{CS}$ falling	0			ns
t_{SU_RSTCN}	Setup time: RESET falling to first rising edge of CONVSTA or CONVSTB	25			ns
t_{PH_RST}	RESET pulse high time	50			ns
t_{D_CNAB}	Delay between rising edges of CONVSTA and CONVSTB			500	µs

7.7 Timing Requirements: Data Read Operation

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), BUSY load = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 2)

		MIN	NOM	MAX	UNIT
t_{DZ_CNCS}	Delay between CONVSTA, CONVSTB rising edge to $\overline{CS}$ falling edge, start of data read operation during conversion	10			ns
t_{DZ_CSBSY}	Delay between $\overline{CS}$ rising edge to BUSY falling edge, end of data read operation during conversion	40			ns
t_{SU_BSYCS}	Setup time: BUSY falling edge to $\overline{CS}$ falling edge, start of data read operation after conversion	0			ns
t_{D_CSCN}	Delay between $\overline{CS}$ rising edge to CONVSTA, CONVSTB rising edge, end of data read operation after conversion	10			ns

7.8 Timing Requirements: Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Tied Together

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[15:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 3)

		MIN	NOM	MAX	UNIT
t_{PH_CS}, t_{PH_RD}	$\overline{CS}$ and $\overline{RD}$ high time	15			ns
t_{PL_CS}, t_{PL_RD}	$\overline{CS}$ and $\overline{RD}$ low time	15			ns
t_{HT_RDDB}, t_{HT_CSDB}	Hold time: $\overline{RD}$ and $\overline{CS}$ rising edge to DB[15:0] invalid	2.5			ns

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7.9 Timing Requirements: Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Separate

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[15:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 4)

		MIN	NOM	MAX	UNIT
t_{SU_CSRD}	Setup time: $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	0			ns
t_{HT_RDCS}	Hold time: $\overline{RD}$ rising edge to $\overline{CS}$ rising edge	0			ns
t_{PL_RD}	$\overline{RD}$ low time	15			ns
t_{PH_RD}	$\overline{RD}$ high time	15			ns
t_{HT_CSDB}	Hold time: $\overline{CS}$ rising edge to DB[15:0] becoming invalid	6			ns
t_{HT_RDDB}	Hold time: $\overline{RD}$ rising edge to DB[15:0] becoming invalid	2.5			ns

7.10 Timing Requirements: Serial Data Read Operation

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DOUTA, DOUTB, and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 5)

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK time period	50			ns
t_{PH_SCLK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_SCLK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{HT_CKDO}	Hold time: SCLK rising edge to DOUTA, DOUTB invalid	7			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to first SCLK edge	8			ns
t_{HT_CKCS}	Hold time: last SCLK active edge to $\overline{CS}$ high	10			ns

7.11 Timing Requirements: Byte Mode Data Read Operation

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[7:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 6)

		MIN	NOM	MAX	UNIT
t_{SU_CSRD}	Setup time: $\overline{CS}$ falling edge to $\overline{RD}$ falling edge	0			ns
t_{HT_RDCS}	Hold time: $\overline{RD}$ rising edge to $\overline{CS}$ rising edge	0			ns
t_{PL_RD}	$\overline{RD}$ low time	15			ns
t_{PH_RD}	$\overline{RD}$ high time	15			ns
t_{HT_CSDB}	Hold time: $\overline{CS}$ rising edge to DB[15:0] becoming invalid	6			ns
t_{HT_RDDB}	Hold time: $\overline{RD}$ rising edge to DB[15:0] becoming invalid	2.5			ns

7.12 Timing Requirements: Oversampling Mode

		MIN	NOM	MAX	UNIT
t_{HT_OS}	Hold time: BUSY falling to OSx	20			ns
t_{SU_OS}	Setup time: BUSY falling to OSx	20			ns

7.13 Timing Requirements: Exit Standby Mode

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C, AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 8)

		MIN	NOM	MAX	UNIT
t_{D_STBYCN}	Delay between $\overline{STBY}$ rising edge to CONVSTA or CONVSTB rising edge[(1)]	100			µs

(1) First conversion data must be discarded or RESET must be issued if the maximum timing is exceeded.

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7.14 Timing Requirements: Exit Shutdown Mode

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 9)

			MIN	NOM	MAX	UNIT
t_{D_SDRST}	Delay between $\overline{STBY}$ rising edge to RESET rising edge	Internal reference mode	50			ms
		External reference mode(1)	13			
t_{PH_RST}	RESET high time		50			ns
t_{D_RSTCN}	Delay between RESET falling edge to CONVSTA or CONVSTB rising edge		25			µs

(1) Excludes wake-up time for external reference device.

7.15 Switching Characteristics: CONVST Control

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), BUSY load = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}	ADC cycle time period	No oversampling, parallel read, serial read with both DOUTA and DOUTB during conversion	4			µs
		No oversampling, serial read after conversion with both DOUTA and DOUTB	5.6			
		No oversampling, serial read after conversion with only DOUTA or DOUTB	8			
t_{CONV}	Conversion time: BUSY high time	No oversampling		3		µs
		Oversampling by 2		7		
		Oversampling by 4		15		
		Oversampling by 8		31		
		Oversampling by 16		63		
		Oversampling by 32		127		
		Oversampling by 64		255		
t_{D_CNBSY}	Delay between trailing rising edges of CONVSTA or CONVSTB and BUSY rising				15	ns

7.16 Switching Characteristics: Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Tied Together

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[15:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D_CSDB}	Delay time: $\overline{CS}$ falling edge to DB[15:0] becoming valid (out of tri-state)				12	ns
t_{D_RDDB}	Delay time: $\overline{RD}$ falling edge to new data on DB[15:0]				17	ns
t_{D_CSFD}, t_{D_RDFD}	Delay time: $\overline{CS}$ and $\overline{RD}$ falling edge to FRSTDATA going high or low out of tri-state				10	ns
t_{DHZ_CSDB}, t_{DHZ_RDDB}	Delay time: $\overline{CS}$ and $\overline{RD}$ rising edge to DB[15:0] tri-state				12	ns
t_{DHZ_CSFD}, t_{DHZ_RDFD}	Delay time: $\overline{CS}$ and $\overline{RD}$ rising edge to FRSTDATA tri-state				10	ns

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7.17 Switching Characteristics: Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Separate

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[15:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D_CSDB}	Delay time: $\overline{CS}$ falling edge to DB[15:0] becoming valid (out of tri-state)				12	ns
t_{D_RDDB}	Delay time: $\overline{RD}$ falling edge to new data on DB[15:0]				17	ns
t_{DHZ_CSDB}	Delay time: $\overline{CS}$ rising edge to DB[15:0] becoming tri-state				12	ns
t_{D_CSFD}	Delay time: $\overline{CS}$ falling edge to FRSTDATA going low out of tri-state				15	ns
t_{DHZ_CSFD}	Delay time: $\overline{CS}$ rising edge to FRSTDATA going to tri-state				10	ns
t_{D_RDFD}	Delay time: $\overline{RD}$ falling edge to FRSTDATA going high or low				15	ns

7.18 Switching Characteristics: Serial Data Read Operation

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DOUTA, DOUTB, and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D_CSDO}	Delay time: $\overline{CS}$ falling edge to DOUTA, DOUTB enable (out of tri-state)				12	ns
t_{D_CKDO}	Delay time: SCLK rising edge to valid data on DOUTA, DOUTB				15	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising edge to DOUTA, DOUTB going to tri-state				12	ns
t_{D_CSFD}	Delay time: $\overline{CS}$ falling edge to FRSTDATA from tri-state to high or low				10	ns
t_{DZ_CKFD}	Delay time: 16th SCLK falling edge to FRSTDATA falling edge				15	ns
t_{DHZ_CSFD}	Delay time: $\overline{CS}$ rising edge to FRSTDATA going to tri-state				10	ns

7.19 Switching Characteristics: Byte Mode Data Read Operation

minimum and maximum specifications are at T_A = –40°C to +125°C, typical specifications are at T_A = 25°C; AVDD = 5 V, 2.3 V ≤ DVDD ≤ 5.25 V, V_{REF} = 2.5 V (internal), load on DB[7:0] and FRSTDATA = 20 pF, V_{IL} and V_{IH} at datasheet limits, and f_{SAMPLE} = 250 kSPS (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{D_CSDB}	Delay time: $\overline{CS}$ falling edge to DB[7:0] becoming valid (out of tri-state)				12	ns
t_{D_RDDB}	Delay time: $\overline{RD}$ falling edge to new data on DB[7:0]				17	ns
t_{DHZ_CSDB}	Delay time: $\overline{CS}$ rising edge to DB[7:0] becoming tri-state				12	ns
t_{D_CSFD}	Delay time: $\overline{CS}$ falling edge to FRSTDATA going low out of tri-state				10	ns
t_{D_RDFD}	Delay time: $\overline{RD}$ falling edge to FRSTDATA going low or high state				15	ns
t_{DHZ_CSFD}	Delay time: $\overline{CS}$ rising edge to FRSTDATA going to tri-state				10	ns

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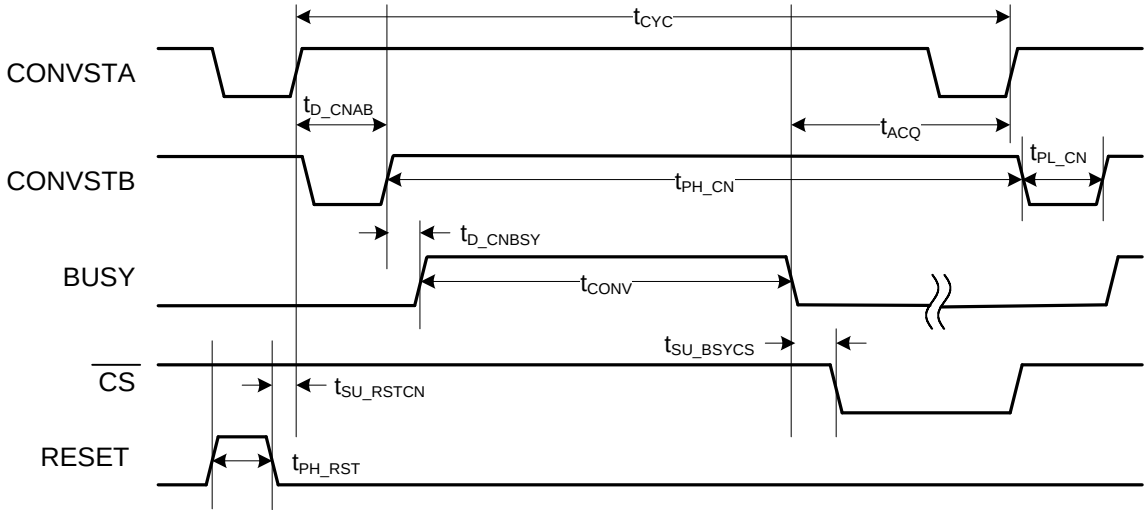

Figure 1. CONVST Control Timing Diagram

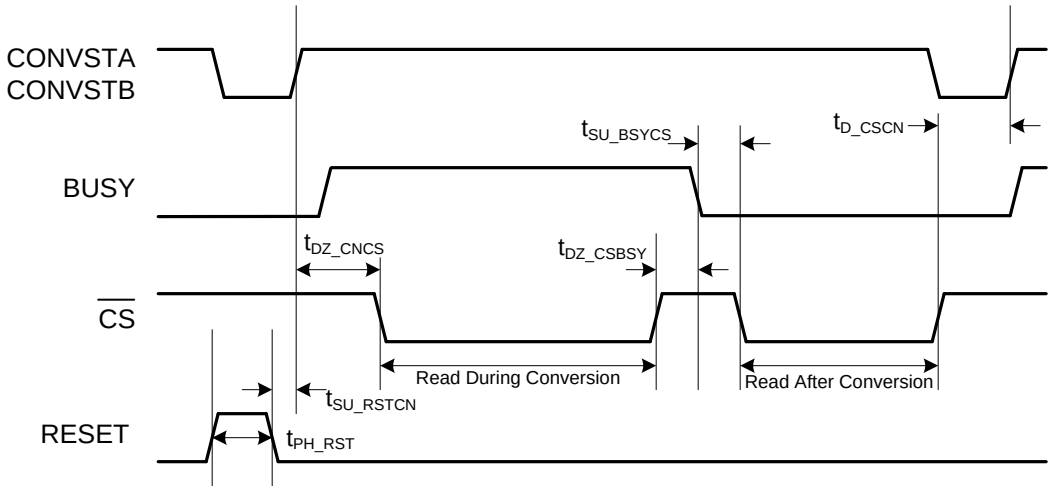

Figure 2. Data Read Operation Timing Diagram

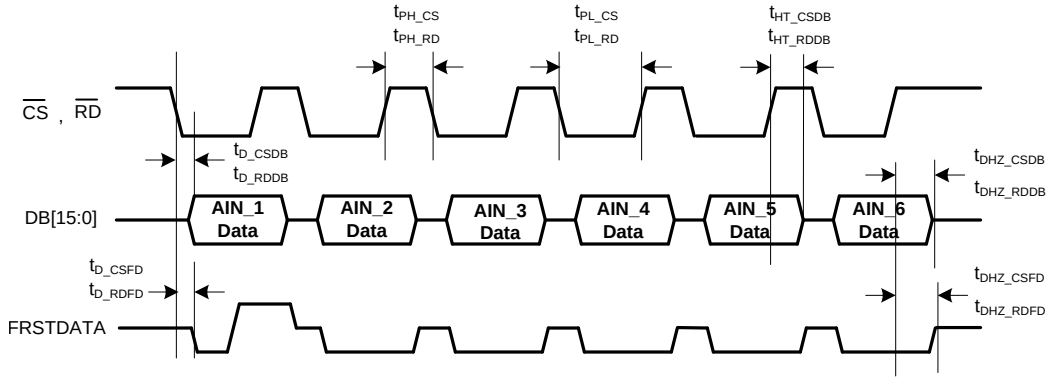

Figure 3. Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Tied Together

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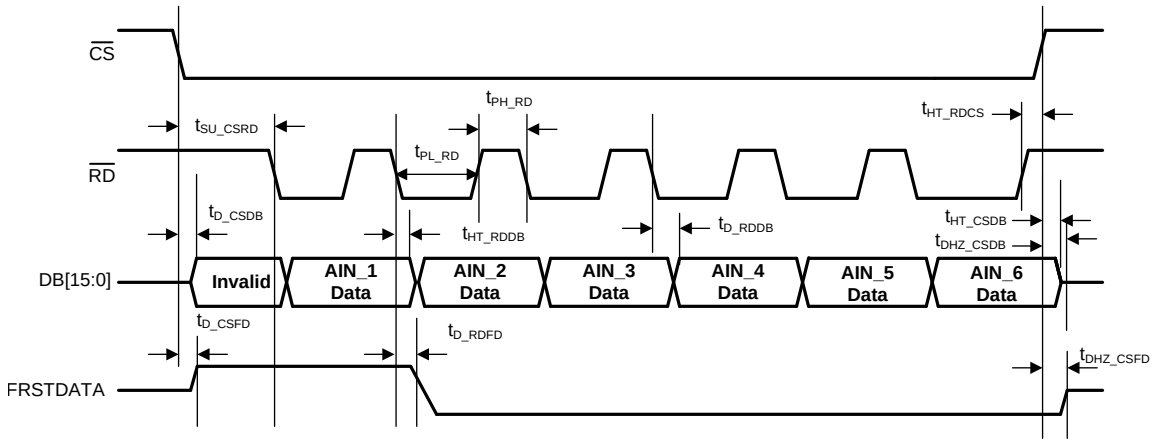

Figure 4. Parallel Data Read Operation, $\overline{CS}$ and $\overline{RD}$ Separate

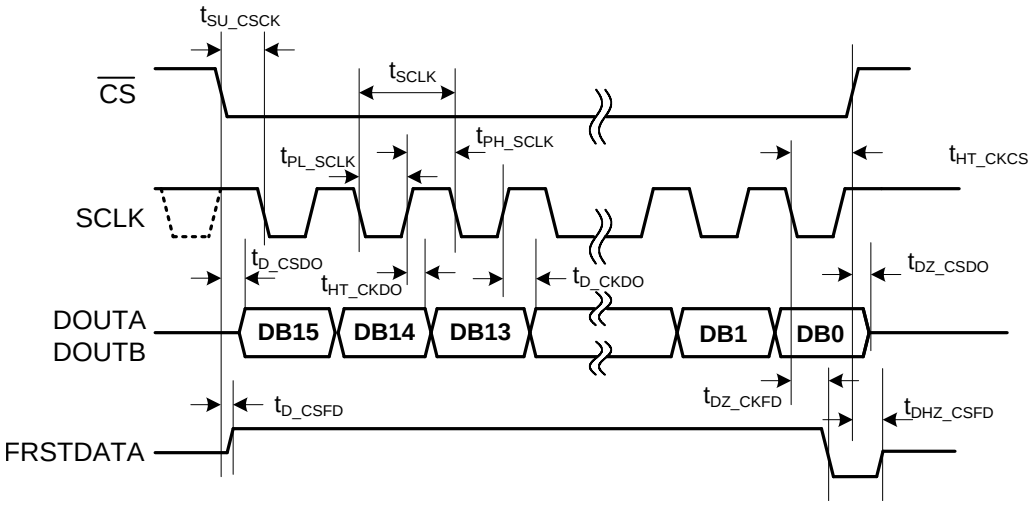

Figure 5. Serial Data Read Operation Timing Diagram

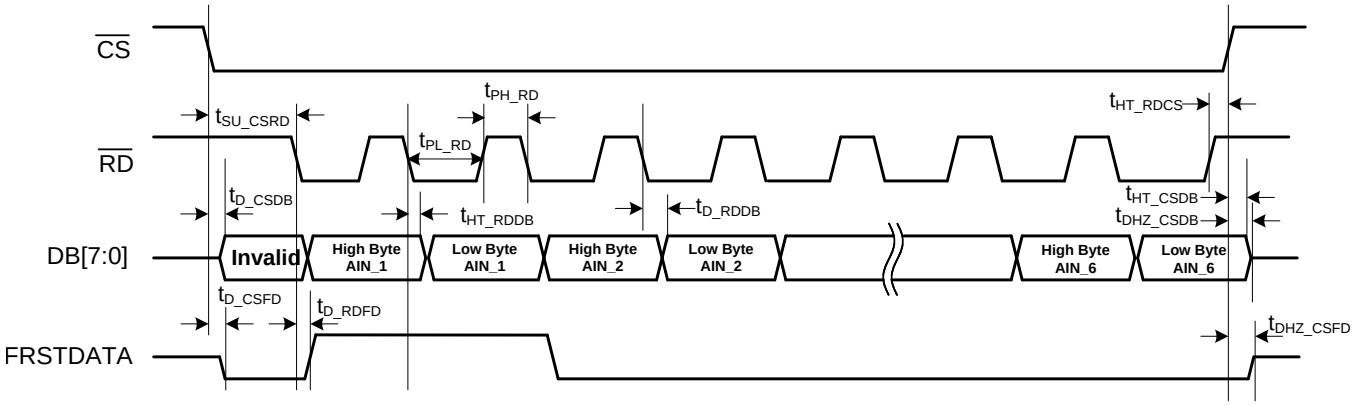

Figure 6. Byte Mode Data Read Operation Timing Diagram

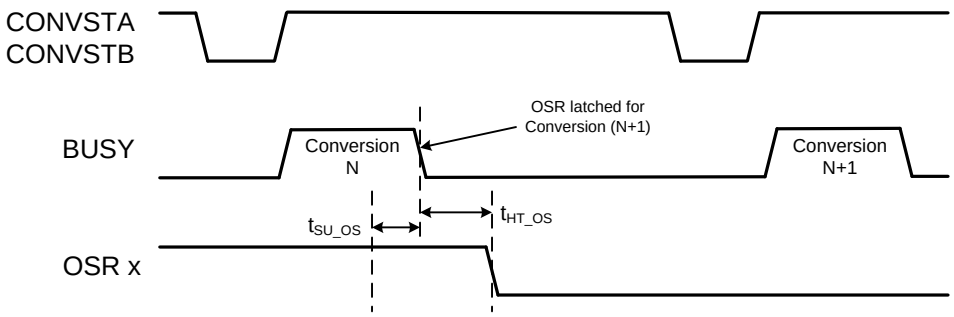

Figure 7. Oversampling Mode Timing Diagram

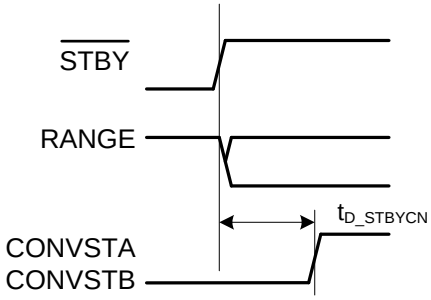

Figure 8. Exit Standby Mode Timing Diagram

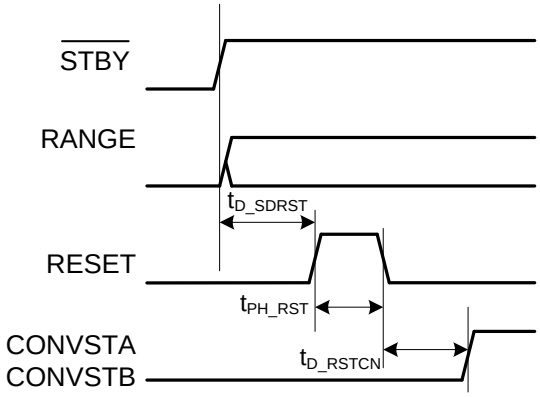

Figure 9. Exit Shutdown Mode Timing Diagram

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7.20 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

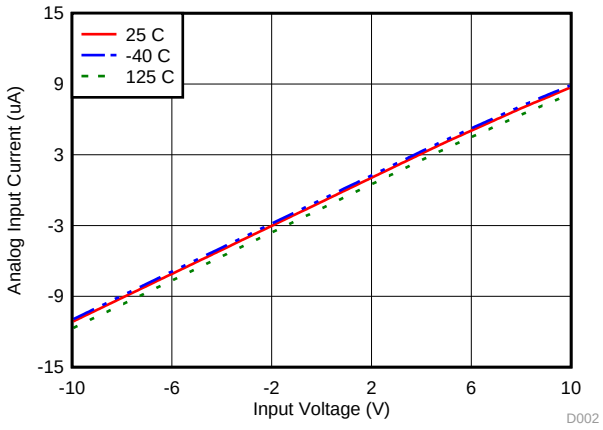


Figure 10. Analog Input Current vs Input Voltage Over Temperature (±10 V)

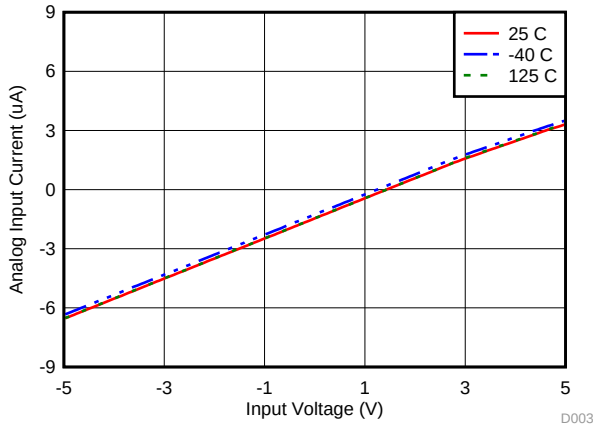


Figure 11. Analog Input Current vs Input Voltage Over Temperature (±5 V)

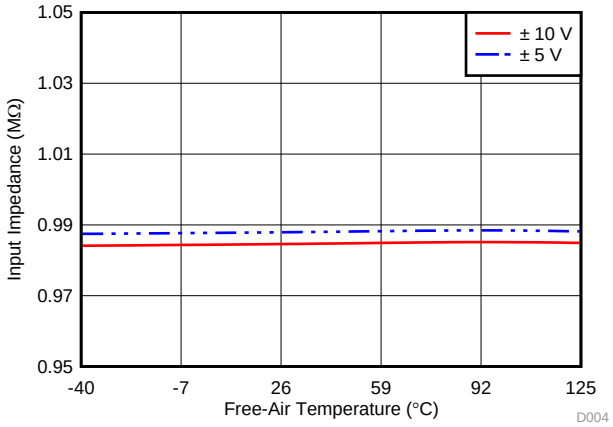
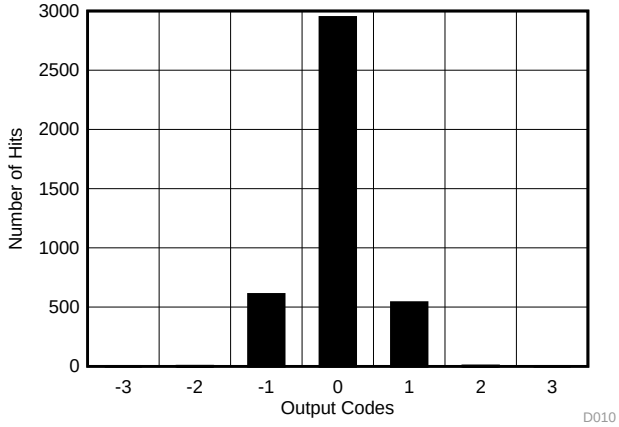
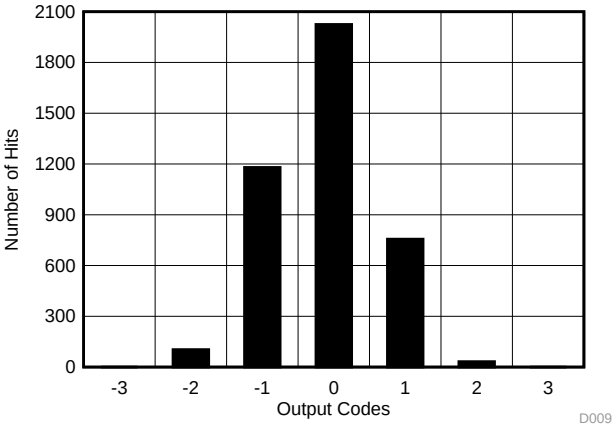


Figure 12. Input Impedance vs Temperature



Mean = –0.14, sigma = 0.51, number of hits = 4096, V_{IN} = 0 V

Figure 13. DC Histogram of Codes (±10 V)



Mean = –0.02, sigma = 0.54, number of hits = 4096, V_{IN} = 0 V

Figure 14. DC Histogram of Codes (±5 V)

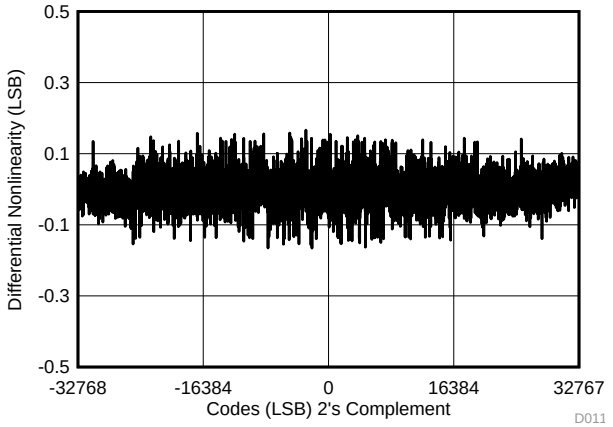


Figure 15. DNL for All Codes

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

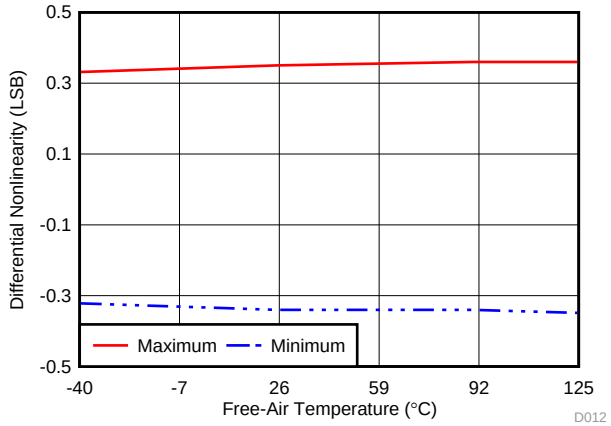


Figure 16. DNL vs Temperature

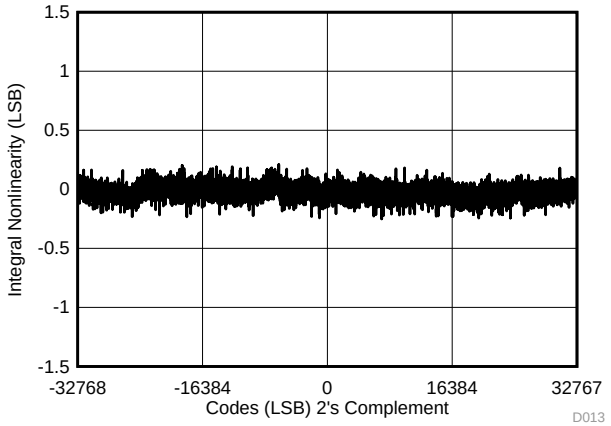


Figure 17. INL vs All Codes (±10 V)

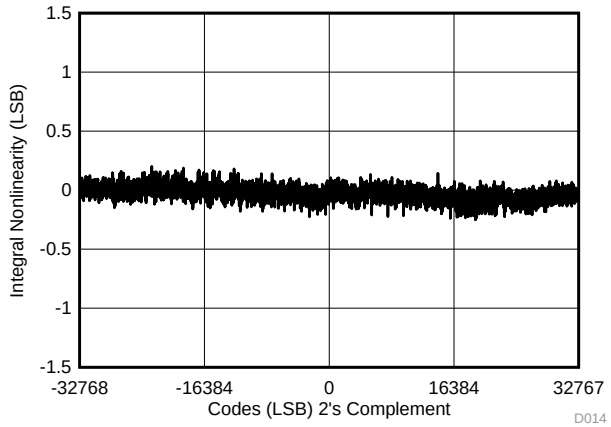


Figure 18. INL vs All Codes (±5 V)

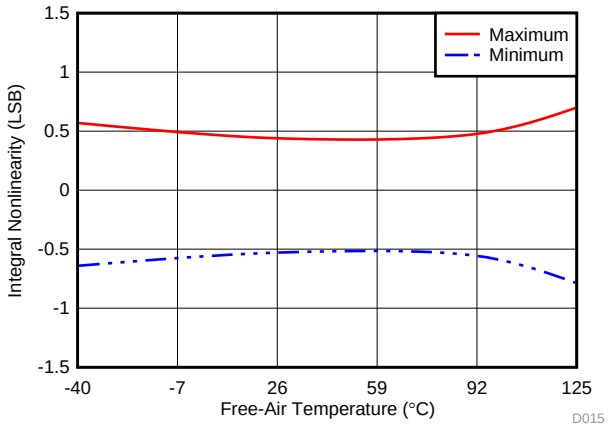


Figure 19. INL vs Temperature (±10 V)

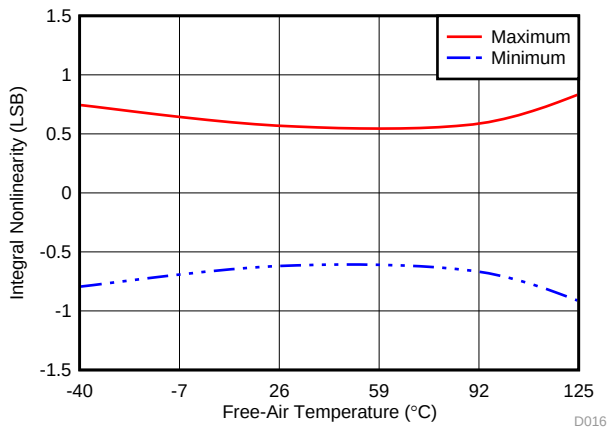


Figure 20. INL vs Temperature (±5 V)

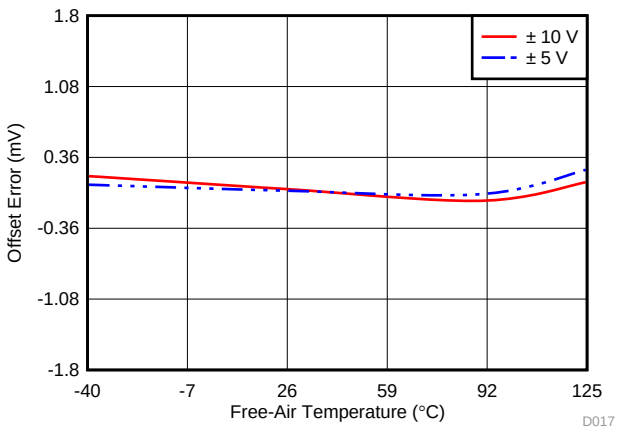


Figure 21. Offset Error vs Temperature

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

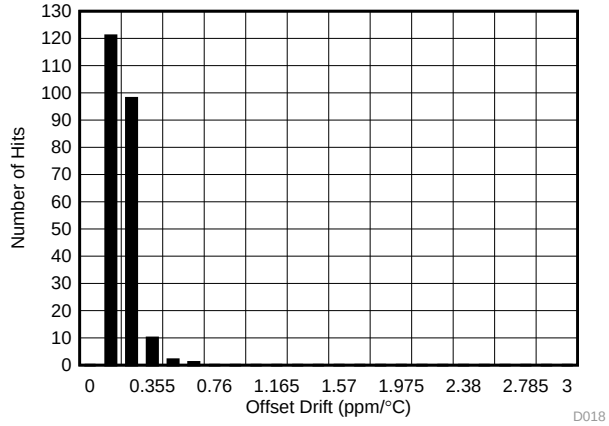

Figure 22. Offset Drift Histogram Distribution (±10 V)

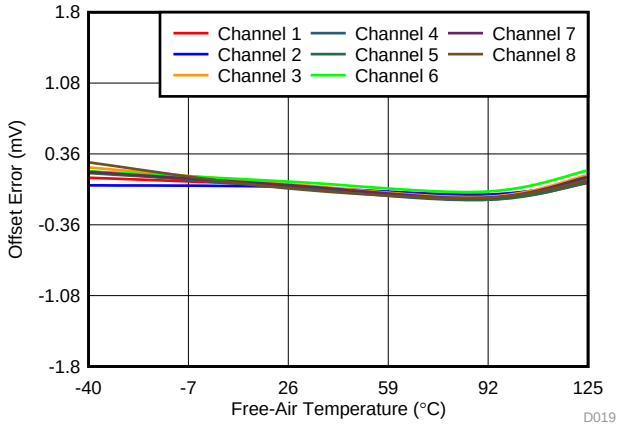

Figure 23. Offset Error Across Channels vs Temperature (±10 V)

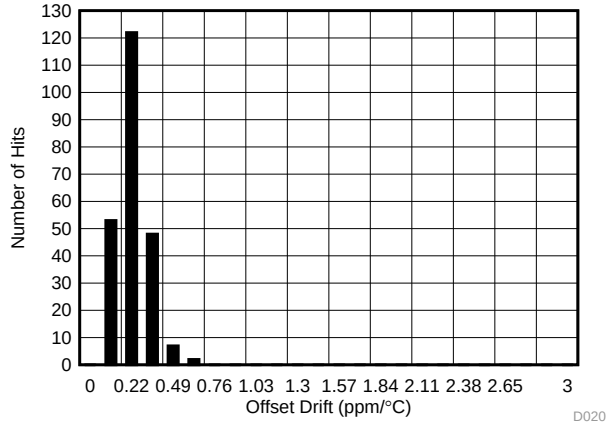

Figure 24. Offset Drift Histogram Distribution (±5 V)

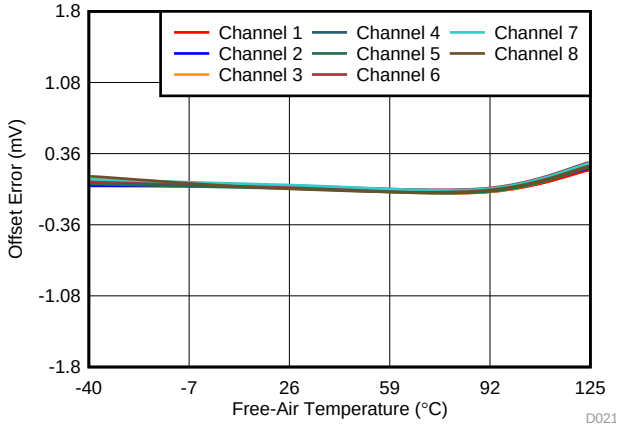

Figure 25. Offset Error Across Channels vs Temperature (±5 V)

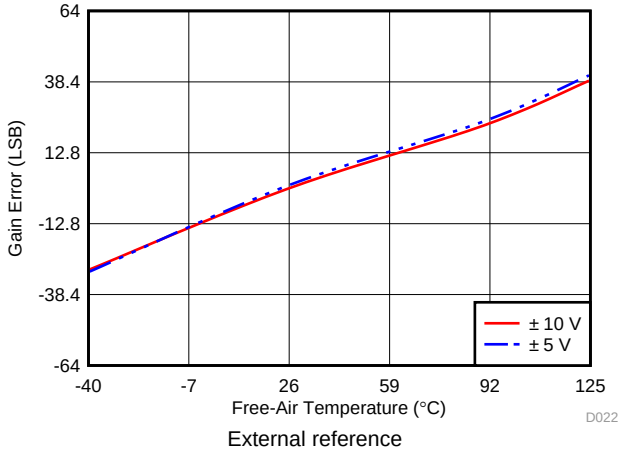

Figure 26. Gain Error vs Temperature

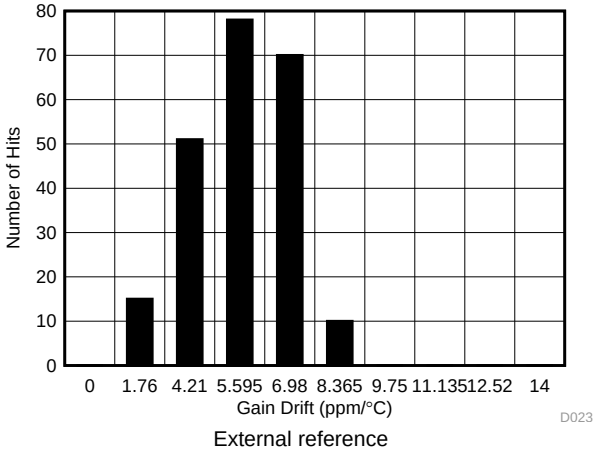

Figure 27. Gain Error Drift Histogram Distribution (±10 V)

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

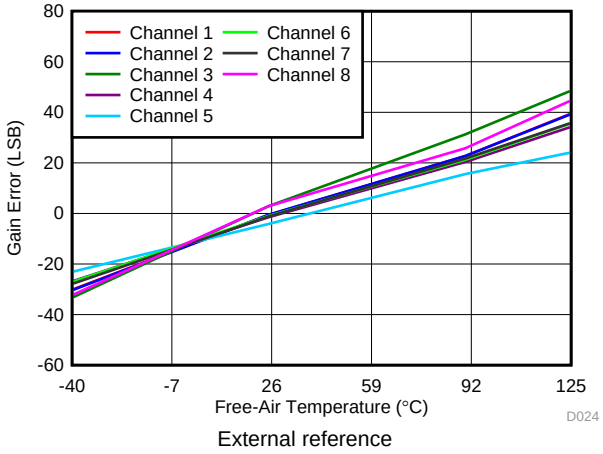


Figure 28. Gain Error Across Channels vs Temperature (±10 V)

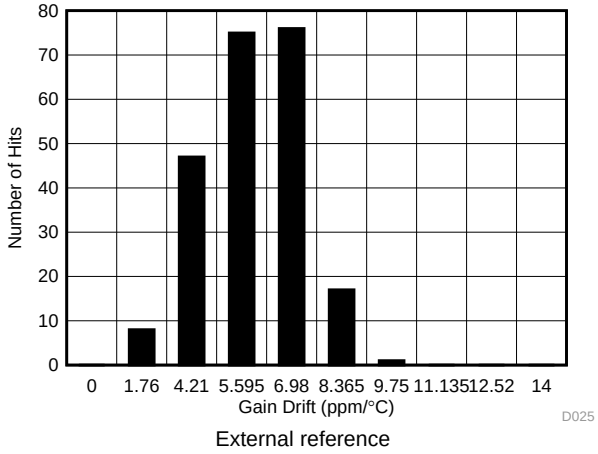


Figure 29. Gain Error Drift Histogram Distribution (±5 V)

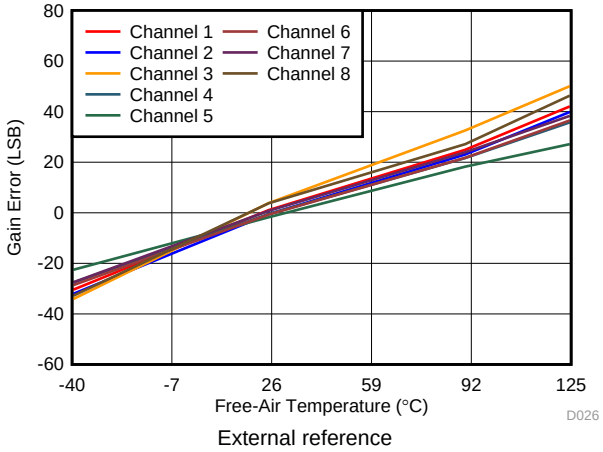


Figure 30. Gain Error Across Channels vs Temperature (±5 V)

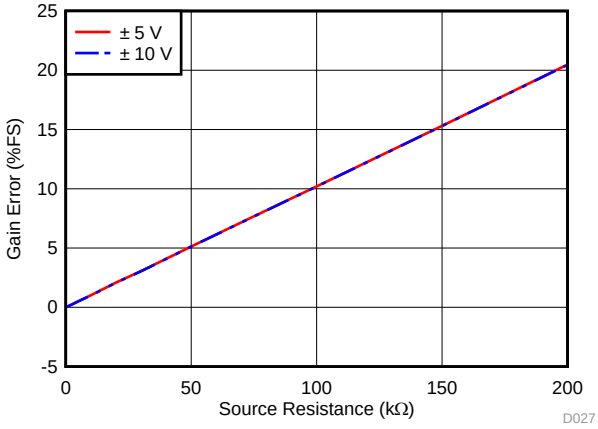
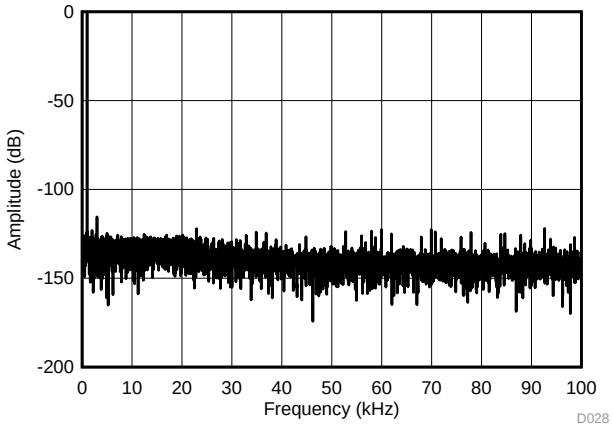
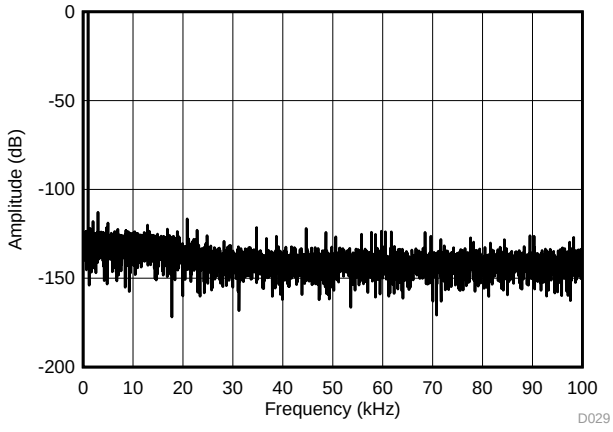


Figure 31. Gain Error as a Function of External Source Resistance



Number of points = 32k, SNR = 92.71 dB,
SINAD = 92.3 dB, THD = –111.72 dB, SFDR = 114.61 dB

Figure 32. Typical FFT Plot (±10 V)



Number of points = 32k, SNR = 92.21 dB,
SINAD = 92.13 dB, THD = –110.79 dB, SFDR = 113.95 dB

Figure 33. Typical FFT Plot (±5 V)

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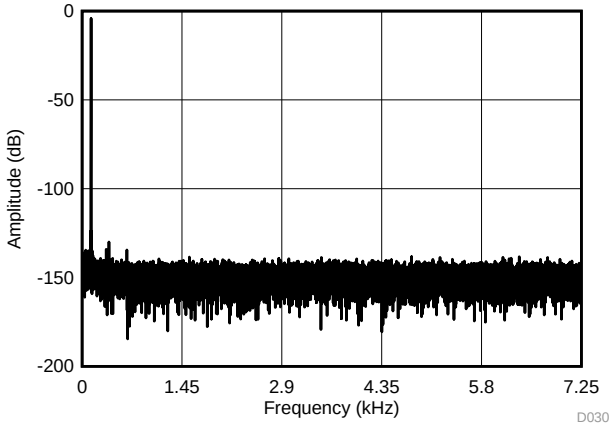
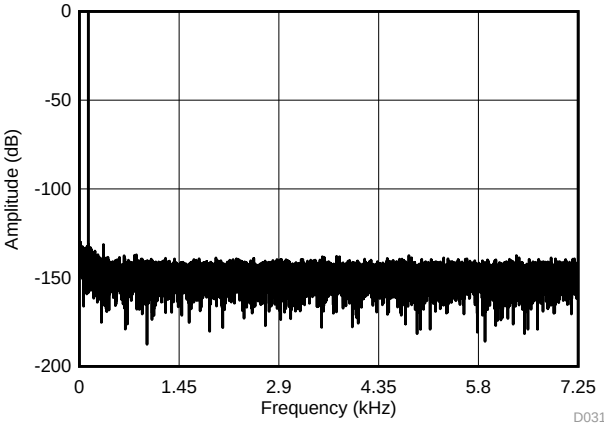
Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)



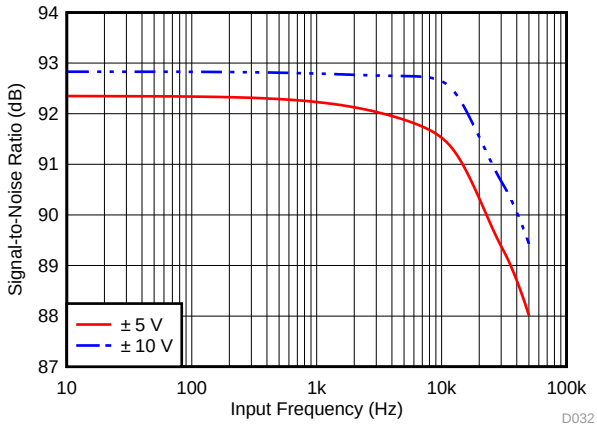
Number of points = 32k, SNR = 96.45 dB,
SINAD = 95.83 dB, THD = –110.78 dB, SFDR = 114.1 dB

Figure 34. Typical FFT Plot for OSR 16x (±10 V)



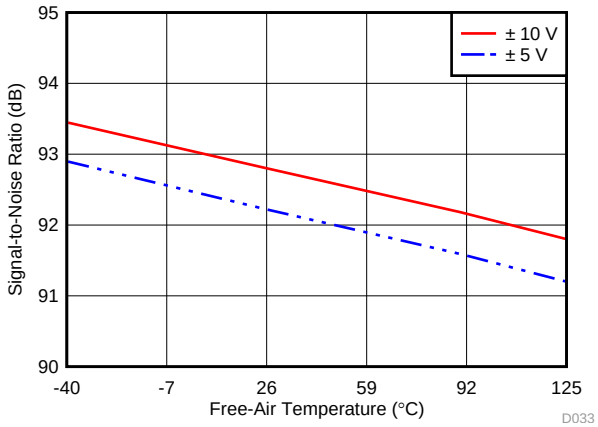
Number of points = 32k, SNR = 95.41 dB,
SINAD = 94.82 dB, THD = –109.95 dB, SFDR = 113.61 dB

Figure 35. Typical FFT Plot for OSR 16x (±5 V)



OSR = 0

Figure 36. SNR vs Input Frequency for Different Input Ranges



OSR = 0

Figure 37. SNR vs Temperature for Different Input Ranges

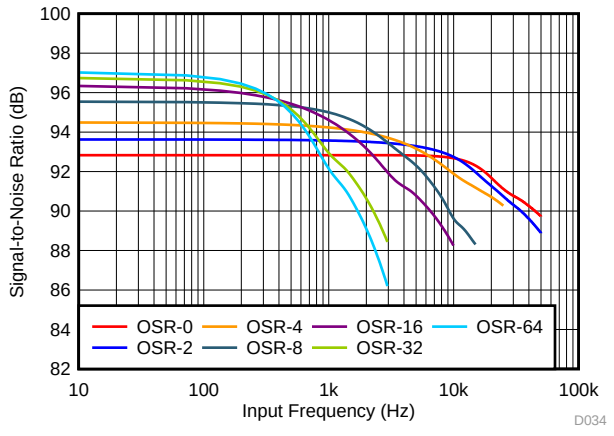


Figure 38. SNR vs Input Frequency for Different OSR (±10 V)

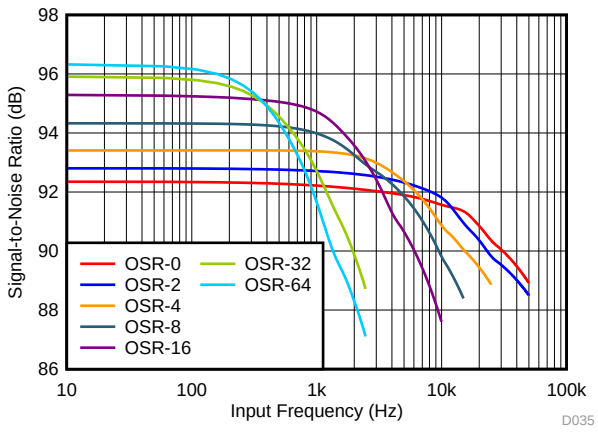


Figure 39. SNR vs Input Frequency for Different OSR (±5 V)

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

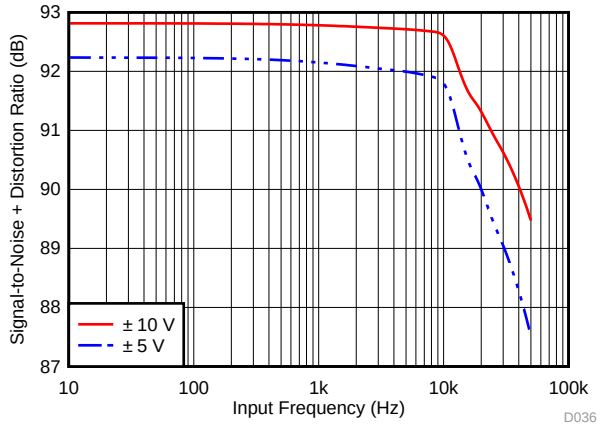

Figure 40. SINAD vs Input Frequency for Different Input Ranges

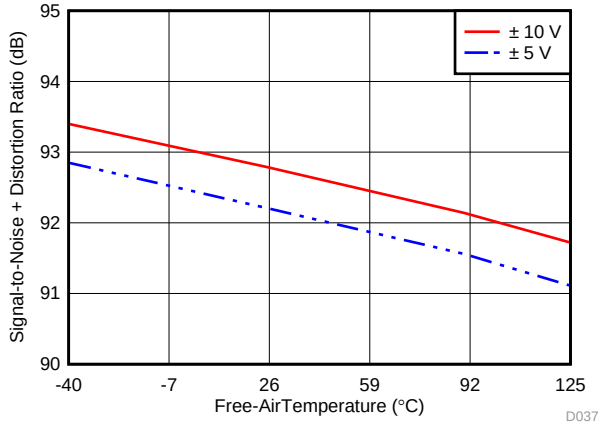

Figure 41. SINAD vs Temperature for Different Input Ranges

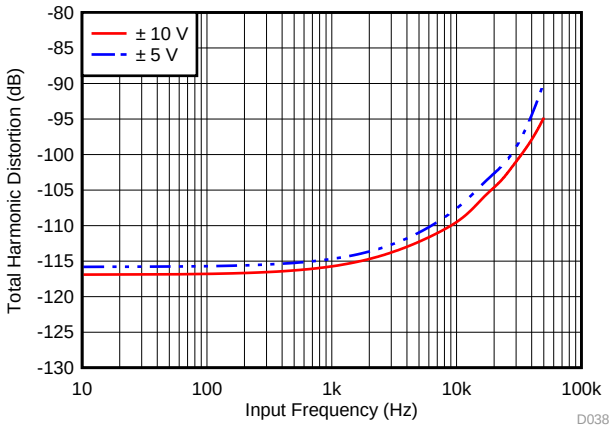

Figure 42. THD vs Input Frequency for Different Input Ranges

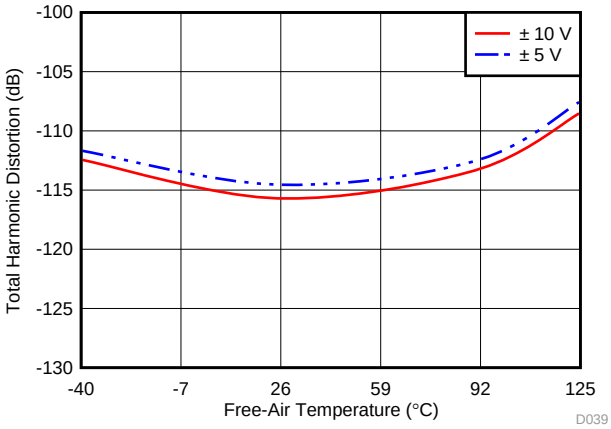

Figure 43. THD vs Temperature for Different Input Ranges

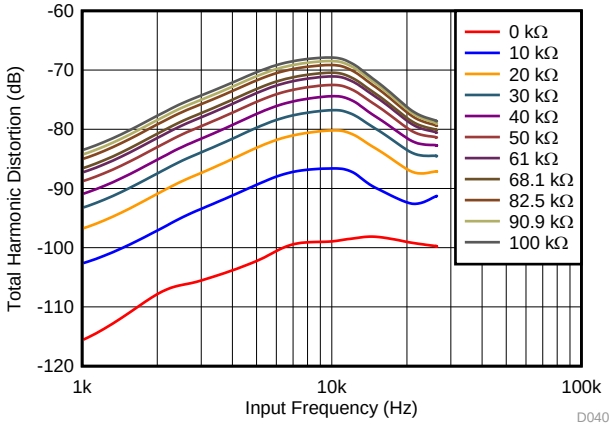

Figure 44. THD vs Input Frequency for Different Source Impedances (±10 V)

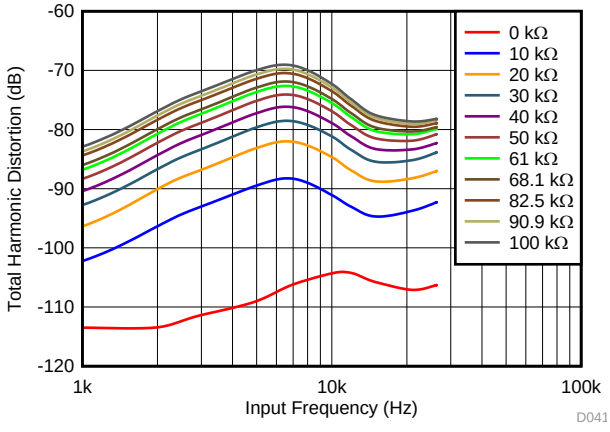

Figure 45. THD vs Input Frequency for Different Source Impedances (±5 V)

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Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 3 V, internal reference V_{REF} = 2.5 V, and f_S = 250 kSPS per channel (unless otherwise noted)

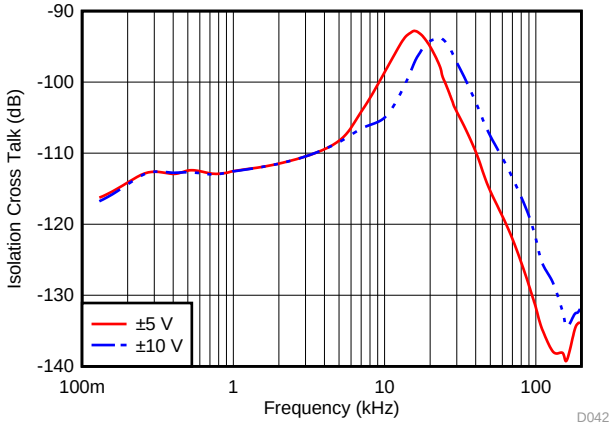

Figure 46. Isolation Crosstalk vs Noise Frequency (Inputs Within Range)

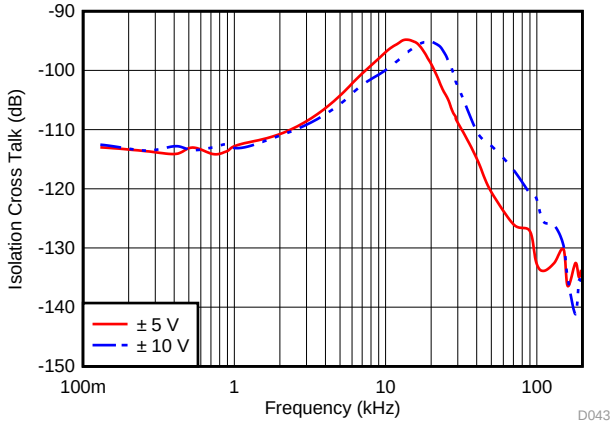

Figure 47. Isolation Crosstalk vs Noise Frequency (Saturated Inputs)

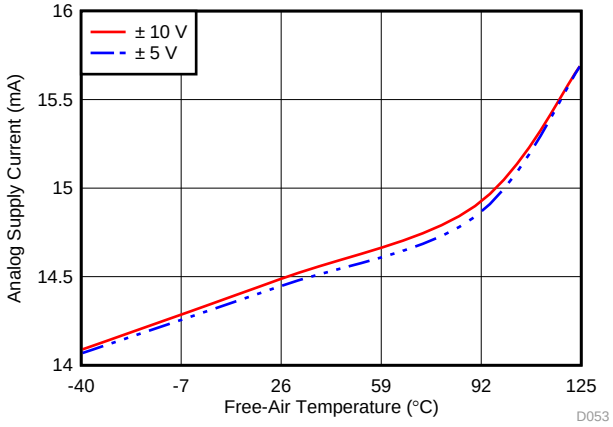

Figure 48. Analog Supply Current (Operational) vs Temperature

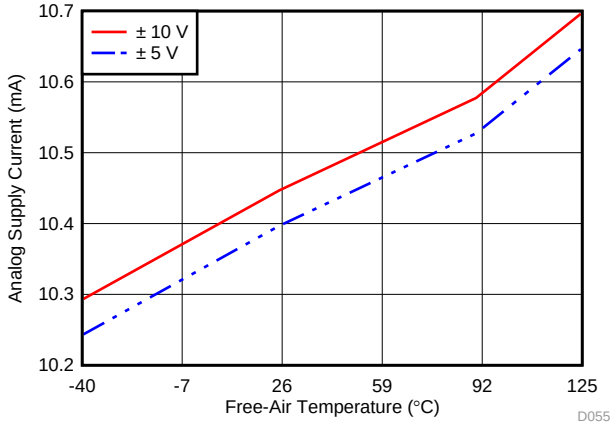

Figure 49. Analog Supply Current (Static) vs Temperature (Sampling)

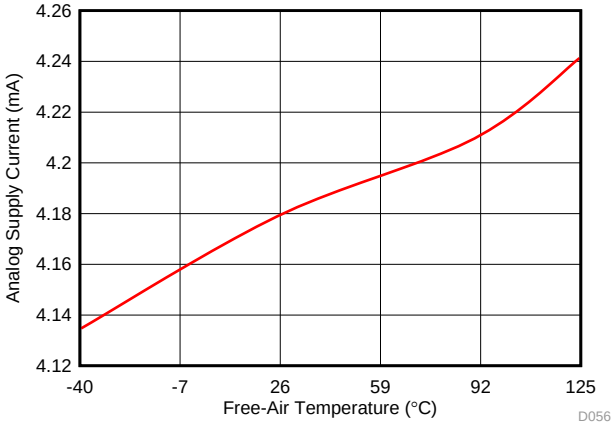

Figure 50. Analog Supply Current vs Temperature (Standby)

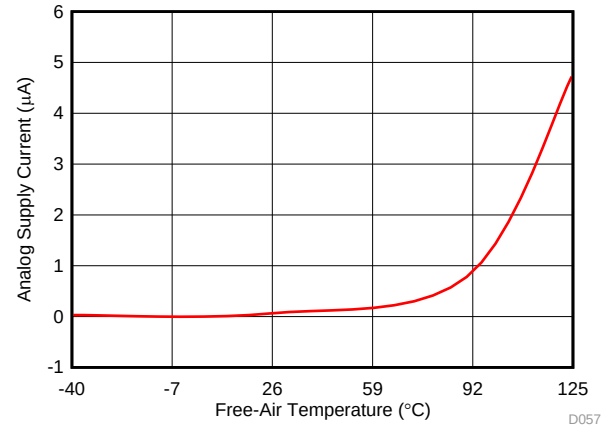

Figure 51. Analog Supply Current vs Temperature (Shutdown)

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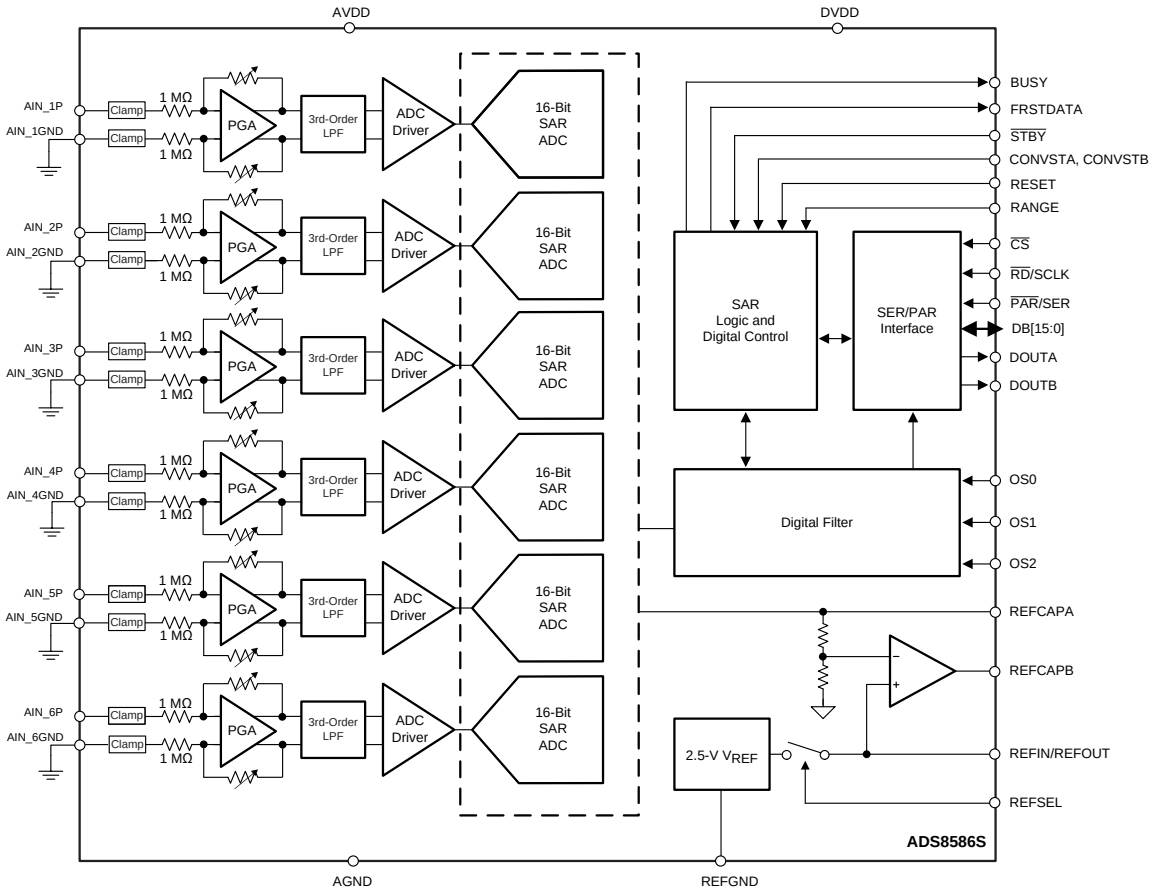
8 Detailed Description

8.1 Overview

The ADS8586S is a 16-bit data acquisition (DAQ) system with 6-channel analog inputs. Each analog input channel consists of an input clamp protection circuit, a programmable gain amplifier (PGA), a third-order, low-pass filter, and a track-and-hold circuit that facilitates simultaneous sampling of the signals on all input channels. The sampled signal is digitized using a 16-bit analog-to-digital converter (ADC), based on the successive approximation register (SAR) architecture. This overall system can achieve a maximum throughput of 250 kSPS per channel. The device features a 2.5-V internal reference with a fast-settling buffer, a programmable digital averaging filter to improve noise performance, and high speed serial and parallel interfaces for communication with a wide variety of digital hosts.

The device operates from a single 5-V analog supply and can accommodate true bipolar input signals of ±10 V and ±5 V. The input clamp protection circuitry can tolerate voltages up to ±15 V. The device offers a constant 1-MΩ resistive input impedance irrespective of the sampling frequency or the selected input range. The integration of multiple, simultaneously sampling precision ADC inputs and analog front-end circuits with high input impedance operating from a single 5-V supply offers a simplified end solution without requiring external high-voltage bipolar supplies and complicated driver circuits.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Analog Inputs

The ADS8586S has 6 analog input channels, such that the positive inputs AIN_*n*P (n = 1 to 6) are the single-ended analog inputs and the negative inputs AIN_*n*GND are tied to GND. Figure 52 shows the simplified circuit schematic for each analog input channel, including the input clamp protection circuit, PGA, low-pass filter, high-speed ADC driver, and a precision 16-bit SAR ADC.

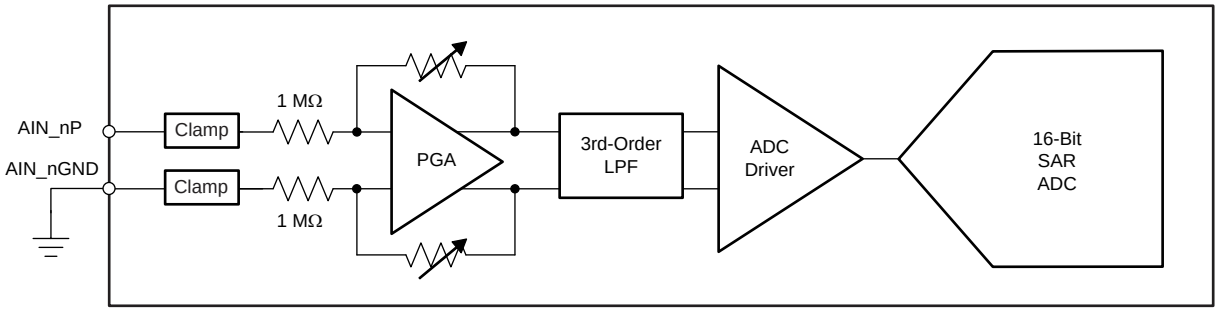

Figure 52. Front-End Circuit Schematic for Each Analog Input Channel

The device can support two bipolar, single-ended input voltage ranges based on the logic level of the RANGE input pin. As explained in the *RANGE (Input)* section, the input voltage range for all analog channels can be configured to bipolar ±10 V or ±5 V. The device samples the voltage difference (AIN_*n*P – AIN_*n*GND) between the selected analog input channel and the AIN_*n*GND pin. The device allows a ±0.3-V range on the AIN_*n*GND pin for all analog input channels. Use this feature in modular systems where the sensor or signal conditioning block is further away from the ADC on the board and when a difference in the ground potential of the sensor or signal conditioner from the ADC ground is possible. In such cases, running separate wires from the AIN_*n*GND pin of the device to the sensor or signal conditioning ground is recommended.

8.3.2 Analog Input Impedance

Each analog input channel in the device presents a constant resistive impedance of 1 MΩ. The input impedance for each channel is independent of either the input signal frequency, the configured range of the ADC, or the oversampling mode. The primary advantage of such high-impedance inputs is the ease of driving the ADC inputs without requiring driving amplifiers with low output impedance. Bipolar, high-voltage power supplies are not required in the system because this ADC does not require any high-voltage, front-end drivers. In most applications, the signal sources or sensor outputs can be directly connected to the ADC input, thus significantly simplifying the design of the signal chain.

In order to maintain the dc accuracy of the system, matching the external source impedance on the AIN_*n*P input pin with an equivalent resistance on the AIN_*n*GND pin is recommended (see Figure 54). This matching helps to cancel any additional offset error contributed by the external resistance.

8.3.3 Input Clamp Protection Circuit

As shown in Figure 52, the ADS8586S features an internal clamp protection circuit on each of the 6 analog input channels. Use of external protection circuits is recommended as a secondary protection scheme to protect the device. Using external protection devices helps with protection against surges, electrostatic discharge (ESD), and electrical fast transient (EFT) conditions.

The input clamp protection circuit on the ADS8586S allows each analog input to swing up to a maximum voltage of ±15 V. Beyond an input voltage of ±15 V, the input clamp circuit turns on, still operating off the single 5-V supply. Figure 53 illustrates a typical current versus voltage characteristic curve for the input clamp. There is no current flow in the clamp circuit for input voltages up to ±15 V. Beyond this voltage, the input clamp circuit turns on.

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Feature Description (continued)

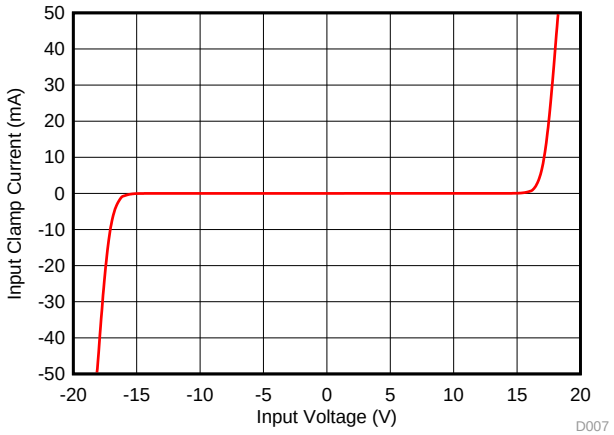

Figure 53. I-V Curve for an Input Clamp Protection Circuit (AVDD = 5 V)

For input voltages above the clamp threshold, make sure that input current never exceeds the absolute maximum rating (see the *Absolute Maximum Ratings* table) of ±10 mA to prevent any damage to the device. Figure 54 shows that a small series resistor placed in series with the analog inputs is an effective way to limit the input current. In addition to limiting the input current, this resistor can also provide an antialiasing, low-pass filter when coupled with a capacitor. In order to maintain the dc accuracy of the system, matching the external source impedance on the AIN_*n*P input pin with an equivalent resistance on the AIN_*n*GND pin is recommended. This matching helps to cancel any additional offset error contributed by the external resistance.

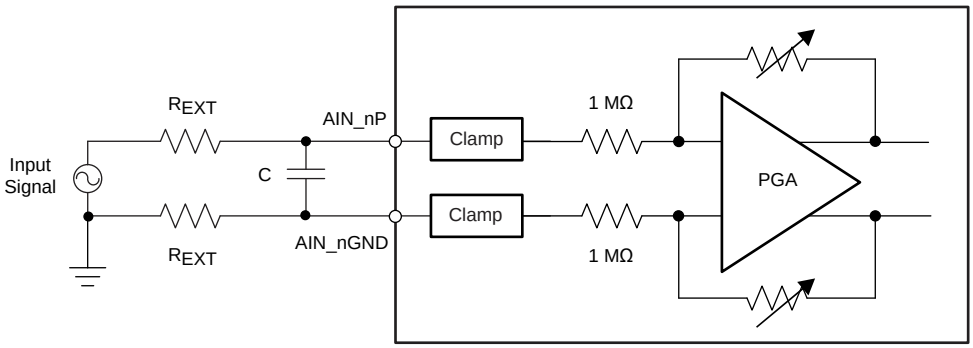

Figure 54. Matching Input Resistors on the Analog Inputs of Devices

The input overvoltage protection clamp on the ADS8586S is intended to control transient excursions on the input pins. Leaving the device in a state such that the clamp circuit is activated for extended periods of time in normal or power-down mode is not recommended because this fault condition can degrade device performance and reliability.

8.3.4 Programmable Gain Amplifier (PGA)

The device offers a programmable gain amplifier (PGA) at each individual analog input channel that converts the original single-ended input signal into a fully-differential signal to drive the internal 16-bit ADC. The PGA also adjusts the common-mode level of the input signal before being fed into the ADC to ensure maximum usage of the ADC input dynamic range. Depending on the range of the input signal, the PGA gain can be accordingly adjusted by configuring the RANGE pin of the ADC (see the *RANGE (Input)* section).

The PGA uses a very highly matched network of resistors for multiple gain configurations. Matching between these resistors and the amplifiers across all channels is accurately trimmed to keep the overall gain error low across all channels and input ranges.

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Feature Description (continued)

8.3.5 Third-Order, Low-Pass Filter (LPF)

In order to mitigate the noise of the front-end amplifiers and gain resistors of the PGA, each analog input channel of the ADS8586S features a third-order, Butterworth, antialiasing, low-pass filter (LPF) at the output of the PGA. Figure 55 and Figure 56, respectively, show the magnitude and phase response of the analog antialiasing filter. For maximum performance, the –3-dB cutoff frequency for the antialiasing filter is designed to be equal to 24 kHz for ±10-V range and 16 kHz for ±5-V range.

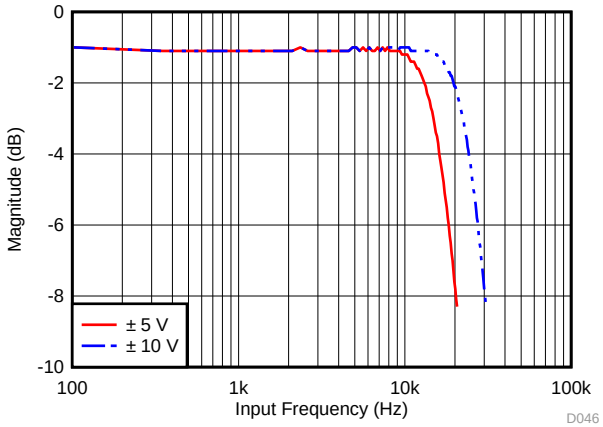

Figure 55. Third-Order LPF Magnitude Response

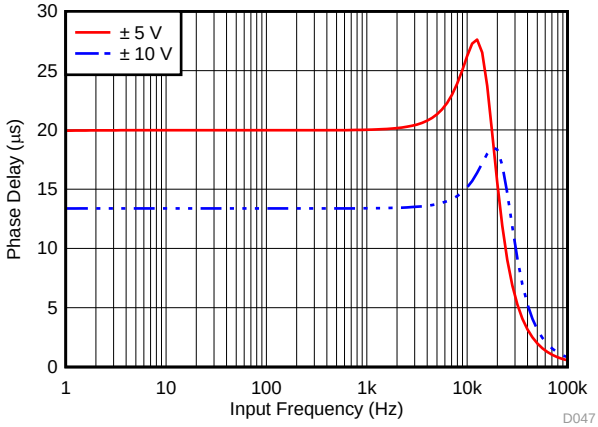

Figure 56. Third-Order LPF Phase Response

8.3.6 ADC Driver

In order to meet the performance of a 16-bit, SAR ADC at the maximum sampling rate (250 kSPS per channel), the capacitors at the input of the ADC must be successfully charged and discharged during the acquisition time window. The inputs of the ADC must settle to better than 16-bit accuracy before any sampled analog voltage gets converted. This drive requirement at the inputs of the ADC necessitates the use of a high-bandwidth, low-noise, and stable amplifier buffer. The ADS8586S features an integrated input driver as part of the signal chain for each analog input. This integrated input driver eliminates the need for any external amplifier, thus simplifying the signal chain design for the user.

8.3.7 Digital Filter and Noise

The ADS8586S features an optional digital averaging filter that can be used in slower throughput applications requiring lower noise and higher dynamic range. As explained in Table 1, the oversampling ratio of the digital filter is determined by the configuration of the OS[2:0] pins. The overall throughput of the ADC decreases proportionally with increase in the oversampling ratio.

Table 1. Oversampling Bit Decoding

OS[2:0]	OS RATIO	SNR ±10-V INPUT (dB)	SNR ±5-V INPUT (dB)	3-dB BANDWIDTH ±10-V INPUT (kHz)	3-dB BANDWIDTH ±5-V INPUT (kHz)	MAX THROUGHPUT PER CHANNEL (kSPS)
000	No OS	92.7	92.2	24	16	250
001	2	93.5	92.5	23	15.7	125
010	4	94.5	93.4	19.2	14.5	62.5
011	8	95.6	94.3	11.2	10.6	31.25
100	16	96.4	95.5	5.6	5.6	15.625
101	32	96.8	96.4	2.8	2.8	7.8125
110	64	97.1	96.9	1.4	1.4	3.906
111	Invalid	—	—	—	—	—

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In oversampling mode (see the *Oversampling Mode of Operation* section), the ADC takes the first sample for each channel at the rising edge of the CONVSTA, CONVSTB signals. After converting the first sample, the subsequent samples are taken by an internally generated sampling control signal. The samples are then averaged to reduce the noise of the signal chain as well as to improve the SNR of the ADC. The final output is also decimated to provide a 16-bit output for each channel. Table 1 lists the typical SNR performance for both the ±10-V and ±5-V input ranges, including the –3-dB bandwidth and proportional maximum throughput per channel. When the oversampling ratio increases, there is a proportional improvement in the SNR performance and decrease in the bandwidth of the input filter.

8.3.8 Reference

The ADS8586S can operate with either an internal voltage reference or an external voltage reference using an internal gain amplifier. The internal or external reference selection is determined by an external REFSEL pin, as explained in the *REFSEL (Input)* section. The REFIN/REFOUT pin outputs the internal band-gap voltage (in internal reference mode) or functions as an input to the external reference voltage (in external reference mode). In both cases, the on-chip amplifier is always enabled. Use this internal amplifier to gain the reference voltage and drive the actual reference input of the internal ADC core for maximizing performance. The REFCAPA (pin 45) and REFCAPB (pin 44) pins must be shorted together externally and a ceramic capacitor of 10 µF (minimum) must be connected between this node and REFGND (pin 43) to ensure that the internal reference buffer is operating as closed loop.

8.3.8.1 Internal Reference

The device has an internal 2.5-V (nominal value) band-gap reference. In order to select the internal reference, the REFSEL pin must be tied high or connected to DVDD. When the internal reference is used, REFIN/REFOUT (pin 42) becomes an output pin with the internal reference value. A 10-µF (minimum) decoupling capacitor, as shown in Figure 57, is recommended to be placed between the REFIN/REFOUT pin and REFGND (pin 43). The capacitor must be placed as close to the REFIN/REFOUT pin as possible. The output impedance of the internal band-gap creates a low-pass filter with this capacitor to band-limit the noise of the band-gap output. The use of a smaller capacitor increases the reference noise in the system, thus degrading SNR and SINAD performance. Do not use the REFIN/REFOUT pin to drive external ac or dc loads because of the limited current output capability of the pin. The REFIN/REFOUT pin can be used as a reference source if followed by a suitable op amp buffer.

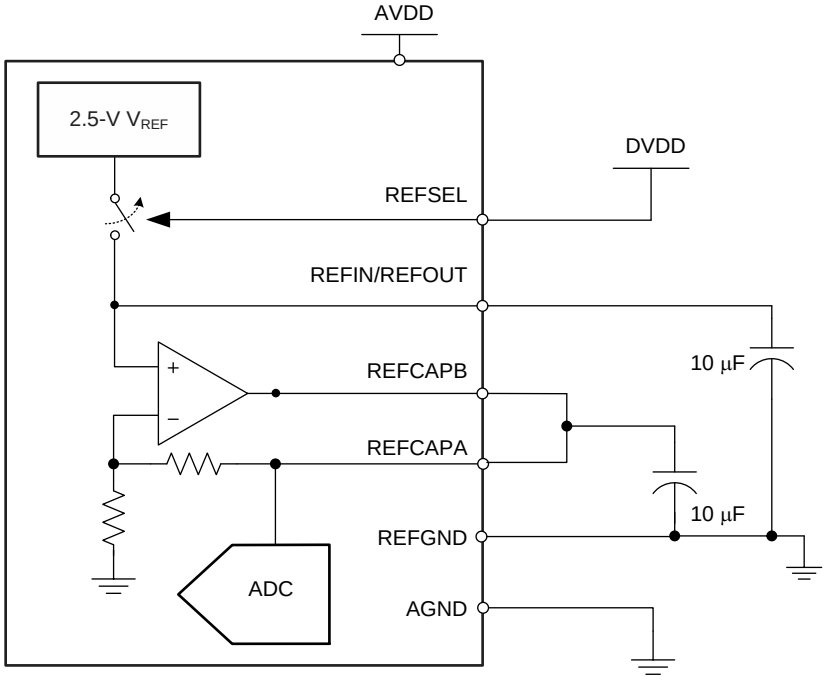

Figure 57. Device Connections for Using an Internal 2.5-V Reference

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The device internal reference is factory trimmed to a maximum initial accuracy of ±2.5 mV. The histogram in Figure 58 shows the distribution of the internal voltage reference output taken from more than 2100 production devices.

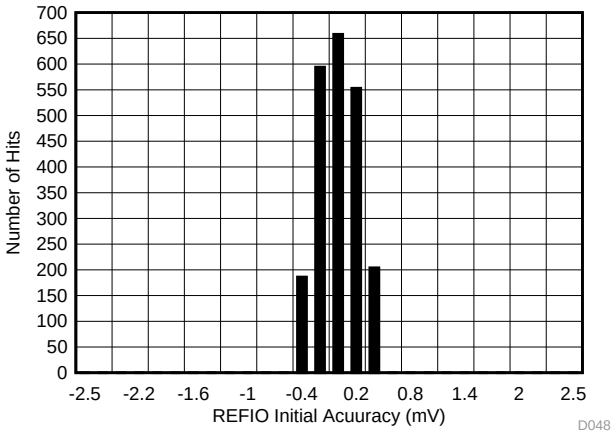

Figure 58. Internal Reference Accuracy at Room Temperature Histogram

The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical, thermal, or environmental stress (such as humidity). Heating the device when being soldered to a printed circuit board (PCB) and any subsequent solder reflow is a primary cause for shifts in the V_{REF} value. The main cause of thermal hysteresis is a change in die stress and therefore is a function of the package, die-attach material, and molding compound, as well as the layout of the device itself.

In order to illustrate this effect, 80 devices were soldered using lead-free solder paste with the suggested manufacturer reflow profile, as explained in the *AN-2029 Handling & Process Recommendations* application report. The internal voltage reference output is measured before and after the reflow process and Figure 59 shows the typical shift in value. Although all tested units exhibit a positive shift in the output voltages, negative shifts are also possible. The histogram in Figure 59 shows the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, which is common on PCBs with surface-mount components on both sides, causes additional shifts in the output voltage. If the PCB is to be exposed to multiple reflows, solder the ADS8586S in the second pass to minimize device exposure to thermal stress.

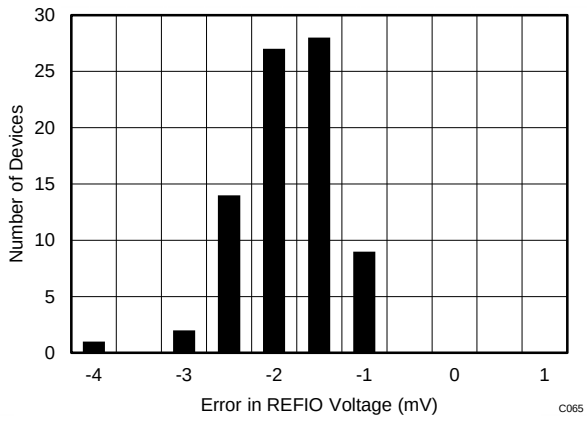

Figure 59. Solder Heat Shift Distribution Histogram

The internal reference is also temperature compensated to provide excellent temperature drift over an extended industrial temperature range of –40°C to 125°C. Figure 60 illustrates the variation of the internal reference voltage across temperature for different values of the AVDD supply voltage. The typical specified value of the reference voltage drift over temperature is 7.5 ppm/°C.

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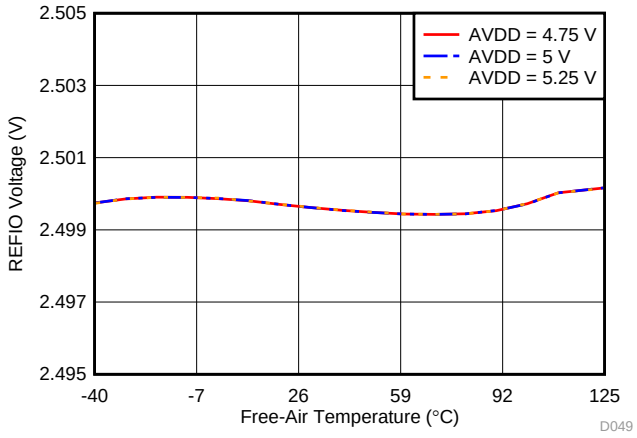

Figure 60. Variation of Internal Reference Output (REFIN/REFOUT) vs Supply and Temperature

8.3.8.2 External Reference

For applications that require a reference voltage with lower temperature drift or a common reference voltage for multiple devices, the ADS8586S offers a provision to use an external reference, using the internal buffer to drive the ADC reference pin. In order to select the external reference mode, either tie the REFSEL pin low or connect this pin to AGND. In this mode, an external 2.5-V reference must be applied at REFIN/REFOUT (pin 42), which becomes a high-impedance input pin. Any low-drift, small-size external reference can be used in this mode because the internal buffer is optimally designed to handle the dynamic loading on the ADC reference input. The output of the external reference must be filtered to minimize the resulting effect of the reference noise on system performance. Figure 61 shows a typical connection diagram for this mode.

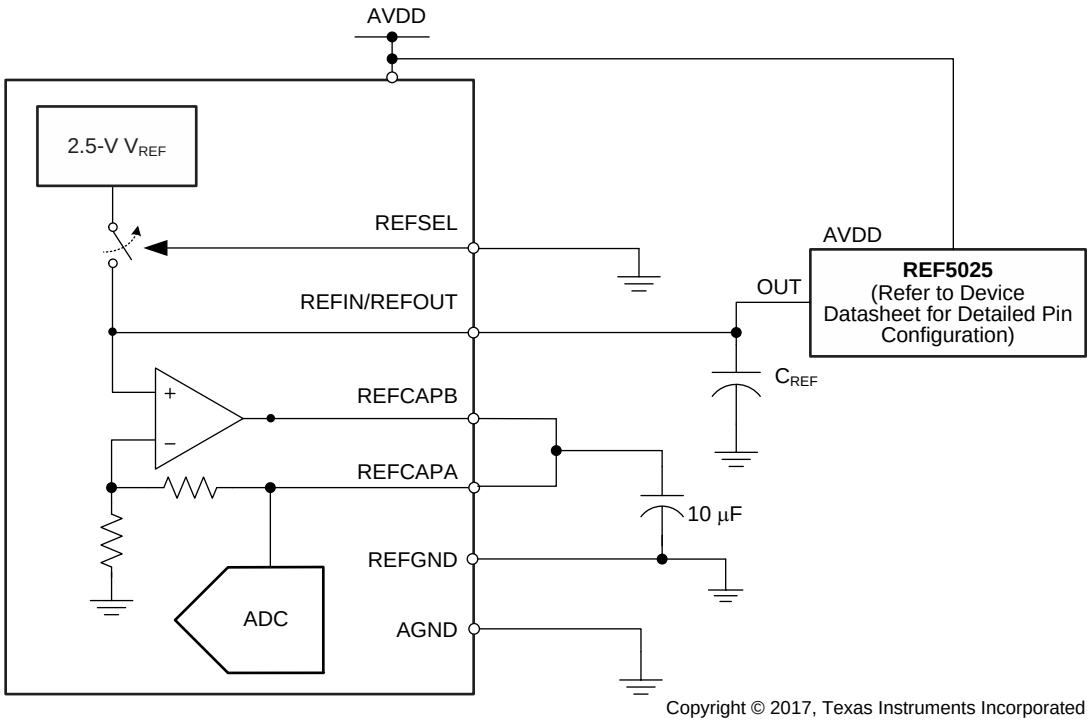

Figure 61. Device Connections for Using an External 2.5-V Reference

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For closed-loop operation of the internal reference buffer, the REFCAPA and REFCAPB pins must be externally shorted together. The output of the internal reference buffer appears at the REFCAP pin. A minimum capacitance of 10 μF must be placed between the REFCAPA, REFCAPB pins and REFGND (pin 43). Do not use this internal reference buffer to drive external ac or dc loads due to it's limited current output capability.

Figure 62 shows that the performance of the internal buffer output is very stable across the entire operating temperature range of –40°C to +125°C. Figure 63 shows that the typical specified value of the reference buffer drift over temperature is 5 ppm/°C.

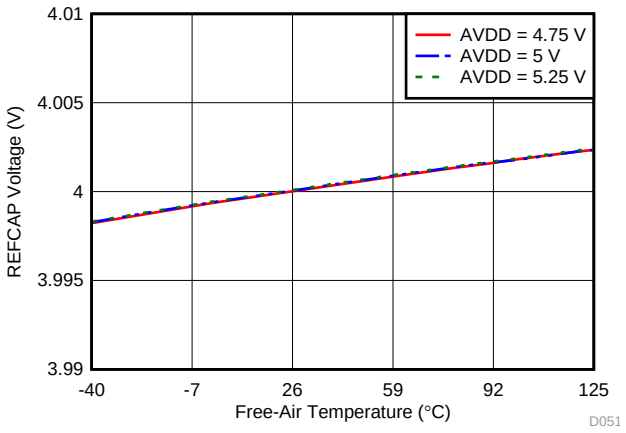

Figure 62. Variation of Reference Buffer Output (REFCAPA, REFCAPB) Across Supply and Temperature

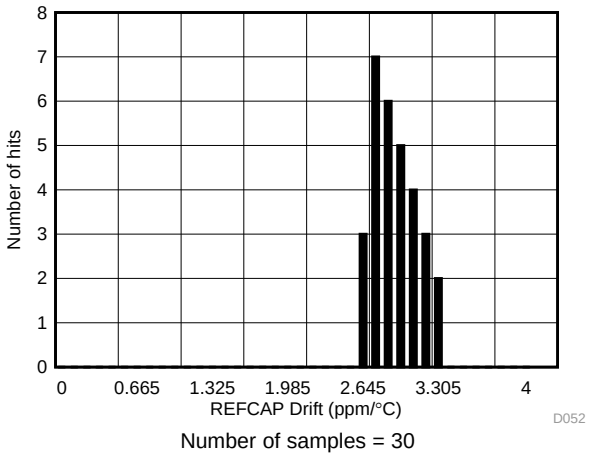

Figure 63. Reference Buffer Temperature Drift Histogram

8.3.8.3 Supplying One V_{REF} to Multiple Devices

For applications that require multiple ADS8586S devices, using the same reference voltage source for all the ADCs helps eliminate any potential errors in the system resulting from mismatch between multiple reference sources.

Figure 64 shows the recommended connection diagram for an application that uses one device in internal reference mode and provides the reference source for other devices. The device used as source of the voltage reference is bypassed by a 10-μF capacitor on the REFIN/REFOUT pin, whereas the other devices are bypassed with a 100-nF capacitor.

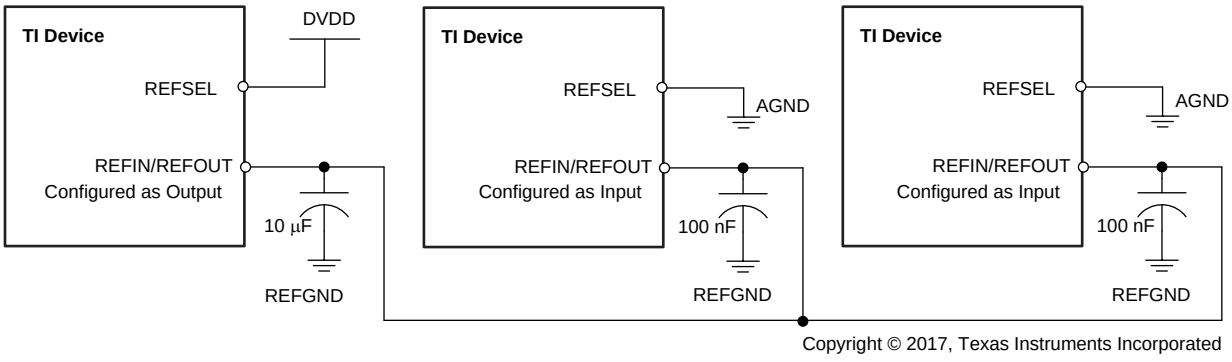

Figure 64. Multiple Devices Connected With an Internal Reference From One Device

Figure 65 shows the recommended connection diagram for an application that uses an external voltage reference (such as the REF5025) to provide the reference source for multiple devices.

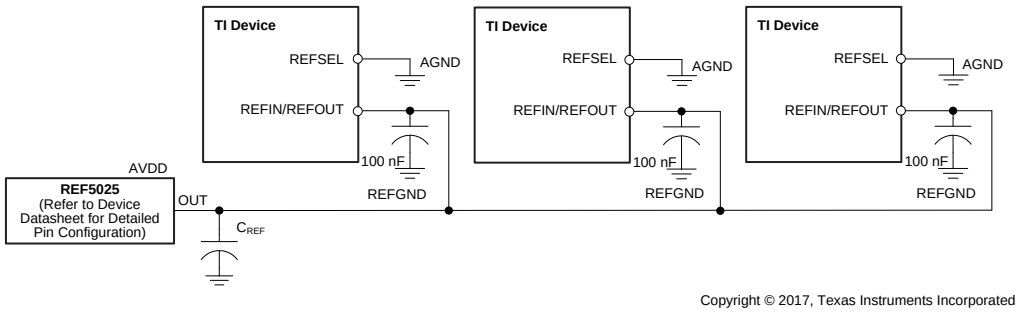

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Figure 65. Multiple Devices Connected Using an External Reference

8.3.9 ADC Transfer Function

The ADS8586S is a multichannel device that supports two single-ended, bipolar input ranges of ±10 V and ±5 V on all input channels. The device outputs 16 bits of conversion data in binary twos complement format for both bipolar input ranges. The format for the output codes is the same across all analog channels.

Figure 66 shows the ideal transfer characteristic for each ADC channel for all input ranges. The full-scale range (FSR) for each input signal is equal to the difference between the positive full-scale (PFS) input voltage and the negative full-scale (NFS) input voltage. The LSB size is equal to FSR / 2^{16} = FSR / 65536 because the resolution of the ADC is 16 bits. Table 2 lists the LSB values corresponding to the different input ranges.

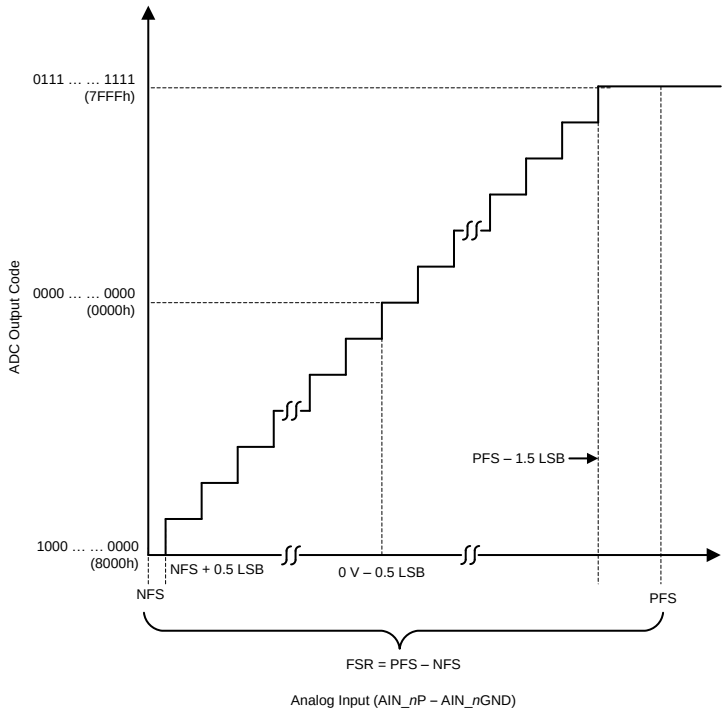

Figure 66. 16-Bit ADC Transfer Function (Twos Complement Binary Format)

Table 2. ADC LSB Values for Different Input Ranges

INPUT RANGE (V)	POSITIVE FULL-SCALE (V)	NEGATIVE FULL-SCALE (V)	FULL-SCALE RANGE (V)	LSB (µV)
±10	10	–10	20	305.18
±5	5	–5	10	152.59

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8.4 Device Functional Modes

8.4.1 Device Interface: Pin Description

8.4.1.1 REFSEL (Input)

The REFSEL pin is a digital input pin that enables selection between the internal and external reference mode of operation for the device. If the REFSEL pin is set to logic high, then the internal reference is enabled and selected. If this pin is set to logic low, then the internal band-gap reference circuit is disabled and powered down. In this mode, an external reference voltage must be provided to the REFIN/REFOUT pin. Under both conditions, the internal reference buffer is always enabled.

The REFSEL pin is an asynchronous logic input. The device output on the REFIN/REFOUT pin starts changing immediately with a change in state of the REFSEL input pin. During power-up, the device wakes up in internal or external reference mode depending on the state of the REFSEL input pin.

8.4.1.2 RANGE (Input)

The RANGE pin is a digital input pin that allows the input range to be selected for all analog input channels. If this pin is set to logic high, the device is configured to operate in the ±10-V input range for all input channels. If this pin is set to logic low, then all input channels operate in the ±5-V input range.

In applications where the input range remains the same for all input channels, the RANGE pin is recommended to be hardwired to the appropriate signal. However, some applications can require an on-the-fly change in the input range by the digital host. For such cases, the RANGE pin functions as an asynchronous input, meaning that any change in the logic input results in an immediate change in the input range configuration of the device. An additional 80 µs must typically be allowed in addition to the device acquisition time for the internal active circuitry to settle to the required accuracy before initiating the next conversion.

The RANGE pin is also used to put the device in standby or shutdown mode depending on the state of the $\overline{\text{STBY}}$ input pin, as explained in the *Power-Down Modes* section.

8.4.1.3 $\overline{\text{STBY}}$ (Input)

The $\overline{\text{STBY}}$ pin is a digital input pin used to put the device into one of the two power-down modes: standby or shut down. Set the $\overline{\text{STBY}}$ pin to logic high for normal device operation. If this pin is set to logic low, the device enters either standby mode or shutdown mode depending on the state of the RANGE input pin. Both of these modes are low-power modes supported by the device. In shutdown mode, all internal circuitry is powered down, but in standby mode the internal reference and regulators remain powered to enable a relatively quicker recovery to normal operation.

The $\overline{\text{STBY}}$ pin functions as an asynchronous input, meaning that this pin can be pulled low at anytime during device operation to put the device into one of the two power-down modes. However, if the $\overline{\text{STBY}}$ input is set high to bring the device out of power-down mode, then wait for the specified recovery time, as specified in the *Timing Requirements: Exit Standby Mode* table for proper operation. See the *Power-Down Modes* section for more details on device operation in the two power-down modes.

8.4.1.4 $\overline{\text{PAR}}$/SER/BYTE SEL (Input)

The $\overline{\text{PAR}}$/SER/BYTE SEL pin is a digital input pin that selects between the parallel, serial, or parallel byte interface for reading the data output from the device. If this pin is tied to logic low, then the device operates in the parallel interface mode (see the *Parallel Data Read* section). If this pin is tied to logic high, then the serial or parallel byte interface mode is selected depending on the state of the DB15/BYTE SEL pin. If the DB15/BYTE SEL is tied low, then serial mode is selected (see the *Serial Data Read* section) and the parallel byte interface is selected if this pin is tied high (see the *Parallel Byte Data Read* section).

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Device Functional Modes (continued)

8.4.1.5 CONVSTA, CONVSTB (Input)

Conversion start A (CONVSTA) and conversion start B (CONVSTB) are active-high, conversion control digital input signals. CONVSTA can be used to simultaneously sample and initiate the conversion process for the first half count of device input channels (channels 1-3 for the ADS8586S), whereas CONVSTB can be used to simultaneously sample and initiate the conversion process for the latter half count of device input channels (channels 4-6 for the ADS8586S). For simultaneous sampling of all input channels, both pins can be shorted together and a single CONVST signal can be used to control the conversion on all input channels. However, in the oversampling mode of operation (see the *Oversampling Mode of Operation* section), both the CONVSTA and CONVSTB signals must be tied together.

On the rising edge of the CONVSTA, CONVSTB signals, the internal track-and-hold circuits for each analog input channel are placed into hold mode and the sampled input signal is converted using an internal clock. The CONVSTA, CONVSTB signals can be pulled low when the internal conversion is over, as indicated by the BUSY signal (see the *BUSY (Output)* section). At this point, the front-end circuit for all analog input channels acquires the respective input signals and the internal ADC is not converting. The output data can be read from the device irrespective of the status of the CONVSTA, CONVSTB pins, as there is no degradation in device performance, as explained in the *Data Read Operation* section.

8.4.1.6 RESET (Input)

The RESET pin is an active-high digital input. A dedicated reset pin allows the device to be reset at any time in an asynchronous manner. All digital circuitry in the device is reset when the RESET pin is set to logic high and this condition remains active until the pin returns low. The device must always be reset after power-up as well as after recovery from shut-down mode when all the supplies and references have settled to the required accuracy. If the RESET is issued during an ongoing conversion process, then the device aborts the conversion and output data are invalid. If the reset signal is applied during a data read operation, then the output data registers are all reset to zero.

In order to initiate the next conversion cycle after deactivating a reset condition, allow for a minimum time delay between the falling edge of the RESET input and the rising edge of the CONVSTA, CONVSTB inputs (see the *Timing Requirements: CONVST Control* table). Any violation in this timing requirement can result in corrupting the results from the next conversion.

8.4.1.7 $\overline{RD}$/SCLK (Input)

$\overline{RD}$/SCLK is a dual-function pin. Table 3 explains the usage of this pin under different operating conditions of the device.

Table 3. $\overline{RD}$/SCLK Pin Functionality

DEVICE OPERATING CONDITION		FUNCTIONALITY OF THE $\overline{RD}$/SCLK INPUT
Parallel interface	$\overline{PAR}$/SER/BYTE SEL = 0 DB15/BYTE SEL = 0	Functions as an active-low digital input pin to read the output data from the device. In parallel or parallel byte interface mode, the output bus is enabled when both the $\overline{CS}$ and $\overline{RD}$ inputs are tied to a logic low input (see the *Data Read Operation* section).
Parallel byte interface	$\overline{PAR}$/SER/BYTE SEL = 1 DB15/BYTE SEL = 1	
Serial interface	$\overline{PAR}$/SER/BYTE SEL = 1 DB15/BYTE SEL = 0	Functions as an external clock input for the serial data interface. In serial mode, all synchronous accesses to the device are timed with respect to the rising edge of the SCLK signal (see the *Serial Data Read* section).

8.4.1.8 $\overline{CS}$ (Input)

The $\overline{CS}$ pin indicates an active-low, chip-select signal. A rising edge on the $\overline{CS}$ signal outputs all the data lines in tri-state mode. This function allows multiple devices to share the same output data lines. The falling edge of the $\overline{CS}$ signal marks the beginning of the output data transfer frame in any interface mode of operation for the device. In the parallel and parallel byte interface modes, both the $\overline{CS}$ and $\overline{RD}$ input pins must be driven low to enable the digital output bus for reading the conversion data (DB[15:0] for parallel and DB[7:0] for parallel byte interface). In serial mode, the falling edge of the $\overline{CS}$ signal takes the DOUTA, DOUTB serial data output lines out of tri-state mode and outputs the MSB of the previous conversion result.

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8.4.1.9 OS[2:0]

The OS[2:0] pins are active-high digital input pins used to configure the oversampling ratio for the internal digital filter on the device. OS2 is the MSB control bit and OS0 is the LSB control bit. Table 1 provides the decoding of the OS[2:0] bits for different oversampling rates. As described in Table 1, an increase in the OSR mode improves the typical SNR performance for both input ranges and reduces the 3-dB input bandwidth as well as the maximum-allowed throughput per channel.

8.4.1.10 BUSY (Output)

BUSY is an active-high digital output signal. This pin goes to logic high after the rising edges of both the CONVSTA and CONVSTB signals, indicating that the front-end, track-and-hold circuits for all input channels are in hold mode and that the ADC conversion has started. When the BUSY signal goes high, any activity on the CONVSTA or CONVSTB inputs has no effect on the device. The BUSY output remains high until the conversion process for all channels is completed and the conversion data are latched into the output data registers for read out. If the conversion data is read for the previous conversion when BUSY is high, ensure that the data read operation is complete before the falling edge of the BUSY output.

8.4.1.11 FRSTDATA (Output)

FRSTDATA is an active-high digital output signal that indicates if the conversion data output for the first analog input channel of the ADC (AIN_1P and AIN_1GND) is being read out in either of the interface modes. The FRSTDATA output pin comes out of tri-state when the $\overline{CS}$ input is pulled from a high to a low logic level. Table 4 indicates the functionality of the FRSTDATA output in different interface modes of the device.

Table 4. FRSTDATA Pin Functionality

DEVICE OPERATING CONDITION		FUNCTIONALITY OF THE FRSTDATA OUTPUT
Parallel mode	$\overline{PAR}$/SER/BYTE SEL = 0, DB15/BYTE SEL = 0	The first falling edge of the $\overline{RD}$ signal corresponding to the output result of channel 1 sets the FRSTDATA output to a logic high level. This setting indicates that the data output from channel 1 is being read on the parallel output bus (DB[15:0]). The FRSTDATA output goes low at the next falling edge of the $\overline{RD}$ signal and remains low until the conversion data output from all other channels is read.
Parallel byte mode	$\overline{PAR}$/SER/BYTE SEL = 1, DB15/BYTE SEL = 1	The first falling edge of the $\overline{RD}$ signal corresponding to one byte of the output of channel 1 sets the FRSTDATA output to a logic high level. This setting indicates that one byte of the data output from channel 1 is being read on the parallel output bus (DB[7:0]). The FRSTDATA output remains high at the next falling edge of the $\overline{RD}$ signal to read the second byte of the channel 1 output. This pin goes low on the third falling edge of the $\overline{RD}$ signal and remains low until the conversion data output from all other channels is read.
Serial mode	$\overline{PAR}$/SER/BYTE SEL = 1, DB15/BYTE SEL = 0	The FRSTDATA output goes to a logic high state on the falling edge of the $\overline{CS}$ signal when the MSB of the channel 1 conversion result is output on DOUTA at this instant. The FRSTDATA pin goes low at the 16th falling edge of the SCLK input, indicating that all 16 bits of the channel 1 output has been read. This pin remains low until the conversion data output from all other channels is read.

8.4.1.12 DB15/BYTE SEL

DB15/BYTE SEL is a dual-function, digital input, output pin.

When the device operates in parallel interface mode ($\overline{PAR}$/SER/BYTE SEL = 0), this pin functions as a digital output. In this mode, this pin outputs the MSB of the conversion data when both the $\overline{CS}$ and $\overline{RD}$ signals are pulled low.

When the device does not operate in parallel interface mode ($\overline{PAR}$/SER/BYTE SEL = 1), this pin functions as a digital control input pin to select between the serial and parallel byte interface modes. The device operates in the serial interface mode when the DB15/BYTE SEL pin is tied low and the device operates in the parallel byte interface mode when this pin is tied to a logic high input.

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8.4.1.13 DB14/HBEN

DB14/HBEN is a dual-function, digital input, output pin

When the device operates in parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 0), this pin functions as a digital output. In this mode, this pin outputs the (MSB-1) bit or bit 14 of the conversion data when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are pulled low.

When the device operates in parallel byte interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1), this pin functions as a digital control input pin that selects if the MSB byte or the LSB byte is output first. If the DB14/HBEN pin is tied to logic high, then the MSB byte is output first followed by the LSB byte and vice-versa if this pin is tied to logic low.

When the device operates in serial interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0), this pin must be tied to AGND or to a logic low input.

8.4.1.14 DB[13:9]

DB[13:9] are digital output pins. In parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 0), these pins output bit 13 to bit 9 of the conversion result for each analog channel when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are pulled low. When the device is not in parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1), these pins must be tied to AGND or to a logic low input.

8.4.1.15 DB8/DOUTB

DB8/DOUTB is a dual-function digital output pin.

In parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 0), use this pin to output bit 8 of the conversion result for each analog channel when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are pulled low.

When the device operates in parallel byte interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1), this pin remains in a tri-state mode.

In serial interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0), this pin outputs the conversion data for the second half count of device input channels (channels 4-6 for the ADS8586S).

8.4.1.16 DB7/DOUTA

DB7/DOUTA is a dual-function digital output pin.

In parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 0), use this pin to output bit 7 of the conversion result for each analog channel when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are pulled low.

When the device operates in parallel byte interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1), this pin outputs the MSB of the output byte of the conversion data.

In serial interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0), use this pin to output conversion data for the first half count of device input channels (channels 1-3 for the ADS8586S).

8.4.1.17 DB[6:0]

DB[6:0] are digital output pins.

In parallel interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 0), these pins output bit 6 to bit 0 (LSB) of the conversion result for each analog channel when both the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ signals are pulled low.

When the device operates in parallel byte interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 1), these pins along with the DB7 pin output the 16-bit conversion result in MSB-first fashion in two consecutive $\overline{\text{RD}}$ operations.

When the device operates in serial interface mode ($\overline{\text{PAR}}$/SER/BYTE SEL = 1 and DB15/BYTE SEL = 0), these pins must be tied to AGND or to a logic low input.

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8.4.2 Device Modes of Operation

The ADS8586S supports multiple modes of operation that can be programmed using the hardware pins. This functionality allows the device to be easily configured without any complicated software programming. This section provides details about the normal, power-down (standby and shutdown), and oversampling modes of operation of the device.

8.4.2.1 Power-Down Modes

For applications that are sensitive to power consumption, the ADS8586S offers a built-in, power-down feature. The device supports two power-down modes: standby mode and shutdown mode. As shown in Table 5, the device can enter either power-down mode by pulling the $\overline{\text{STBY}}$ pin to a logic low level. Additionally, the selection between these two power-down modes is done by the state of the RANGE pin.

Table 5. Power-Down Mode Selection

POWER-DOWN MODE	$\overline{\text{STBY}}$	RANGE
Standby	0	1
Shutdown	0	0

8.4.2.1.1 Standby Mode

The device supports a low-power standby mode in which only part of the circuit is powered down. The analog front-end, signal-conditioning circuit for each channel remains powered down in this mode, but the internal reference and regulator are not powered down. In standby mode, the total power consumption of the device is typically equal to 19 mW.

In order to enter standby mode, the $\overline{\text{STBY}}$ input pin must be set to logic low and the RANGE input pin must be set to a logic high value. The device can be asynchronously put into this mode by configuring the $\overline{\text{STBY}}$ and RANGE inputs at anytime during device operation.

The device exits standby mode when a logic high input is applied to the $\overline{\text{STBY}}$ pin. At this time, the internal circuitry starts powering up and takes a minimum time of 100 µs to settle before the next conversion can be initiated. See the *Timing Requirements: Exit Standby Mode* table and Figure 8 for timing details.

8.4.2.1.2 Shutdown Mode

The device supports a low-power shutdown mode in which the entire internal circuitry is powered down. In shutdown mode, the total power consumption of the device is typically equal to 1 µW.

In order to enter shutdown mode, the $\overline{\text{STBY}}$ input pin must be set to logic low and the RANGE input pin must be set to a logic low value. The device can be asynchronously put into this mode by configuring the $\overline{\text{STBY}}$ and RANGE inputs at anytime during device operation.

The device exits shutdown mode when a logic high input is applied to the $\overline{\text{STBY}}$ pin. At this time, the internal circuitry starts powering up and takes a minimum time of 13 ms to settle in external reference mode before the next conversion can be initiated. After recovery from shutdown mode, a RESET signal must be applied before the next conversion can be initiated. See the *Timing Requirements: Exit Shutdown Mode* table and Figure 9 for timing details.

8.4.2.2 Conversion Control

The ADS8586S offers easy and precise control to simultaneously sample all analog input channels or pairs of input channels. The sampling instant can be user-controlled through the digital pins, CONVSTA and CONVSTB. Simultaneously capturing the input signal on all analog input channels is extremely useful in certain applications that are sensitive to additional phase delay between input channels caused by sequential sampling. This section describes the methodology to simultaneously sample all input channels or pairs of input channels for the device.

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8.4.2.2.1 Simultaneous Sampling on All Input Channels

The ADS8586S allows all the analog input channels to be simultaneously sampled. In order to do so, the CONVSTA and CONVSTB signals (as shown in Figure 67) must be tied together and a single CONVST signal must be used to control the sampling of all analog input channels of the device. Figure 67 also shows the sequence of events described in this section.

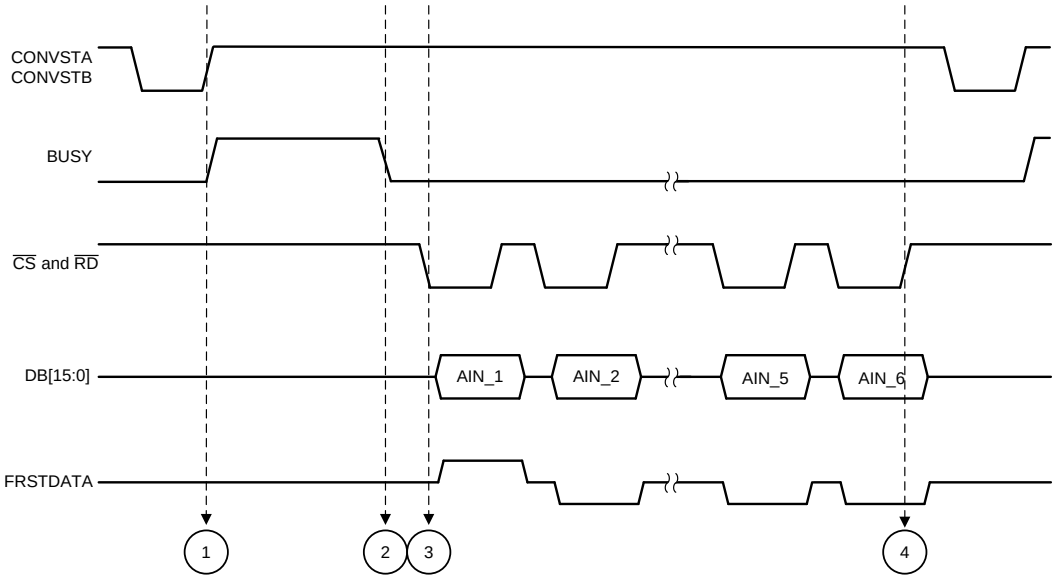

Figure 67. Simultaneous Sampling of All Input Channels in Parallel Interface Timing Diagram

There are four events that describe the internal operation of the device when all input channels are simultaneously sampled and the data are read back. These events are:

- ***Event 1:*** Simultaneous sampling of all analog input channels is initiated with the rising edge of the CONVST signal. The input signals on all channels are sampled at this same instant because both the CONVSTA and CONVSTB inputs are tied together. The sampled signals are then converted by the ADC using a precise on-chip oscillator clock. At the beginning of the conversion phase of the ADC, the BUSY output goes high and remains high through a maximum-specified conversion time of t_{CONV} (see the *Timing Requirements: CONVST Control* table).
- ***Event 2:*** At this instant, the ADC has completed the conversion for all input channels and the BUSY output goes to logic low. The falling edge of the BUSY signal indicates end of conversion and that the internal registers are updated with the conversion data. At this instant, the device is ready to output the correct conversion results for all channels on the parallel output bus (DB[15:0]), serial output lines (DOUTA, DOUTB), or parallel byte bus (DB[7:0]).
- ***Event 3:*** This example shows the data read operation in parallel interface mode with both $\overline{CS}$ and $\overline{RD}$ tied together. After BUSY goes low, the first falling edges of $\overline{CS}$ and $\overline{RD}$ output the conversion result of channel 1 (AIN_1) on the parallel output bus. Similarly, the conversion results for the remaining channels are output on the parallel bus on subsequent falling edges of the $\overline{CS}$ and $\overline{RD}$ signals in a sequential manner. If all channels are not used in the conversion process, tie the unused channels to AGND or any known voltage within the selected input range. The ADC always converts all analog input channels and the results for unused channels are included in the output data stream, thus all unused channels must be tied. The FRSTDATA output goes high on the first falling edges of the $\overline{CS}$ and $\overline{RD}$ signals, indicating that the parallel bus is carrying the output result from channel 1. On the next falling edges of the $\overline{CS}$ and $\overline{RD}$ signals, FRSTDATA goes low and stays low if the $\overline{CS}$ and $\overline{RD}$ inputs are low.
- ***Event 4:*** After the conversion results for all analog channels are output from the device, the data frame can be terminated by pulling the $\overline{CS}$ and $\overline{RD}$ signals to logic high. The parallel bus and FRSTDATA output go to tri-state until the entire sequence is repeated beginning from event 1.

Events 1 and 2 are common to all interface modes of operation (parallel, serial, or parallel byte).

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8.4.2.2.2 Simultaneous Sampling Two Sets of Input Channels

The ADS8586S allows two sets of analog input channels to be simultaneously sampled. In order to do so, the CONVSTA and CONVSTB signals must be separate control inputs (as shown in Figure 68) and the device must not operate in any oversampling mode. Electrical grid relay protection is an application that can benefit from being able to sample the inputs in two groups. The delay of the signal through the voltage channels is often different from the delay on the channels measuring current. The difference in delay created by the voltage and current signal paths can be corrected by adjusting the sampling of the two groups of inputs (voltage and current) to the device.

The timing diagram of Figure 68 shows the sequence of events described in this section.

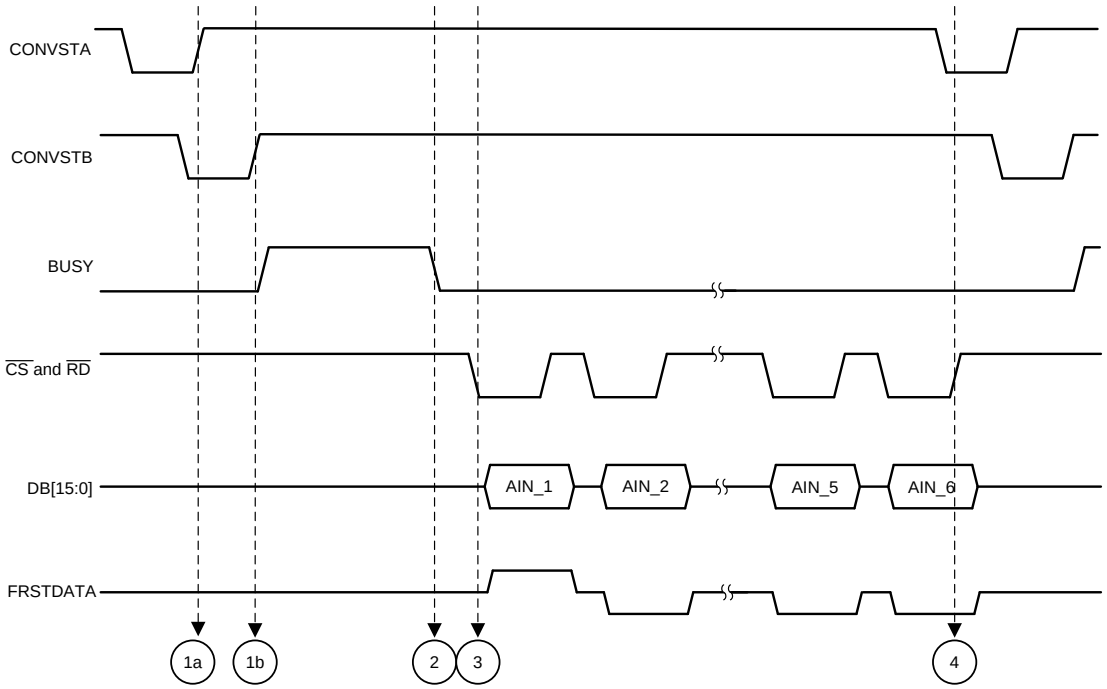

Figure 68. Simultaneous Sampling of All Input Channels in Parallel Interface Timing Diagram

There are four events that describe the internal operation of the device when pairs of input channels are simultaneously sampled and the data are read back. These events are:

- ***Event 1(a):*** A rising edge on the CONVSTA signal initiates simultaneous sampling of the first set of analog input channels (channels 1-3 for the ADS8586S). The sampling circuits on the first set of analog input channels enter hold mode and the input signals on these channels are sampled at the same instant. The ADC does not begin conversion until the input signals on the second set of channels are sampled.
- ***Event 1(b):*** A rising edge on the CONVSTB signal initiates simultaneous sampling of the second set of analog input channels (channels 4-6 for the ADS8586S). The sampling circuits for the second set of analog input channels enter hold mode and the input signals on these channels are sampled at the same instant. When the rising edges of both the CONVSTA and CONVSTB signals have occurred, the ADC converts all sampled signals using a precise, on-chip oscillator clock. At the beginning of the conversion phase of the ADC, the BUSY output goes high and remains high through a maximum-specified conversion time of t_{CONV} (see the *Timing Requirements: CONVST Control* table).
- ***Event 2:*** Same as event 2 in the *Simultaneous Sampling on All Input Channels* section.
- ***Event 3:*** Same as event 3 in the *Simultaneous Sampling on All Input Channels* section.
- ***Event 4:*** Same as event 4 in the *Simultaneous Sampling on All Input Channels* section.

Events 1(a), 1(b), and 2 are common to all interface modes of operation (parallel, serial, or parallel byte).

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8.4.2.3 Data Read Operation

The ADS8586S updates the internal data registers with the conversion data for all analog channels at the end of every conversion phase (when BUSY goes low). As described in the *Timing Requirements: Data Read Operation* table, if the output data are read after BUSY goes low, then the device outputs the conversion results for the current sample. However, if the output data are read when BUSY is high, then the device outputs conversion results for the previous sample. Under both conditions, the device supports three interface options depending on the status of the PAR/SER/BYTE SEL and DB15/BYTE SEL pins, as explained in Table 6.

Table 6. Data Read Back Interface Mode Selection

SELECTED INTERFACE MODE	PAR/SER/BYTE SEL	DB15/BYTE SEL
Parallel interface	0	0
Parallel byte interface	1	1
Serial interface	1	0

8.4.2.3.1 Parallel Data Read

The ADS8586S supports a parallel interface mode for reading the device output data using the control inputs (CS and RD) the parallel output bus (DB[15:0]), and the BUSY indicator. This interface mode is selected by applying a logic low input on the PAR/SER/BYTE SEL input pin. Depending on the application requirements, the CS and RD control inputs can be tied together or used as separate control inputs in the parallel interface mode.

For applications that use only one device in the system and does not share the parallel output bus with any other devices, the CS and RD input signals can be tied together. Alternatively, the CS signal can be permanently tied low and the RD signal can be used to clock the data out of the device. The timing diagram for this mode of operation is described in the *Timing Requirements: Parallel Data Read Operation, CS and RD Tied Together* table. In this mode the parallel output bus, DB[15:0], is activated (comes out of tri-state) on the falling edge of the CS/RD signal. At the first falling edge of the CS/RD signal, the output data of channel 1 becomes available on the parallel bus to be read by the digital host. At this instant the FRSTDATA output also goes high, indicating channel 1 data are ready to be read back. The output data for the remaining channels are clocked out on the parallel bus on subsequent falling edges of the CS and RD signal in a sequential manner.

For applications that use multiple devices in the system, the CS and RD input signals must be driven separately. The timing diagram for this mode of operation is described in the *Timing Requirements: Parallel Data Read Operation, CS and RD Separate* table. A falling edge of the CS input can be used to activate the parallel bus for a particular device in the system. The RD signal clocks the conversion data out of the device. At the first falling edge of the RD signal, the output data of channel 1 become available on the parallel bus to be read by the digital host. At this instant the FRSTDATA output also goes, high indicating channel 1 data are ready to be read back. On subsequent falling edges of the RD signal, the output data for the remaining channels are clocked out on the parallel bus in a sequential manner. At the second falling edge of the RD signal, the FRSTDATA output goes low and remains low until going to tri-state at the next rising edge of the CS signal.

8.4.2.3.2 Parallel Byte Data Read

The ADS8586S supports a parallel byte interface mode for reading the device output data using the control inputs (CS and RD) the parallel output bus (DB[15:0]), and the BUSY indicator. This interface mode is selected by applying a logic high input on the PAR/SER/BYTE SEL input pin and a logic high input on the DB15/BYTE SEL input pin. The parallel byte interface mode is very similar to the parallel interface mode, except that the output data for each channel is read in two data transfers of 8-bit byte sizes.

The order of most significant byte (MSB byte) and least significant byte (LSB byte) is decided by the logic input state of the DB14/HBEN pin. In parallel byte mode, the DB14/HBEN pin functions as a control input. When DB14/HBEN pin is tied high, the MSB byte of the conversion results is output first followed by the LSB byte. This order is reversed when DB14/HBEN is tied to logic low.

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The *Timing Requirements: Byte Mode Data Read Operation* table describes the data read back operation during parallel byte mode when the DB14/HBEN pin is tied high. A falling edge of the $\overline{CS}$ input is used to activate the parallel bus, DB[7:0] for the device. The $\overline{RD}$ signal is then used to clock the conversion data out of the device. In this mode, two $\overline{RD}$ pulses are required to read the full data output for each analog channel. At the first falling edge of the $\overline{RD}$ signal, the first byte of the channel 1 conversion result becomes available on DB[7:0]. This byte is followed by the second byte of conversion data on the next falling edge of the $\overline{RD}$ signal. On subsequent falling edges of the $\overline{RD}$ signal, the output data for the remaining channels are clocked out in chunks of 8-bit bytes on DB[7:0] in a sequential manner. Thus, a total of 12 $\overline{RD}$ pulses are required to read the output from all input channels of the ADS8586S.

In this mode, the FRSTDATA output goes high at the first falling of the $\overline{RD}$ signal. FRSTDATA remains high for two $\overline{RD}$ pulses until both bytes of the channel 1 conversion result are output. At the third falling edge of the $\overline{RD}$ signal, the FRSTDATA output goes low and remains low throughout the data read operation until going to tri-state at the next rising edge of the $\overline{CS}$ signal.

8.4.2.3.3 Serial Data Read

The ADS8586S also supports a serial interface mode for reading the device output data. This interface mode is selected by applying a logic high input on the PAR/$\overline{SER}$/BYTE SEL input pin and a logic low input on the DB15/BYTE SEL input pin. This interface mode uses a $\overline{CS}$ control input, a communication clock input (SCLK), BUSY and FRSTDATA output indicators, and serial data output lines DOUTA and DOUTB.

Figure 5 illustrates the timing diagram for data read in serial mode for one channel of the ADC, framed by the $\overline{CS}$ signal. When the $\overline{CS}$ input is high, the serial data output and FRSTDATA output lines are in tri-state and the SCLK input is ignored. On the falling edge of the $\overline{CS}$ signal, the output lines become active and the MSB of the conversion result comes out on DOUTA, DOUTB. The MSB can be read by the host processor on the next falling edge of the SCLK signal. The remaining 15 bits of the conversion result are output on the subsequent rising edges of the SCLK signal and can be read by the host processor on the corresponding falling edges. Thus, a total of 16 SCLK cycles are required to clock out 16 bits of conversion result for each channel and the same process can be repeated for the remaining channels in an ascending order. The $\overline{CS}$ input can be left at a logic low level for the entire data retrieval process for all analog channels or used to frame the retrieval of the 16-bit output data for each analog channel.

The ADS8586S can output the conversion results on one or both of the serial data output lines, DOUTA and DOUTB. The conversion results from the first set of channels (channels 1-3 for the ADS8586S) appear first on DOUTA, followed by the second set of channels (channels 4-6 for the ADS8586S) if only DOUTA is used for reading data. This order is reversed for DOUTB, in which the second set of channels appear first followed by the first set of channels. The use of both data output lines reduces the time needed for data retrieval and a higher throughput can therefore be achieved in this mode.

The FRSTDATA output is in tri-state when the $\overline{CS}$ signal is high. As illustrated in Figure 5, FRSTDATA goes high on the first falling edge of the $\overline{CS}$ signal when the MSB of channel 1 is output on DOUTA. The FRSTDATA output remains high for the next 16 SCLK cycles until all data bits of channel 1 are read from the device. The FRSTDATA output returns to a logic low level at the 16th falling edge of the SCLK signal. If data are also read on DOUTB in the serial mode, then FRSTDATA remains high when the first channel of the second set of channels is read from the device. The high state of FRSTDATA corresponds to channel 4 for the ADS8586S.

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Based on the previous description of the different pins in serial interface mode, conversion data can be read out of the device in several different ways. Some example recommendations are provided as follows:

- The conversion data can be read out of the device using only one of the two serial output lines, DOUTA or DOUTB. In this case, using DOUTA for output data read back is recommended because channel 1 data appear first on DOUTA followed by the data for other channels in ascending order. To read the data for all channels, provide a total of 16 × 6 = 96 SCLK cycles for the ADS8586S. This entire data frame can be created within a single $\overline{CS}$ pulse or each group of 16 SCLK cycles can be individually framed by the $\overline{CS}$ signal. The primary disadvantage of using just one data line for reading conversion data is that the throughput is reduced if a data read operation is performed after conversion. Figure 69 shows this operation.
- Alternatively, only DOUTB can be used for reading the conversion data from all channels. In this case, everything else remains the same and the output bit stream contains data for all channels in the following order: channels 4, 5, 6, 1, 2, and 3 for the ADS8586S. Figure 69 shows this operation.

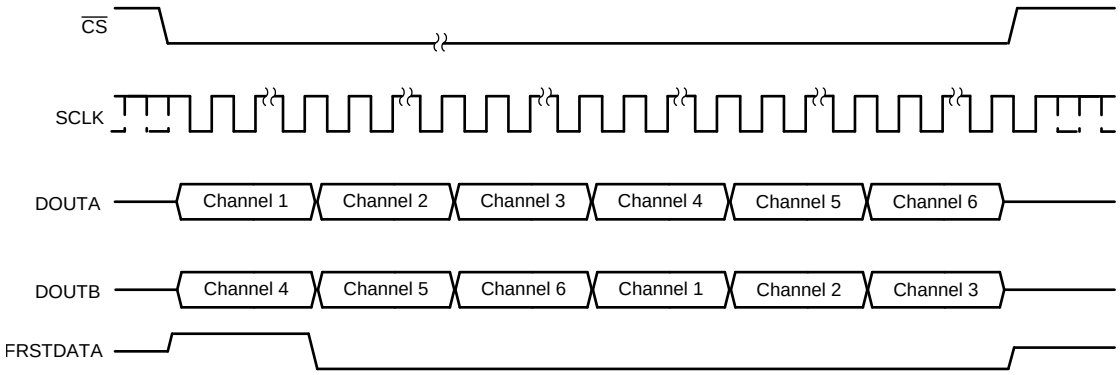

Figure 69. Data Read Back in the Serial Interface Using Either DOUTA or DOUTB Timing Diagram

- In order to minimize the time for the data read operation in serial mode, both DOUTA and DOUTB can be used to read data out of the device. In this case, the conversion results from the first set of channels (channels 1-3 for the ADS8586S) appear on DOUTA and the conversion results from the second set of channels (channels 4-6 for the ADS8586S) appear first on DOUTB. To read the data for all channels, provide a total of 16 × 3 = 48 SCLK cycles for the ADS8586S. This entire data frame can be created within a single $\overline{CS}$ pulse or each group of 16 SCLK cycles can be individually framed by the $\overline{CS}$ signal. Figure 70 shows an example timing diagram.

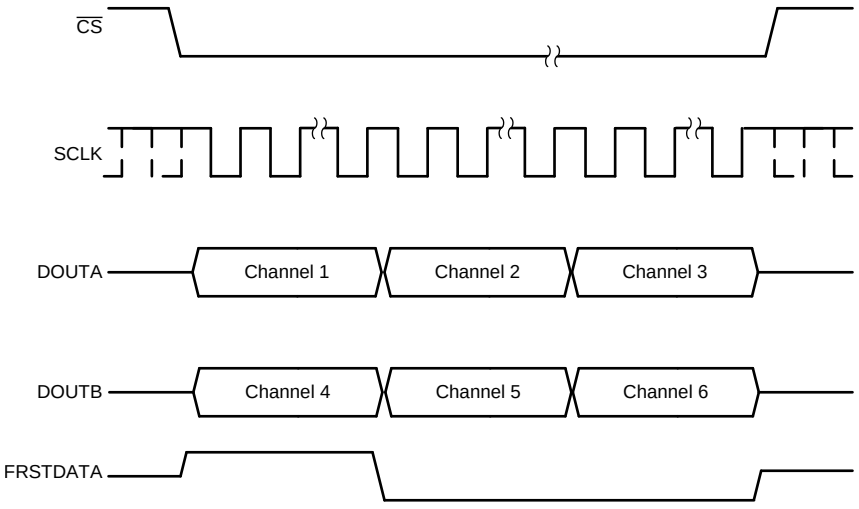

Figure 70. Data Read Back in the Serial Interface Using Both DOUTA and DOUTB Timing Diagram

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8.4.2.3.4 Data Read During Conversion

The ADS8586S supports data read operation when the BUSY output is high and the internal ADC is converting. The ADC outputs conversion results for previous samples if data read back is performed during an ongoing conversion. Any of the three interface modes (parallel, parallel byte, or serial) in any combination of oversampling modes can be used to read the device output during an ongoing conversion. The data read back during conversion mode allows faster throughput to be achieved from the device. There is no degradation in performance if the data is read from the device during the conversion process, using any of the three interface modes.

The *Timing Requirements: Data Read Operation* table describes the timing diagram for data read back during conversion. The timing specification t_{DZ_CSBSY} (the delay between the rising edge of the $\overline{CS}$ signal and the falling edge of the BUSY signal) must be met because the output data registers are updated with the current conversion results just before the falling edge of the BUSY signal and any read operation during this time can corrupt the register update.

8.4.2.4 Oversampling Mode of Operation

The ADS8586S supports the oversampling mode of operation using an on-chip averaging digital filter, as explained in the *Digital Filter and Noise* section. The device can be configured in oversampling mode by the OS[2:0] pins (see the *OS[2:0]* section). Figure 71 shows a typical timing diagram for the oversampling mode of operation. The input on the OS pins is latched on the falling edge of the BUSY signal to configure the oversampling rate for the next conversion.

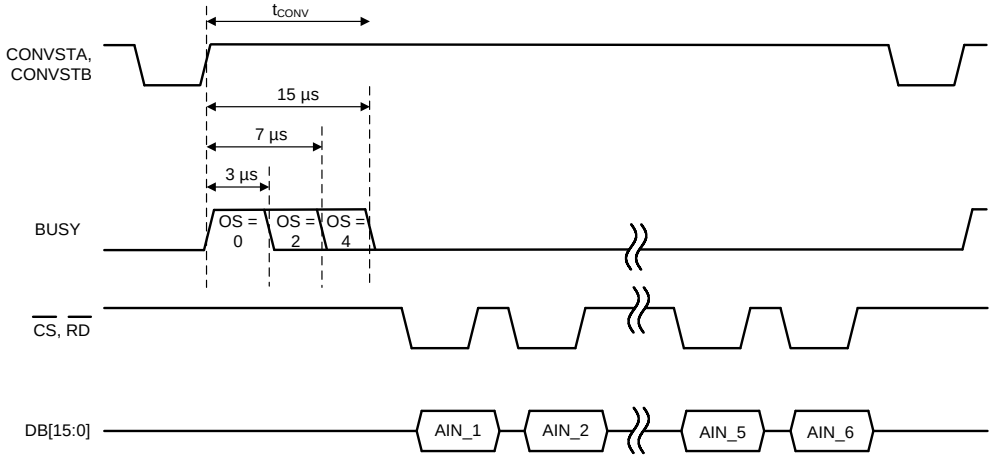

Figure 71. OSR Mode Operation Timing Diagram

In the oversampling mode of operation, both the CONVST A and CONVST B signals must be tied together or driven together. As shown in Figure 71, the BUSY signal duration varies with the OSR setting because the conversion time increases with increases in OSR, The high time for the BUSY signal increases with the OSR setting, as listed in the *Timing Requirements: CONVST Control* table.

For any particular OSR setting, the maximum achievable throughput per channel is specified in Table 1. If the application is running at a lower throughput, then a higher OSR setting can be selected for further noise reduction and SNR improvement. To maximize the throughput per channel, perform a data read when BUSY is high and a conversion is ongoing in OSR mode. This process enables data read for the previous conversion (see the *Data Read During Conversion* section). At the falling edge of the BUSY signal, the internal data registers are updated with the new conversion data; thus the read operation must complete and $\overline{CS}$ must be pulled high for at least t_{SU_CSBSY} before BUSY goes low (see the *Timing Requirements: Data Read Operation* table).

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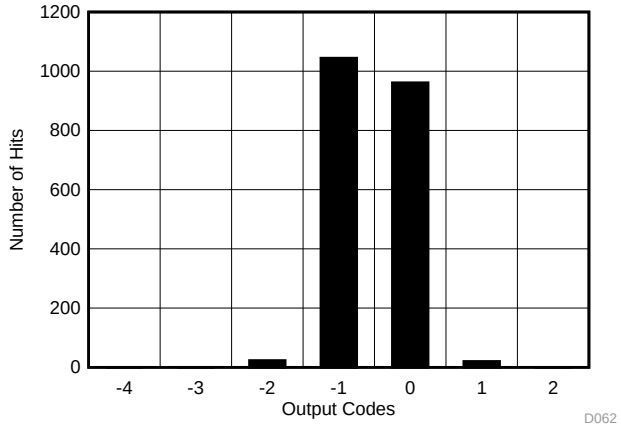
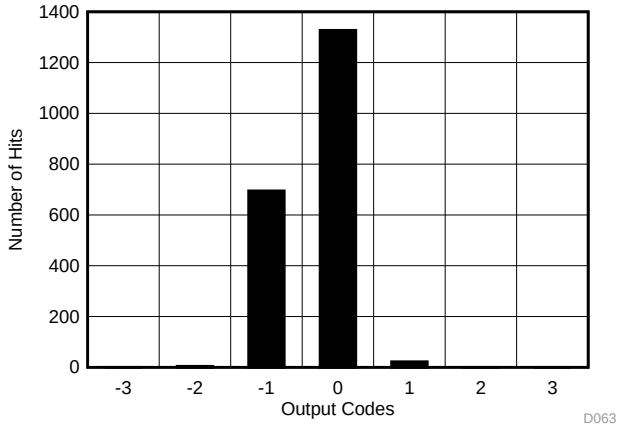
Oversampling the input signal reduces noise during the conversion process, thus reducing the histogram code spread for a dc input signal to the ADC. Figure 72 to Figure 77 show the effect of oversampling on the output code spread in a dc histogram plot.



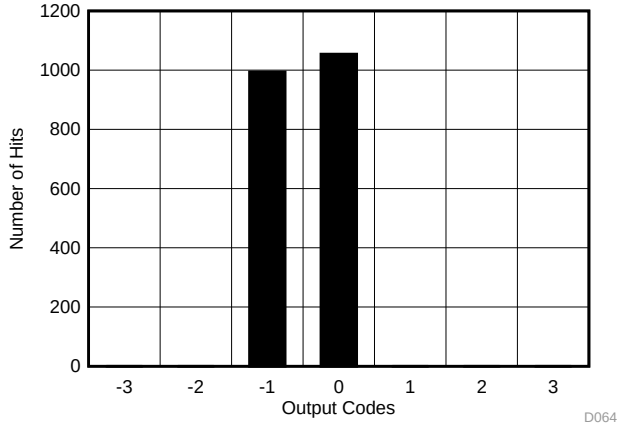
Mean = –0.52, sigma = 0.47

Figure 72. DC Histogram for OSR2



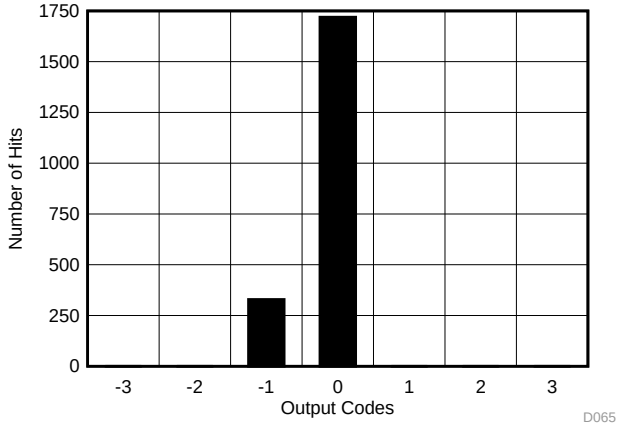
Mean = –0.33, sigma = 0.41

Figure 73. DC Histogram for OSR4



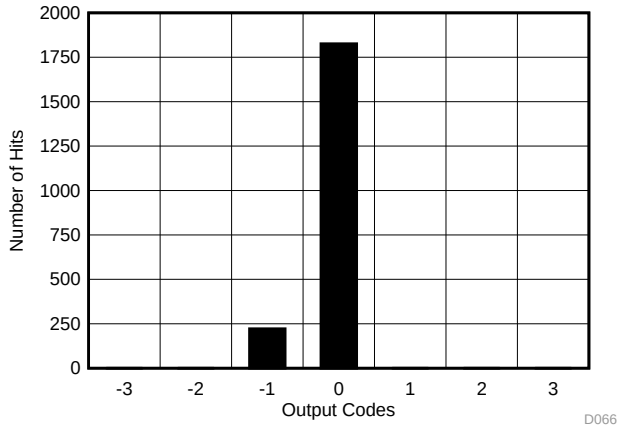
Mean = –0.49, sigma = 0.36

Figure 74. DC Histogram for OSR8



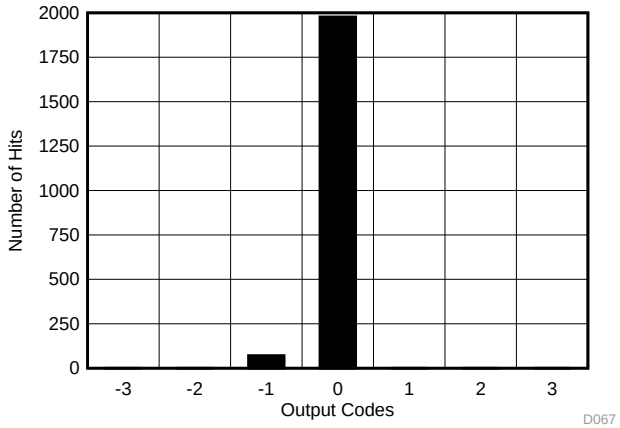
Mean = –0.16, sigma = 0.33

Figure 75. DC Histogram for OSR16



Mean = –0.11, sigma = 0.32

Figure 76. DC Histogram for OSR32



Mean = –0.03, sigma = 0.31

Figure 77. DC Histogram for OSR64

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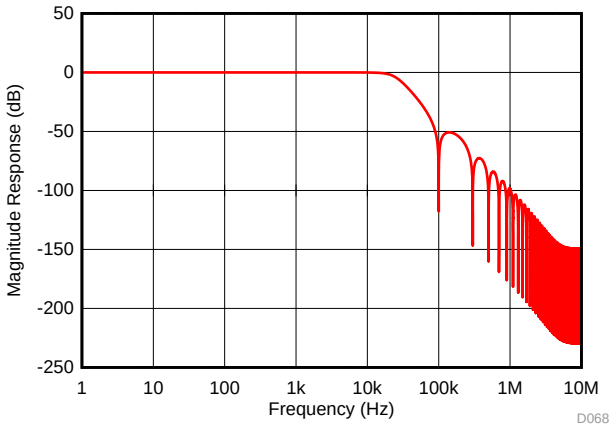
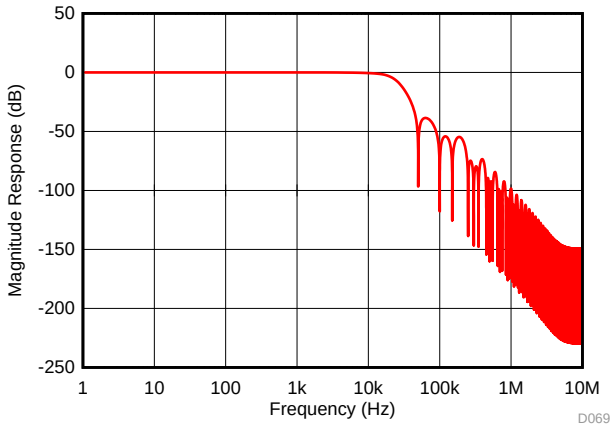
In OSR modes, the device adds a digital filter at the output of the ADC. The digital filter affects the frequency response of the entire data acquisition system including the internal low-pass analog filter and the oversampling digital filter. Figure 78 to Figure 83 show the frequency response curves for different OSR settings in the ±10-V range.



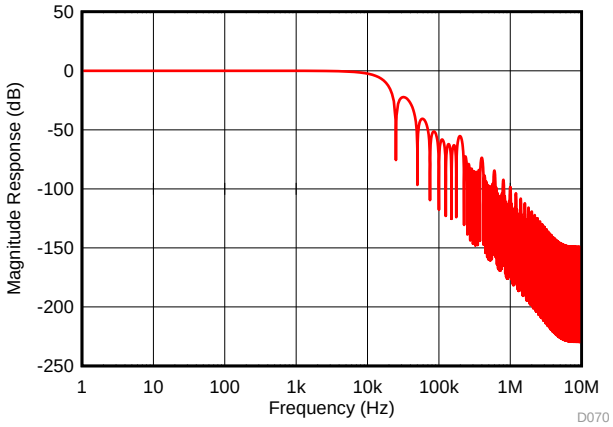
AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 78. Digital Filter Response for OSR = 2



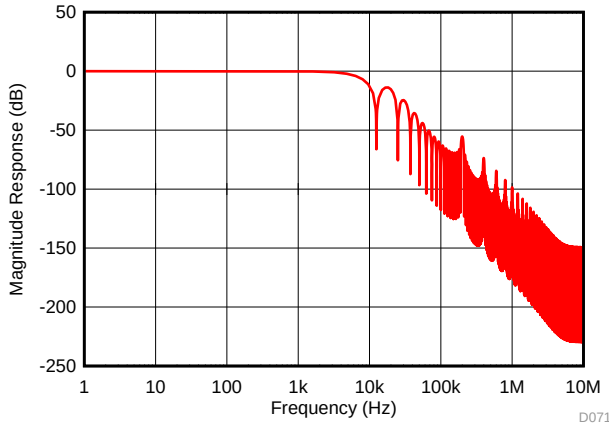
AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 79. Digital Filter Response for OSR = 4



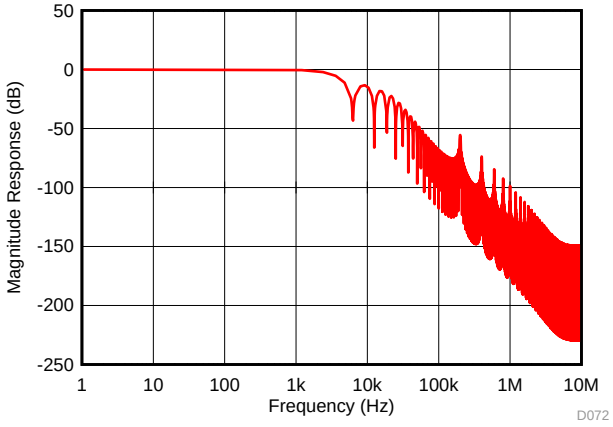
AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 80. Digital Filter Response for OSR = 8



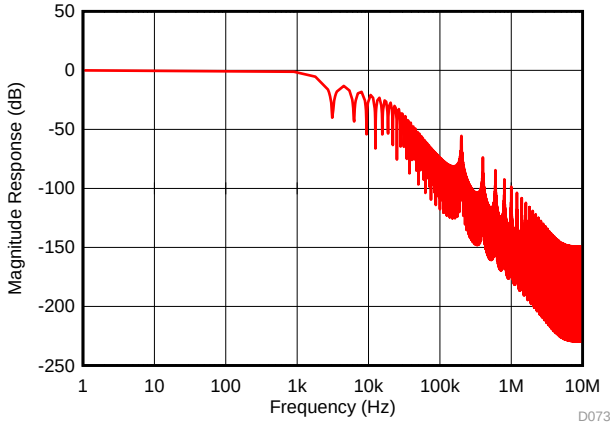
AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 81. Digital Filter Response for OSR = 16



AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 82. Digital Filter Response for OSR = 32



AVDD = 5 V, DVDD = 5 V, T_A = 25°C, input range = ±10 V

Figure 83. Digital Filter Response for OSR = 64

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9 Application and Implementation

NOTE

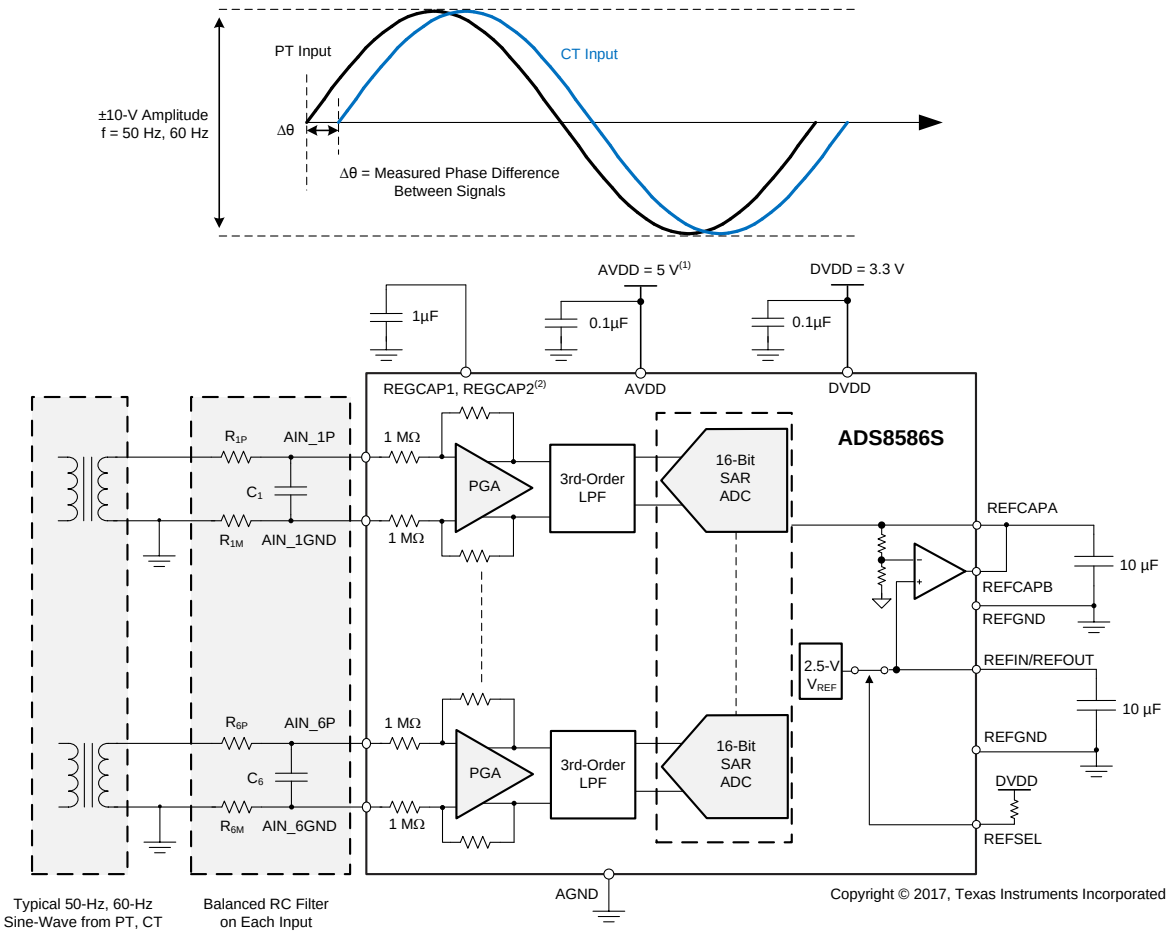
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS8586S enables high-precision measurement of up to six analog signals simultaneously. The device is a fully-integrated data acquisition system based on a 16-bit data acquisition (DAQ) system based on a 16-bit successive approximation (SAR) analog-to-digital converter (ADC). The device includes an integrated analog front-end for each input channel and an integrated voltage reference with a precision reference buffer. As such, this device does not require any additional active circuits for driving the reference analog input pins of the ADC.

9.2 Typical Application

9.2.1 6-Channel, Data Acquisition System (DAQ) for Power Automation



(1) Decoupling the AVDD capacitor applies to each AVDD pin.

(2) REGCAP1 and REGCAP2: each pin requires separate decoupling capacitors.

(3) PT: Potential transformer.

(4) CT: Current transformer.

Figure 84. 6-Channel DAQ for Power Automation Using the ADS8586S

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Typical Application (continued)

This application example involves the measurement of electrical variables in a power system. The accurate measurement of electrical variables in a power grid is extremely critical because this measurement helps to determine the operating status and running quality of the grid. Such accurate measurements also help to diagnose potential problems with the power network so that these problems can be resolved quickly without having any significant service impact. The key electrical parameters include amplitude, frequency, and phase measurement of the voltage and current on the power lines. These parameters are important to enable metrology in the power automation system to perform harmonic analysis, power factor calculation, power quality assessment, and so forth.

9.2.1.1 Design Requirements

To begin the design process, a few parameters must be decided upon. The designer must know the following:

- Output range of the potential transformers (elements labeled PT in Figure 84)
- Output range of the current transformers (elements labeled CT in Figure 84)
- Input impedance required from the analog front-end for each channel
- Fundamental frequency of the power system
- Number of harmonics that must be acquired
- Type of signal conditioning required from the analog front end for each channel

9.2.1.2 Detailed Design Procedure

For the ADS8586S, each channel incorporates an analog front end composed of a programmable gain amplifier (PGA), analog low-pass filter, and ADC input driver. The analog input for each channel presents a constant resistive impedance of 1 MΩ independent of the ADC sampling frequency and range setting. The high input impedance of the analog front end circuit allows direct connection to potential transformers (PT) and current transformers (CT). The ADC inputs can support up to ±10-V or ± 5-V bipolar inputs and the integrated signal conditioning eliminates the need for external amplifiers or ADC driver circuits.

The PT and CT used in the system, as illustrated in Figure 84, have a ±10-V output range. Although the PT and CT provide isolation from the power system, a series resistor must be placed on the analog input channels. The series resistor helps limit the input current to ±10 mA if the input voltages exceed ±15 V. For applications that require protection against overvoltage or fast transient events beyond the specified absolute maximum ratings of the device, an external protection clamp circuit using transient voltage suppressors (TVS) and ESD diodes is recommended.

A low-pass filter is used on each analog input channel to eliminate high-frequency noise pickup and minimize aliasing. Figure 85 shows an example of the recommended configuration for an input RC filter. A balanced RC filter configuration matches the external source resistance on the positive path (AIN_nP) with an equal resistance on the negative path (AIN_nGND). Matching the source impedance in the positive and negative path allows for better common-mode noise rejection and helps in maintaining the DC accuracy of the system by canceling any additional offset error contributed by the external series resistance.

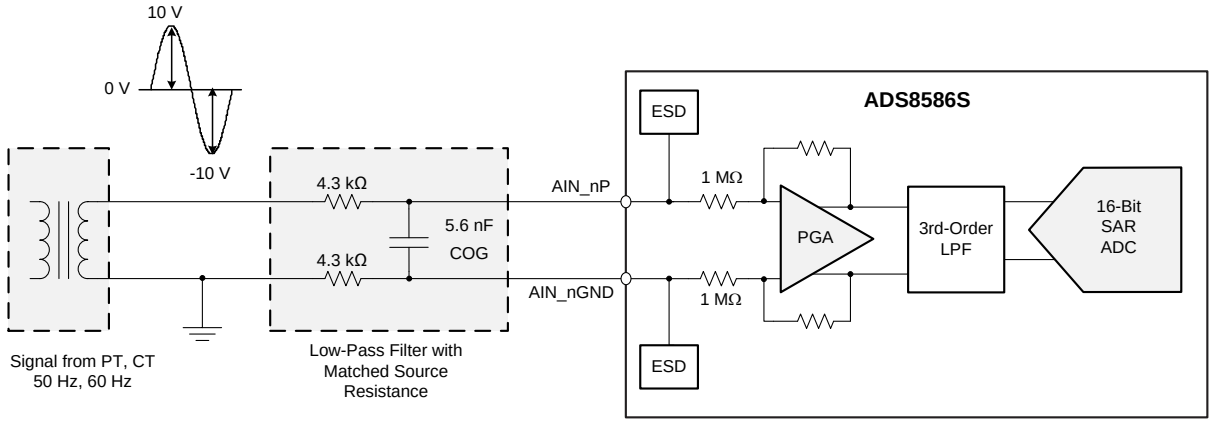

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Figure 85. Input RC Low-Pass Filter

Typical Application (continued)

The primary goal of the data acquisition system illustrated in Figure 84 is to measure up to 20 harmonics in a 60-Hz power network. Thus, the analog front-end must have sufficient bandwidth to detect signals up to 1260 Hz, as shown in Equation 1.

$$f_{MIN} = (20 + 1) \times 60\,Hz = 1260\,Hz \quad (1)$$

Based on the bandwidth calculated in Equation 1, the ADS8586S is set to simultaneously sample all six channels at 20 kSPS, which is sufficient throughput to clearly resolve the highest harmonic component of the input signal. The pass band of the low-pass filter configuration shown in Figure 85 is determined by the –3-dB frequency, calculated according to Equation 2.

$$f_{-3dB} = \frac{1}{2\pi \times (R1 + R2) \times C_f} = \frac{1}{2\pi \times (4.3k\Omega + 4.3k\Omega) \times 5.6nF} = 3.3\,kHz \quad (2)$$

The value of C_F is selected as 5.6 nF, a standard capacitance value available in 0603-size surface-mount components. In combination with the resistor R_F, this low-pass filter provides sufficient bandwidth to accommodate the required 20 harmonics for the input signal of 60 Hz.

The ADS8586S can operate with either the internal voltage reference or an external reference. The *Internal Reference* section describes the electrical connections and recommended bypass capacitors when using the internal reference. Alternatively for applications that require a higher precision voltage reference, Figure 86 shows an example of an external reference circuit. The REF5025 provides a very low drift, and very accurate external 2.5-V reference. The resistor R_{FILT} and capacitor C_{FILT} form a low-pass filter to reduce the broadband noise and minimize the resulting effect of the reference noise on the system performance.

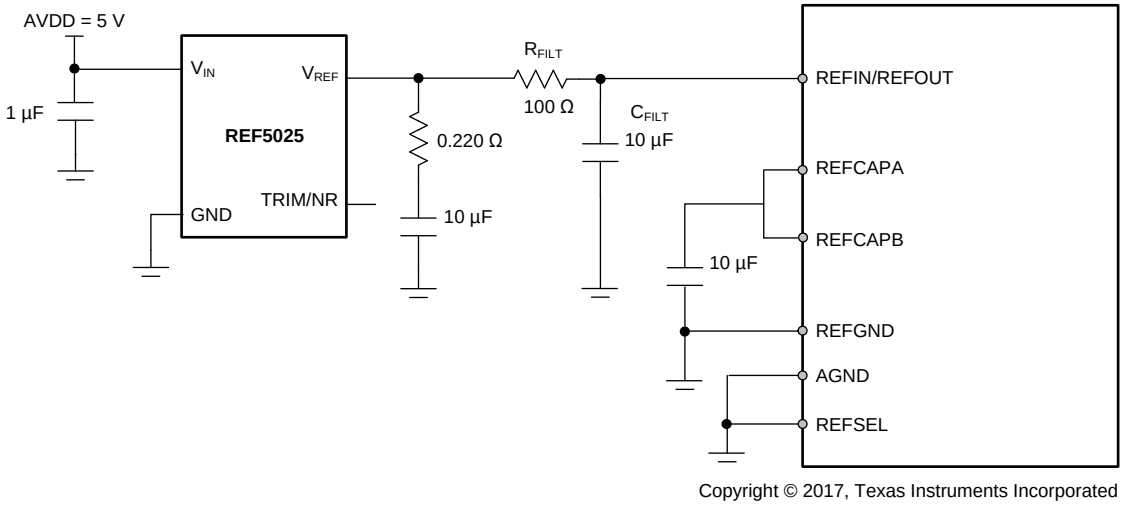

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Figure 86. External Reference Circuit for the ADS8586S

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Typical Application (continued)

9.2.1.3 Application Curve

Figure 87 shows the frequency spectrum of the data acquired by the ADS8586S for a sinusoidal, ±10-V input at 60 Hz.

The ac performance parameters measured by this design are:

- SNR = 92.75 dB; SINAD = 92.6 dB
- THD = –107 dB; SFDR = 110.7 dB

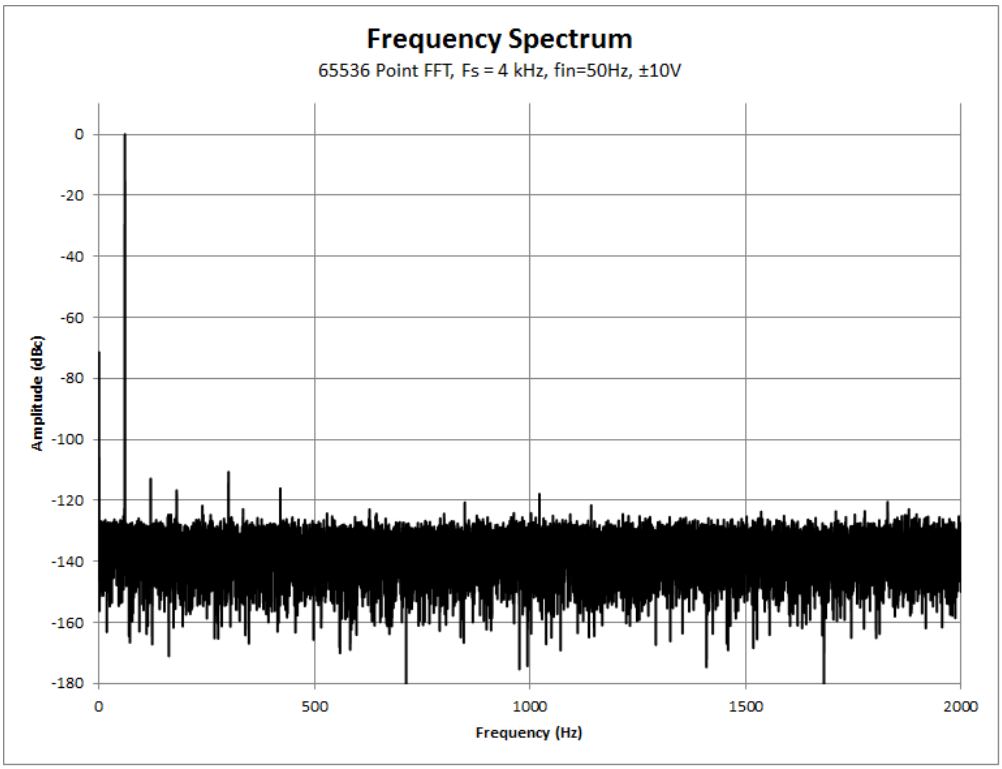

Figure 87. Frequency Spectrum for a Sinusoidal ±10-V Signal at 50 Hz

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10 Power Supply Recommendations

The ADS8586S uses two separate power supplies: AVDD and DVDD. The AVDD supply provides power to the ADC and internal circuits, and DVDD is used for the digital interface. AVDD and DVDD can be set independently to voltages within the permissible range.

The AVDD supply can be set in the range of 4.75 V to 5.25 V. A low-noise, linear regulator is recommended to generate the analog supply voltage. The device has four AVDD pins. Each AVDD pin must be decoupled with respect to AGND using a 1-µF capacitor. Place the 1-µF capacitor as close to the supply pins as possible.

The DVDD supply is used to drive the digital I/O buffers and can be set in the range of 2.3 V to a maximum value equal to the AVDD voltage. This range allows the device to interface with most state-of-the-art processors and controllers. Place a 1-µF (minimum 100-nF) decoupling capacitor in close proximity to the DVDD supply to provide the high-frequency digital switching current.

There are no specific requirements with regard to the power-supply sequencing of the device. However, issue a reset after the supplies are powered up and are stable to ensure the device is properly configured.

The typical PSRR curve with the decoupling capacitors is as shown in Figure 88.

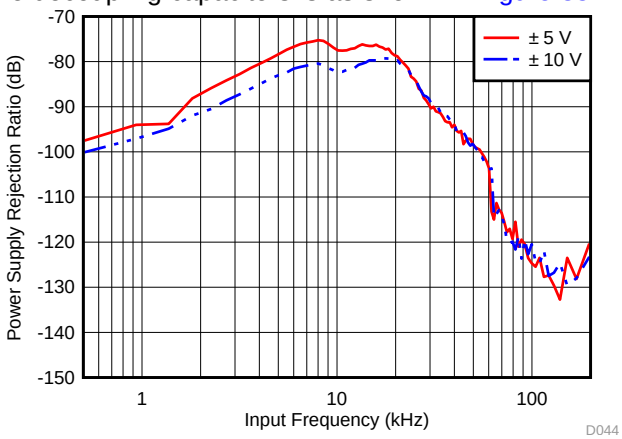

Figure 88. PSRR Across Frequency (With Decoupling Capacitor)

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11 Layout

11.1 Layout Guidelines

Figure 89 and Figure 90 illustrate a PCB layout example for the ADS8586S.

- Partition the PCB into analog and digital sections. Care must be taken to ensure that the analog signals are kept away from the digital lines. This layout helps keep the analog input and reference input signals away from the digital noise. In this layout example, the analog input and reference signals are routed on the left side of the board and the digital connections are routed on the right side of the board.
- Using a single common ground plane is strongly recommended. For designs requiring a split analog and digital ground planes, the analog and digital ground planes must be at the same potential joined together in close proximity to the device.
- Power sources to the ADS8586S must be clean and well-bypassed. As a result of dynamic currents during conversion, each AVDD must have a decoupling capacitor to keep the supply voltage stable. Use wide traces or a dedicated analog supply plane to minimize trace inductance and reduce glitches. Using a 1-μF, X7R-grade, 0603-size ceramic capacitor is recommended in close proximity to each analog (AVDD) supply pins. Bypass capacitors for AVDD pins 1 and 48 are located on the top layer; see Figure 89. AVDD supply pins 37 and 38 are connected to bypass capacitors in the bottom layer using an isolated via (1); see Figure 90. A separate via (2) is used to connect the bypass capacitor to the AVDD plane.
- For decoupling the digital (DVDD) supply pin, a 1-μF, X7R-grade, 0603-size ceramic capacitor is recommended. The DVDD bypass capacitor is located in the bottom layer; see Figure 90.
- REFCAPA and REFCAPB must be shorted together and decoupled to REFGND using a 10-μF, X7R-grade, 0603-size ceramic capacitor placed in close proximity to the pins of the device. This capacitor is placed on the top layer and directly connected to the pins of the device. Avoid placing vias between the REFCAPA, REFCAPB pins and the decoupling capacitor.
- The REFIN/REFOUT pin also must be decoupled to REFGND with a 10-μF, X7R-grade, 0603-size ceramic capacitor if the internal reference of the device is used. The capacitor must be placed on the top layer in close to the device pin. Avoid placing vias between the REFIN/REFOUT pin and the decoupling capacitor.
- The REGCAP1 and REGCAP2 pins must be decoupled to GND using a separate 1-μF, X7R-grade, 0603-size ceramic capacitor on each pin.
- All ground pins (AGND) must be connected to the ground plane using short, low-impedance paths and independent vias to the ground plane. Connect REFGND to the common GND plane.
- For the optional channel input low-pass filters, ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

Figure 89 and Figure 90 illustrate a recommended layout for the ADS8586S along with proper decoupling and reference capacitor placement and connections.

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Layout Example (continued)

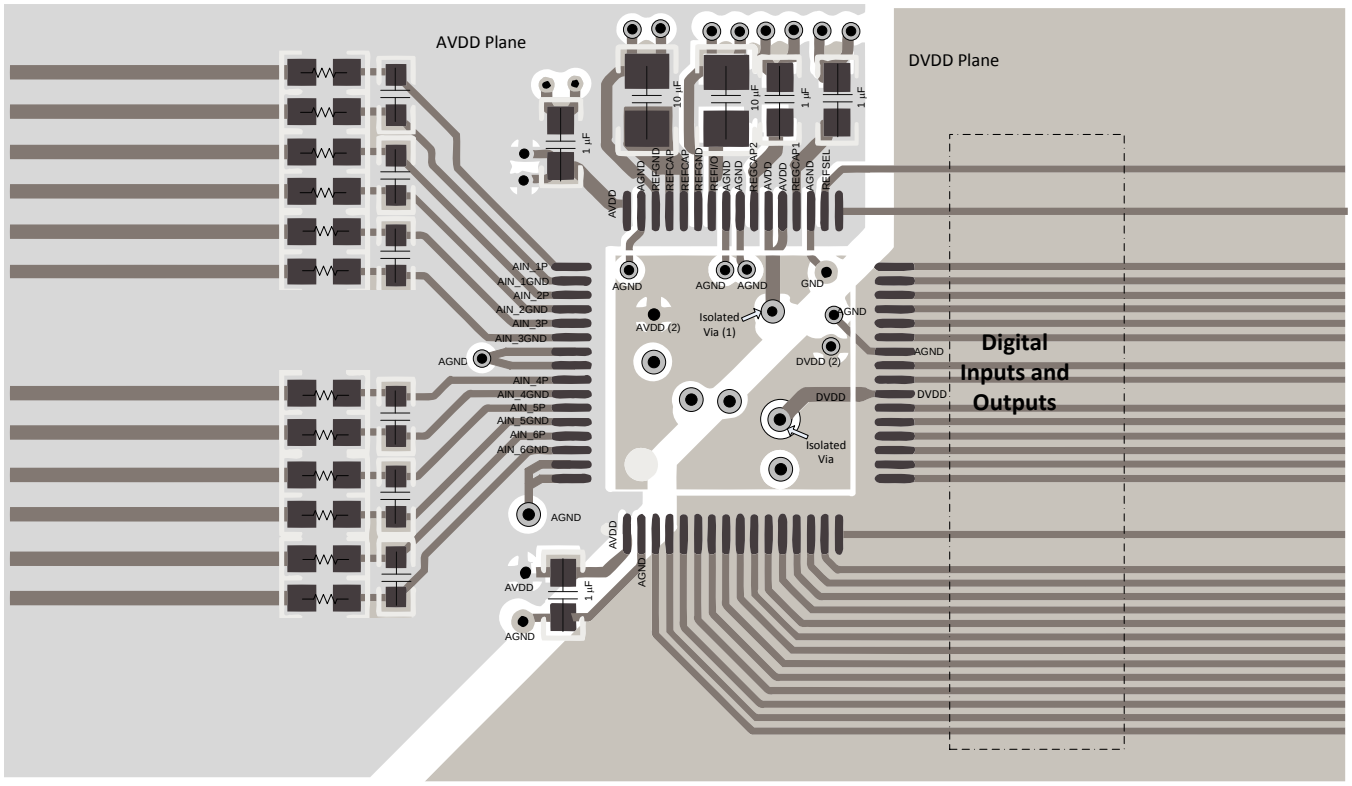

Figure 89. Top Layer Layout

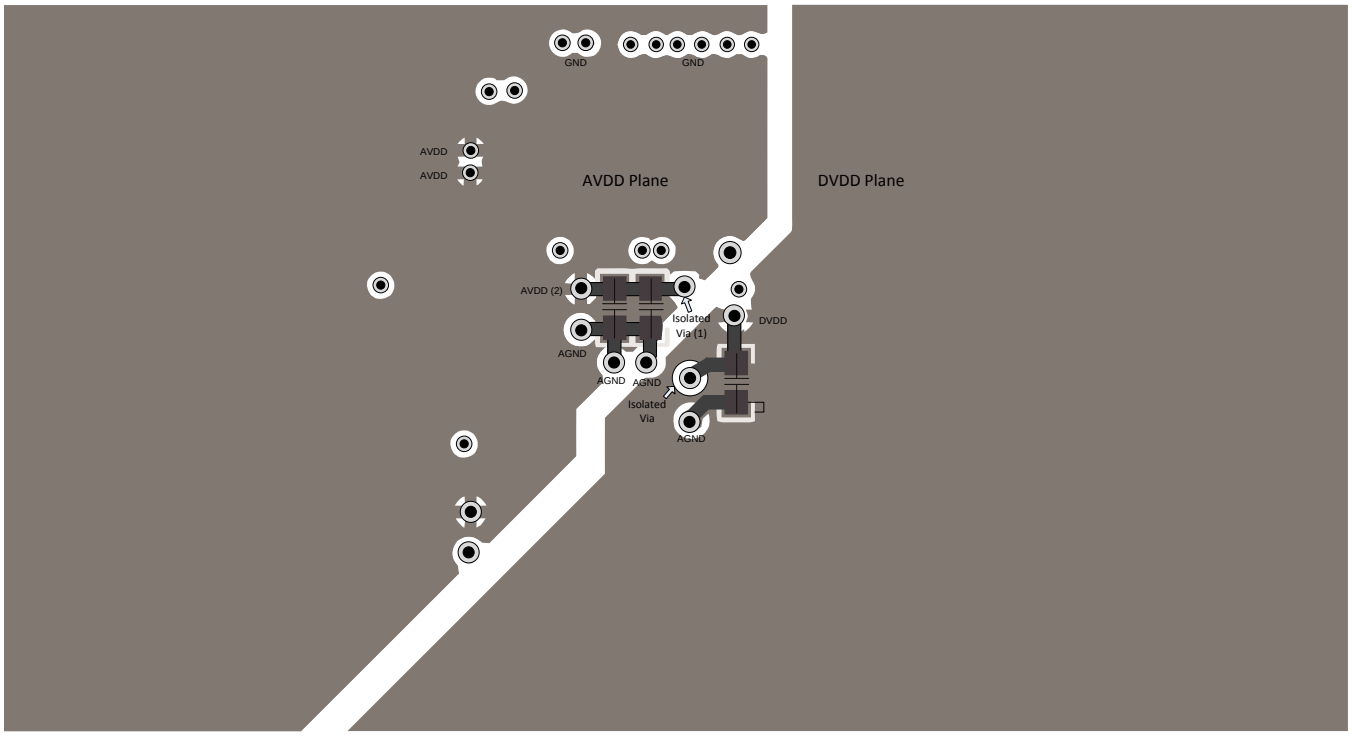

Figure 90. Bottom Layer Layout

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください：

- 『OPAx320 高精度、20MHz、0.9pA、低ノイズ、RRIO、シャットダウン搭載のCMOSオペアンプ』
- 『AN-2029 取り扱いおよびプロセスの推奨事項』アプリケーション・レポート
- 『REF50xx 低ノイズ、超低ドリフト係数、高精度基準電圧』

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12.3 コミュニティ・リソース

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8586SIPM	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8586S
ADS8586SIPM.A	Active	Production	LQFP (PM) | 64	160 | JEDEC TRAY (5+1)	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8586S
ADS8586SIPMR	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8586S
ADS8586SIPMR.A	Active	Production	LQFP (PM) | 64	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS8586S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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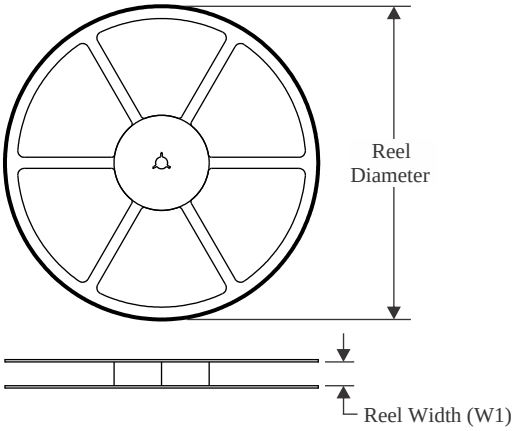
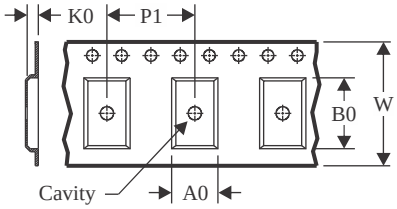
TAPE AND REEL INFORMATION

REEL DIMENSIONS

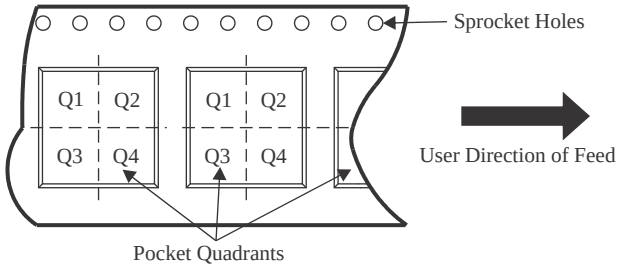


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

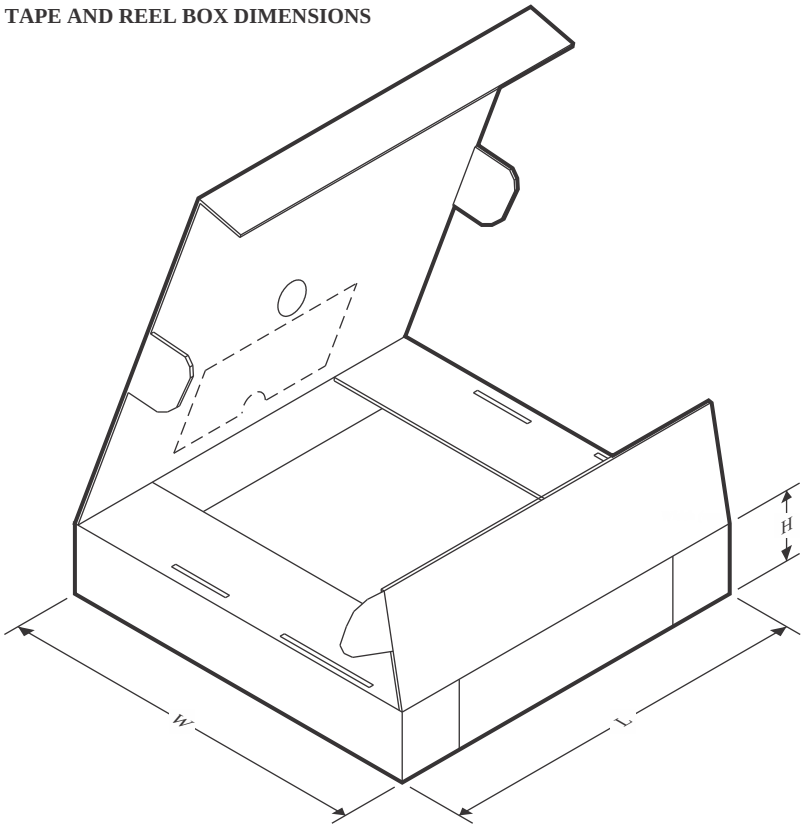
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8586SIPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

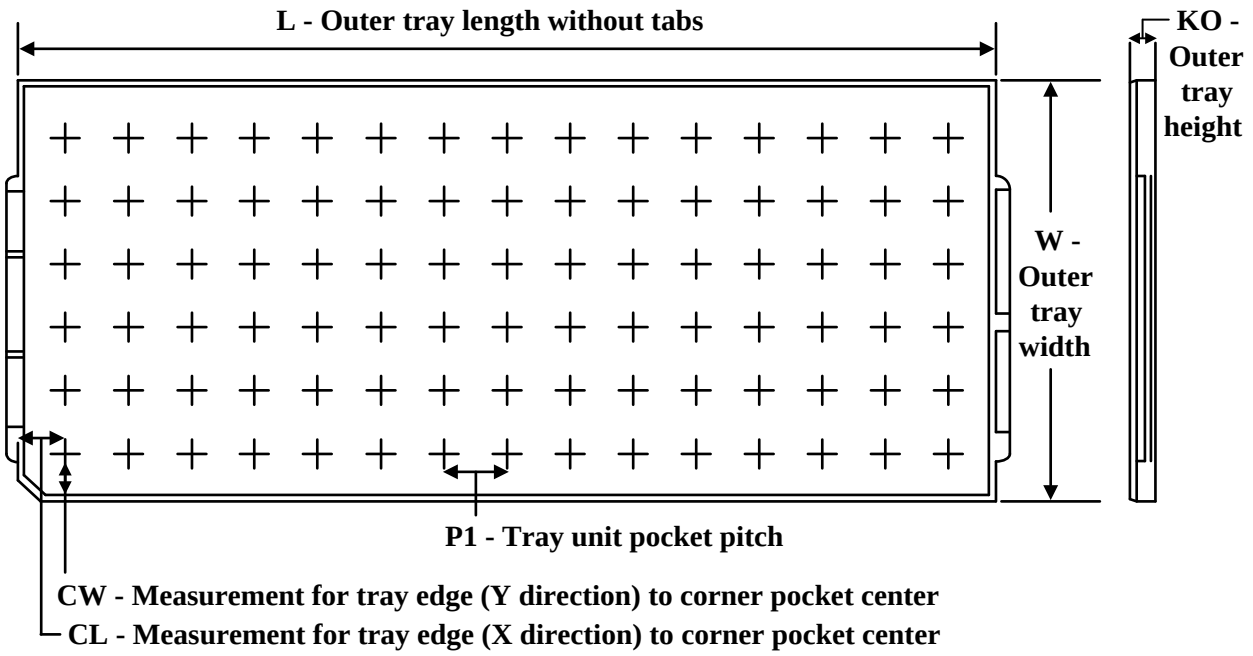
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8586SIPMR	LQFP	PM	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

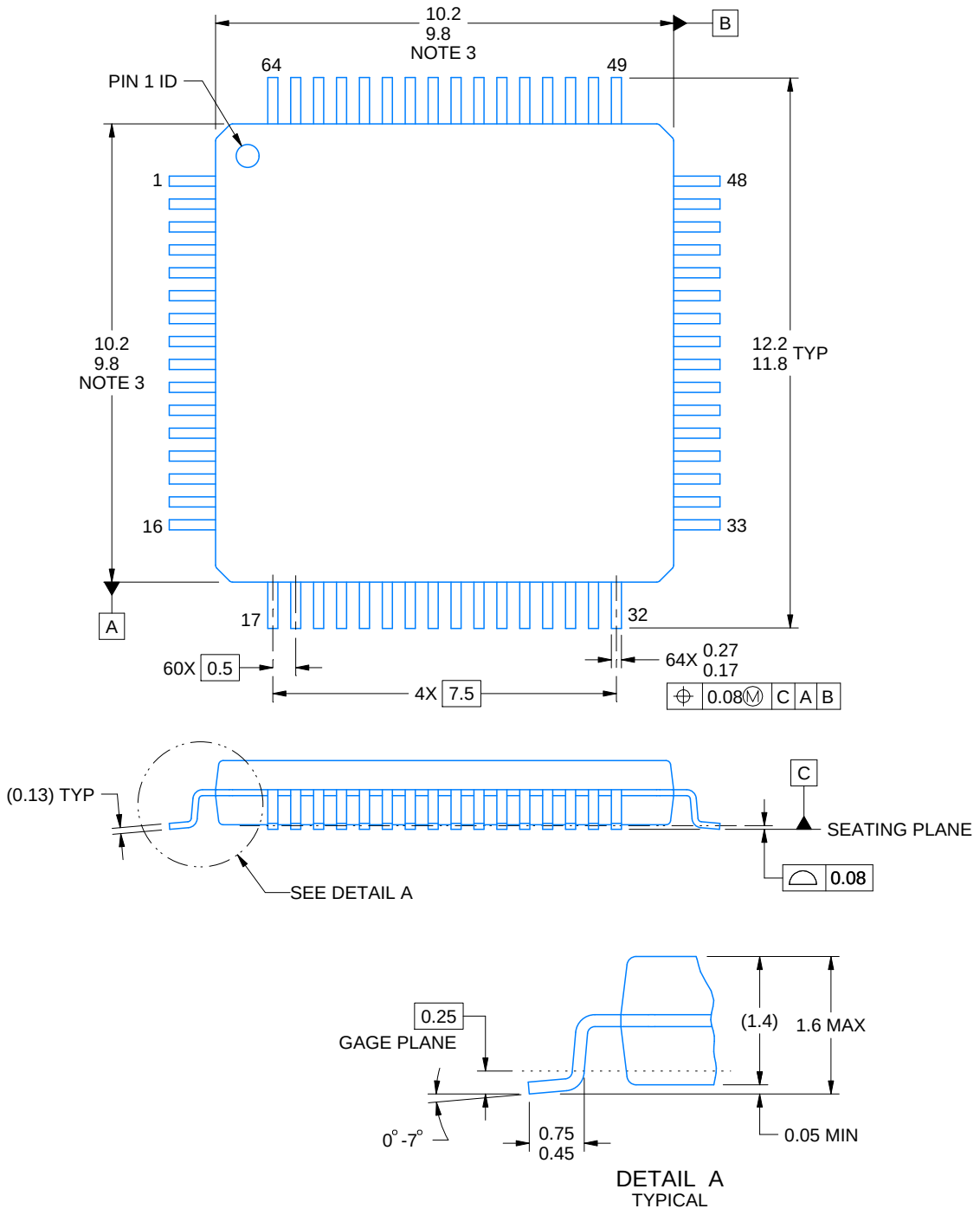
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADS8586SIPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
ADS8586SIPM.A	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

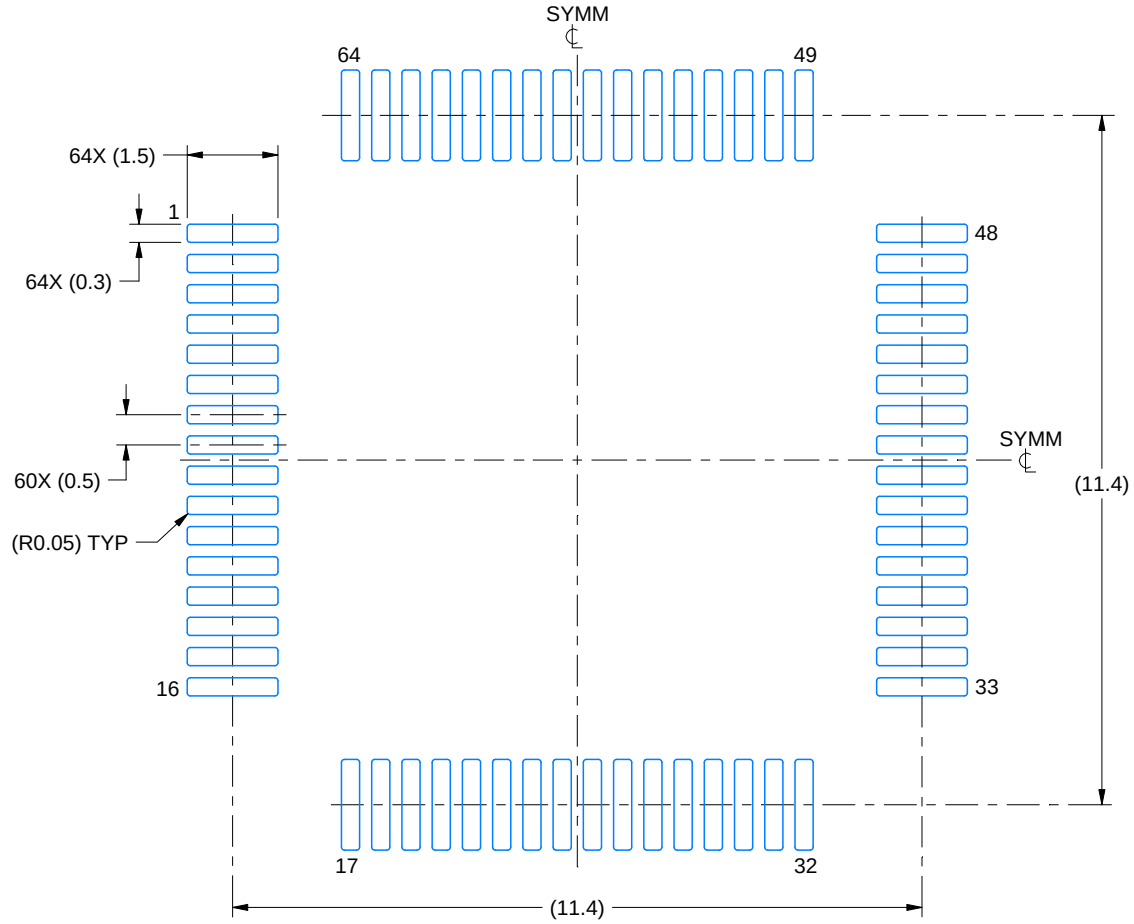
PLASTIC QUAD FLATPACK



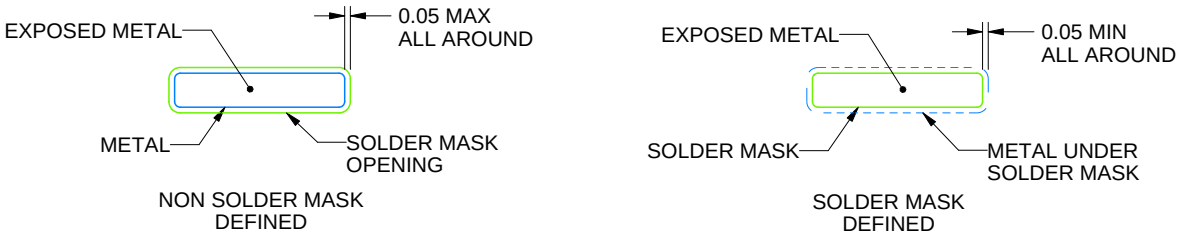
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

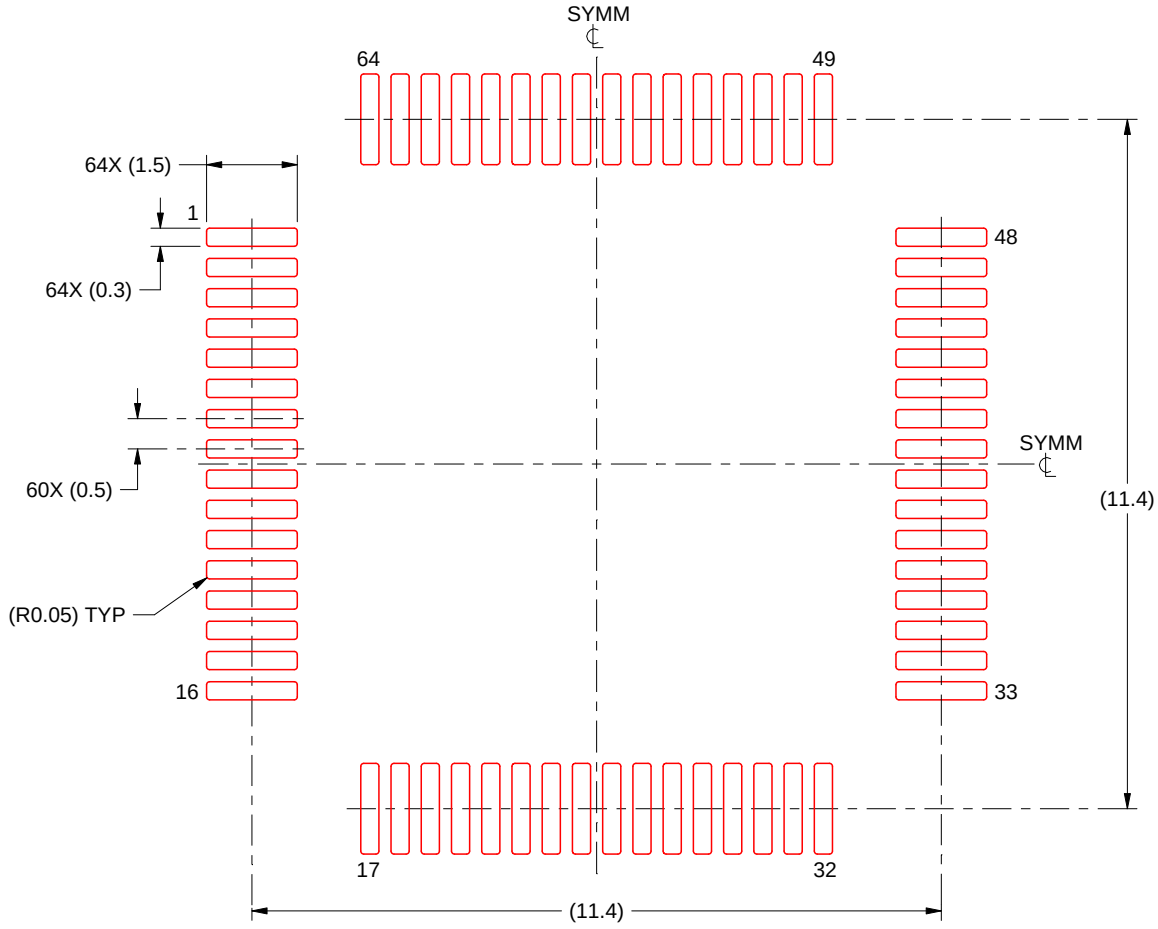


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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