AFE11612-SEP マルチチャネルの ADC、DAC、および温度センサ搭載 放射線耐性のあるアナログ・モニタおよびコントローラ

1 特長

- 放射線耐性:
  - LET = 43MeV-cm^2/mg (125℃) まで、SEL (Single-event latch-up) 耐性
  - LET = 43MeV-cm^2/mg まで、SEFI (Single-Event Functional Interrupt) 特性を評価済み
  - 20krad (Si) まで、総吸収線量 (TID) RLAT/RHA 特性を評価済み
- 宇宙用強化プラスチック (宇宙用 EP):
  - ASTM E595 アウトガス仕様に適合
  - VID (Vendor Item Drawing) V62/22614
  - 軍用温度範囲:-55℃～+125℃
  - 単一の製造、アセンブリ、テスト施設
  - 金ボンド・ワイヤ、NiPdAu リード仕上げ
  - ウェハ・ロットをトレース可能
  - 長い製品ライフ・サイクル
- 12 個の単調性 12 ビット DAC
  - 出力電圧範囲:0V～5V
  - ユーザー定義の DAC シャットダウン・レベル
- 16 入力、12 ビット逐次比較型 (SAR) ADC
  - 高いサンプル・レート:500kSPS
  - 16 個のシングルエンド入力、または 2 個の差動入力と 12 個のシングルエンド入力
  - 範囲外アラームをプログラム可能
- 8 ピン GPIO
- 内部 2.5V リファレンス
- 2 つのリモート温度センサ
- 内部温度センサ
- 設定可能な SPI および I^{2}C インターフェイス
  - 2.7V～5.5V で動作

2 アプリケーション

- コマンドとデータの処理 (C&DH)
- 通信ペイロード
- レーダー画像処理ペイロード
- 光学画像処理ペイロード
- 一般的なアナログ・モニタリングおよび制御

3 概要

AFE11612-SEP は、高密度の汎用モニタおよび制御システム用に設計された、高集積のアナログ・モニタおよび制御デバイスです。このデバイスには、12 ビットの D/A コンバータ (DAC) が 12 個と、16 チャネル、12 ビットの A/D コンバータ (ADC) が搭載されています。さらに、8 つの汎用入出力 (GPIO)、2 つのリモート温度センサ・チャネル、およびローカル温度センサ・チャネルも内蔵されています。

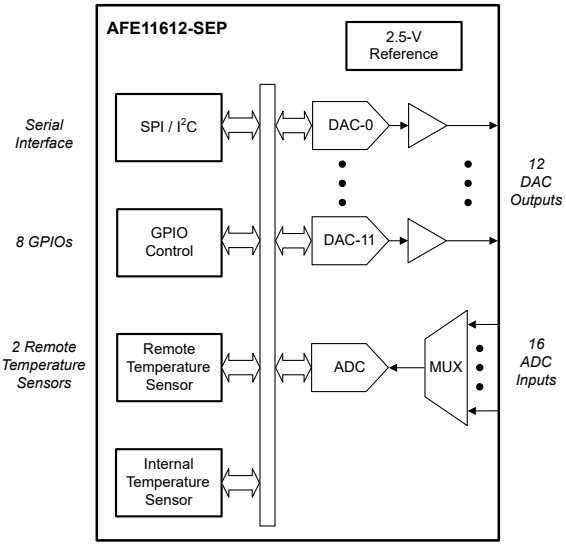
このデバイスには、DAC の出力電圧を 0V～5V の範囲に規定する 2.5V の内蔵基準電圧があり、また、外部基準電圧を使用した動作もサポートしています。このデバイスに対しては、SPI 互換と I^{2}C 互換、2 種類のインターフェイス経由での通信が可能です。

本デバイスの高集積は、部品点数の大幅な低減や、閉ループ・システム設計の簡素化に貢献します。これにより、放射線耐性やボード面積を重視する高密度アプリケーションにとって、優れた選択肢になっています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (2)
AFE11612-SEP	PAP (HTQFP、64)	10.0mm × 10.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) 本体サイズ (長さ × 幅) は公称値であり、ピンは含まれていません。



概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2022) to Revision A (September 2023)	Page
• 長期にわたる製品変更通知に関する「特長」の箇条書き項目を削除	1
• Changed external reference input voltage minimum value from 2.4 V to 1.4 V in *Electrical Characteristics*	7
• Changed plots to move test conditions from figures to text and improve color contrast in figures containing multiple plots in all *Typical Characteristics* sections	16
• Changed *Overview* section to provide required information	25
• Added *DAC Output Mode* subsection	45
• Added *ADC Conversion Modes* subsection to *Device Functional Modes*; moved from *Feature Description*	45
• Changed Table 7-10, *Register Maps*,to provide more information	59
• Changed all register subsections to show register name to match global register map	59
• Changed all register subsection Field Descriptions tables to remove unnecessary content	59
• Added Field Description tables to subsections that were missing this table	59
• Changed some registers to be grouped together	59
• Changed R0, R1, R2 to RATE in *Temperature Conversion Rate* register	65
• Changed Table 7-12, *Temperature Conversion Time* to Table 7-15, *Temperature Conversion Rate Field Descriptions*	65
• Changed Table 7-14, *NADJUST and ηEFF Values* to Table 7-17, *η-Factor Correction Register Field Descriptions*	66
• Changed *ADC Channel Register 1* section text for accuracy	74
• Added *Application and Implementation* section and *Application Information* and *Typical Application* subsections	85
• Added *Layout* section and *Layout Guidelines* and *Layout Example* subsections	90

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5 Pin Configuration and Functions

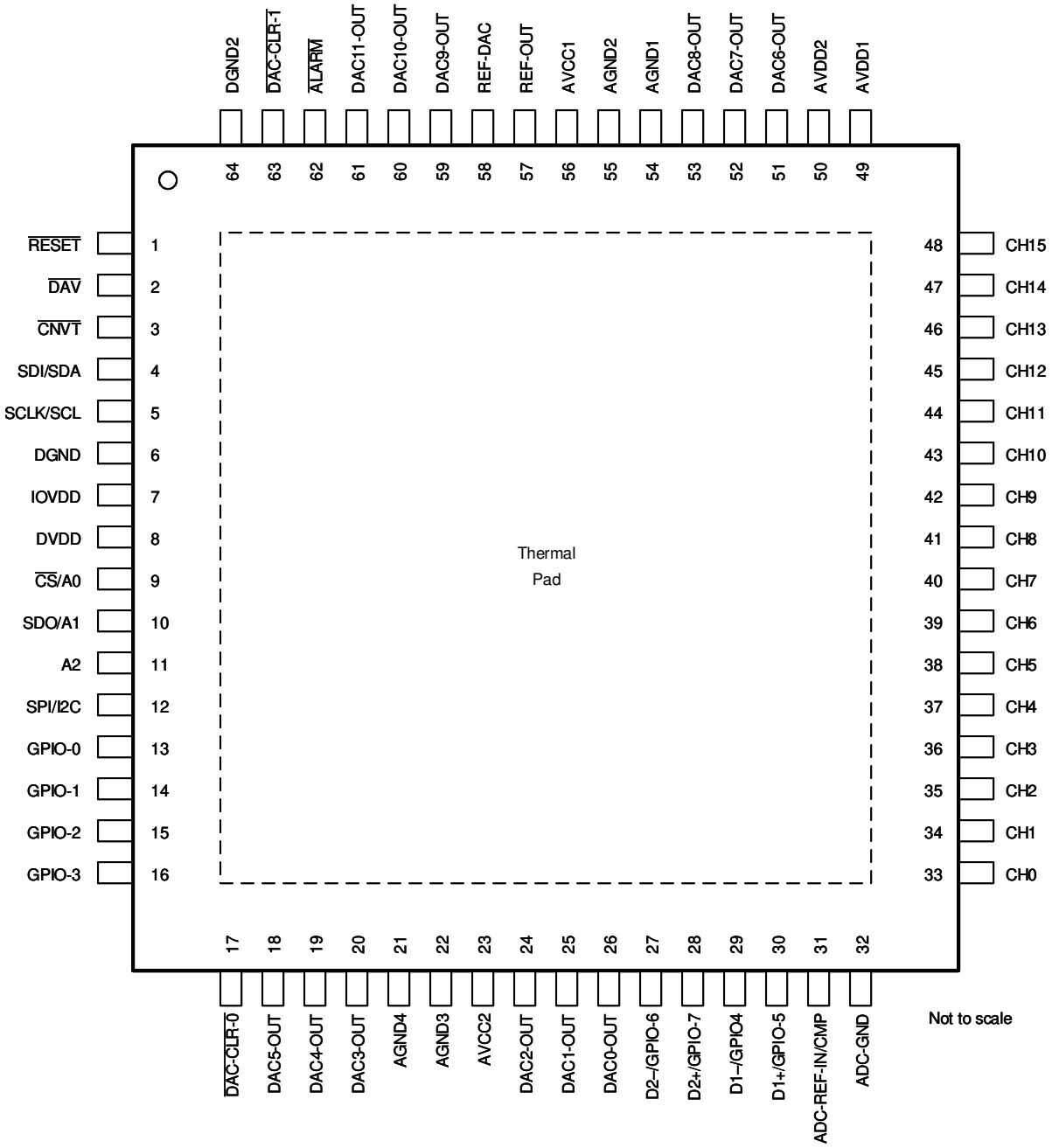


図 5-1. PAP Package, 64-Pin HTQFP (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A2	11	I	Target address selection A2 for I^2C when the SPI/I2C pin is low.
ADC-GND	32	I	ADC ground. Must be connected to AGND.
ADC-REF-IN/CMP	31	I/O	External ADC reference input when external V_{REF} is used to drive the ADC. A compensation capacitor connection (connect a 4.7-µF capacitor between this pin and AGND) when internal V_{REF} is used to drive the ADC.
AGND1	54	I	Analog ground
AGND2	55	I	Analog ground
AGND3	22	I	Analog ground
AGND4	21	I	Analog ground
$\overline{ALARM}$	62	O	Global alarm. Open-drain output. An external 10-kΩ pullup resistor is required. This pin goes low (active) when one (or more) analog channels are out of range.
AVCC1	56	I	Positive analog power for DAC6-OUT, DAC7-OUT, DAC8-OUT, DAC9-OUT, DAC10-OUT, and DAC11-OUT; must be tied to AVCC2
AVCC2	23	I	Positive analog power for DAC0-OUT, DAC1-OUT, DAC2-OUT, DAC3-OUT, DAC4-OUT, and DAC5-OUT; must be tied to AVCC1
AVDD1	49	I	Positive analog power supply
AVDD2	50	I	Positive analog power supply
CH0	33	I	Analog input of channel 0. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended.
CH1	34	I	Analog input of channel 1. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended.
CH2	35	I	Analog input of channel 2. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended.
CH3	36	I	Analog input of channel 3. CH0, CH1, CH2, and CH3 can be programmed as differential or single-ended.
CH4	37	I	Analog input of channel 4. CH4 to CH15 are single-ended.
CH5	38	I	Analog input of channel 5. CH4 to CH15 are single-ended.
CH6	39	I	Analog input of channel 6. CH4 to CH15 are single-ended.
CH7	40	I	Analog input of channel 7. CH4 to CH15 are single-ended.
CH8	41	I	Analog input of channel 8. CH4 to CH15 are single-ended.
CH9	42	I	Analog input of channel 9. CH4 to CH15 are single-ended.
CH10	43	I	Analog input of channel 10. CH4 to CH15 are single-ended.
CH11	44	I	Analog input of channel 11. CH4 to CH15 are single-ended.
CH12	45	I	Analog input of channel 12. CH4 to CH15 are single-ended.
CH13	46	I	Analog input of channel 13. CH4 to CH15 are single-ended.
CH14	47	I	Analog input of channel 14. CH4 to CH15 are single-ended.
CH15	48	I	Analog input of channel 15. CH4 to CH15 are single-ended.
$\overline{CNVT}$	3	I	External conversion trigger, active low. The falling edge initiates the sampling and conversion of the ADC.
$\overline{CS}$/A0	9	I	Chip-select signal for SPI when the SPI/I2C pin high. Target address selection A0 for I^2C when SPI/I2C low.
D1–/GPIO4	29	I/O	Remote sensor D1 negative input when D1 enabled; GPIO-6 when D1 disabled. Pullup resistor required for output.
D1+/GPIO-5	30	I/O	Remote sensor D1 positive input when D1 enabled; GPIO-7 when D1 disabled. Pullup resistor required for output.
D2–/GPIO-6	27	I/O	Remote sensor D2 negative input when D2 enabled; GPIO-6 when D2 disabled. Pullup resistor required for output.
D2+/GPIO-7	28	I/O	Remote sensor D2 positive input when D2 enabled; GPIO-7 when D2 disabled. Pullup resistor required for output.
DAC0-OUT	26	O	DAC channel 0 output
DAC1-OUT	25	O	DAC channel 1 output
DAC2-OUT	24	O	DAC channel 2 output
DAC3-OUT	20	O	DAC channel 3 output
DAC4-OUT	19	O	DAC channel 4 output
DAC5-OUT	18	O	DAC channel 5 output
DAC6-OUT	51	O	DAC channel 6 output
DAC7-OUT	52	O	DAC channel 7 output
DAC8-OUT	53	O	DAC channel 8 output
DAC9-OUT	59	O	DAC channel 9 output
DAC10-OUT	60	O	DAC channel 10 output

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表 5-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
DAC11-OUT	61	O	DAC channel 11 output
$\overline{\text{DAC-CLR-0}}$	17	I	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-0 pin enter a CLEAR state, the DAC latch is loaded with a predefined code, and the output is set to the corresponding level. However, the DAC-data register does not change. When the DAC goes back to normal operation, the DAC latch is loaded with the previous data from the DAC-data register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation.
$\overline{\text{DAC-CLR-1}}$	63	I	DAC clear control signal, digital input, active low. When low, all DACs associated with the DAC-CLR-1 pin enter a CLEAR state, the DAC latch is loaded with a predefined code, and the output is set to the corresponding level. However, the DAC-data register does not change. When the DAC goes back to normal operation, the DAC latch is loaded with the previous data from the DAC-data register and the output returns to the previous level, regardless of the status of the SLDAC-n bit. When this pin is high, the DACs are in normal operation.
$\overline{\text{DAV}}$	2	O	Data available indicator, active low output. In direct mode, the $\overline{\text{DAV}}$ pin goes low (active) when the conversion ends. In auto mode, a 1-µs pulse (active low) appears on this pin when a conversion cycle completes (for details, see the *Primary ADC Operation* and *Register Maps* sections). $\overline{\text{DAV}}$ stays high when deactivated.
DGND	6	I	Digital ground
DGND2	64	I	Digital ground
DVDD	8	I	Digital power supply (3 V to 5 V). Must be the same value as AV_{DD}.
GPIO-0	13	I/O	General-purpose digital input and output. This bidirectional, open-drain, digital I/O pin requires an external pullup resistor. For more details, see the *General-Purpose Input and Output Pins (GPIO-0 To GPIO-7)* section.
GPIO-1	14	I/O	General-purpose digital input and output. This bidirectional, open-drain, digital I/O pin requires an external pullup resistor. For more details, see the *General-Purpose Input and Output Pins (GPIO-0 To GPIO-7)* section.
GPIO-2	15	I/O	General-purpose digital input and output. This bidirectional, open-drain, digital I/O pin requires an external pullup resistor. For more details, see the *General-Purpose Input and Output Pins (GPIO-0 To GPIO-7)* section.
GPIO-3	16	I/O	General-purpose digital input and output. This bidirectional, open-drain, digital I/O pin requires an external pullup resistor. For more details, see the *General-Purpose Input and Output Pins (GPIO-0 To GPIO-7)* section.
IOVDD	7	I	Interface power supply
REF-DAC	58	I	DAC reference input
REF-OUT	57	O	Internal reference output
$\overline{\text{RESET}}$	1	I	Reset input, active low. A logic low on this pin causes the device to perform a hardware reset.
SCLK/SCL	5	I	Serial clock input of the main serial interface. This pin functions as the SPI clock when the SPI/I2C pin is high. This pin functions as the I^2C clock when the SPI/I2C pin is low.
SDI/SDA	4	I/O	Serial interface data. This pin functions as SDI for the serial peripheral interface (SPI) when the SPI/I2C pin (pin 12) is high. This pin functions as SDA for the I^2C interface when the SPI/I2C pin is low.
SDO/A1	10	I/O	SDO for SPI when the SPI/I2C pin is high. Target address selection A1 for I^2C when the SPI/I2C pin is low.
SPI/I2C	12	I	Interface selection pin; digital input. When this pin is tied to IOVDD, the SPI is enabled and the I^2C interface is disabled. When this pin is tied to ground, the SPI is disabled and the I^2C interface is enabled.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage	AVDD pins to GND	–0.3	6	V
		DVDD pins to GND	–0.3	6	
		IOVDD pins to GND	–0.3	6	
		AVCC pins to GND	–0.3	6	
	Pin voltage	Analog input pins to GND	–0.3	AV_{DD} + 0.3	V
		Digital input pins to GND	–0.3	IOV_{DD} + 0.3	
		ALARM, GPIO-[0:3], SCLK/SCL, SDI/SDA pins to GND	–0.3	6	
		D1+/GPIO-4, D1–/GPIO-5, D2+/GPIO-6, D2–/GPIO-7 pins to GND	–0.3	AV_{DD} + 0.3	
		SDO and DAV pins to GND	–0.3	IOV_{DD} + 0.3	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AV_{DD} (1)	Analog supply voltage	2.7		5.5	V
DV_{DD}	Digital supply voltage	2.7		5.5	V
IOV_{DD}	Digital IO supply voltage	2.7		5.5	V
AV_{CC}	Output buffer supply voltage	4.5		5.5	V
T_A	Operating ambient temperature	–55		125	°C

(1) AV_{DD} must be greater than or equal to (V_{REF} + 1.2 V).

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6.4 Thermal Information

THERMAL METRIC[1]		AFE11612-SEP PAP (HTQFP) 64 PINS	UNIT
Θ_{JA}	Junction-to-ambient thermal resistance	33.7	°C/W
$\Theta_{JC(top)}$	Junction-to-case (top) thermal resistance	9.5	°C/W
Θ_{JB}	Junction-to-board thermal resistance	9.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.9	°C/W
$\Theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

all minimum and maximum specifications at T_A = –55°C to +125°C, all typical specifications at T_A = 25°C, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC CHARACTERISTICS[1]						
	Resolution		12			Bits
	Full-scale output voltage	V_{REF} = 2.5 V	0		5	V
DNL	Differential nonlinearity	Specified 12-bit monotonic	–1		1	LSB
INL	Integral nonlinearity		–1.25		1.25	LSB
TUE	Total unadjusted error	T_A = 25°C	–10		10	mV
	Offset error	T_A = 25°C	–2		2	mV
	Offset error temperature drift			±1		ppm/°C
	Gain error	External 2.5-V reference	–0.15		0.15	%FSR
	Gain error temperature drift			±2		ppm/°C
	Load current[2]	Source within 200 mV of supply		10		mA
		Sink within 300 mV of supply		–10		mA
	Short-circuit current[2]			±30		mA
	Capacitive load stability[3]		0		10	nF
	DC output impedance[3]	Midscale code		0.3		Ω
	Output voltage settling time	R_L = 2 kΩ, C_L = 200 pF, 1/4 to 3/4 scale settling to 1/2 LSB		3		µs
	Slew rate	1/4 to 3/4 scale transition, 10% to 90%		1.5		V/µs
	Output noise	f = 0.1 Hz to 10 Hz, midscale code		8		µVpp
	Output noise density	f = 1 kHz, midscale code, external reference		81		nV/√Hz
	Code change glitch impulse	1 LSB change around major carrier		0.15		nV-s
	Supply ramp-up glitch amplitude	AV_{CC} = 0-V to 5-V, 2-ms ramp		5		mV
	Digital feedthrough	Device is not accessed		0.15		nV-s

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6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CHARACTERISTICS						
	Resolution			12		Bits
	Full-scale input voltage	Single-ended, 0 V to V_{REF}	0		V_{REF}	V
		Single-ended, 0 V to 2 × V_{REF}	0		2 × V_{REF}	
		Fully differential, V_{IN+} – $V_{IN–}$, 0 V to V_{REF}	–V_{REF}		V_{REF}	
		Fully differential, V_{IN+} – $V_{IN–}$, 0 V to 2 × V_{REF}	–2 × V_{REF}		2 × V_{REF}	
	Absolute input voltage		GND – 0.2		AV_{DD} + 0.2	V
DNL	Differential nonlinearity	Specified 12-bit monotonic	–1		1	LSB
INL	Integral nonlinearity		–1		1	LSB
	Offset error		–3		3	LSB
	Offset error match			±0.4		LSB
	Gain error	Single-ended mode, external 2.5-V reference	–5		5	LSB
		Differential mode, 0 V to V_{REF}, V_{CM} = 1.25 V, external 2.5-V reference	–5		5	
		Differential mode, 0 V to 2 × V_{REF}, V_{CM} = 2.5 V, external 2.5-V reference	–5		5	
	Gain error match	Single-ended mode		±0.4		LSB
		Differential mode		±0.5		
	Zero code error	Differential mode, 0 V to V_{REF}, V_{CM} = 1.25 V, external 2.5-V reference	–3		3	LSB
		Differential mode, 0 V to 2 × V_{REF}, V_{CM} = 2.5 V, external 2.5-V reference	–3		3	
	Zero code error match			±0.5		LSB
	Common-mode rejection	Differential mode, 0 V to 2 × V_{REF}, measured at dc		67		dB
	Input capacitance	0 V to V_{REF}		118		pF
		0 V to 2 × V_{REF}		73		
	Input bias current	Unselected ADC input		±10		μA
	Conversion rate	External single analog channel, auto-mode conversion		500		kSPS
		External single analog channel, direct-mode conversion		167		
	Conversion time	External single analog channel		2		μs
	Autocycle update rate	All 16 single-ended inputs enabled		32		μs
	Throughput rate	SCLK ≥ 12 MHz, external single-channel			500	kSPS
INTERNAL TEMPERATURE SENSOR CHARACTERISTICS						
	Accuracy	AV_{DD} = 5 V, T_A = –55°C to +125°C	–4.5		4.5	°C
		AV_{DD} = 5 V, T_A = 0°C to 100°C	–1.5		1.5	
	Resolution			0.125		°C
	Conversion rate	Remote temperature sensors disabled		15		ms

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6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REMOTE TEMPERATURE SENSOR CHARACTERISTICS						
	Accuracy(4)	AV_{DD} = 5 V, T_A = –55°C to +125°C, T_D = –40°C to +150°C	–6		6	°C
		AV_{DD} = 5 V, T_A = 0°C to +100°C, T_D = –40°C to +150°C	–1.5		1.5	
	Resolution			0.125		°C
	Conversion rate per sensor	With resistance cancellation (RC = 1)		93		ms
		Without resistance cancellation (RC = 0)		44		
INTERNAL REFERENCE CHARACTERISTICS						
$V_{REF-OUT}$	Internal reference voltage	T_A = 25°C, REF-OUT pin	2.48	2.5	2.52	V
	Internal reference temperature coefficient	T_A = –55°C to +125°C		25		ppm/°C
	Internal reference impedance			0.4		Ω
	Internal reference output noise	f = 0.1 Hz to 10 Hz		13		μV_{PP}
	Internal reference noise density	f = 1 kHz		260		nV/√Hz
	Internal reference load current			±5		mA
EXTERNAL REFERENCE CHARACTERISTICS						
V_{REF}	Input voltage	DAC reference input, REF-DAC pin	1.4	2.5	2.6	V
		ADC reference input, ADC-REF-IN pin	1.4	2.5	2.6	
	Input current	DAC reference input, V_{REF} = 2.5 V		170		µA
		ADC reference input, V_{REF} = 2.5 V		145		
	ADC reference buffer offset	T_A = 25°C	–5		5	mV
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	High-level input voltage	IOV_{DD} = 5 V	2.1			V
		IOV_{DD} = 3.3 V	2.2			
V_{IL}	Low-level input voltage	IOV_{DD} = 5 V			0.8	V
		IOV_{DD} = 3.3 V			0.7	
	Input current	All except SCL, SDA, $\overline{ALARM}$ and GPIO	–1		1	µA
		SCL, SDA, $\overline{ALARM}$ and GPIO	–5		5	
	Input pin capacitance			5		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	High-level output voltage	IOV_{DD} = 5 V, I_{SOURCE} = 3 mA	4.8			V
		IOV_{DD} = 3.3 V, I_{SOURCE} = 3 mA	2.9			
V_{OL}	Low-level output voltage	I_{SINK} = 3 mA			0.4	V
V_{OL}	Open-drain low-level output voltage	GPIO and $\overline{ALARM}$, IOV_{DD} = 5 V, I_{SINK} = 5 mA			0.4	V
		GPIO and $\overline{ALARM}$, IOV_{DD} = 3.3 V, I_{SINK} = 2 mA			0.4	
		SDA and SCL, IOV_{DD} = 5 V, I_{SINK} = 3 mA			0.4	
		SDA and SCL, IOV_{DD} = 3.3 V, I_{SINK} = 3 mA			0.4	
	High-impedance leakage		–5		5	µA
	Output pin capacitance			10		pF

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6.5 Electrical Characteristics (続き)

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION CHARACTERISTICS						
I_{VDD}	AV_{DD} and DV_{DD} supply current	AV_{DD} and DV_{DD} combined, no DAC load, DACs at midscale code and ADC at the fastest autoconversion rate		8	19	mA
		AV_{DD} and DV_{DD} combined, power-down mode		1.6		
I_{AVCC}	AV_{CC} supply current	No DAC load, DACs at midscale code and ADC at the fastest autoconversion rate			7	mA
	Power consumption	No DAC load, DACs at midscale code and ADC at the fastest autoconversion rate, AV_{DD} = DV_{DD} = 5 V, AV_{CC} = 5 V		95	120	mW

(1) End point fit between codes 32 to 4095.
(2) Overload condition protection. Junction temperature can be exceeded during current limit. Operation greater than the specified maximum junction temperature can impair device reliability.
(3) Specified by design and characterization. Not tested during production.
(4) T_D is the external diode temperature.

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6.6 Timing Characteristics

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C STANDARD MODE TIMING REQUIREMENTS					
$f_{(SCL)}$ (1)	I²C clock frequency	0		100	kHz
$t_{(LOW)}$	SCL clock low period	4.7			µs
$t_{(HIGH)}$	SCL clock high period	4.0			µs
$t_{(SUSTA)}$	Repeated start condition setup time	4.7			µs
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated	4.0			µs
$t_{(SUSTO)}$	Stop condition setup time	4.0			µs
$t_{(BUF)}$	Bus free time between stop and start condition	4.7			µs
$t_{(SUDAT)}$	Data setup time	250			ns
$t_{(HDDAT)}$	Data hold time	0		3.45	µs
$t_{R,SCL}$	Clock rise time			1000	ns
$t_{F,SCL}$	Clock fall time			300	ns
$t_{R,SDA}$	Data rise time			1000	ns
$t_{F,SDA}$	Data fall time			300	ns
C_B	Capacitive load for each bus line			400	pF
I²C FAST MODE TIMING REQUIREMENTS					
$f_{(SCL)}$ (1)	I²C clock frequency	0		400	kHz
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(HDDAT)}$	Data hold time	0		0.9	µs
$t_{R,SCL}$	Clock rise time	20 + 0.1 C_B		300	ns
$t_{F,SCL}$	Clock fall time	20 + 0.1 C_B		300	ns
$t_{R,SDA}$	Data rise time	20 + 0.1 C_B		300	ns
$t_{F,SDA}$	Data fall time	20 + 0.1 C_B		300	ns
C_B	Capacitive load for each bus line			400	pF
$t_{(SP)}$	Pulse duration of spike suppressed	0		50	ns

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6.6 Timing Characteristics (続き)

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C Hs MODE TIMING REQUIREMENTS, C_B = 400 pF					
$f_{(SCL)}$ (1)	I²C clock frequency	0		1.7	MHz
$t_{(LOW)}$	SCL clock low period	320			ns
$t_{(HIGH)}$	SCL clock high period	120			ns
$t_{(SUSTA)}$	Repeated start condition setup time	160			ns
$t_{(HDSTA)}$	Hold time after repeated start condition	160			ns
$t_{(SUSTO)}$	Stop condition setup time	160			ns
$t_{(SUDAT)}$	Data setup time	10			ns
$t_{(HDDAT)}$	Data hold time	0		150	ns
$t_{R,SCL}$	Clock rise time	20		80	ns
$t_{R,SCL1}$	Clock rise time after a repeated start condition and after an acknowledge bit	20		160	ns
$t_{F,SCL}$	Clock fall time	20		80	ns
$t_{R,SDA}$	Data rise time	20		160	ns
$t_{F,SDA}$	Data fall time	20		160	ns
C_B (2)	Capacitive load for each bus line			400	pF
$t_{(SP)}$	Pulse duration of spike suppressed	0		10	ns
I²C Hs MODE TIMING REQUIREMENTS, C_B = 10 pF to 100 pF					
$f_{(SCL)}$	I²C clock frequency	0		3.4	MHz
$t_{(LOW)}$	SCL clock low period	160			ns
$t_{(HIGH)}$	SCL clock high period	60			ns
$t_{(SUSTA)}$	Repeated start condition setup time	160			ns
$t_{(HDSTA)}$	Hold time after repeated start condition	160			ns
$t_{(SUSTO)}$	Stop condition setup time	160			ns
$t_{(SUDAT)}$	Data setup time	10			ns
$t_{(HDDAT)}$	Data hold time	0		70	ns
$t_{R,SCL}$	Clock rise time	10		40	ns
$t_{R,SCL1}$	Clock rise time after a repeated start condition and after an acknowledge bit	10		80	ns
$t_{F,SCL}$	Clock fall time	10		40	ns
$t_{R,SDA}$	Data rise time	10		80	ns
$t_{F,SDA}$	Data fall time	10		80	ns
C_B (2)	Capacitive load for each bus line	10		100	pF
$t_{(SP)}$	Pulse duration of spike suppressed	0		10	ns

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6.6 Timing Characteristics (続き)

all minimum and maximum specifications at T_A = –55℃ to +125℃, all typical specifications at T_A = 25℃, AV_{CC} = 5.5 V, AV_{DD} = DV_{DD} = 4.5 V to 5.5 V, IOV_{DD} = 2.7 V to 5.5 V, internal reference, and DAC outputs unloaded (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SPI TIMING REQUIREMENTS					
$f_{(SCLK)}$	SCLK frequency			20	MHz
$t_{(SCLKHIGH)}$	SCLK high time	8			ns
$t_{(SCLKLOW)}$	SCLK low time	8			ns
$t_{(SDISU)}$	SDI setup time	5			ns
$t_{(SDIHD)}$	SDI hold time	4			ns
$t_{(SDODLY)}$ (3)	SDO output delay	3		20	ns
$t_{(CSSU)}$	$\overline{CS}$ setup time	5			ns
$t_{(CSHD)}$	$\overline{CS}$ hold time	10			ns
$t_{(CSHIGH)}$	$\overline{CS}$ high time	30			ns

(1) Use an SCL operating frequency of at least 1 kHz to avoid the I^2C timeout function.
(2) For bus line loads where CB is between 100 pF and 400 pF, linearly interpolate the timing parameters.
(3) SDO loaded with 10-pF load capacitance.

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6.7 Timing Diagrams

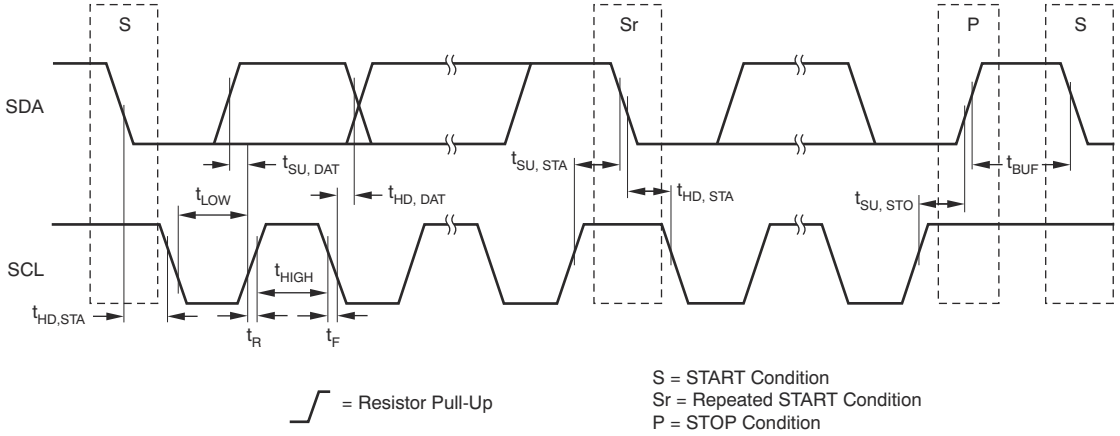


図 6-1. Timing for Standard and Fast Mode Devices on I²C Bus

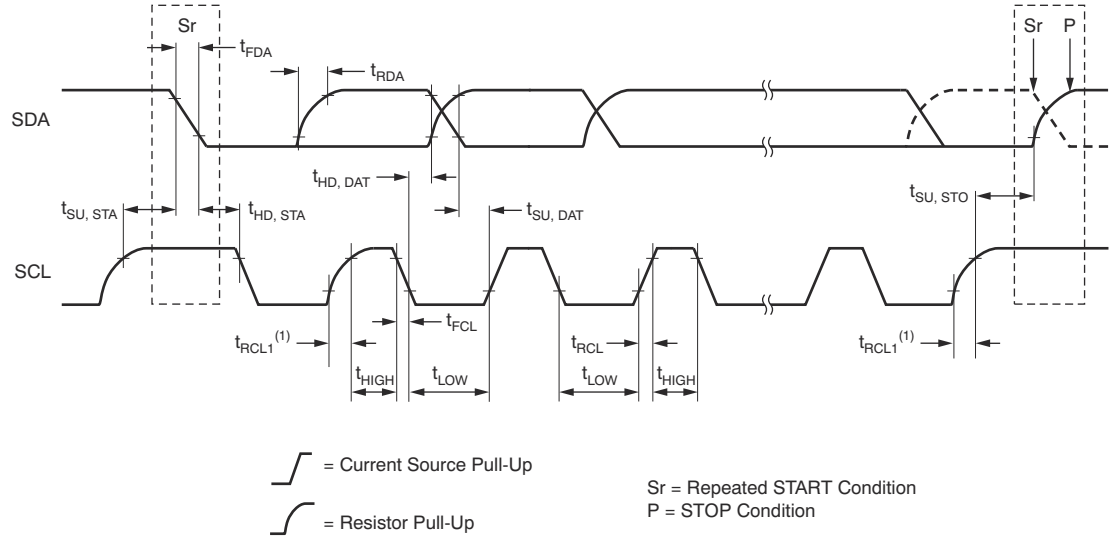


図 6-2. Timing for High-Speed (Hs) Mode Devices on I²C Bus

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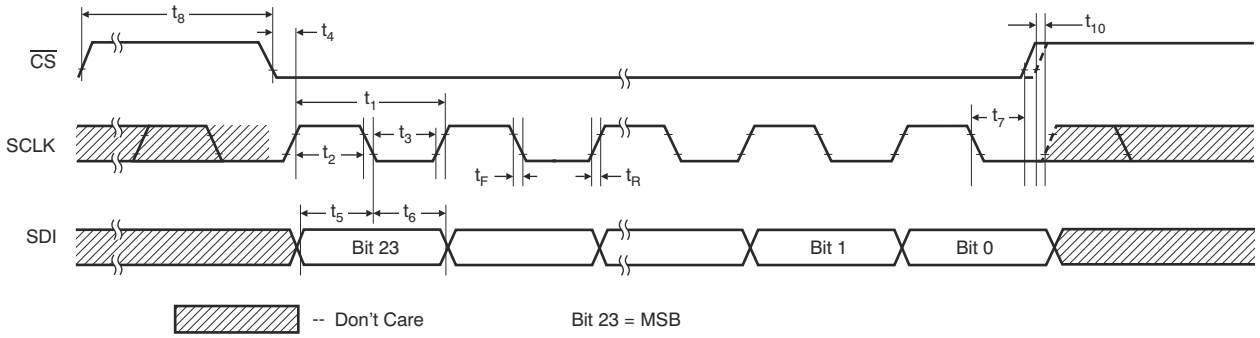


図 6-3. Timing for SPI Single-Chip Write Operation

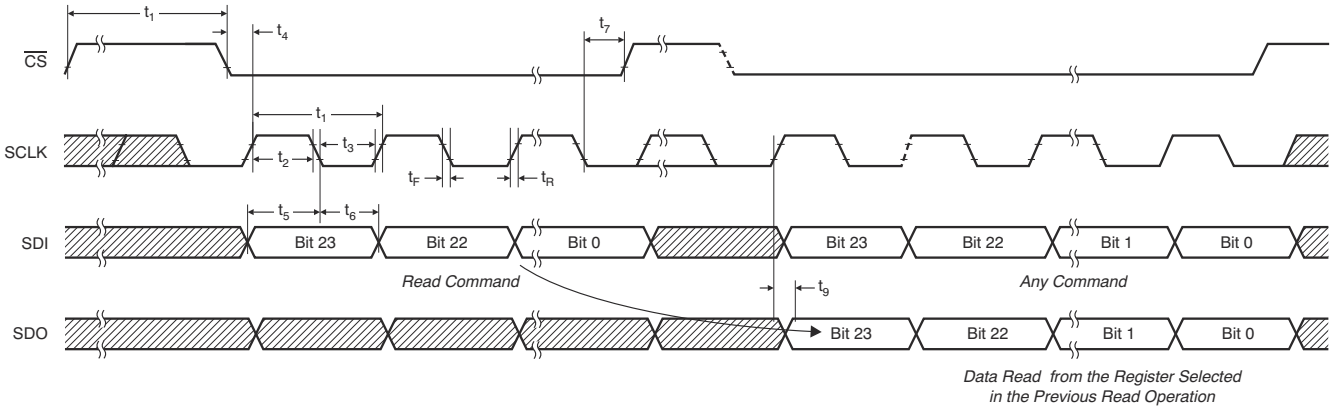


図 6-4. Timing for SPI Single-Chip Read Operation

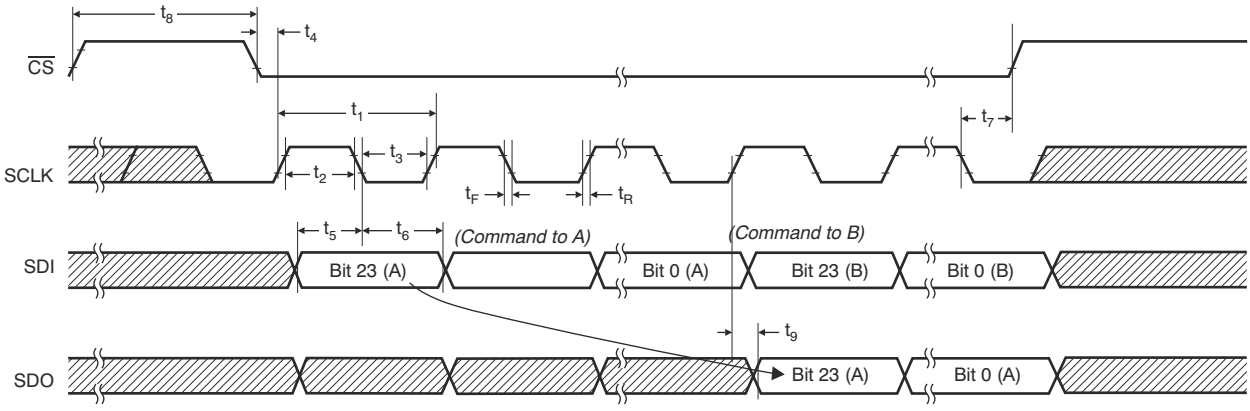
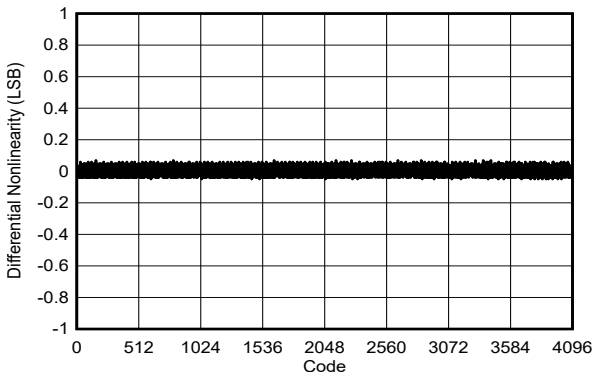


図 6-5. Timing for SPI Daisy-Chain Operation

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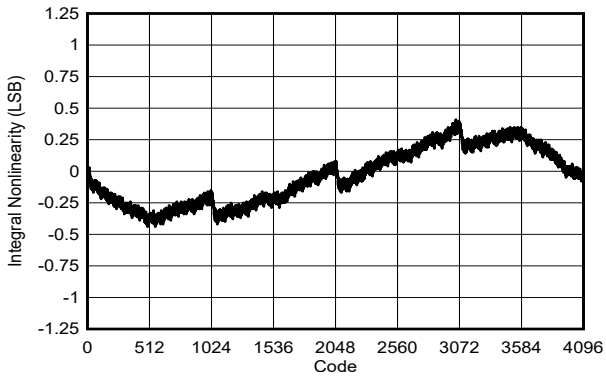
6.8 Typical Characteristics: DAC

at +25°C (unless otherwise noted), V_{REF} generated by internal reference.



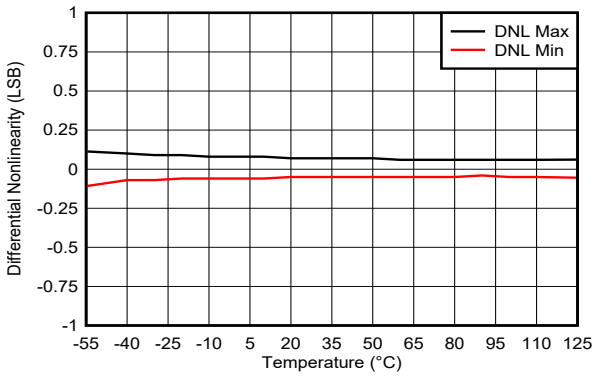
V_{REF} = 2.5 V

図 6-6. Differential Linearity Error vs Code



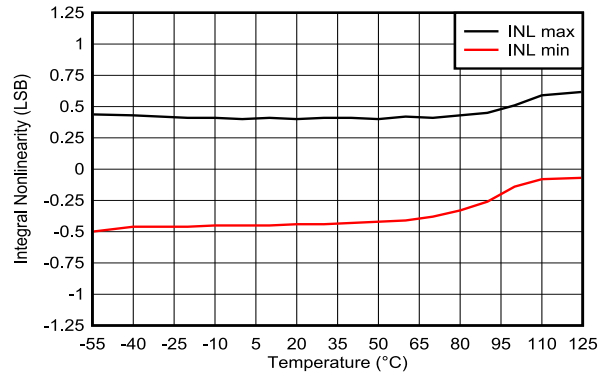
V_{REF} = 2.5 V

図 6-7. Integral Linearity Error vs Code



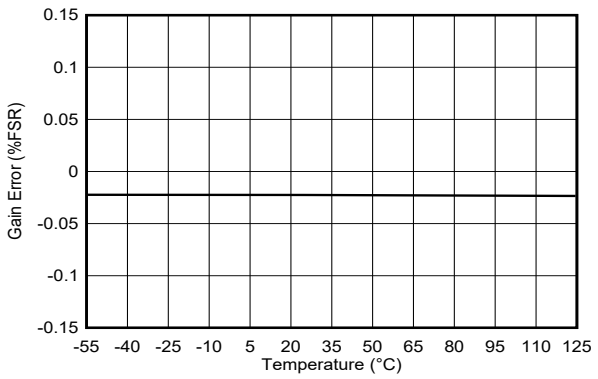
V_{REF} = 2.5 V

図 6-8. Differential Linearity Error vs Temperature



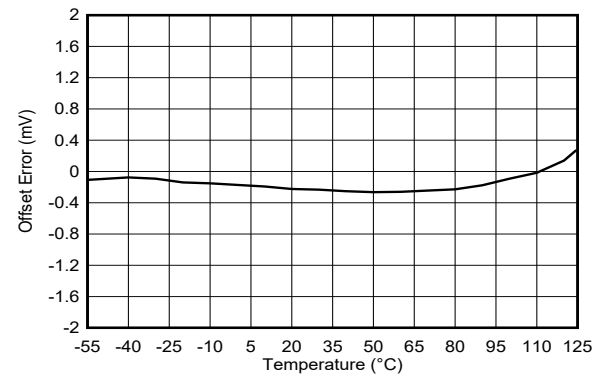
V_{REF} = 2.5 V

図 6-9. Integral Linearity Error vs Temperature



V_{REF} = 2.5 V

図 6-10. Gain Error vs Temperature



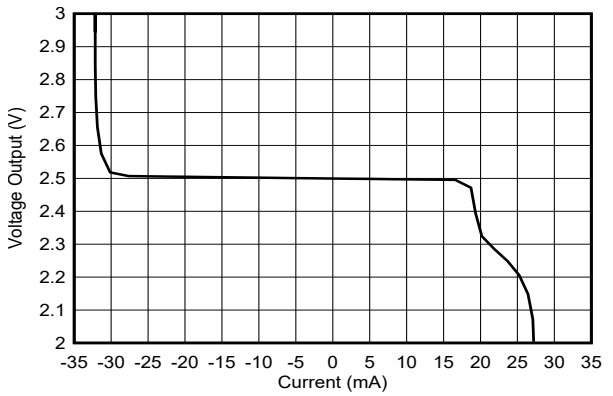
Code = 020h Code = 020h

図 6-11. Offset Error vs Temperature

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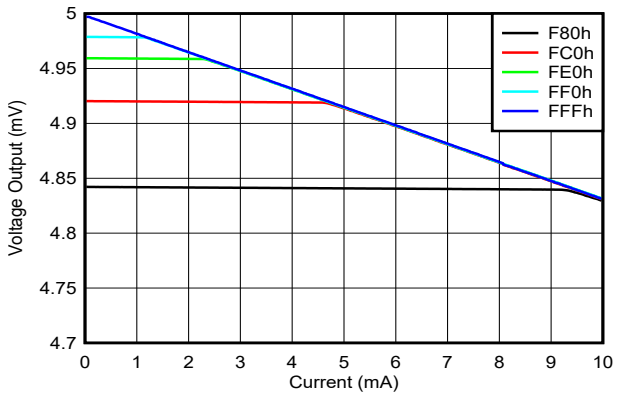
6.8 Typical Characteristics: DAC (continued)

at +25°C (unless otherwise noted), V_{REF} generated by internal reference.



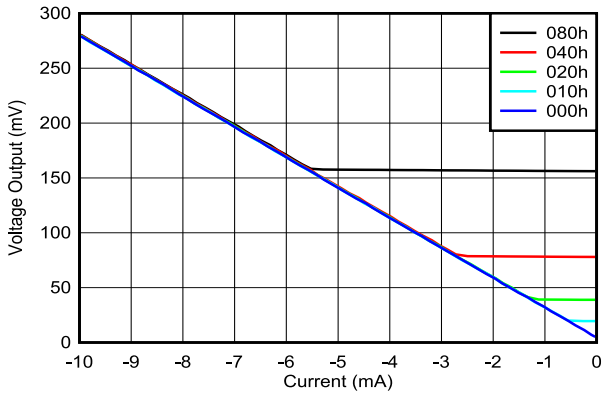
A_{VCC} = 5.5 V Code = 800h V_{REF} = 2.5 V

図 6-12. Output Voltage vs Output Current



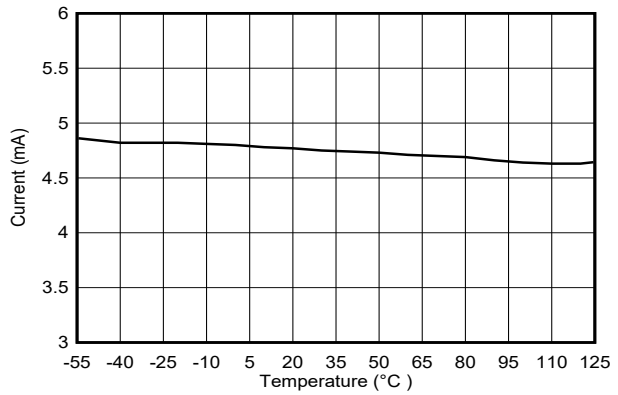
A_{vcc} = 5.5 V V_{REF} = 2.5 V

図 6-13. Output Voltage vs Source Current Capability



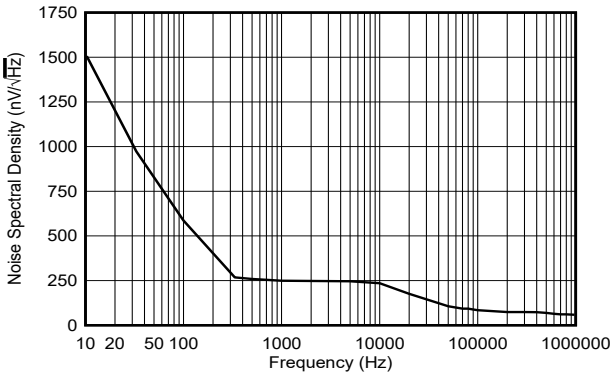
A_{vcc} = 5.5 V V_{REF} = 2.5 V

図 6-14. Output Voltage vs Sink Current Capability



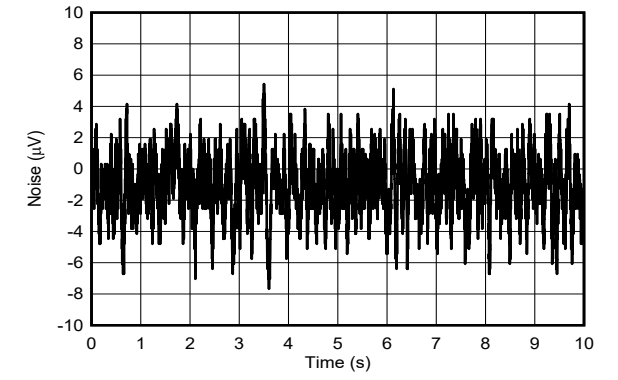
V_{REF} = 2.5 V Code = 800h

図 6-15. Supply Current vs Temperature



V_{REF} = 2.5 V

図 6-16. DAC Noise Voltage vs Frequency



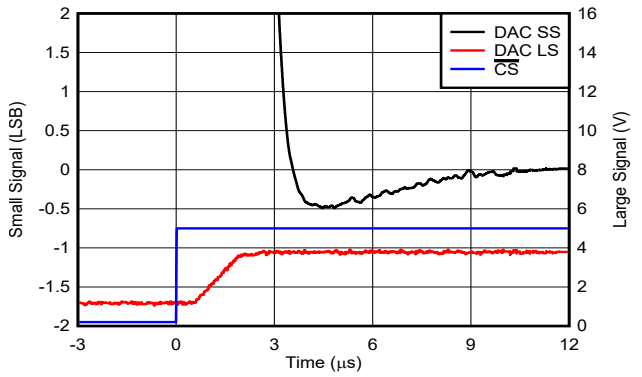
V_{REF} = 2.5 V Code = 800h

図 6-17. DAC Noise (0.1 Hz to 10 Hz)

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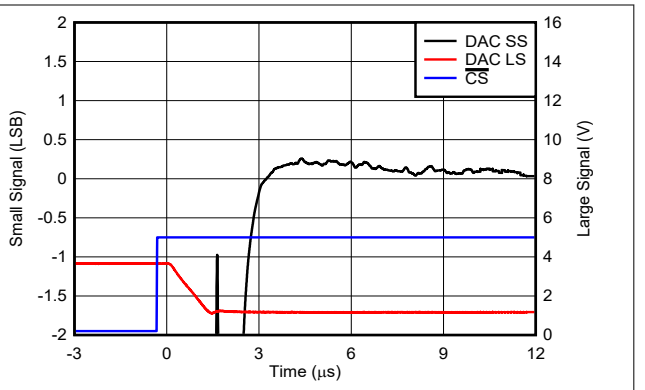
6.8 Typical Characteristics: DAC (continued)

at +25°C (unless otherwise noted), V_{REF} generated by internal reference.



V_{REF} = 2.5 V R_L = 2 kΩ C_L = 250 pF

図 6-18. Settling-Time Rising Edge



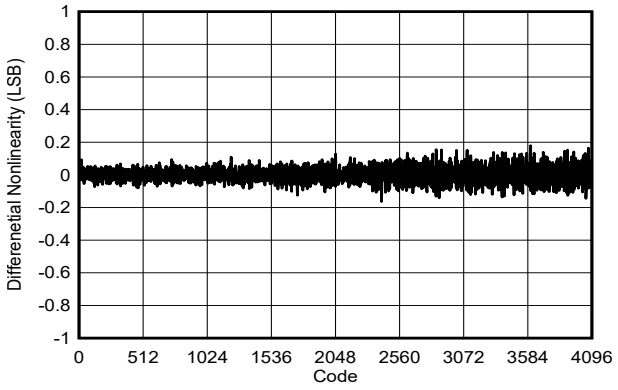
V_{REF} = 2.5 V R_L = 2 kΩ C_L = 250 pF

図 6-19. Settling-Time Falling Edge

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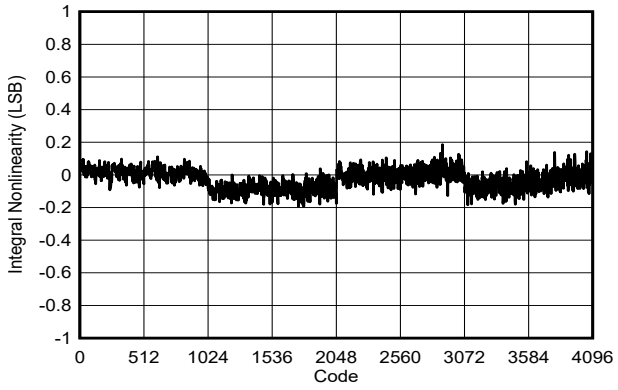
6.9 Typical Characteristics: ADC

t +25°C (unless otherwise noted). V_{REF} generated by internal reference.



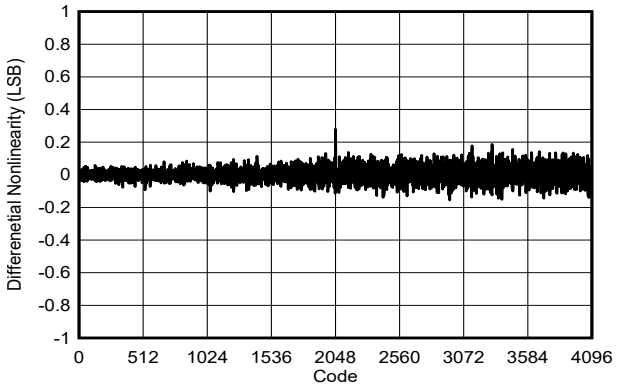
0 to V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-20. Differential Linearity Error vs Code



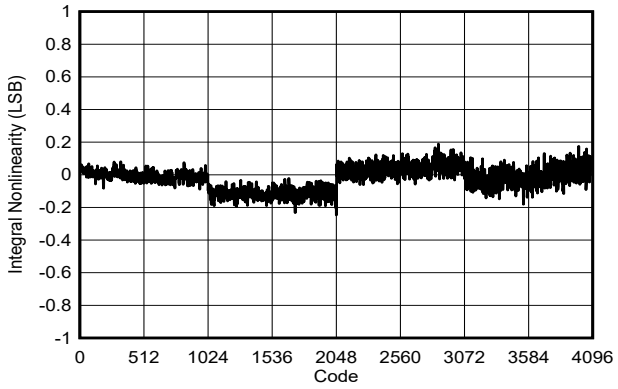
0 to V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-21. Integral Linearity Error vs Code



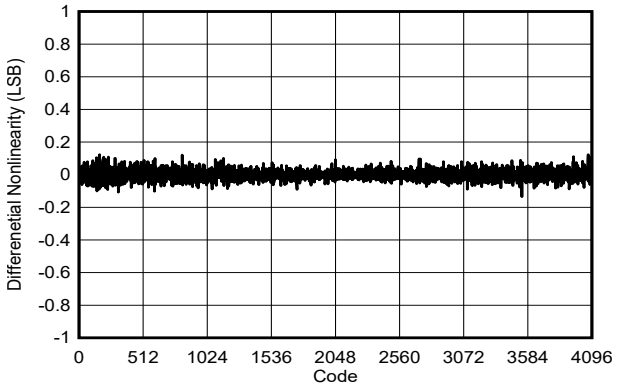
0 to 2 × V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-22. Differential Linearity Error vs Code



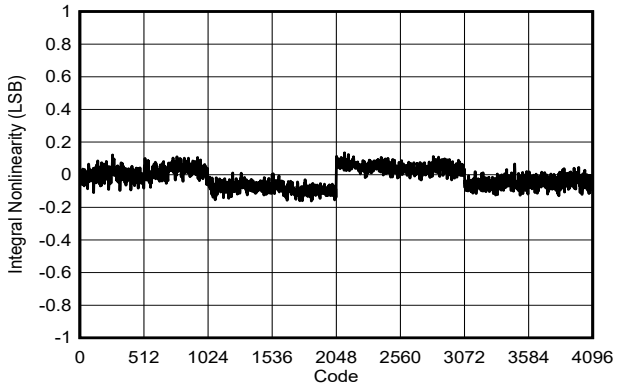
0 to 2 × V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-23. Integral Linearity Error vs Code



0 to V_{REF} range (Differential Mode) V_{REF} = 2.5 V

図 6-24. Differential Linearity Error vs Code



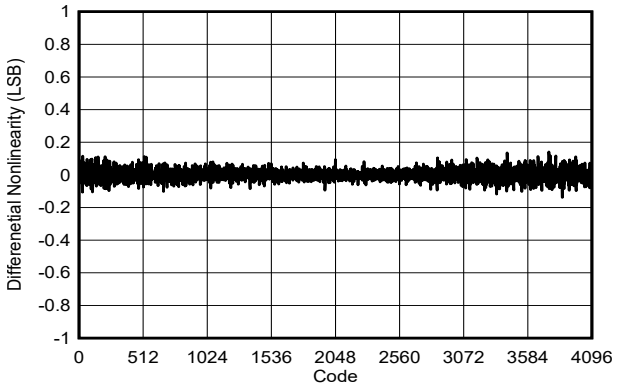
0 to V_{REF} range (Differential Mode) V_{REF} = 2.5 V

図 6-25. Integral Linearity Error vs Code

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6.9 Typical Characteristics: ADC (continued)

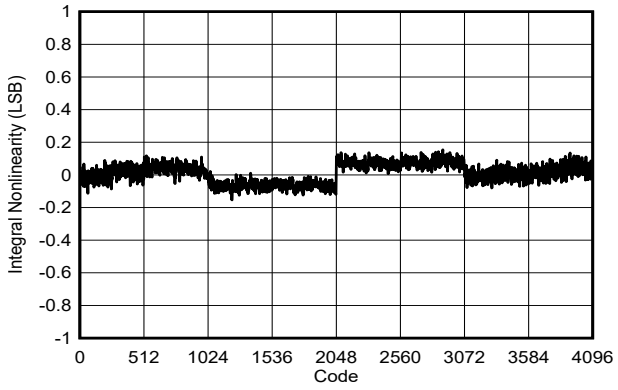
t +25°C (unless otherwise noted). V_{REF} generated by internal reference.



0 to 2 × V_{REF} range (Differential Mode)

V_{REF} = 2.5 V

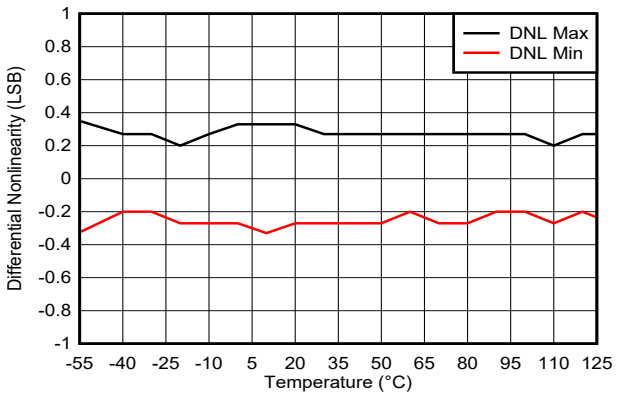
図 6-26. Differential Linearity Error vs Code



0 to 2 × V_{REF} range (Differential Mode)

V_{REF} = 2.5 V

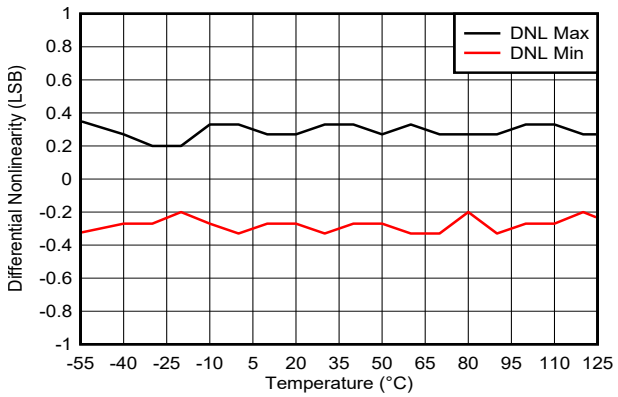
図 6-27. Integral Linearity Error vs Code



0 to V_{REF} range (single-ended mode)

V_{REF} = 2.5 V

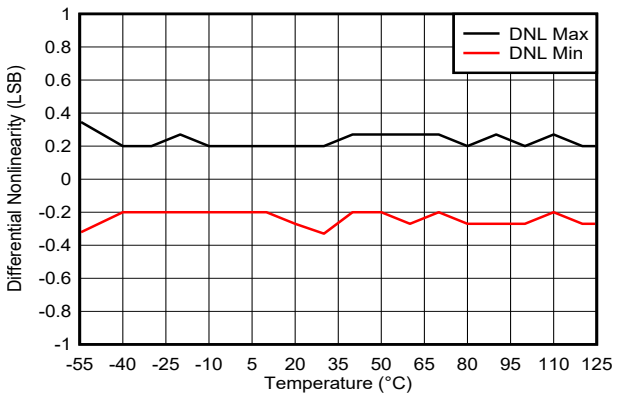
図 6-28. Differential Linearity Error vs Temperature



0 to 2 × V_{REF} range (single-ended mode)

V_{REF} = 2.5 V

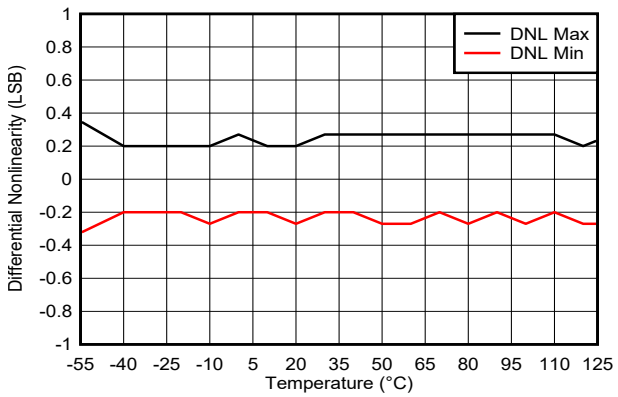
図 6-29. Differential Linearity Error vs Temperature



0 to V_{REF} range (Differential Mode)

V_{REF} = 2.5 V

図 6-30. Differential Linearity Error vs Temperature



0 to 2 × V_{REF} range (Differential Mode)

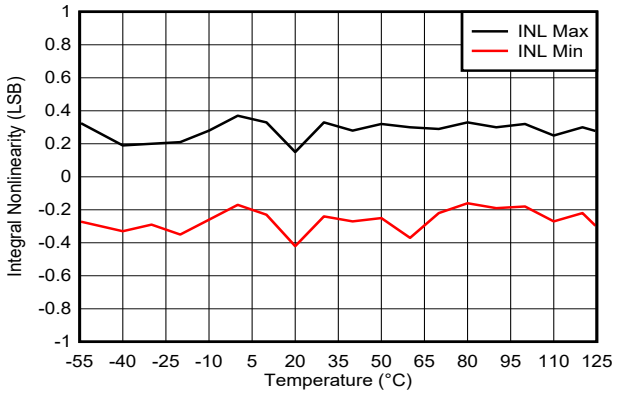
V_{REF} = 2.5 V

図 6-31. Differential Linearity Error vs Temperature

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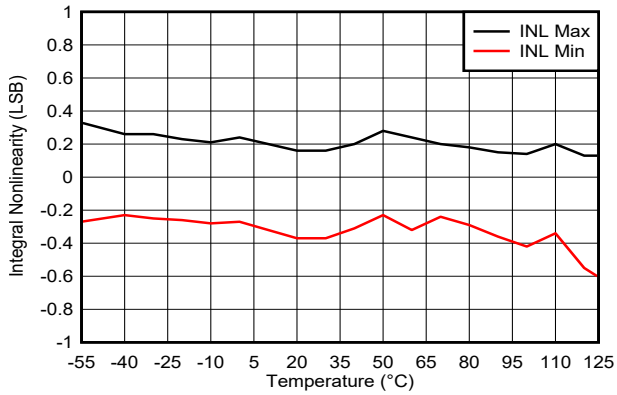
6.9 Typical Characteristics: ADC (continued)

t +25°C (unless otherwise noted). V_{REF} generated by internal reference.



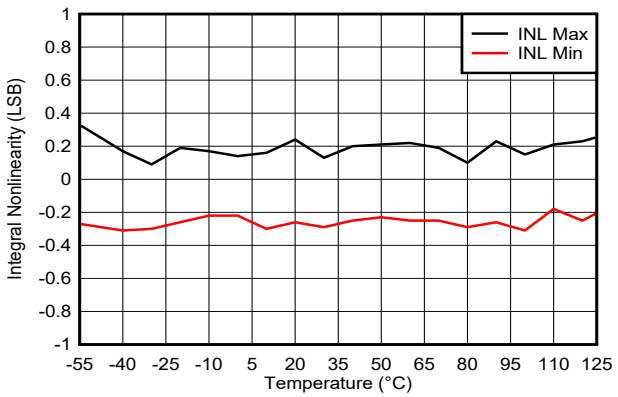
0 to V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-32. Integral Linearity Error vs Temperature



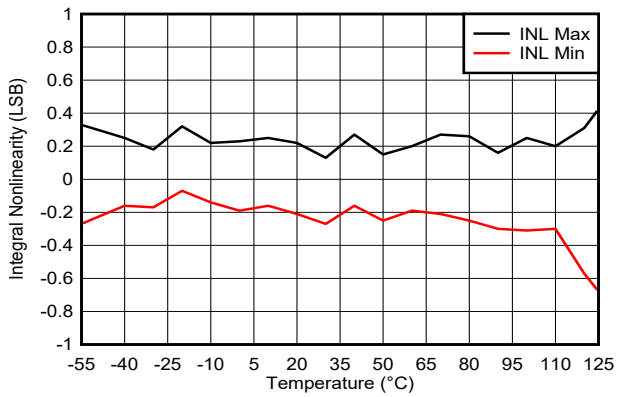
0 to 2 × V_{REF} range (single-ended mode) V_{REF} = 2.5 V

図 6-33. Integral Linearity Error vs Temperature



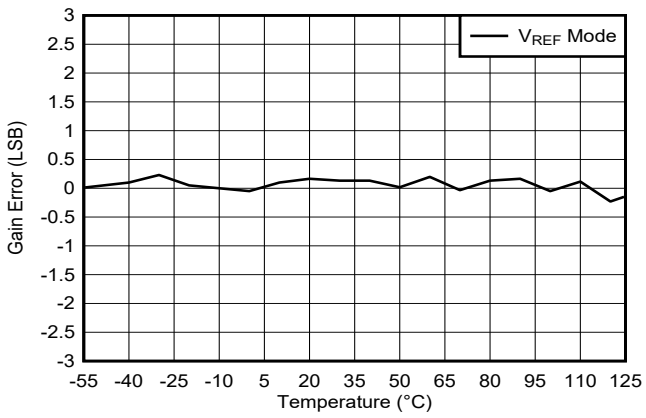
0 to V_{REF} range (Differential Mode) V_{REF} = 2.5 V

図 6-34. Integral Linearity Error vs Temperature



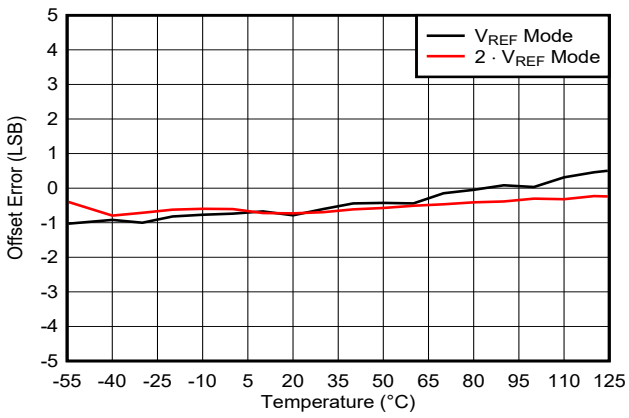
0 to 2 × V_{REF} range (Differential Mode) V_{REF} = 2.5 V

図 6-35. Integral Linearity Error vs Temperature



Single-ended mode V_{REF} = 2.5 V

図 6-36. Gain Error vs Temperature



Single-ended mode V_{REF} = 2.5 V

図 6-37. Offset vs Temperature

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6.9 Typical Characteristics: ADC (continued)

t +25°C (unless otherwise noted). V_{REF} generated by internal reference.

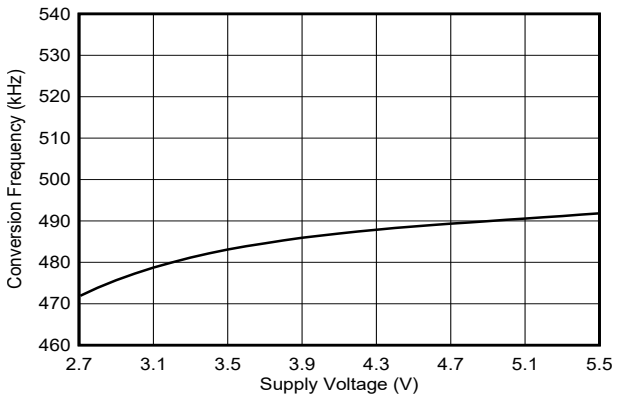


図 6-38. Conversion Frequency vs Supply

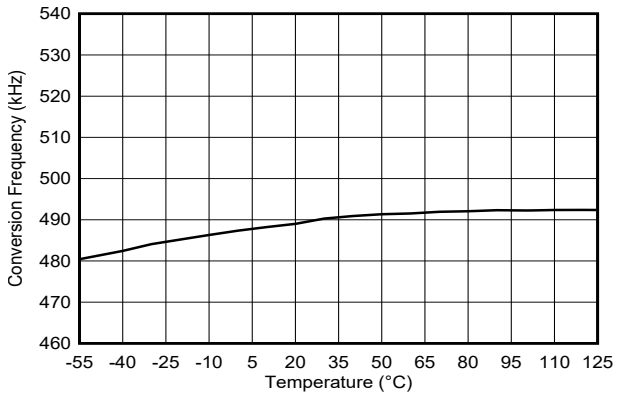


図 6-39. Conversion Frequency vs Temperature

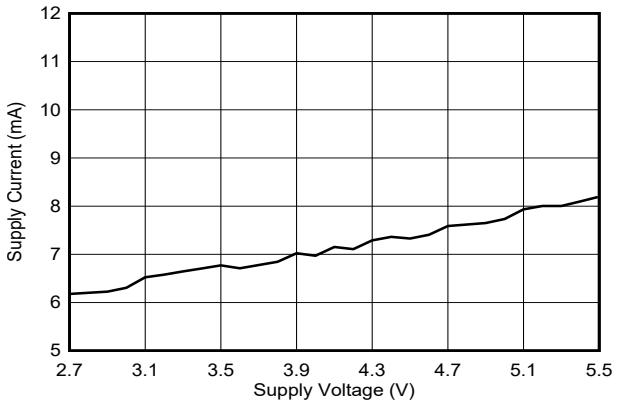


図 6-40. Supply Current vs Supply Voltage

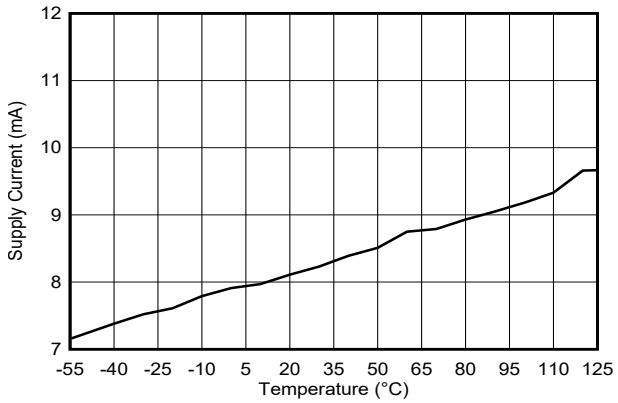


図 6-41. Supply Current vs Temperature

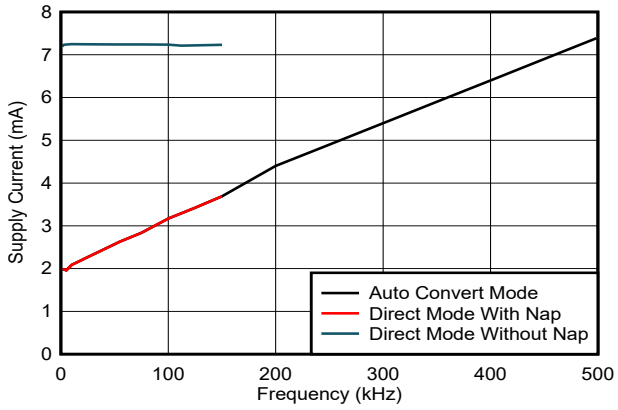


図 6-42. Supply Current vs Conversion Rate

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6.10 Typical Characteristics: Internal Reference

at +25°C (unless otherwise noted)

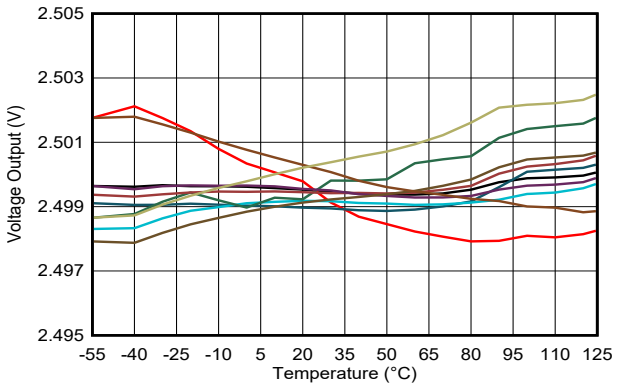


図 6-43. Output Voltage vs Temperature

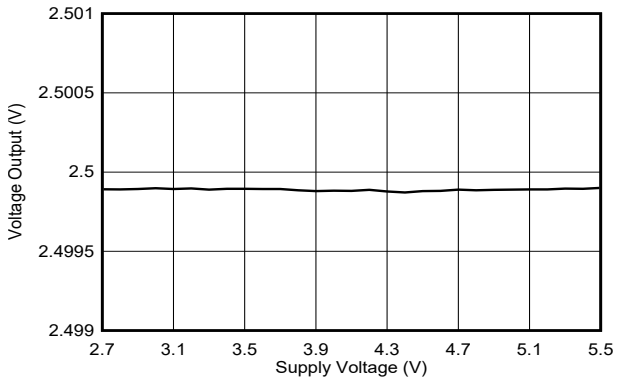


図 6-44. Output Voltage vs Supply

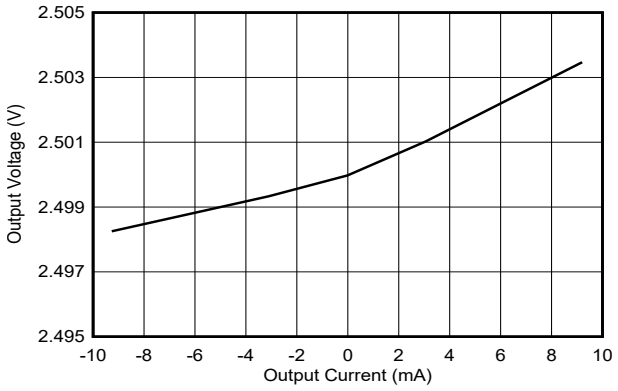


図 6-45. Output Voltage vs Output Current

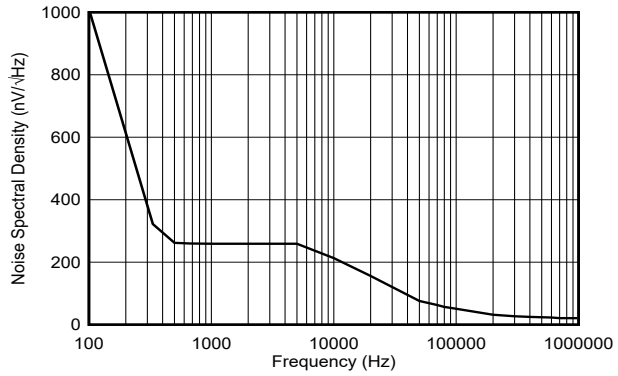


図 6-46. Internal Reference Noise vs Frequency

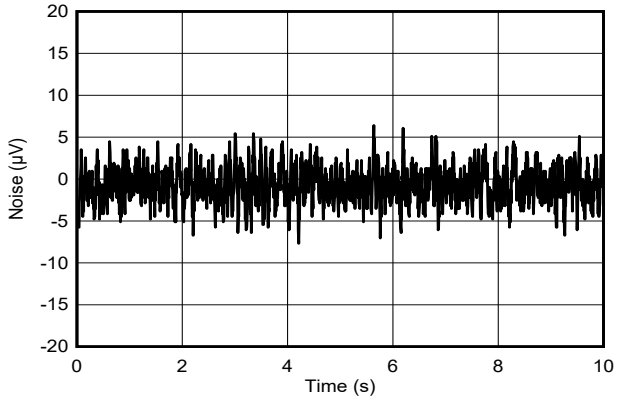


図 6-47. Internal Reference Noise (0.1 Hz to 10 Hz)

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6.11 Typical Characteristics: Temperature Sensor

at +25°C (unless otherwise noted)

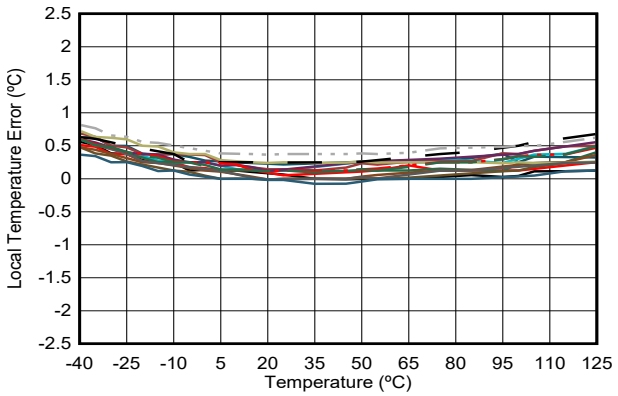


図 6-48. Local Temperature Error vs Temperature

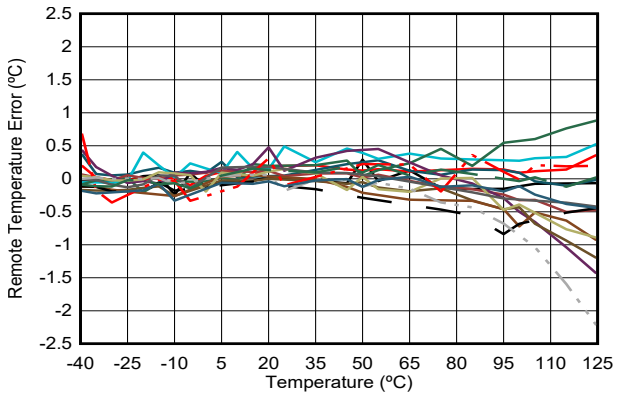


図 6-49. Remote Temperature Error vs Temperature

6.12 Typical Characteristics: Digital Inputs

at +25°C (unless otherwise noted)

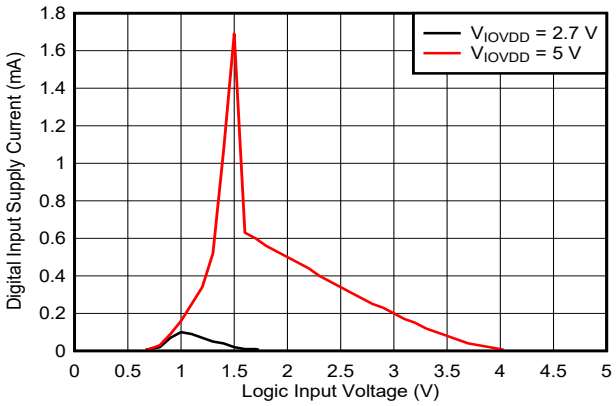


図 6-50. Supply Current vs Input Voltage

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7 Detailed Description

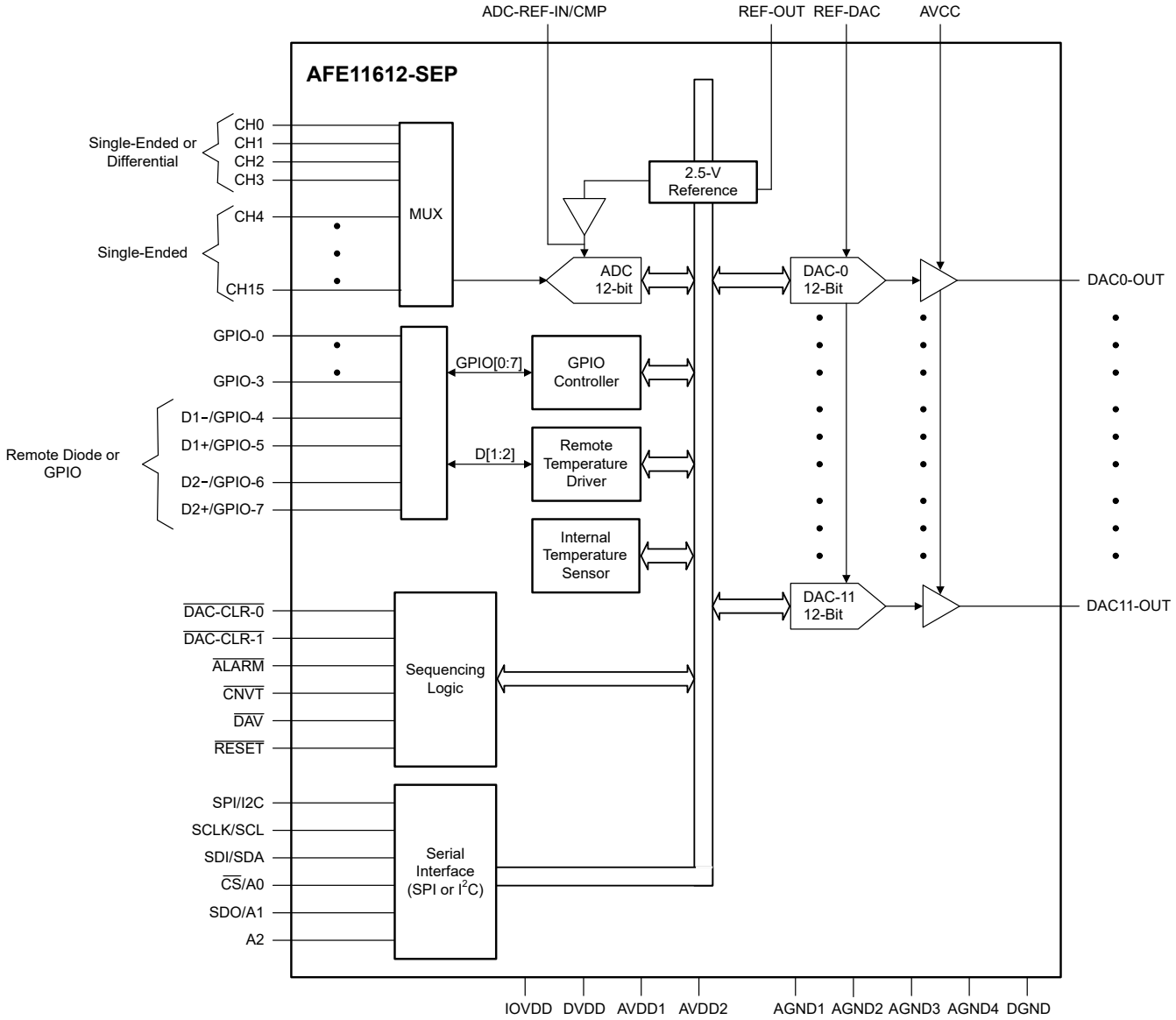
7.1 Overview

The AFE11612-SEP is a highly integrated analog monitor and control device with gate bias switch control that is capable of voltage and temperature supervision.

The AFE11612-SEP features twelve 12-bit digital-to-analog converters (DACs) that all operate at a 0-V to 5-V output voltage range. The device also features a 2.5-V internal reference, with an output current limited to 200 mA.

The AFE11612-SEP external signal supervisor uses an accurate analog-to-digital converter (ADC) that samples input data using two unique conversion modes. The supervisor is capable of monitoring high-voltage external inputs, high-common mode current sense inputs, and the device internal temperature. Communication to the device is performed through an SPI- and I^{2}C-compatible interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Primary ADC Operation

The device has two analog-to-digital converters (ADCs): a primary ADC and a secondary ADC. The primary ADC features a 16-channel multiplexer, an on-chip track-and-hold, and a successive approximation register (SAR) ADC based on a capacitive digital-to-analog converter (DAC). This ADC runs at 500 kSPS and converts the analog channel inputs, CH0 to CH15. The analog input range for the device can be selected as 0 V to V_{REF} or 0 V to (2 × V_{REF}). The analog input can be configured for either single-ended or differential signals. The device has an on-chip 2.5-V reference that can be disabled when an external reference is preferred. If the internal ADC reference is to be used elsewhere in the system, the output must first be buffered. The various monitored and uncommitted input signals are multiplexed into the ADC. The secondary ADC is a part of the temperature-sensing function that converts the analog temperature signals.

7.3.1.1 Analog Inputs

The device has 16 uncommitted analog inputs; 12 of these inputs (CH4 to CH15) are single-ended. The inputs for CH0 to CH3 can be configured as four single-ended inputs or two fully-differential channels, depending on the setup of the ADC channel registers, ADC Channel Register 0 and ADC Channel Register 1. See *セクション 7.6* for details. 図 7-1 shows the device equivalent input circuit. The (peak) input current through the analog inputs depends on the sample rate, input voltage, and source impedance. The current into the device charges the internal capacitor array during the sample period. After this capacitance is fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance to a 12-bit settling level within the acquisition time. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

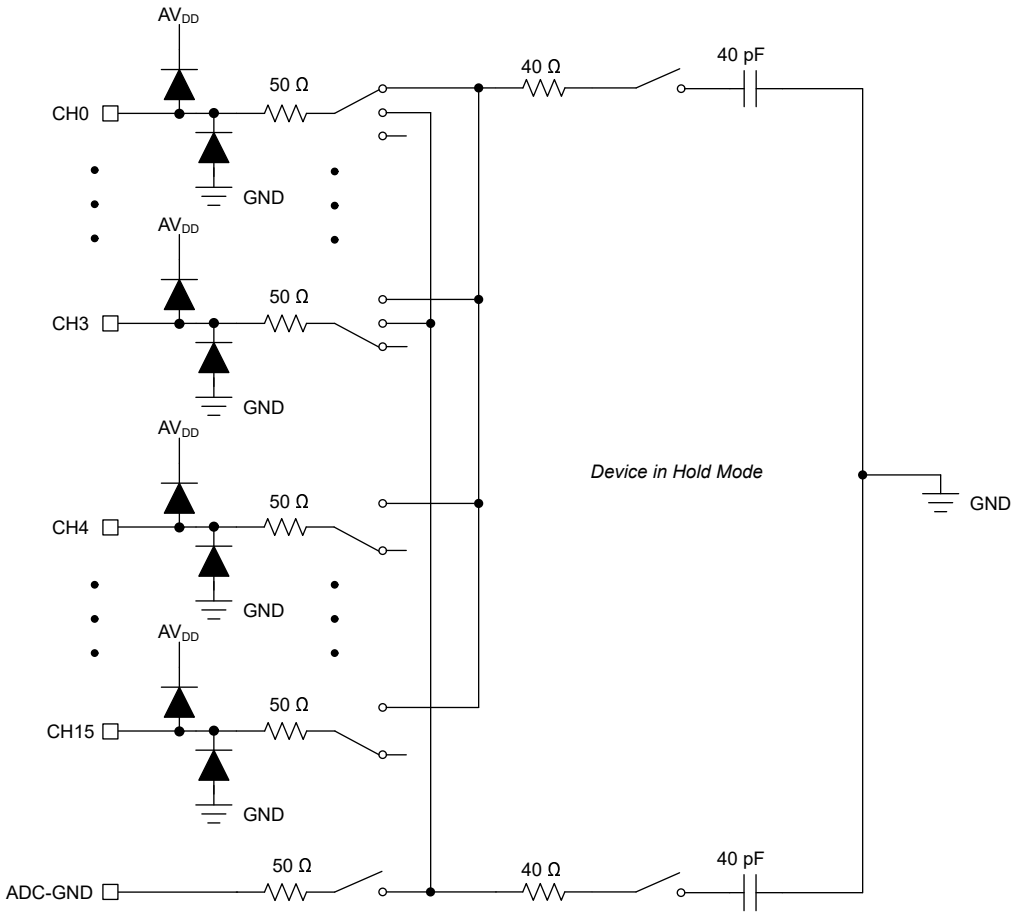


図 7-1. Equivalent Input Circuit

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7.3.1.1.1 Single-Ended Analog Input

In applications where the signal source has high impedance, buffer the analog input. The analog input range can be programmed to be either 0 V to V_{REF} or 0 V to (2 × V_{REF}). In 2 × V_{REF} mode, the input is effectively divided by two before the conversion takes place. The voltage with respect to GND on the ADC analog input pins cannot exceed AV_{DD}.

7.3.1.1.2 Fully Differential Input

When the device is configured as a differential input, the differential signal is defined as V_{DM}, as shown in 図 7-2(a). The differential signal is the equivalent of the difference between the V1 and V2 signals, as shown in 図 7-2(b). The common-mode input V_{COMMON} is equal to (V1 + V2) / 2.

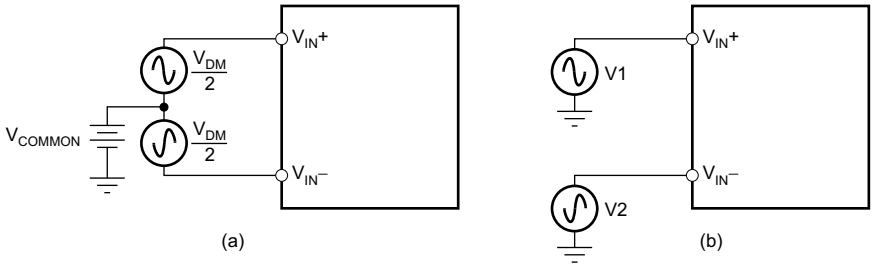


図 7-2. Fully Differential Analog Input

When the conversion occurs, only the differential mode voltage (V_{DM}) is converted; the common-mode voltage (V_{COMMON}) is rejected. This process results in a virtually noise-free signal with a maximum amplitude of –V_{REF} to +V_{REF} for the V_{REF} range, or (–2 × V_{REF}) to (+2 × V_{REF}) for the (2 × V_{REF}) range. The results are stored in straight binary or 2's complement format.

7.3.1.2 ADC Trigger Signals (See AFE configuration register 0)

The ADC can be triggered externally by the falling edge of the external trigger $\overline{CNVT}$, or internally by writing to the ICONV bit in AFE Configuration Register 0. The ADC channel registers specify which external analog channel is converted.

When a new trigger activates, the ADC stops any existing conversion immediately and starts a new cycle. For example, the ADC is programmed to sample channel 0 to channel 3 repeatedly (auto-mode). During the conversion of channel 1, an external trigger is activated. The ADC stops converting channel 1 immediately and starts converting channel 0 again, instead of proceeding to convert channel 2.

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7.3.1.3 Double-Buffered ADC Data Registers

The host can access all 16, double-buffered ADC data registers, as shown in 図 7-3. The conversion result from the analog input with channel address *n* (where n = 0 to 15) is stored in the ADC-*n*-data register. When the conversion of an individual channel completes, the data are immediately transferred into the corresponding ADC-*n* temporary (TMPRY) register, the first stage of the data buffer. When the conversion of the last channel completes, all data in the ADC-*n* TMPRY registers are simultaneously transferred into the corresponding ADC-*n*-data registers, the second stage of the data buffer. However, if a data transfer is in progress between any ADC-*n*-data register and the AFE shift register, no ADC-*n*-data registers are updated until the data transfer is complete. The conversion result from channel address *n* is stored in the ADC-*n*-data register. For example, the result from channel 0 is stored in the ADC-0-data register, and the result from channel 3 is stored in the ADC-3-data register.

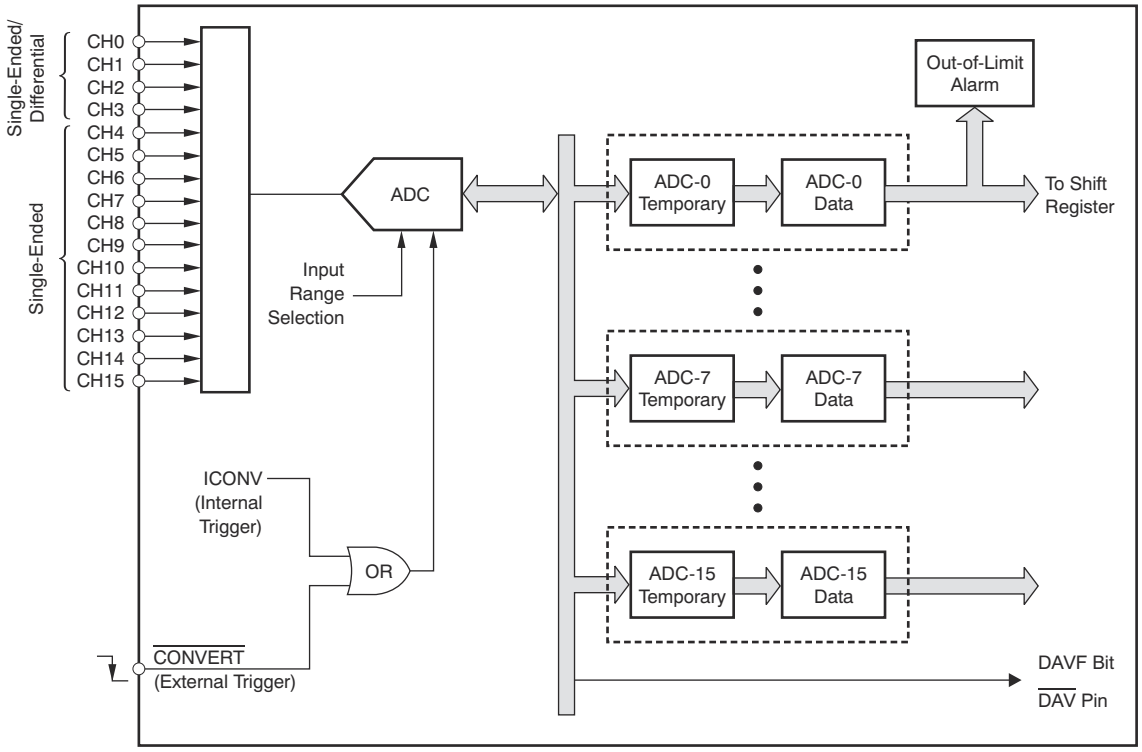


図 7-3. Double-Buffered ADC Structure

7.3.1.3.1 ADC Data Format

For a single-ended input, the conversion result is stored in straight binary format. For a differential input, the results are stored in 2's complement format.

7.3.1.4 SCLK Clock Noise Reduction

To avoid noise caused by the bus clock, TI recommends that no bus clock activity occur for at least the conversion process time immediately after the ADC conversion starts.

7.3.1.5 Data Available Pin ($\overline{DAV}$)

$\overline{DAV}$ is an output pin that indicates the completion of ADC conversions. The DAVF bit in AFE configuration register 0 determines the status of the $\overline{DAV}$ pin. In direct mode, after the selected group of input channels are converted and the ADC is stopped, the DAVF bit is set to 1 and the $\overline{DAV}$ pin is driven to logic low (active). In ADC auto mode, each time the group of input channels are sequentially converted, a 1-µs pulse (low) appears on the $\overline{DAV}$ pin.

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7.3.1.6 Convert Pin ($\overline{CNVT}$)

$\overline{CNVT}$ is the input pin for the external ADC trigger signal. ADC channel conversions begin on the falling edge of the $\overline{CNVT}$ pulse. If a $\overline{CNVT}$ pulse occurs when the ADC is already converting, then the ADC continues converting the current channel. After the current channel completes, the existing conversion cycle finishes and a new conversion cycle starts. The selected channels specified in the ADC channel registers are converted sequentially in order of enabled channels.

7.3.1.7 Analog Input Out-of-Range Detection (See The *Analog Input Out-of-Range Alarm* Section)

The CH0 to CH3 analog inputs and the temperature inputs are implemented with out-of-range detection. When any of these inputs is out of the preset range, the corresponding alarm flag in the status register is set. If any inputs are out of range, the global out-of-range pin ($\overline{ALARM}$) goes low. To avoid a false alarm, the device is implemented with false-alarm protection. See the *Alarm Operation* section for more details.

7.3.1.8 Full-Scale Range of the Analog Input

The gain bit of the ADC gain register determines the full-scale range of the analog input. Full-scale range is V_{REF} when ADG*n* = 0, or ($2 \times V_{REF}$) when ADG*n* = 1. If a channel pair is configured for differential operation, the input ranges are either $\pm V_{REF}$ or $\pm(2 \times V_{REF})$. In ($2 \times V_{REF}$) mode, the input is effectively divided by two before the conversion takes place. Each input must not exceed the supply value of AV_{DD} + 0.2 V or AGND – 0.2 V. When the REF-OUT pin is connected to the REF-ADC pin, the internal reference is used as the ADC reference. When an external reference voltage is applied to the REF-ADC pin, the external reference is used as the ADC reference.

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7.3.2 Secondary ADC and Temperature Sensor Operation

The device contains one local and two remote temperature sensors. The temperature sensors continuously monitor the three temperature inputs, and new readings are automatically available every cycle. The on-chip integrated temperature sensor (shown in 図 7-4) is used to measure the device temperature. Two remote diode sensor inputs are used to measure the two external temperatures. All analog signals are converted by the secondary ADC that runs in the background at a lower speed. The measurement relies on the characteristics of a semiconductor junction operation at a fixed current level. The forward voltage of the diode (V_{BE}) depends on the current passing through the diode and the ambient temperature. The change in V_{BE} when the diode operates at two different currents (a low current of I_{LOW} and a high current of I_{HIGH}) is shown in 式 1:

$$V_{BE_HIGH} - V_{BE_LOW} = \frac{\eta kT}{q} \ln\left(\frac{I_{HIGH}}{I_{LOW}}\right) \quad (1)$$

where:

- k is Boltzmann's constant.
- q is the charge of the carrier.
- T is the absolute temperature in kelvins (K).
- η is the ideality of the transistor as a sensor.

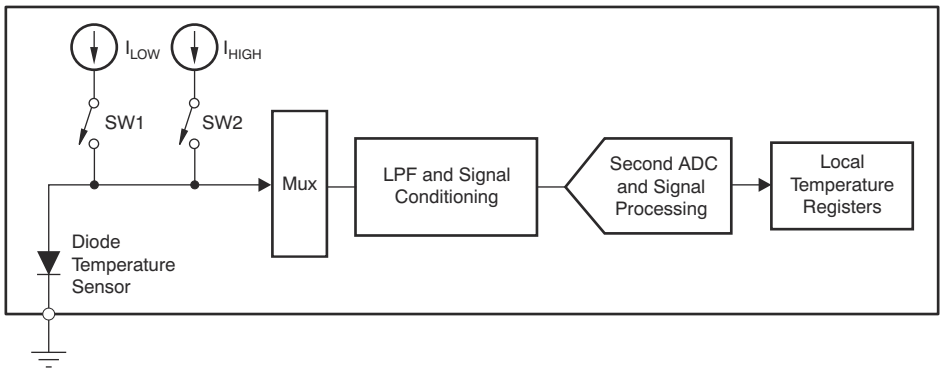


図 7-4. Integrated Local Temperature Sensor

The remote sensing transistor can be a discrete, small-signal type transistor or a substrate transistor built within the microprocessor. This architecture is shown in 図 7-5. An internal voltage source biases the D– pin above ground to prevent the ground noise from interfering with measurement. An external capacitor (up to 330 pF) can be placed between D+ and D– to further reduce noise interference.

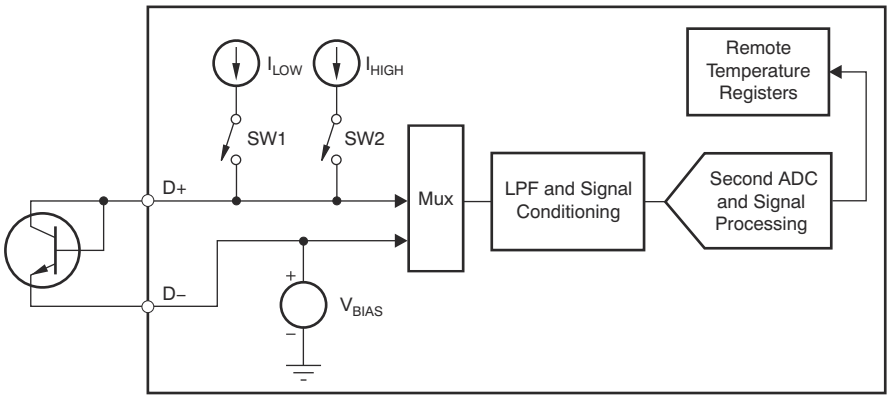


図 7-5. Remote Temperature Sensor

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The device has three temperature sensors: two remote (D1 and D2) and one on-chip (LT). If any sensor is not used, the sensor can be disabled by clearing the corresponding enable bit (bits D2EN, D1EN, and LTEN of the temperature configuration register). When disabled, the sensors are not converted. The device continuously monitors the selected temperature sensors in the background, leaving the user free to perform conversions on the other channels. When one monitor cycle finishes, a signal passes to the control logic to automatically initiate a new conversion.

The analog sensing signal is preprocessed by a low-pass filter and signal-conditioning circuitry, and then digitized by the ADC. The resulting digital signal is further processed by the digital filter and processing unit. The final result is stored in the LT-temperature-data register, the D1-temperature-data register, and the D2-temperature-data register, respectively. The format of the final result is in 2's complement, as shown in 表 7-1.

表 7-1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL CODE
+255.875	011111111111
+150	010010110000
+100	001100100000
+50	000110010000
+25	000011001000
+1	000000001000
0	000000000000
–1	111111111000
–25	111100111000
–50	111001110000
–100	110011100000
–150	101101010000
–256	100000000000

7.3.2.1 Remote Sensing Diode

Errors in remote temperature sensor readings are typically the consequence of the ideality factor and current excitation used by the device versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a low-level (I_{LOW}) and high-level (I_{HIGH}) current for the temperature-sensing substrate transistors. The device uses 6 µA for I_{LOW} and 120 µA for I_{HIGH}. The device is designed to function with discrete transistors, such as the 2N3904 and 2N3906. If an alternative transistor is used, the device operates as specified, as long as the following conditions are met:

1. Base-emitter voltage is greater than 0.25 V at 6 µA, at the highest sensed temperature.
2. Base-emitter voltage is less than 0.95 V at 120 µA, at the lowest sensed temperature.
3. Base resistance is less than 100 Ω.
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

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7.3.2.2 Ideality Factor

The ideality factor (η) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The device allows for different η-factor values, according to 表 7-2. The device is trimmed for a power-on reset (POR) value of η = 1.008. If η is different, the η-factor correction register can be used. The value (N_{ADJUST}) written in this register must be in 2's complement format, as shown in 表 7-2. This value is used to adjust the effective η-factor according to 式 2 and 式 3.

表 7-2. η-Factor Range (Single Byte)

N_{ADJUST}			η_{EFF}
BINARY	HEX	DECIMAL	
0111 1111	7F	127	1.747977
0000 1010	0A	10	1.042759
0000 1000	08	8	1.035616
0000 0110	06	6	1.028571
0000 0100	04	4	1.021622
0000 0010	02	2	1.014765
0000 0001	01	1	1.011371
0000 0000	00	0	1.008
1111 1111	FF	–1	1.004651
1111 1110	FE	–2	1.001325
1111 1100	FC	–4	0.994737
1111 1010	FA	–6	0.988235
1111 1000	F8	–8	0.981818
1111 0110	F6	–10	0.975484
1000 0000	80	–128	0.706542

$$\eta_{eff} = \frac{1.008 \times 300}{300 - N_{ADJUST}} \quad (2)$$

$$N_{ADJUST} = 300 - \left(\frac{300 \times 1.008}{\eta_{eff}} \right) \quad (3)$$

where:

- η_{EFF} is the actual ideality of the transistor used and
- N_{ADJUST} is the corrected ideality used in the calculation.

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7.3.2.3 Filtering

図 7-6(a) and 図 7-6(b) show the connection of recommended NPN or PNP transistors, respectively. Remote junction temperature sensors are usually implemented in a noisy environment. Noise is most often created by fast digital signals, and can corrupt measurements. The device has a built-in 65-kHz filter on the D+ and D– inputs to minimize the effects of noise. However, a bypass capacitor placed differentially across the inputs of the remote temperature sensor can make the application more robust against unwanted coupled signals. If filtering is required, limit the capacitance between D+ and D– to 330 pF or less for good measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the device.



(a) NPN (b) PNP

図 7-6. Remote Temperature Sensor Using Transistor

7.3.2.4 Series Resistance Cancellation

Parasitic resistance (in series with the remote diode) to the D+ and D– inputs of the device is caused by a variety of factors, including printed circuit board (PCB) trace resistance and trace length. This series resistance appears as a temperature offset in the remote sensor temperature measurement, and causes more than 0.45°C error per ohm. The device implements a technology to automatically cancel out the effect of this series resistance, thus providing a more accurate result without requiring user characterization of this resistance. With this technology, the device is able to reduce the effects of series resistance to typically less than 0.0075°C per ohm. The resistance cancellation is disabled when the RC bit in the temperature configuration register is cleared (0).

7.3.2.5 Reading Temperature Data

Temperature is always read as 12-bit data. When the conversion finishes, the temperature is sent to the corresponding temperature-data register. However, if a data transfer is in progress between the temperature-data register and the AFE shift register, the temperature-data register is frozen until data transfer completes.

7.3.2.6 Conversion Time

The conversion time depends on the type of sensor and configuration, as shown in 表 7-3.

表 7-3. Conversion Times

TEMPERATURE SENSOR	MONITORING CYCLE TIME (ms)	PROGRAMMABLE DELAY RANGE (s)
Local sensor is active, remote sensors are disabled or in power-down	15	0.48 to 3.84
One remote sensor is active and RC = 0, local sensor and one remote sensor are disabled or in power-down	44	1.40 to 11.2
One remote sensor is active and RC = 1, local sensor and one remote sensor are disabled or in power-down	93	2.97 to 23.8
One remote sensor and local sensor are active and RC = 0, one remote sensor is disabled or in power-down	59	1.89 to 15.1
One remote sensor and local sensor are active and RC = 1, one remote sensor is disabled or in power-down	108	3.45 to 27.65
Two remote sensors are active and RC = 0, local sensor is disabled or in power-down	88	2.81 to 22.5
Two remote sensors are active and RC = 1, local sensor is disabled or in power-down	186	5.95 to 47.6
All sensors are active and RC is 0	103	3.92 to 26.38
All sensors are active and RC is 1	201	6.43 to 51.45

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7.3.3 Reference Operation

This section describes the operation of the internal and external references.

7.3.3.1 Internal Reference

The device includes a 2.5-V internal reference. The internal reference is externally available at the REF-OUT pin. A 100-pF to 10-nF capacitor is recommended between the reference output and GND for noise filtering. The internal reference is a bipolar transistor-based, precision band-gap voltage reference. The output current is limited by design to approximately 100 mA.

The internal reference drives all temperature sensors. When connecting the REF-OUT pin to the REF-DAC pin, the internal reference functions as the DAC reference.

The ADC-REF-IN/CMP pin has a dual function. When an external reference is connected to this pin, the external reference is used as the ADC reference. When a compensation capacitor (4.7 µF, typical) is connected between this pin and AGND, the internal reference is used as the ADC reference. When using an external reference to drive the ADC, the ADC-REF-INT bit in AFE configuration register 0 must be cleared (0) to turn off the ADC reference buffer. When using the internal reference to drive the ADC, the ADC-REF-INT bit in AFE configuration register 0 must be set to 1 to turn on the ADC reference buffer.

7.3.3.2 External Reference

図 7-7 shows how the external reference is used as the DAC reference when applied on the DAC-REF pin, and as the ADC reference when applied on the ADC-REF pin. 図 7-8 shows the use of the internal reference.

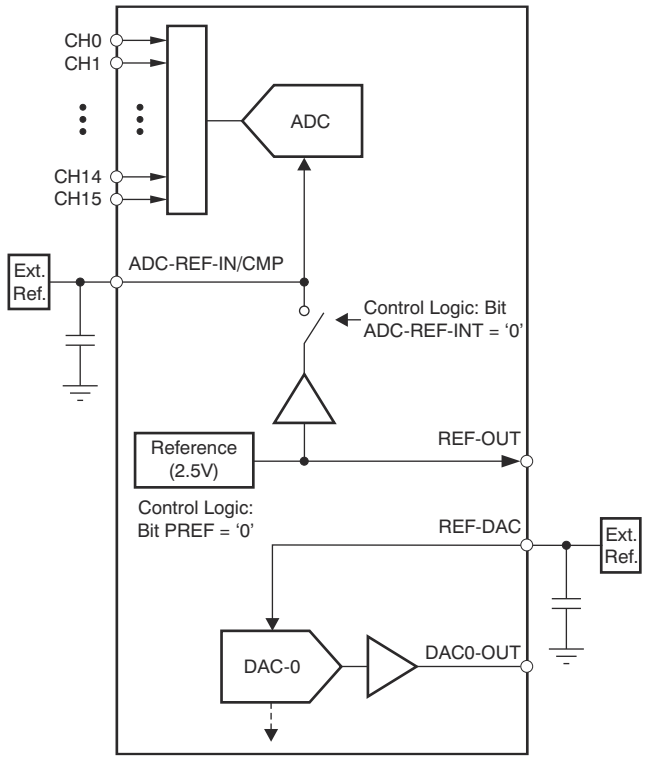


図 7-7. Use of the External Reference

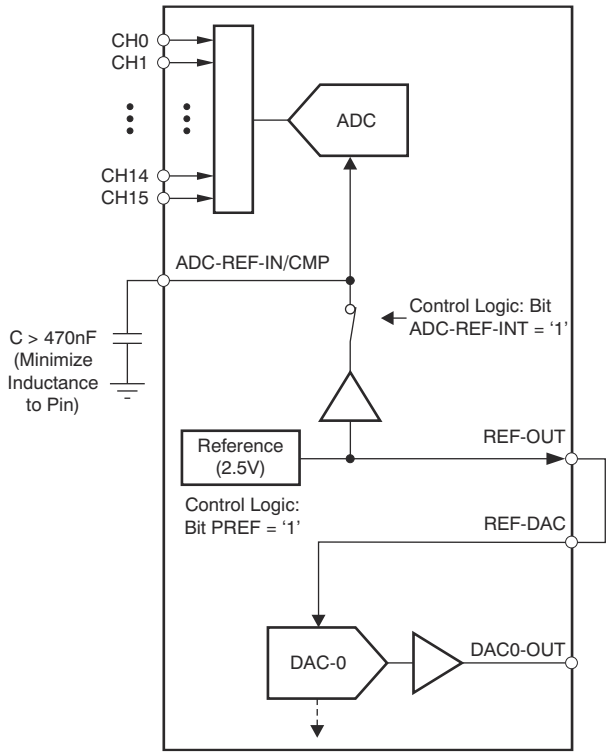


図 7-8. Use of the Internal Reference

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7.3.4 DAC Operation

The device contains 12 DACs that provide digital control with 12 bits of resolution using an internal or external reference. The DAC core is a 12-bit string DAC and output buffer. The DAC drives the output buffer to provide an output voltage. Refer to the DAC configuration register for details. 図 7-9 shows a function block diagram of the DAC architecture. The DAC latch stores the code that determines the output voltage from the DAC string. The code is transferred from the DAC-*n*-data register to the DAC latch when the internal DAC-load signal is generated.

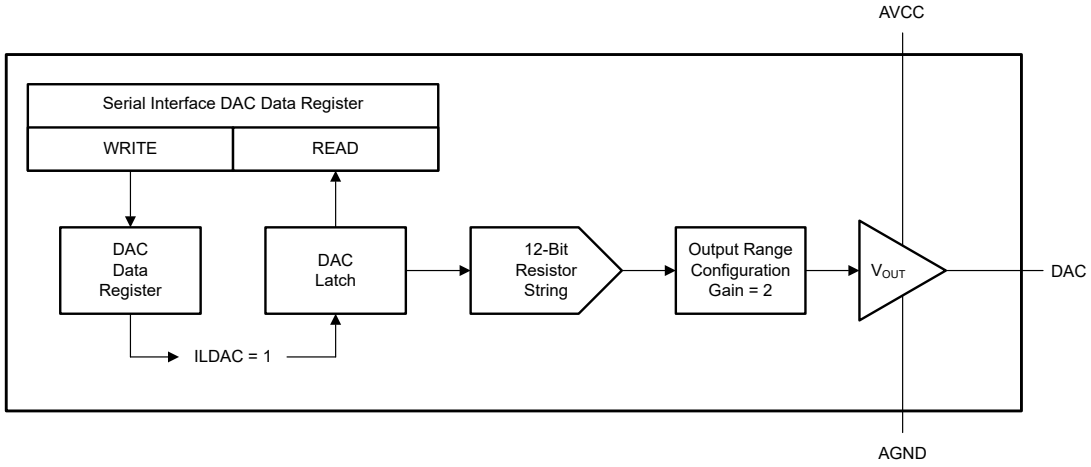


図 7-9. DAC Block Diagram

7.3.4.1 Resistor String

The resistor string structure is shown in 図 7-10. The resistor string consists of a string of resistors, each of value *R*. The code loaded to the DAC latch determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. This architecture is inherently monotonic, voltage out, and low glitch. The resistor string architecture is also linear because all the resistors are of equal value.

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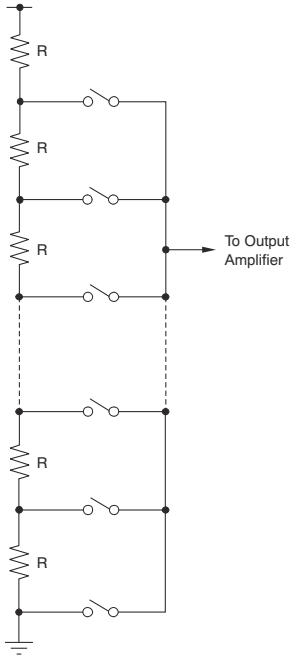


図 7-10. Resistor String

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7.3.4.2 DAC Output

The output range is set by the gain bits in the DAC gain register to 0 V to (2 × V_{REF}). The maximum output is AV_{CC}. The output buffer amplifier is capable of generating rail-to-rail voltages on the output, giving an output range of 0 V to AV_{CC}. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics.

7.3.4.2.1 Full-Scale Output Range

The full-scale output range of each DAC is set by the product of the value of the reference voltage times the gain of the DAC output buffer (V_{REF} × gain). The gain bits of the DAC gain register set the output range of each DAC-*n* to 0 V to (2 × V_{REF}). The full-scale output range of each DAC is limited by the analog power supply. The maximum output from the DAC must not be greater than AV_{CC}, and the minimum output must not be less than AGND.

7.3.4.2.2 DAC Output After Power-On Reset

After power-on, the DAC output buffer is in power-down mode. The output buffer is in a Hi-Z state and the DACx-OUT (where x = 0 to 11) output pin connects to the analog ground through an internal 10-kΩ resistor. After power-on or a hardware reset, all DAC-*n*-data registers, DAC-*n* latches, and the DAC output are set to default values (000h).

7.3.4.3 Double-Buffered DAC Data Registers

There are 12 double-buffered DAC data registers. Each DAC has an internal latch preceded by a DAC data register. Data are initially written to an individual DAC-*n*-data register and then transferred to the corresponding DAC-*n* latch. When the DAC-*n* latch is updated, the output of DAC-*n* changes to the newly set value. When the host reads the register memory map location labeled DAC-*n*-data, the value held in the DAC-*n* latch is returned (not the value held in the input DAC-*n*-data register).

7.3.4.4 Load DAC Latch

See 図 7-9 for the structure of the DAC register and DAC latch. The contents of the DAC-*n* latch determine the output level of the DAC-*n* pin. After writing to the DAC-*n*-data register, the DAC latch updates when the synchronous DAC loading signal triggers. Set the ILDAC bit in AFE configuration register 0 to trigger the loading signal.

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7.3.4.5 Synchronous Output Updating

The SLDA-*n* (synchronous load) bit of the DAC configuration register must be set to 1 to enable proper DAC output update operation.

表 7-4. DAC-*n* Output Update Summary for Manual Mode Update

SLDA-*n* BIT	WRITING TO ILDAC BIT	OPERATION
0	Don't care	Reserved for DACs not being updated.
1	1	Simultaneously update all DACs by internal trigger. Writing 1 to the ILDAC bit generates an internal load DAC trigger signal that updates the DAC-*n* latches and DAC-*n* outputs with the contents of the corresponding DAC-*n*-data register.

The value of the DAC-*n*-data register is transferred to the DAC-*n* latch only after an active DAC synchronous loading signal (ILDAC) occurs, which immediately updates the DAC-*n* output. Under synchronous loading operation, writing data into a DAC-*n*-data register changes only the value in that register, but not the content of DAC-*n* latch nor the output of DAC-*n*, until the synchronous load signal occurs.

The DAC synchronous load is triggered by writing 1 to the ILDAC bit in AFE configuration register 0. When this DAC synchronous load signal occurs, all DACs with the SLDA-*n* bit set to 1 are simultaneously updated with the value of the corresponding DAC-*n*-data register. By setting the SLDA-n bit properly, several DACs can be updated at the same time. For example, to update DAC0 and DAC1 synchronously, set bits SLDA-0 and SLDA-1 to 1 first, and then write the proper values into the DAC-0-data and DAC-1-data registers, respectively. After this presetting, set the ILDAC bit to 1 to simultaneously load DAC0 and DAC1. The outputs of DAC0 and DAC1 change at the same time.

The device updates the DAC latch only if the latch was accessed from the last time ILDAC was issued, thereby eliminating any unnecessary glitches. Any DAC channels that are not accessed are not reloaded again. When the DAC latch is updated, the corresponding output changes to the new level immediately.

注

When DACs are *cleared* by an external DAC-CLR-n or by the internal CLR bit, the DAC latch is loaded with the predefined value of the DAC-*n*-CLR-setting register and the output is set to the corresponding level immediately, regardless of the SLDA-*n* bit value. However, the DAC data register does not change.

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7.3.4.6 Clear DACs

DAC-*n* can be cleared with hardware or software, as shown in 図 7-11. When DAC-*n* goes to a *clear* state, DAC-*n* is immediately loaded with predefined code in the DAC-*n*-CLR-setting register, and the output is set to the corresponding level to shut down the external LDMOS device. However, the DAC-*n*-data register does not change. When the DAC goes back to normal operation, DAC-*n* is immediately loaded with the previous data from the DAC-*n*-data register and the output of DAC*n*-OUT is set back to the previous level to restore LDMOS to the status before shutdown, regardless of the SLDAC-*n* bit status.

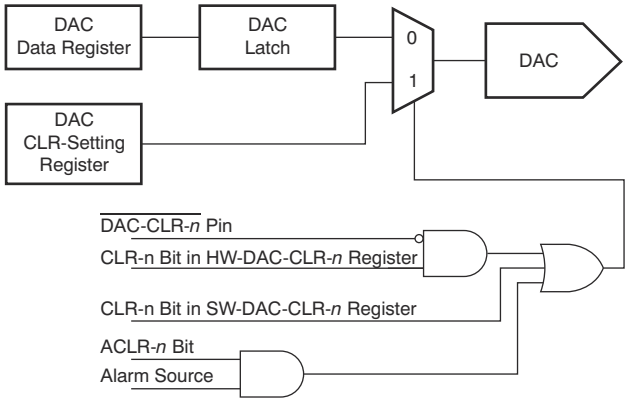


図 7-11. Clearing DAC-*n*

The device is implemented with two external control lines, the $\overline{\text{DAC-CLR-0}}$ and $\overline{\text{DAC-CLR-1}}$ pins, to clear the DACs. When either pin goes low, the corresponding user-selected DACs are in a *cleared* state. The HW_DAC-CLR-0 register determines which DAC is cleared when the $\overline{\text{DAC-CLR-0}}$ pin is low. The register contains 12 clear bits (CLR-*n*), one per DAC. If the CLR-*n* bit is 1, DAC-*n* is in a cleared state when the $\overline{\text{DAC-CLR-0}}$ pin is low. However, if the CLR-*n* bit is 0, DAC-*n* does not change when the pin is low. Likewise, the HW-DAC-CLR-1 register determines which DAC is cleared when the $\overline{\text{DAC-CLR-1}}$ pin is low.

Writing directly to the SW_DAC_CLR register puts the selected DACs in a cleared state. DACs can also be forced into a clear state by alarm events. The AUTO-DAC-CLR-SOURCE register specifies which alarm events force the DACs into a clear state, and the AUTO-DAC-CLR-EN register defines which DACs are forced into a clear state. Refer to the AUTO-DAC-CLR-SOURCE register and AUTO-DAC-CLR-EN register for further details.

7.3.4.7 DAC Output Thermal Protection

A significant amount of power can be dissipated in the DAC outputs. The device implements a thermal protection circuit that sets the THERM-ALR bit in the status register if the die temperature exceeds +150°C. The THERM-ALR bit can be used in combination with THERM-ALR-CLR (bit 2 in the AUTO-DAC-CLR-SOURCE register) and ACLR-*n* (bits[14:3] in the AUTO-DAC-CLR-EN register) to set the DAC output to a predefined code when this condition occurs. Note that this feature is disabled when the local temperature sensor powers down.

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7.3.5 Alarm Operation

The device continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range, an alarm triggers. When an alarm state occurs, the corresponding individual alarm bit in the status register is set (1). The global alarm bit (GALR) in AFE configuration register 0 is the OR of individual alarms, see 図 7-12. When the ALARM-LATCH-DIS bit in the alarm control register is cleared (0), the alarm is latched. The global alarm bit (GALR) maintains 1 until the corresponding error conditions subside and the alarm status is read. The alarm bits are referred to as being *latched* because these bits remain set until read by software. This design makes sure that out-of-limit events cannot be missed if the software is polling the device periodically. All bits are cleared when reading the status register, and all bits are reasserted if the out-of limit condition still exists on the next monitoring cycle, unless otherwise noted.

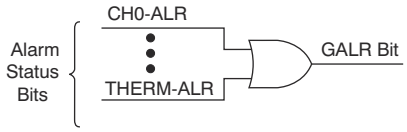


図 7-12. Global Alarm Bit

When the ALARM-LATCH-DIS bit in the alarm control register is set (1), the alarm bit is not latched. The alarm bit in the status register goes to 0 when the error condition subsides, regardless of whether the bit is read or not. When GALR is 1, the $\overline{\text{ALARM}}$ pin goes low. When the GALR bit is 0, the $\overline{\text{ALARM}}$ is high (inactive).

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7.3.5.1 Analog Input Out-of-Range Alarm

The device provides out-of-range detection for four individual analog inputs (CH0, CH1, CH2, and CH3), as shown in 図 7-13. When the measurement is out-of-range, the corresponding alarm bit in the status register is set to 1 to flag the out-of-range condition. The value in the high-threshold register defines the upper bound threshold of the *N*th analog input, while the value in the low-threshold register defines the lower bound. These two bounds specify a window for the out-of-range detection.

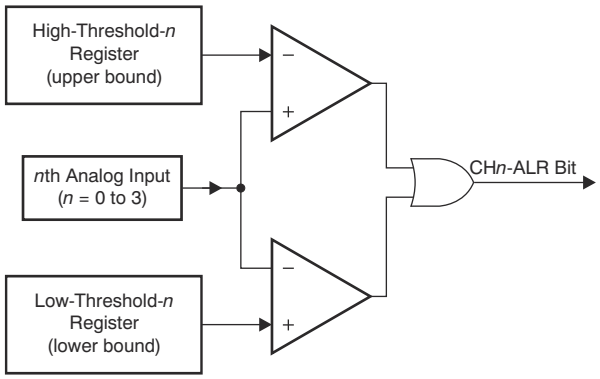


図 7-13. Ch*n* Out-of-Range Alarm

The device also has high-limit or low-limit detection for the temperature sensors (D1, D2, and LT), as shown in 図 7-14. To implement single, upper-bound threshold detection for analog input CH*n*, the host processor can set the upper-bound threshold to the desired value and the lower-bound threshold to the default value. For lower-bound threshold detection, the host processor can set the lower-bound threshold to the desired value and the upper-bound threshold to the default value. Note that the value of the high-threshold register must not be less than the value of the low-threshold register; otherwise, ALR-*n* is always set to 1 and the alarm indicator is always active. Each temperature sensor has two alarm bits: High-ALR (high-limit alarm) and Low-ALR (low-limit alarm).

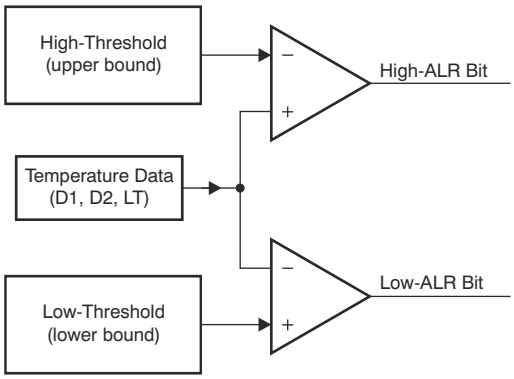


図 7-14. Temperature Out-of-Range Alarm

7.3.5.2 $\overline{\text{ALARM}}$ Pin

The $\overline{\text{ALARM}}$ pin is a global alarm indicator. $\overline{\text{ALARM}}$ is an open-drain pin, as 図 7-15 illustrates; an external pullup resistor is required. When the pin is activated, the pin goes low. When the pin is inactive, the pin is in Hi-Z status. The $\overline{\text{ALARM}}$ pin functions as an interrupt to the host so that this pin can query the status register to determine the alarm source. Any alarm event (including analog inputs, temperatures, diode status, and device thermal condition) activates the pin if the alarm is not masked (the corresponding EALR bit in the alarm control register is 1). When the alarm pin is masked (EN-ALARM bit is 0), the occurrence of the event sets the corresponding status bit in status register to 1, but does not activate the $\overline{\text{ALARM}}$ pin.

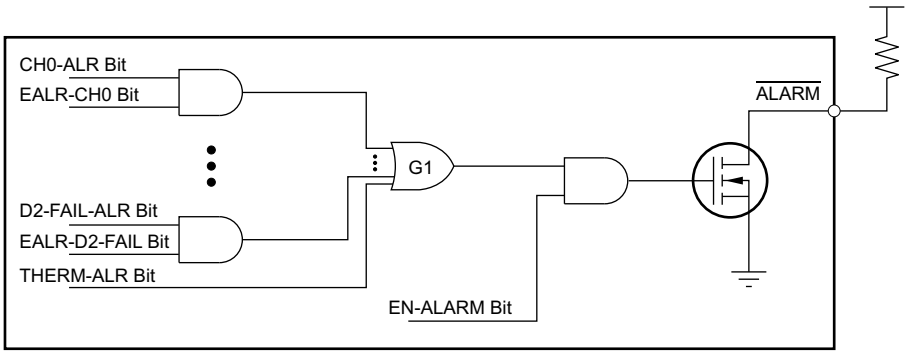


図 7-15. $\overline{\text{ALARM}}$ Pin

When the ALARM-LATCH-DIS bit in the alarm control register is cleared (0), the alarm is latched. Reading the status register clears the alarm status bit. Whenever an alarm status bit is set, indicating an alarm condition, the bit remains set until the event that caused the alarm is resolved and the status register is read. The alarm bit can only be cleared by reading the status register after the event is resolved, or by a hardware reset, software reset, or power-on reset (POR). All bits are cleared when reading the status register, and all bits are reasserted if the out-of-limit condition still exists after the next conversion cycle, unless otherwise noted. When the ALARM-LATCH-DIS bit in the alarm control register is set (1), the $\overline{\text{ALARM}}$ pin is not latched. The alarm bit clears to 0 when the error condition subsides, regardless of whether the bit is read or not.

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7.3.5.3 Hysteresis

The device continuously monitors the analog input channels and temperatures. If any alarms are out of range and the alarm is enabled, the alarm bit is set (1). However, the alarm condition is cleared only when the conversion result returns to a value of at least *hys* below the value of the high threshold register, or *hys* above the value of low threshold register. The hysteresis registers store the value for each analog input (CH0, CH1, CH2, and CH3) and temperature (D1, D2, and LT). *hys* is the value of hysteresis that is programmable: 0 LSB to 127 LSB for analog inputs, and 0°C to +31°C for temperatures. For the THERM-ALR bit, the hysteresis is fixed at 8°C. The hysteresis behavior is shown in 図 7-16.

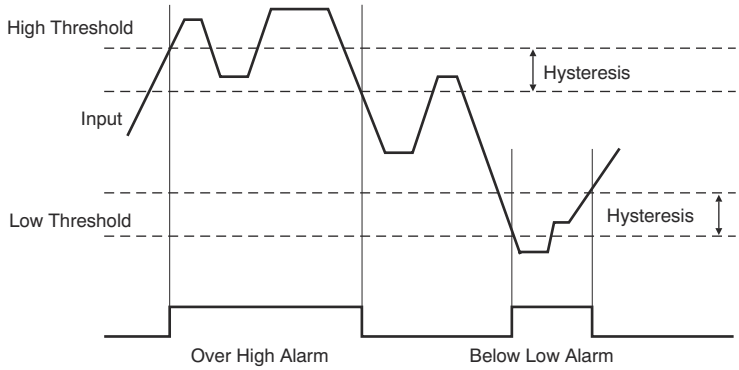


図 7-16. Hysteresis

7.3.5.4 False-Alarm Protection

As noted previously, the device continuously monitors all analog inputs and temperatures in normal operation. When any input is out of the specified range in *N* consecutive conversions, the corresponding alarm bit is set (1). If the input returns to the normal range before *N* consecutive times, the alarm bit remains clear (0). This design avoids false alarms.

The number *N* is programmable by the CH-FALR-CT-[2:0] bits in AFE configuration register 1 for analog input CHn as shown in 表 7-5, or by the TEMP-FALR-CT-[1:0] bits for temperature monitors as shown in 表 7-6.

表 7-5. Consecutive Sample Number for False Alarm Protection for Ch*n*

CH-FALR-CT-2	CH-FALR-CT-1	CH-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	0	1
0	0	1	4
0	1	0	8
0	1	1	16 (default)
1	0	0	32
1	0	1	64
1	1	0	128
1	1	1	256

表 7-6. Consecutive Sample Number for False Alarm Protection for Temperature Channels

TEMP-FALR-CT-1	TEMP-FALR-CT-0	*N* CONSECUTIVE SAMPLES BEFORE ALARM IS SET
0	0	1
0	1	2
1	0	4 (default)
1	1	8

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7.3.6 General-Purpose Input and Output Pins (GPIO-0 To GPIO-7)

The device has eight GPIO pins. The GPIO-0, GPIO-1, GPIO-2 and GPIO-3 pins are dedicated to general, bidirectional, digital I/O signals. GPIO-4, GPIO-5, GPIO-6, and GPIO-7 are dual-function pins and can be programmed as either bidirectional digital I/O pins or remote temperature sensors D1 and D2. When D1 or D2 is disabled, the pins function as GPIOs. These pins can receive an input or produce an output. When the GPIO-*n* pin functions as an output, the pin has an open-drain and the status is determined by the corresponding GPIO-*n* bit of the GPIO register. The output state is high impedance when the GPIO-*n* bit is set to 1, and is logic low when the GPIO-*n* bit is cleared (0). A 10-kΩ pullup resistor is required when using the GPIO-*n* pin as an output; see 図 7-17. Do not tie the dual-function pins GPIO-4, GPIO-5, GPIO-6, and GPIO-7 to a pullup voltage that exceeds the AV_{DD} supply. The dedicated GPIO-0, GPIO-1, GPIO-2, and GPIO-3 pins are only restricted by the absolute maximum voltage. To use the GPIO-*n* pin as an input, the corresponding GPIO-*n* bits in the GPIO register must be set to 1. When the GPIO-*n* pin functions as an input, the digital value on the pin is acquired by reading the corresponding GPIO-*n* bit. After a power-on reset or any forced hardware or software reset, all GPIO-*n* bits are set to 1, and the GPIO-*n* pin goes to a high-impedance state.

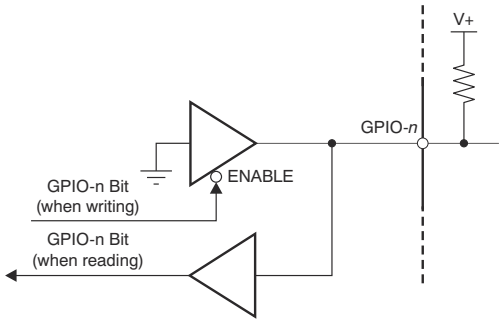


図 7-17. GPIO Pins

7.3.7 Device Reset Options

The device can be reset through a power-on reset (POR) condition as well as customer-initiated hardware and software reset events.

7.3.7.1 Hardware Reset

Pulling the $\overline{\text{RESET}}$ pin low performs a hardware reset. When the $\overline{\text{RESET}}$ pin is low, the device enters a reset state and all registers are set to default values (including the power-down register). Therefore, all function blocks (except the internal temperature sensor) are in power-down mode. On the $\overline{\text{RESET}}$ rising edge, the device returns to the normal operating mode. After returning to this mode, all registers remain set to default values until a new value is written. After reset, the power-down register must be properly written to activate the device. Only issue a hardware reset when DVDD reaches the minimum specification of 2.7 V or greater.

7.3.7.2 Software Reset

Software reset returns all register settings to default values and is performed by writing to the software reset register. In the case of I^2C communication, any value written to this register results in a reset condition. In the case of SPI communications, only writing the specific value of 6600h to this register resets the device; for details, see *セクション 7.6*. During reset, all communication is blocked. After issuing the reset, wait at least 30 µs before attempting to resume communication.

7.3.7.3 Power-On Reset (POR)

When powered on, the internal POR circuit invokes a power-on reset, which performs the equivalent function of the $\overline{\text{RESET}}$ pin. To perform a POR, DVDD must start from a level less than 750 mV.

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7.4 Device Functional Modes

The device has one output mode for the DAC channels, and two conversion modes for the ADC channels.

7.4.1 DAC Output Mode

In the AFE11612-SEP, the DAC channels can only be set to a positive voltage-output range (0 V to 5 V).

The maximum DAC output for each group cannot be greater than the corresponding AV_{CC} voltage. In all-positive DAC range mode, the AVCC1 and AVCC2 pins must be connected to a positive supply voltage; however these pins are not required to be tied to the same potential. Typically, the positive voltage at each of these pins is dictated by the desired positive-voltage output range, but this configuration is not required.

7.4.2 ADC Conversion Modes

Two types of ADC conversion modes are available: direct and auto. The conversion mode (CMODE) bit of the AFE Configuration 0 register specifies the conversion mode.

In direct mode, each analog channel within the specified group is converted a single time. After the last channel is converted, the ADC enters an idle state and waits for a new trigger.

Auto mode is a continuous operation. In auto mode, each analog channel within the specified group is converted sequentially and repeatedly.

The flow chart of the ADC conversion sequence in 図 7-18 shows the conversion process.

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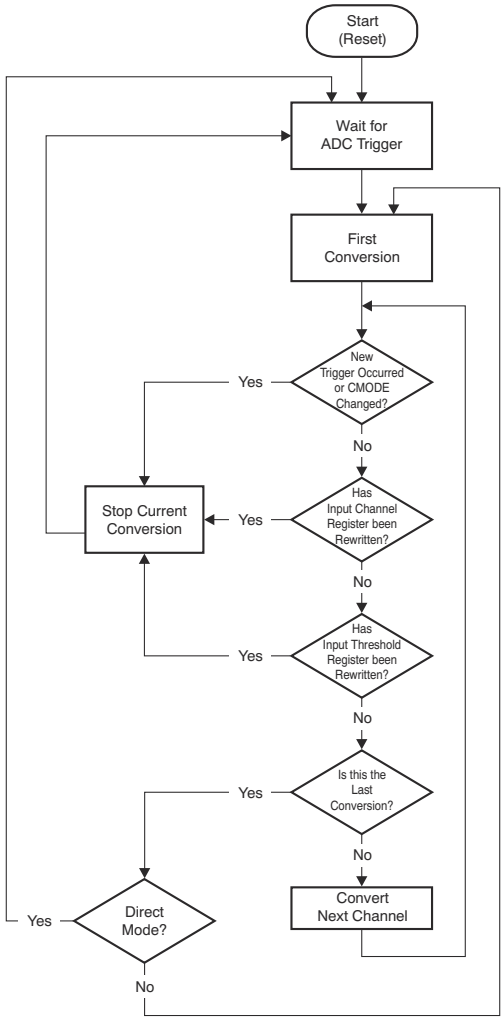


図 7-18. ADC Conversion Sequence

The current conversion cycle stops immediately if:

- A new trigger is issued
- The conversion mode changes
- Either ADC channel register is rewritten
- Any of the analog input threshold registers are rewritten

When a new external or internal trigger activates, the ADC starts a new conversion cycle. Do not issue the internal trigger at the same time the conversion mode is changed. If a 1 is simultaneously written to the ICONV bit when changing the CMODE bit to 0 or 1, the current conversion stops and immediately returns to the *wait for ADC trigger* state.

7.4.2.1 Programmable Conversion Rate

The maximum conversion rate is 500 kSPS for a single channel in auto mode, as shown in 表 7-7. The conversion rate is programmable through the CONV-RATE-[1:0] bits of the AFE configuration register 1. When more than one channel is selected, the conversion rate is divided by the number of channels selected in ADC channel register 0 and ADC channel register 1. In auto mode, the CONV-RATE-[1:0] bits determine the actual conversion rate. In direct mode, the CONV-RATE-[1:0] bits limit the maximum possible conversion rate. The actual conversion rate in direct mode is determined by the rate of the conversion trigger. Be aware that when a trigger is issued, there can be a delay of up to 4 µs to internally synchronize and initiate the start of the

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sequential channel conversion process. In both direct and auto modes, when the CONV-RATE-[1:0] bits are set to a value other than the maximum rate (00), nap mode is activated between conversions. By activating nap mode, the AI_{DD} supply current is reduced; see 図 6-42.

表 7-7. ADC Conversion Rate

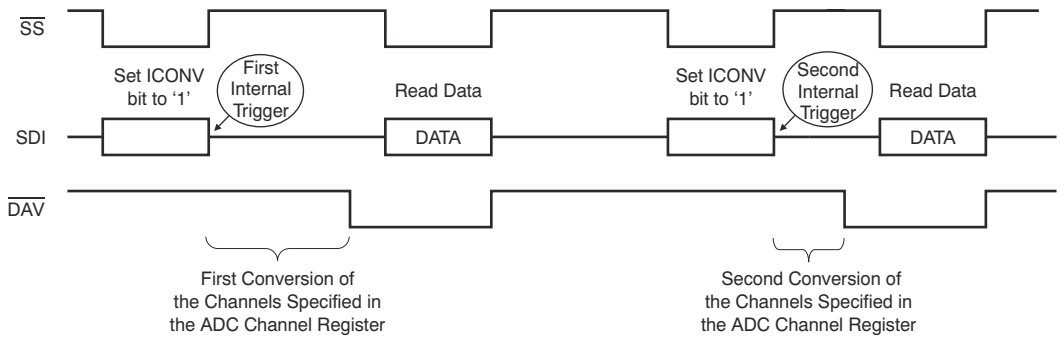
CONV-RATE-1	CONV-RATE-0	t_{ACQ} (µs)	t_{CONV} (µs)	NAP ENABLED	THROUGHPUT (Single-Channel Auto Mode)
0	0	0.375	1.625	No	500 kSPS (default)
0	1	2.375	1.625	Yes	250 kSPS
1	0	6.375	1.625	Yes	125 kSPS
1	1	14.375	1.625	Yes	62.5 kSPS

7.4.2.2 Handshaking with the Host (See AFE configuration register 0)

The DAV pin and the DAVF (data available flag) bit in AFE configuration register 0 provide handshaking with the host. Pin and bit status depend on the conversion mode (direct or auto); see 図 7-19 and 図 7-20. In direct mode, after ADC-*n*-data registers of all selected channels are updated, the DAVF bit in AFE configuration register 0 is set immediately to 1, and the DAV pin is active (low) to signify that new data are available. By reading the ADC-*n*-data register or restarting through the external $\overline{CNVT}$ pin, the ADC clears the DAVF bit to 0 and deactivates the DAV pin (high). If an internal convert start (ICONV bit) is used to start the new ADC conversion, an ADC-*n*-data register must be read after the current conversion completes before a new conversion can be started to reset the DAV status.

In auto-mode, after the ADC-*n*-data registers of the selected channels are updated, a pulse of 1 µs (low) appears on the DAV pin to signify that new data are available. However, the DAVF bit is always cleared to 0 in auto-mode.

a) Internal Trigger, Direct Mode:



b) Internal Trigger, Auto Mode:

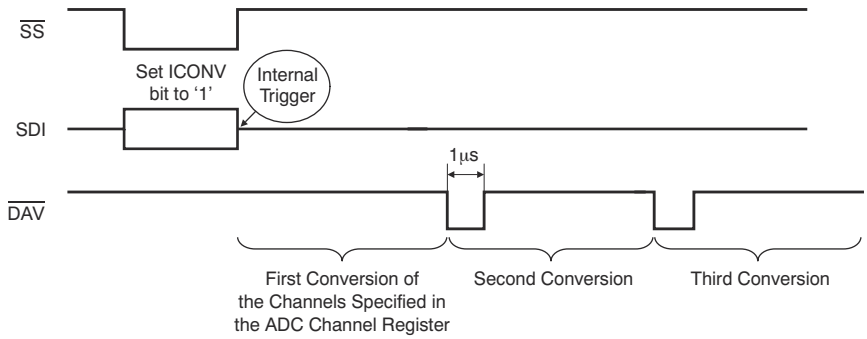
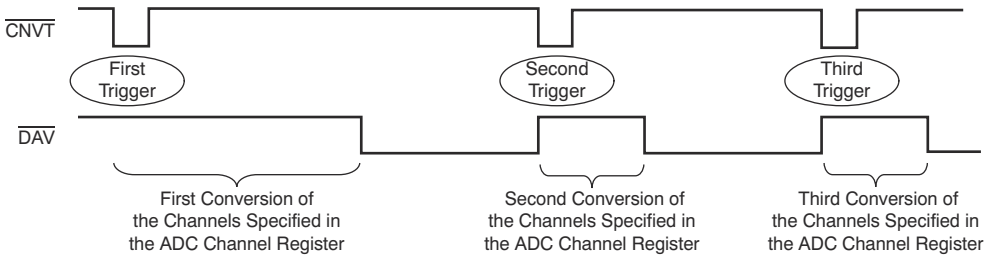


図 7-19. ADC Internal Trigger

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a) External Trigger, Direct Mode:



b) External Trigger, Auto Mode:

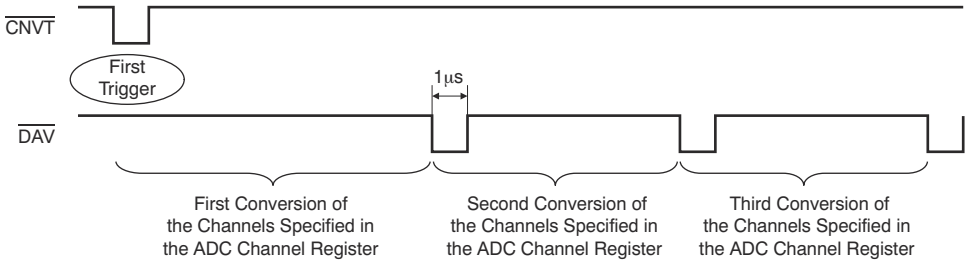


図 7-20. ADC External Trigger

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7.5 Programming

The device communicates with the system controller through the primary communication interface, which can be configured as either an I^{2}C-compatible two-wire bus or an SPI bus. When the SPI/I2C pin is tied to ground, the I^{2}C interface is enabled and the SPI is disabled. When the SPI/I2C pin is tied to IOVDD, the I^{2}C interface is disabled and the SPI is enabled.

7.5.1 I^{2}C-Compatible Interface

This device uses a two-wire serial interface compatible with the I^{2}C-bus specification, version 2.1. The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All I^{2}C-compatible devices connect to the I^{2}C bus through open-drain I/O pins SDA and SCL. A controller device, usually a microcontroller or a digital signal processor (DSP), controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the start and stop of data transfers. A target device receives and transmits data on the bus under control of the controller device. The device functions as a target and supports the following data transfer modes, as defined in the I^{2}C-bus specification: standard mode (100Kbps), fast mode (400Kbps), and high-speed mode (3.4Mbps). The data transfer protocol for standard and fast modes is exactly the same; therefore, both are referred to as F/S mode in this document. The protocol for high-speed mode is different from the F/S mode, and is referred to as Hs mode. The device supports 7-bit addressing. However 10-bit addressing and general-call addressing are not supported. The device target address is determined by the status of pins A0, A1, and A2, as shown in 表 7-8.

表 7-8. Target Addresses

A0	A1	A2	TARGET ADDRESS
GND	GND	GND	1100001
GND	GND	IOV_{DD}	0101100
GND	IOV_{DD}	GND	1100100
GND	IOV_{DD}	IOV_{DD}	0101110
IOV_{DD}	GND	GND	1100010
IOV_{DD}	GND	IOV_{DD}	0101101
IOV_{DD}	IOV_{DD}	GND	1100101
IOV_{DD}	IOV_{DD}	IOV_{DD}	0101111

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7.5.1.1 F/S-Mode Protocol

The controller initiates the data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high. All I^2C-compatible devices must recognize a start condition.

The controller then generates the SCL pulses, and transmits the 7-bit address and the read or write direction bit (R/W) on the SDA line. During all transmissions, the controller makes sure that data are valid. A valid data condition requires that the SDA line is stable during the entire high period of the clock pulse. All devices recognize the address sent by the controller and compare the address to the internal fixed addresses. Only the target device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the ninth SCL cycle. When this acknowledge is detected, the controller recognizes that a communication link is established with a target.

The controller generates further SCL cycles to either transmit data to the target (R/W bit is 1) or receive data from the target (R/W bit is 0). In either case, the receiver must acknowledge the data sent by the transmitter. Therefore, an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low-to-high while the SCL line is high. This action releases the bus and stops the communication link with the addressed target. All I^2C-compatible devices must recognize the stop condition. When a stop condition is received, all devices recognize that the bus is released and wait for a start condition followed by a matching address.

7.5.1.2 Hs-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pull-up devices.

The controller generates a start condition followed by a valid serial byte containing Hs controller code 00001xxx. This transmission is made in F/S mode at no more than 400Kbps. No device is allowed to acknowledge the Hs controller code, but all devices must recognize the Hs controller code and switch the internal setting to support 3.4Mbps operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as for F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends Hs mode and switches all internal settings of the target devices to support F/S mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in Hs mode.

7.5.1.3 Address Pointer

The device address pointer register is an 8-bit register. Each register has an address and, when accessed, the address pointer points to the register address. All the device registers are 16 bits, consisting of a high byte (D[15:8]) and a low byte (D[7:0]). The high byte is always accessed first, and the low byte accessed second. When the register is accessed, the entire register is frozen until the operation on the low byte is complete. During a write operation, the new content does not take effect until the low byte is written. In read operation, the whole register value is frozen until the low byte is read.

The address pointer does not change after the current register is accessed. To change the pointer, the controller issues a target address byte with the R/W bit low, followed by the pointer register byte; no additional data are required.

7.5.1.4 Timeout Function

The device resets the serial interface if either SCL or SDA are held low for 32.8 ms (typical) between a START and STOP condition. If the device is holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the timeout function, a communication speed of at least 1 kHz for the SCL operating frequency must be maintained.

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7.5.1.5 Device Communication Protocol For I²C

The device uses the following I²C protocols: writing a single word of data to a 16-bit register, writing multiple words to different registers, reading a single word from any register, and reading the same register multiple times. This section discusses these I²C protocols.

7.5.1.5.1 Writing A Single Register (図 7-21)

図 7-21 shows a diagram of this protocol. Steps for this protocol are:

1. The controller device asserts a start condition.
2. The controller then sends the 7-bit device target address followed by a 0 for the direction bit, indicating a write operation.
3. The device asserts an acknowledge signal on SDA.
4. The controller sends a register address.
5. The device asserts an acknowledge signal on SDA.
6. The controller sends a data byte of the high byte of the register (D[15:8]).
7. The device asserts an acknowledge signal on SDA.
8. The controller sends a data byte of the low byte of the register (D[7:0]).
9. The device asserts an acknowledge signal on SDA.
10. The controller asserts a stop condition to end the transaction.

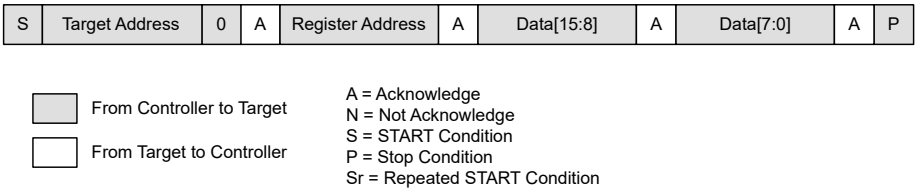


図 7-21. Write Single Register

7.5.1.5.2 Writing Multiple Registers (図 7-22)

A complete word must be written to a register (high byte and low byte) for proper operation, as shown in 図 7-22. Steps for this process are:

1. The controller device asserts a start condition.
2. The controller then sends the 7-bit device target address followed by a 0 for the direction bit, indicating a write operation.
3. The device asserts an acknowledge signal on SDA.
4. The controller sends the first register address.
5. The device asserts an acknowledge signal on SDA.
6. The controller sends the high byte of the data word to the first register.
7. The device asserts an acknowledge signal on SDA.
8. The controller sends the low byte of the data word to the first register.
9. The device asserts an acknowledge signal on SDA.
10. The controller sends a second register address.
11. The device asserts an acknowledge signal on SDA.
12. The controller then sends the high byte of the data word to the second register.
13. The device asserts an acknowledge on SDA.
14. The controller sends the low byte of the data word to the second register.
15. The device asserts an acknowledge signal on SDA.
16. The controller and the device repeat steps 4 to 15 until the last data are transferred.
17. The controller then asserts a stop condition to end the transaction.

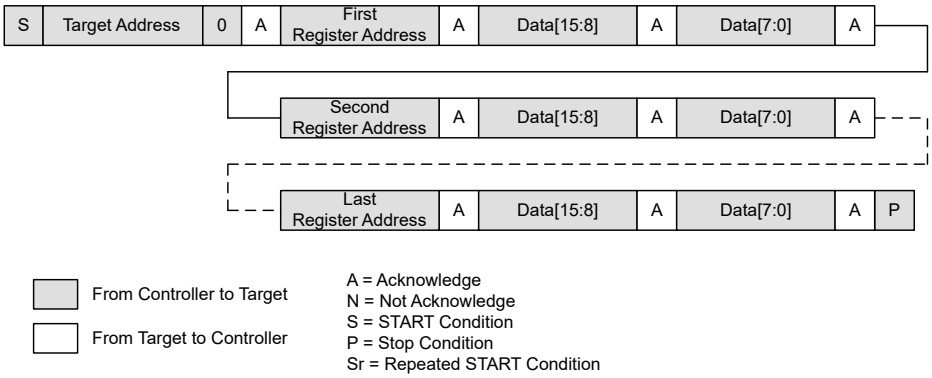


図 7-22. Write to Multiple Registers

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7.5.1.5.3 Reading a Single Register (図 7-23)

図 7-23 shows a diagram of this protocol. Steps for this protocol are:

1. The controller device asserts a start condition.
2. The controller then sends the 7-bit device target address followed by a 0 for the direction bit, indicating a write operation.
3. The device asserts an acknowledge signal on SDA.
4. The controller sends a register address.
5. The device asserts an acknowledge signal on SDA.
6. The controller device asserts a restart condition.
7. The controller then sends the 7-bit device target address followed by a 1 for the direction bit, indicating a read operation.
8. The device asserts an acknowledge signal on SDA.
9. The device then sends the high byte of the register (D[15:8]).
10. The controller asserts an acknowledge signal on SDA.
11. The device sends the low byte of the register (D[7:0]).
12. The controller asserts a not acknowledge signal on SDA.
13. The controller then asserts a stop condition to end the transaction.

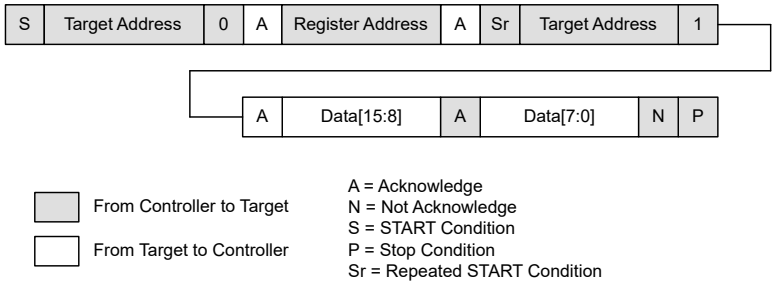


図 7-23. Read A Single Register

7.5.1.5.4 Reading Multiple Registers (図 7-24 and 図 7-25)

図 7-24 and 図 7-25 illustrate the process for this protocol. Steps for this protocol are:

1. The controller device asserts a start condition.
2. The controller then sends the 7-bit device target address followed by a 0 for the direction bit, indicating a write operation.
3. The device asserts an acknowledge signal on SDA.
4. The controller sends a register address.
5. The device asserts an acknowledge signal on SDA.
6. The controller device asserts a restart condition.
7. The controller then sends the 7-bit device target address followed by a 1 for the direction bit, indicating a read operation.
8. The device asserts an acknowledge signal on SDA.
9. The device then sends the high byte of the register (D[15:8]).
10. The controller asserts an acknowledge signal on SDA.
11. The device sends the low byte of the register (D[7:0]).
12. The controller asserts an acknowledge signal on SDA.
13. The device and the controller repeat steps 9 to 12 until the low byte of last reading is transferred.
14. After receiving the low byte of the last register, the controller asserts a not acknowledge signal on SDA.
15. The controller then asserts a stop condition to end the transaction.

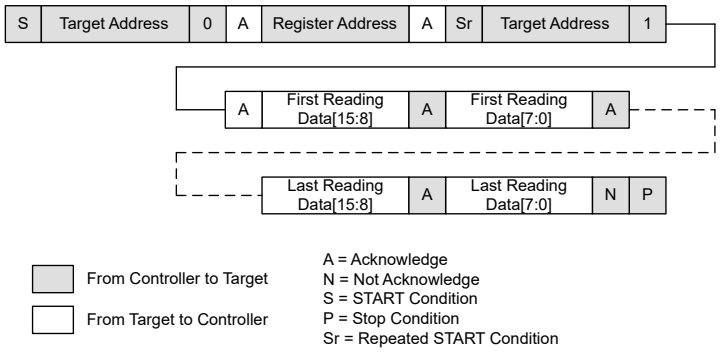


図 7-24. Read Same Register Multiple Times

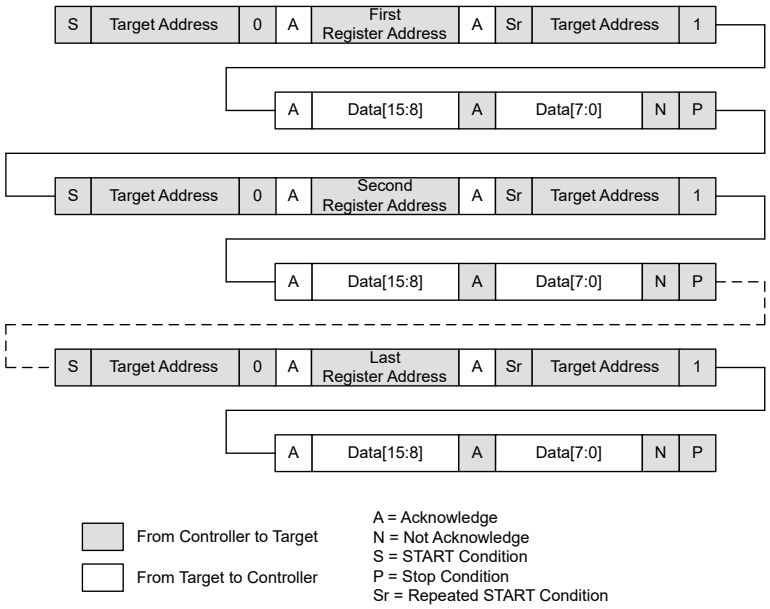


図 7-25. Read Multiple Registers Using the *Reading Single Word From Any Register* Method

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7.5.2 Serial Peripheral Interface (SPI)

The device can be controlled over a versatile three-wire serial interface that operates at clock rates of up to 20 MHz. The SPI communication command consists of a read or write (R/W) bit, seven register address bits, and 16 data bits (see 表 7-9), for a total of 24 bits.

7.5.2.1 SPI Shift Register

The SPI shift register is 24 bits wide. Data are loaded into the device MSB first as a 24-bit word under the control of the serial clock input, SCLK. The $\overline{CS}$ falling edge starts the communication cycle. Data are latched into the SPI shift register on the SCLK falling edge, while $\overline{CS}$ is low. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked out and the SDO line is in a high-impedance state. The contents of the SPI shift register are loaded into the device internal register on the $\overline{CS}$ rising edge (with delay). During the transfer, the command is decoded and new data are transferred into the proper registers.

The serial interface functions with both a continuous and non-continuous serial clock. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock to latch the data.

7.5.2.2 SPI Communications Command

The device is entirely controlled by registers. Reading from and writing to these registers is accomplished by issuing a 24-bit operation word shown in 表 7-9.

表 7-9. 24-Bit Word Structure for Read and Write Operation

OPERATION	I/O	BIT 23 (MSB)	BIT22:BIT16	BIT15:BIT0
Write	SDI	0 (R/W)	Addr[6:0]	Data to be written
	SDO	Data are undefined	Data are undefined	Undefined or data depending on the previous frame
Read frame 1	SDI	1 (R/W)	Addr[6:0]	Don't care
	SDO	Data are undefined	Data are undefined	Undefined or data depending on the previous frame
Read frame 2	SDI	1 (R/W)	Addr[6:0]	Don't care
	SDO	Data are undefined	Data are undefined	Data for address specified in frame 1

Bit 23 **R/W**. Indicates a read from or a write to the addressed register.

0 = The write operation is set and data are written to the specified register
1 = A read operation where bits Addr[6:0] select the register to be read. The remaining bits are *don't care*. Data read from the selected register appear on the SDO pin in the next SPI cycle.

Bits[22:16] **Addr6:Addr0.** Register address; specifies which register is accessed.

Bits[15:0] **DATA.** 16-bit data bits.

In a write operation, these bits are written to bits[15:0] of the register with the address of (Addr[6:0]).
In a read operation, these bits are determined by the previous operation. If the previous operation is a read, these bits are from bits[15:0] of the internal register specified in previous read operation. If the previous operation is a write, these data bits are *don't care* (undefined). Data read from the current read operation appear on SDO in the next operation cycle.

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7.5.2.3 Standalone Operation

In standalone mode, as shown in 図 7-26, each device has an SPI bus. The serial clock can be continuous or gated. The first $\overline{CS}$ falling edge starts the operation cycle. Exactly 24 falling clock edges must be applied before $\overline{CS}$ is brought high again. If $\overline{CS}$ is brought high before the 24th falling SCLK edge, or if more than 24 SCLK falling edges are applied before $\overline{CS}$ is brought high, then the input data are incorrect. The device input register is updated from the shift register on the $\overline{CS}$ rising edge, and data are automatically transferred to the addressed registers as well. For another serial transfer to occur, $\overline{CS}$ must be brought low again. 図 7-27 and 図 7-28 show write and read operations in standalone mode.

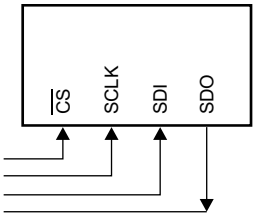
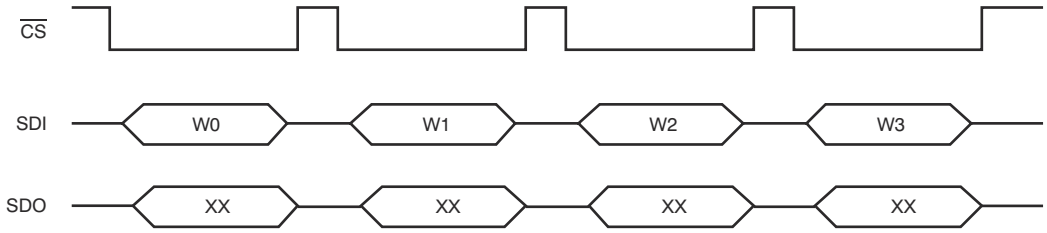
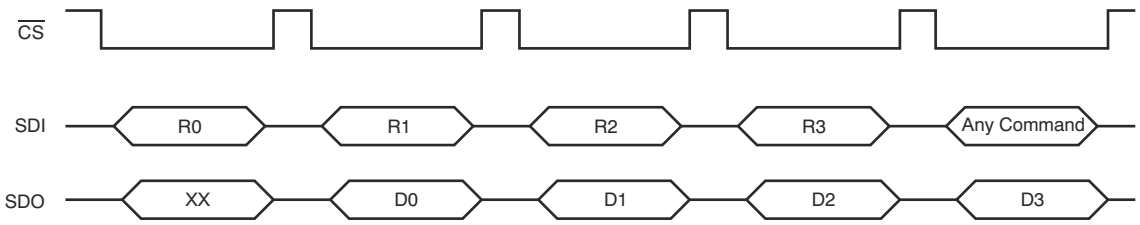


図 7-26. Standalone Operation



W*n* = Write Command for Register *N*
XX = Don't care, undefined

図 7-27. Write Operation in Standalone Mode



R*n* = Read Command for Register *N*
D*n* = Data from Register *N*
XX = Don't care, undefined

図 7-28. Read Operation in Standalone Mode

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7.5.2.4 Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy-chain multiple devices together. This daisy-chain feature is useful in reducing the number of serial interface lines. The first $\overline{CS}$ falling edge starts the operation cycle. SCLK is continuously applied to the input shift register when $\overline{CS}$ is low.

If more than 24 clock pulses are applied, data ripple out of the shift register and appear on the SDO line. These data are clocked out on the SCLK rising edge and are valid on the falling edge. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24*N*, where *N* is the total number of devices in the daisy chain. When the serial transfer to all devices is complete, $\overline{CS}$ is taken high. This action transfers data from the SPI shifter registers to the internal register of each device in the daisy-chain and prevents any further data from being clocked in. The serial clock can be continuous or gated. A continuous SCLK source can only be used if $\overline{CS}$ is held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used and $\overline{CS}$ must be taken high after the final clock in order to latch the data. 図 7-29 to 図 7-32 illustrate the daisy-chain operation.

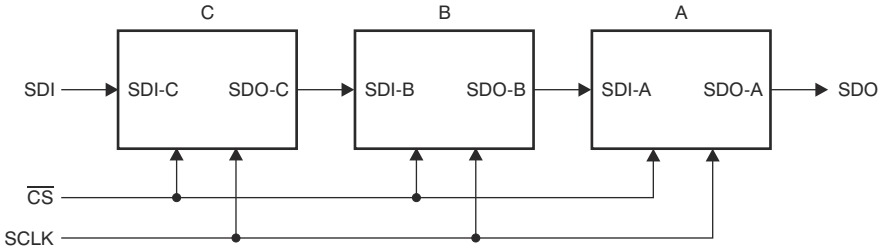
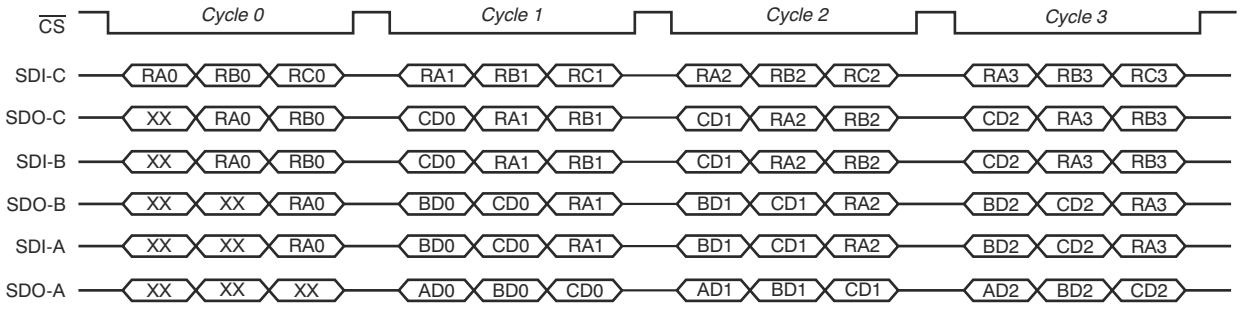


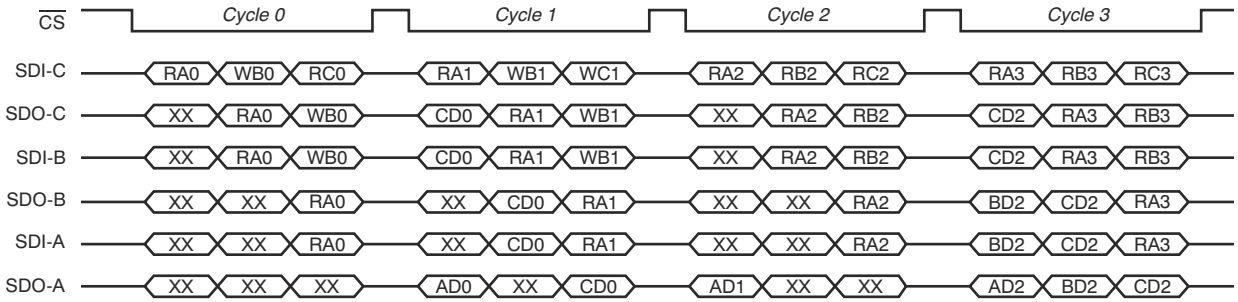
図 7-29. Three devices in a Daisy-Chain Configuration



RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B,C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

図 7-30. Reading Multiple Registers

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WB*n* (WC*n*) = Write Command for Register *N* of device A (B,C)
RA*n* (RB*n*, RC*n*) = Read Command for Register *N* of device A (B, C)
AD*n* (BD*n*, CD*n*) = Data from Register *N* of device A (B, C)
XX = Don't care, undefined

図 7-31. Mixed Operation: Reading Devices A and C, and Writing to Device B; Then Reading A, and Writing to B and C; Then Reading A, B, and C Twice

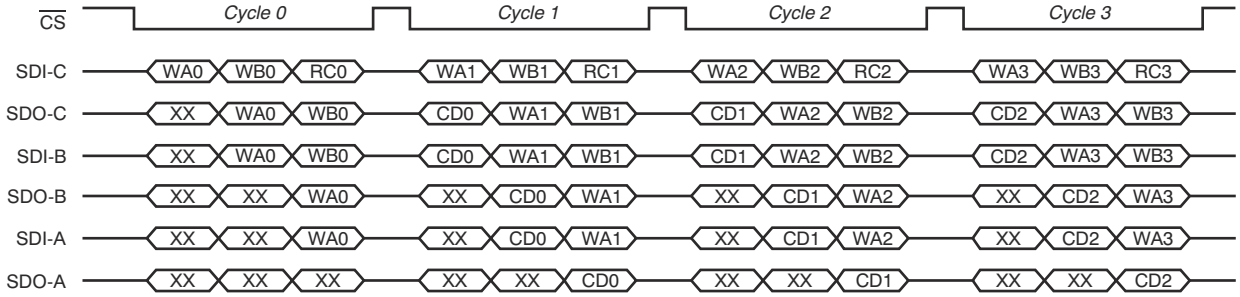


図 7-32. Writing to Devices A and B, and Reading Device C

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7.6 Register Maps

The device has several 16-bit registers that consist of a high byte (8 MSBs) and a low byte (8 LSBs). An 8-bit register pointer points to the proper register. The pointer does not change after an operation. 表 7-10 lists the registers for the device. The default values are for SPI operation; see the following subsections for I^2C default values.

表 7-10. Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	LT_ TEMP	R	0000	LT_DATA [11:0]												Reserved			
01	D1_ TEMP	R	0000	D1_DATA [11:0]												Reserved			
02	D2_ TEMP	R	0000	D2_DATA [11:0]												Reserved			
0A	TEMP_ CONFIG	R/W	003C	Reserved										D2EN	D1EN	LTEN	RC	Reserved	
0B	TEMP_ CONV_ RATE	R/W	0007	Reserved													RATE[2:0]		
21	D1_N_ ADJUST	R/W	0000	Reserved								N_ADJUST[7:0]							
22	D2_N_ ADJUST	R/W	0000	Reserved								N_ADJUST[7:0]							
23	ADC_0	R	0000	Reserved				ADC[11:0]											
24	ADC_1	R	0000	Reserved				ADC[11:0]											
25	ADC_2	R	0000	Reserved				ADC[11:0]											
26	ADC_3	R	0000	Reserved				ADC[11:0]											
27	ADC_4	R	0000	Reserved				ADC[11:0]											
28	ADC_5	R	0000	Reserved				ADC[11:0]											
29	ADC_6	R	0000	Reserved				ADC[11:0]											
2A	ADC_7	R	0000	Reserved				ADC[11:0]											
2B	ADC_8	R	0000	Reserved				ADC[11:0]											
2C	ADC_9	R	0000	Reserved				ADC[11:0]											
2D	ADC_10	R	0000	Reserved				ADC[11:0]											
2E	ADC_11	R	0000	Reserved				ADC[11:0]											
2F	ADC_12	R	0000	Reserved				ADC[11:0]											
30	ADC_13	R	0000	Reserved				ADC[11:0]											
31	ADC_14	R	0000	Reserved				ADC[11:0]											
32	ADC_15	R	0000	Reserved				ADC[11:0]											
33	DAC_0	R/W	0000	Reserved				DAC[11:0]											
34	DAC_1	R/W	0000	Reserved				DAC[11:0]											
35	DAC_2	R/W	0000	Reserved				DAC[11:0]											
36	DAC_3	R/W	0000	Reserved				DAC[11:0]											

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表 7-10. Register Map (続き)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
37	DAC_4	R/W	0000	Reserved				DAC[11:0]											
38	DAC_5	R/W	0000	Reserved				DAC[11:0]											
39	DAC_6	R/W	0000	Reserved				DAC[11:0]											
3A	DAC_7	R/W	0000	Reserved				DAC[11:0]											
3B	DAC_8	R/W	0000	Reserved				DAC[11:0]											
3C	DAC_9	R/W	0000	Reserved				DAC[11:0]											
3D	DAC_10	R/W	0000	Reserved				DAC[11:0]											
3E	DAC_11	R/W	0000	Reserved				DAC[11:0]											
3F	DAC_0_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
40	DAC_1_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
41	DAC_2_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
42	DAC_3_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
43	DAC_4_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
44	DAC_5_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
45	DAC_6_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
46	DAC_7_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
47	DAC_8_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
48	DAC_9_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
49	DAC_10_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
4A	DAC_11_CLR	R/W	0000	Reserved				DAC_CLR[11:0]											
4B	GPIO	R/W	00FF	Reserved								GPIO[7:0]							
4C	AFE_CONFIG_0	R/W	2000	Reserved		CMODE	ICONV	ILDAC	ADC_REF_INT	EN_ALARM	Reserved	DAVF	GALR	Reserved					
4D	AFE_CONFIG_1	R/W	0070	Reserved						CONV_RATE_1	CONV_RATE_0	CH_FALR_CT_2	CH_FALR_CT_1	CH_FALR_CT_0	TEMP_FALR_CT_1	TEMP_FALR_CT_0	Reserved		
4E	ALR_CTRL	R/W	0000	Reserved	EALR_CH0	EALR_CH1	EALR_CH2	EALR_CH3	EALR_LT_LOW	EALR_LT_HIGH	EALR_D1_LOW	EALR_D1_HIGH	EALR_D2_LOW	EALR_D2_HIGH	EALR_D1_FAIL	EALR_D2_FAIL	ALARM_LATCH_DIS	Reserved	
4F	STATUS	R	0000	Reserved	CH0_ALR	CH1_ALR	CH2_ALR	CH3_ALR	LT_LOW_ALR	LT_HIGH_ALR	D1_LOW_ALR	D1_HIGH_ALR	D2_LOW_ALR	D2_HIGH_ALR	D1_FAIL_ALR	D2_FAIL_ALR	THERM_ALR	Reserved	

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表 7-10. Register Map (続き)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
50	ADC_CH0	R/W	0000	Reserved	SE0	SE1	DF (CH0+, CH1-)	SE2	SE3	DF (CH2+, CH3-)	SE4	SE5	SE6	SE7	SE8	SE9	SE10	SE11	SE12
51	ADC_CH1	R/W	0000	Reserved	SE13	SE14	SE15	Reserved											
52	ADC_GAIN	R/W	FFFF	ADG0	ADG1	ADG2	ADG3	ADG4	ADG5	ADG6	ADG7	ADG8	ADG9	ADG10	ADG11	ADG12	ADG13	ADG14	ADG15
53	AUTO_DAC_CLR_SOURCE	R/W	0004	Reserved	CH0_ALR_CLR	CH1_ALR	CH2_ALR_CLR	CH3_ALR_CLR	LT_LOW_ALR_CLR	LT_HIGH_ALR_CLR	D1_LOW_ALR_CLR	D1_HIGH_ALR_CLR	D2_LOW_ALR_CLR	D2_HIGH_ALR_CLR	D1_FAIL_ALR_CLR	D2_FAIL_ALR_CLR	THERM_ALR_CLR	Reserved	
54	AUTO_DAC_CLR_EN	R/W	0000	Reserved	ACLR[11:0]												Reserved		
55	SW_DAC_CLR	R/W	0000	Reserved	ICLR[11:0]												Reserved		
56	HW_DAC_CLR_EN_0	R/W	0000	Reserved	H0CLR[11:0]												Reserved		
57	HW_DAC_CLR_EN_1	R/W	0000	Reserved	H1CLR[11:0]												Reserved		
58	DAC_CONFIG	R/W	0000	Reserved				SLDA[11:0]											
59	DAC_GAIN	R/W	0000	Reserved				DAC_GAIN[11:0]											
5A	IN_0_HIGH_THRESHOLD	R/W	0FFF	Reserved				THRH[11:0]											
5B	IN_0_LOW_THRESHOLD	R/W	0000	Reserved				THRL[11:0]											
5C	IN_1_HIGH_THRESHOLD	R/W	0FFF	Reserved				THRH[11:0]											
5D	IN_1_LOW_THRESHOLD	R/W	0000	Reserved				THRL[11:0]											
5E	IN_2_HIGH_THRESHOLD	R/W	0FFF	Reserved				THRH[11:0]											
5F	IN_2_LOW_THRESHOLD	R/W	0000	Reserved				THRL[11:0]											
60	IN_3_HIGH_THRESHOLD	R/W	0FFF	Reserved				THRH[11:0]											
61	IN_3_LOW_THRESHOLD	R/W	0000	Reserved				THRL[11:0]											
62	LT_HIGH_THRESHOLD	R/W	07FF	Reserved				THRH[11:0]											
63	LT_LOW_THRESHOLD	R/W	0800	Reserved				THRL[11:0]											

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表 7-10. Register Map (続き)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
64	D1_ HIGH_ THRESHOLD	R/W	07FF	Reserved				THRH[11:0]											
65	D1_ LOW_ THRESHOLD	R/W	0800	Reserved				THRL[11:0]											
66	D2_ HIGH_ THRESHOLD	R/W	07FF	Reserved				THRH[11:0]											
67	D2_ LOW_ THRESHOLD	R/W	0800	Reserved				THRL[11:0]											
68	HYST_0	R/W	0810	Reserved	CH0_HYS [6:0]							CH1_HYS [6:0]							Reserved
69	HYST_1	R/W	0810	Reserved	CH2_HYS [6:0]							CH3_HYS [6:0]							Reserved
6A	HYST_2	R/W	2108	Reserved	D2_ HYS_7	D2_ HYS_6	D2_ HYS_5	D2_ HYS_4	D2_ HYS_3	D1_ HYS_7	D1_ HYS_6	D1_ HYS_5	D1_ HYS_4	D1_ HYS_3	LT_ HYS_7	LT_ HYS_6	LT_ HYS_5	LT_ HYS_4	LT_ HYS_3
6B	PWR_DOWN	R/W	0000	Reserved	PADC	PREF	PDAC0	PDAC1	PDAC2	PDAC3	PDAC4	PDAC5	PDAC6	PDAC7	PDAC8	PDAC9	PDAC10	PDAC11	Reserved
6C	DEVICE_ID	R	1220	DEVICE_ID[15:0]															
7C	SW_RST	R/W	N/A	SW_RST[15:0]															

注

A few registers have different reset values when using SPI and I^2C respectively; for these registers, the table lists the SPI reset value (register descriptions contain separate I^2C reset values wherever applicable).

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7.6.1 Temperature Data Registers (Read-Only)

In 2's complement format, 0.125°C/LSB.

7.6.1.1 LT-Temperature-Data (LT_TEMP) Register (address = 00h) [reset = 0000h, 0°C]

図 7-33. LT-Temperature-Data (LT_TEMP) Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LT_DATA [11:0]												Reserved			
R-0h												R-0h			

表 7-11. LT_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	LT_DATA	R	0h	Local temperature sensor reading in 2's complement data format.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.6.1.2 D1-Temperature-Data (D1_TEMP) Register (address = 01h) [reset = 0000h, 0°C]

図 7-34. D1-Temperature-Data Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D1_DATA [11:0]												Reserved			
R-0h												R-0h			

表 7-12. D1-Temperature-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	D1_DATA	R	0h	Remote temperature sensor D1 reading in 2's complement data format.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.6.1.3 D2-Temperature-Data (D2_TEMP) Register (address = 02h) [reset = 0000h, 0°C]

Store the remote temperature sensor D2 reading in 2's complement data format.

図 7-35. D2-Temperature-Data Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D2_DATA [11:0]												Reserved			
R-0h												R-0h			

表 7-13. D2-Temperature-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	D2_DATA	R	0h	Remote temperature sensor D2 reading in 2's complement data format.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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7.6.2 Temperature Configuration (TEMP_CONFIG) Register (address = 0Ah) [reset = 003Ch or 3CFFh]

When using the SPI, the bit configuration shown in 図 7-36 must be used; default = 003Ch.

図 7-36. Temperature Configuration Register for SPI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										D2EN	D1EN	LTEN	RC	Reserved	
R/W-0h										R/W-1	R/W-1	R/W-1	R/W-1	R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When using the I^{2}C interface, the bit configuration shown in 図 7-37 must be used; default = 3CFFh.

図 7-37. Temperature Configuration Register for I^{2}C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		D2EN	D1EN	LTEN	RC	Reserved		Reserved							
R/W-0h		R/W-1	R/W-1	R/W-1	R/W-1	R/W-0h		R/W-FFh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Bit descriptions for the temperature configuration register are shown in 表 7-14.

表 7-14. Temperature Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
13 (I^{2}C), 5 (SPI)	D2EN	R/W	1	Remote temperature sensor D2 enable. 0 = D2 is disabled 1 = D2 is enabled
12 (I^{2}C), 4 (SPI)	D1EN	R/W	1	Remote temperature sensor D1 enable. 0 = D1 is disabled 1 = D1 is enabled
11 (I^{2}C), 3 (SPI)	LTEN	R/W	1	Local temperature sensor enable. 0 = LT is disabled 1 = LT is enabled
10 (I^{2}C), 2 (SPI)	RC	R/W	1	Resistance correction enable. 0 = Correction is disabled 1 = Correction is enabled

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7.6.3 Temperature Conversion Rate (TEMP_CONV_RATE) Register (address = 0Bh) [reset = 0007h or 07FFh]

When using the SPI, the bit configuration shown in 図 7-38 must be used; default = 0007h.

図 7-38. Temperature Conversion Rate Register for SPI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													RATE [2:0]		
R/W-0h													R/W-7h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When using the I^{2}C interface, the bit configuration shown in 図 7-39 must be used; default = 07FFh.

図 7-39. Temperature Conversion Rate Register for I^{2}C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved					RATE [2:0]			Reserved							
R/W-0h					R/W-7h			R/W-FFh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-15. Temperature Conversion Rate Field Descriptions

Bit	Field	Type	Reset	Description
10-8 (I^{2}C), 2-0 (SPI)	RATE	R/W	7h	Configures conversion rate for temperature data. 000: 128 × speed 001: 64 × speed 010: 32 × speed 011: 16 × speed 100: 8 × speed 101: 4 × speed 110: 2 × speed 111: base (minimum) speed

表 7-16. Temperature Monitoring Cycle Time

TEMPERATURE SENSOR STATUS	MONITORING CYCLE TIME (ms)
Local sensor is active, remote sensors are disabled or in power-down.	15
One remote sensor is active and RC is 0, local sensor and one remote sensor are disabled or in power-down.	44
One remote sensor is active and RC is 1, local sensor and one remote sensor are disabled or in power-down.	93
One remote sensor and local sensor are active and RC is 0, one remote sensor is disabled or in power-down.	59
One remote sensor and local sensor are active and RC is 1, one remote sensor is disabled or in power-down.	108
Two remote sensors are active and RC is 0, local sensor is disabled or in power-down.	88
Two remote sensors are active and RC is 1, local sensor is disabled or in power-down.	186
All sensors are active and RC is 0.	103
All sensors are active and RC is 1.	201

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7.6.4 η-Factor Correction Registers: D1_N_ADJUST and D2_N_ADJUST (address = 21h and 22h) [reset = 0000h or 00FFh]

Only the low byte is used; the high byte is ignored.

When using the SPI, the bit configuration shown in 図 7-40 must be used; default = 0000h.

図 7-40. η-Factor Correction Register for SPI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								N_{ADJUST}							
R/W-0h								R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

When using the I^2C, the bit configuration shown in 図 7-41 must be used; default = 00FFh.

図 7-41. η-Factor Correction Register for I^2C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N_{ADJUST}								Reserved							
R/W-0h								R/W-FFh							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-17. η-Factor Correction Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8 (I^2C), 7-0 (SPI)	N_{ADJUST}	R/W	0h	Configures η-Factor correction term for remote temperature data. 7Fh: η_{EFF} = 1.747977 0Ah: η_{EFF} = 1.042759 08h: η_{EFF} = 1.035616 06h: η_{EFF} = 1.028571 04h: η_{EFF} = 1.021622 02h: η_{EFF} = 1.014675 01h: η_{EFF} = 1.011371 00h: η_{EFF} = 1.008 (default) FFh: η_{EFF} = 1.004651 FEh: η_{EFF} = 1.001325 FCh: η_{EFF} = 0.994737 FAh: η_{EFF} = 0.988235 F8h: η_{EFF} = 0.981818 F6h: η_{EFF} = 0.975484 80h: η_{EFF} = 0.706542

For further details, see *セクション 7.3.2.2*.

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7.6.5 ADC-*n*-Data (ADC_*n*) Registers (addresses = 23h to 32h) [reset = 0000h]

図 7-42. ADC-*n*-Data Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				ADC [11:0]											
R-0h				R-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-18. ADC-*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	ADC	R	000h	ADC data, stored in binary format.

Four ADC data registers are available. The ADC-*n*-data registers (where n = 0 to 15) store the conversion results of the corresponding analog channel-*n*, as shown in 表 7-19.

表 7-19. ADC Data Register Definitions

INPUT CHANNEL	INPUT TYPE	CONVERSION RESULT STORED IN	FORMAT
Channel 0	Single-ended	ADC-0-data register	Straight binary
Channel 1	Single-ended	ADC-1-data register	Straight binary
Channel 2	Single-ended	ADC-2-data register	Straight binary
Channel 3	Single-ended	ADC-3-data register	Straight binary
CH0+ or CH1–	Differential	ADC-0-data register	2's complement
CH2+ or CH3–	Differential	ADC-2-data register	2's complement
Channel 4	Single-ended	ADC-4-data register	Straight binary
Channel 5	Single-ended	ADC-5-data register	Straight binary
Channel 6	Single-ended	ADC-6-data register	Straight binary
Channel 7	Single-ended	ADC-7-data register	Straight binary
Channel 8	Single-ended	ADC-8-data register	Straight binary
Channel 9	Single-ended	ADC-9-data register	Straight binary
Channel 10	Single-ended	ADC-10-data register	Straight binary
Channel 11	Single-ended	ADC-11-data register	Straight binary
Channel 12	Single-ended	ADC-12-data register	Straight binary
Channel 13	Single-ended	ADC-13-data register	Straight binary
Channel 14	Single-ended	ADC-14-data register	Straight binary
Channel 15	Single-ended	ADC-15-data register	Straight binary

7.6.6 DAC-*n*-Data (DAC_*n*) Registers (addresses = 33h to 3Eh) [reset = 0000h)

Each DAC has a DAC data register to store the data (DAC[11:0]) that are loaded into the DAC latches.

図 7-43. DAC-*n*-Data Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DAC [11:0]											
R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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表 7-20. DAC-*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	DAC	R/W	000h	DAC data, in binary format

7.6.7 DAC-*n*-CLR-Setting (DAC_*n*_CLR) Registers (addresses = 3Fh to 4Ah) [reset = 0000h]

Each DAC has a DAC-CLR-setting register to store the data to be loaded into the DAC latch when the DAC is cleared.

図 7-44. DAC-*n*-CLR-Setting Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DAC_CLR [11:0]											
R/W-0h				R/W-0h											

表 7-21. DAC-*n*-CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	DAC_CLR	R/W	000h	Stores binary data, to be loaded into the DAC latch when the DAC is cleared

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

7.6.8 GPIO Register (address = 4Bh) [reset = 00FFh]

図 7-45. GPIO Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								GPIO [7:0]							
R/W-0h								R/W-7h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-22. DAC-*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	GPIO	R/W	7h	For write operations, the GPIO pin operates as an output. Each of the *n* bits can be set to 0 or 1. 0: GPIO-*n* pin to logic low. 1: GPIO-*n* pin to high impedance. For read operations, the GPIO pin operates as an input

注

After power-on reset, or any forced hardware or software reset, the GPIO-*n* bit is set to 1 and is in a high-impedance state.

注

When D1 is enabled, GPIO-4 and GPIO-5 are ignored. When D2 is enabled, GPIO-6 and GPIO-7 are ignored.

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7.6.9 AFE Configuration Register 0 (AFE_CONFIG_0) (address = 4Ch) [reset = 2000h]

図 7-46. AFE Configuration Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		CMODE	ICONV	ILDAC	ADC-REF-INT	EN-ALARM	Reserved	DAVF	GALR	Reserved					
R-0h		R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-0	R-0h					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-23. AFE Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
13	CMODE	R/W	1	ADC conversion mode bit. This bit selects between the two operating conversion modes (direct or auto). 0: Direct mode. The analog inputs specified in the ADC channel registers are converted sequentially (see the ADC channel registers) one time. When one set of conversions are complete, the ADC is idle and waits for a new trigger. 1: Auto mode. The analog inputs specified in the AFE channel registers are converted sequentially and repeatedly (see the ADC channel registers). When one set of conversions are complete, the ADC multiplexer returns to the first channel and repeats the process. Repetitive conversions continue until the CMODE bit is cleared (0).
12	ICONV	R/W	0	Internal conversion bit. Set this bit to 1 to start the ADC conversion internally. The bit is automatically cleared (0) after the ADC conversion starts.
11	ILDAC	R/W	0	Load DAC bit. Set this bit to 1 to synchronously load the DAC data registers, which are programmed for synchronous update mode (SLDAC-*n* = 1). The device updates the DAC latch only if the ILDAC bit is set (1), thereby eliminating any unnecessary glitches. Any DAC channels that are not accessed are not reloaded. When the DAC latch is updated, the corresponding output changes to the new level immediately. This bit is cleared (0) after the DAC data register is updated.
10	ADC-REF-INT	R/W	0	ADC V_{REF} select bit. 0: The internal reference buffer is off and the external reference drives the ADC. 1: The internal buffer is on and the internal reference drives the ADC. Note that a compensation capacitor is required.
9	EN-ALARM	R/W	0	Enable $\overline{\text{ALARM}}$ pin bit. 0: The $\overline{\text{ALARM}}$ pin is disabled 1: The $\overline{\text{ALARM}}$ pin is enabled
7	DAVF	R		ADC Data available flag bit. For direct mode only. Always cleared (set to 0) in Auto mode. 0: The ADC conversion is in progress (data are not ready) or the ADC is in auto mode. 1: The ADC conversions are complete and new data are available. In direct mode, the DAVF bit sets the DAV pin. DAV goes low when DAVF is 1, and goes high when DAVF is 0. In auto mode, DAVF is always cleared to 0. However, a 1-µs pulse (active low) appears on the DAV pin when the last input specified in the ADC channel registers is converted. DAVF is cleared to 0 in one of three ways: by reading the ADC data register, by starting a new ADC conversion, or by writing 0 to this bit. Reading the status register does not clear this bit.
6	GALR	R	0	Global alarm bit. This bit is the OR function of all individual alarm bits of the status register. This bit is set (1) when any alarm condition occurs, and remains 1 until the status register is read. This bit is cleared (0) after reading the status register.

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7.6.10 AFE Configuration Register 1 (AFE_CONFIG_1) (Address = 4Dh) [reset = 0070h]

図 7-47. AFE Configuration Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CONV_RATE [1:0]		CH_FALR_CT [2:0]			TEMP_FALR_CT [1:0]		Reserved		
R-0h						R/W-0h		R/W-3h			R/W-2h		R-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-24. AFE Configuration Register 1 Field Descriptions

Bit	Field	Reset	Type	Description
9-8	CONV_RATE	0h	R/W	ADC conversion rate bit setting. 00h: 500 kSPS (default). 01h: 250 kSPS. 10h: 125 kSPS. 11h: 62.5 kSPS.
7-5	CH_FALR_CT	3h	R/W	Count of consecutive out-of-range samples to be taken before alarm is set, for CH0 through CH3. 000h: 1. 001h: 4. 010h: 8. 011h: 16 (default). 100h: 32. 101h: 64. 110h: 128. 111h: 256.
4-3	TEMP_FALR_CT	2h	R/W	Count of consecutive out-of-range samples to be taken before alarm is set, for temperature sensor. 00h: 1 (default). 01h: 2. 10h: 4. 11h: 8.

7.6.11 Alarm Control Register (ALR_CTRL) (address = 4Eh) [reset = 0000h]

図 7-48. Alarm Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	EALR_CH0	EALR_CH1	EALR_CH2	EALR_CH3	EALR_LT_LOW	EALR_LT_HIGH	EALR_D1_LOW	EALR_D1_HIGH	EALR_D2_LOW	EALR_D2_HIGH	EALR_D1_FAIL	EALR_D1_FAIL	ALARM_LATCH_DIS	Reserved	
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-25. Alarm Control Register Field Descriptions

Bit	Field	Type	Reset	Description
14	EALR_CH0	R/W	0	CH0 and (CH0+, CH1–) alarm enable bit. 0: The alarm is masked. When the input of CH0 or (CH0+, CH1–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH0_ALR bit is set. 1: The alarm is enabled, the CH0_ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH0 or (CH0+, CH1–) is out of range.
13	EALR_CH1	R/W	0	CH1 alarm enable bit. 0: The alarm is masked. When the input of CH1 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH1_ALR bit is set. 1: The alarm is enabled, the CH1_ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH1 is out of range.

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表 7-25. Alarm Control Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
12	EALR_CH2	R/W	0	CH2 and (CH2+, CH3–) alarm enable bit. 0: The alarm is masked. When the input of CH2 or (CH2+, CH3–) is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH2_ALR bit is set. 1: The alarm is enabled, the CH2_ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH2 or (CH2+, CH3–) is out of range.
11	EALR_CH3	R/W	0	CH3 alarm enable bit. 0: The alarm is masked. When the input of CH3 is out of range, the $\overline{\text{ALARM}}$ pin does not go low, but the CH3_ALR bit is set. 1: The alarm is enabled, the CH3_ALR bit is set, and the $\overline{\text{ALARM}}$ pin goes low (if enabled) when the input of CH3 is out of range.
10	EALR_LT_LOW	R/W	0	Local sensor low alarm enable bit. 0: The LT_Low alarm is masked. When LT is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT_Low_ALR bit is set. 1: The LT_Low alarm is enabled. When LT is below the specified range, the LT_Low_ALR bit is set (1) and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
9	EALR_LT_HIGH	R/W	0	Local sensor high alarm enable bit. 0: The LT-High alarm is masked. When LT is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the LT_High_ALR bit is set. 1: The LT-High alarm is enabled. When LT is above the specified range, the LT-High-ALR bit is set (1) and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
8	EALR_D1_LOW	R/W	0	D1 low alarm enable bit. 0: The D1-Low alarm is masked. When D1 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1_Low_ALR bit is set. 1: The D1-Low alarm is enabled. When D1 is below the specified range, the D1_Low_ALR bit is set (1), and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
7	EALR_D1_HIGH	R/W	0	D1 high alarm enable bit. 0: The D1-High alarm is masked. When D1 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D1_High_ALR bit is set. 1: The D1-High alarm is enabled. When D1 is above the specified range, the D1_High_ALR bit is set (1), and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
6	EALR_D2_LOW	R/W	0	D2 low alarm enable bit. 0: The D2-Low alarm is masked. When D2 is below the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2_Low_ALR bit is set. 1: The D2-Low alarm is enabled. When D2 is below the specified range, the D2_Low_ALR bit is set (1), and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
5	EALR_D2_HIGH	R/W	0	D2 high alarm enable bit. 0: The D2-High alarm is masked. When D2 is above the specified range, the $\overline{\text{ALARM}}$ pin does not go low, but the D2_High_ALR bit is set. 1: The D2-High alarm is enabled. When D2 is above the specified range, the D2_High_ALR bit is set (1), and the $\overline{\text{ALARM}}$ pin goes low (if enabled).
4	EALR_D1_FAIL	R/W	0	D1 fail alarm enable bit. 0: The D1-FAIL alarm is masked. When D1 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D1_FAIL_ALR bit is set. 1: The D1-Fail alarm is enabled. When D1 fails, the D1_FAIL_ALR bit is set (1), the $\overline{\text{ALARM}}$ pin goes low (if enabled).
3	EALR_D2_FAIL	R/W	0	D2 fail alarm enable bit. 0: The D2-FAIL alarm is masked. When D2 fails, the $\overline{\text{ALARM}}$ pin does not go low, but the D2_FAIL_ALR bit is set. 1: The D2-Fail alarm is enabled. When D2 fails, the D2_FAIL_ALR bit is set (1), the $\overline{\text{ALARM}}$ pin goes low (if enabled).
2	ALARM_LATCH_DIS	R/W	0	Alarm latch disable bit. 0: The status register bits are latched. When an alarm occurs, the corresponding alarm bit is set (1). The alarm bit remains 1 until the error condition subsides and the status register is read. Before reading, the alarm bit is not cleared (0) even if the alarm condition disappears. 1: The status register bits are not latched. When the alarm condition subsides, the alarm bits are cleared regardless of whether the status register is read or not.

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7.6.12 STATUS Register (Address = 4Fh) [reset = 0000h]

図 7-49. Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CH0_ ALR	CH1_ ALR	CH2_ ALR	CH3_ ALR	LT_ LOW_ ALR	LT_ HIGH_ ALR	D1_ LOW_ ALR	D1_ HIGH_ ALR	D2_ LOW_ ALR	D2_ HIGH_ ALR	D1_ FAIL_ ALR	D2_ FAIL_ ALR	THERM_ ALR	Reserved	
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-26. Status Register Field Descriptions

Bit	Field	Reset	Type	Description
14	CH0_ALR	0	R	0: The analog input is not out of the specified range. 1: The single-ended channel 0 or differential input pair (CH0+, CH1–) is out of the range defined by the corresponding threshold registers.
13	CH1_ALR	0	R	0: The analog input is not out of the specified range. 1: The single-ended channel 1 is out of the range defined by the corresponding threshold registers.
12	CH2_ALR	0	R	0: The analog input is not out of the specified range. 1: The single-ended channel 2 or differential input pair (CH2+, CH3–) is out of the range defined by the corresponding threshold registers.
11	CH3_ALR	0	R	0: The analog input is not out of the specified range. 1: The single-ended channel 3 is out of the range defined by the corresponding threshold registers.
10	LT_LOW_ALR	0	R	Local temperature underrange flag. 0: The local temperature is not less than the range. 1: The local temperature is less than the low-bound threshold. This bit is only checked when LT is enabled (EN-LT is 1); this bit is ignored when EN-LT is 0.
9	LT_HIGH_ALR	0	R	Local temperature overrange flag. 0: The local temperature is not greater than the range. 1: The local temperature is greater than the high-bound threshold. This bit is only checked when LT is enabled (EN-LT is 1); this bit is ignored when EN-LT is 0.
8	D1_LOW_ALR	0	R	Remote temperature reading of D1 when less than the range flag. 0: The local temperature is not less than the range. 1: The local temperature is less than the low-bound threshold. This bit is only checked when D1 is enabled (EN-D1 is 1); this bit is ignored when EN-D1 is 0.
7	D1_HIGH_ALR	0	R	Remote temperature reading of D1 when greater than the range flag. 0: The local temperature is not greater than the range. 1: The local temperature is greater than the high-bound threshold. This bit is only checked when D1 is enabled (EN-D1 is 1); this bit is ignored when EN-D1 is 0.
6	D2_LOW_ALR	0	R	Remote temperature reading of D2 when less than the range flag. 0: The local temperature is not less than the range. 1: The local temperature is less than the low-bound threshold. This bit is only checked when D2 is enabled (EN-D2 is 1); this bit is ignored when EN-D2 is 0.
5	D2_HIGH_ALR	0	R	Remote temperature reading of D2 when greater than the range flag. 0: The local temperature is not greater than the range. 1: The local temperature is greater than the high-bound threshold. This bit is only checked when D2 is enabled (EN-D2 is 1); this bit is ignored when EN-D2 is 0.
4	D1_FAIL_ALR	0	R	Remote sensor D1 failure flag. 0: The sensor is in a normal condition. 1: The sensor is an open-circuit or short-circuit. This bit is only checked when D1 is enabled (EN-D1 is 1); this bit is ignored when EN-D1 is 0.
3	D2_FAIL_ALR	0	R	Remote sensor D2 failure flag. 0: The sensor is in a normal condition. 1: The sensor is an open-circuit or short-circuit. This bit is only checked when D2 is enabled (EN-D2 is 1); this is ignored when EN-D2 is 0.
2	THERM_ALR	0	R	Thermal alarm flag. When the die temperature is equal to or greater than +150°C, the bit is set (1) and the THERM-ALR flag activates. The on-chip temperature sensor (LT) monitors the die temperature. If LT is disabled, the THERM-ALR bit is always 0. The hysteresis of this alarm is 8°C.

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7.6.13 ADC Channel Register 0 (ADC_CH0) (address = 50h) [reset = 0000h]

図 7-50. ADC Channel Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SE0	SE1	DF (CH0+, CH1–)	SE2	SE3	DF (CH2+, CH3–)	SE4	SE5	SE6	SE7	SE8	SE9	SE10	SE11	SE12
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

These bits specify the external analog auxiliary input channels (CH0 to CH12) to be converted. The specified channels are accessed sequentially in order from bit 14 to bit 0. The input is converted when the corresponding bit is set (1).

表 7-27. ADC Channel Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
14, 13, 11, 10, 8-0	SE0 to SE12	R/W	0	External single-ended analog input for CH*n*. The result is stored in ADC-*n*-data register in straight binary format.
12	DF (CH0+, CH1–)	R/W	0	External analog differential input pair, CH0 and CH1, with CH0 as positive and CH1 as negative. The difference of (CH0 – CH1) is converted and the result is stored in the ADC-0-data register in 2's complement format.
9	DF (CH2+, CH3–)	R/W	0	External analog differential input pair, CH2 and CH3, with CH2 as positive and CH3 as negative. The difference of (CH2 – CH3) is converted and the result is stored in the ADC-2-data register in 2's complement format.

表 7-28. CH0 and CH1 Bit Settings

BIT 14	BIT 13	BIT 12	DESCRIPTION
1	1	0	CH0 and CH1 are both accessed as single-ended inputs. Bit 12 is ignored.
1	0	0	CH0 is accessed as a single-ended input. CH1 is not accessed. Bit 12 is ignored.
0	1	0	CH1 is accessed as a singled-ended. CH0 is not accessed. Bit 12 is ignored.
0	0	1	Differential input pair CH0 + and CH1– is accessed as a differential input.
0	0	0	CH0, CH1, and differential pair CH0+, CH1– are not accessed.

表 7-29. CH2 and CH3 Bit Settings

BIT 11	BIT 10	BIT 9	DESCRIPTION
1	1	0	CH2 and CH3 are both accessed as single-ended inputs. Bit 9 is ignored.
1	0	0	CH2 is accessed as a single-ended input. CH3 is not accessed. Bit 9 is ignored.
0	1	0	CH3 is accessed as a singled-end input. CH2 is not accessed. Bit 9 is ignored.
0	0	1	Differential input pair CH2+ and CH3– is accessed as a differential input.
0	0	0	CH2, CH3, and differential pair CH2+, CH3– are not accessed.

表 7-30. CH4 to CH12 Bit Settings

BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DESCRIPTION
1	—	—	—	—	—	—	—	—	CH4 is accessed as a single-ended input
—	1	—	—	—	—	—	—	—	CH5 is accessed as a single-ended input
—	—	1	—	—	—	—	—	—	CH6 is accessed as a single-ended input
—	—	—	1	—	—	—	—	—	CH7 is accessed as a single-ended input
—	—	—	—	1	—	—	—	—	CH8 is accessed as a single-ended input
—	—	—	—	—	1	—	—	—	CH9 is accessed as a single-ended input
—	—	—	—	—	—	1	—	—	CH10 is accessed as a single-ended input
—	—	—	—	—	—	—	1	—	CH11 is accessed as a single-ended input
—	—	—	—	—	—	—	—	1	CH12 is accessed as a single-ended input

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7.6.14 ADC Channel Register 1 (ADC_CH1) (address = 51h) [reset = 0000h]

図 7-51. ADC Channel Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	SE13	SE14	SE15	Reserved											
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The specified channel is accessed sequentially in the order from bit 14 to bit 0 of ADC channel register 0, and then bit 14 to bit 12 of ADC channel register 1. The input is converted when the corresponding bit is set (1).

表 7-31. ADC Channel Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
14-12	SE13 to SE15	R/W	0	These bits specify the external analog auxiliary input channels (CH13, CH14, and CH15) to be converted. The input is converted when the corresponding bit is set (1). The result is stored in the ADC-*n*-data register in straight binary format.

7.6.15 ADC Gain Register (ADC_GAIN) (address = 52h) [reset = FFFFh]

図 7-52. ADC Gain Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADG 0	ADG 1	ADG 2	ADG 3	ADG 4	ADG 5	ADG 6	ADG 7	ADG 8	ADG 9	ADG 10	ADG 11	ADG 12	ADG 13	ADG 14	ADG 15
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-32. ADC Gain Register Field Descriptions

Bit	Field	Type	Reset	Description
15	ADG0	R/W	1	0: The analog input range of single-ended input CH0 (SE0) is 0 V to V_{REF} or differential input pair DF (CH0+, CH1–) is $–V_{REF}$ to $+V_{REF}$ 1: The analog input range of single-ended input CH0 (SE0) is 0 V to ($2 \times V_{REF}$) or differential input pair DF (CH0+, CH1–) is ($–2 \times V_{REF}$) to ($+2 \times V_{REF}$)
14	ADG1	R/W	1	0: The analog input range of single-ended input CH1 (SE1) is 0 V to V_{REF} 1: The analog input range is 0 V to ($2 \times V_{REF}$)
13	ADG2	R/W	1	0: The analog input range of single-ended input CH2 (SE2) is 0 V to V_{REF} or differential input pair DF (CH2+, CH3–) is $–V_{REF}$ to $+V_{REF}$ 1: The analog input range of single-ended input CH2 (SE2) is 0 V to ($2 \times V_{REF}$) or differential input pair DF (CH2+, CH3–) is ($–2 \times V_{REF}$) to ($+2 \times V_{REF}$)
12	ADG3	R/W	1	0: The analog input range of single-end input CH3 (SE3) is 0 V to V_{REF} 1: The analog input range is 0 V to ($2 \times V_{REF}$)
11-0	ADG4 to ADG15	R/W	1	0: The analog input range of CH*n* (where n = 4 to 15) is 0 V to V_{REF} 1: The analog input range is 0 V to ($2 \times V_{REF}$)

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7.6.16 AUTO_DAC_CLR_SOURCE Register (address = 53h) [reset = 0004h]

This register selects which alarm forces the DAC into a *clear* state, regardless of which DAC operation mode is active, auto, or manual.

図 7-53. AUTO_DAC_CLR_SOURCE Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CH0_ ALR_ CLR	CH1_ ALR_ CLR	CH2_ ALR_ CLR	CH3_ ALR_ CLR	LT_ LOW_ ALR_ CLR	LT_ HIGH_ ALR_ CLR	D1_ LOW_ ALR_ CLR	D1_ HIGH_ ALR_ CLR	D2_ LOW_ ALR_ CLR	D2_ HIGH_ ALR_ CLR	D1_ FAIL_ CLR	D2_ FAIL_ CLR	THERM_ ALR_ CLR	Reserved	
R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-33. AUTO_DAC_CLR_SOURCE Register

Bit	Field	Type	Reset	Description
14	CH0_ALR_CLR	R/W	0	CH0 alarm clear bit. 0: CH1_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the CH0_ALR bit in the status register are set (1)
13	CH1_ALR_CLR	R/W	0	CH1 alarm clear bit. 0: CH1_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the CH1_ALR bit in the status register are set (1)
12	CH2_ALR_CLR	R/W	0	CH2 alarm clear bit. 0: CH2_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the CH2_ALR bit in the status register are set (1)
11	CH3_ALR_CLR	R/W	0	CH3 alarm clear bit. 0: CH3_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the CH3_ALR bit in the status register are set (1)
10	LT_LOW_ALR_ CLR	R/W	0	Local temperature sensor low alarm clear bit. 0: LT_LOW_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the LT_LOW_ALR bit in the status register are set (1)
9	LT_HIGH_ALR_ CLR	R/W	0	Local temperature sensor high alarm clear bit. 0: LT_HIGH_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the LT_HIGH_ALR bit in the status register are set (1)
8	D1_LOW_ALR_ CLR	R/W	0	Remote temperature sensor D1 low alarm clear bit. 0: D1_LOW_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D1_LOW_ALR bit in the status register are set (1)
7	D1_HIGH_ALR_ CLR	R/W	0	Remote temperature sensor D1 high alarm clear bit. 0: D1_High_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D1_High_ALR bit in the status register are set (1)
6	D2_LOW_ALR_ CLR	R/W	0	Remote temperature sensor D2 low alarm clear bit. 0: D2_LOW_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D2_LOW_ALR bit in the status register are set (1)
5	D2_HIGH_ALR_ CLR	R/W	0	Remote temperature sensor D2 high alarm clear bit. 0: D2_HIGH_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D2_HIGH_ALR bit in the status register are set (1)
4	D1_FAIL_CLR	R/W	0	D1 fail alarm clear bit. 0: D1_FAIL_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D2_FAIL_ALR bit in the status register are set (1)

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表 7-33. AUTO_DAC_CLR_SOURCE Register (続き)

Bit	Field	Type	Reset	Description
3	D2_FAIL_CLR	R/W	0	D2 fail alarm clear bit. 0: D2_FAIL_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the D2_FAIL_ALR bit in the status register are set (1)
2	THERM_ALR_CLR	R/W	1	Thermal alarm clear bit. 0: THERM_ALR goes to 1 and does not force any DAC to a clear status 1: DAC*n* is forced to a clear status if both the ACLR*n* bit in the AUTO_DAC_CLR_EN register and the THERM_ALR bit in the status register are set (1)

7.6.17 AUTO_DAC_CLR_EN Register (address = 54h) [reset = 0000h]

図 7-54. AUTO_DAC_CLR_EN Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ACLR [11:0]												Reserved		
R/W-0	R/W-0h												R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-34. AUTO_DAC_CLR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
14-3	ACLR	R/W	0	Auto clear DAC-*n* enable bit. 0: DAC-*n* is not forced to a clear state when the alarm occurs (default) 1: DAC-*n* is forced to a clear state when the alarm occurs

注

ACLR*n* is always ignored when an alarm occurs for a temperature greater than +150°C (THERM-ALR is 1). If an alarm activates for a temperature greater than +150°C, and if the THERM-ALR-CLR bit in the AUTO-DAC-CLR-SOURCE register is set (1), all DACs are forced into a clear status. However, if THERM-ALR-CLR is cleared (0), the over +150°C alarm does not force any DAC to a clear status.

7.6.18 SW_DAC_CLR Register (address = 55h) [reset = 0000h]

This register uses software to force the DAC into a clear state.

図 7-55. SW_DAC_CLR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	ICLR [11:0]												Reserved		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-35. SW_DAC_CLR Register Field Descriptions

Bit	Field	Type	Reset	Description
14-3	ICLR	R/W	0	Software clear DAC*n* bit. 0: DAC*n* is restored to normal operation 1: DAC*n* is forced into a clear state

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7.6.19 HW_DAC_CLR_EN_0 Register (address = 56h) [reset = 0000h]

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low.

図 7-56. HW_DAC_CLR_EN_0 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	H0CLR [11:0]												Reserved		
R/W-0	R/W-0												R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-36. HW_DAC_CLR_EN_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
14-3	H0CLR	R/W	0	Hardware clear DAC-*n* enable 0 bit. If.H0CLR*n* = 1, DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-0}}$ pin goes low. If H0CLR*n* = 0, pulling the $\overline{\text{DAC-CLR-0}}$ pin low does not effect the state of DAC-*n*.

7.6.20 HW_DAC_CLR_EN_1 Register (address = 57h) [reset = 0000h]

This register determines which DAC is in a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low.

図 7-57. HW_DAC_CLR_EN_1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	H1CLR												Reserved		
R/W-0	R/W-0h												R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-37. HW_DAC_CLR_EN_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
14-3	H1CLR	R/W	0h	Hardware clear DAC-*n* enable 1 bit. If H1CLR*n* = 0, pulling the $\overline{\text{DAC-CLR-1}}$ pin low does not effect the state of DAC-*n* If H1CLR*n* = 1, DAC-*n* is forced into a clear state when the $\overline{\text{DAC-CLR-1}}$ pin goes low

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7.6.21 DAC Configuration (DAC_CONFIG) Register (address = 58h) [reset = 0000h]

図 7-58. DAC Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SLDA [11:0]											
R/W-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-38. DAC Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	SLDA	R/W	0h	DAC synchronous load enable bit. 0: Reserved for DACs not being updated. The synchronous load DAC signal (ILDAC) does not affect DAC*n*. The default value of SLDA-*n* is 0. 1: Synchronous load must be enabled for proper DAC operation. When internal load DAC signal ILDAC occurs, the DAC-*n* latch is loaded with the value of the corresponding DAC*n*-data register, and the output of DAC-*n* updates immediately. The internal load DAC signal ILDAC is generated by writing a 1 to the ILDAC bit in the AFE configuration register. A write command to the DAC-*n*-data register updates that register only, and does not change the DAC-*n* output. Any DAC channels that are not accessed are not reloaded.

注

The DACs can be forced to a clear state immediately by the external $\overline{\text{DAC-CLR-n}}$ signal, by alarm events, and by writing to the SW-DAC-CLR register. In these cases, the SLDA-*n* bit is ignored.

7.6.22 DAC Gain (DAC_GAIN) Register (address = 59h) [reset = 0000h]

The DAC*n* GAIN bits specify the output range of DAC*n*.

図 7-59. DAC Gain Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				DAC_GAIN											
R-0h				R-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-39. DAC Gain Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	DAC_GAIN	R	0h	DAC*n* gain bits. In this device, gain is fixed at 2 and the output is always 0 V to 2 × V_{REF}

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7.6.23 Analog Input Channel Threshold Registers (addresses = 5Ah To 61h)

Four analog auxiliary inputs (CH0, CH1, CH2, and CH3) and three temperature sensors (LT, D1, and D2; see セクション 7.6.24) implement an out-of-range alarm function. Threshold-High-*n* and Threshold-Low-*n* (where n = 0, 1, 2, 3) define the upper bound and lower bound of the *n*th analog input range, as shown in 表 7-40. This window determines whether the *n*th input is out-of-range. When the input is outside the window, the corresponding CH-ALR-*n* bit in the status register is set to 1.

For normal operation, the value of Threshold-High-*n* must be greater than the value of Threshold-Low-*n*; otherwise, CH-ALR-*n* is always set to 1 and an alarm is always indicated. When the analog channel is accessed as single-ended input, the analog-channel threshold is in a straight binary format. However, when the channel is accessed as a differential pair, the threshold is in 2's complement format.

表 7-40. Threshold Coding

INPUT CHANNEL	INPUT TYPE	THRESHOLD STORED IN	FORMAT
Channel 0	Single-ended	Input-0-Threshold-High-Byte Input-0-Threshold-Low-Byte	Straight binary
Channel 1	Single-ended	Input-1-Threshold-High-Byte Input-1-Threshold-Low-Byte	Straight binary
Channel 2	Single-ended	Input-2-Threshold-High-Byte Input-2-Threshold-Low-Byte	Straight binary
Channel 3	Single-ended	Input-3-Threshold-High-Byte Input-3-Threshold-Low-Byte	Straight binary
CH0+, CH1–	Differential	Input-0-Threshold-High-Byte Input-0-Threshold-Low-Byte	2's complement
CH2+, CH3–	Differential	Input-2-Threshold-High-Byte Input-2-Threshold-Low-Byte	2's complement

7.6.23.1 Input-n-High-Threshold Register (where n = 0, 1, 2, 3; addresses: 0 = 5Ah, 1 = 5Ch, 2 = 5Eh, 3 = 60h) [reset = 0FFFh]

図 7-60. Input-*n*-High-Threshold Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRH [11:0]											
R-0h				R/W-FFFh											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-41. Input-*n*-High-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRH	R/W	FFFh	Data bits of the upper-bound threshold of the *n*th analog input.

7.6.23.2 Input-n-Low-Threshold Register (where n = 0, 1, 2, 3; addresses: 0 = 5Bh, 1 = 5Dh, 2 = 5Fh, 3 = 61h) (reset = 0000h)

図 7-61. Input-*n*-Low-Threshold Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRL [11:0]											
R-0h				R/W-0h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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表 7-42. Input-*n*-Low-Threshold Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRH	R/W	0h	Data bits of the lower-bound threshold of the *n*th analog input.

7.6.24 Temperature Threshold Registers

7.6.24.1 LT_HIGH_THRESHOLD Register (address = 62h) [reset = 07FFh, +255.875°C]

図 7-62. LT_HIGH_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRH											
R-0h				R/W-7FFh											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-43. LT_HIGH_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRH	R/W	7FFh	Data bits of the upper-bound threshold for the local temperature sensor.

7.6.24.2 LT_LOW_THRESHOLD Register (address = 63h) [reset = 0800h, –256°C]

図 7-63. LT_LOW_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRL											
R-0h				R/W-800h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-44. LT_LOW_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRL	R/W	800h	Data bits of the lower-bound threshold for the local temperature sensor.

7.6.24.3 D1_HIGH_THRESHOLD Register (address = 64h) [reset = 07FFh, +255.875°C]

図 7-64. D1_HIGH_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRH											
R-0h				R/W-7FFh											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-45. D1_HIGH_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRH	R/W	7FFh	Data bits of the upper-bound threshold for the remote temperature sensor (D1).

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7.6.24.4 D1_LOW_THRESHOLD Register (address = 65h) [reset = 0800h, –256°C]

図 7-65. D1_LOW_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRL											
R-0h				R/W-800h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-46. D1_LOW_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRL	R/W	800h	Data bits of the lower-bound threshold for the remote temperature sensor (D1).

7.6.24.5 D2_HIGH_THRESHOLD Register (address = 66h) [reset = 07FFh, +255.875°C]

図 7-66. D2_HIGH_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRH											
R-0h				R/W-7FFh											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-47. D2_HIGH_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRH	R/W	7FFh	Data bits of the upper-bound threshold for the remote temperature sensor (D1).

7.6.24.6 D2_LOW_THRESHOLD Register (address = 67h) [reset = 0800h, –256°C]

図 7-67. D2_LOW_THRESHOLD Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				THRL											
R-0h				R/W-800h											

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-48. D2_LOW_THRESHOLD Register Field Descriptions

Bit	Field	Type	Reset	Description
11-0	THRL	R/W	800h	Data bits of the lower-bound threshold for the remote temperature sensor (D2).

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7.6.25 Hysteresis Registers

The hysteresis registers define the hysteresis in the alarm detection of an individual alarm.

7.6.25.1 Hysteresis Register 0 (HYST_0) (address = 68h) [reset = 0810h, 8 LSB]

This register contains the hysteresis values for CH0 and CH1.

図 7-68. Hysteresis Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CH0_HYS [6:0]							CH1_HYS [6:0]							Reserved
R/W-0	R/W-8h							R/W-8h							R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-49. Hysteresis Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
14-8	CH0_HYS	R/W	08h	Hysteresis of CH0, 1 LSB per step.
7-1	CH1_HYS	R/W	08h	Hysteresis of CH1, 1 LSB per step.

7.6.25.2 Hysteresis Register 1 (HYST_1) (address = 69h) [reset = 0810h, 8 LSB]

This register contains the hysteresis values for CH2 and CH3.

図 7-69. Hysteresis Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	CH2_HYS [6:0]							CH3_HYS [6:0]							Reserved
R/W-0	R/W-8h							R/W-8h							R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-50. Hysteresis Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
14-8	CH2_HYS	R/W	08h	Hysteresis of CH0, 1 LSB per step.
7-1	CH3_HYS	R/W	08h	Hysteresis of CH1, 1 LSB per step.

7.6.25.3 Hysteresis Register 2 (HYST_2) (address = 6Ah) [reset = 2108h, 8°C]

This register contains the hysteresis values for D2, D1, and LT. The range is 0°C to +31°C.

図 7-70. Hysteresis Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	D2_ HYS_7	D2_ HYS_6	D2_ HYS_5	D2_ HYS_4	D2_ HYS_3	D1_ HYS_7	D1_ HYS_6	D1_ HYS_5	D1_ HYS_4	D1_ HYS_3	LT_ HYS_7	LT_ HYS_6	LT_ HYS_5	LT_ HYS_4	LT_ HYS_3
R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-51. Hysteresis Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
14-10	D2-HYS_7 to D2_HYS_3	R/W	01000	Hysteresis of D2, 1°C per step. Note that bits D2_HYS_*n* [2:0] are always 0.
9-5	D1_HYS_7 to D1_HYS_3	R/W	01000	Hysteresis of D1, 1°C per step. Note that bits D1_HYS_*n* [2:0] are always 0.
4-0	LT_HYS_7 to LT_HYS_3	R/W	01000	Hysteresis of LT, 1°C per step. Note that bits LT_HYS_*n* [2:0] are always 0.

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7.6.26 Power-Down Register (PWR_DOWN) (address = 6Bh) [reset = 0000h)

図 7-71. Power-Down Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved	PADC	PREF	PDAC0	PDAC1	PDAC2	PDAC3	PDAC4	PDAC5	PDAC6	PDAC7	PDAC8	PDAC9	PDAC10	PDAC11	Reserved
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-52. Power-Down Register Field Descriptions

Bit	Field	Type	Reset	Description
14	PADC	RW	0	Power-down mode control bit. 0: The ADC is inactive in low-power mode. 1: The ADC is in normal operating mode.
13	PREF	R/W	0	Internal reference in power-down mode control bit. 0: The reference buffer amplifier is inactive in low-power mode. 1: The reference buffer amplifier is powered on.
12-1	PDAC0 to PDAC11	R/W	0	DAC*n* power-down control bit. 0: DAC*n* is inactive in low-power mode and the output buffer amplifier is in a Hi-Z state. The output pin of DAC*n* is internally switched from the buffer output to the analog ground through an internal resistor. 1: DAC*n* is in normal operating mode.

7.6.27 Device ID Register (DEVICE_ID) (read only address = 6Ch) [reset = 1220h]

Model and revision information.

図 7-72. Device ID Data Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEVICE_ID [15:0]															
R-1220h															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-53. ADC-*n*-Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEVICE_ID	R	1220h	Device ID

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7.6.28 Software Reset (SW_RST) Register (read or write address = 7Ch) [reset = N/A)

The software reset register resets all registers to the default values, except for the DAC data register, DAC latch, and DAC clear register. The software reset is similar to a hardware reset, which resets all registers including the DAC data register, DAC latch, and DAC clear register. After a software reset, make sure that the DAC data register, DAC latch, and DAC clear register are set to the desired values before the DAC is powered on.

7.6.28.1 SPI Mode

図 7-73. Software Reset Register (SPI Mode)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SW_RST [15:0]															
R/W-0h															

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7-54. Software Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SW_RST	R/W	0h	Writing 6600h to this register forces the device to reset.

7.6.28.2 I^2C Mode

Writing to this register (with any data) forces the device to perform a software reset. Reading this register returns an undefined value that must be ignored. Note that this register is 8-bit, instead of 16-bit. Both reading from and writing to this register are single-byte operations. Writing data to the software reset register in I^2C mode is described in the following steps:

1. The controller device asserts a start condition.
2. The controller then sends the 7-bit device target address followed by a 0 for the direction bit, indicating a write operation.
3. The device asserts an acknowledge signal on SDA.
4. The controller sends register address 7Ch.
5. The device asserts an acknowledge signal on SDA.
6. The controller sends a data byte.
7. The device asserts an acknowledge signal on SDA.
8. The controller asserts a stop condition to end the transaction.

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8 Application and Implementation

注

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8.1 Application Information

The AFE11612-SEP is a flexible device that can be used in control, monitoring, and biasing applications. Examples are supply rail monitoring, temperature sensor monitoring, power amplifier (PA) gate-bias control, and servo control. The AFE11612-SEP has features that can be used to detect alarm conditions, and has a dedicated $\overline{\text{ALARM}}$ pin to alert the host of any problems.

8.2 Typical Application

図 8-1 shows an example schematic for PA biasing using a single AFE11612-SEP to bias the GaN and LDMOS PAs simultaneously. In this application, one DAC is used in the positive output range, and a second DAC is used in the negative range through the use of a differential operational amplifier.

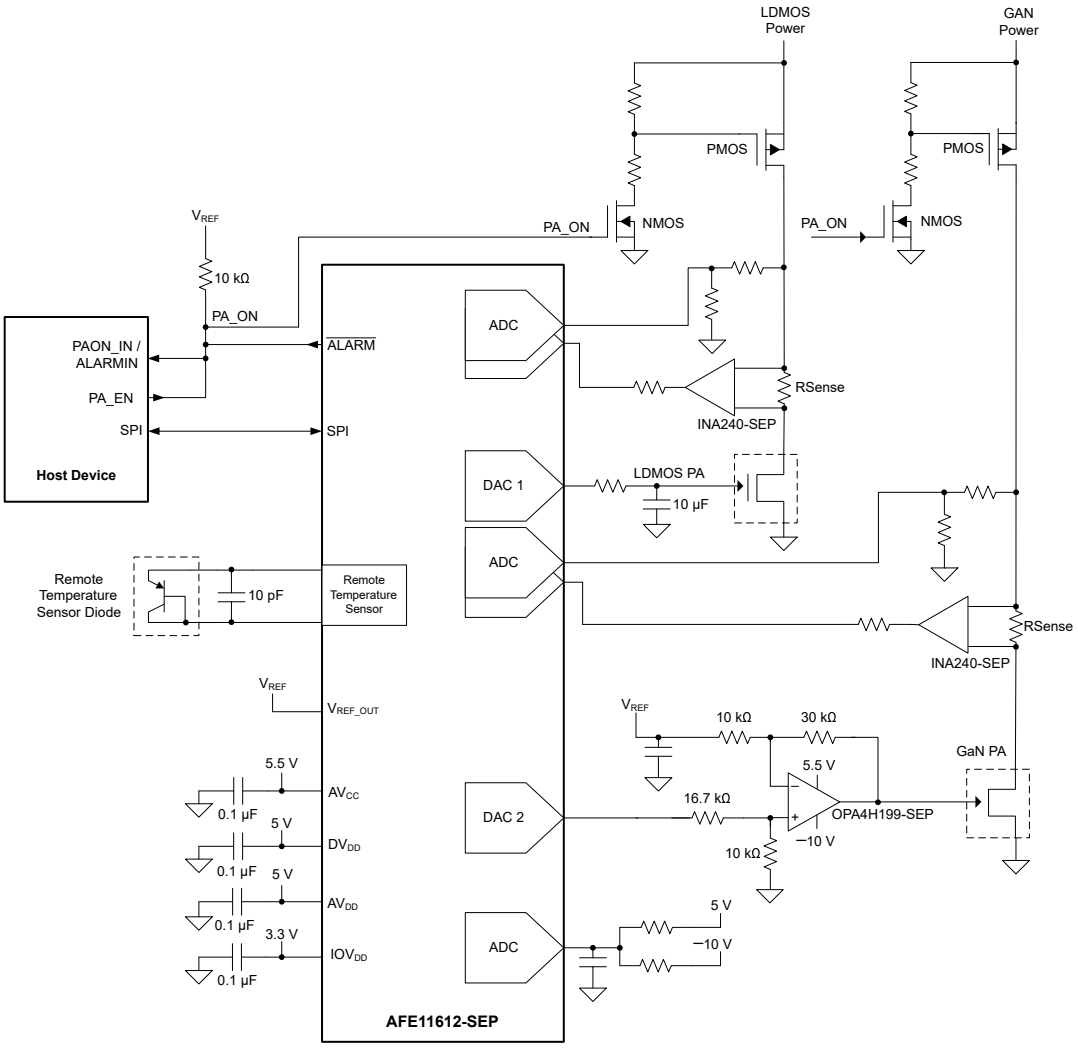


図 8-1. Power Amplifier (PA) Biasing

8.2.1 Design Requirements

The example schematic uses the majority of the design parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Analog supply voltage	4.5 V to 5.5 V
Digital supply voltage	3.3 V
DAC outputs voltage	0 V to 5 V
DAC outputs voltage (optional)	–7.5 V to 0 V
ADC voltage	5 V

8.2.2 Detailed Design Procedure

Use the parameters in 表 8-1 and the following steps to facilitate the design process:

- Connect the analog and digital pins to the voltage supply
- Scale the analog inputs to be in range of the ADC.
- Select series resistance for the DAC output based on the capacitive load.
- Optional: configure op-amp circuit for a negative output range.

8.2.2.1 Sequencing

Powering the PA on and off in a controlled routine is necessary to prevent the V_{GS} voltage from being too high when the V_{DRAIN} is applied. Such a state causes the PA to operate in saturation mode which can result in thermal damage in the PA or any connected board. Powering on a PA requires the following steps:

1. First, apply the V_{GS} signal to the PA. The V_{GS} voltage must transition to the V_{GS} pinch-off voltage or lower. This makes sure that when the V_{DRAIN} voltage is applied, the gate is already low.
2. Next, enable the drain voltage supply and allow the V_{DRAIN} to be powered to the nominal value (50 V, for example). As the V_{GS} is at the pinch-off voltage, I_{DS} must be minimal.
3. After the V_{DRAIN} is applied, increase the V_{GS} bias voltage to set the desired power output of the PA.
4. Finally, enable the RF signal. This allows the PA to transmit a signal.

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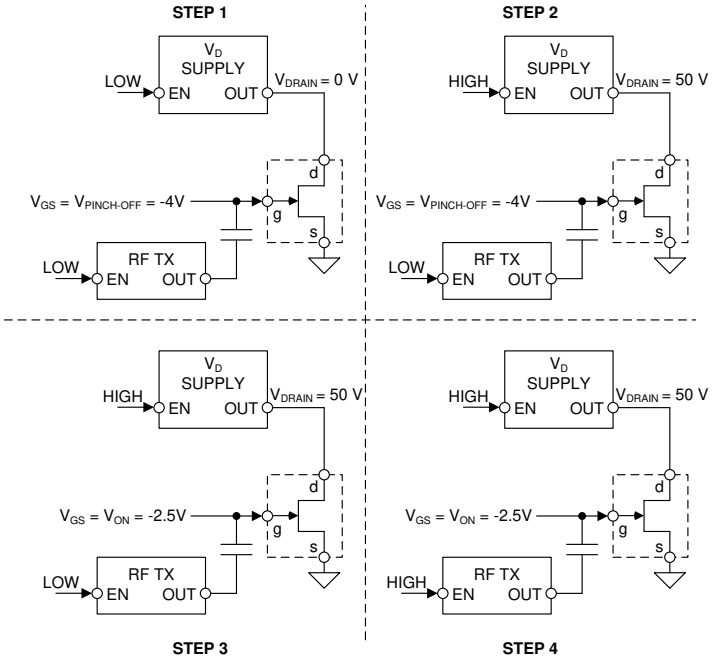


図 8-2. GaN Power Sequencing

The PA can be safely shut down by reversing the power-on steps.

1. Disable the RF signal from the PA.
2. Reduce the V_{GS} voltage to the pinch-off value, eliminating the power output of the PA.
3. Disable the V_{DRAIN} voltage by sending a disable signal to the drain supply.
4. Finally, the V_{GS} voltage can be allowed to collapse to ground as the PA is fully disabled.

8.2.2.2 Negative GaN Biasing

The AFE11612-SEP features twelve 12-bit DACs. The device has an internal 2.5-V reference that scales the DAC output range from 0 V to 5 V. GaN PAs require negative gate voltage to be properly biased, with pinch-off voltages being more negative than the on voltages. The DAC output can be converted to a negative voltage through the use of a differential op-amp circuit that is powered by a negative power supply (V_{SS}). The following circuit uses the op-amp OPA4H199-SEP to offset and scale the 5-V output range to –7.5 V to 0 V. A differential op-amp circuit is used to protect the PA in case of an alarm shutdown. In an alarm state, the DAC drives the voltage to 0 V. The differential circuit outputs –7.5 V to the GaN gate, making sure that the GaN PA turns off.

> **注意**
> The use of an inverting amplifier configuration is not recommended as the *off state* drives the output to 0 V, which can damage the PA in an alarm state.

The AFE11612-SEP 2.5-V reference output provides the offset voltage for the differential circuit. The resistors in the circuit were selected with the purpose of providing a –7.5 V to 0 V output range, while not significantly loading V_{REF}. The OPA4H199-SEP has a 40-V supply range, and the circuit can be modified to support greater negative-voltage applications if needed.

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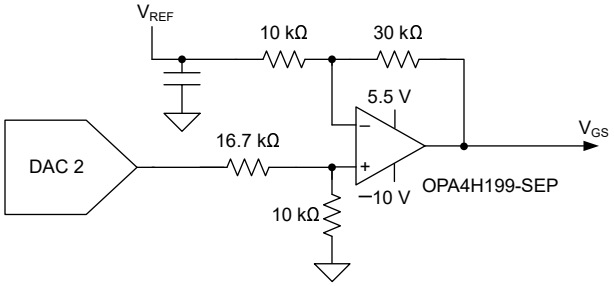


図 8-3. Differential Operational Amplifier Circuit

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8.2.2.3 V_{DRAIN} Monitoring

The V_{DRAIN} voltage must be monitored to make sure that the PA drain supply is operating at the expected voltage. A resistor divider is required to properly scale the V_{DRAIN} voltage, as the voltage range for the ADC is selected to be 0 V to 2.5 V or 0 V to 5 V. This can be accomplished using the integrated successive-approximation register (SAR) ADC in the AFE11612-SEP. SAR ADCs have an internal sampling capacitor which must be charged every time there is an ADC conversion. This capacitor must be charged within the sample acquisition time to make sure the ADC measures the voltage correctly. This is done using a charge-bucket filter with an external capacitor (C_{FILT}) of approximately 1 nF. Limit the impedance of the resistor divider to 10 kΩ to allow sufficient current to charge the sampling capacitor.

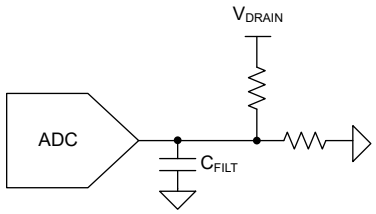


図 8-4. V_{DRAIN} Monitor Circuit

8.2.3 Application Curves

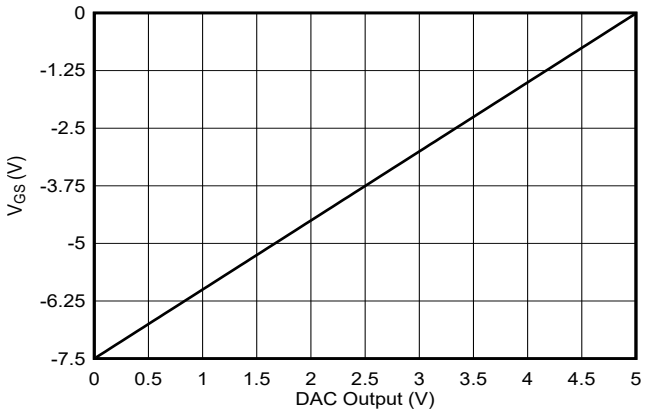


図 8-5. Differential Operational Amplifier Output

8.3 Power Supply Recommendations

8.3.1 Power-Supply Sequence

The preferred (not required) order for applying power is IOV_{DD}, DV_{DD} or AV_{DD}, and then AV_{CC}. All registers initialize to default values after these supplies are established. Communication with the device is valid after a 250-µs maximum power-on reset delay. The default state of all analog blocks is off as determined by the power-down register (6Bh). Before writing to this register, issue a hardware reset to maintain specified device operation. Device communication is valid after a maximum 250-µs reset delay from the $\overline{RESET}$ rising edge. If DV_{DD} falls to less than 2.7 V, the minimum supply value of DV_{DD}, either issue a hardware or power-on reset to resume proper operation.

To avoid activating the device ESD protection diodes, do not apply the GPIO-4, GPIO-5, GPIO-6, and GPIO-7 inputs before AV_{DD} is established. Also, if using the external reference configuration of the ADC, do not apply ADC-REF-IN/CMP before AVDD.

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8.4 Layout

8.4.1 Layout Guidelines

- Bypass all power supply pins to ground with a low-ESR ceramic bypass capacitor. Bypass capacitors on the AV_{CC} and inputs are recommended to be 3 to 4 times the total capacitance on the DAC outputs to make sure the inrush current does not cause localized supply collapse when the outputs transition to different voltage output. The typical recommended bypass capacitor has a value of 10 µF and is ceramic with X7R or NP0 dielectric.
- To reduce noise on the internal reference, a 4.7 µF capacitor is recommended between the ADC-REF-IN/CMP pin and ground if internal reference is used to drive the ADC.
- If only using internal reference, short REF-DAC and REF-OUT as close as possible to the device.
- Bypass REF-DAC and REF-OUT with bypass capacitors that have a value of around 10 nF.
- When using the local temperature sensor for the output bias voltage temperature compensation, place the device geographically close to the PA, preferably sharing a solid ground plane for thermal conduction.
- Connect the thermal pad on the device to a large copper area, preferably a ground plane.

8.4.2 Layout Diagram

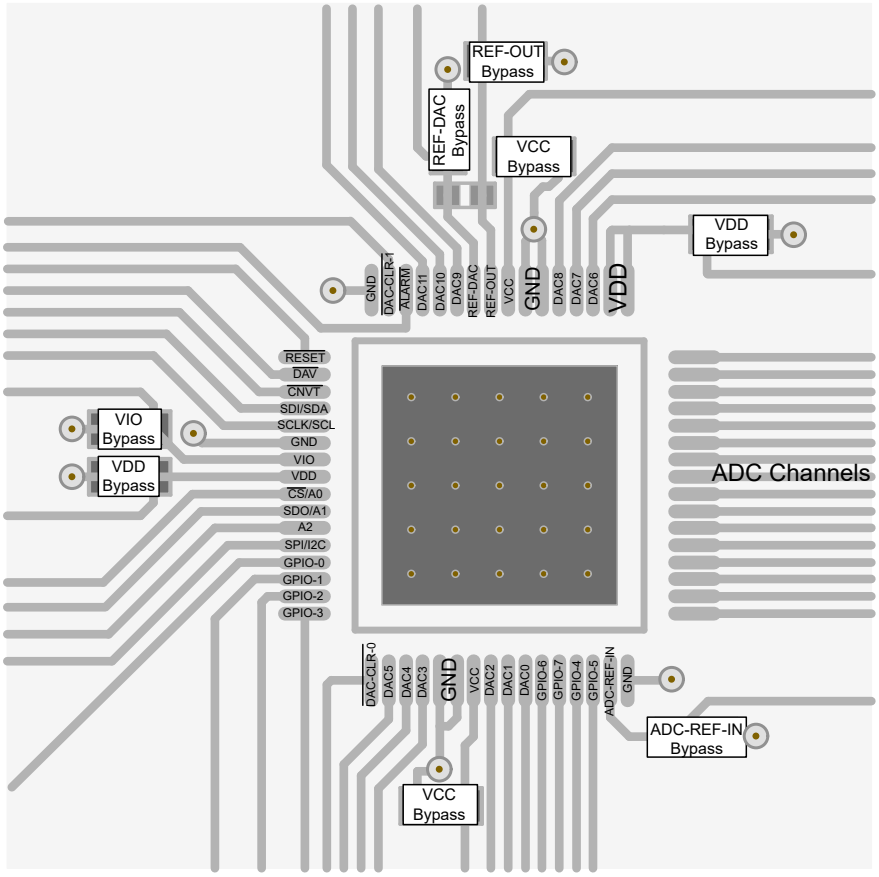


図 8-6. AFE11612-SEP Layout Example

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9 Device and Documentation Support

9.1 Documentation Support

注

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.4 Trademarks

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9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE11612PAPSEP	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP
AFE11612PAPSEP.A	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AFE11612 PAPSEP
V62/22614-01XE	Active	Production	HTQFP (PAP) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	See AFE11612PAPSEP	AFE11612 PAPSEP

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

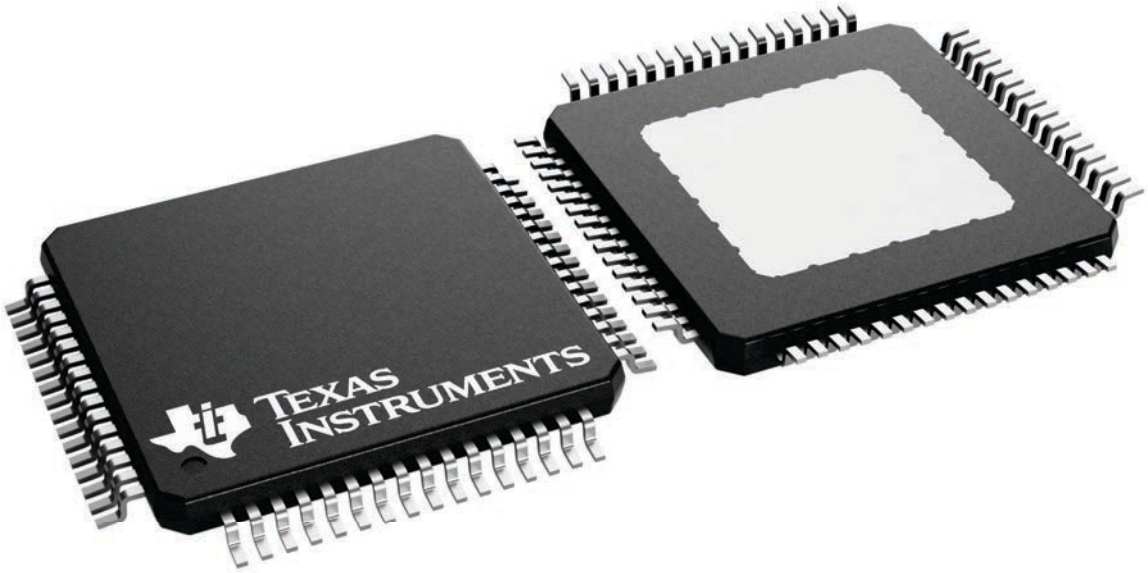
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



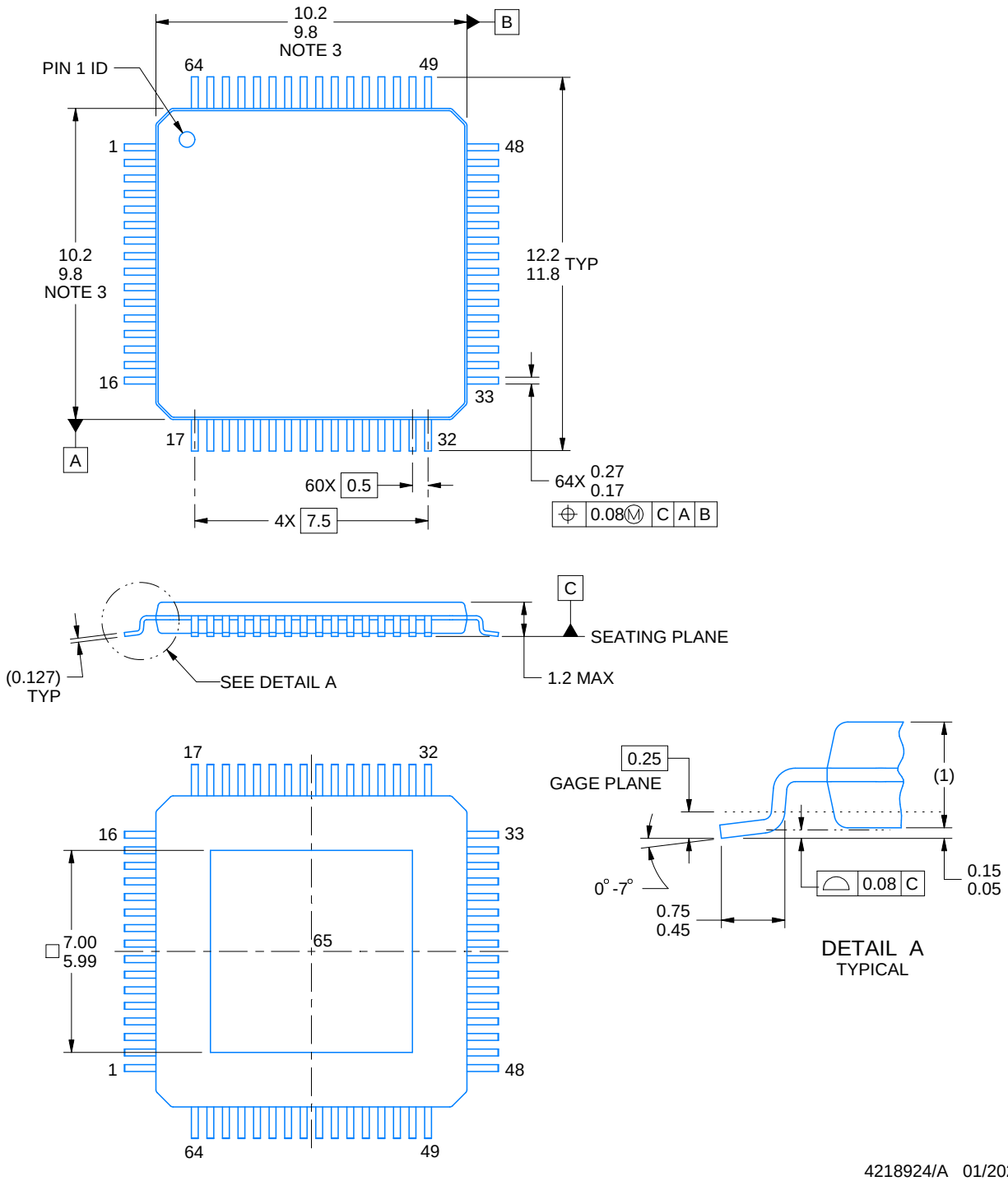
4226442/A

PACKAGE OUTLINE

PAP0064G

PowerPAD™ TQFP - 1.2 mm max height

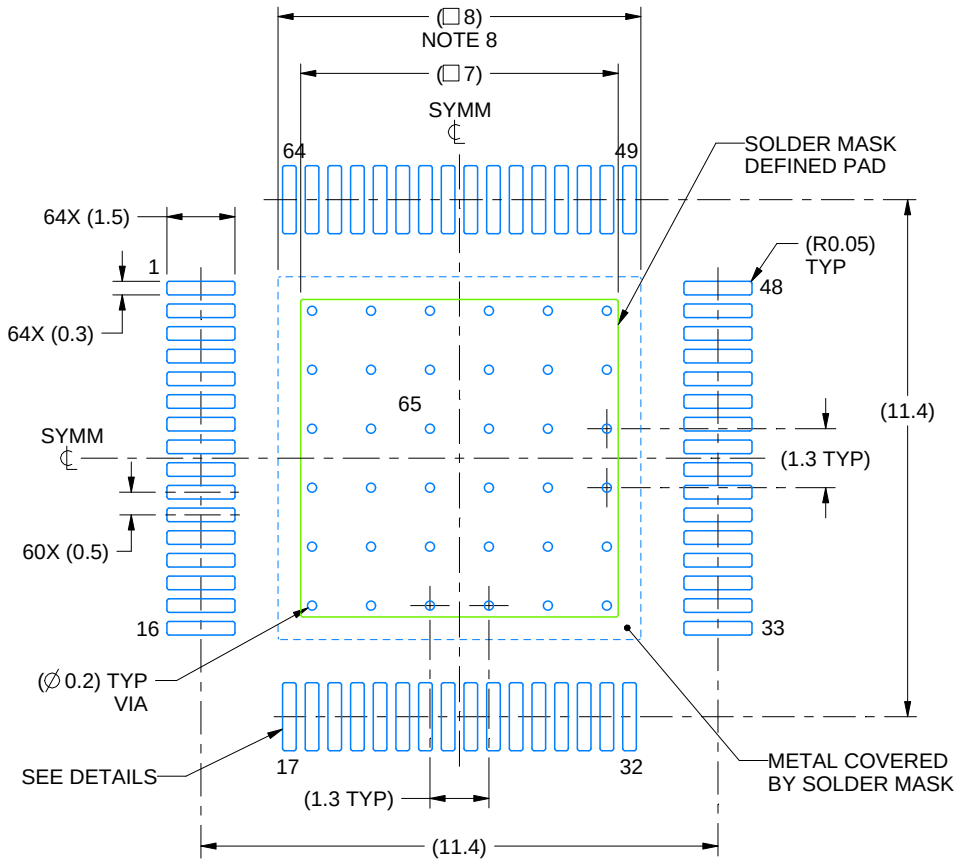
PLASTIC QUAD FLATPACK



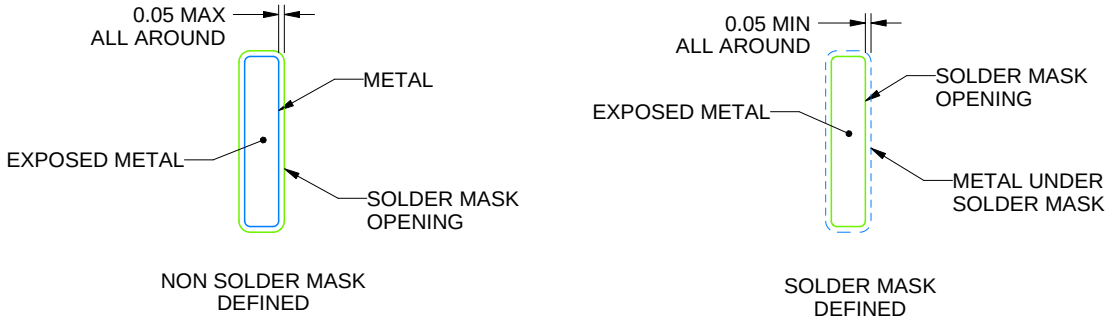
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

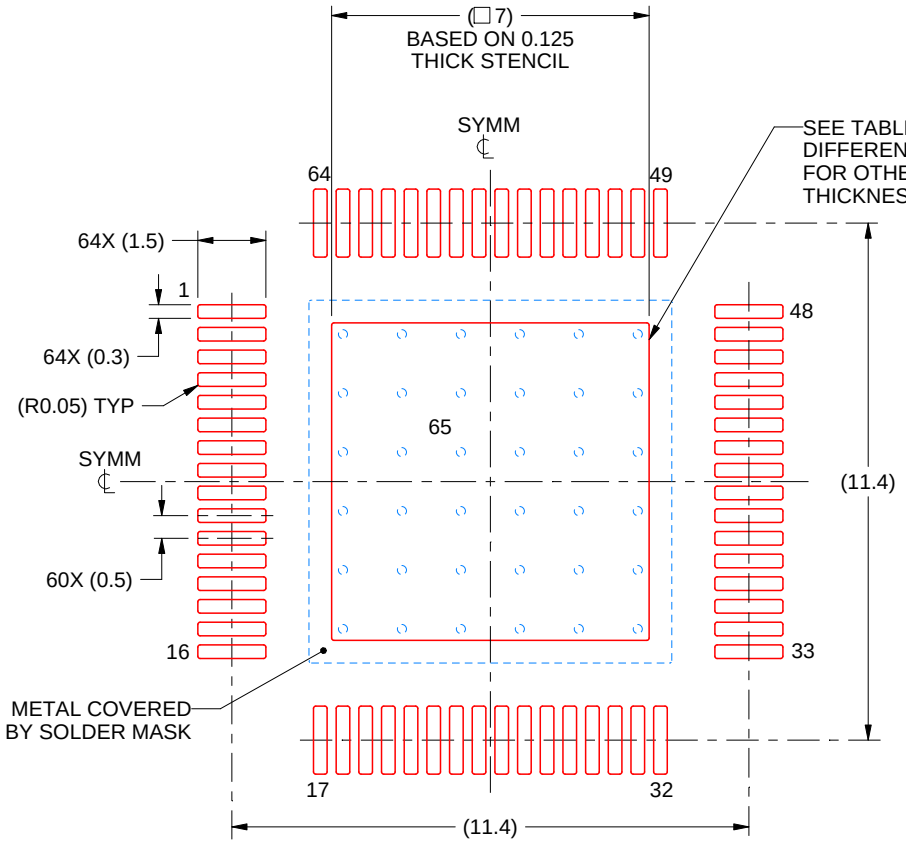


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.83 X 7.83
0.125	7.0 X 7.0 (SHOWN)
0.15	6.39 X 6.39
0.175	5.92 X 5.92

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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