AFE7900 12GSPS DAC と 3GSPS ADC 搭載、4T6R RF サンプリング AFE

1 特長

- データシート全体のご請求
- クワッド RF サンプリング 12GSPS 送信 DAC
- クワッド RF サンプリング 3GSPS 受信 ADC
- デュアル RF サンプリング 3GSPS フィードバック (補助 RX) ADC
- 最大 RF 信号帯域幅:
  - 4TX または 2FB:1200MHz または 2TX: 2400MHz
  - RX):1200MHz (FB なし)、600MHz (FB 付き)
- RF 周波数範囲:
  - TX:5MHz～7.4GHz
  - RX/FB:5MHz ～7.4GHz
- デジタル・ステップ・アッテネータ (DSA):
  - TX:40dB レンジ、0.125dB ステップ
  - RX または FB:25dB レンジ、0.5dB ステップ
- TX と RX 向けにシングルバンドまたはデュアルバンド DUC または DDC を搭載
- TX または RX と FB に対応する 16 個の NCO
- DAC もしくは ADC クロック用の内部 PLL もしくは VCO、または DAC もしくは ADC サンプル・レートでの外部クロックを選択可能
- Sysref アライメント検出器
- SerDes データ・インターフェイス:
  - JESD204B、JESD204C 適合
  - 8 つの SerDes トランシーバ (最高 29.5Gbps)
  - サブクラス 1 のマルチデバイス同期
- パッケージ:17mm × 17mm FCBGA、0.8mm ピッチ

2 アプリケーション

- レーダー
- 追尾フロント・エンド
- 防衛無線
- 戦術通信網
- ワイヤレス通信テスト

3 説明

AFE7900 は、高性能で広帯域幅のマルチチャネル・トランシーバで、4 つの RF サンプリング・トランスミッタ・チェーン、4 つの RF サンプリング・レシーバ・チェーン、2 つの RF サンプリング・フィードバック・チェーン (合計 6 つの RF サンプリング ADC) を統合しています。このデバイスは、最大 7.4GHz で動作するため、追加の周波数変換段を必要とせず、L、S、C バンドの周波数範囲について直接 RF サンプリングが可能です。密度と柔軟性の向上により、多くのチャネル数を持つマルチミッション・システムが可能になります。

TX 信号パスは、4 個の TX で最大 1200MHz の信号帯域幅、または 2 個の TX で 2400MHz を実現する、補間およびデジタル・アップコンバージョン・オプションをサポートしています。DUC の出力は、2 次ナイキスト動作を拡張する混在モード出力方式で 12GSPS の DAC (D/A コンバータ) を駆動します。DAC 出力は、40dB レンジ、1dB アナログ・ステップ、0.125dB デジタル・ステップの可変ゲイン・アンプ (TX DSA) を内蔵しています。

各レシーバ・チェーンは、3GSPS の ADC (A/D コンバータ) に接続された 25dB レンジの DSA (デジタル・ステップ・アッテネータ) を備えています。各レシーバ・チャネルは、外部または内部の自律的な AGC (自動ゲイン制御) を補助するためのアナログ・ピーク電力検出器とさまざまなデジタル電力検出器、およびデバイスの信頼性を確保するための RF 過負荷検出器を備えています。柔軟なデシメーション・オプションによりデータ帯域幅を最適化でき、FB パスなしの 4 つの RX では最高 1200MHz、2 つの FB パス付き (それぞれ 1200MHz の帯域幅) では最高 600MHz が得られます。

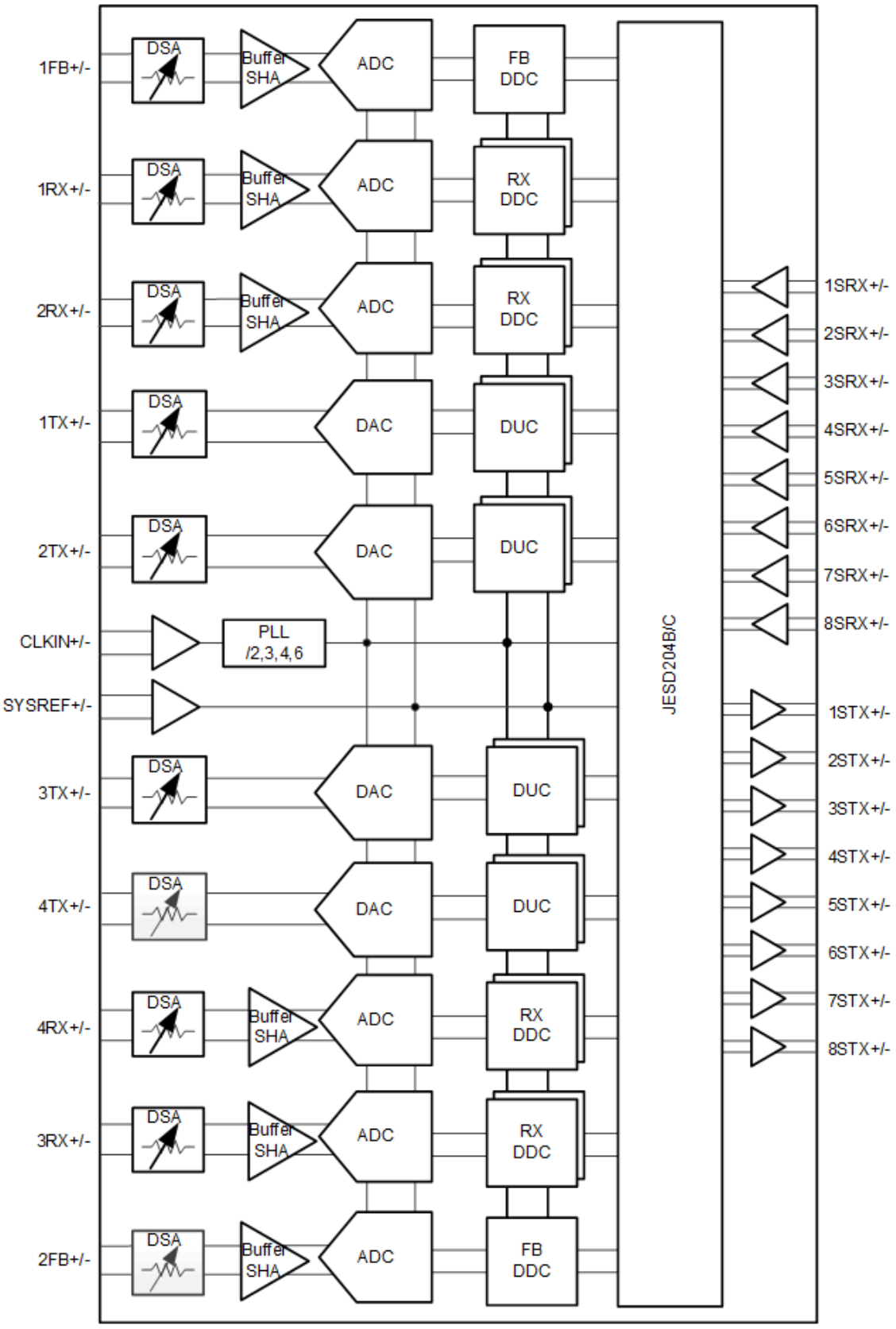
SYSREF タイミング検出器を搭載しているため、デバイス・クロックを基準とした SYSREF 入力タイミングの最適化が可能です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
AFE7900	FC-BGA	17mm × 17mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。



機能ブロック図

Copyright © 2023 Texas Instruments Incorporated

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 説明 ... 1
4 Revision History ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 Recommended Operating Conditions ... 5
5.4 Thermal Information ... 5
5.5 Transmitter Electrical Characteristics ... 6
5.6 RF ADC Electrical Characteristics ... 15
5.7 PLL/VCO/Clock Electrical Characteristics ... 21
5.8 Digital Electrical Characteristics ... 23
5.9 Power Supply Electrical Characteristics ... 25
5.10 Timing Requirements ... 30
5.11 Switching Characteristics ... 31
5.12 Typical Characteristics ... 32
6 Device and Documentation Support ... 150
6.1 ドキュメントの更新通知を受け取る方法 ... 150
6.2 サポート・リソース ... 150
6.3 商標 ... 150
6.4 静電気放電に関する注意事項 ... 150
6.5 用語集 ... 150
7 Mechanical, Packaging, and Orderable Information 150

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from August 6, 2021 to June 14, 2023 (from Revision A (August 2021) to Revision B (June 2023)) — **Page**

- 「パッケージ情報」表を変更して、注 2 を追加 ... 1
- Changed I_{IH} and I_{IL} units to µA ... 23
- Changed 0RX - 3RX to 1RX - 4RX in several plots ... 54
- Changed 0RX - 3RX to 1RX - 4RX in several plots ... 59
- Changed 0TX - 3TX to 1TX - 4TX ... 72
- Removed dither plot. This is set automatically in the configuration software ... 72
- Deleted TX Clock Dither Enabled from all TX Typical Characteristics Sections ... 72
- Change 0TX - 3TX to 1TX to 4TX in several plots ... 102
- Removed figure vs dither. This is set automatically in the configuration software ... 102
- Changed 0TX - 3TX to 1TX - 4TX ... 115
- Removed dither plot. This is set automatically in the configuration software ... 115
- Change 0TX - 3TX to 1TX - 4TX ... 136
- Changed 1st Nyquist zone output to 2nd Nyquist zone output ... 136

Changes from Revision * (February 2021) to Revision A (August 2021) — **Page**

- データシート全体のご請求に「特長」を追加 ... 1
- Added the Specification tables to the data sheet ... 4

Copyright © 2023 Texas Instruments Incorporated

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	–0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	–0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	–0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	–0.5	VDDRX1P8+0.3	V
	1FBIN+/-, 2FB+/-	–0.5	VDDFB1P8+0.3	V
	{1/2/3/4}TXOUT+/-	–0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	–0.3	1.4	V
	{1:8}SRX+/-	–0.3	1.4	V
	{1:8}STX+/-	–0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1	–0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	–0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	–0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Copyright © 2023 Texas Instruments Incorporated

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/TXENC/PLL/PLLVCO/FB/FBCLK/GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T_A	Ambient temperature	–40		85	°C
T_J	Operating Junction Temperature			110(1)	°C
	Maximum Operating Junction Temperature	125			°C

(1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to SBAA403 application note for additional details

5.4 Thermal Information

THERMAL METRIC(1)		AFE7900 FC-BGA 400 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	16.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.42	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.85	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC_{RES}	DAC resolution			14		bits
f_{RFout}	RF output frequency range	f_{DAC} = 12 GSPS, 1st Nyquist	5		6000	MHz
		f_{DAC} = 9 GSPS, 1st Nyquist	5		4500	
		f_{DAC} = 9 GSPS, 2nd Nyquist	4500		7400	
		f_{DAC} = 6 GSPS, 1st Nyquist	5		3000	
		f_{DAC} = 6 GSPS, 2nd Nyquist	3000		6000	
P_{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f_{out} = 10 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 30 MHz, f_{DAC} = 6GSPS, -0.1dBFS		6.5		dBm
		f_{out} = 400 MHz, f_{DAC} = 6GSPS, -0.1dBFS		5.6		dBm
		f_{out} = 850 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		4.3		dBm
		f_{out} = 1800 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS		3.2		dBm
		f_{out} = 2600 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS		2.3		dBm
		f_{out} = 3500 MHz, -0.5dBFS		2.9		dBm
		f_{out} = 4900 MHz, -0.5dBFS		-0.6		dBm
		f_{out} = 3500 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-2.3		dBm
		f_{out} = 4900 MHz, f_{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		-3.4		dBm
		f_{out} = 4900 MHz, f_{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-3.9		dBm
R_{TERM}	Output termination resistor	Default setting		100		Ω
ATT_{range}	DSA Attenuation range			40		dB
ATT_{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL) (2)	0 < Atten < 40dB, after calibration		±0.1		dB
		0 < Atten < 40dB, before calibration		±0.2		
ATT_{step}	DSA Gain Steps Phase accuracy, any 8dB range(2)	f_{out} = 30MHz		±1		deg
		f_{out} = 400MHz		±1		deg
		f_{out} = 850MHz		±1		deg
		f_{out} = 1800MHz		±1		deg
		f_{out} =2600MHz		±1		deg
		f_{out} = 3500MHz		±1		
		f_{out} = 4900MHz		±1		deg
G_{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F_{out} < 4.9G		1.2		

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion	f_{DAC} =6 GSPS, f_{out} = 5MHz ±1MHz, -7dBFS each tone		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -7dBFS each tone		-47		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -7dBFS each tone		-51		dBc
		f_{out} = 850MHz ±10MHz, -7dBFS each tone		-61		dBc
		f_{out} = 1800MHz ±10MHz, -7dBFS each tone		-62		dBc
		f_{out} = 2600MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 3500MHz ±10MHz, -7dBFS each tone		-63		dBc
		f_{out} = 4900MHz ±10MHz, -7dBFS each tone		-64		dBc
		f_{out} = 5MHz ±1MHz, -13dBFS each tone		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30MHz ±1MHz, -13dBFS each tone		-71		dBc
		f_{DAC} =6 GSPS, f_{out} = 400MHz ±2MHz, -13dBFS each tone		-72		dBc
		f_{out} = 850MHz ±10MHz, -13dBFS each tone		-73		dBc
		f_{out} = 1800MHz ±10MHz, -13dBFS each tone		-75		dBc
		f_{out} = 2600MHz ±10MHz, -13dBFS each tone		-79		dBc
		f_{out} = 3500MHz ±10MHz, -13dBFS each tone		-77		dBc
		f_{out} = 4900MHz ±10MHz, -13dBFS each tone		-77		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	f_{out} = 30 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		45		dBc
		f_{out} = 400 MHz, f_{DAC} = 6000 MSPS, interleave mode, 20Gbps SerDes rate		48		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		62		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		56		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		39		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		42		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		60		dBc

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_S/2 - f_{OUT}$	Interleaving Image	f_{DAC} = 5898.24MSPS, interleave mode		-47		dBc
		f_{DAC} = 8847.36 MSPS, interleave mode		-43		dBc
		f_{DAC} = 11796.48MSPS, interleave mode		-43		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-72		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-75		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-73		dBc
		f_{out} = 400 MHz		-46		dBc
		f_{out} = 850 MHz		-65		dBc
		f_{out} = 1800 MHz		-68		dBc
		f_{out} = 2600 MHz		-47		dBc
		f_{out} = 3500 MHz		-59		dBc
		f_{out}= 4900 MHz		-48		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-74		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-67		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-58		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-69		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-59		dBc
HD3	3rd Harmonic Distortion (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-46		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-48		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-49		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-49		dBc
		f_{out} = 850 MHz		-56		dBc
		f_{out} = 1800 MHz		-58		dBc
		f_{out} = 2600 MHz		-60		dBc
		f_{out} = 3500 MHz		-63		dBc
		f_{out}= 4900 MHz		-66		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-83		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-82		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-79		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-84		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-88		dBc

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	f_{DAC} =6 GSPS, f_{out} = 5 MHz		-58		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz		-60		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz		-61		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz		-50		dBc
		f_{out} = 850 MHz		-85		dBc
		f_{out} = 1800 MHz		-90		dBc
		f_{out} = 2600 MHz		-84		dBc
		f_{out} = 3500 MHz		-86		dBc
		f_{out}= 4900 MHz		-87		dBc
		f_{DAC} =6 GSPS, f_{out} = 5 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{DAC} =6 GSPS, f_{out} = 30 MHz, A_{OUT}=-12dBFS		-94		dBc
		f_{DAC} =6 GSPS, f_{out} = 100 MHz, A_{OUT}=-12dBFS		-93		dBc
		f_{DAC} =6 GSPS, f_{out} = 400 MHz, A_{OUT}=-12dBFS		-85		dBc
		f_{out} = 850 MHz, A_{OUT}=-12dBFS		-89		dBc
		f_{out} = 1800 MHz, A_{OUT}=-12dBFS		-92		dBc
		f_{out} = 2600 MHz, A_{OUT}=-12dBFS		-87		dBc
		f_{out} = 3500 MHz, A_{OUT}=-12dBFS		-88		dBc
		f_{out}= 4900 MHz, A_{OUT}=-12dBFS		-89		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	f_{DAC} =6 GSPS, f_{out} = 400 MHz		87		dBc
		f_{out} = 850 MHz, f_{DAC} = 11796.48 MSPS		84		dBc
		f_{out} = 1800 MHz, f_{DAC} = 11796.48 MSPS		78		dBc
		f_{out} = 2600 MHz, f_{DAC} = 11796.48 MSPS		80		dBc
		f_{out} = 3500 MHz, f_{DAC} = 11796.48 MSPS		81		dBc
		f_{out}= 4900 MHz, f_{DAC} = 11796.48 MSPS		74		dBc
$f_S/4$	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/4-50MHz		-95		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/4-50MHz		-88		dBFS
		f_{DAC} = 11796.48MSPS, f_{OUT}=f_{DAC}/4-50MHz		-76		dBFS
$f_S/2$	Fixed Spur	f_{DAC} = 5898.24MSPS, f_{OUT}=f_{DAC}/2-50MHz		-52		dBFS
		f_{DAC} = 8847.36MSPS, f_{OUT}=f_{DAC}/2-50MHz		-45		dBFS
		f_{DAC} = 11796.48 MSPS, f_{OUT}=f_{DAC}/2-50MHz		-49		dBFS

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_S/4$	Fixed Spur	2nd Nyquist, f_{DAC} = 5898.24MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-82		dBFS
		2nd Nyquist, f_{DAC} = 8847.36MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-75		dBFS
		2nd Nyquist, f_{DAC} = 11796.48MSPS, $f_{OUT}=3*f_{DAC}/4$-50MHz		-49		dBFS
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 0.85 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-70		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-62		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 1.8425 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-61		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-50		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-72		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-66		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-60		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-71		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-69		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-64		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-58		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-47		dBc

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 2.6 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-65		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-59		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-53		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-49		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-38		dBc
$ACPR_{1xcarr}$	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f_{out} = 4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-63		dBc
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-56		dBc
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-51		dBc
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFS		-41		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	F_{out} =0.85 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.16		%
		F_{out} =1.8425 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.21		%
		F_{out} =2.6 GHz, f_{DAC} = 11796.48MSPS, P_{OUT}=-13dBFs		0.24		%
		F_{out} =3.5 GHz, P_{OUT}=-13dBFs		0.27		%
		F_{out} =4.9 GHz, P_{OUT}=-13dBFs		0.38		%
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 5 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-148		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-143		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-129		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 30 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-154		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-142		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-132		dBFS/Hz

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 100 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-158		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-146		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-136		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 400 MHz	Atten=0dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-160		dBFS/Hz
		Atten=20dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-153		dBFS/Hz
		Atten=28dB, f_{DAC} =6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-150		dBFS/Hz
		Atten=39dB, f_{DAC} = 6000MSPS, 20Gbps SerDes rate, Pout=-12dBFs		-139		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 0.85 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-158.8		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-152.7		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-148.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-137.9		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 1.8 GHz	Atten=0dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-157.9		dBFS/Hz
		Atten=20dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-151.3		dBFS/Hz
		Atten=28dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-145.6		dBFS/Hz
		Atten=39dB, f_{DAC} = 5898.24MSPS, Pout=-13dBFs		-134.8		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset f_{OUT} = 2.6 GHz	Atten=0dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-158.3		dBFS/Hz
		Atten=20dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-151.6		dBFS/Hz
		Atten=28dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-144.9		dBFS/Hz
		Atten=39dB, f_{DAC} = 8847.36MSPS, Pout=-13dBFs		-134.0		dBFS/Hz
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =3.5 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-158.2		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-150.9		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-144.4		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-133.4		dBFS/Hz

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD_{dBFS}	Noise Spectral Density 20MHz offset F_{out} =4.9 GHz	Atten=0dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-154.6		dBFS/Hz
		Atten=20dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-147.0		dBFS/Hz
		Atten=28dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-140.7		dBFS/Hz
		Atten=39dB, f_{DAC} = 11796.48MSPS, Pout=-13dBFs		-129.9		dBFS/Hz
S22	Output Return Loss, +/- fc * 10%	with matching		-12		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT(1)	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(3)		-96		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-97		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-102		dB
		f_{out} = 400 MHz, f_{DAC} = 6000MSPS, straight mode(4)		-85		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-80		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-77		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-64		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-61		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-60		dB
Isolation	Far Channel: 1/2TXOUT to 3/4TXOUT	f_{out} = 10 MHz, f_{DAC} =6000MSPS, straight mode(3)		-104		dB
		f_{out} = 30 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-100		dB
		f_{out} = 100 MHz, f_{DAC} = 6000MSPS, straight mode(3)		-105		dB
		f_{out} = 400 MH, f_{DAC} = 6000MSPS, straight mode(4)		-97		dB
		f_{out} = 900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-90		dB
		f_{out} = 1850 MHz, f_{DAC} = 8847.36MSPS, straight mode		-91		dB
		f_{out} = 2600 MHz, f_{DAC} = 8847.36MSPS, straight mode		-93		dB
		f_{out} = 3500 MHz, f_{DAC} = 8847.36MSPS, straight mode		-94		dB
		f_{out}= 4900 MHz, f_{DAC} = 8847.36MSPS, straight mode		-83.2		dB

Copyright © 2023 Texas Instruments Incorporated

5.5 Transmitter Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS below 6GHz and 750MSPS above 6GHz, f_{DAC} = 11796.48MSPS below 6GHz and f_{DAC} = 9000MSPS above 6GHz; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN_{TXADD}	Additive Phase Noise External Clock Mode (5)	f_{out} = 3.7GHz, f_{OFFSET} = 100Hz		-97		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1kHz		-106		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10kHz		-117		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 100kHz		-128		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 1MHz		-138		dBc/Hz
		f_{out} = 3.7GHz, f_{OFFSET} = 10MHz		-144		dBc/Hz

(1) Measured with differential 100 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
(2) After DSA calibration procedure
(3) measured with 1µH DC feed inductor
(4) measured with 0.39µH DC feed inductor
(5) Input clock phase noise subtracted.

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC_{RES}	ADC resolution			14		bits
F_{RFin}	RF input frequency range		5		7400	MHz
$P_{FS_CW,min}$	Min Full scale input power, at device pins (1)	f_{IN} = 5 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-0.4		dBm
		f_{IN} = 30 MHz, DSA=0dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-2.2		dBm
		f_{IN} = 410 MHz, DSA=0dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 12		-2.5		dBm
		f_{IN} = 830 MHz, DSA=0dB		-2.9		dBm
		f_{IN} = 1760 MHz, DSA=0dB		-2.8		dBm
		f_{IN} = 2610 MHz, DSA=0dB		-1.8		dBm
		f_{IN} = 3610 MHz, DSA=0dB		-0.4		dBm
		f_{IN} = 4910 MHz, DSA=0dB		0.1		dBm
$P_{FS_CW,MAX}$	MAX Full scale input power - reliability limited, at device pins	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		19.7		dBm
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		17.8		dBm
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		17.6		dBm
		f_{IN} = 830 MHz		16.7		dBm
		f_{IN} = 1760 MHz		17.0		dBm
		f_{IN} = 2610 MHz		18		dBm
		f_{IN} = 3610 MHz		18.5		dBm
		f_{IN} = 4910 MHz		19.3		dBm
R_{TERM}	Input reference impedance			100.0		Ω
ATT_{range}	DSA Attenuation range			25.0		dB
ATT_{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F_{in}=3610MHz, after calibration		0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=3610MHz, after calibration		0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F_{in}=4910MHz, after calibration		1.8		deg
G_{flat}	Gain flatness	Measured Over 80MHz BW		0.2		dB
		Measured Over 200MHz BW		0.5		dB
		Measured Over 400MHz BW		1.1		dB

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise Density (3) (small signal = -30dBFS)	f_{IN} = 5 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-147.1		dBFS/Hz
		f_{IN} = 30 MHz, DSA = 3dB, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-150.7		dBFS/Hz
		f_{IN} = 410 MHz, DSA = 3dB, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-155.4		dBFS/Hz
		f_{IN} = 830 MHz, DSA = 3dB		-156.2		dBFS/Hz
		f_{IN} = 1760 MHz, DSA = 3dB		-156.0		dBFS/Hz
		f_{IN} = 2610 MHz, DSA = 3dB		-155.4		dBFS/Hz
		f_{IN} = 3610 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 4910 MHz, DSA = 3dB		-155.1		dBFS/Hz
		f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48, 3<=Atten<=22		-147.8		dBFS/Hz
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24, 3<=Atten<=22		-151.5		dBFS/Hz
		f_{IN} = 410 MHz, 3<=Atten<=22, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-156.6		dBFS/Hz
		f_{IN} = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f_{IN} = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f_{IN} = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f_{IN} = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f_{IN} = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
NF_{min}	Noise Figure min DSA Atten=0 - 3dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		29.4		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		24.5		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		19.3		dB
		f_{IN} = 830 MHz		19.1		dB
		f_{IN} = 1760 MHz		19.0		dB
		f_{IN} = 2610 MHz		20.9		dB
		f_{IN} = 3610 MHz		22.8		dB
		f_{IN} = 4910 MHz		22.4		dB

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise Figure[4] DSA Atten=4dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		30.6		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		25.1		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		20.1		dB
		f_{IN} = 830 MHz		20.0		dB
		f_{IN} = 1760 MHz		20.6		dB
		f_{IN} = 2610 MHz		21.9		dB
		f_{IN} = 3610 MHz		23.5		dB
		f_{IN} = 4910 MHz		22.3		dB
NF_{max}	Noise Figure DSA Atten=20dB	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		45.9		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		40.2		dB
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		35.0		dB
		f_{IN} = 830 MHz		34.7		dB
		f_{IN} = 1760 MHz		35.2		dB
		f_{IN} = 2610 MHz		36.0		dB
		f_{IN} = 3610 MHz		37.3		dB
		f_{IN} = 4910 MHz		37.6		dB
IMD3	3rd order intermodulation 2 tones at at f_{IN} ± 10MHz -7dBFS each tone	f_{IN} = 30±1 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-82		dBc
		f_{IN} = 400MHz and 405MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-75		dBc
		f_{IN} = 840 MHz		-82		dBc
		f_{IN} = 1770 MHz		-84		dBc
		f_{IN} = 2610 MHz		-74		dBc
		f_{IN} = 3610 MHz		-77		dBc
		f_{IN} = 4920 MHz		-76		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		100		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		94		dBFS
		f_{IN} = 830 MHz		88		dBFS
		f_{IN} = 1760 MHz		81		dBFS
		f_{IN} = 2610 MHz		88		dBFS
		f_{IN} = 3610 MHz		84		dBFS
		f_{IN} = 4910 MHz		79		dBFS

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion A_{IN} = -3 dBFS(2)	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-84		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-90		dBFS
		f_{IN} = 830 MHz		-86		dBFS
		f_{IN} = 1760 MHz		-90		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-87		dBFS
		f_{IN} = 4910 MHz		-84		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-78		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-96		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-94		dBFS
		f_{IN} = 830 MHz		-80		dBFS
		f_{IN} = 1760 MHz		-85		dBFS
		f_{IN} = 2610 MHz		-86		dBFS
		f_{IN} = 3610 MHz		-78		dBFS
		f_{IN} = 4910 MHz		-75		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -3 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-94		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-94		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-94		dBFS
		f_{IN} = 830 MHz		-88		dBFS
		f_{IN} = 1760 MHz		-81		dBFS
		f_{IN} = 2610 MHz		-88		dBFS
		f_{IN} = 3610 MHz		-84		dBFS
		f_{IN} = 4910 MHz		-82		dBFS
SFDR	Spurious Free Dynamic Range A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		101		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		95		dBFS
		f_{IN} = 830 MHz		89		dBFS
		f_{IN} = 1760 MHz		89		dBFS
		f_{IN} = 2610 MHz		95		dBFS
		f_{IN} = 3610 MHz		87		dBFS
		f_{IN} = 4910 MHz		90		dBFS

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion[2] A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-104		dBFS
		f_{IN} = 830 MHz, with board trim		-79		dBFS
		f_{IN} = 1760 MHz, with board trim		-102		dBFS
		f_{IN} = 2610 MHz, with board trim		-100		dBFS
		f_{IN} = 3610 MHz, with board trim		-101		dBFS
		f_{IN} = 4910 MHz, with board trim		-99		dBFS
HD3	3rd Harmonic Distortion A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-103		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, Bypass Mode (TI only test mode)		-84		dBFS
		f_{IN} = 381 MHz, f_{ADC} = 3000MSPS, Bypass Mode (TI only test mode)		-91		dBFS
		f_{IN} = 830 MHz		-95		dBFS
		f_{IN} = 1760 MHz		-95		dBFS
		f_{IN} = 2610 MHz		-98		dBFS
		f_{IN} = 3610 MHz		-97		dBFS
		f_{IN} = 4910 MHz		-94		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 A_{IN} = -13 dBFS	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-104		dBFS
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-105		dBFS
		f_{IN} = 410 MHz, f_{ADC} = 3000MSPS, f_{NCO} = 400MHz, Decimate by 24		-95		dBFS
		f_{IN} = 830 MHz		-89		dBFS
		f_{IN} = 1760 MHz		-89		dBFS
		f_{IN} = 2610 MHz		-95		dBFS
		f_{IN} = 3610 MHz		-90		dBFS
		f_{IN} = 4910 MHz		-90		dBFS
RX-RX/FB Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN 1FBIN to 1RXIN 2FBIN to 3RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-98		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-98		dB
		f_{IN} = 400 MHz		-88		dB
		f_{IN} = 830 MHz		-77		dB
		f_{IN} = 1760 MHz		-71		dB
		f_{IN} = 2610 MHz		-74		dB
		f_{IN} = 3610 MHz		-77		dB
		f_{IN} = 4910 MHz		-65		dB

Copyright © 2023 Texas Instruments Incorporated

5.6 RF ADC Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency, f_{ADC} = 2949.12MSPS below 6GHz and f_{ADC} = 3000MSPS above 6GHz; PLL clock mode with f_{REF} = 491.52MHz below 6GHz input frequency and External clock mode with f_{CLK} = 11796.48MHz above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX-FB Isolation	Near Channel: 1TXOUT to 1FBIN 3TXOUT to 2FBIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-92		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-93		dB
		f_{IN} = 400 MHz		-92		dB
		f_{IN} = 830 MHz		-84		dB
		f_{IN} = 1760 MHz		-88		dB
		f_{IN} = 2610 MHz		-86		dB
		f_{IN} = 3610 MHz		-82		dB
		f_{IN} = 4910 MHz		-81		dB
TX-RX Isolation	Far Channel: 1TXOUT to 1RXIN 3TXOUT to 2RXIN	f_{IN} = 5 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 17MHz, Decimate by 48		-105		dB
		f_{IN} = 30 MHz, f_{ADC} = 1500MSPS, f_{NCO} = 30MHz, Decimate by 24		-101		dB
		f_{IN} = 400 MHz		-99		dB
		f_{IN} = 830 MHz		-86		dB
		f_{IN} = 1760 MHz		-87		dB
		f_{IN} = 2610 MHz		-84		dB
		f_{IN} = 3610 MHz		-82		dB
		f_{IN} = 4910 MHz		-82		dB

(1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
(2) After HD2 trim on specific printed circuit board.
(3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
(4) NF increase 1dB per DSA 1dB above DSA = 3dB

Copyright © 2023 Texas Instruments Incorporated

5.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.848	GHz
	VCO2 max frequency		9.216			GHz
f_{VCO3}	VCO3 min frequency				9.8304	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.7965	GHz
	VCO4 max frequency		12.288			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
DIV_{FBADC}	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV_{RXADC}	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise F_{PLL} = 11.79848 GHz F_{REF}=491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		–141		dBc/Hz
	Closed Loop Phase Noise F_{PLL}=8.84736 GHz F_{REF}=491.52MHz	600kHz		-114		dBc/Hz
		800kHz		–118		dBc/Hz
		1MHz		–120		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–135		dBc/Hz
		50MHz		–142		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 9.8403 GHz F_{REF}=491.52MHz	600kHz		–113		dBc/Hz
		800kHz		–116		dBc/Hz
		1MHz		–119		dBc/Hz
		1.8MHz		–125		dBc/Hz
		5MHz		–134		dBc/Hz
		50MHz		–140		dBc/Hz
	Closed Loop Phase Noise F_{PLL}= 7.86432GHz F_{REF}=491.52MHz	600kHz		–116		dBc/Hz
		800kHz		–119		dBc/Hz
		1MHz		–122		dBc/Hz
		1.8MHz		–127		dBc/Hz
		5MHz		–136		dBc/Hz
		50MHz		–143		dBc/Hz
F_{rms}	Clock PLL integrated phase error(1)	f_{PLL}=11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f_{PLL}=8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f_{PLL}=9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
PN_{pll_flat}	Normalized PLL flat Noise	f_{VCO} = 11796.48MHz		–226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz

Copyright © 2023 Texas Instruments Incorporated

5.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{DAC} = f_{VCO}$, $f_{OUT} = f_{DAC}/4$, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SS}	Input Clock level		0.6		1.8	Vppdiff
Coupling				AC Coupling Only		
	REFCLK input impedance(2)	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

(1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

Copyright © 2023 Texas Instruments Incorporated

5.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V_{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V_{SRCOM}	SerDes Input Common Mode			400		mV
Z_{SRdiff}	SerDes Internal Differential Termination(1)			100		Ω
F_{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance(2)	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V_{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V_{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z_{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V_{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V_{IL}	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I_{IH}	High-Level Input Current		–250		250	µA
I_{IL}	Low-Level Input Current		–250		250	µA
C_L	CMOS input capacitance			2		pF
V_{OH}	High-Level Input Voltage		VDD1P8G PIO–0.2			V
V_{OL}	Low-Level Input Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
$F_{SYSREFMAX}$	SYSREF Input Frequency Maximum			40		MHz
$V_{SWINGSRMAX}$	SYSREF Input Swing Maximum			1.8		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} < 500MHz		0.3		Vppdiff(3)
$V_{SWINGSRMIN}$	SYSREF Input Swing Minimum	f_{REF} > 500MHz		0.6		Vppdiff(3)
$V_{COMSRMAX}$	SYSREF Input Common Mode Voltage Maximum			0.8		V
$V_{COMSRMIN}$	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z_T	Input termination	differential		100 (1)		Ω
C_L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V_{ICOM}	Input Common Voltage			1.2		V
V_{ID}	Differential Input Voltage swing			450		Vppdiff(3)
Z_T	Input termination	differential		100		Ω
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V_{OCOM}	Output Common Voltage			1.2		V

Copyright © 2023 Texas Instruments Incorporated

5.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential Output Voltage swing			500		Vppdiff(3)
Z_T	Internal Termination			100		Ω

(1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
(2) Loss tolerance is bump to bump from STX to SRX
(3) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

Copyright © 2023 Texas Instruments Incorporated

5.9 Power Supply Electrical Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T2F - FDD FB 100% on, no RX TX/FB Rate: 491.52 Msps Single Band: 12x Int, FB 6x Dec f_{DAC} = 5898.24 SPS f_{ADC} = 2949.12MSPS f_{TX} = 1.85 GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1		948.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			533.7		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			299.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			804.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			49.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2041.3		mA
P_{diss}	Power Dissipation			6027.1		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Dual Band: 12x Int, FB 6x Dec, RX 24x Dec TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 8847.36MSPS f_{ADC} = 2949.12MSPS f_{OUT}=f_{IN}= 1.9, 2.6 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		820.4		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			735.2		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.4		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			289.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			822.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.6		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2263.8		mA
P_{diss}	Power Dissipation			6359.2		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R2F - FDD FB 100% on TX Dual Band: 12x Int, FB 6x Dec RX Dual Band: RX 24x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 1.85 + 2.15 GHz f_{RX} = 1.75 + 1.88 GHz 64/66 coding, 16.22Gbps TX: 8-16-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1668.6		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			965.1		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			893.4		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			879.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			50.7		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3826.9		mA
P_{diss}	Power Dissipation			10513.0		mW

Copyright © 2023 Texas Instruments Incorporated

5.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R2F - FDD FB 100% on 7.5 GSPS DAC, 2.5 GSPS ADC Single Band: 15x Int, FB 5x Dec Dual Band: RX 20x TX/FB Rate 491.52 Msps RX Rate 122.88 Msps f_{DAC} = 7372.8 MSPS f_{ADC} = 2457.6 MSPS f_{TX} = 1.85 + 2.15 GHz f_{RX} = 1.75 + 1.88 GHz 64/66 coding, 16.22Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-16-16-1		1611.5		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			694.5		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			768.5		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			940.5		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			45.5		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3000.5		mA
P_{diss}	Power Dissipation			9087.4		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: 4T4R - TDD 1F shared with RX TX 75%, RX 25%, FB 75% Single Band: 12x Int, FB 3x Dec, RX 6x Dec TX/FB Rate = 983.04 Msps RX Rate 491.52 Msps f_{DAC} = 11796.48 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 3.5 GHz f_{RX} =3.5 GHz 64/66 coding, 16.22Gbps TX: 8-8-2-1, FB: 4-4-4-2, RX: 4-8-4-1		821.8		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			808.5		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.4		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			289.5		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			682.0		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			49.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2123.3		mA
P_{diss}	Power Dissipation			6209.3		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 8: same configuration as mode 7, Sleep Mode. SLEEP pin is pull high.		20.3		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			292.8		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			12.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			4.6		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			54.3		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			15.3		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			313.1		mA
P_{diss}	Power Dissipation			956.8		mW

Copyright © 2023 Texas Instruments Incorporated

5.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 9: 4T4R2F - FDD FB 100% on TX Single Band: 24x Int, FB 12x Dec RX Single Band: RX 24x TX/FB Rate 245.76 Msps RX Rate 122.88 Msps f_{DAC} = 5898.24 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 0.85 GHz f_{RX} = 0.8 GHz 8/10 coding, 9.8304Gbps TX: 4-8-4-1, FB: 2-4-4-1, RX: 2-8-8-1		1593.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			840.6		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			77.3		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			905.0		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			817.7		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			52.1		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2405.2		mA
P_{diss}	Power Dissipation			8814.3		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 10: 4T4R2F - FDD FB 100% on TX Single Band: 18x Int, FB 6x Dec RX Single Band: RX 12x TX/FB Rate 491.52 Msps RX Rate 245.76 Msps f_{DAC} = 8847.36 MSPS f_{ADC} = 2949.12 MSPS f_{TX} = 1.85 GHz f_{RX} = 1.75 GHz 8/10 coding, 9.8304Gbps TX: 8-8-2-1, FB: 4-4-2-1, RX: 4-8-4-1		1626.2		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			976.4		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			74.6		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			902.7		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			1111.9		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			48.0		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3578.9		mA
P_{diss}	Power Dissipation			10515.0		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11a: TDD 4T1FB (RX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS f_{TX} = f_{RX} = 3.7 GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		797		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			817		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73.2		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			179		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			906		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.5		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2483		mA
P_{diss}	Power Dissipation			6754		mW

Copyright © 2023 Texas Instruments Incorporated

5.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11b: TDD 4R (TX in Standby) Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS f_{TX} = f_{RX} = 3.7 GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		726		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			876		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			72.8		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			270		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			71.6		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2130		mA
P_{diss}	Power Dissipation			6124		mW

Copyright © 2023 Texas Instruments Incorporated

5.9 Power Supply Electrical Characteristics (continued)

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 737.28MSPS, f_{DAC} = 8847.36MSPS interleave mode; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11c: TDD 4T4R1FB average TX/FB: 75%, RX 25% Single Band: 8x Int, FB 2x Dec, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS f_{TX} = f_{RX} = 3.7 GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		779		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			832		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73.1		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			280		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			747		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			70.8		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2395		mA
P_{diss}	Power Dissipation			6596		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 11d: FDD 4T4R Single Band: 8x Int, RX uses FB TX/FB/RX Rate = 1474.56 Msps f_{DAC} = 11796.48 MSPS, interleave mode, f_{ADC} = 2949.12 MSPS f_{TX} = f_{RX} = 3.7 GHz 64/66 coding, 24.33 Gbps TX: 8-8-2-1, FB/RX: 8-8-2-1		1236		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			915		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVCO			73.2		mA
I_{VDD1P2}	Group 2A: VDD1P2FB + VDD1P2RX			583		mA
	Group 2B: VDD1P2TXCLK + VDD1P2TXENC			923		mA
	Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF			72		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3097		mA
P_{diss}	Power Dissipation			8798		mW

Copyright © 2023 Texas Instruments Incorporated

5.10 Timing Requirements

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{s(SYSREF)}$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{h(SYSREF)}$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{s(SENB)}$	Setup Time, SENB to Rising Edge of SCLK		15		ns
$t_{h(SENB)}$	Hold Time, SENB after last Rising Edge of SCLK (1)		5 + t_{SCLK}		ns
$t_{s(SDIO)}$	Setup Time, SDIO valid to Rising Edge of SCLK		15		ns
$t_{h(SDIO)}$	Hold Time, SDIO valid after Rising Edge of SCLK		5		ns
$t_{(SCLK)_W}$	Minimum SCLK period: registers write		25		ns
$t_{(SCLK)_R}$	Minimum SCLK period: registers read		50		ns
$t_{d(data_out)}$	Minimum Data Output delay after Falling Edge of SCLK		0		ns
	Maximum Data Output delay after Falling Edge of SCLK		15		ns
t_{RESET}	Minimum RESETZ Pulse Width		1		ms

(1) SDEN\\ need to be held one more extra clock cycle with the last SCLK edge

Copyright © 2023 Texas Instruments Incorporated

5.11 Switching Characteristics

Typical values at T_A = +25°C, full temperature range is $T_{A,MIN}$ = -40°C to $T_{J,MAX}$ = +110°C; TX Input Rate = 491.52MSPS, f_{DAC} = 8847.36MSPS; f_{ADC} = 2949.12MSPS; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t_{JESDTX}	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles(1)
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t_{JESDRX}	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles(1)
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)		118		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t_{JESDFB}	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles(1)
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

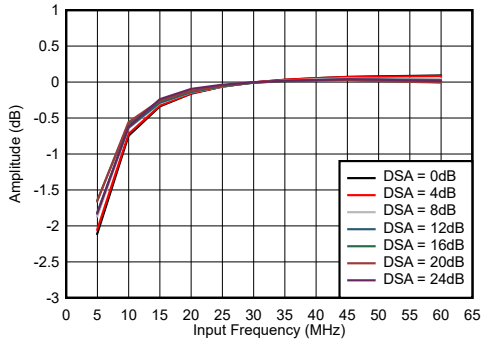
(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

Copyright © 2023 Texas Instruments Incorporated

5.12 Typical Characteristics

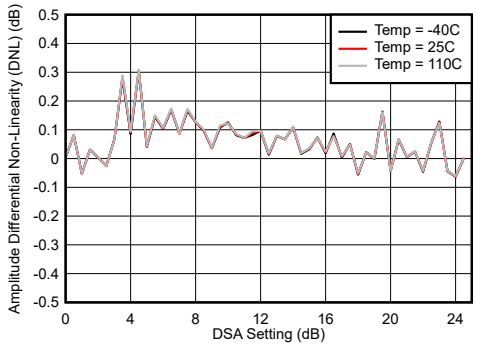
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



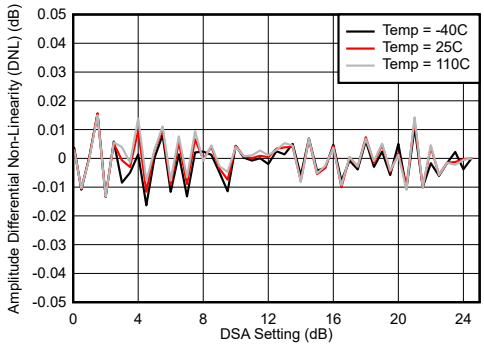
Normalized to 30 MHz

図 5-1. RX In-Band Gain Flatness, f_{IN} = 30 MHz



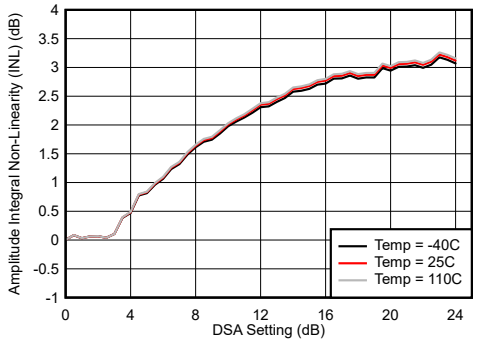
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



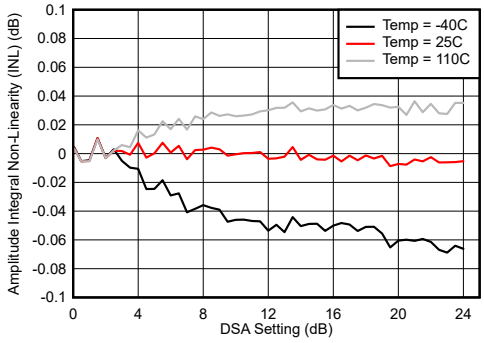
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz



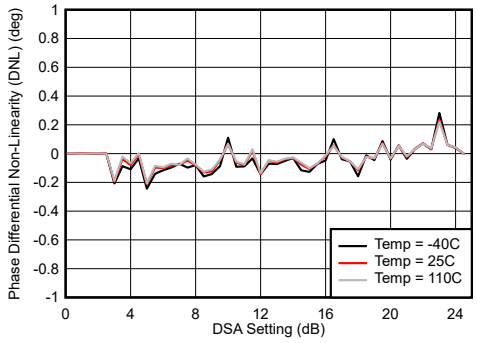
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



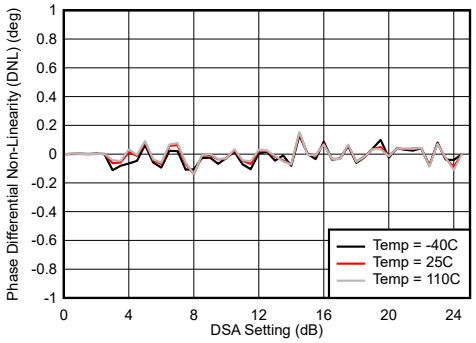
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

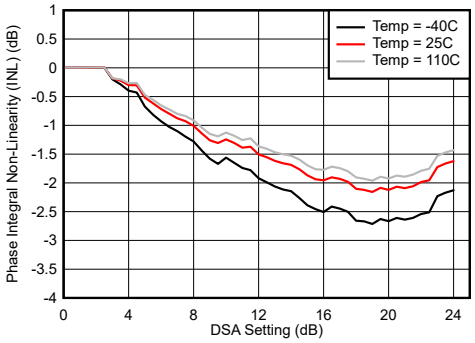
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



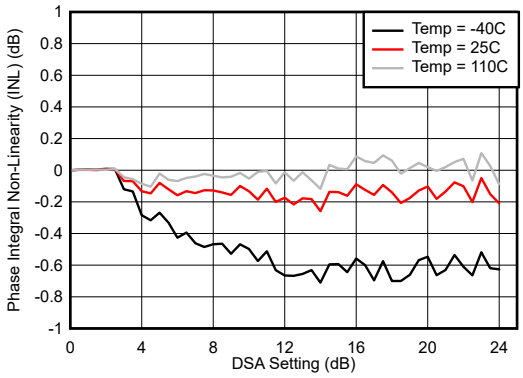
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz



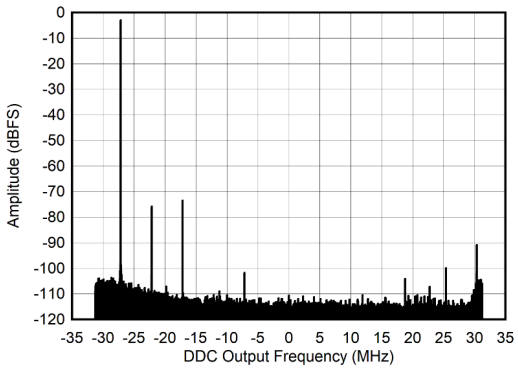
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz



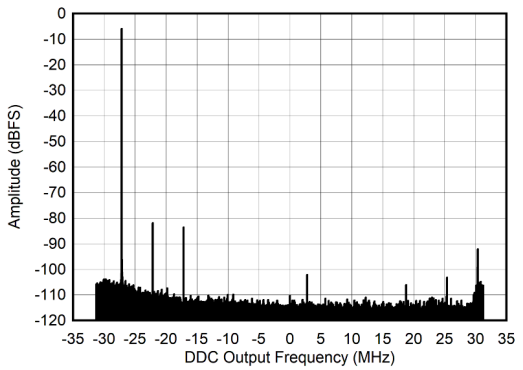
With 0.8 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz



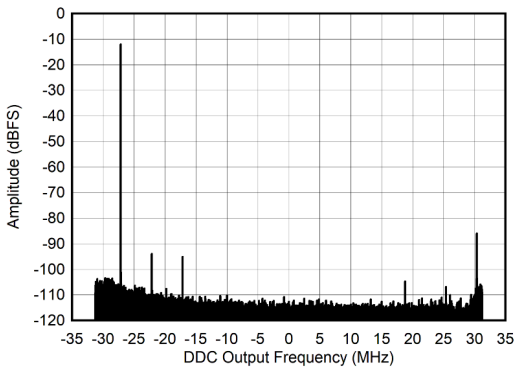
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-10. RX Output FFT at 5 MHz



A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 5-11. RX Output FFT at 5 MHz



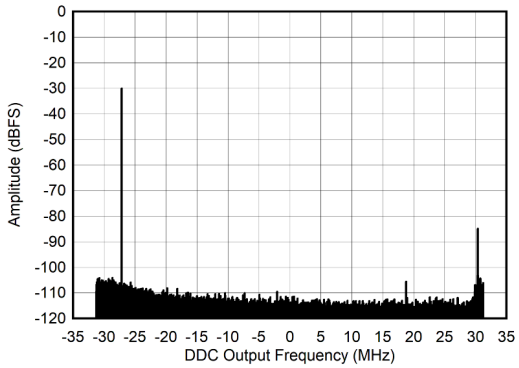
A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-12. RX Output FFT at 5 MHz

Copyright © 2023 Texas Instruments Incorporated

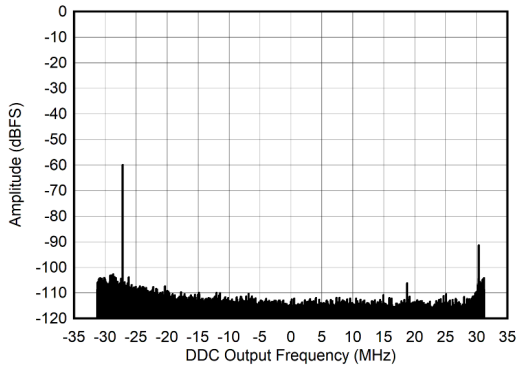
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



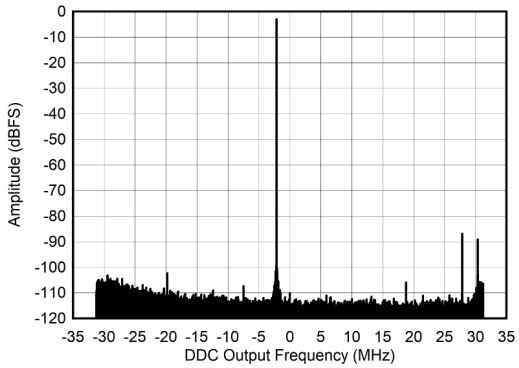
A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-13. RX Output FFT at 5 MHz



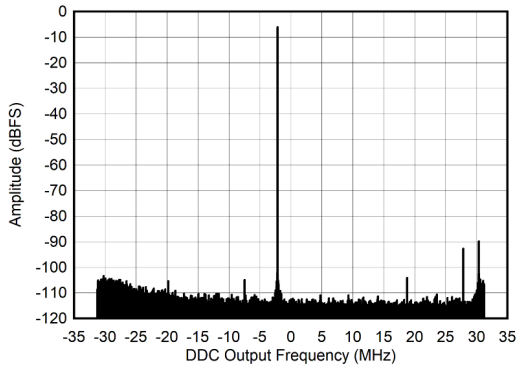
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-14. RX Output FFT at 5 MHz



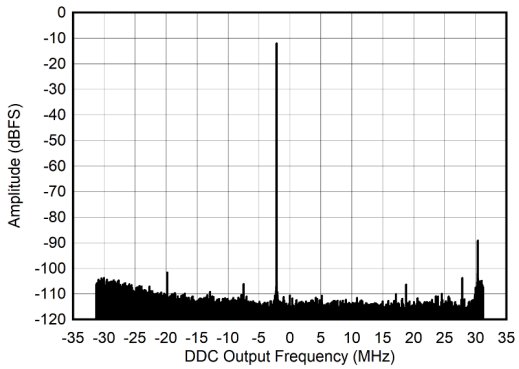
A_{IN} = -3 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-15. RX Output FFT at 30 MHz



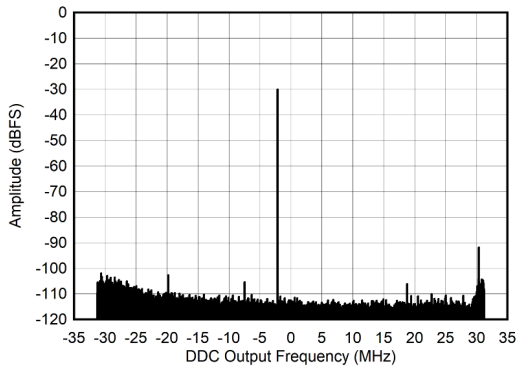
A_{IN} = -6 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-16. RX Output FFT at 30 MHz



A_{IN} = -12 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-17. RX Output FFT at 30 MHz



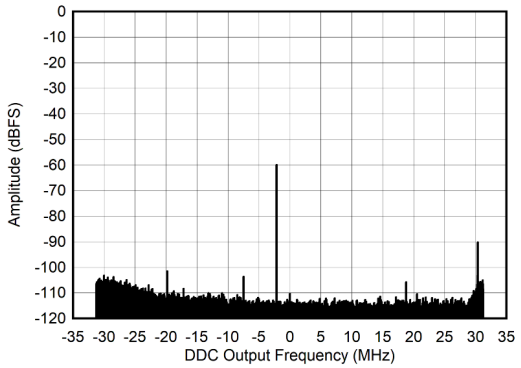
A_{IN} = -30 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-18. RX Output FFT at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

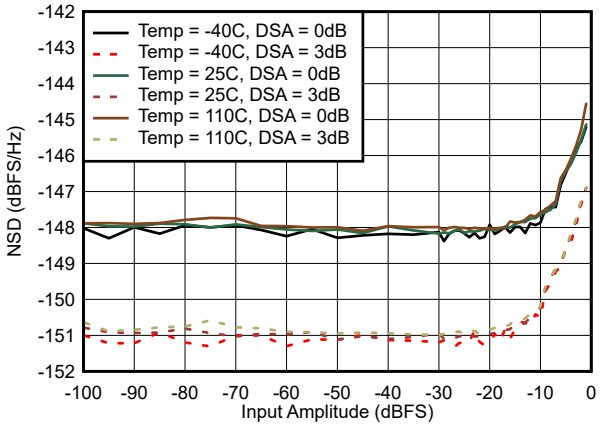
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



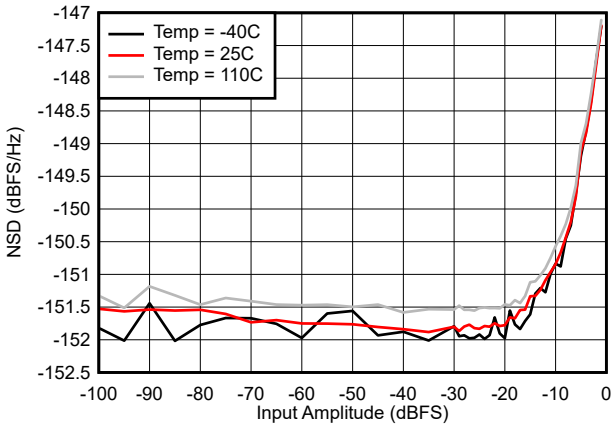
A_{IN} = -60 dBFS, f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-19. RX Output FFT at 30 MHz



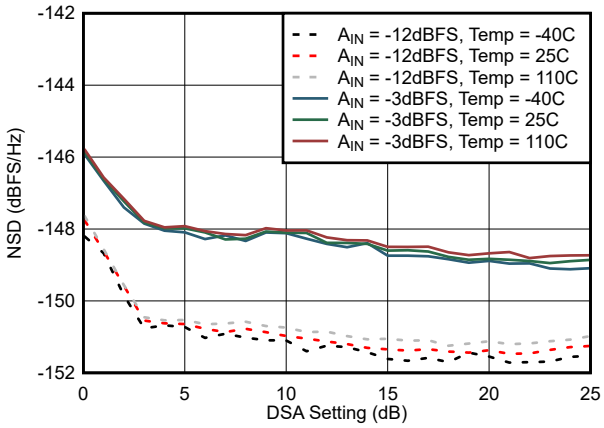
f_{ADC} = 1500MSPS, f_{NCO} = 32.13MHz, Decimate by 24x

図 5-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-21. NSD vs Input Amplitude at 30 MHz with DSA = 12

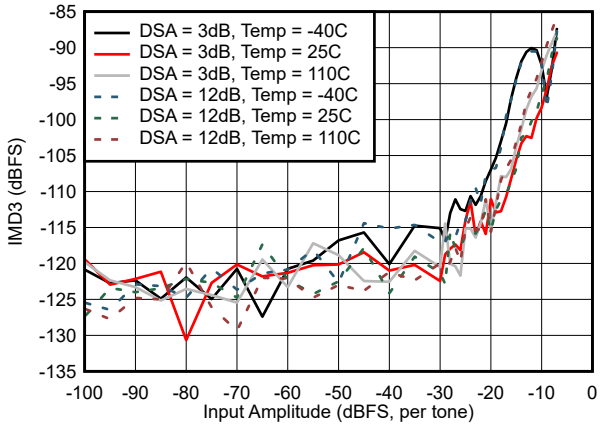


f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-22. NSD vs DSA Attenuation at 30 MHz

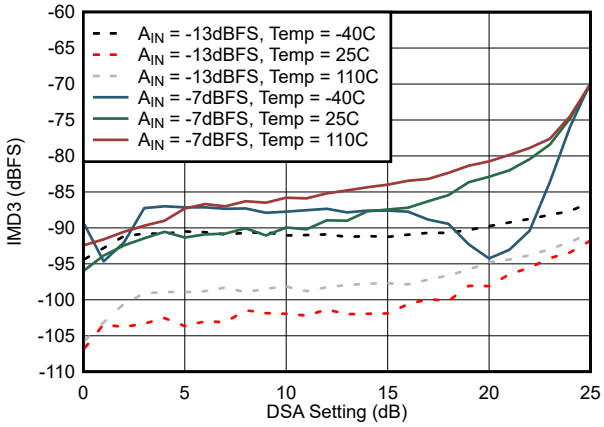
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



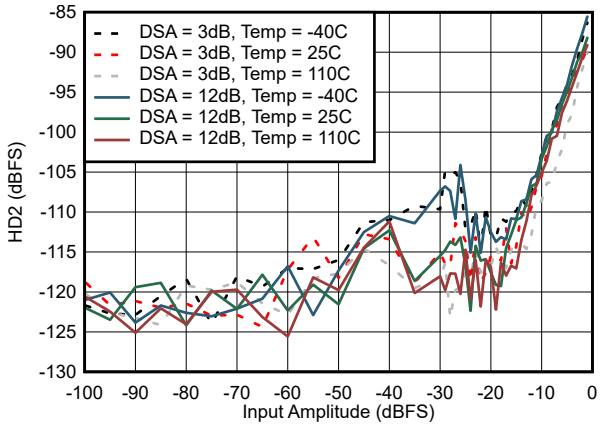
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-23. IMD3 vs Input Amplitude at 30 MHz



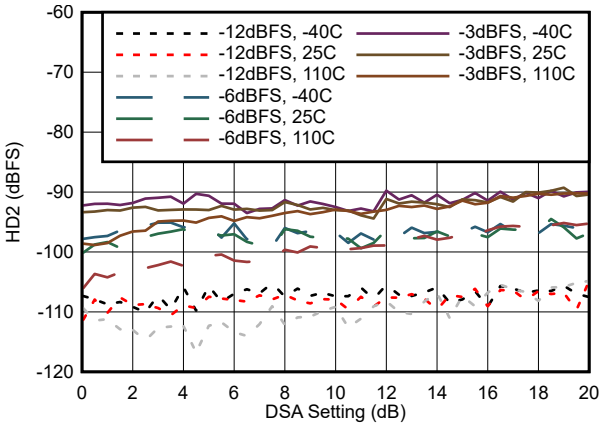
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-24. IMD3 vs DSA Setting at 30 MHz



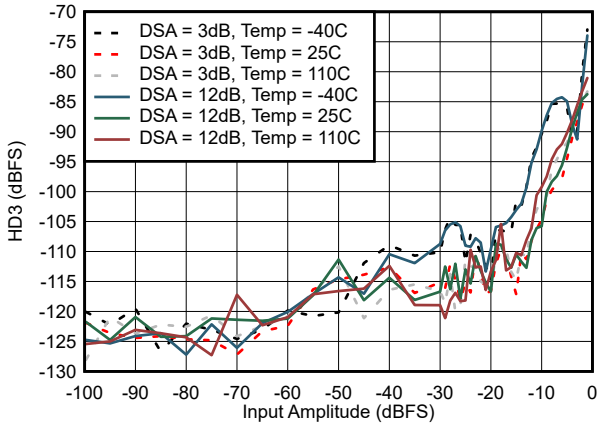
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-25. HD2 vs Input Amplitude at 30 MHz



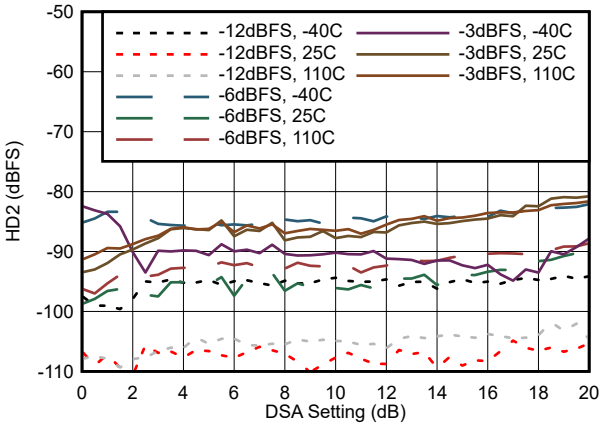
f_{ADC} = 1500 MSPS, f_{NCO} = 32. , Decimate by 24x

図 5-26. HD2 vs DSA Setting at 30 MHz



f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-27. HD3 vs Input Amplitude at 30 MHz



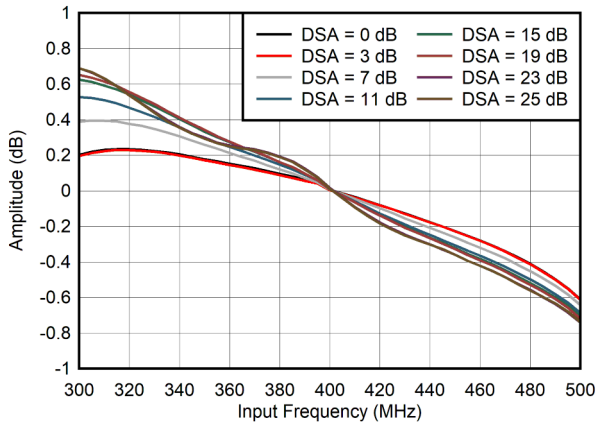
f_{ADC} = 1500 MSPS, f_{NCO} = 32.13 MHz, Decimate by 24x

図 5-28. HD3 vs DSA Setting at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

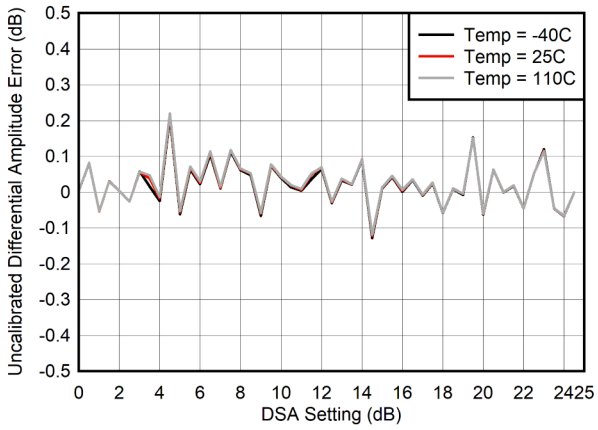
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



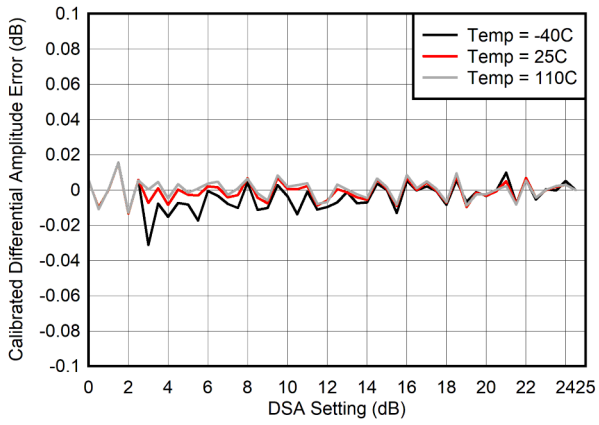
Normalized to 4000 MHz

図 5-29. RX In-Band Gain Flatness, f_{IN} = 400 MHz



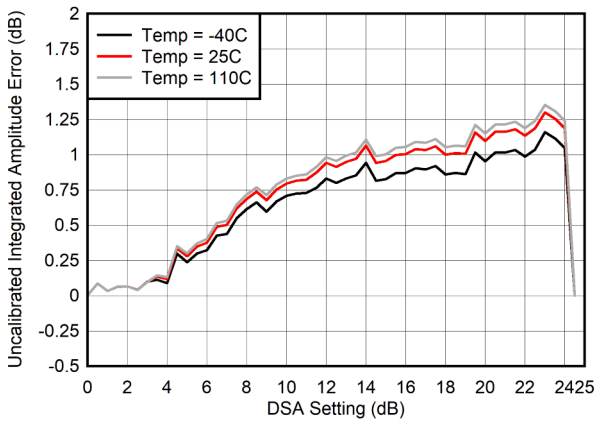
Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz



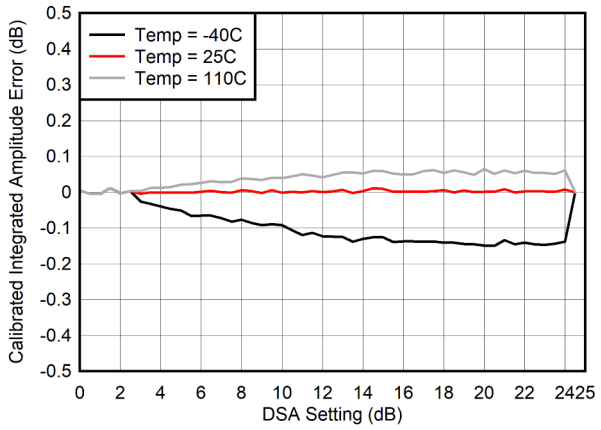
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

Copyright © 2023 Texas Instruments Incorporated

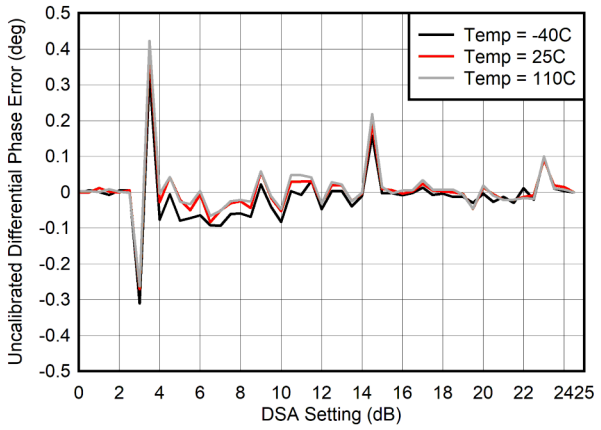
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



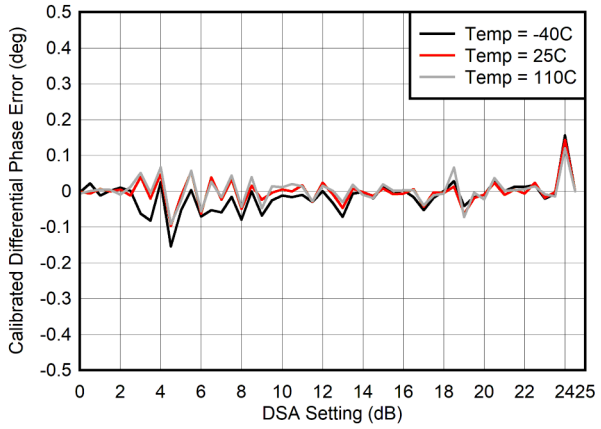
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



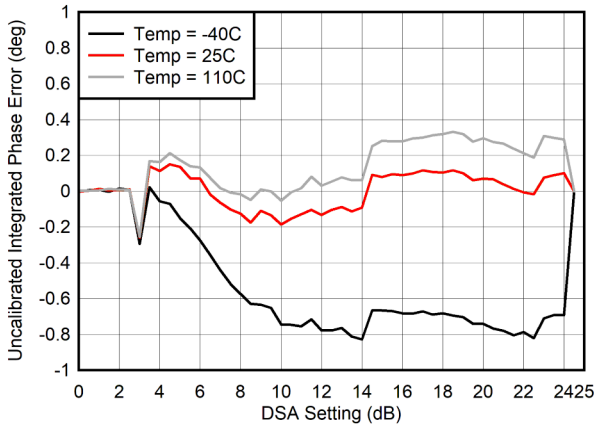
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz



Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz



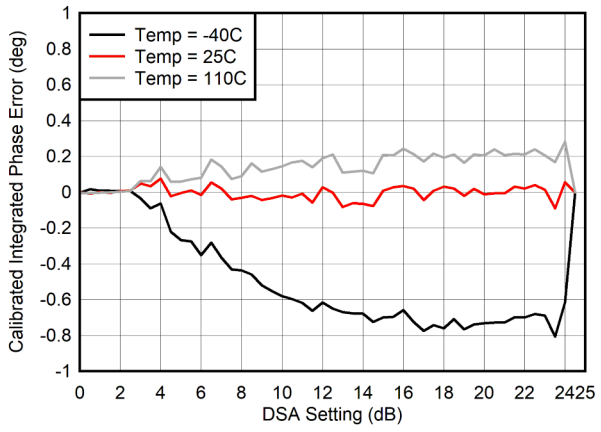
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz

Copyright © 2023 Texas Instruments Incorporated

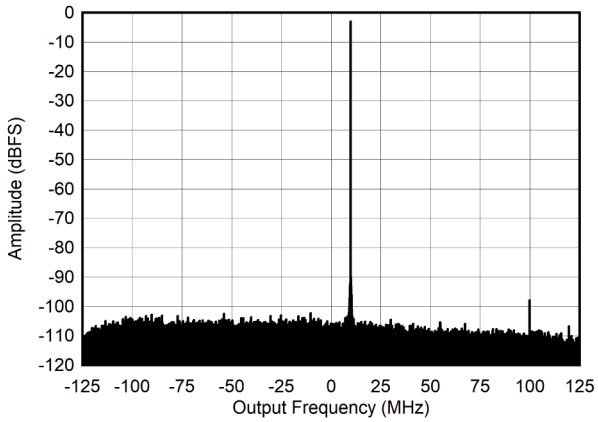
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



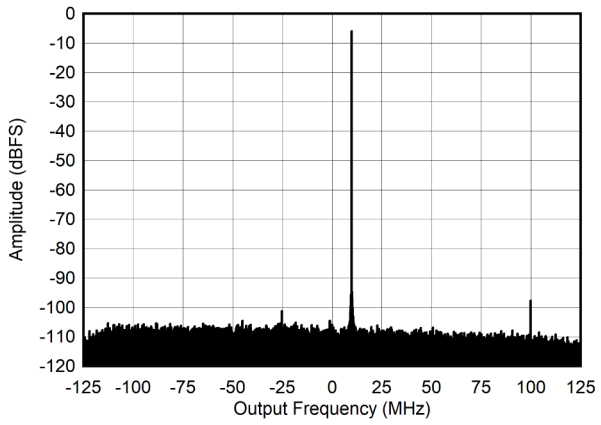
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz



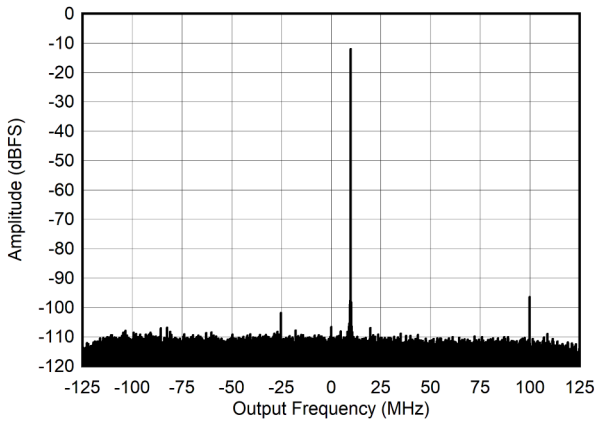
f_{NCO} = 400MHz

図 5-38. RX Output FFT at 405 MHz and -3dBFS



f_{NCO} = 400MHz

図 5-39. RX Output FFT at 405 MHz and -6dBFS

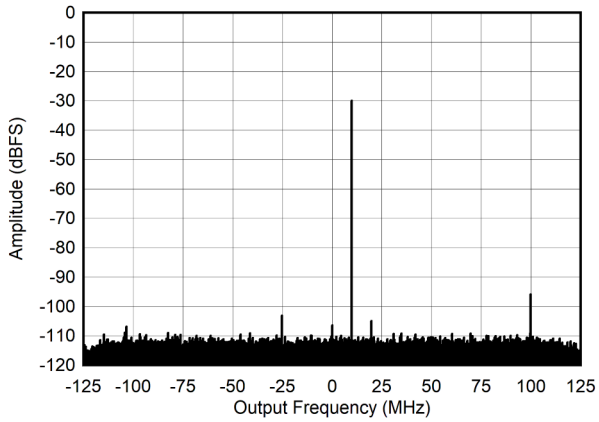


f_{NCO} = 400MHz

図 5-40. RX Output FFT at 405 MHz and -12dBFS

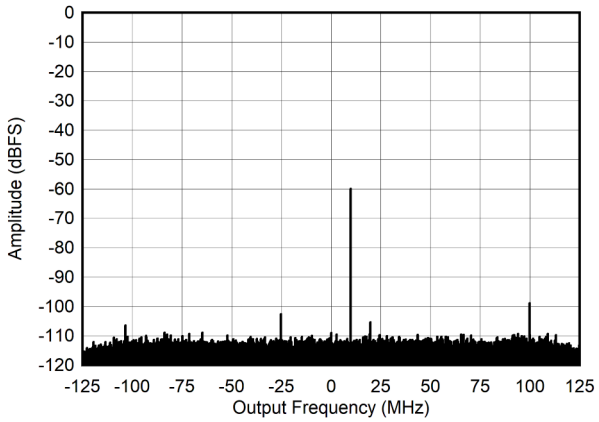
5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.



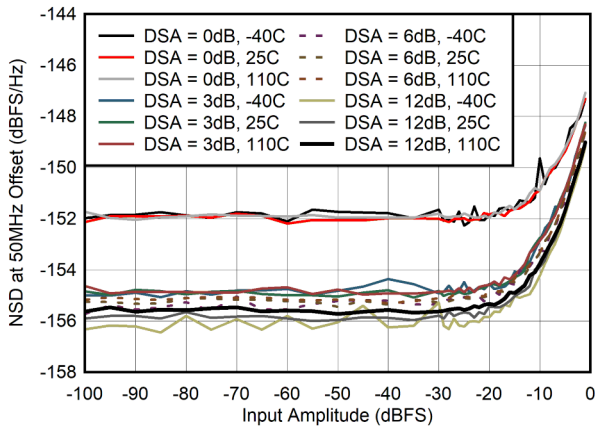
f_{NCO} = 400MHz

図 5-41. RX Output FFT at 405 MHz and -30dBFS



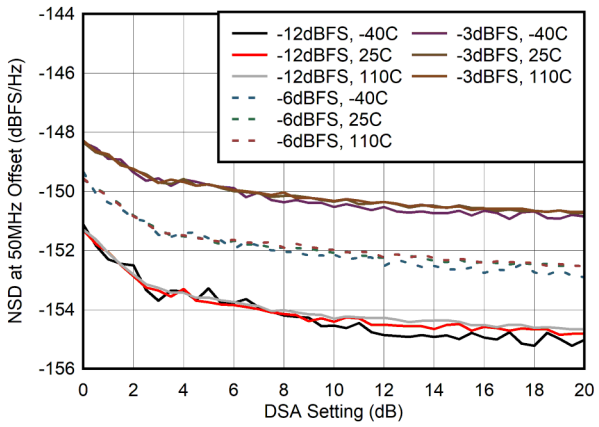
f_{NCO} = 400MHz

図 5-42. RX Output FFT at 405 MHz and -60dBFS



f_{OFFSET} = 50MHz

図 5-43. NSD vs Input Amplitude at 400MHz



f_{OFFSET} = 50MHz

図 5-44. NSD vs DSA Setting at 400MHz

Copyright © 2023 Texas Instruments Incorporated

5.12.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at T_A = +25°C. Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with f_{REF} = 500 MHz, A_{IN} = –3 dBFS, DSA setting = 3 dB.

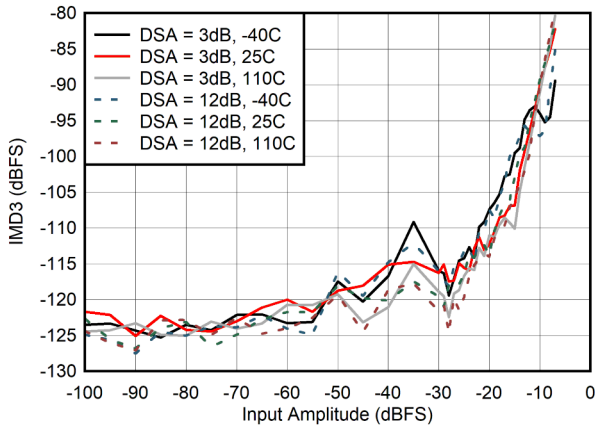


図 5-45. IMD3 vs Input Amplitude at 400MHz

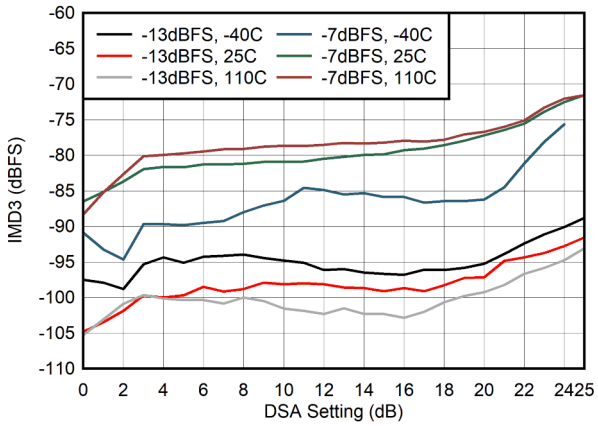


図 5-46. IMD3 vs DSA Setting at 400MHz

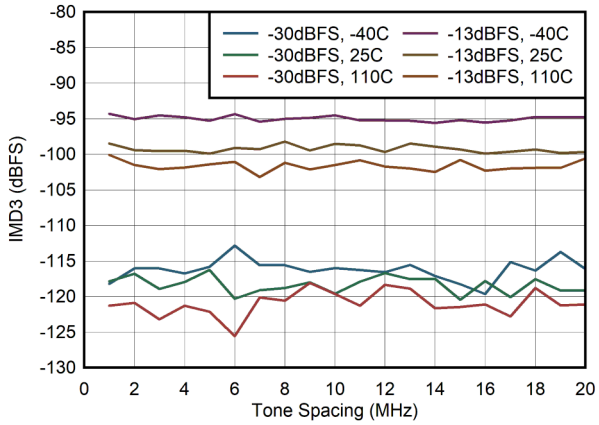


図 5-47. IMD3 vs Tone Spacing at 400MHz

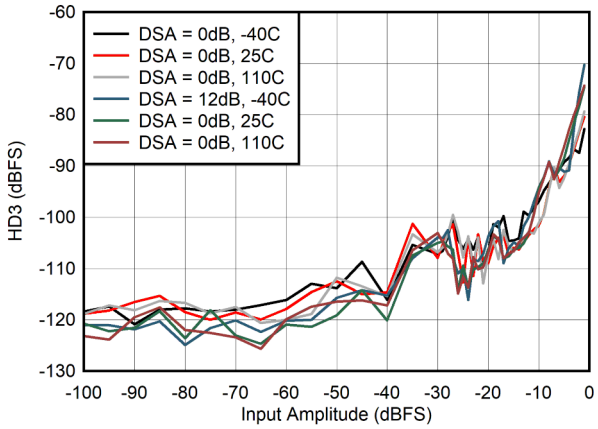


図 5-48. HD3 vs Input Amplitude at 400MHz

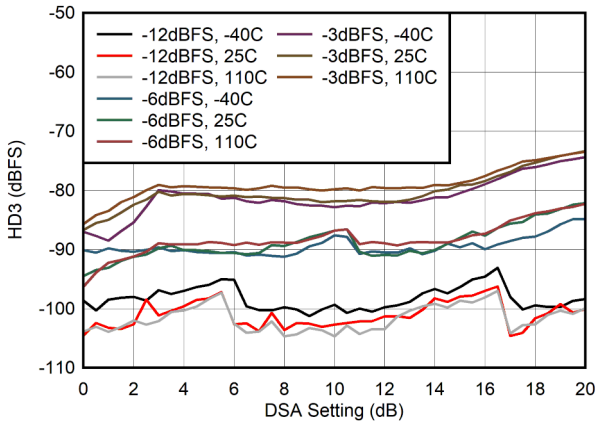
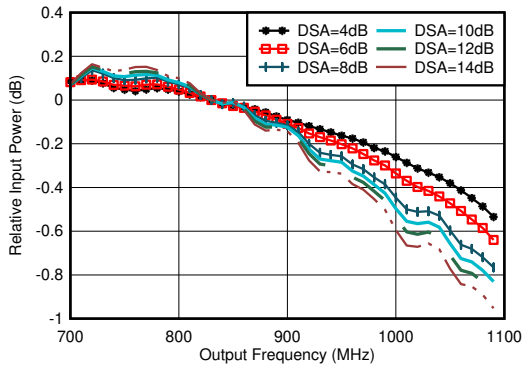


図 5-49. HD3 vs DSA Setting at 400MHz

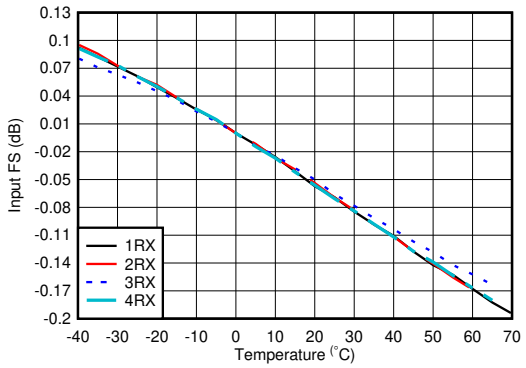
5.12.2 RX Typical Characteristics at 800MHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



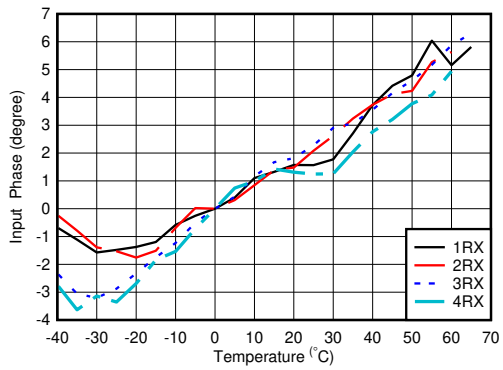
With 0.8 GHz matching, normalized to 830 MHz

図 5-50. RX In-Band Gain Flatness for Channel 1RX, f_{IN} = 830 MHz



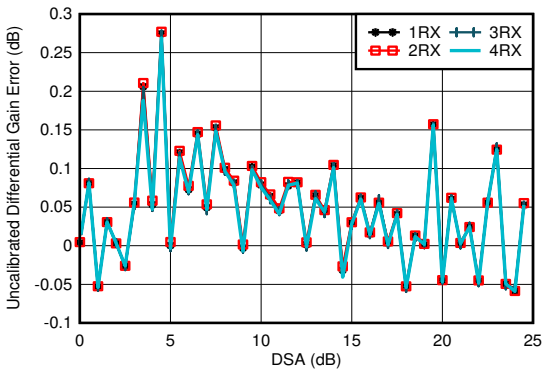
With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

図 5-51. RX Input Fullscale vs Temperature and Channel at 800MHz



With 0.8 GHz matching, normalized to phase at 25°C

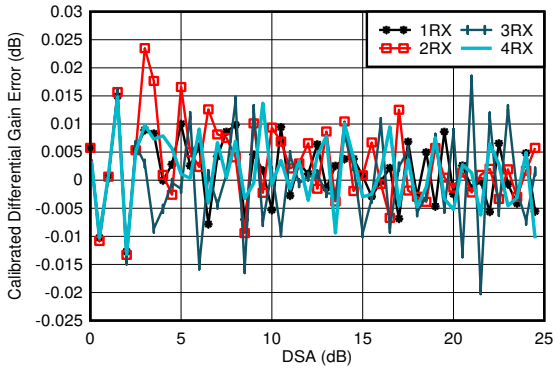
図 5-52. RX Input Phase vs Temperature and DSA at f_{OUT} = 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

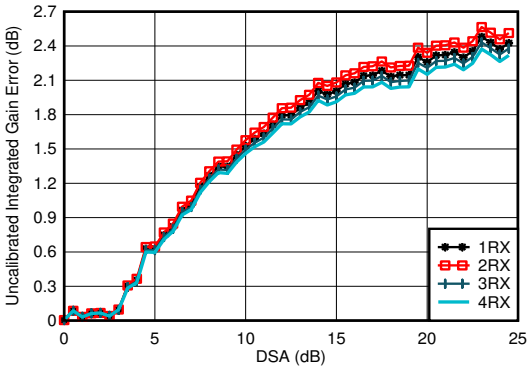
図 5-53. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-54. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

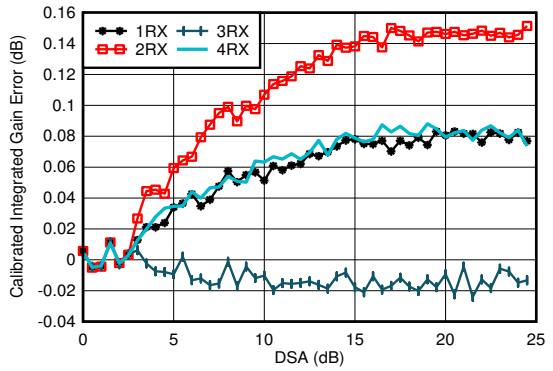
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-55. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.2 RX Typical Characteristics at 800MHz (continued)

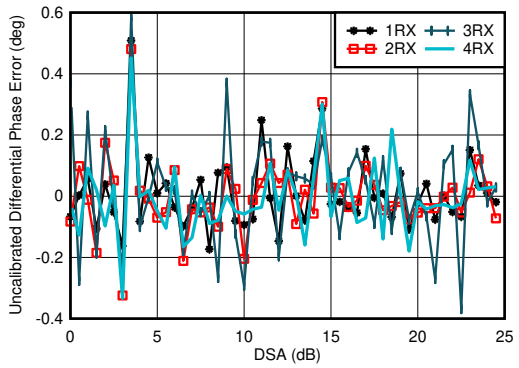
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

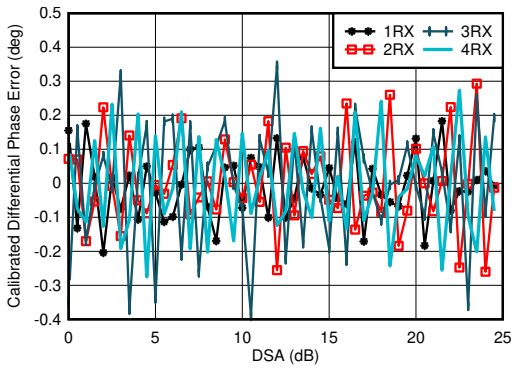
図 5-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

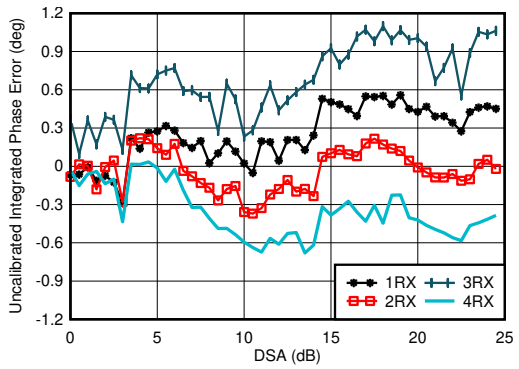
図 5-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



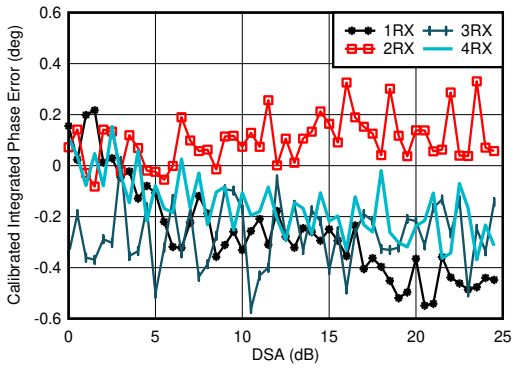
With 0.8 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

5.12.2 RX Typical Characteristics at 800MHz (continued)

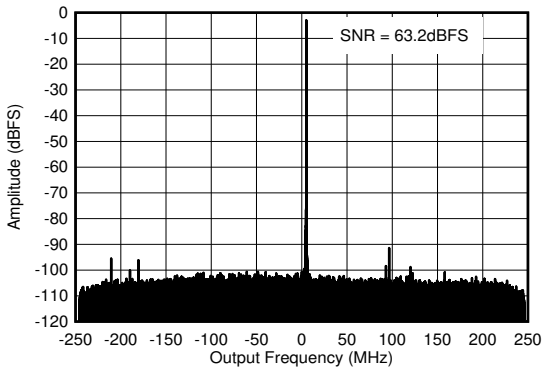
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 0.8 GHz matching

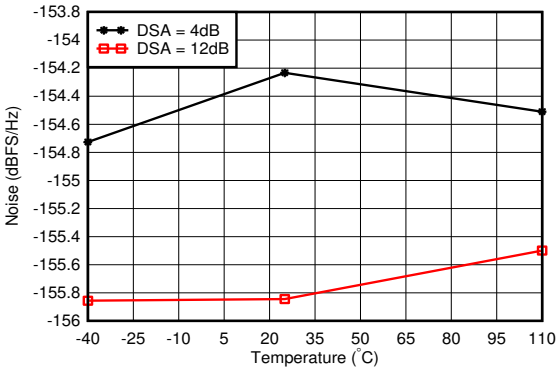
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-60. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



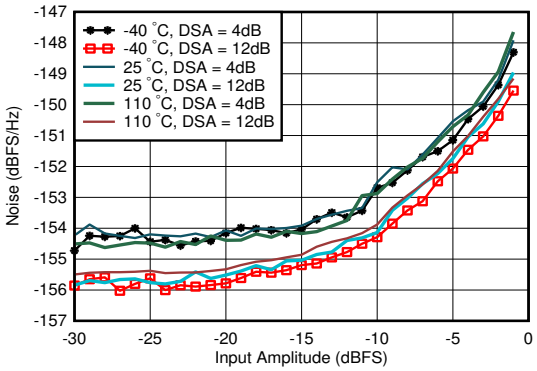
With 0.8 GHz matching, f_{IN} = 840 MHz, A_{IN}= –3 dBFS

図 5-61. RX Output FFT at 0.8 GHz



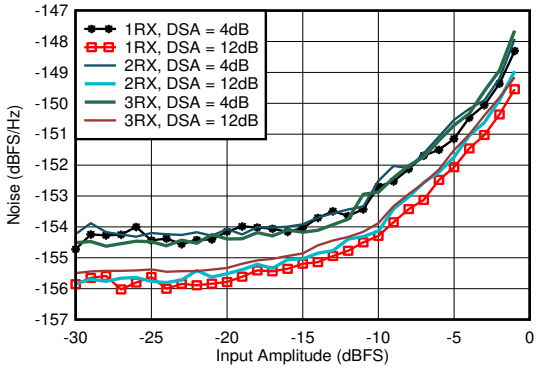
With 0.8 GHz matching, 12.5-MHz offset from tone

図 5-62. RX Noise Spectral Density vs Temperature at 0.8 GHz



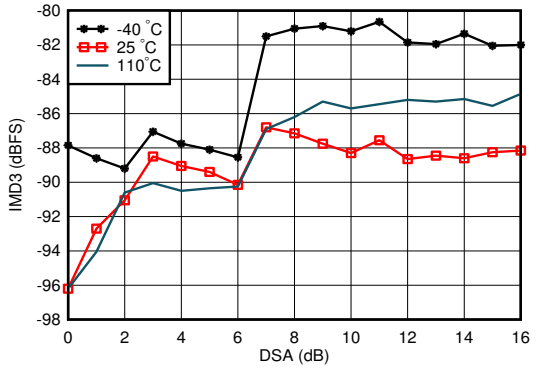
With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 5-63. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

図 5-64. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



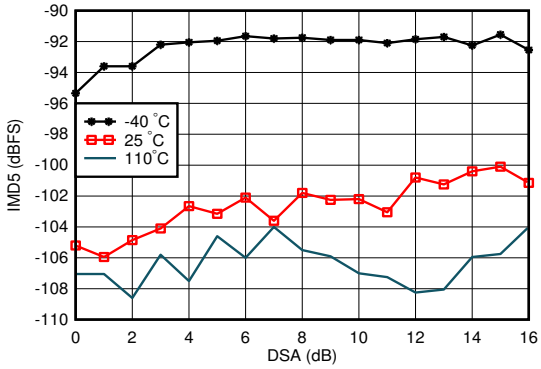
A. With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 5-65. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz

Copyright © 2023 Texas Instruments Incorporated

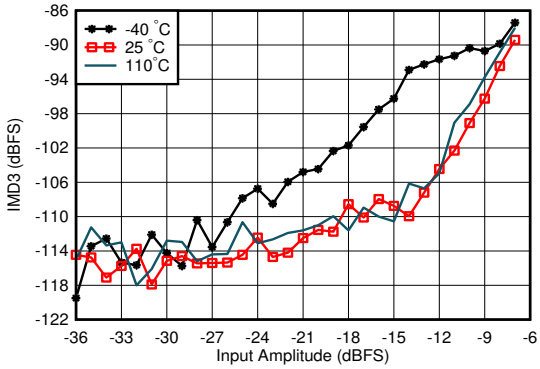
5.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



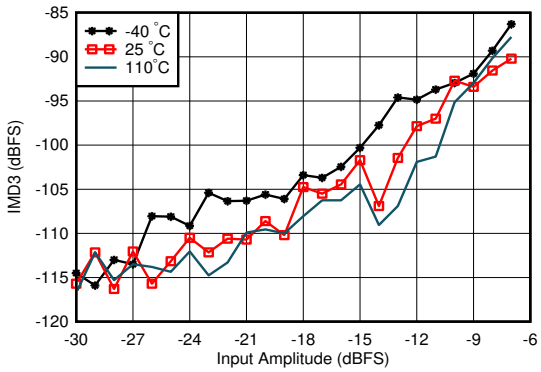
With 0.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 5-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



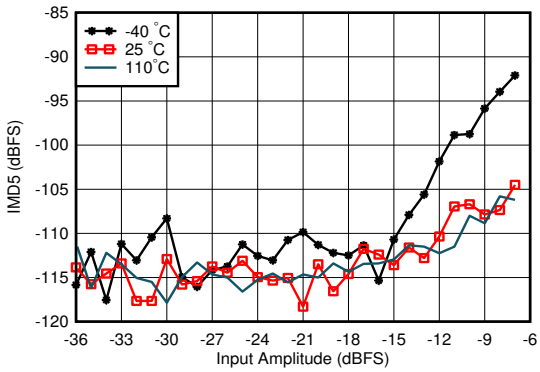
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 5-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz



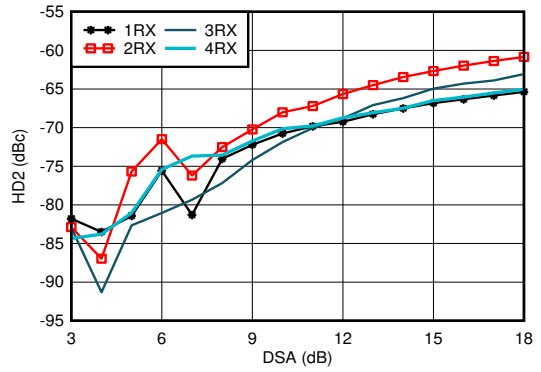
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 5-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



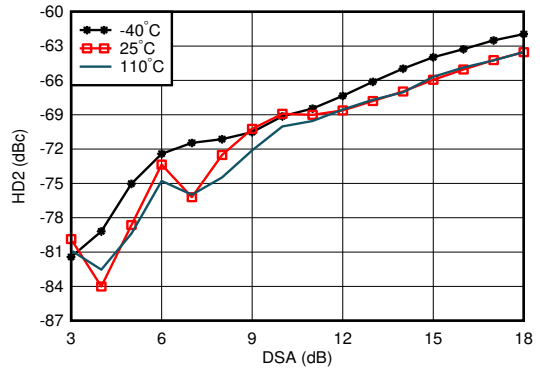
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 5-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz



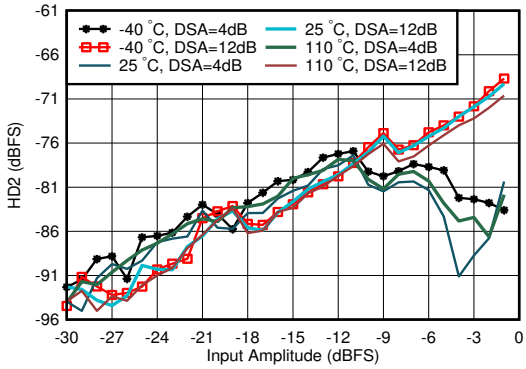
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz

Copyright © 2023 Texas Instruments Incorporated

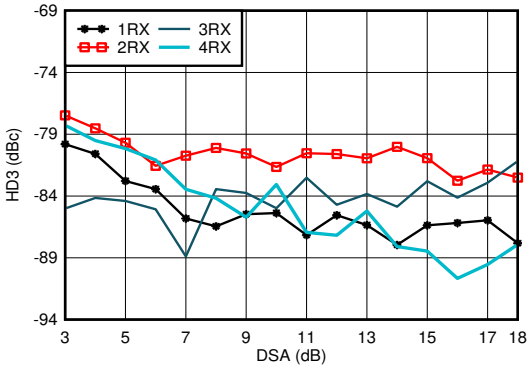
5.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



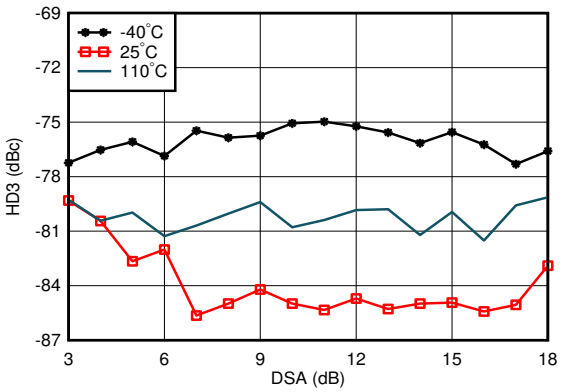
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-72. RX HD2 vs Input Level and Temperature at 0.8 GHz



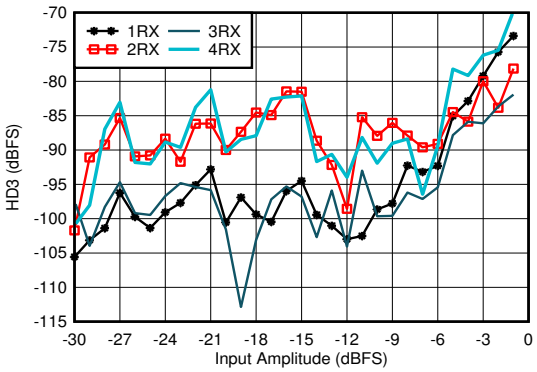
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz



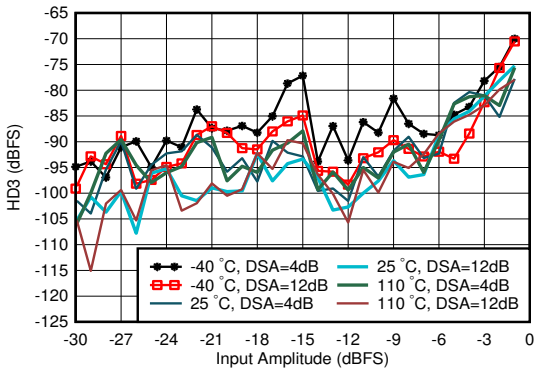
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



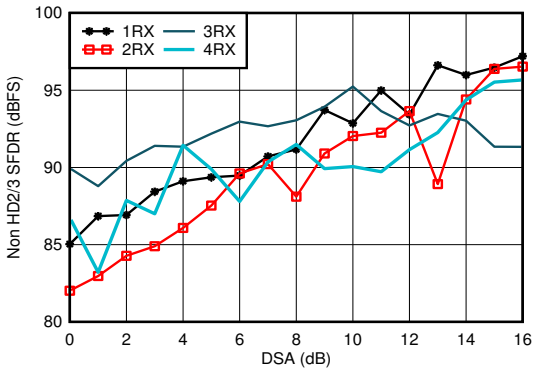
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-75. RX HD3 vs Input Level and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-76. RX HD3 vs Input Level and Temperature at 0.8 GHz



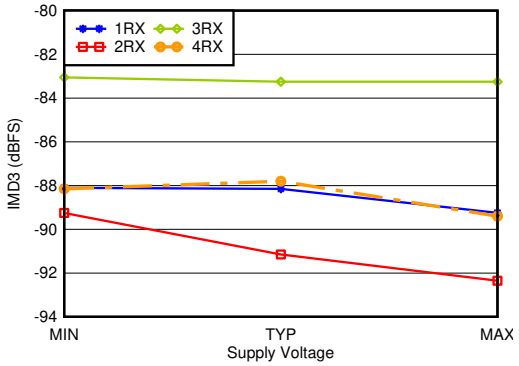
With 0.8 GHz matching

図 5-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz

Copyright © 2023 Texas Instruments Incorporated

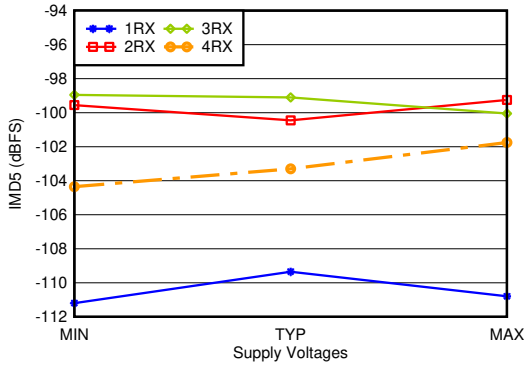
5.12.2 RX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



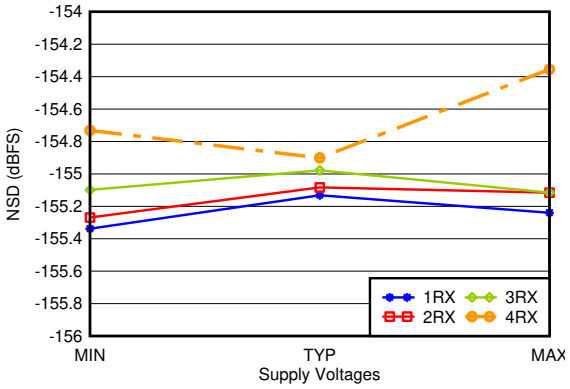
With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-78. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-79. RX IMD5 vs Supply and Channel at 0.8 GHz

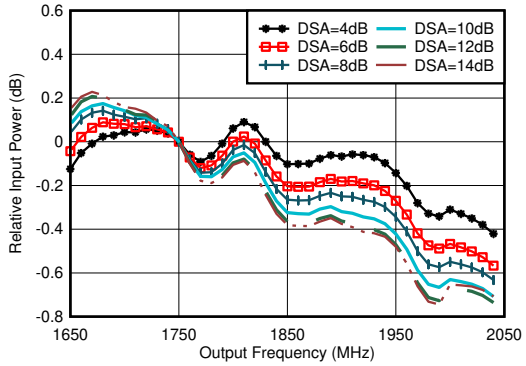


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

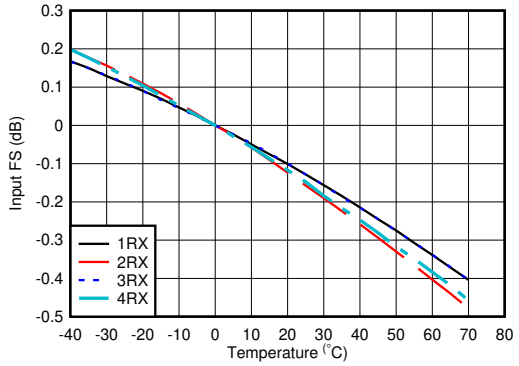
5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



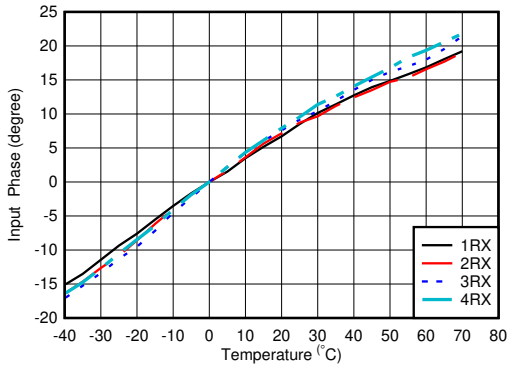
With 1.8 GHz matching, normalized to 1.75 GHz

図 5-81. RX In-Band Gain Flatness, f_{IN} = 1750 MHz



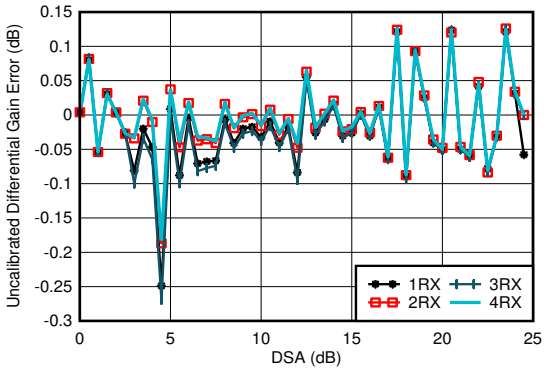
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

図 5-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

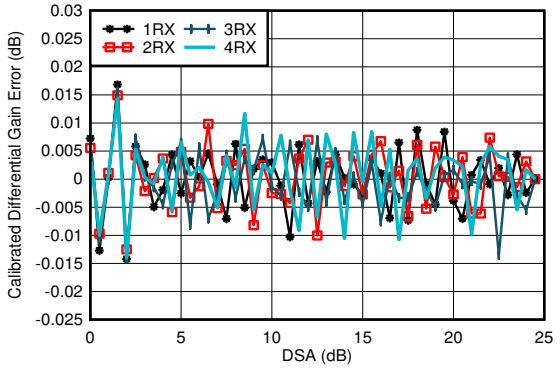
図 5-83. RX Input Phase vs Temperature and DSA at f_{IN} = 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

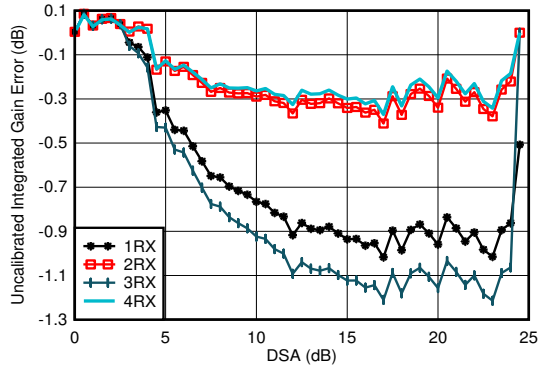
図 5-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

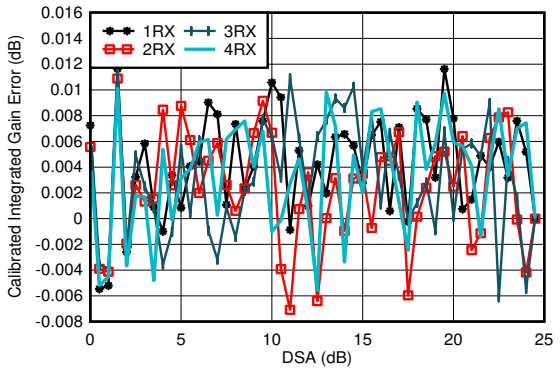
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

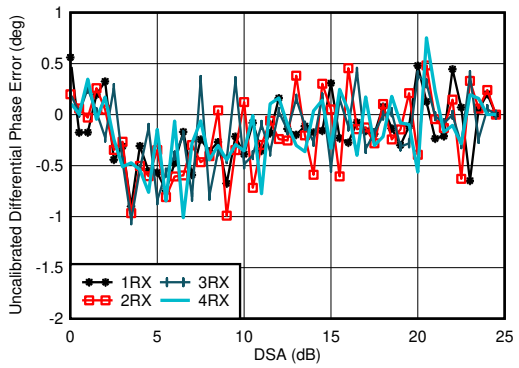
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

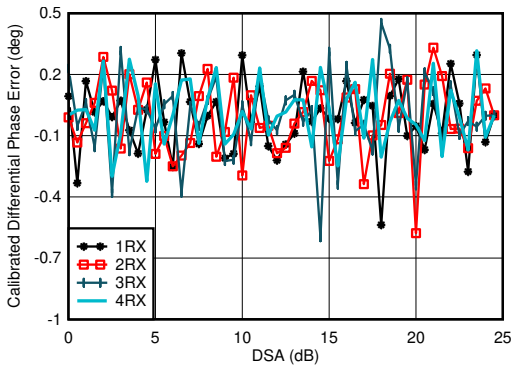
図 5-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

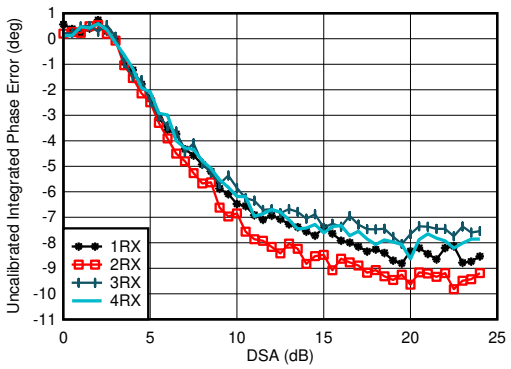
図 5-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

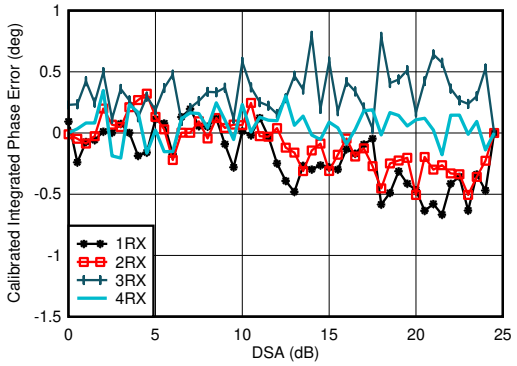
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

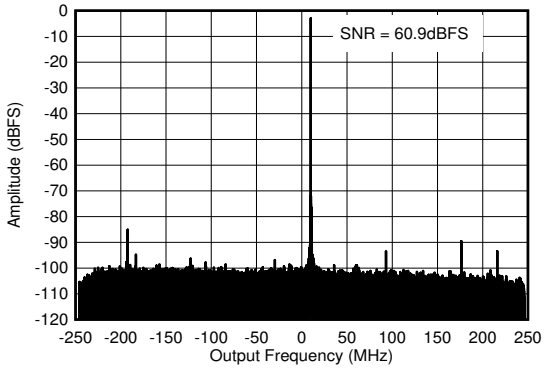
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching

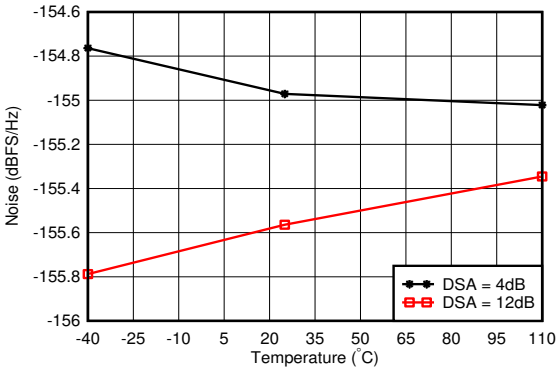
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-91. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



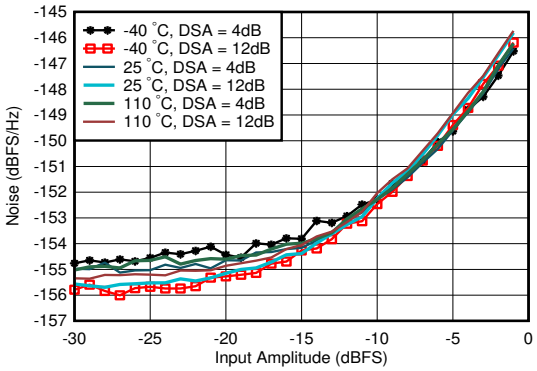
With 1.8 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 5-92. RX Output FFT at 1.75 GHz



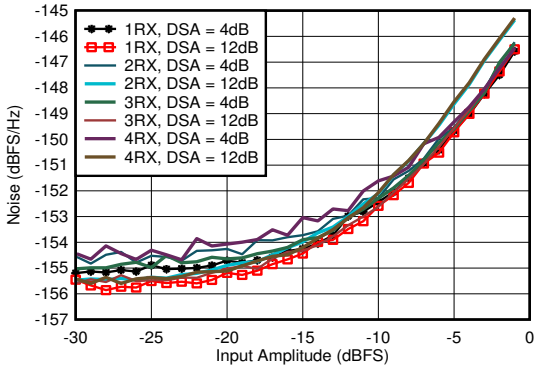
With 1.8 GHz matching, 12.5-MHz offset from tone

図 5-93. RX Noise Spectral Density vs Temperature at 1.75 GHz



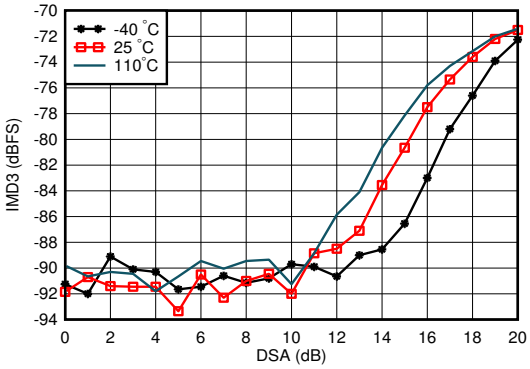
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 5-94. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



With 1.8 GHz matching, 12.5-MHz offset from tone

図 5-95. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



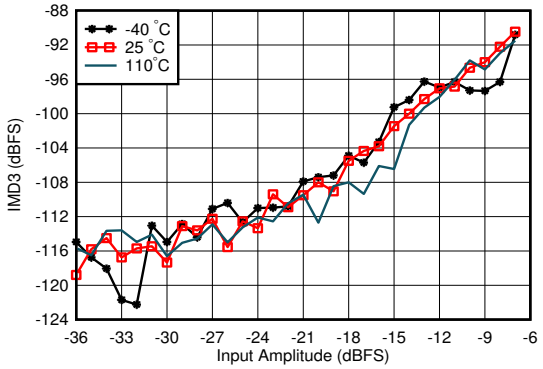
With 1.8 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 5-96. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz

Copyright © 2023 Texas Instruments Incorporated

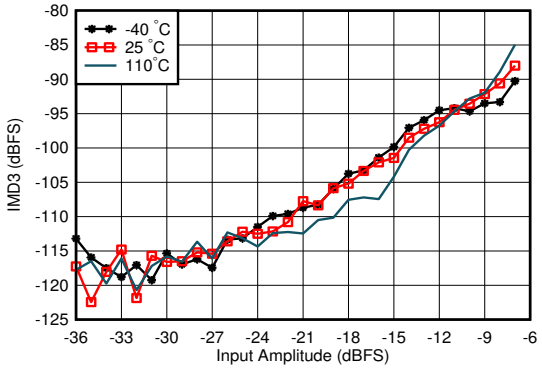
5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



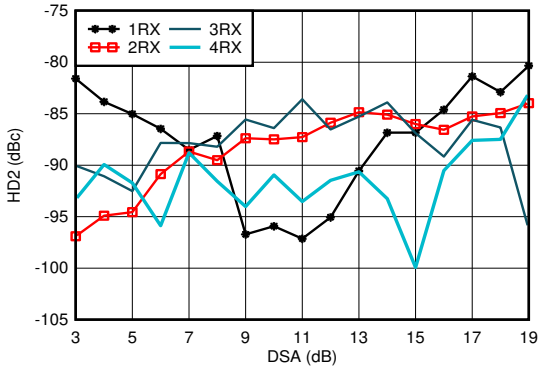
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 5-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz



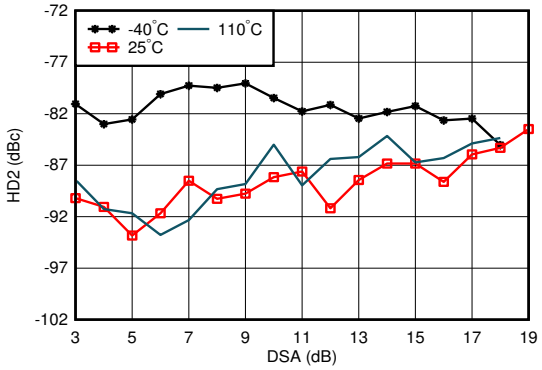
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 5-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz



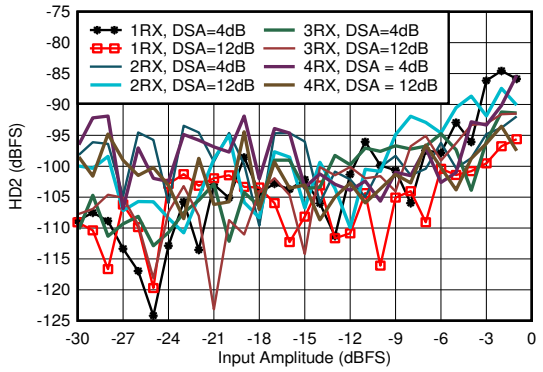
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



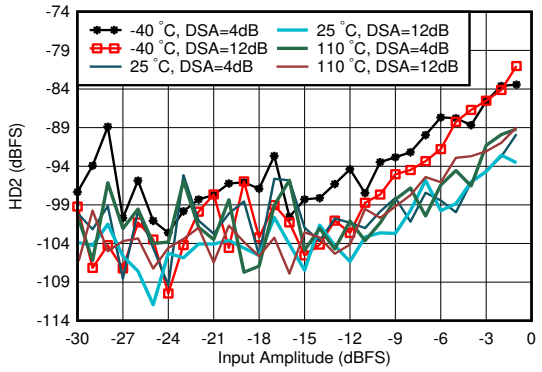
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



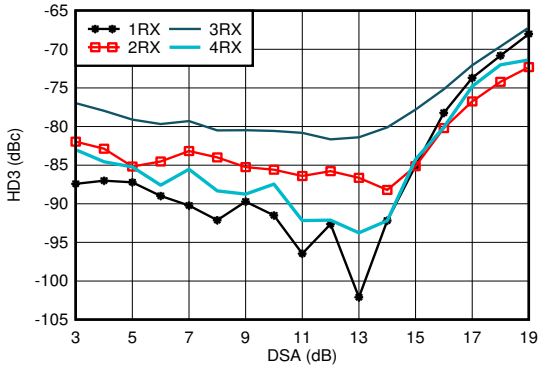
With 1.8 GHz matching, f_{in} = 1900MHz, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

Copyright © 2023 Texas Instruments Incorporated

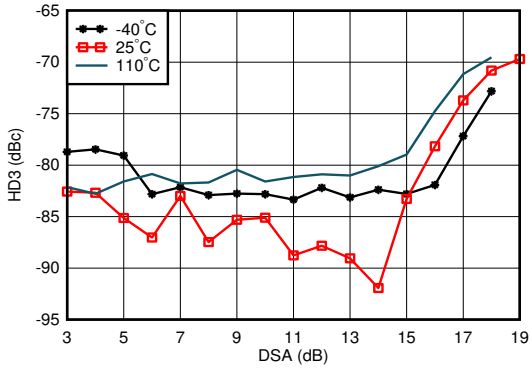
5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



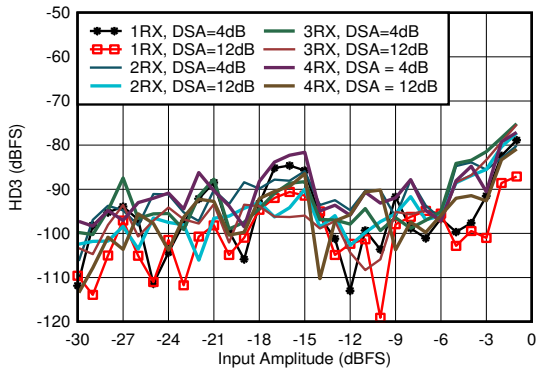
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 5-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz



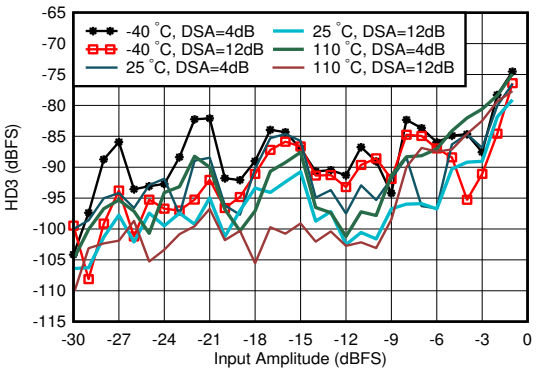
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 5-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



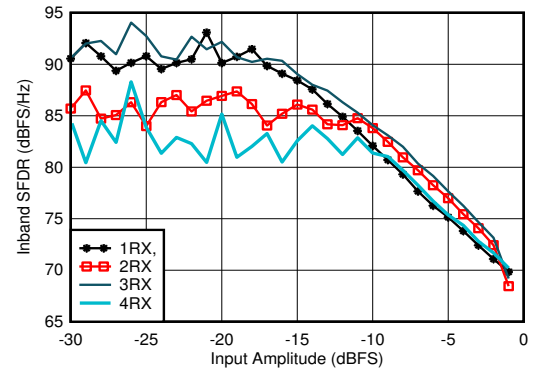
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 5-105. RX HD3 vs Input Level and Channel at 1.9 GHz



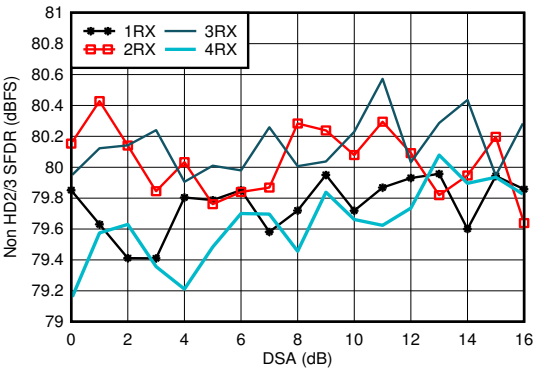
With 1.8 GHz matching, f_{in} = 1900MHz, DDC bypass mode (TI only mode for characterization)

図 5-106. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 3

図 5-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz



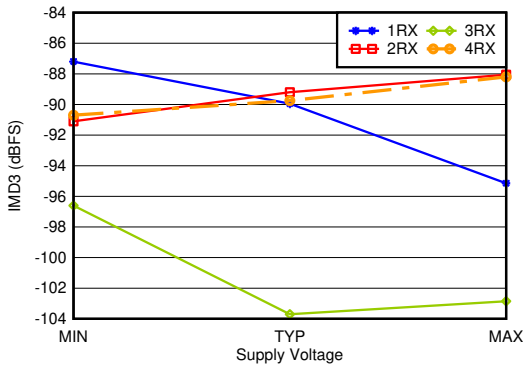
With 1.8 GHz matching

図 5-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz

Copyright © 2023 Texas Instruments Incorporated

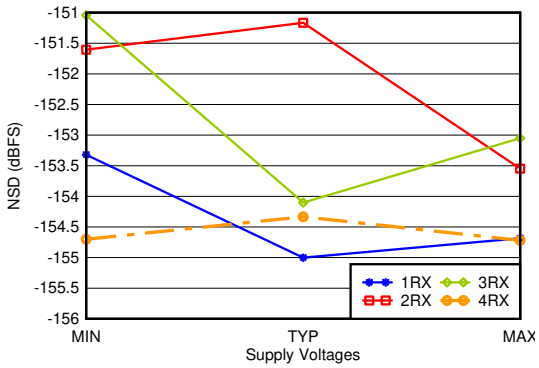
5.12.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 1.8 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-109. RX IMD3 vs Supply and Channel at 1.75 GHz

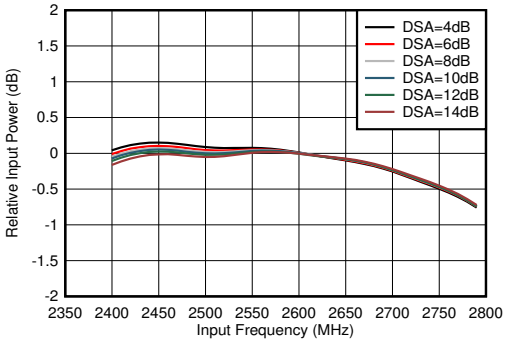


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-110. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

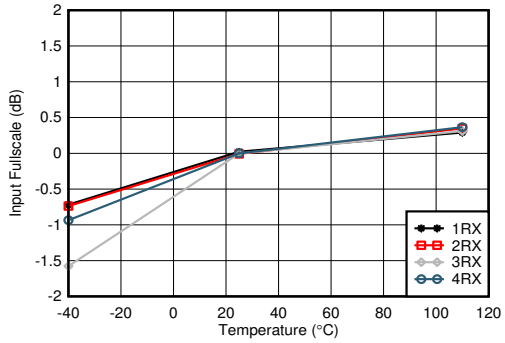
5.12.4 RX Typical Characteristics 2.6GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



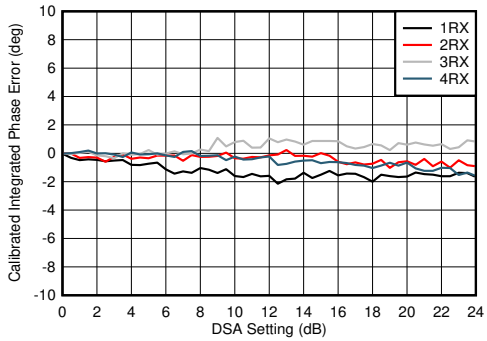
With matching, normalized to power at 2.6 GHz for each DSA setting

図 5-111. RX Inband Gain Flatness, f_{IN} = 2600 MHz



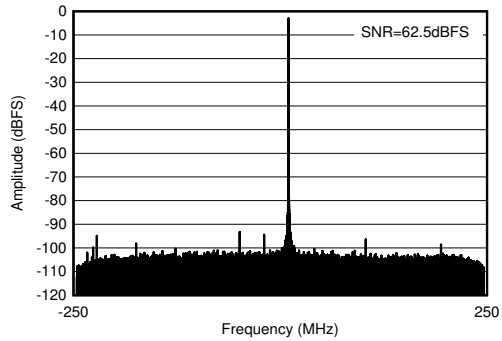
With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

図 5-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



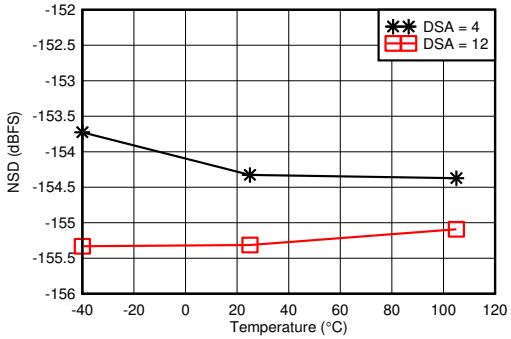
With 2.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



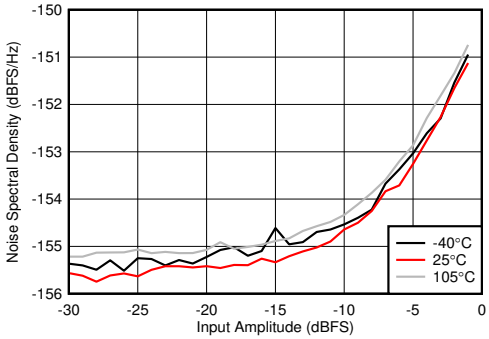
With 2.6 GHz matching, f_{IN} = 2610 MHz, A_{IN}= –3 dBFS

図 5-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

図 5-115. RX Noise Spectral Density vs Temperature at 2.6 GHz



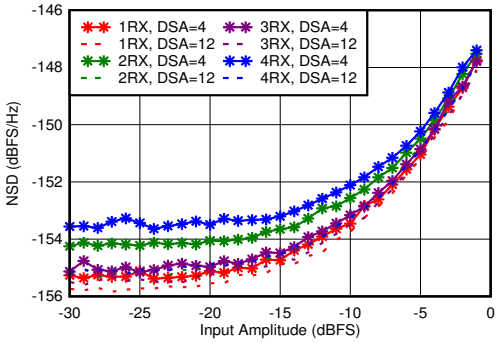
With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 5-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

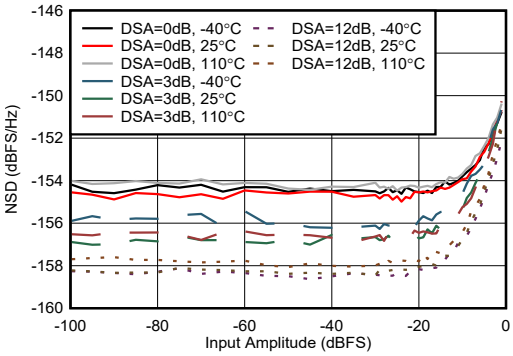
5.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



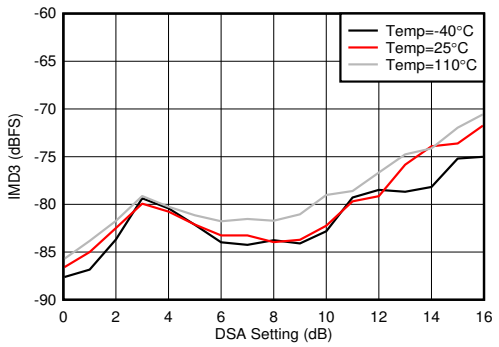
With 2.6 GHz matching, 12.5-MHz offset from tone

図 5-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



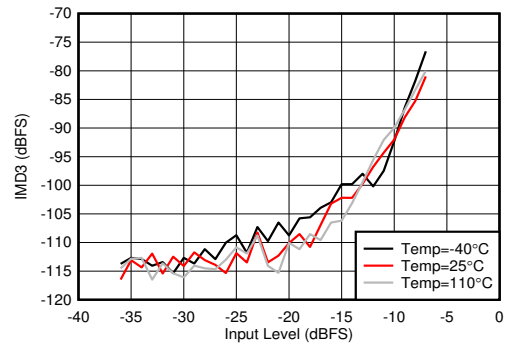
50-MHz offset from tone, external clock mode

図 5-118. RX Noise Spectral Density vs Input Amplitude at 2.61 GHz (Ext. Clock)



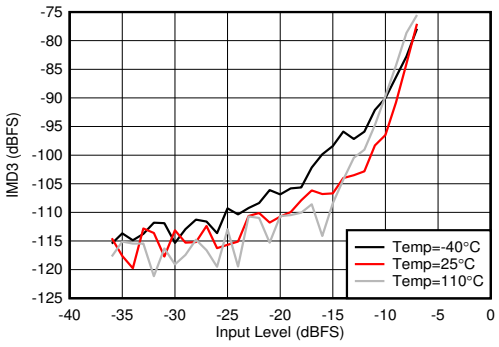
With 2.6 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 5-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



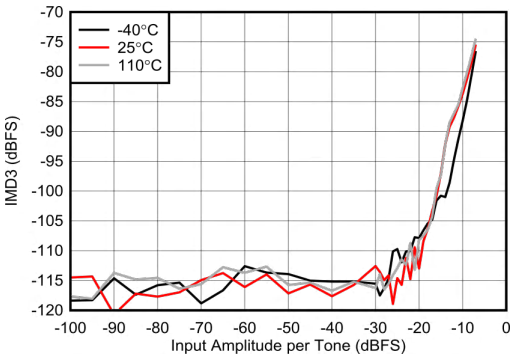
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 5-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 5-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz



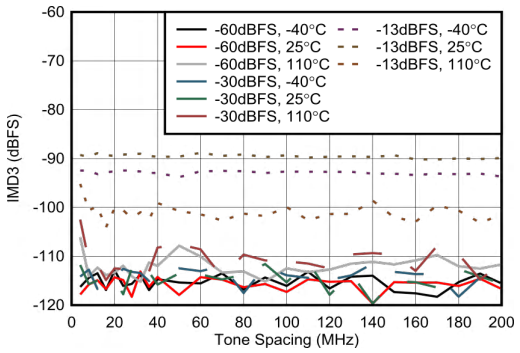
Tone spacing = 50 MHz, External clock mode

図 5-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

Copyright © 2023 Texas Instruments Incorporated

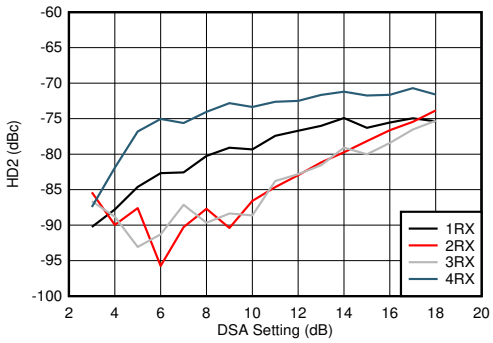
5.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



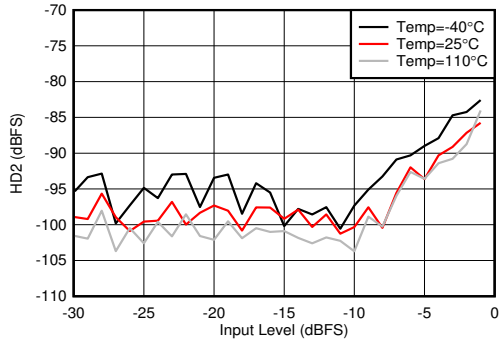
External clock mode

図 5-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



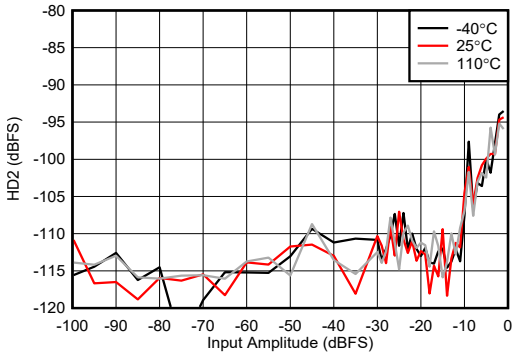
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



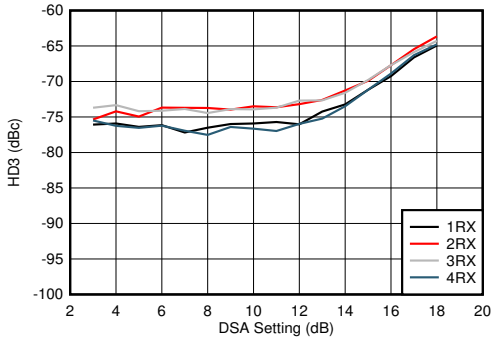
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



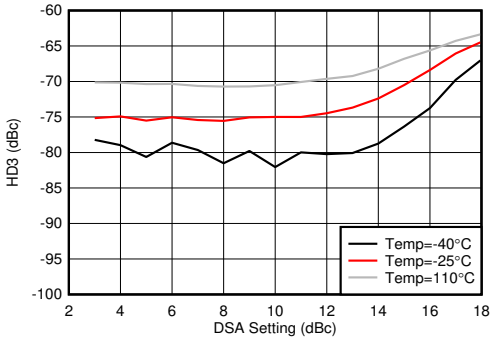
External clock mode

図 5-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz



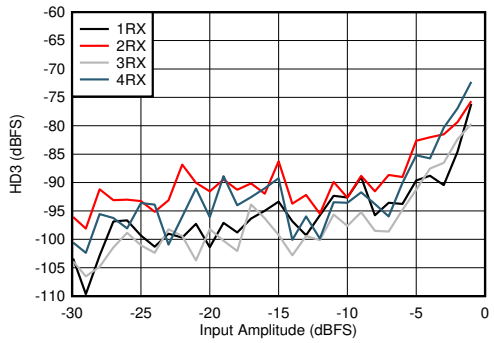
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

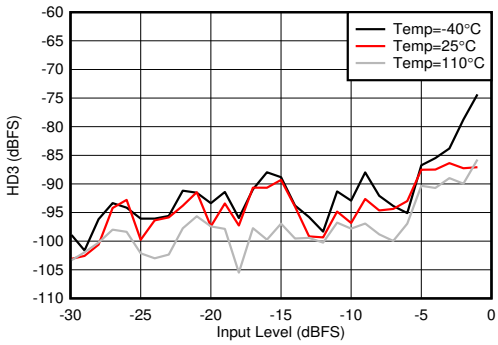
5.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



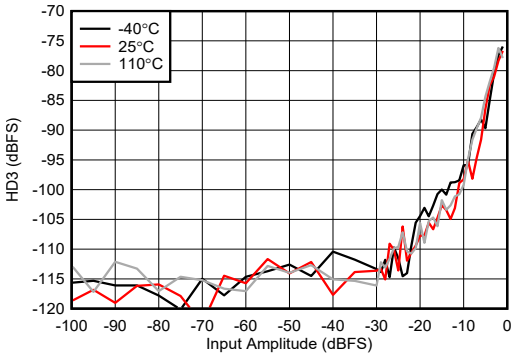
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-129. RX HD3 vs Input Level and Channel at 2.6 GHz



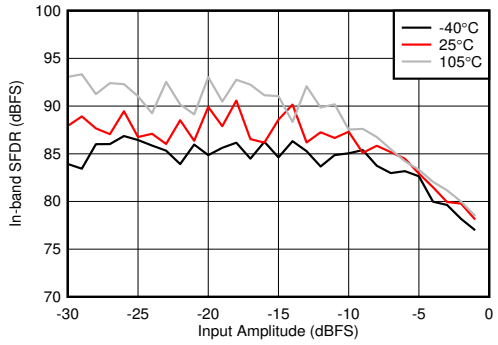
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-130. RX HD3 vs Input Level and Temperature at 2.6 GHz



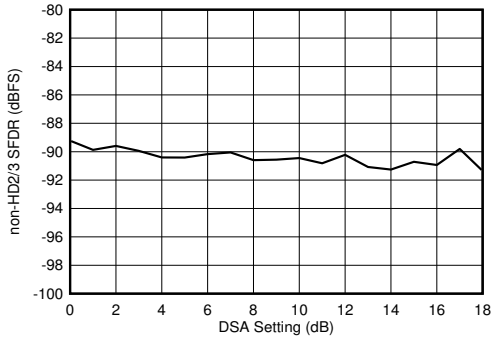
External clock mode

図 5-131. RX HD3 vs Input Level and Temperature at 2.6 GHz



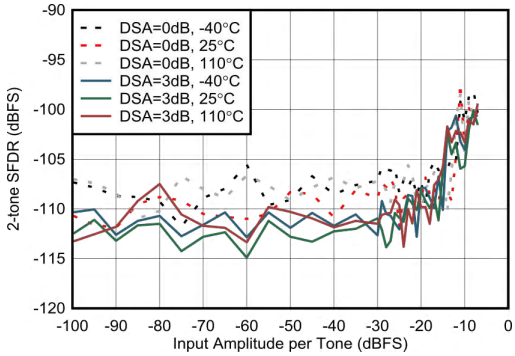
With 2.6 GHz matching, decimate by 4

図 5-132. RX In-Band SFDR (±300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



With 2.6 GHz matching

図 5-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz



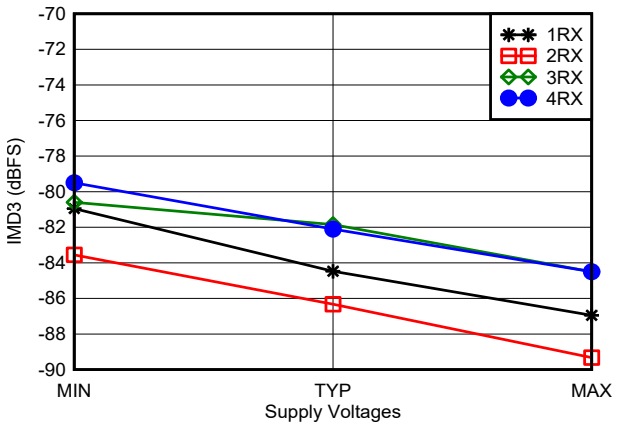
External clock mode, 50MHz tone spacing, excluding 3rd order distortion

図 5-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

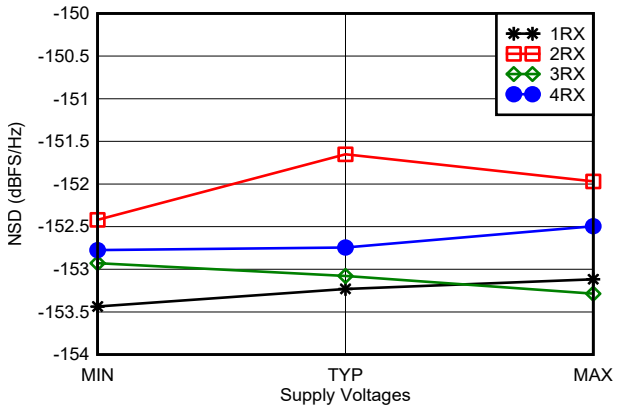
5.12.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 2.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-135. RX IMD3 vs Supply and Channel at 2.6 GHz



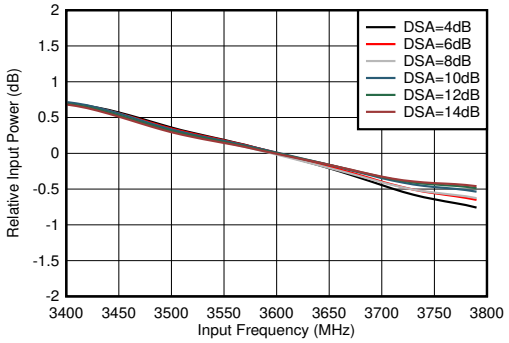
With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-136. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

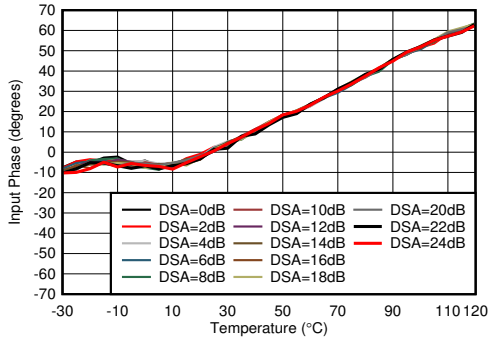
5.12.5 RX Typical Characteristics 3.5GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



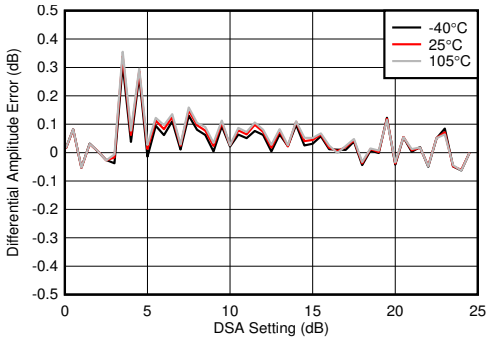
With 3.6 GHz matching, normalized to 3.6 GHz

図 5-137. RX In-Band Gain Flatness, f_{IN} = 3600 MHz



With 3.6 GHz matching, normalized to phase at 25°C

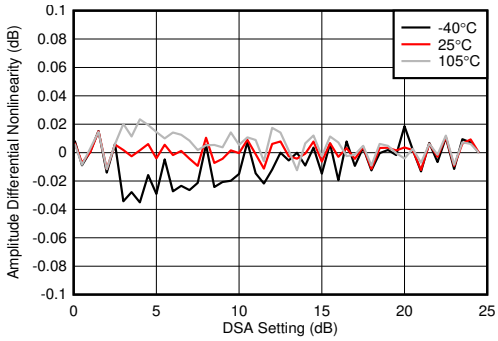
図 5-138. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

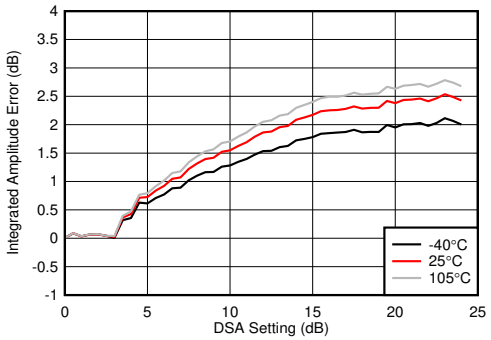
図 5-139. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

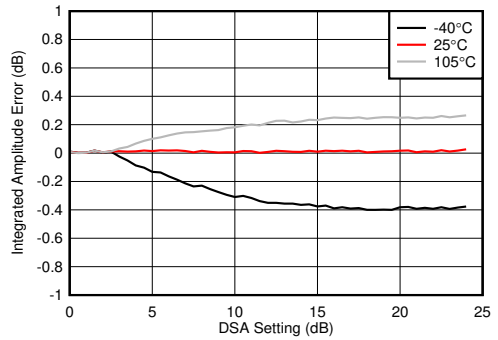
図 5-140. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-141. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

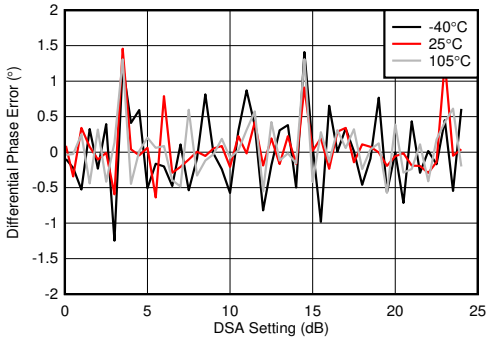
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-142. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

Copyright © 2023 Texas Instruments Incorporated

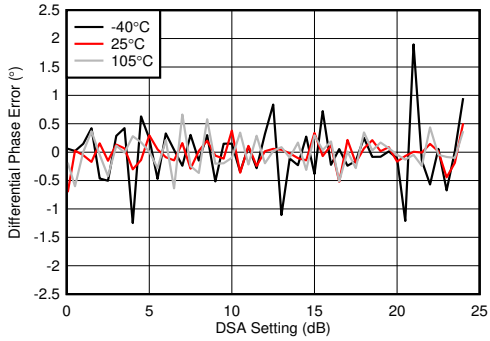
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



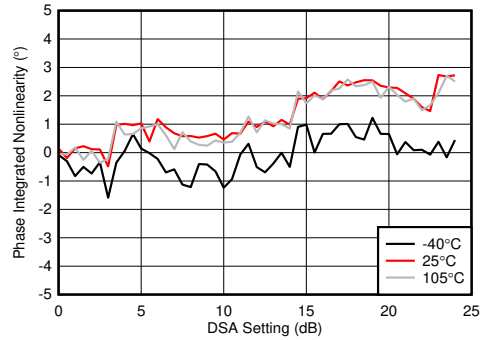
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



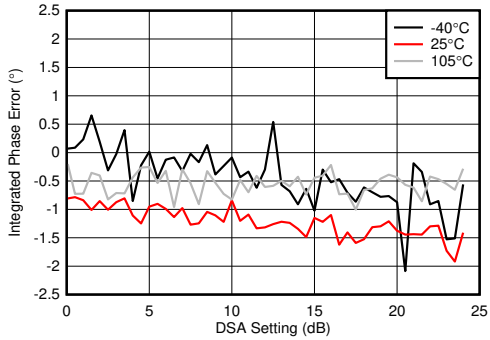
With 3.6 GHz matching
Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



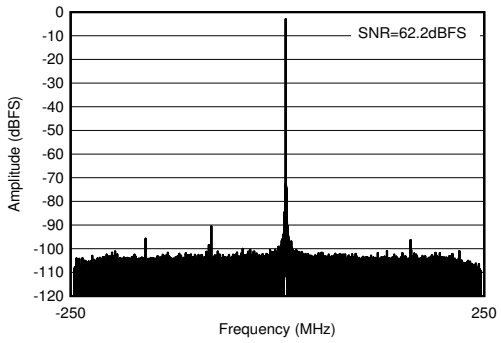
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



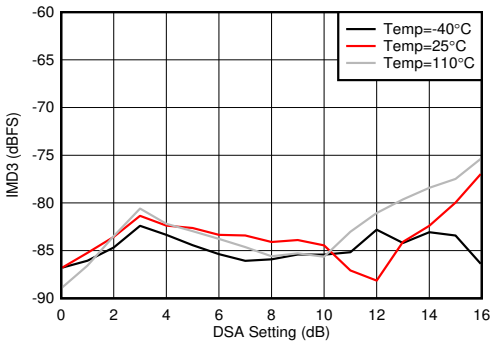
With 3.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching , f_{IN} = 3610 MHz, A_{IN} = –3 dBFS

図 5-147. RX Output FFT at 3.6 GHz



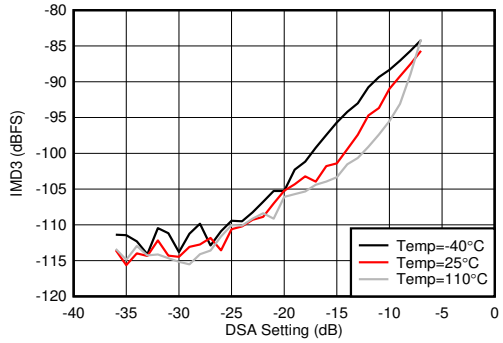
With 3.5 GHz matching, each tone at –7 dBFS, 20-MHz tone spacing

図 5-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

Copyright © 2023 Texas Instruments Incorporated

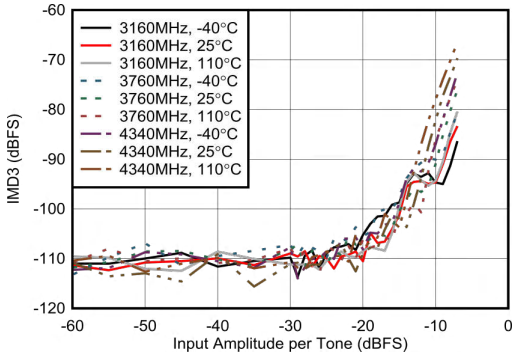
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



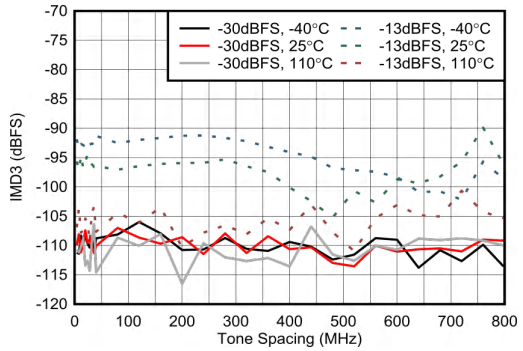
With 3.5 GHz matching, 20-MHz tone spacing

図 5-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



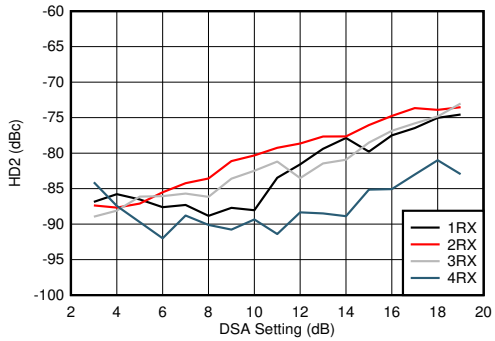
External clock mode, 20-MHz tone spacing, 2x Decimation

図 5-150. RX IMD3 vs Input Level



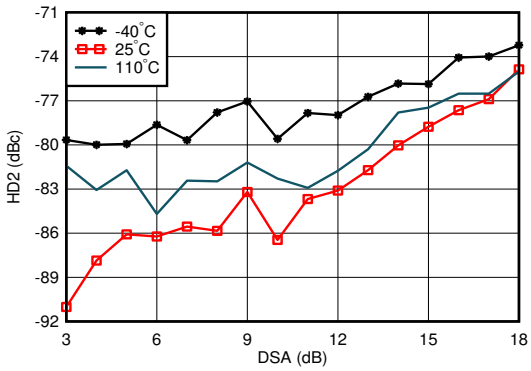
External clock mode, 2x Decimation

図 5-151. RX IMD3 vs Tone Spacing at 3.76GHz



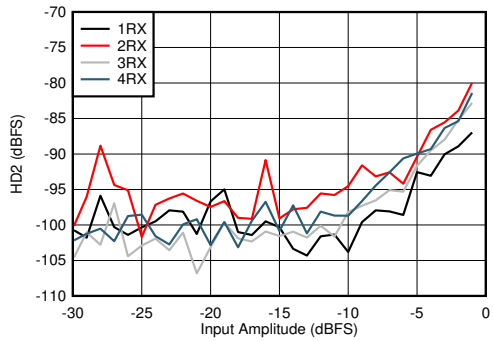
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

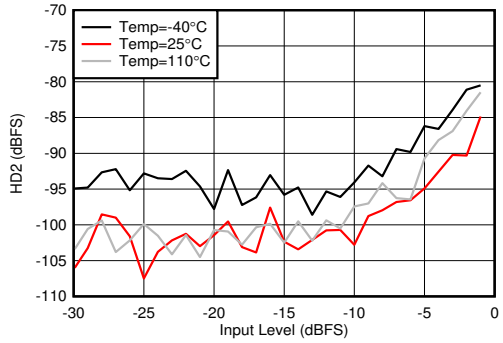


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-154. RX HD2 vs Input Level and Channel at 3.6 GHz

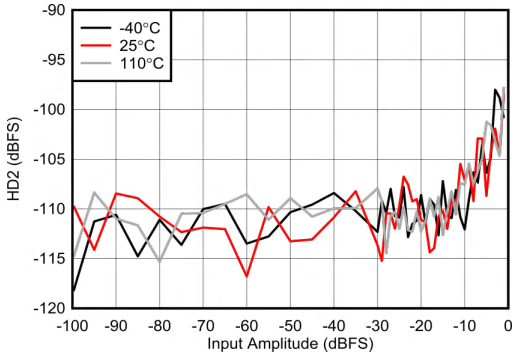
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



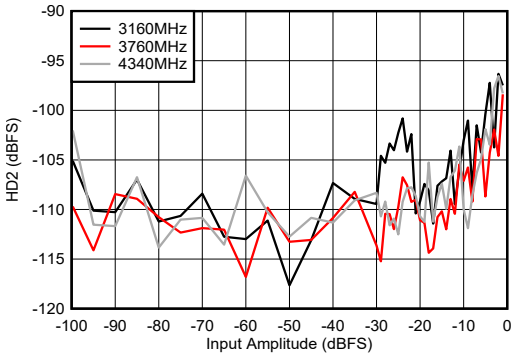
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



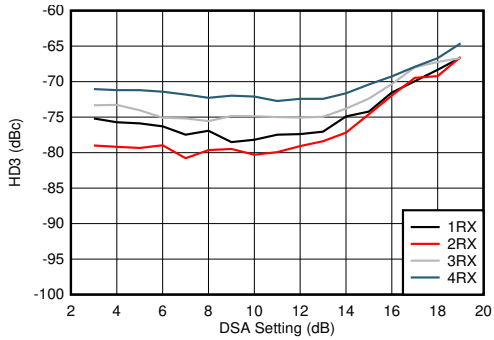
External clock mode, 2x Decimation

図 5-156. RX HD2 vs Input Level at 3.76 GHz



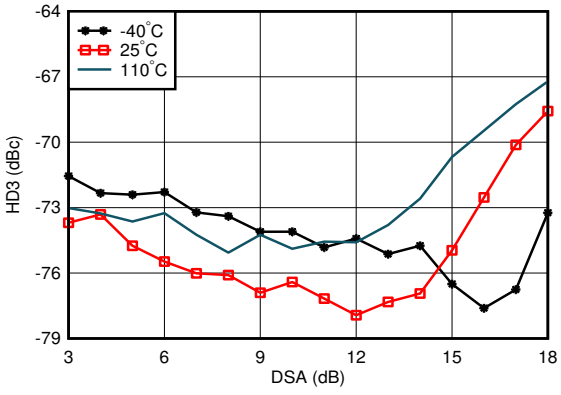
External clock mode, 25°C, 2x Decimation

図 5-157. RX HD2 vs Input Level



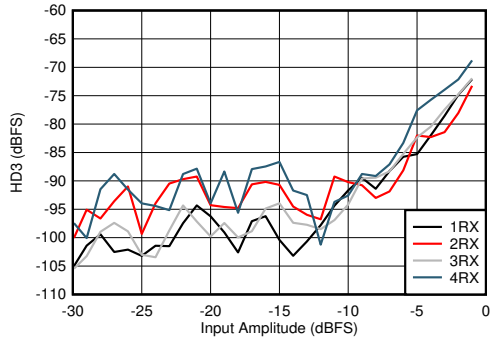
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



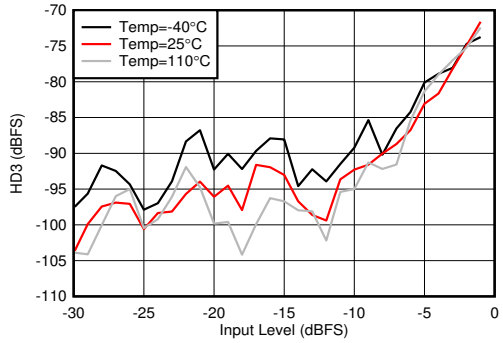
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-160. RX HD3 vs Input Level and Channel at 3.6 GHz

Copyright © 2023 Texas Instruments Incorporated

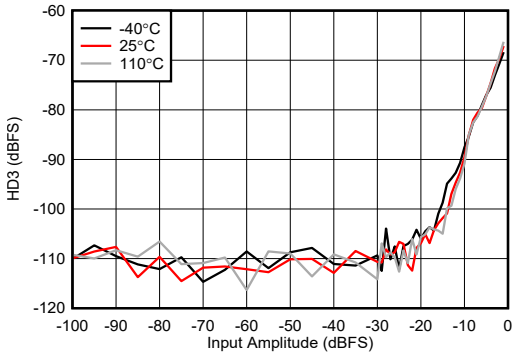
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



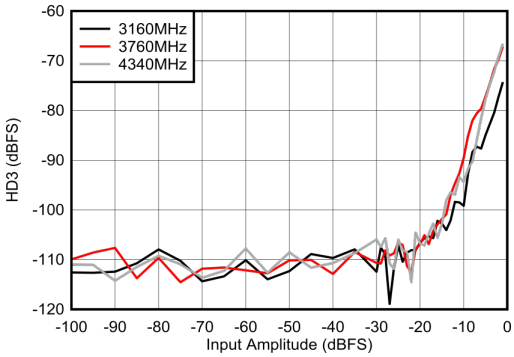
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



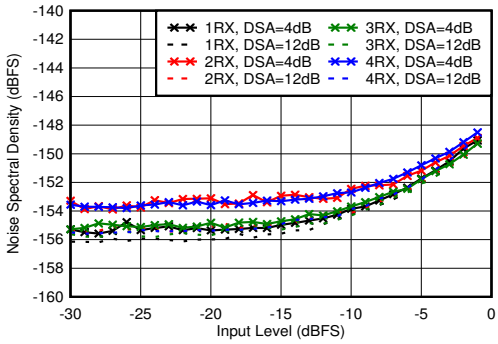
External clock mode, 2x Decimation

図 5-162. RX HD3 vs Input Level at 3.76GHz



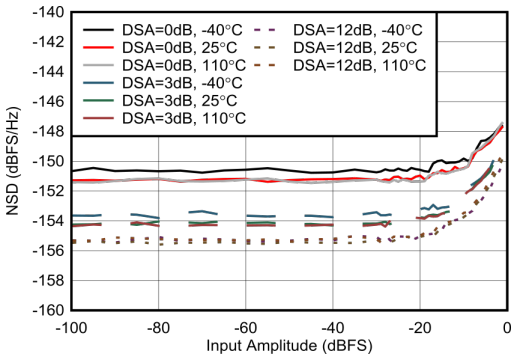
External clock mode, 25°C, 2x Decimation

図 5-163. RX HD3 vs Input Level



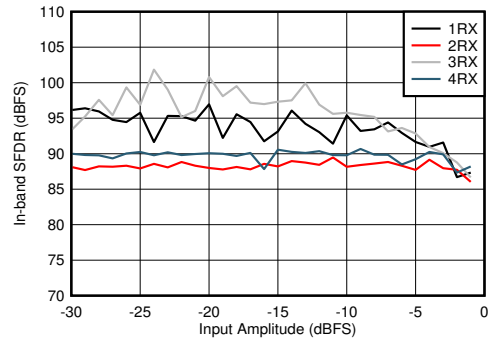
With 3.5 GHz matching, 12.5-MHz offset from tone

図 5-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

図 5-165. RX Noise Spectral Density vs Input Level at 3.76GHz

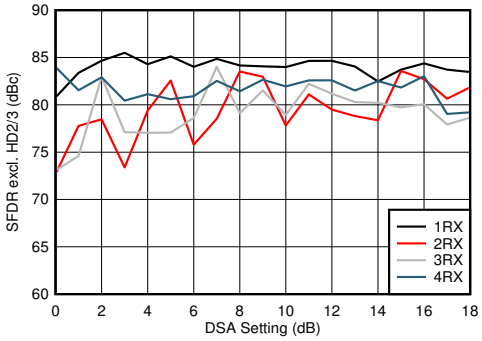


With 3.5 GHz matching

図 5-166. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

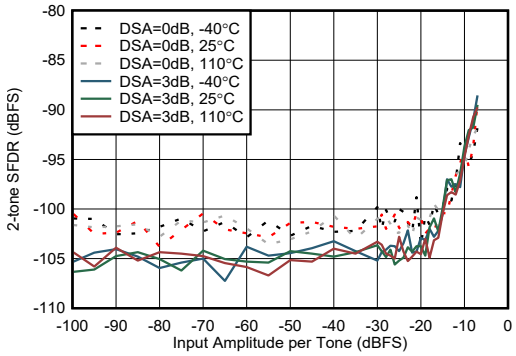
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



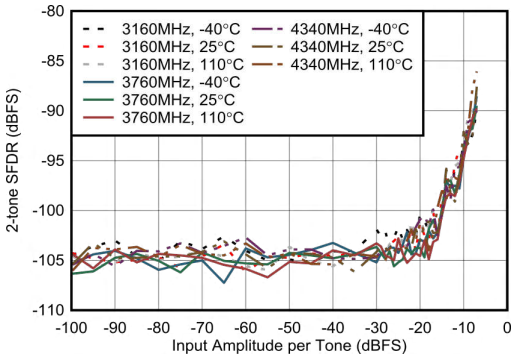
With 3.5 GHz matching

図 5-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



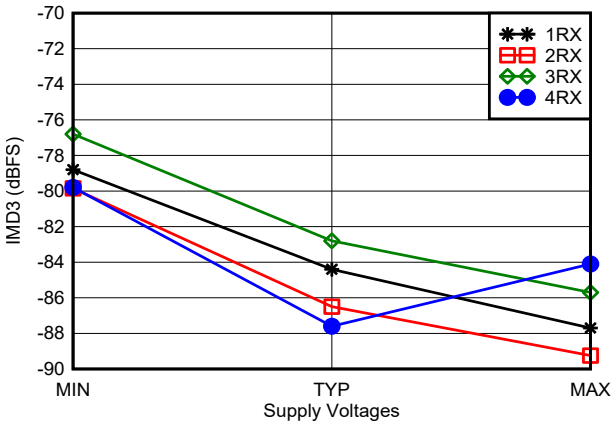
External clock mode, 20MHz tone spacing, excluding 3rd order distortion

図 5-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



External clock mode, 20MHz tone spacing, excluding 3rd order distortion

図 5-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz



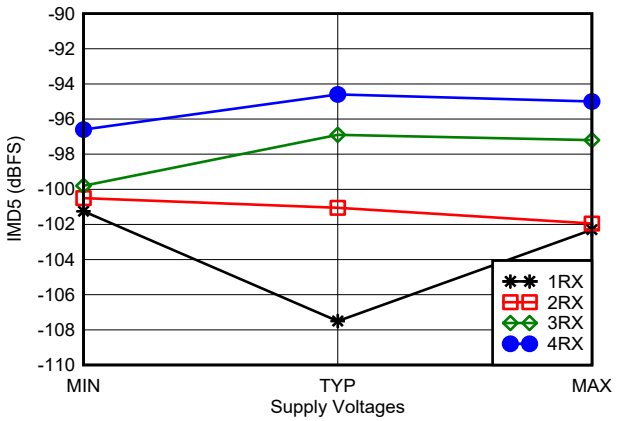
With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz

Copyright © 2023 Texas Instruments Incorporated

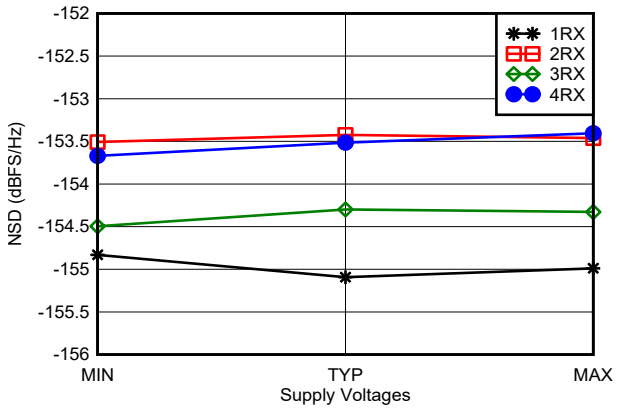
5.12.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 3.6 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

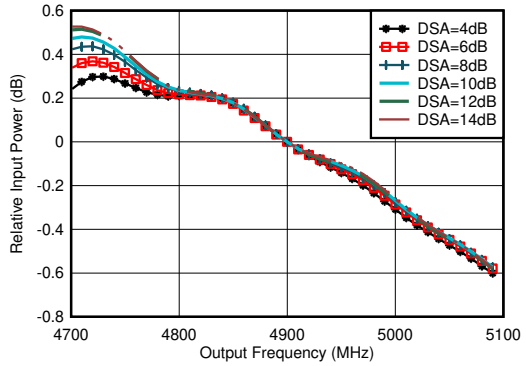


With 3.6 GHz matching, tone at –20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

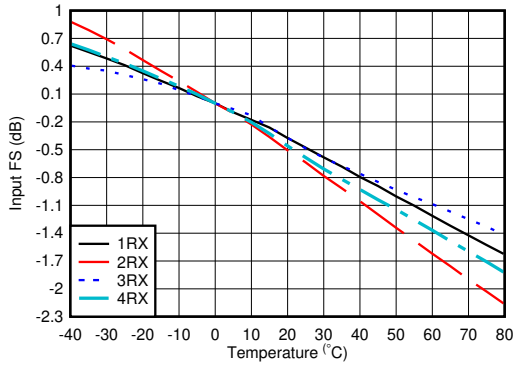
5.12.6 RX Typical Characteristics 4.9GHz

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



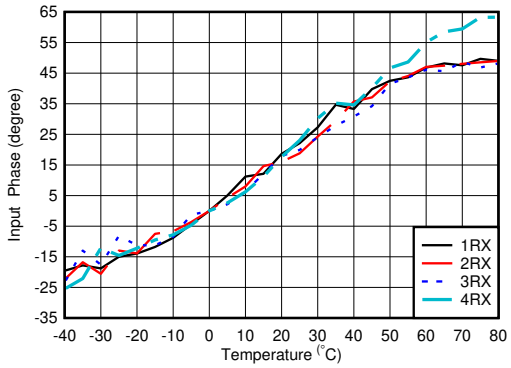
With matching, normalized to power at 4.9GHz for each DSA setting

図 5-173. RX Inband Gain Flatness, f_{IN} = 4900 MHz



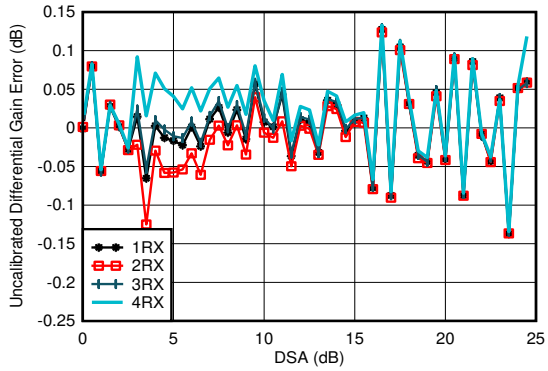
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

図 5-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

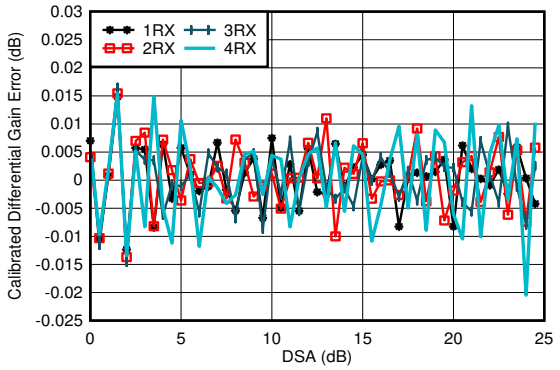
図 5-175. RX Input Phase vs Temperature and DSA at f_{OUT} = 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

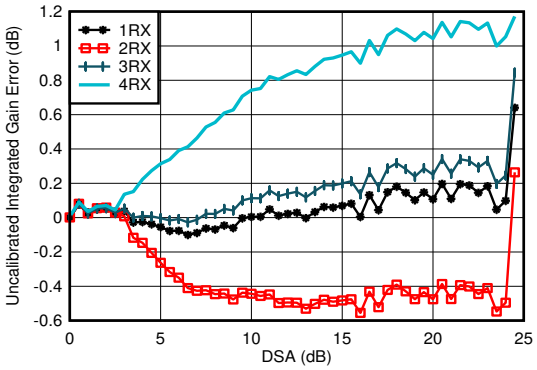
図 5-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = P_{IN}(DSA Setting – 1) – P_{IN}(DSA Setting) + 1

図 5-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

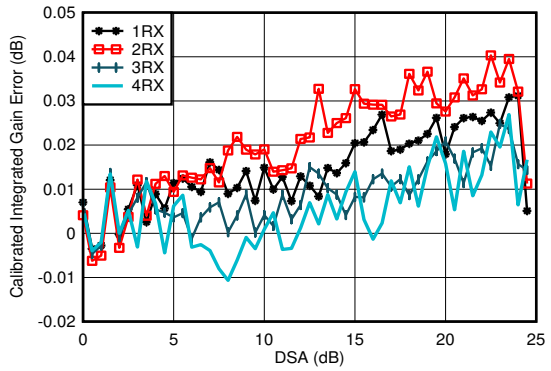
Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

図 5-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.6 RX Typical Characteristics 4.9GHz (continued)

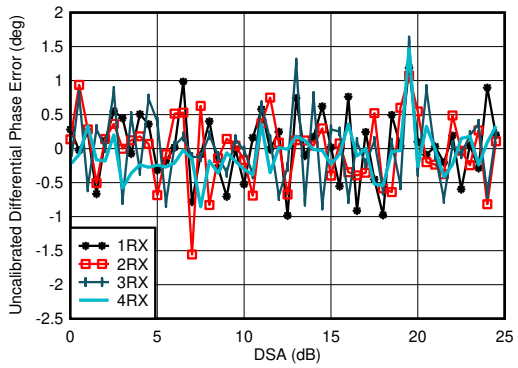
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = P_{IN}(DSA Setting) – P_{IN}(DSA Setting = 0) + (DSA Setting)

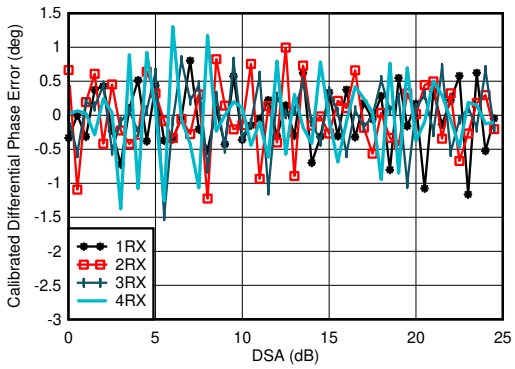
図 5-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

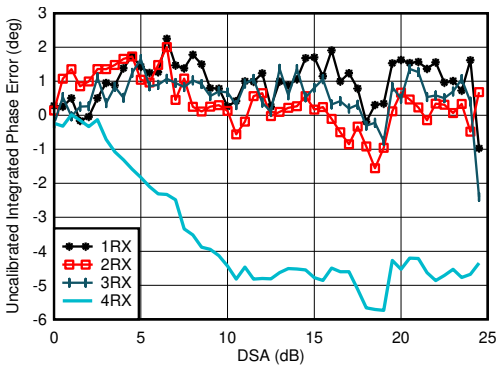
図 5-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $Phase_{IN}$(DSA Setting – 1) – $Phase_{IN}$(DSA Setting)

図 5-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



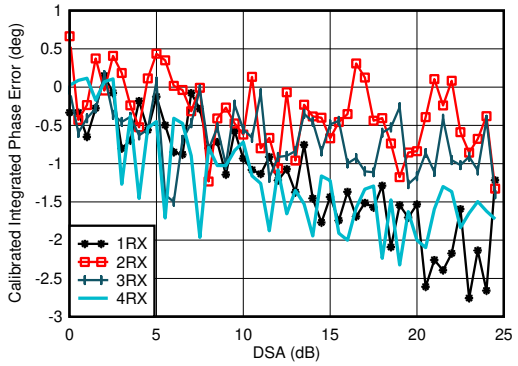
With 4.9 GHz matching

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

5.12.6 RX Typical Characteristics 4.9GHz (continued)

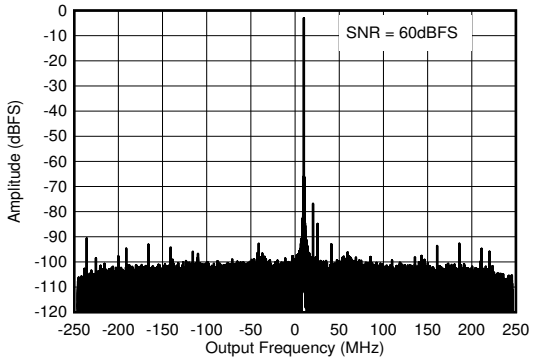
Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



With 4.9 GHz matching

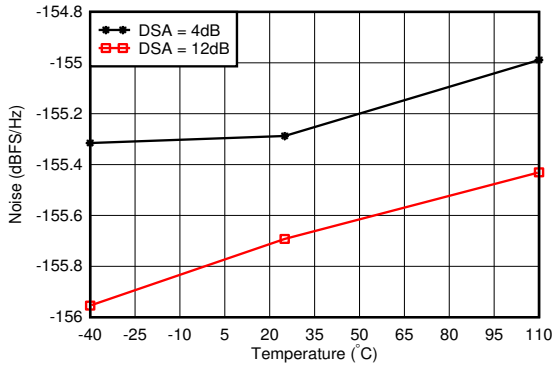
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-183. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



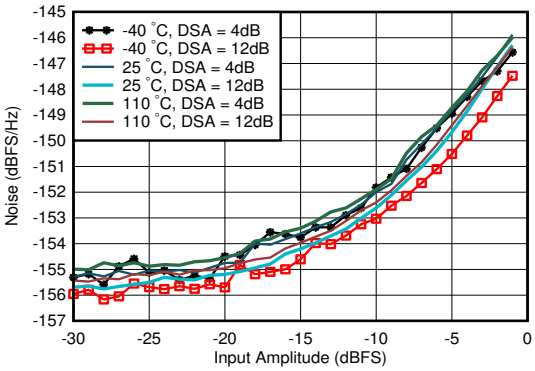
With 4.9 GHz matching, f_{IN} = 4910 MHz, A_{IN}= –3 dBFS

図 5-184. RX Output FFT at 4.9 GHz



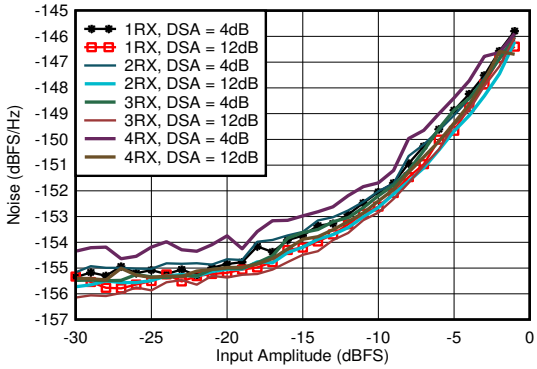
With 4.9 GHz matching, 12.5-MHz offset from tone

図 5-185. RX Noise Spectral Density vs Temperature at 4.9 GHz



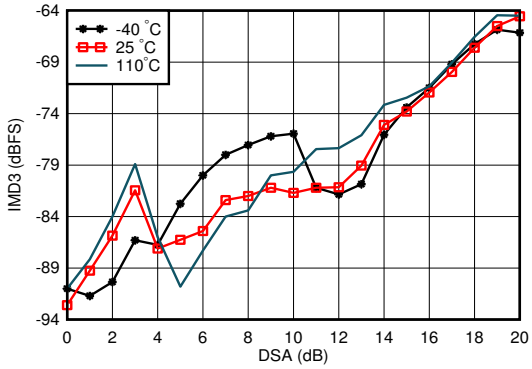
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

図 5-186. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset from tone

図 5-187. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



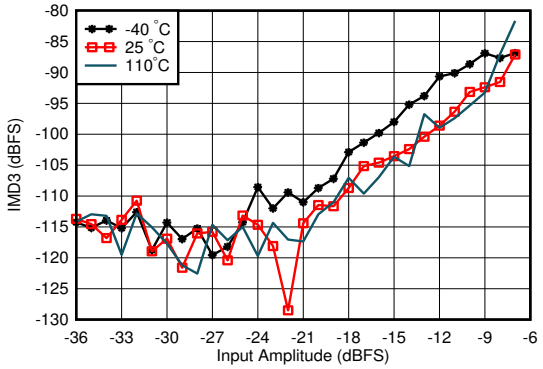
With 4.9 GHz matching, each tone –7 dBFS, tone spacing = 20 MHz

図 5-188. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

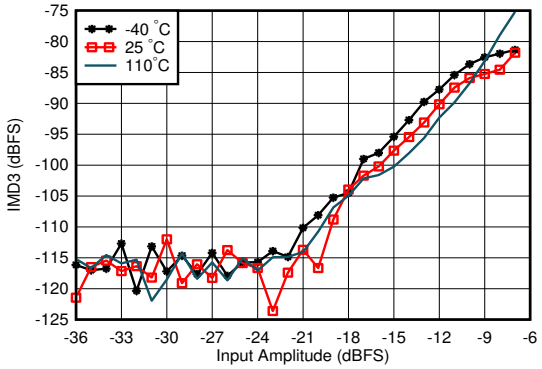
5.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



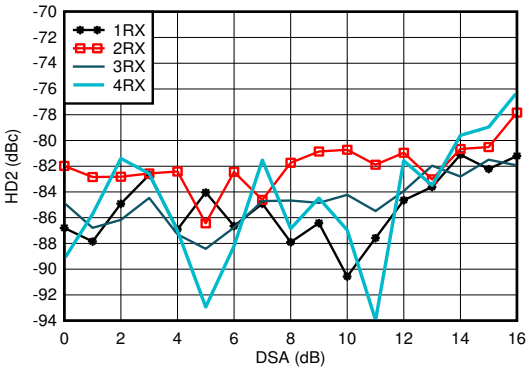
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

図 5-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz



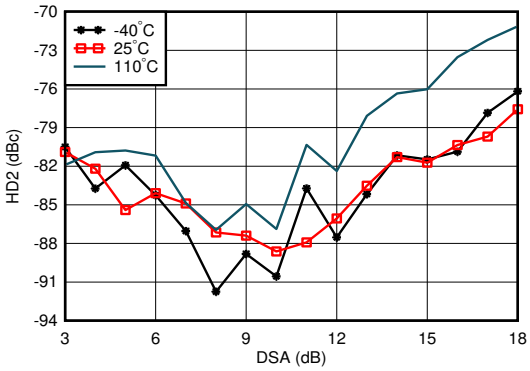
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

図 5-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz



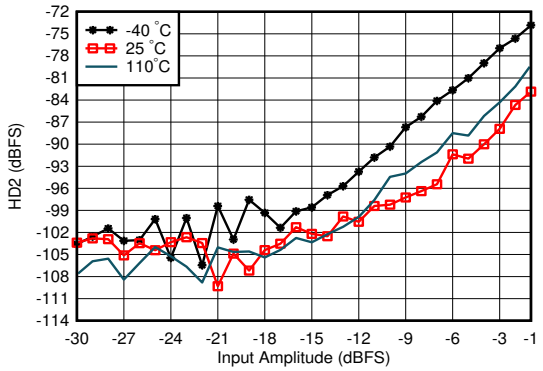
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



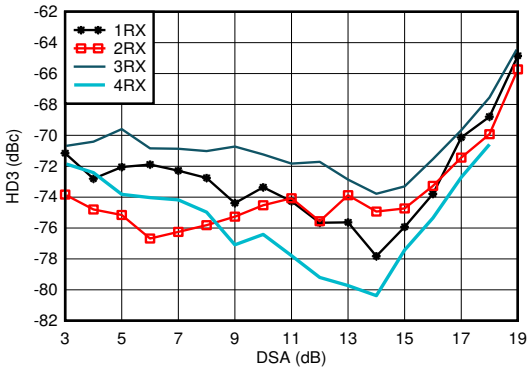
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-192. RX HD2 vs DSA and Temperature at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

図 5-193. RX HD2 vs Input Level and Temperature at 4.9 GHz



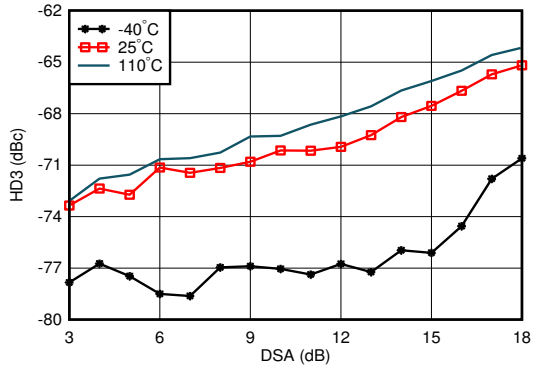
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

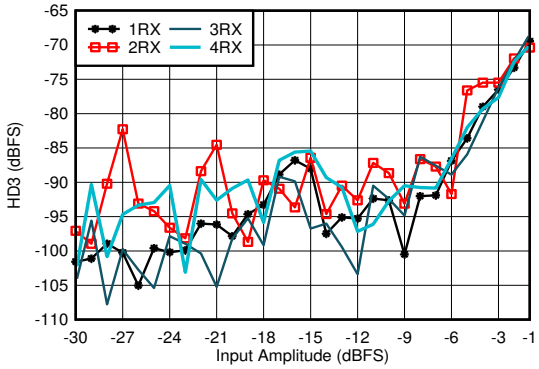
5.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.



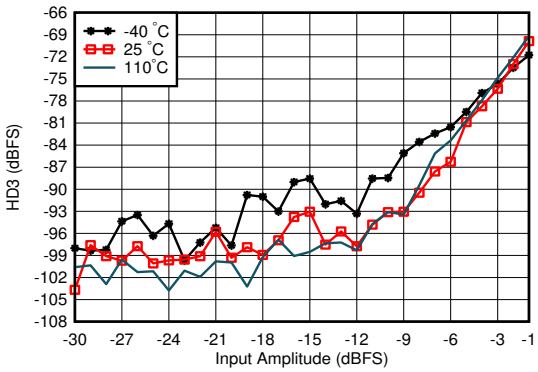
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



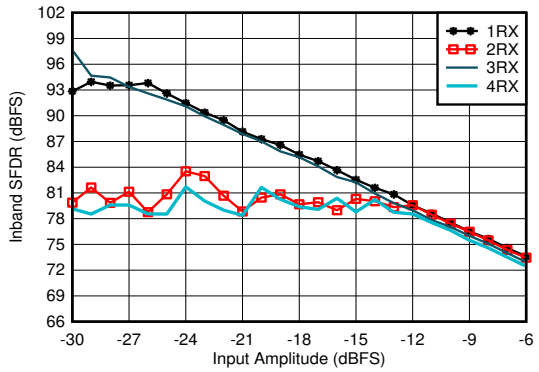
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-196. RX HD3 vs Input Level and Channel at 4.9 GHz



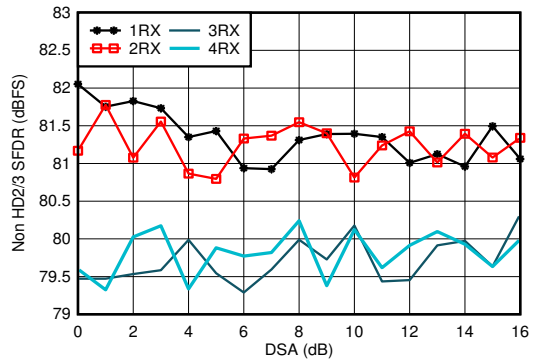
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

図 5-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



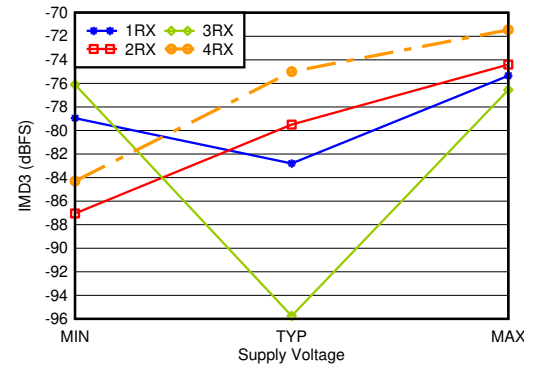
With 4.9 GHz matching, decimate by 3

図 5-198. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

図 5-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



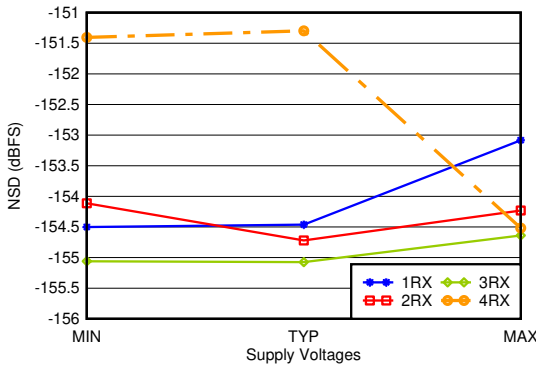
With 4.9 GHz matching, –7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-200. RX IMD3 vs Supply and Channel at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at T_A = +25°C, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with f_{REF} = 491.52MHz, A_{IN} = –3 dBFS, DSA setting = 4 dB.

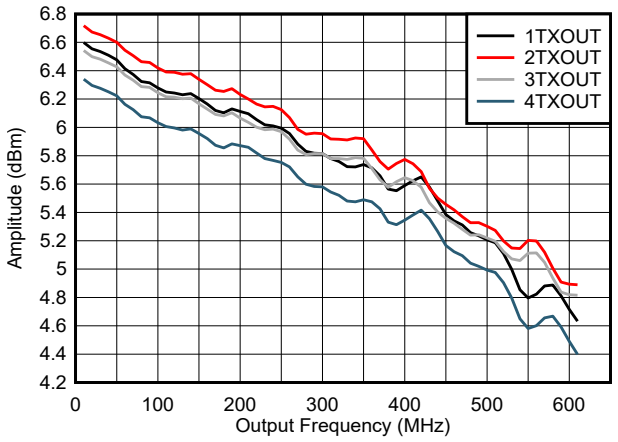


With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

図 5-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

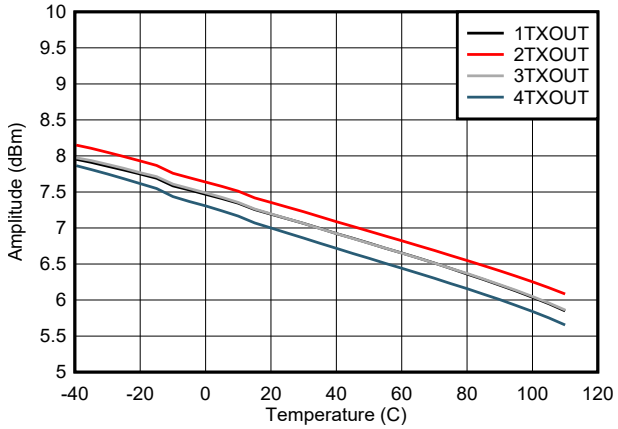
5.12.7 TX Typical Characteristics at 30MHz and 400MHz

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



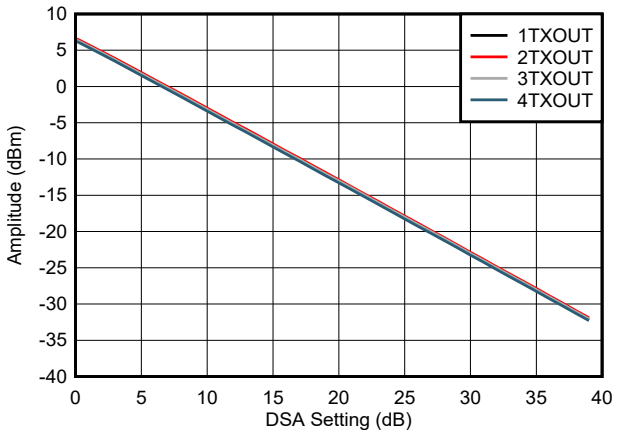
including PCB and cable losses

図 5-202. TX Output Fullscale vs Output Frequency: 5 MHz - 600 MHz



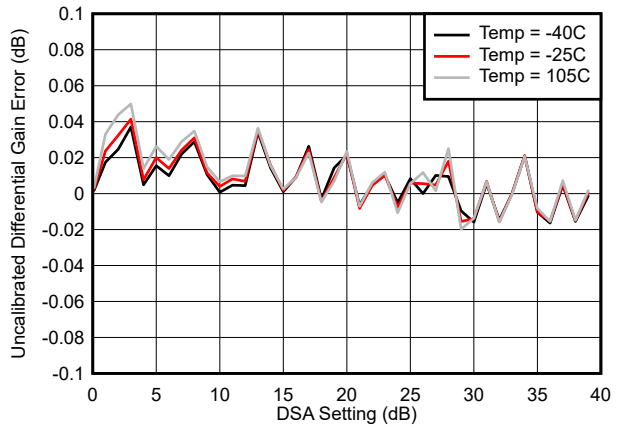
including PCB and cable losses

図 5-203. TX Output Fullscale vs Temperature at 30 MHz



including PCB and cable losses

図 5-204. TX Output Fullscale vs DSA Setting at 30 MHz



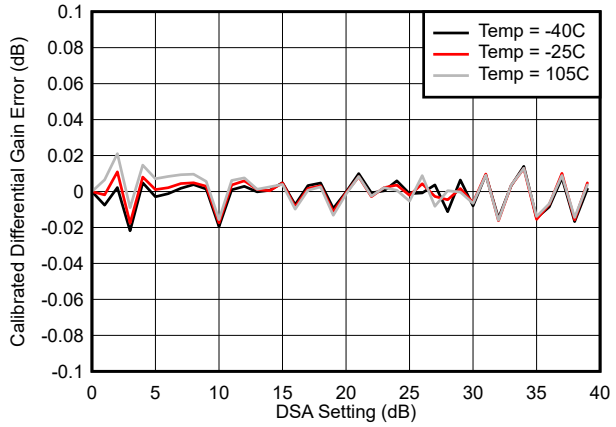
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-205. Uncalibrated TX Differential Gain Error (DNL) at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

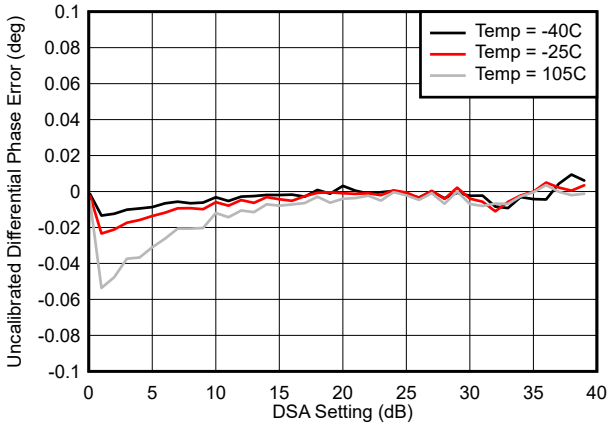
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



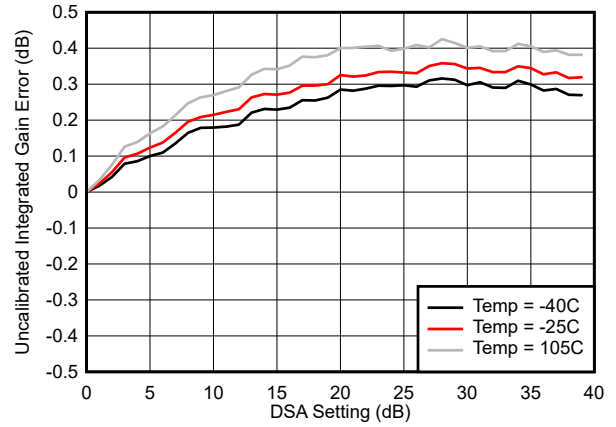
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-206. Calibrated TX Differential Gain Error (DNL) at 30MHz



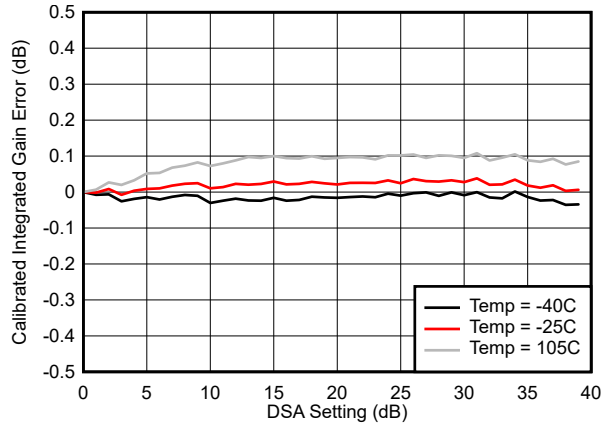
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-207. Calibrated TX Differential Gain Error (DNL) at 30 MHz



Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 5-208. Uncalibrated TX Integrated Gain Error (INL) at 30 MHz



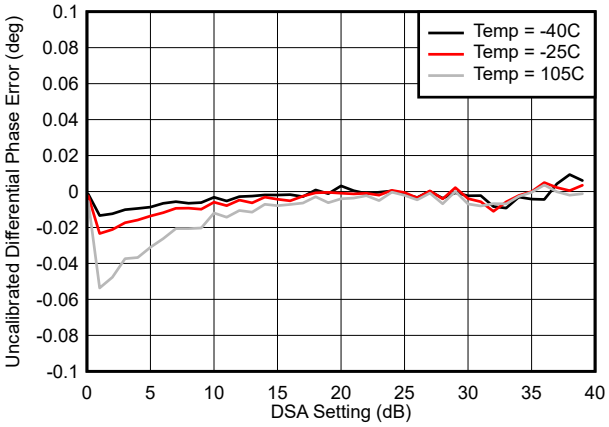
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 5-209. Calibrated TX Integrated Gain Error (INL) at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

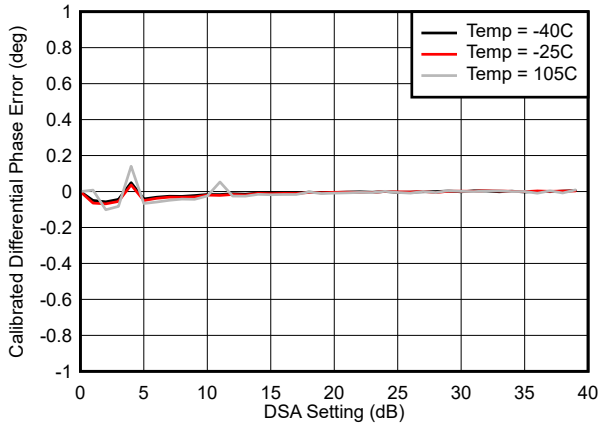
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



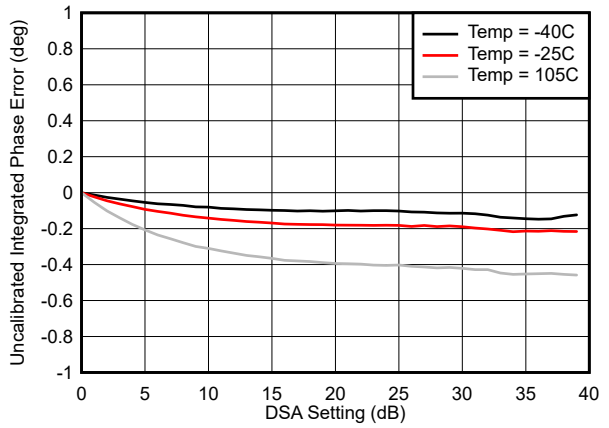
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-210. Uncalibrated TX Differential Phase Error (DNL) at 30 MHz



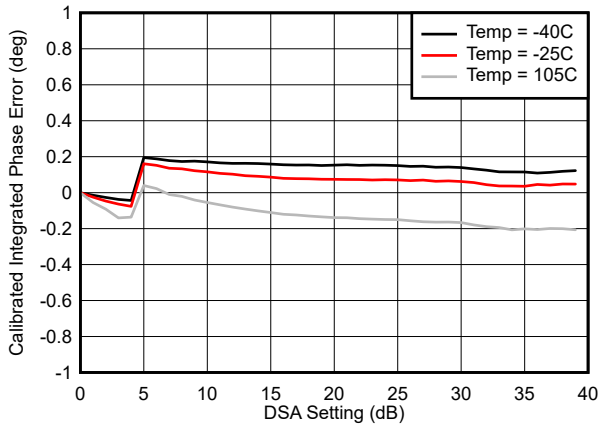
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-211. Calibrated TX Differential Phase Error (DNL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 5-212. Uncalibrated TX Integrated Phase Error (INL) at 30 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 5-213. Calibrated TX Integrated Phase Error (INL) at 30 MHz

Copyright © 2023 Texas Instruments Incorporated

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

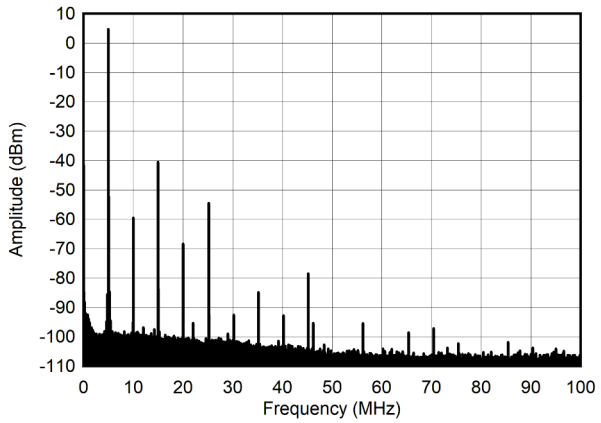


図 5-214. Single Tone Spectrum at 5 MHz and -1 dBFS (0 - 100 MHz)

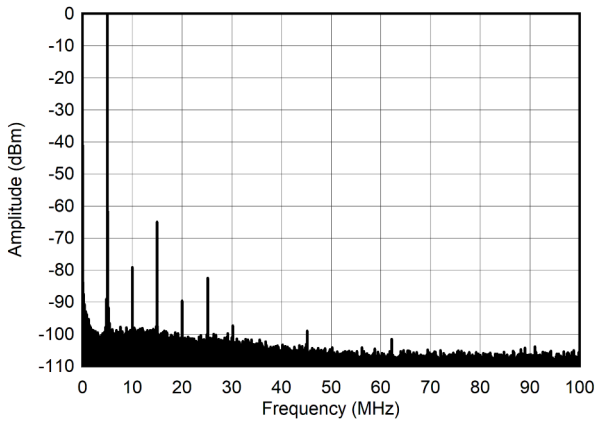


図 5-215. Single Tone Spectrum at 5 MHz and -6d BFS (0 - 100 MHz)

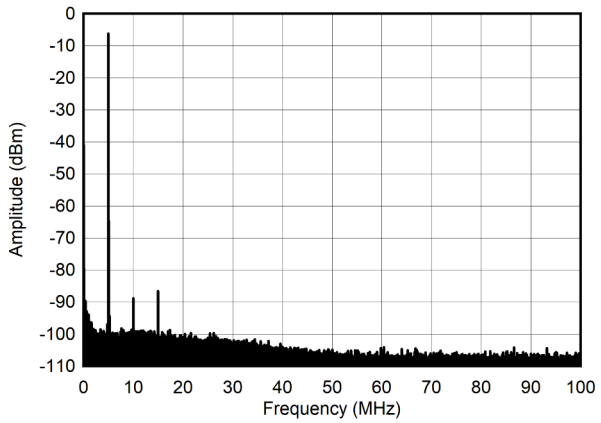


図 5-216. Single Tone Spectrum at 5 MHz and -12 dBFS (0 - 100 MHz)

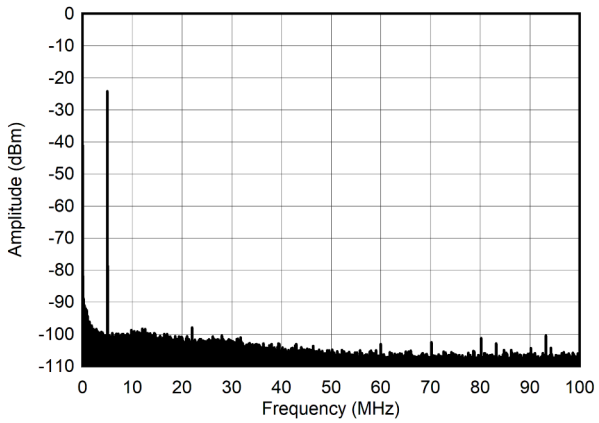


図 5-217. Single Tone Spectrum at 5 MHz and -30 dBFS (0 - 100 MHz)

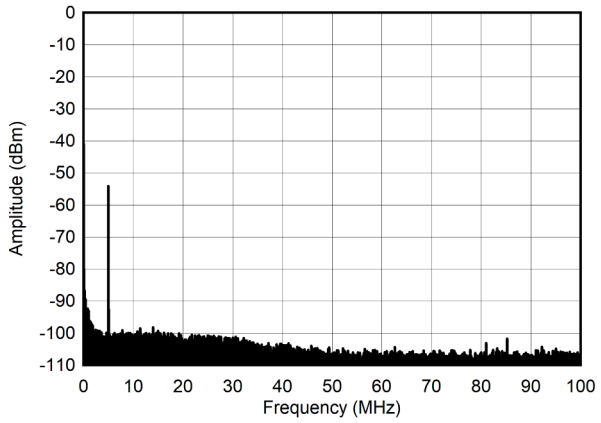


図 5-218. Single Tone Spectrum at 5 MHz and -60 dBFS (0 - 100 MHz)

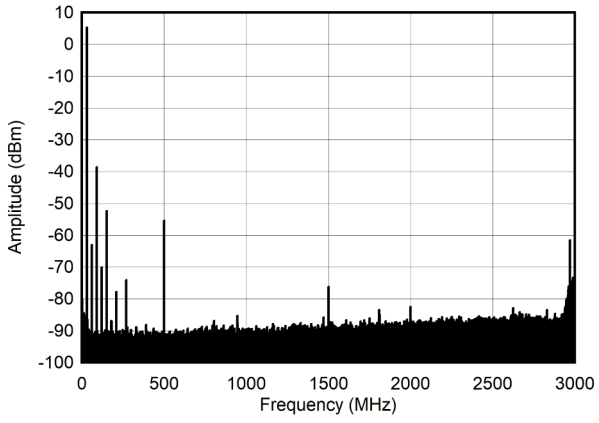


図 5-219. Single Tone Spectrum at 30 MHz and -1 dBFS (Nyquist)

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

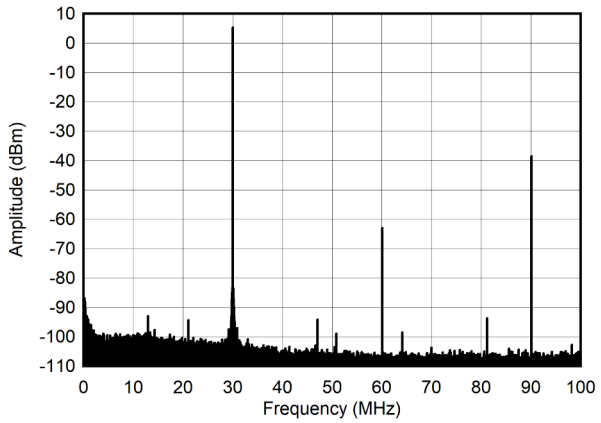


図 5-220. Single Tone Spectrum at 30 MHz and -1 dBFS (0 - 100 MHz)

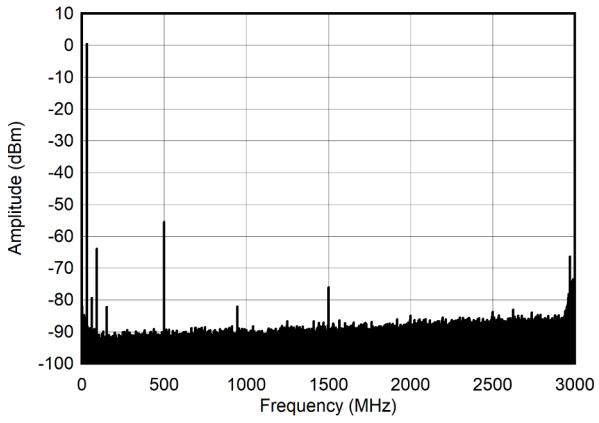


図 5-221. Single Tone Spectrum at 30 MHz and -6 dBFS (Nyquist)

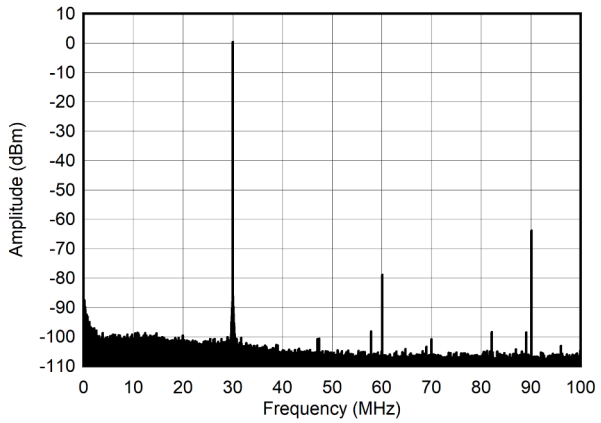


図 5-222. Single Tone Spectrum at 30 MHz and -6 dBFS (0 - 100 MHz)

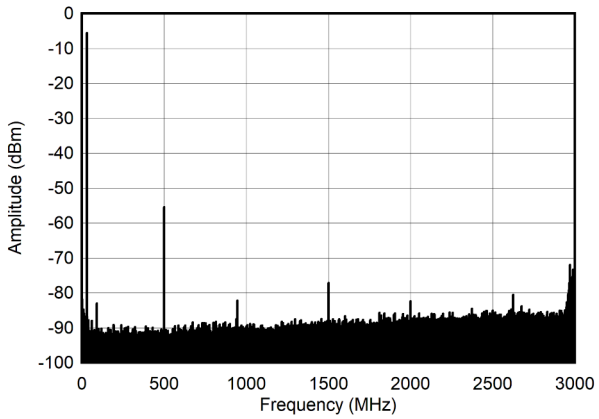


図 5-223. Single Tone Spectrum at 30 MHz and -12 dBFS (Nyquist)

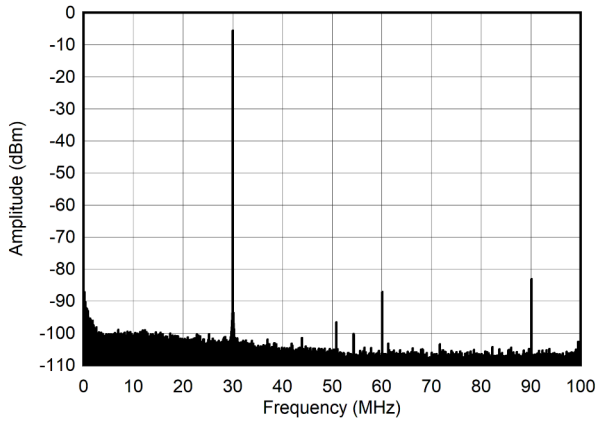


図 5-224. Single Tone Spectrum at 30 MHz and -12 dBFS (0 - 100 MHz)

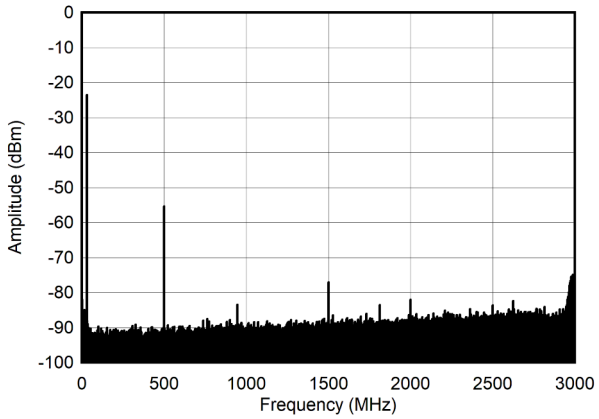


図 5-225. Single Tone Spectrum at 30 MHz and -30 dBFS (Nyquist)

Copyright © 2023 Texas Instruments Incorporated

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

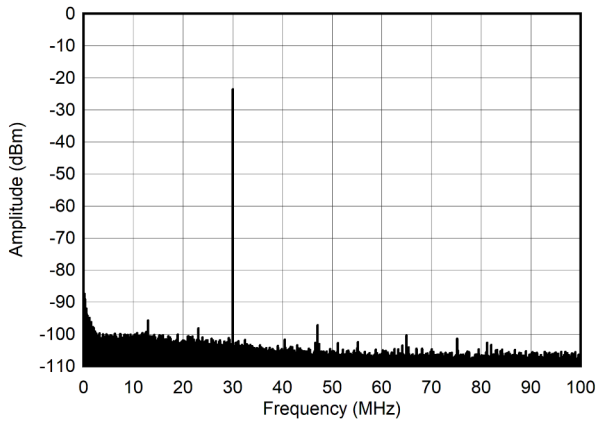


図 5-226. Single Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

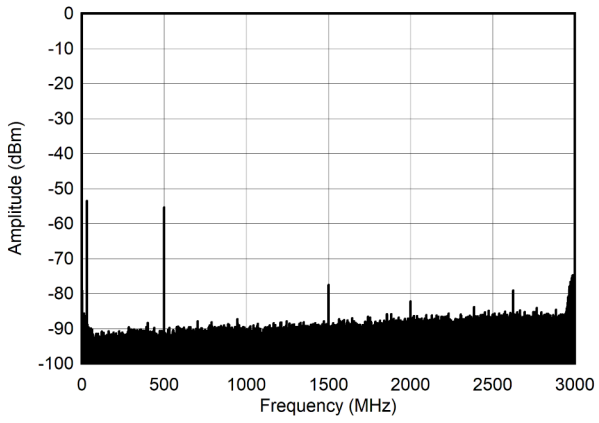


図 5-227. Single Tone Spectrum at 30 MHz and -60 dBFS (Nyquist)

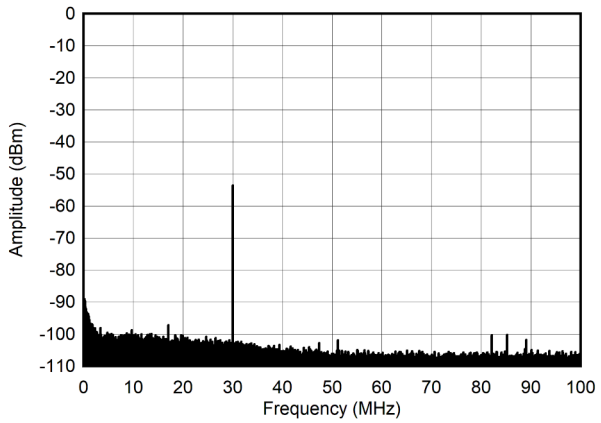


図 5-228. Single Tone Spectrum at 30 MHz and -60 dBFS (0 - 100 MHz)

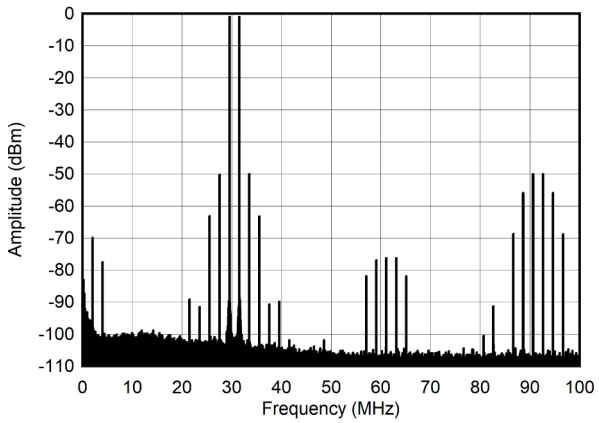


図 5-229. Dual Tone Spectrum at 30 MHz and -7 dBFS (0 - 100 MHz)

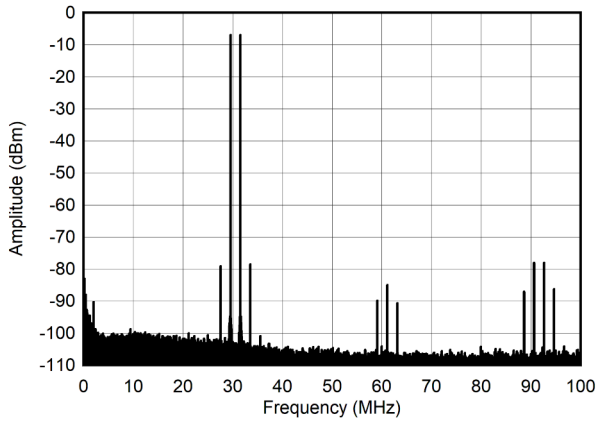


図 5-230. Dual Tone Spectrum at 30 MHz and -13 dBFS (0 - 100 MHz)

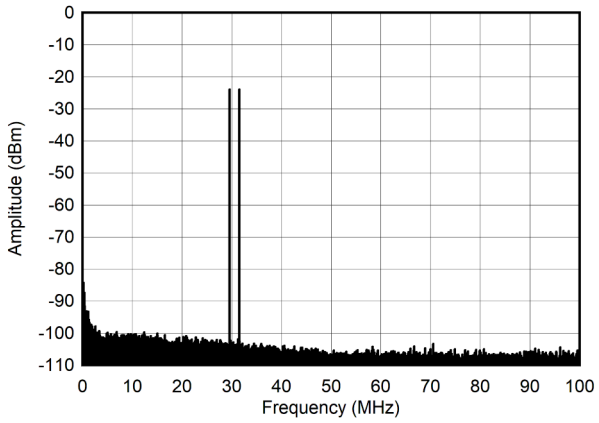


図 5-231. Dual Tone Spectrum at 30 MHz and -30 dBFS (0 - 100 MHz)

Copyright © 2023 Texas Instruments Incorporated

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

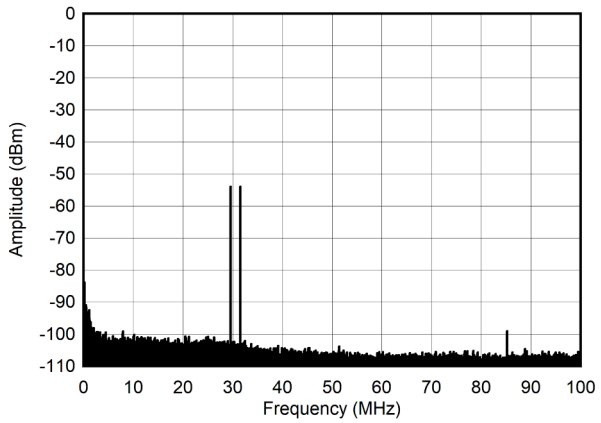
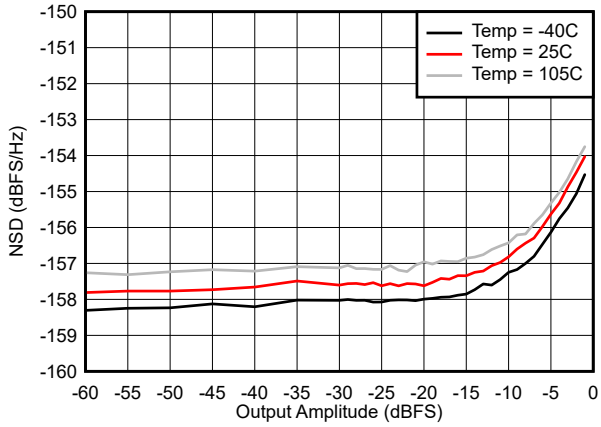
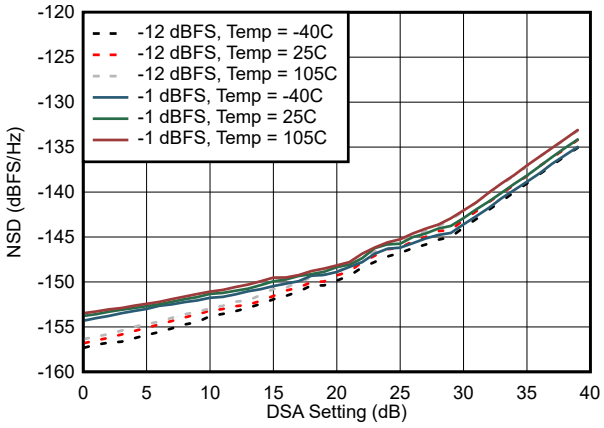


図 5-232. Dual Tone Spectrum at 30 MHz and -60d BFS (0 - 100 MHz)



measured at +50 MHz offset

図 5-233. Noise Spectral Density vs Digital Amplitude at 30 MHz



measured at +50 MHz offset

図 5-234. Noise Spectral Density vs DSA Setting at 30 MHz

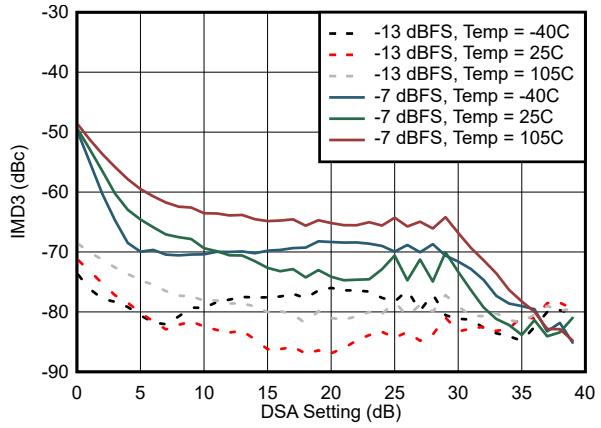


図 5-235. IMD3 vs DSA Setting at 30 MHz

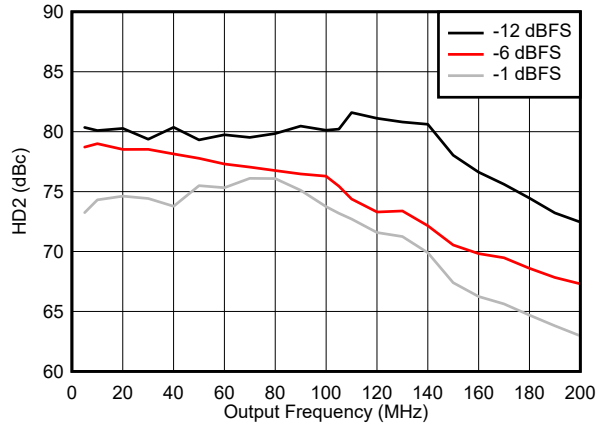


図 5-236. HD2 vs Frequency 0 - 200 MHz

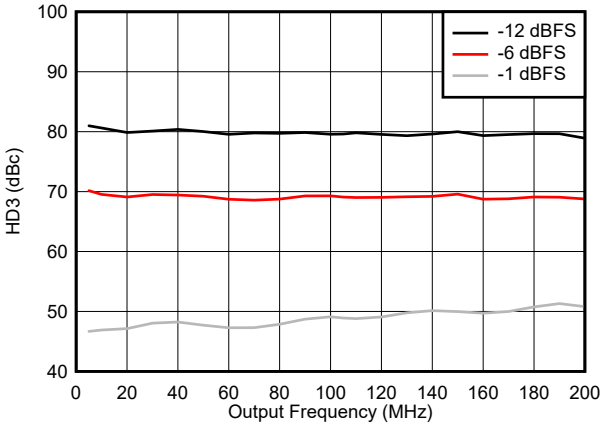
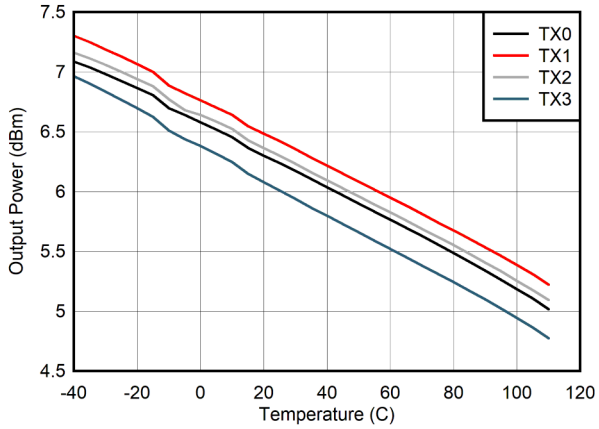


図 5-237. HD3 vs Frequency 0 - 200 MHz

Copyright © 2023 Texas Instruments Incorporated

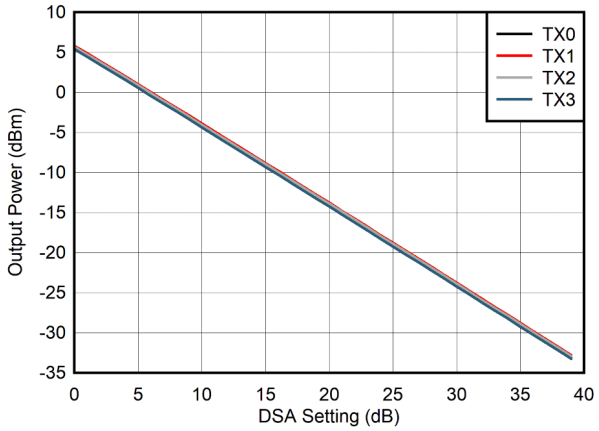
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



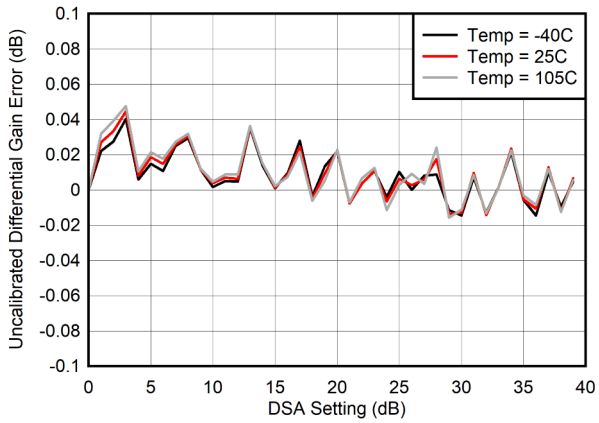
including PCB and cable losses

図 5-238. TX Output Fullscale vs Temperature at 400 MHz



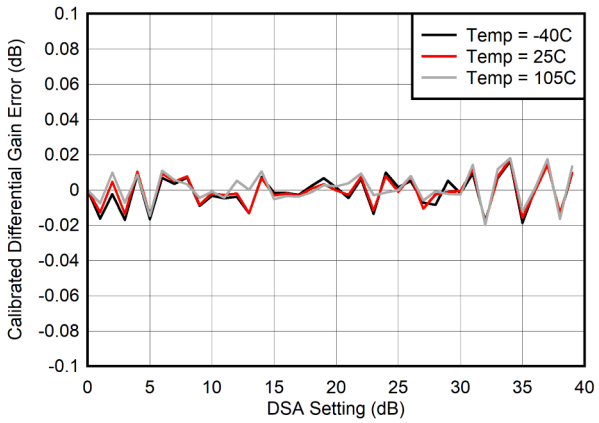
including PCB and cable losses

図 5-239. TX Output Fullscale vs DSA Setting at 400 MHz



Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-240. Uncalibrated TX Differential Gain Error (DNL) at 400 MHz



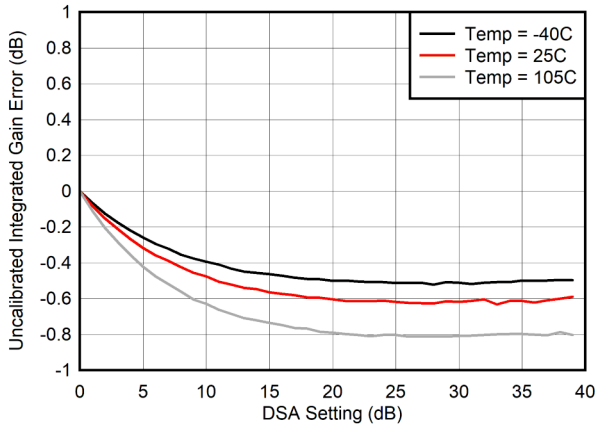
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-241. Calibrated TX Differential Gain Error (DNL) at 400 MHz

Copyright © 2023 Texas Instruments Incorporated

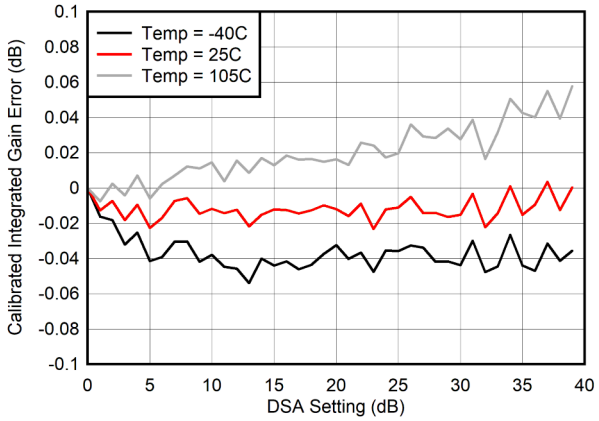
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



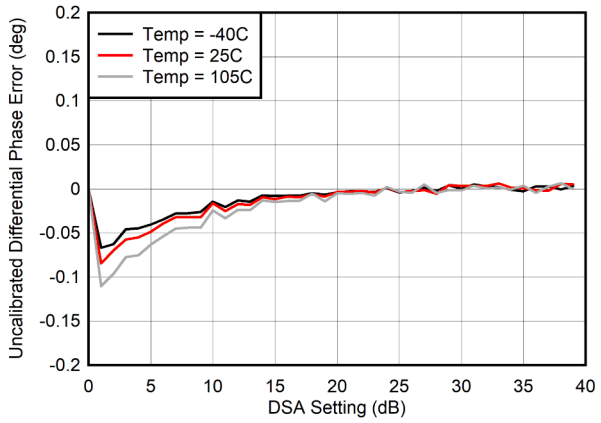
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 5-242. Uncalibrated TX Integrated Gain Error (INL) at 400 MHz



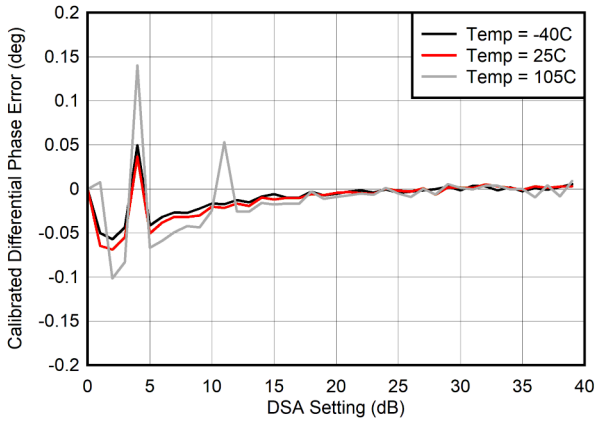
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSASetting = 0) + (DSA Setting)

図 5-243. Calibrated TX Integrated Gain Error (INL) at 400 MHz



Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-244. Uncalibrated TX Differential Phase Error (DNL) at 400 MHz



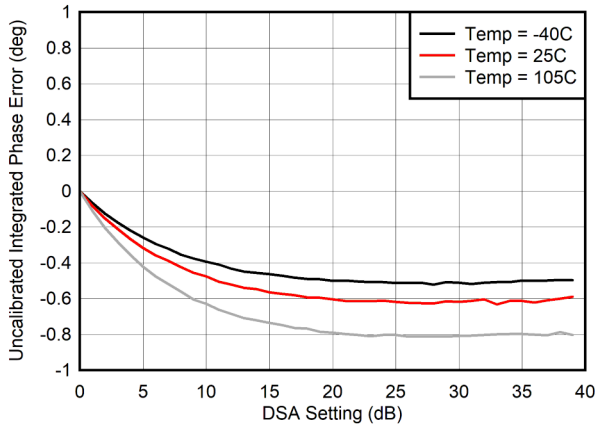
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-245. Calibrated TX Differential Phase Error (DNL) at 400 MHz

Copyright © 2023 Texas Instruments Incorporated

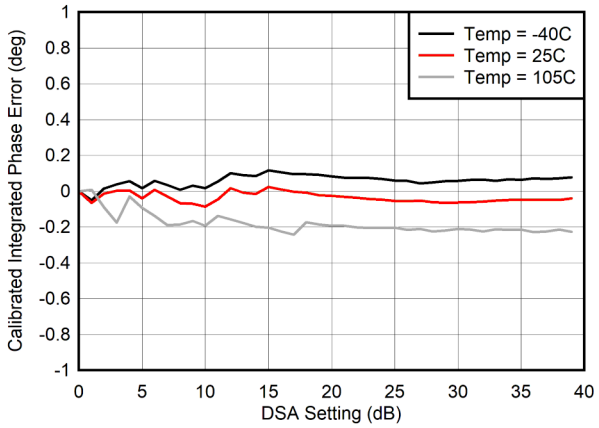
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 5-246. Uncalibrated TX Integrated Phase Error (INL) at 400 MHz



Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSASetting = 0)

図 5-247. Calibrated TX Integrated Phase Error (INL) at 400 MHz

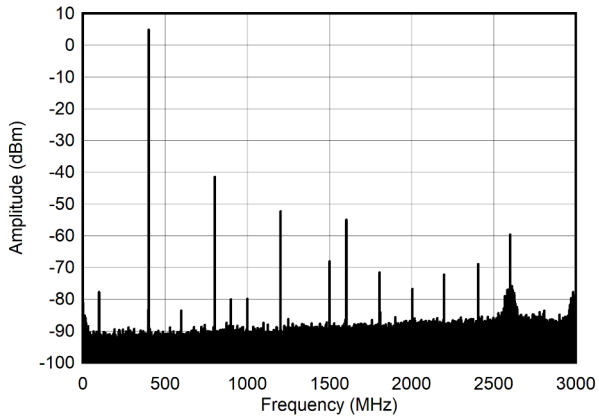


図 5-248. Single Tone Spectrum at 400 MHz and -1 dBFS (Nyquist)

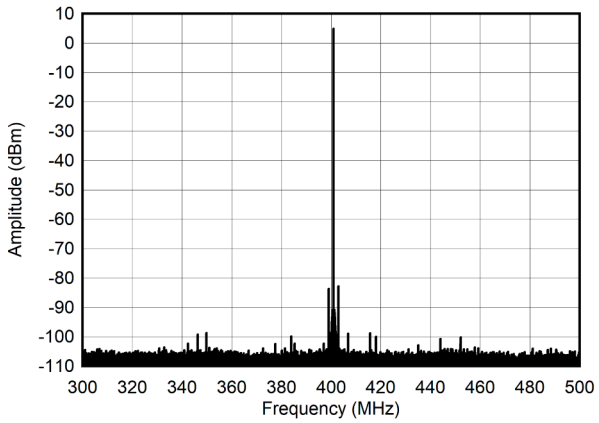


図 5-249. Single Tone Spectrum at 400 MHz and -1 dBFS (±100MHz)

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

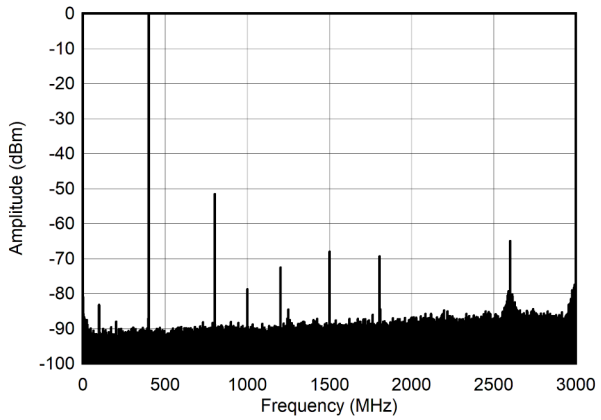


図 5-250. Single Tone Spectrum at 400 MHz and -6 dBFS (Nyquist)

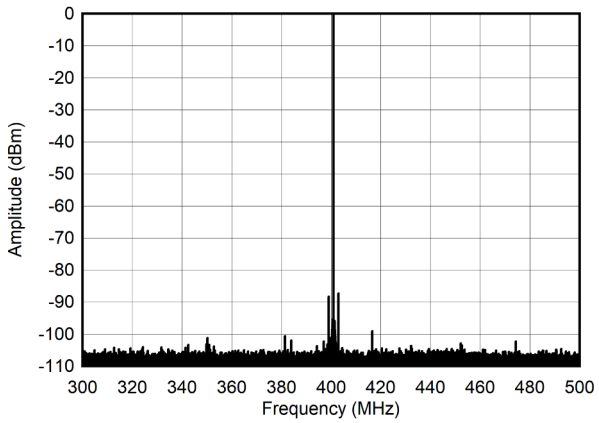


図 5-251. Single Tone Spectrum at 400 MHz and -6 dBFS (±100MHz)

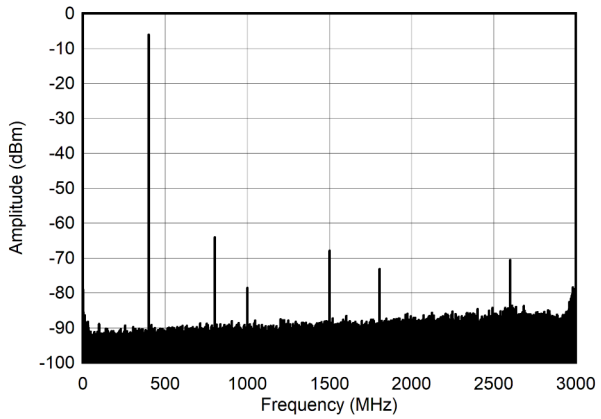


図 5-252. Single Tone Spectrum at 400 MHz and -12 dBFS (Nyquist)

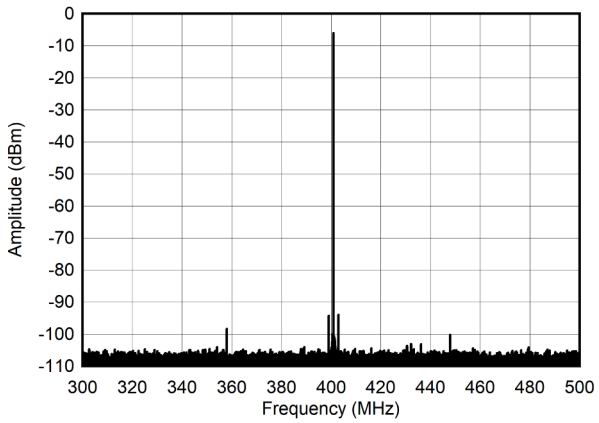


図 5-253. Single Tone Spectrum at 400 MHz and -12 dBFS (±100MHz)

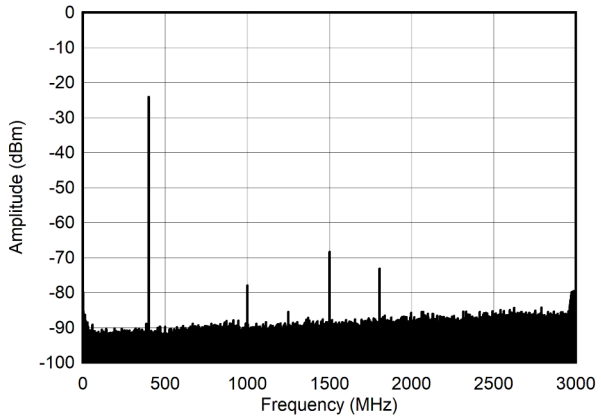


図 5-254. Single Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)

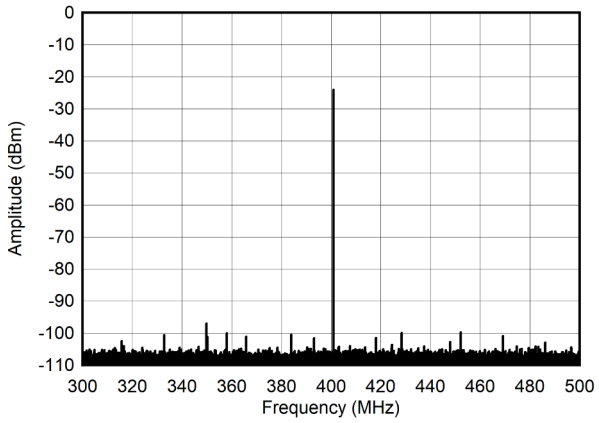


図 5-255. Single Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)

Copyright © 2023 Texas Instruments Incorporated

5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

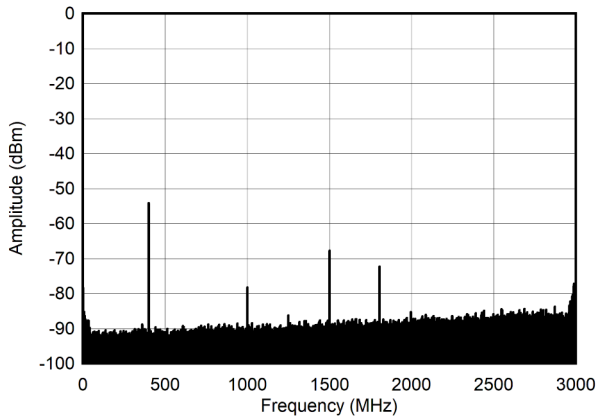


図 5-256. Single Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)

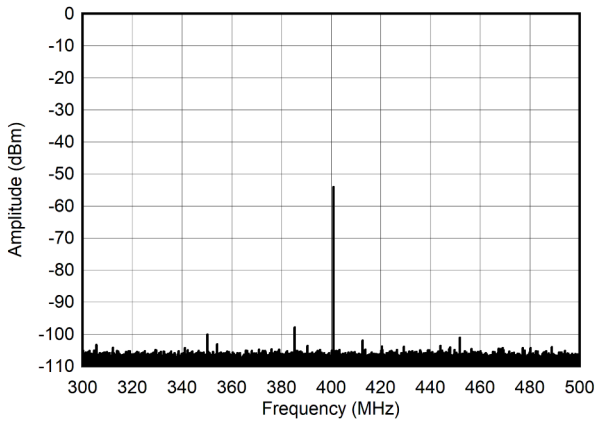
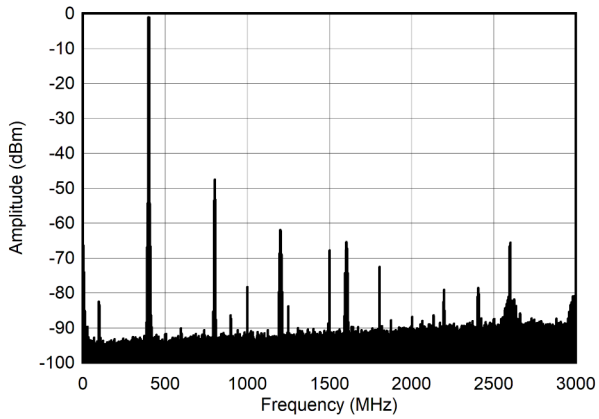
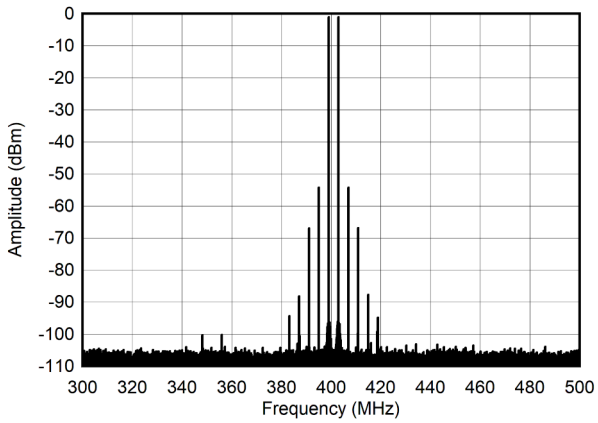


図 5-257. Single Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)



Tone Spacing = 4 MHz

図 5-258. Dual Tone Spectrum at 400 MHz and -7 dBFS (Nyquist)

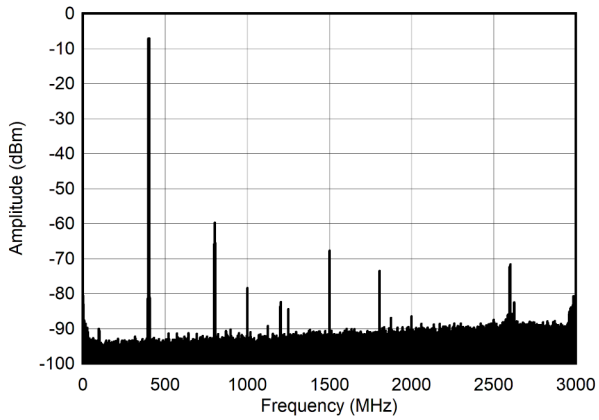


Tone Spacing = 4 MHz

図 5-259. Dual Tone Spectrum at 400 MHz and -7 dBFS (±100MHz)

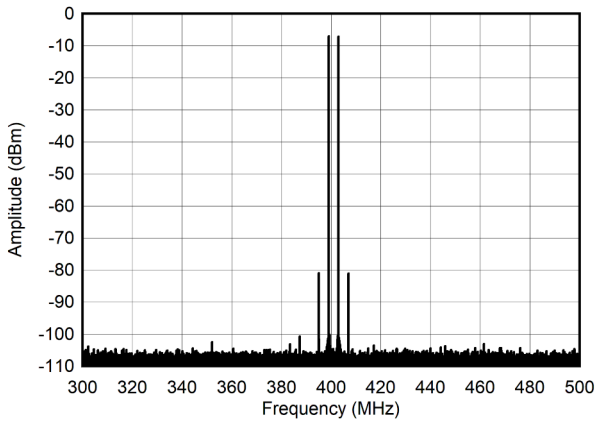
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



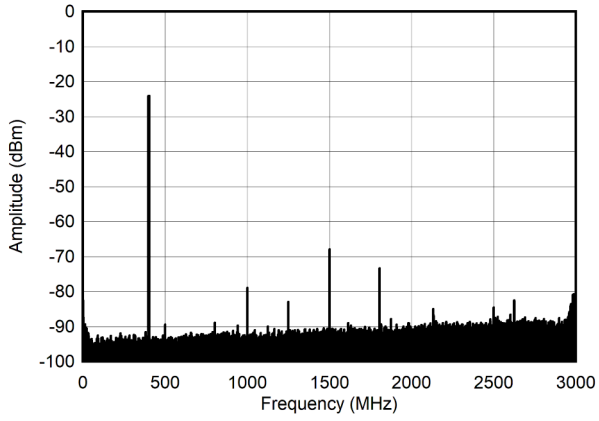
Tone Spacing = 4 MHz

図 5-260. Dual Tone Spectrum at 400 MHz and -13 dBFS (Nyquist)



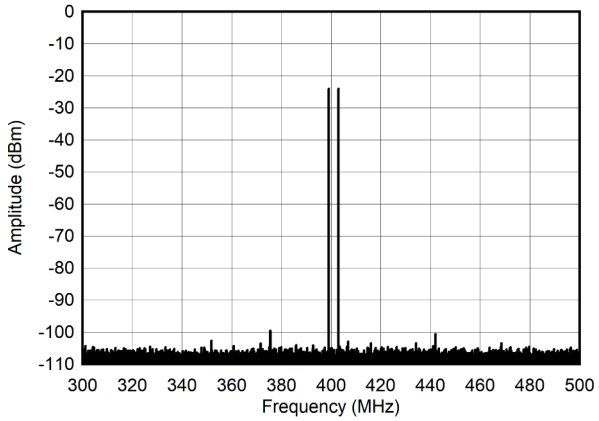
Tone Spacing = 4 MHz

図 5-261. Dual Tone Spectrum at 400 MHz and -13 dBFS (±100MHz)



Tone Spacing = 4 MHz

図 5-262. Dual Tone Spectrum at 400 MHz and -30 dBFS (Nyquist)



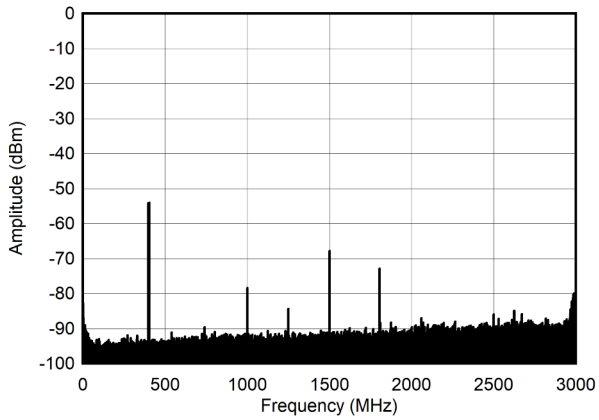
Tone Spacing = 4 MHz

図 5-263. Dual Tone Spectrum at 400 MHz and -30 dBFS (±100MHz)

Copyright © 2023 Texas Instruments Incorporated

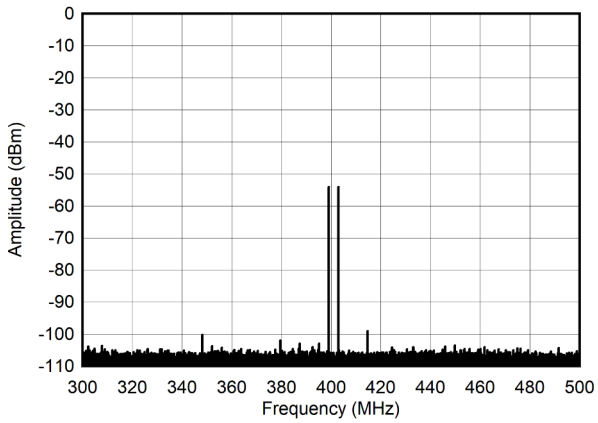
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



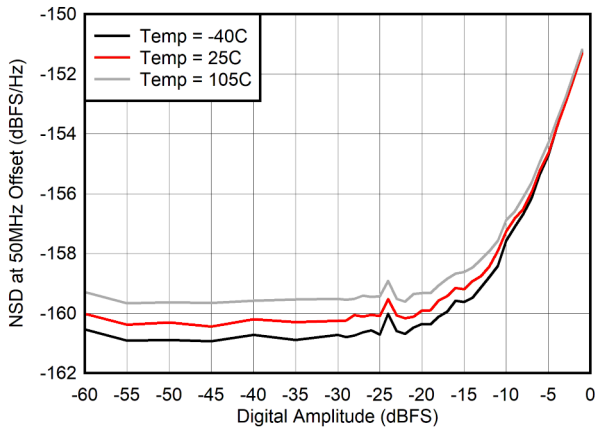
Tone Spacing = 4 MHz

図 5-264. Dual Tone Spectrum at 400 MHz and -60 dBFS (Nyquist)



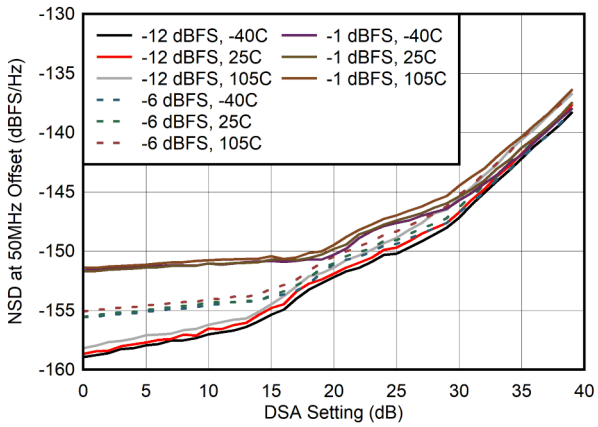
Tone Spacing = 4 MHz

図 5-265. Dual Tone Spectrum at 400 MHz and -60 dBFS (±100MHz)



measured at 50 MHz offset

図 5-266. Noise Spectral Density vs Digital Amplitude at 400 MHz

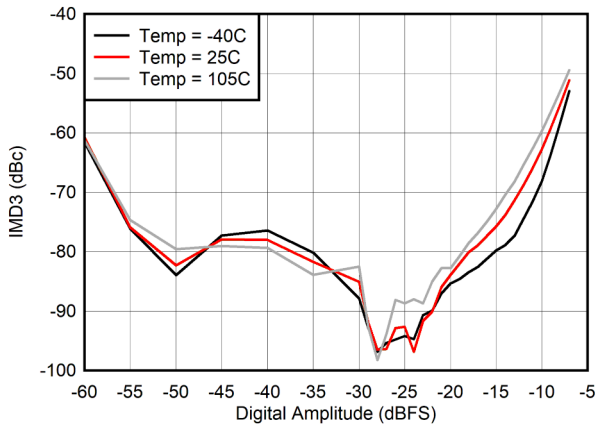


measured at 50 MHz offset

図 5-267. Noise Spectral Density vs DSA Setting at 400 MHz

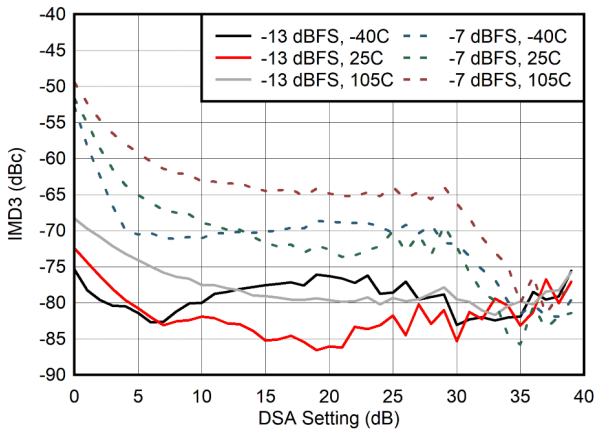
5.12.7 TX Typical Characteristics at 30MHz and 400MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Default conditions: TX input data rate = 125 MSPS, f_{DAC} = 6000 MSPS (48x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with f_{REF} = 500 MHz. Additional default conditions for all plots, A_{OUT} = –1 dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



Tone Spacing = 4 MHz

図 5-268. IMD3 vs Digital Amplitude at 400 MHz



Tone Spacing = 4 MHz

図 5-269. IMD3 vs DSA Setting at 400 MHz

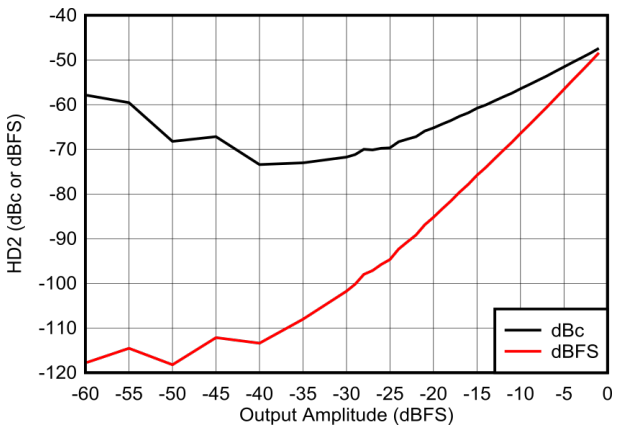


図 5-270. HD2 vs Amplitude at 400 MHz

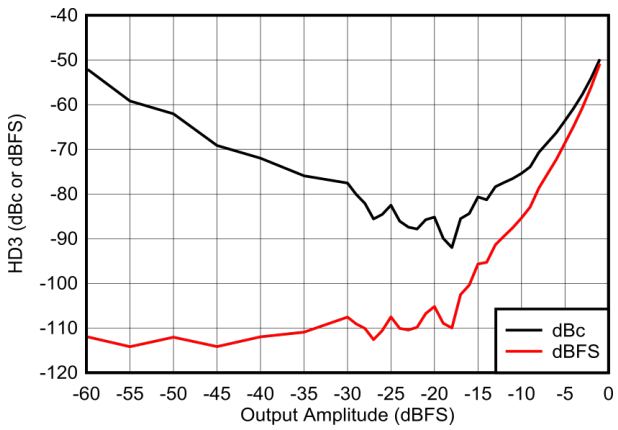
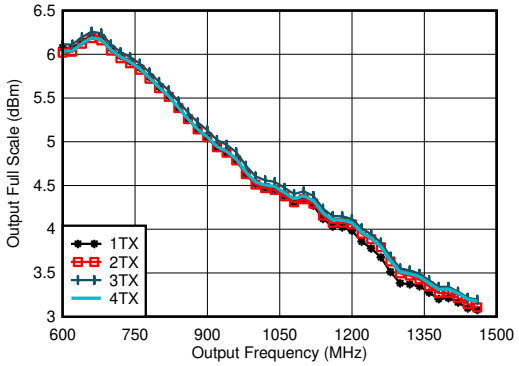


図 5-271. HD3 vs Amplitude at 400 MHz

Copyright © 2023 Texas Instruments Incorporated

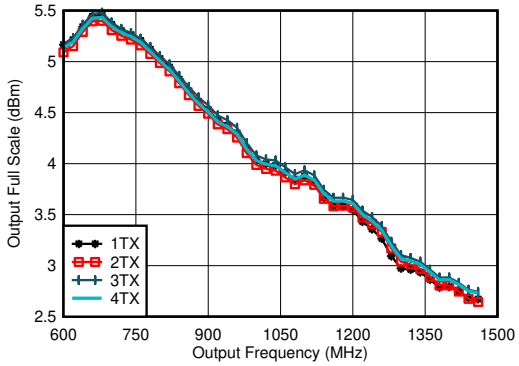
5.12.8 TX Typical Characteristics at 800MHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



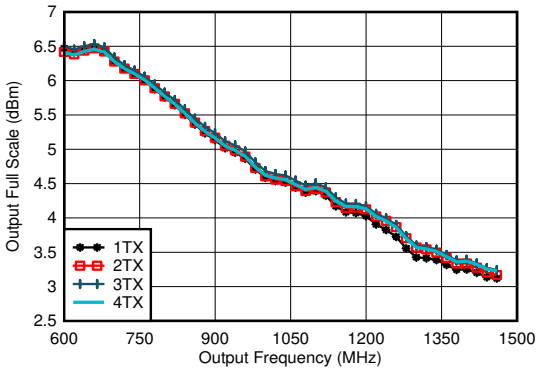
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-272. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Straight Mode



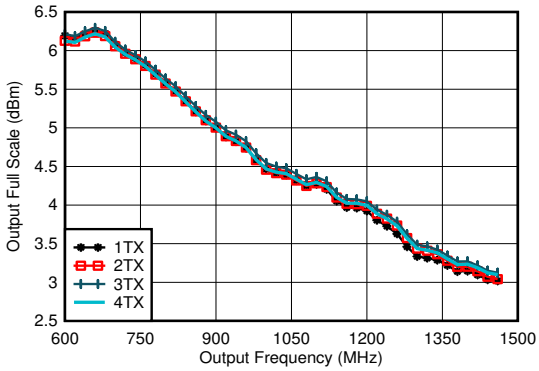
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHzmatching

図 5-273. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Straight Mode



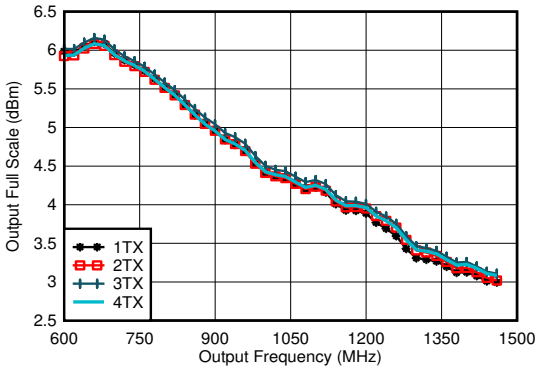
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-274. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Interleave Mode



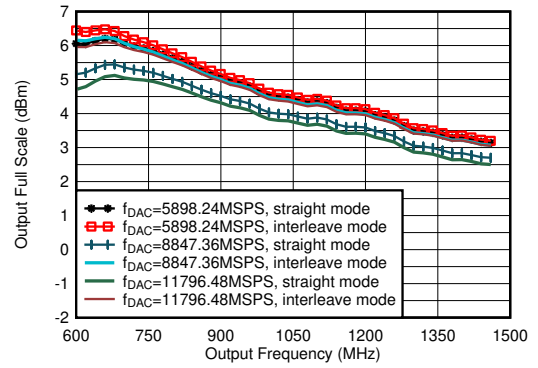
Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-275. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Interleave Mode



Including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-276. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS, Interleave Mode



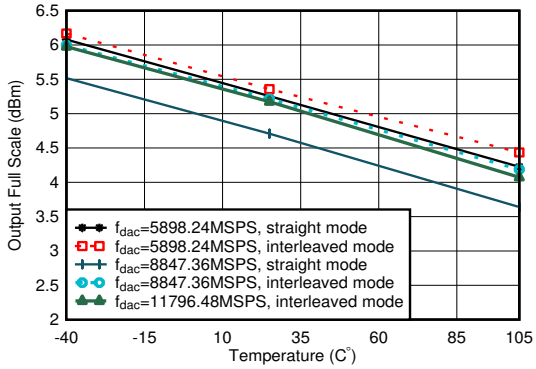
including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-277. TX Output Fullscale vs Output Frequency

Copyright © 2023 Texas Instruments Incorporated

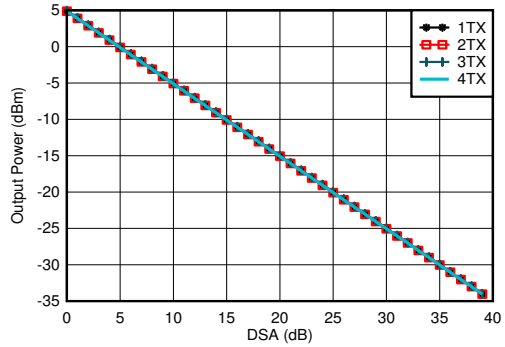
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



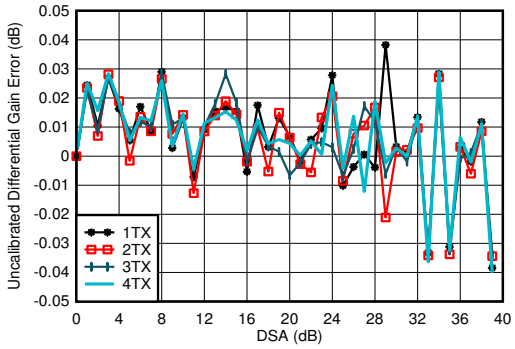
including PCB and cable losses, A_{out} = -0.5dFBS, DSA = 0, 0.8 GHz matching

図 5-278. TX Output Fullscale vs Temperature



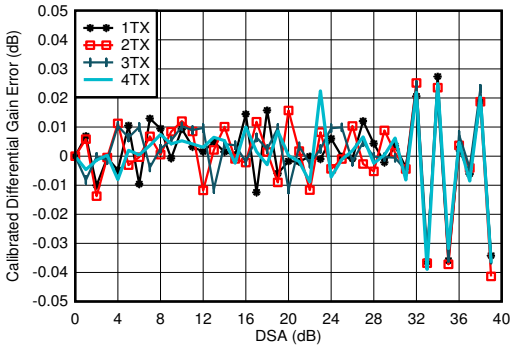
f_{DAC} = 11796.48 MSPS, interleave mode, A_{out} = -0.5dFBS, matching 0.8 GHz

図 5-279. TX Output Power vs DSA Setting and Channel at 0.85 GHz



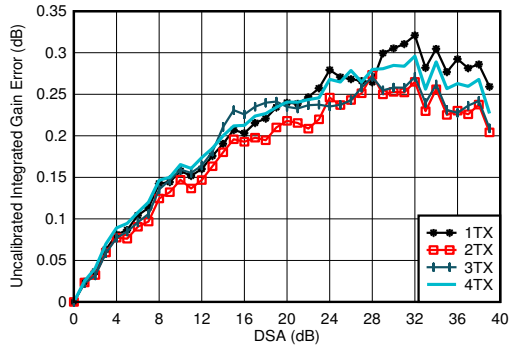
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-280. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



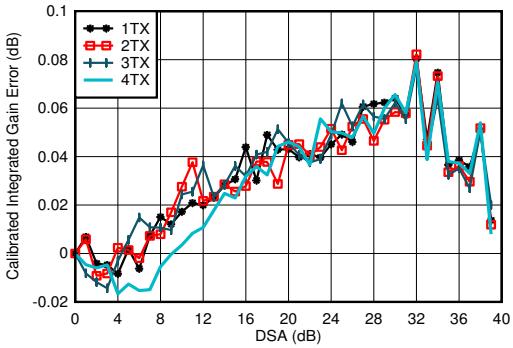
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-281. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Settings

図 5-282. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



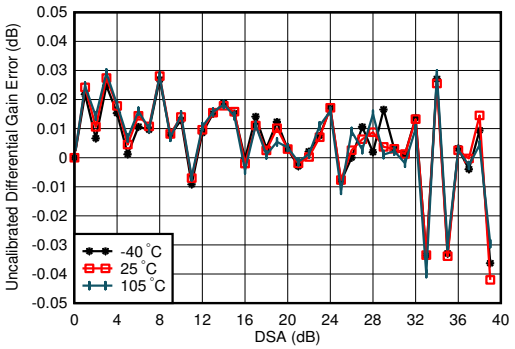
f_{DAC}=5898.24MSPS, interleave mode, matching at 0.8 GHz Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 5-283. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

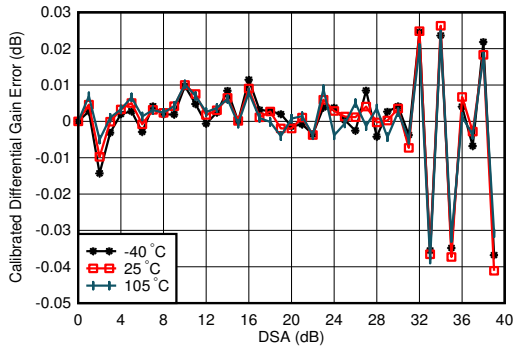
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



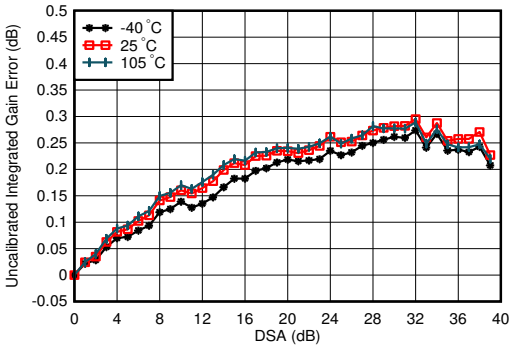
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-284. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



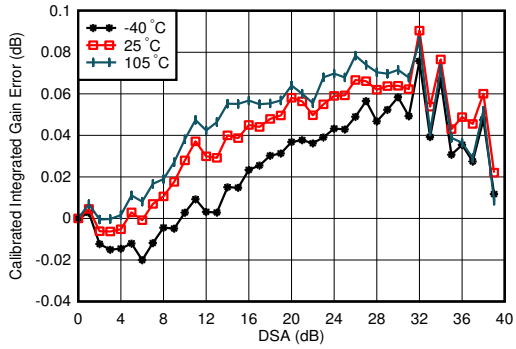
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-285. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 5-286. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

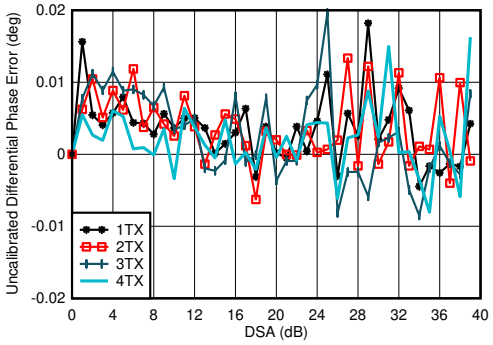


f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + DSA Setting

図 5-287. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

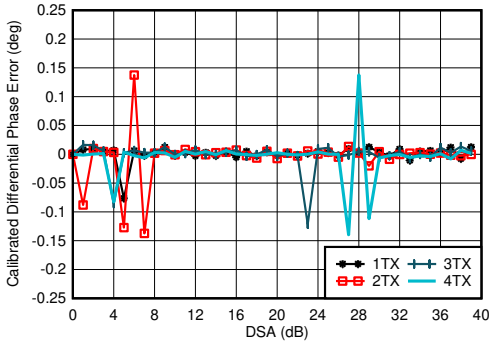
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



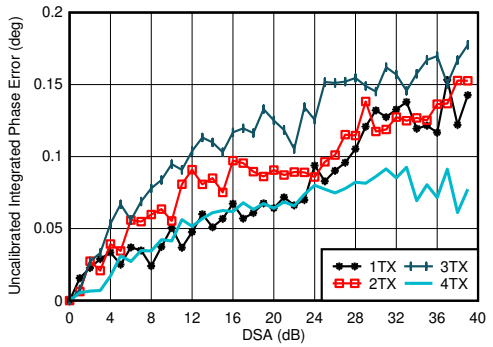
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-288. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



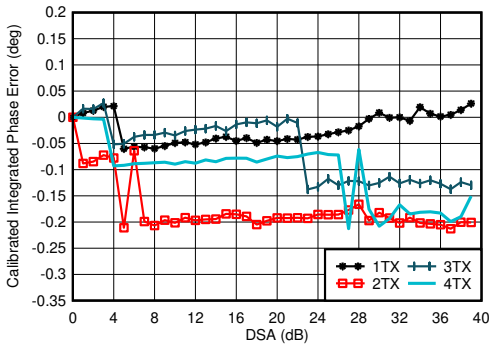
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 5-289. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 5-290. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



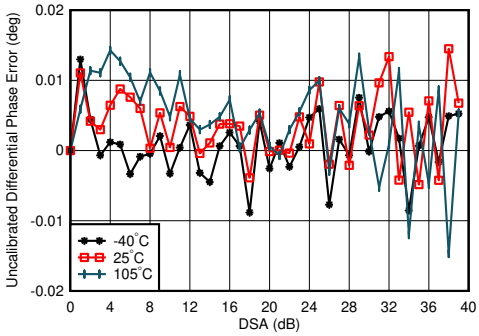
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 5-291. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

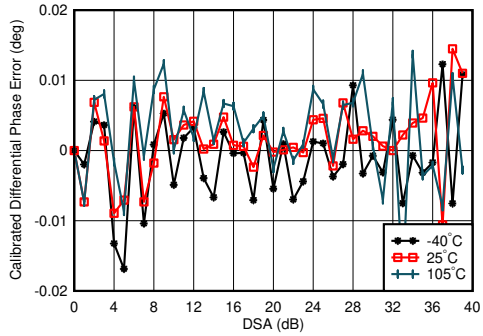
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



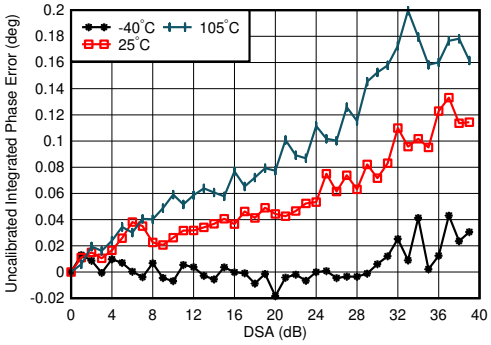
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 5-292. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



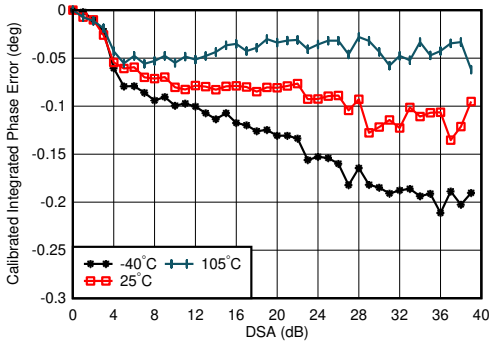
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting) + 1

図 5-293. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



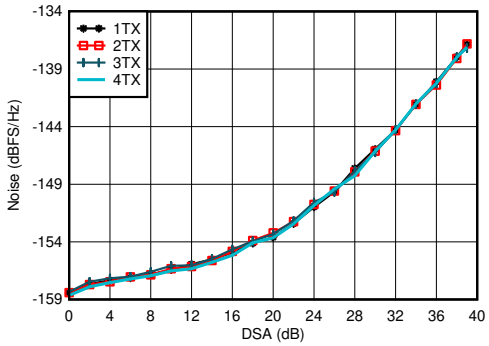
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 5-294. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



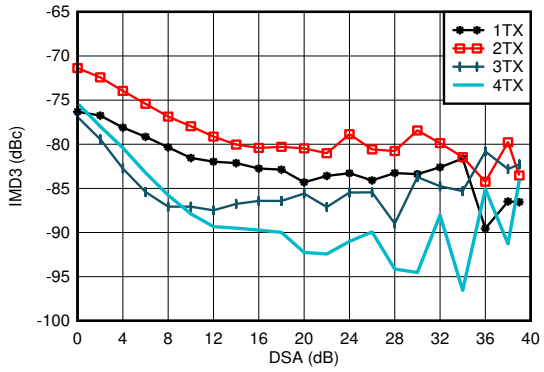
f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $Phase_{OUT}$(DSA Setting) – $Phase_{OUT}$(DSA Setting = 0)

図 5-295. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, matching at 0.8 GHz, P_{OUT} = –13 dBFS

図 5-296. TX Output Noise vs Channel and Attenuation at 0.85 GHz



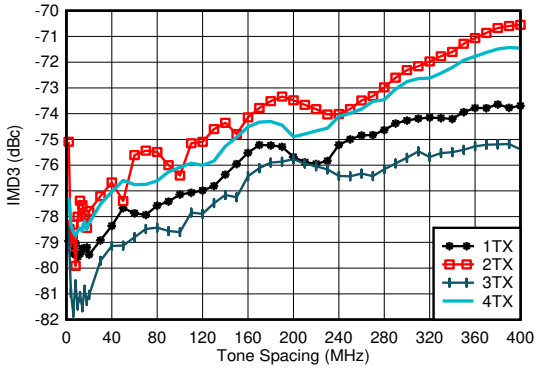
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 5-297. TX IMD3 vs DSA Setting at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

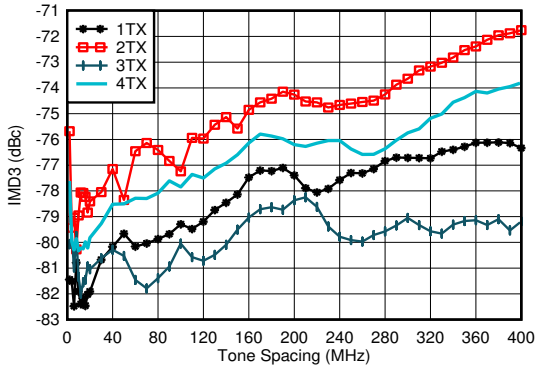
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



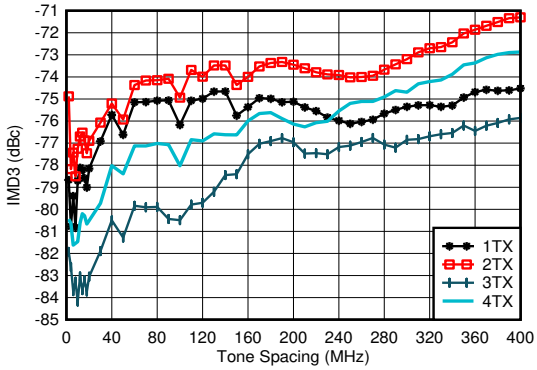
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 5-298. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



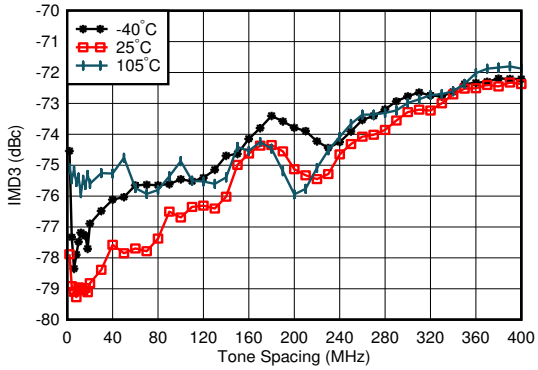
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 5-299. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



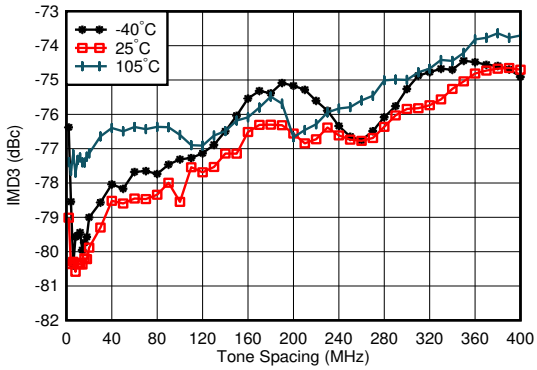
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone

図 5-300. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



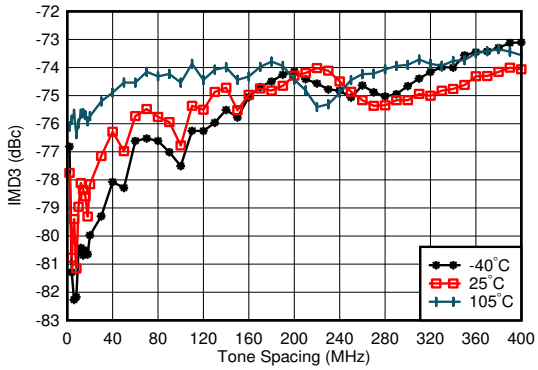
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 5-301. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 5-302. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



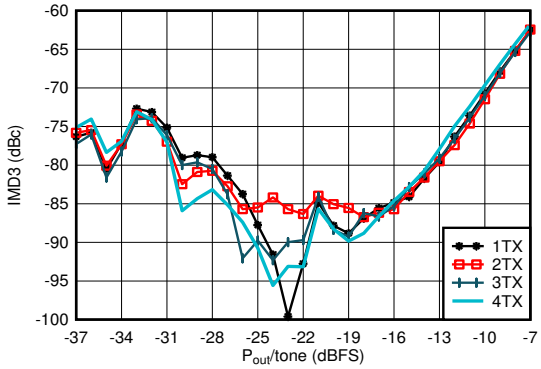
f_{DAC} = 11796.48MSPS, straight mode, f_{CENTER} =0.85 GHz, matching at 0.8 GHz, –13 dBFS each tone, worst channel

図 5-303. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

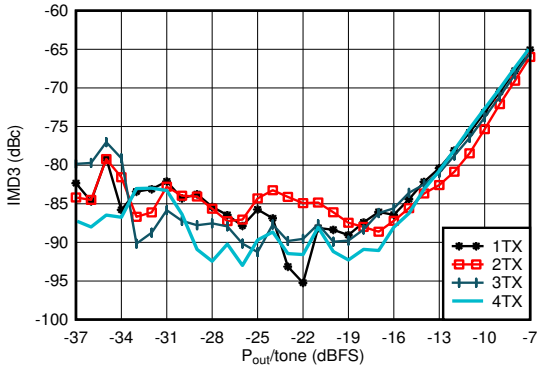
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



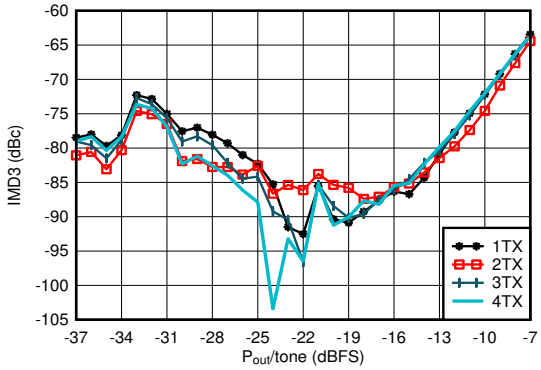
f_{DAC} = 5898.24MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 5-304. TX IMD3 vs Digital Level at 0.85 GHz



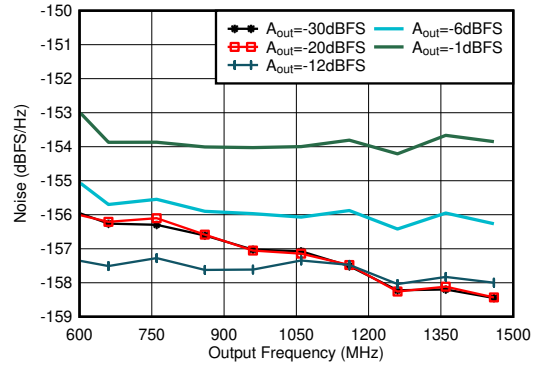
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 5-305. TX IMD3 vs Digital Level at 0.85 GHz



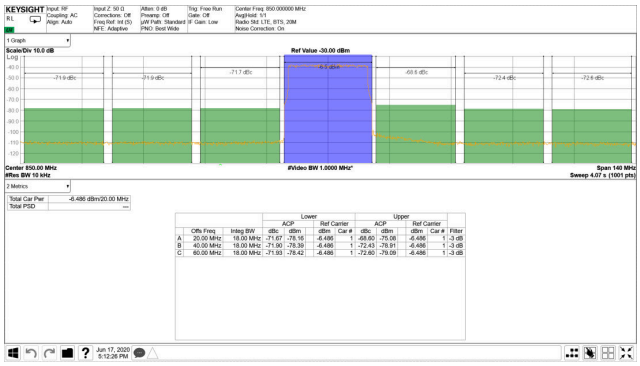
f_{DAC} = 11796.48MSPS, interleave mode, f_{CENTER} = 0.85 GHz, $f_{SPACING}$ = 20 MHz, matching at 0.8 GHz

図 5-306. TX IMD3 vs Digital Level at 0.85 GHz



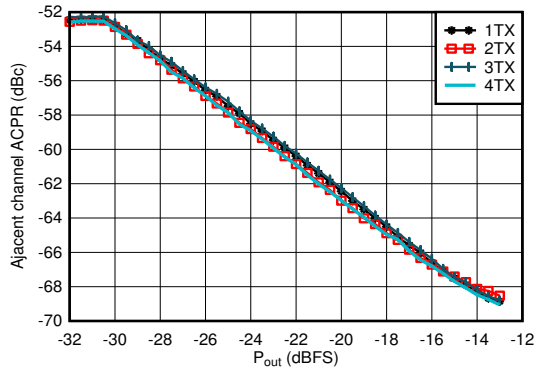
Matching at 0.8 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset, DSA = 0dB

図 5-307. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-308. TX 20-MHz LTE Output Spectrum at 0.85 GHz



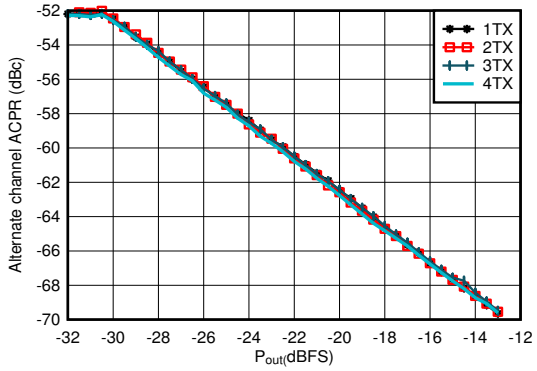
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-309. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

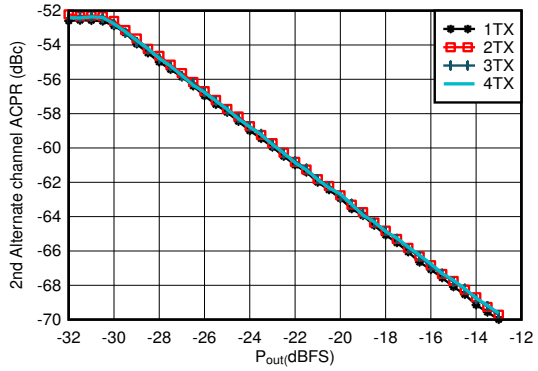
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



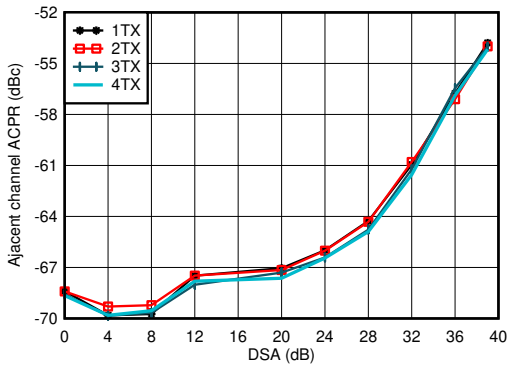
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-310. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz



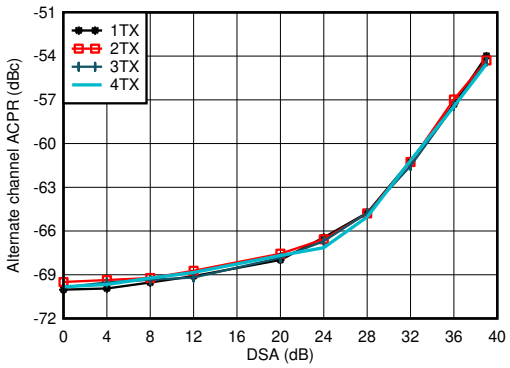
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-311. TX 20-MHz LTE alt2-ACPR vs Digital Level at 0.85 GHz



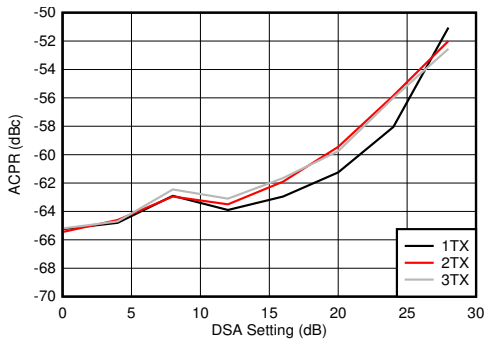
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-312. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



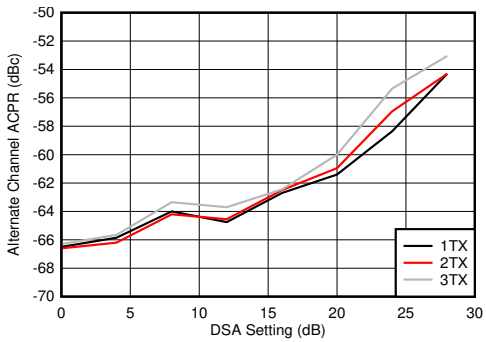
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-313. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-314. TX 100-MHz NR ACPR vs DSA at 0.85 GHz



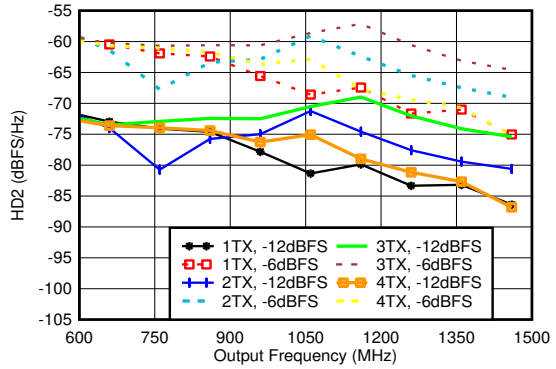
Matching at 0.8 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-315. TX 100-MHz NR alt-ACPR vs DSA at 0.85 GHz

Copyright © 2023 Texas Instruments Incorporated

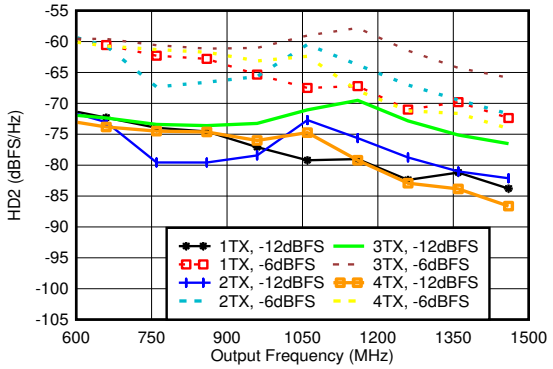
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



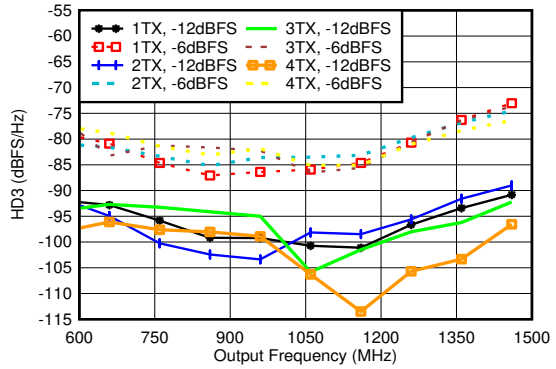
Matching at 0.8 GHz, f_{DAC} = 5898.24GSPS, straight mode

図 5-316. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



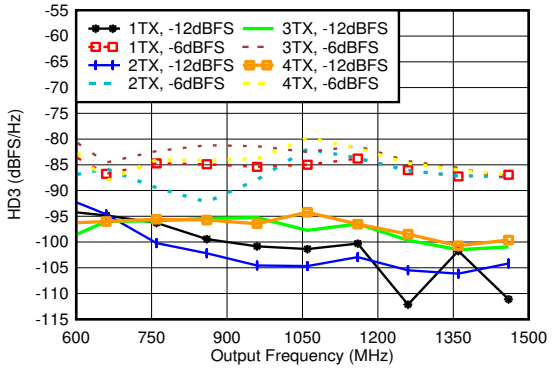
Matching at 0.8 GHz, f_{DAC} = 8847.36GSPS, straight mode

図 5-317. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



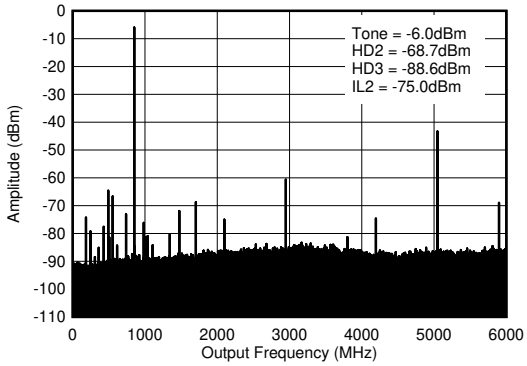
Matching at 0.8 GHz, f_{DAC} = 5898.24MSPS, straight mode, normalized to output power at harmonic frequency

図 5-318. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



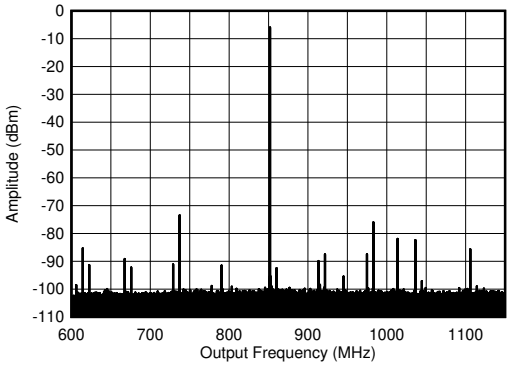
Matching at 0.8 GHz, f_{DAC} = 8847.36MSPS, straight mode, normalized to output power at harmonic frequency

図 5-319. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz



f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-320. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



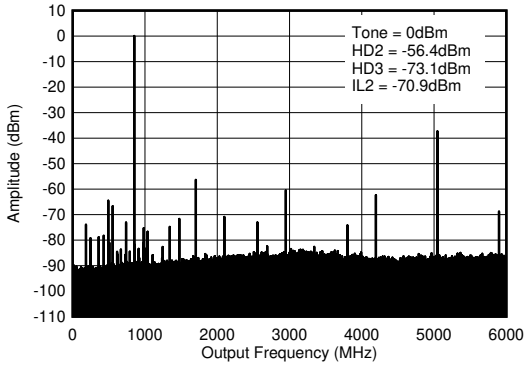
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 5-321. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

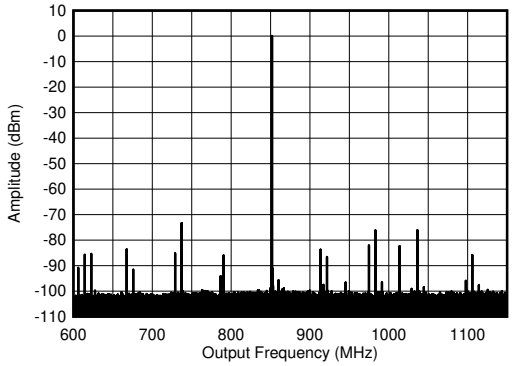
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



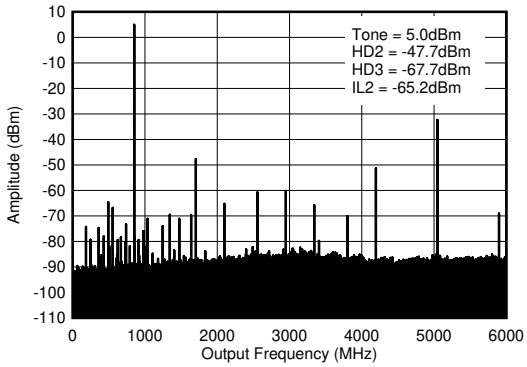
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-322. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



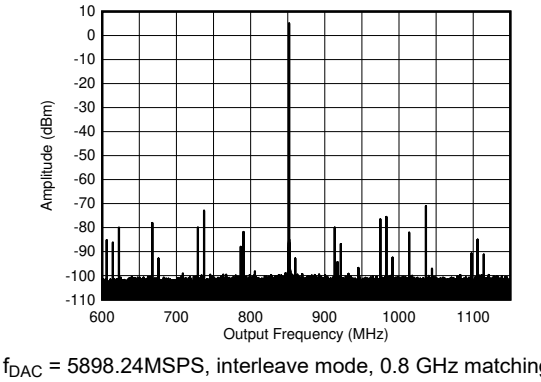
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 5-323. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



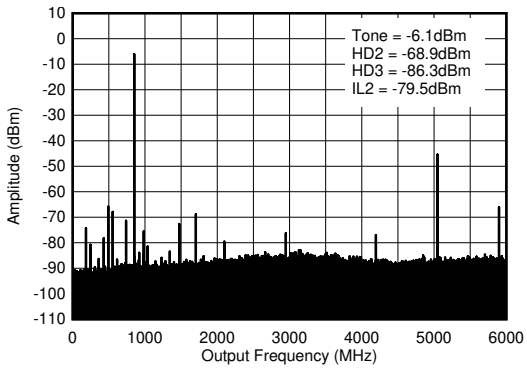
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-324. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



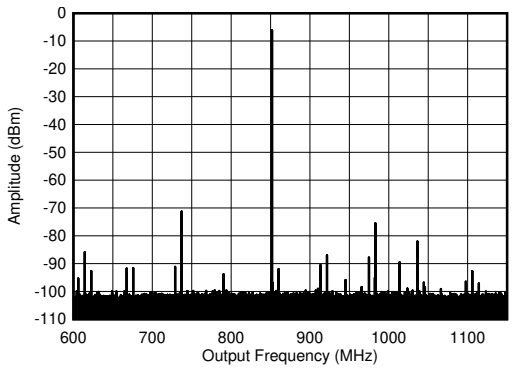
f_{DAC} = 5898.24MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses

図 5-325. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-326. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



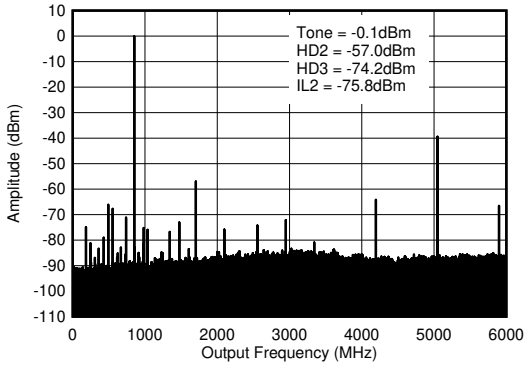
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 5-327. TX Single Tone (–12 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

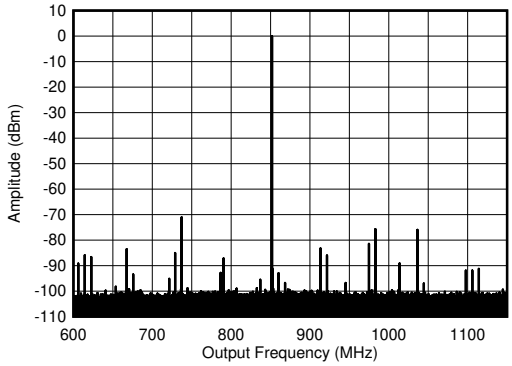
5.12.8 TX Typical Characteristics at 800MHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



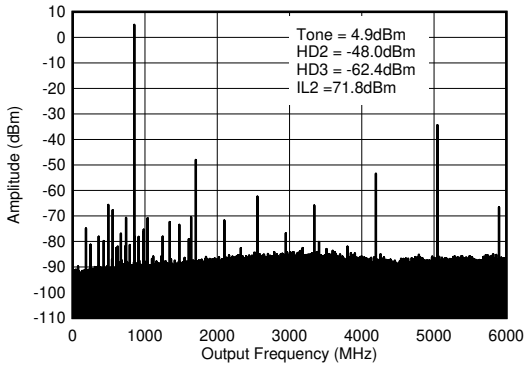
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-328. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



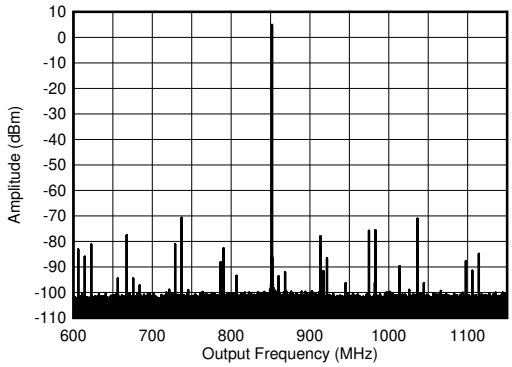
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 5-329. TX Single Tone (–6 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)



f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-330. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (0-f_{DAC})



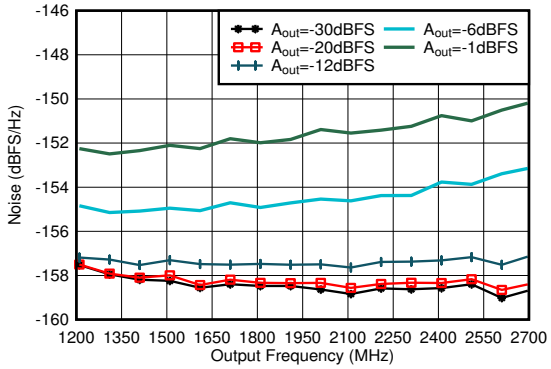
f_{DAC} = 5898.24MSPS, straight mode, 0.8 GHz matching, includes PCB and cable losses

図 5-331. TX Single Tone (–1 dBFS) Output Spectrum at 0.85 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

5.12.9 TX Typical Characteristics at 1.8GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

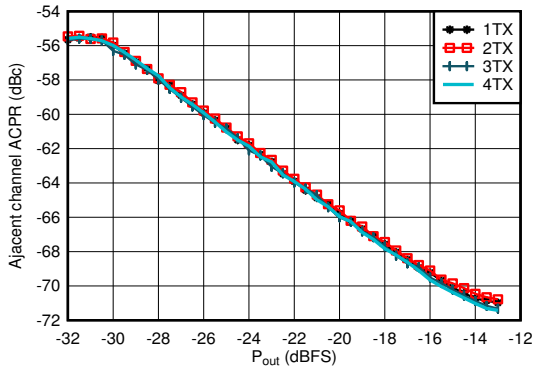


Matching at 1.8 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

図 5-332. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz

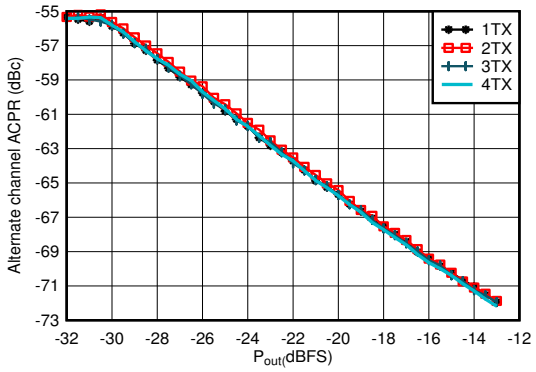
TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-333. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



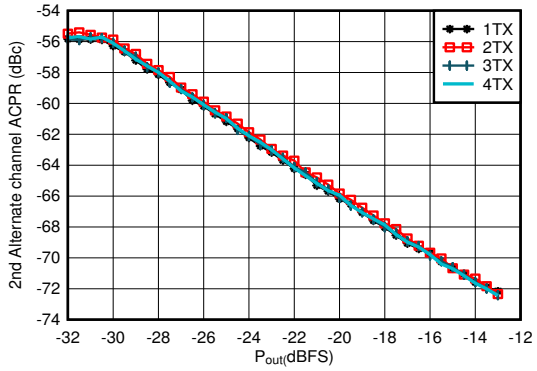
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-334. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



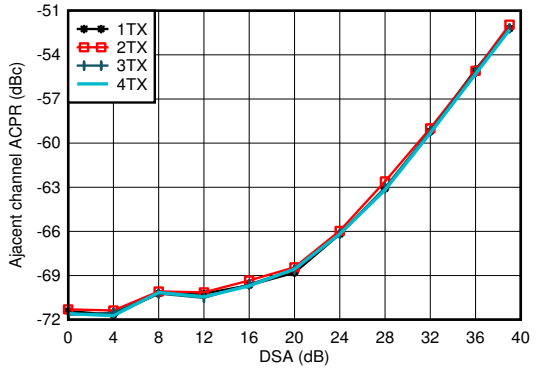
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-335. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-336. TX 20-MHz LTE alt2-ACPR vs Digital Level at 1.8425 GHz



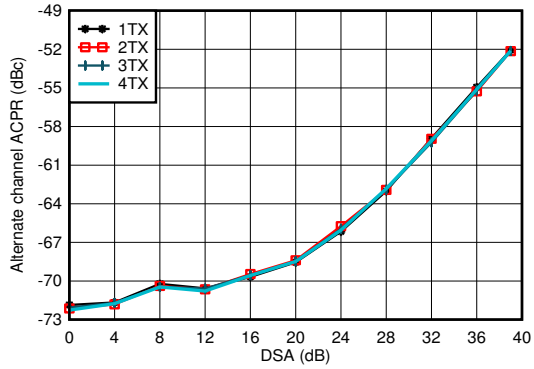
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-337. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

Copyright © 2023 Texas Instruments Incorporated

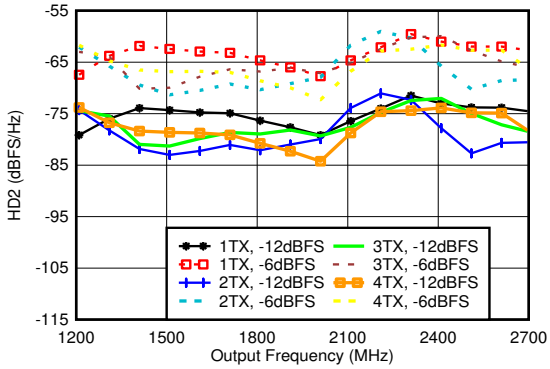
5.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



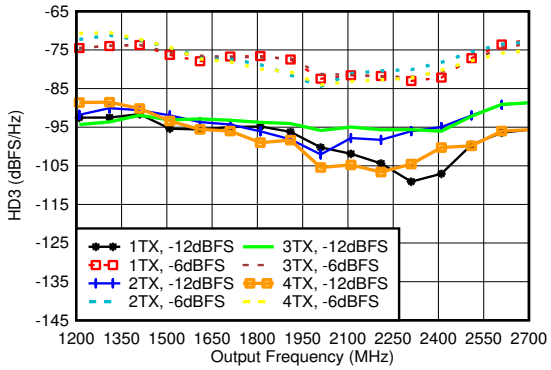
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-338. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



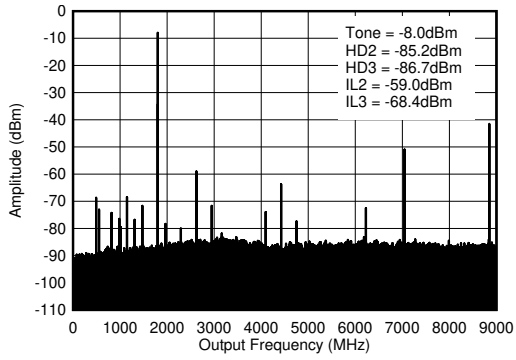
Matching at 1.8 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-339. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



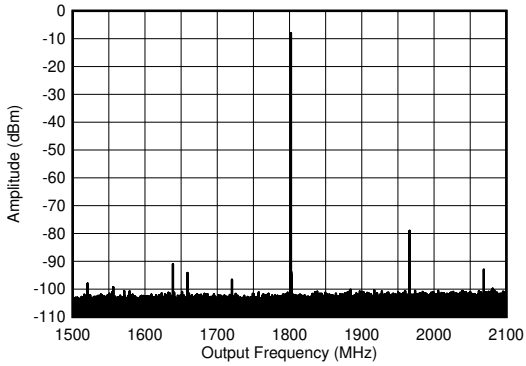
Matching at 1.8 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-340. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



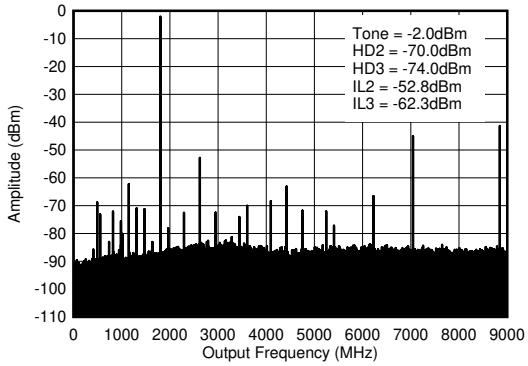
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-341. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 5-342. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



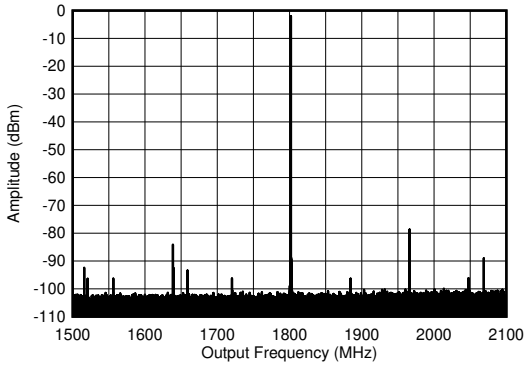
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-343. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

Copyright © 2023 Texas Instruments Incorporated

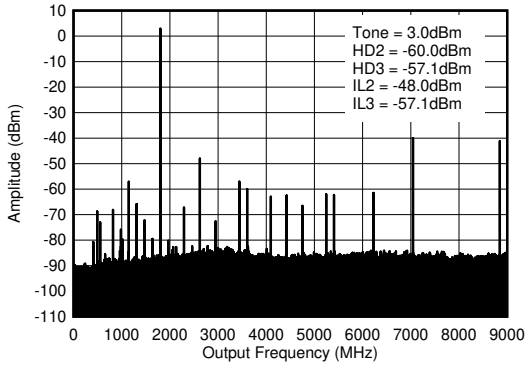
5.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



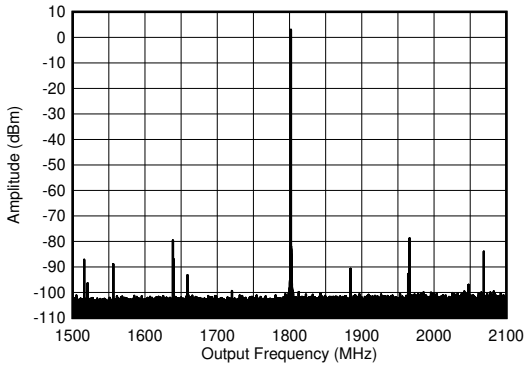
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 5-344. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



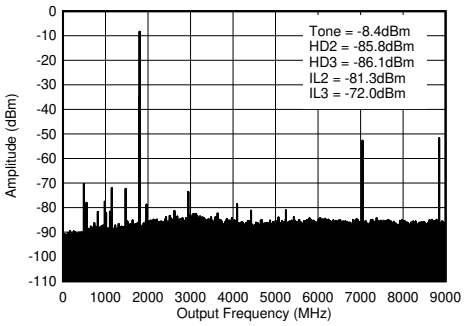
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-345. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



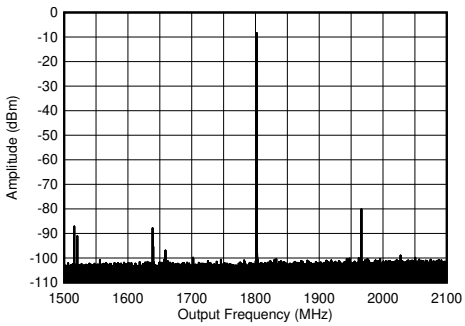
f_{DAC} = 8847.36MSPS, interleave mode, 1.8 GHz matching, includes PCB and cable losses

図 5-346. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



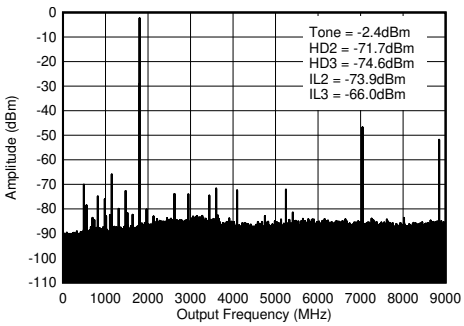
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-347. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})



f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 5-348. TX Single Tone (–12 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



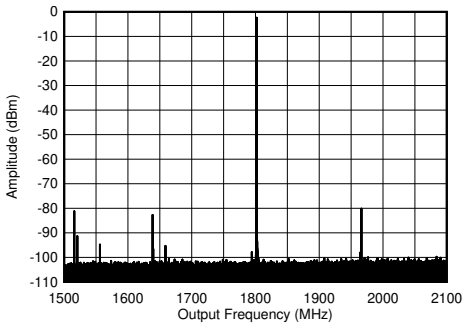
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-349. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

Copyright © 2023 Texas Instruments Incorporated

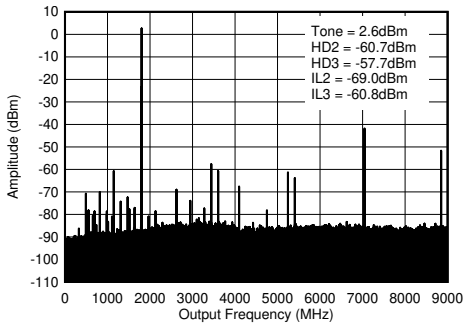
5.12.9 TX Typical Characteristics at 1.8GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



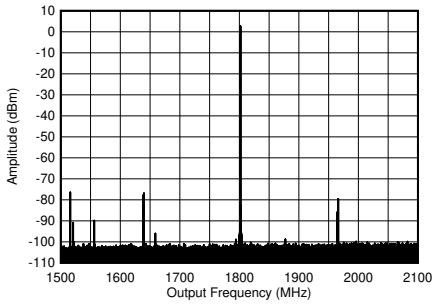
f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 5-350. TX Single Tone (–6 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-351. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (0-f_{DAC})

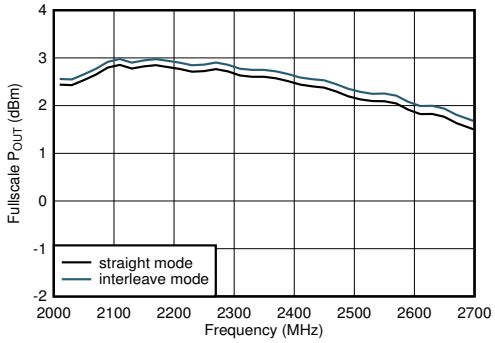


f_{DAC} = 8847.36MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses

図 5-352. TX Single Tone (–1 dBFS) Output Spectrum at 1.8 GHz (±300 MHz)

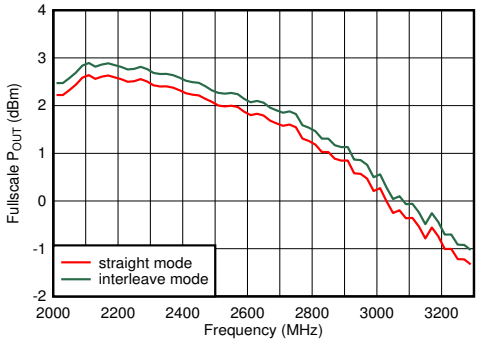
5.12.10 TX Typical Characteristics at 2.6GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



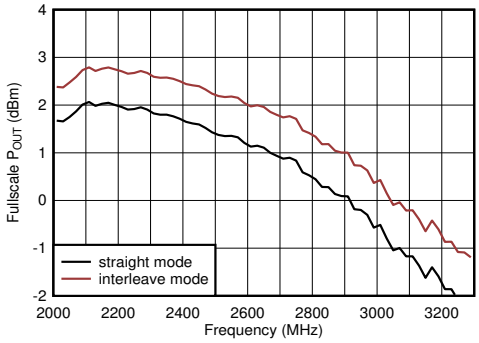
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

図 5-353. TX Full Scale vs RF Frequency at 5898.24MSPS



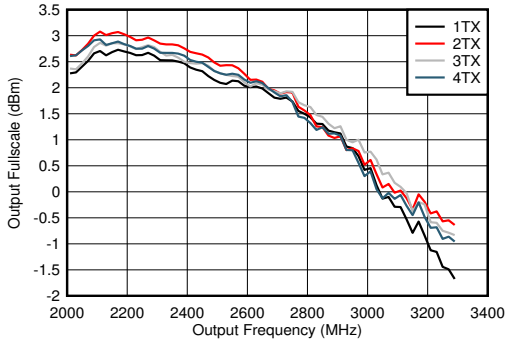
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

図 5-354. TX Full Scale vs RF Frequency at 8847.36MSPS



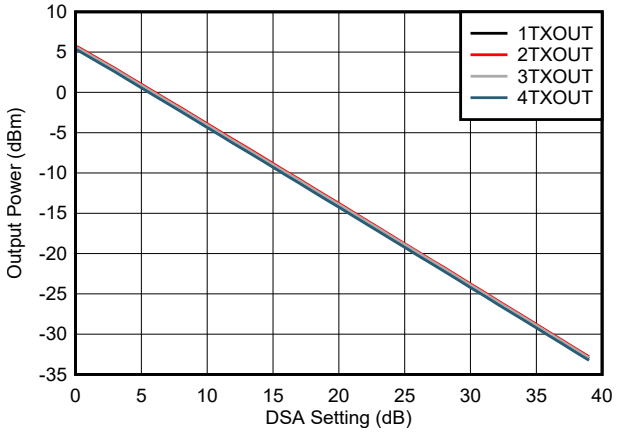
Including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

図 5-355. TX Full Scale vs RF Frequency at 11796.48MSPS



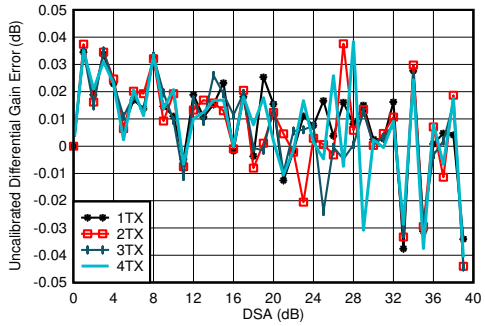
f_{DAC} = 8847.36MSPS, interleave mode, including PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 2.6 GHz matching

図 5-356. TX Output Fullscale vs Output Frequency and Channel



f_{DAC} = 8847.36 MSPS, A_{out} = -0.5dBFS, matching 2.6 GHz

図 5-357. TX Output Power vs DSA Setting and Channel at 2.6 GHz



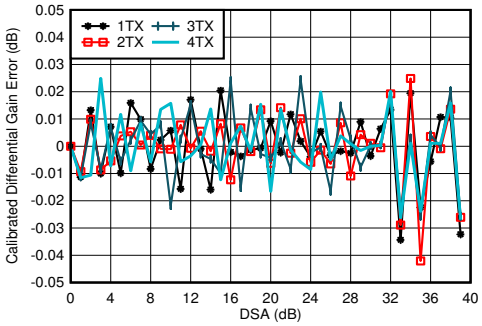
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-358. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

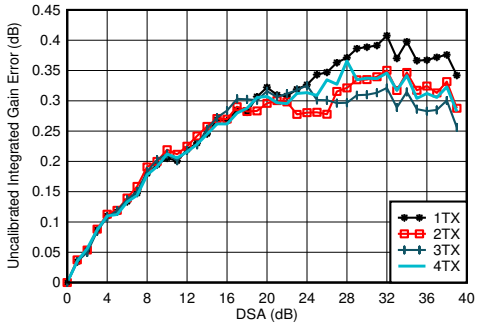
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



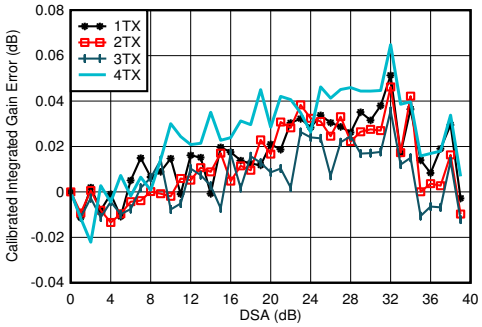
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-359. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



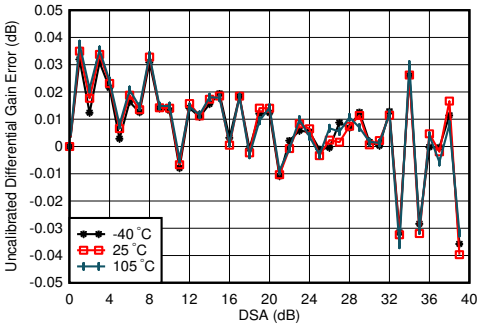
f_{DAC}=8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-360. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



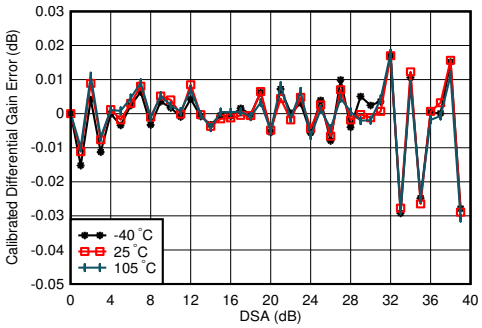
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-361. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz



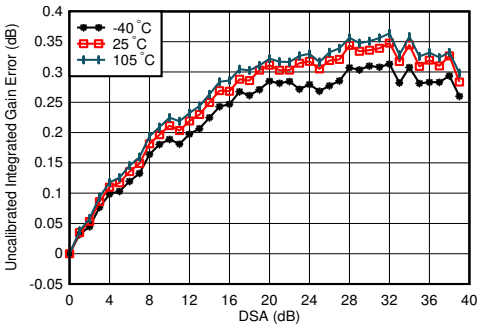
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-362. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-363. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



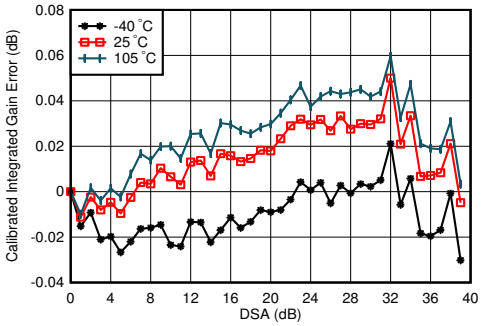
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-364. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

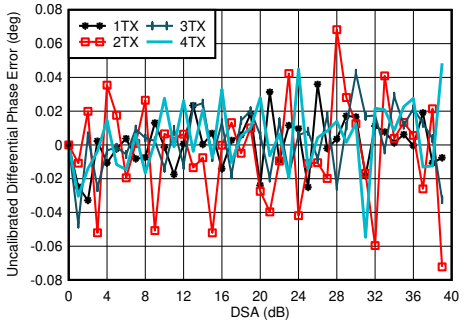
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



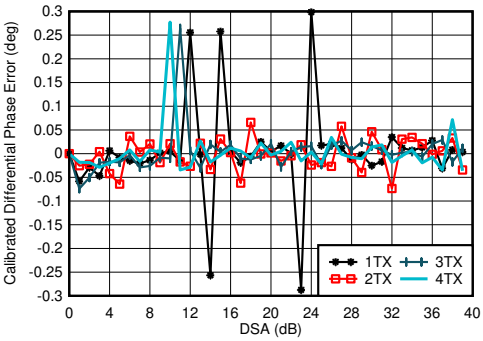
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-365. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz



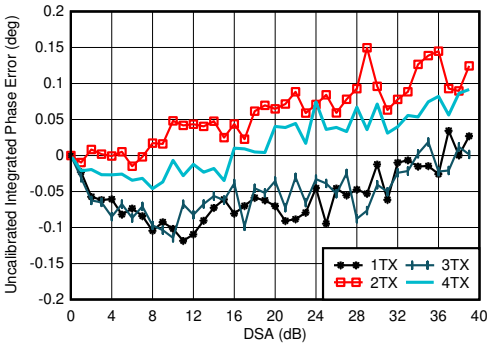
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-366. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)
Phase DNL spike may occur at any DSA setting.

図 5-367. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



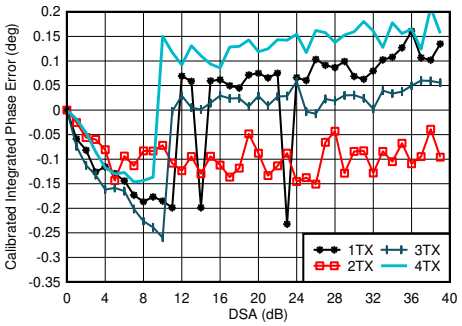
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-368. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

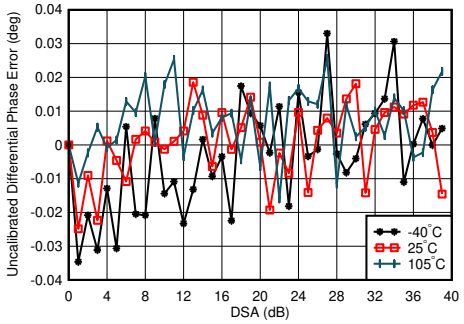
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



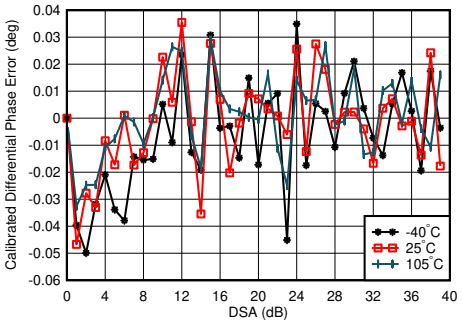
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-369. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz



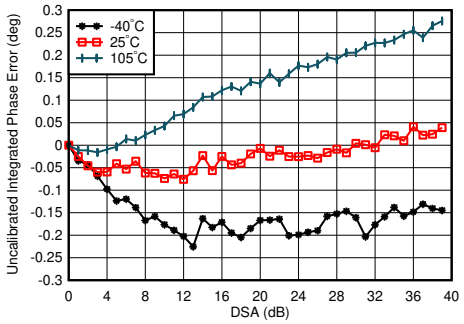
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-370. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



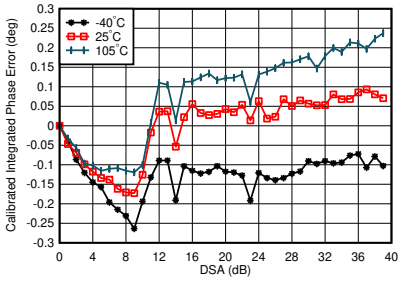
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-371. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



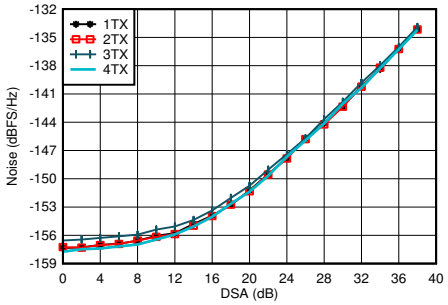
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-372. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-373. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



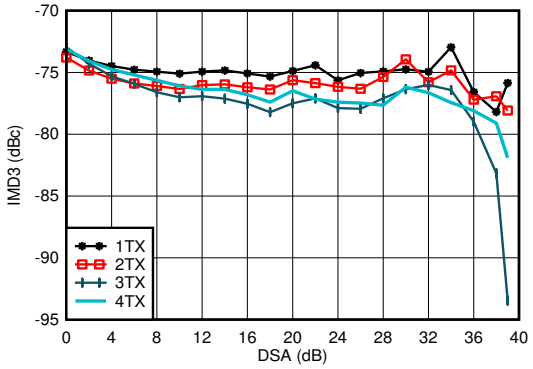
f_{DAC} = 8847.36MSPS, straight mode, matching at 2.6 GHz, P_{OUT} = –13 dBFS

図 5-374. TX Output Noise vs Channel and Attenuation at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

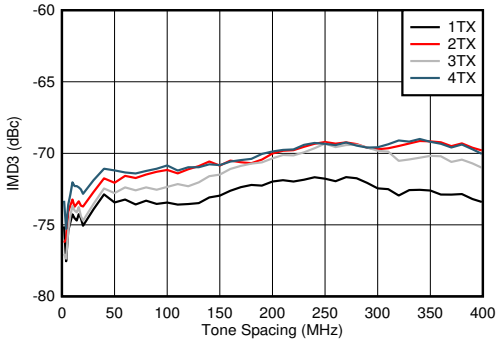
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



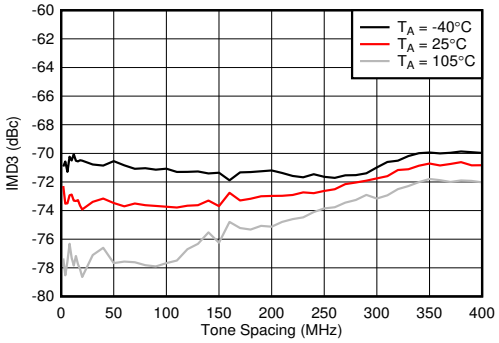
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 5-375. TX IMD3 vs DSA Setting at 2.6 GHz



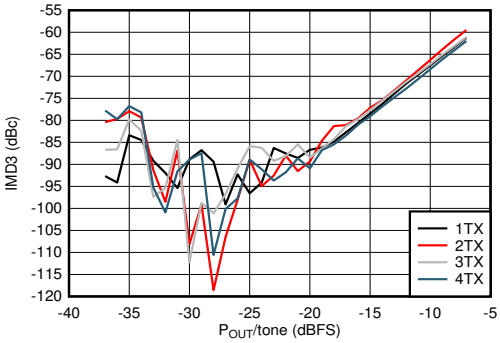
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 5-376. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



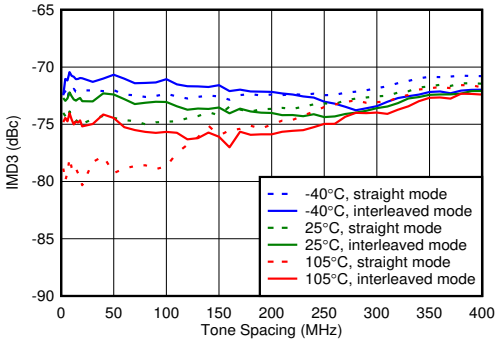
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone, worst channel.

図 5-377. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



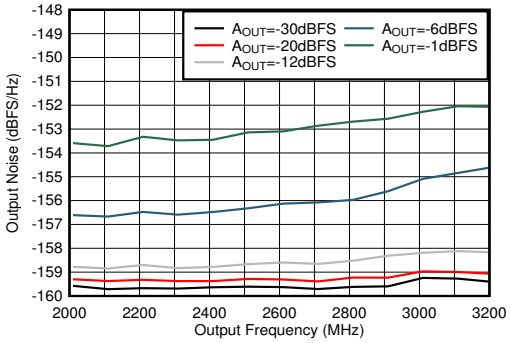
f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, $f_{SPACING}$ = 20 MHz, matching at 2.6 GHz

図 5-378. TX IMD3 vs Digital Level at 2.6 GHz



f_{DAC} = 8847.36MSPS, straight mode, f_{CENTER} = 2.6 GHz, matching at 2.6 GHz, –13 dBFS each tone

図 5-379. TX IMD3 vs Tone Spacing and Temperature



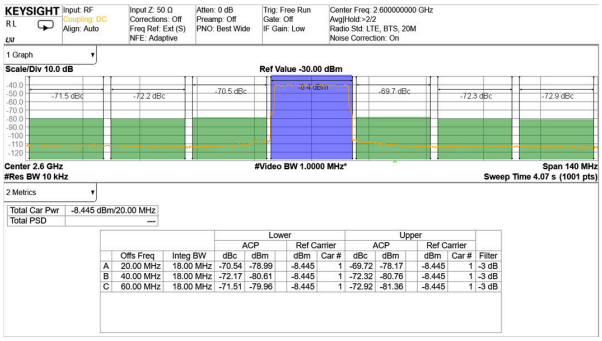
Matching at 2.6 GHz, Single tone, f_{DAC} = 11.79648GSPS, interleave mode, 40-MHz offset

図 5-380. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

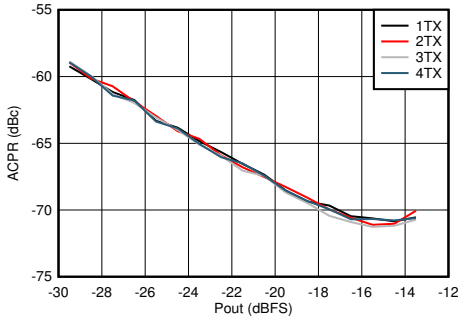
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



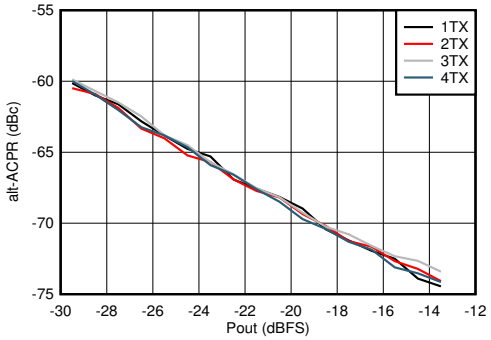
TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-381. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)



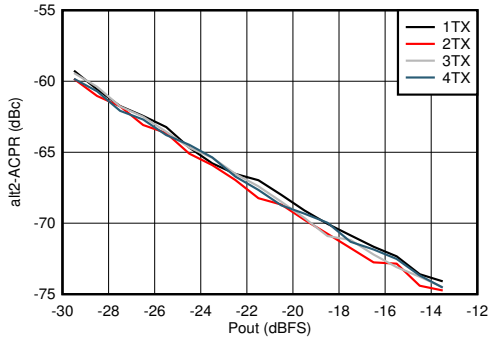
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-382. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



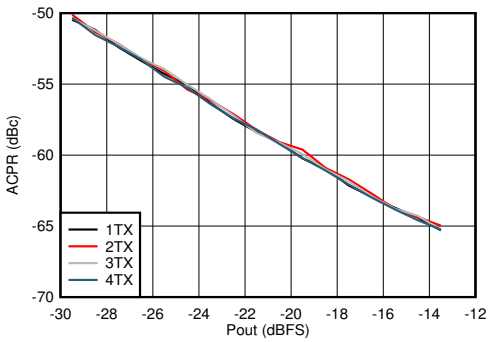
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-383. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



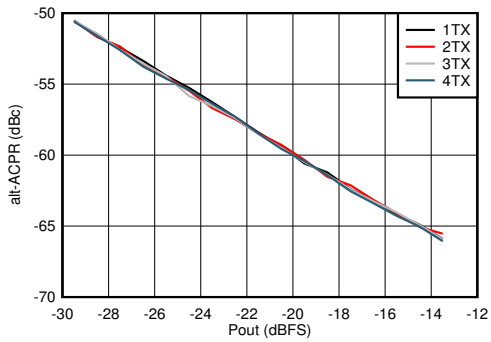
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-384. TX 20-MHz LTE alt2-ACPR vs Digital Level at 2.6 GHz



Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-385. TX 100-MHz NR ACPR vs Digital Level at 2.6 GHz



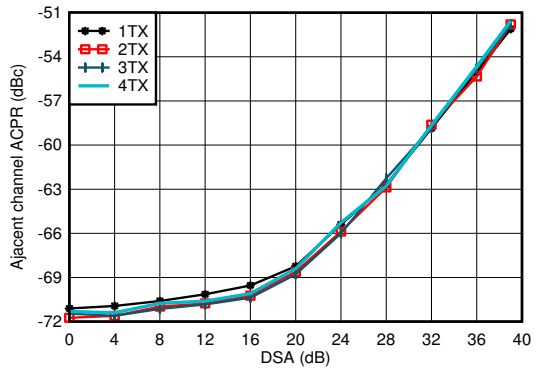
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-386. TX 100-MHz NR alt-ACPR vs Digital Level at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

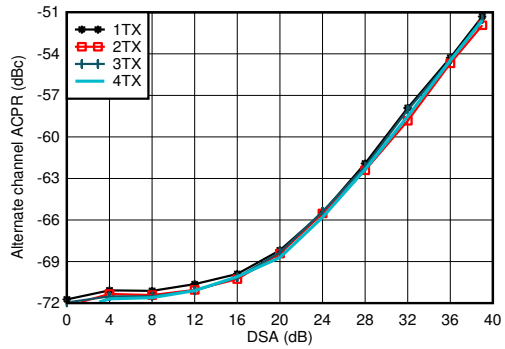
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



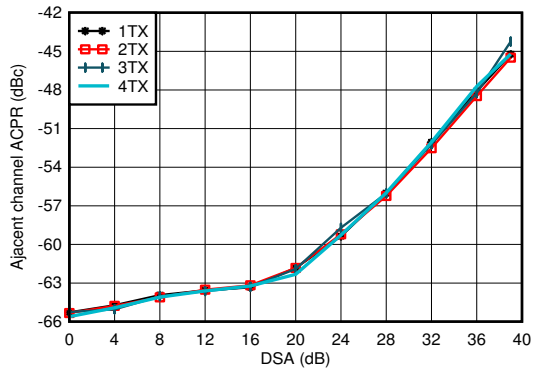
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-387. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



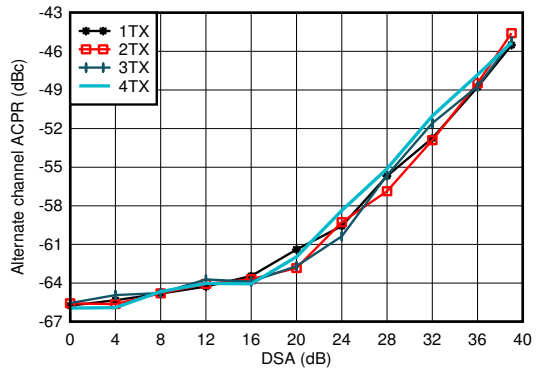
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-388. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



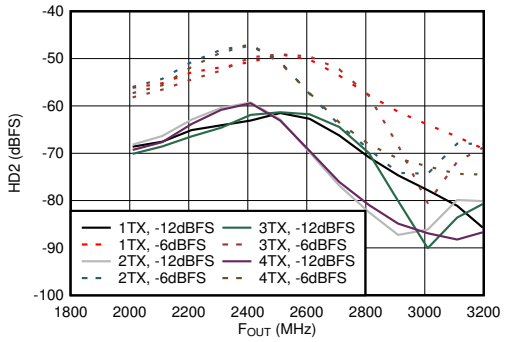
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-389. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



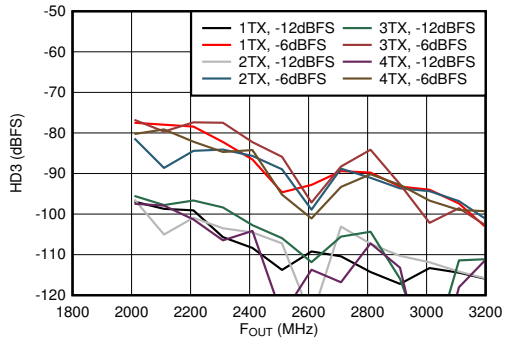
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-390. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-391. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



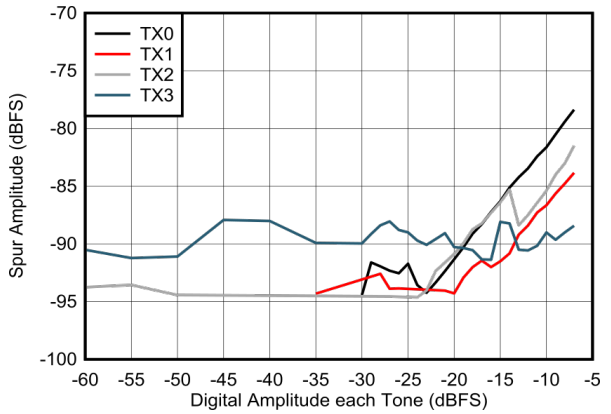
Matching at 2.6 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-392. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

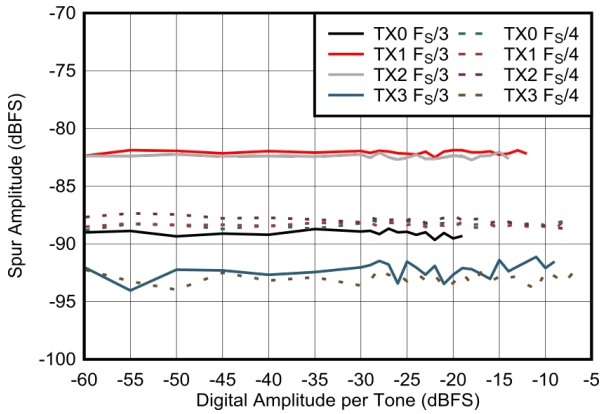
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



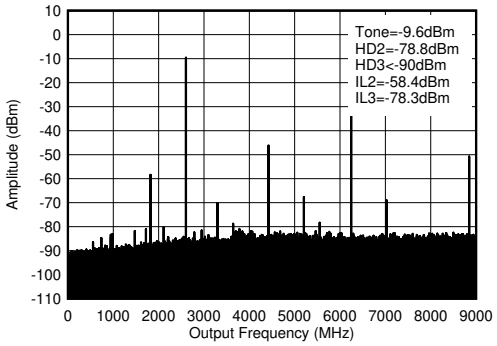
Inband = 2600MHz ± 600MHz, f_{DAC} = 12GSPS, not including F_S/3 and F_S/4, external clock mode, non-interleave mode

図 5-393. Two Tone Inband SFDR vs Digital Amplitude at 2.6 GHz



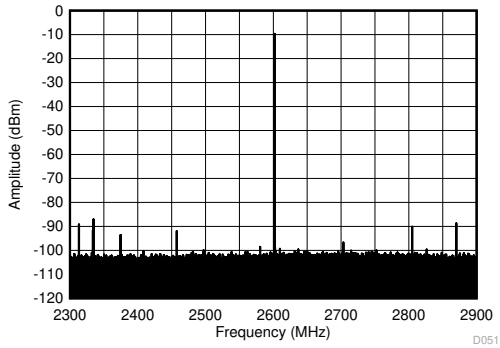
Inband = 2600MHz ± 600MHz, f_{DAC} = 12GSPS, external clock mode, non-interleave mode

図 5-394. Two Tone Inband Fixed Spurs vs Digital Amplitude at 2.6 GHz



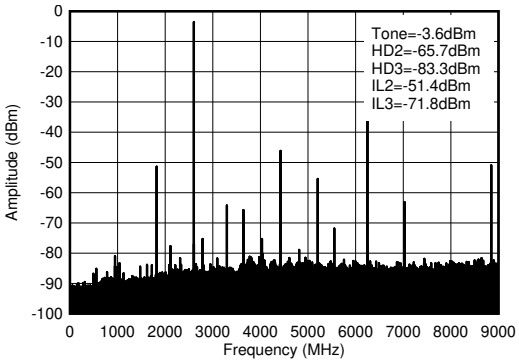
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-395. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



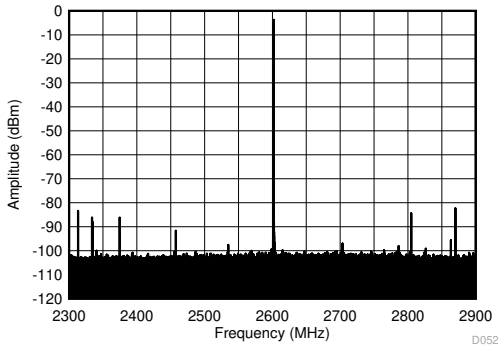
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 5-396. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-397. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



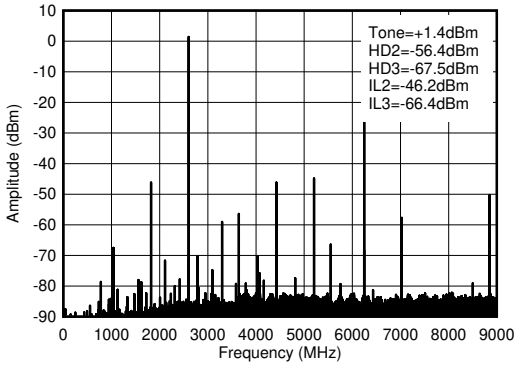
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 5-398. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

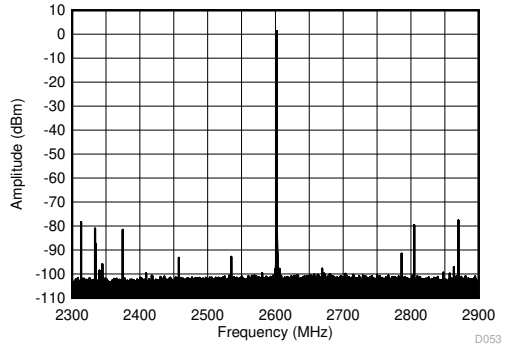
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



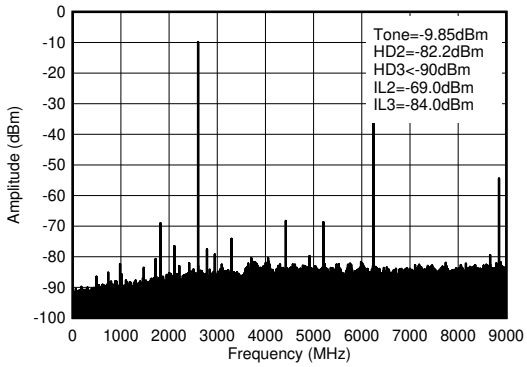
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-399. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



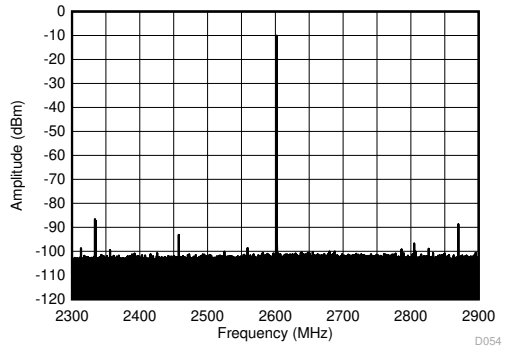
f_{DAC} = 8847.36MSPS, interleave mode, 2.6 GHz matching, includes PCB and cable losses

図 5-400. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-401. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



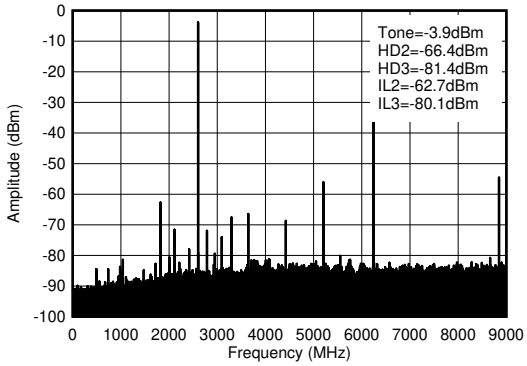
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 5-402. TX Single Tone (–12 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

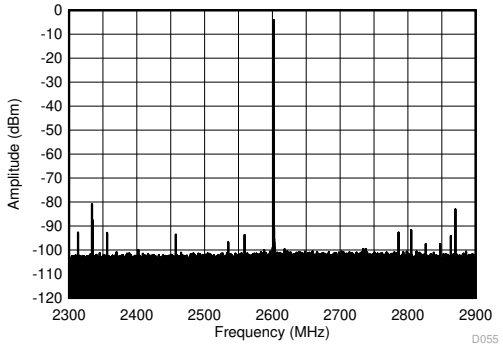
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



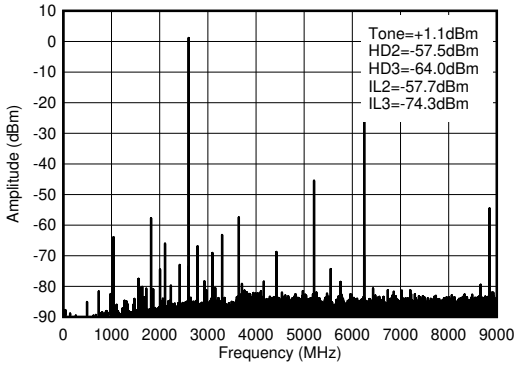
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-403. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



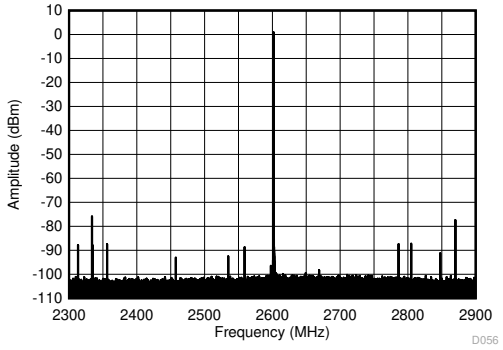
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 5-404. TX Single Tone (–6 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)



f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$ and is due to mixing with digital clocks.

図 5-405. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (0-f_{DAC})



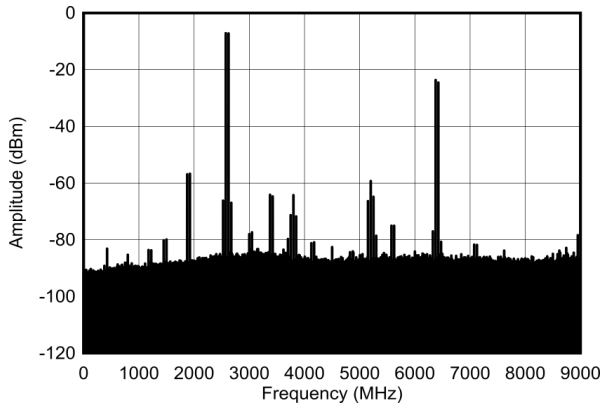
f_{DAC} = 8847.36MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses

図 5-406. TX Single Tone (–1 dBFS) Output Spectrum at 2.6 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

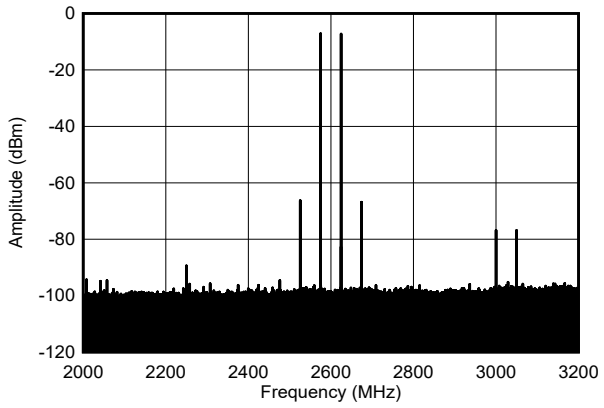
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



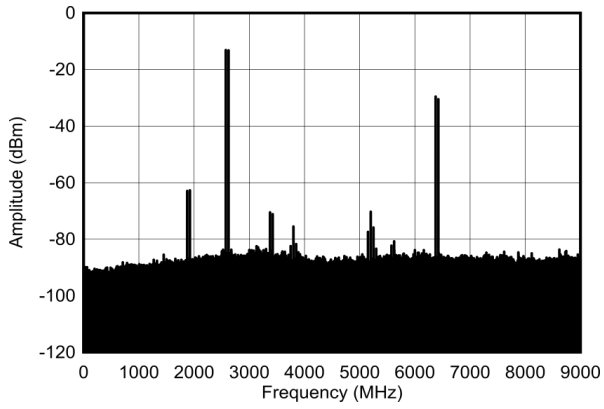
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-407. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each (0 - $_{DAC}$)



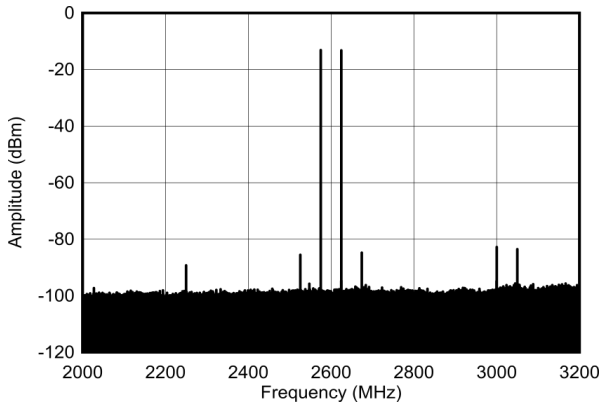
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-408. TX Dual Tone Output Spectrum at 2.6 GHz, -7dBFS each (±600 MHz)



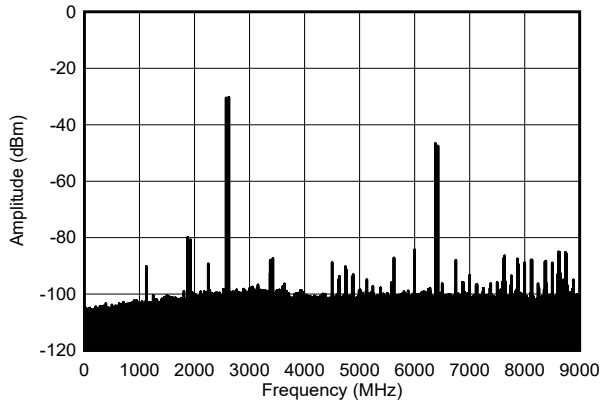
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-409. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each (0 - $_{DAC}$)



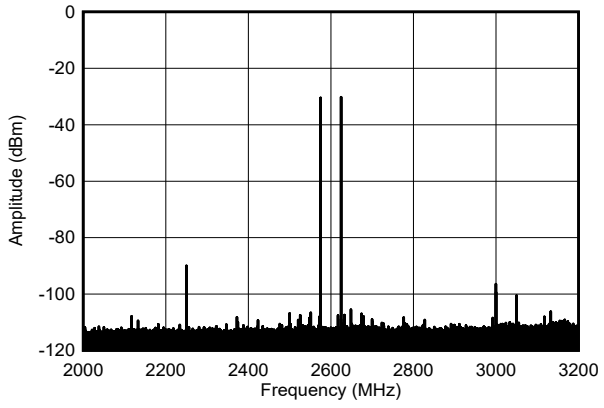
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-410. TX Dual Tone Output Spectrum at 2.6 GHz, -13dBFS each (±600 MHz)



f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-411. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each (0 - $_{DAC}$)



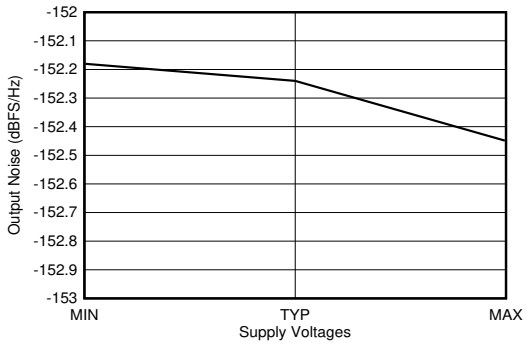
f_{DAC} = 9000MSPS, external clock mode, non-interleave mode

図 5-412. TX Dual Tone Output Spectrum at 2.6 GHz, -30dBFS each (±600 MHz)

Copyright © 2023 Texas Instruments Incorporated

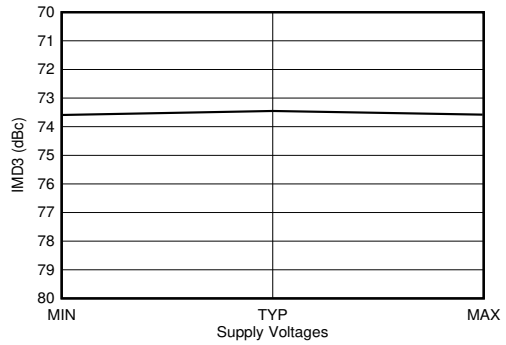
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



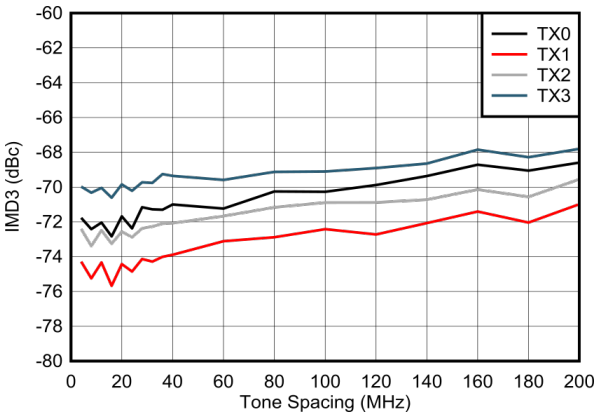
f_{DAC} = 11796.48MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –1 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

図 5-413. TX Output Noise vs Supply Voltage at 2.6 GHz



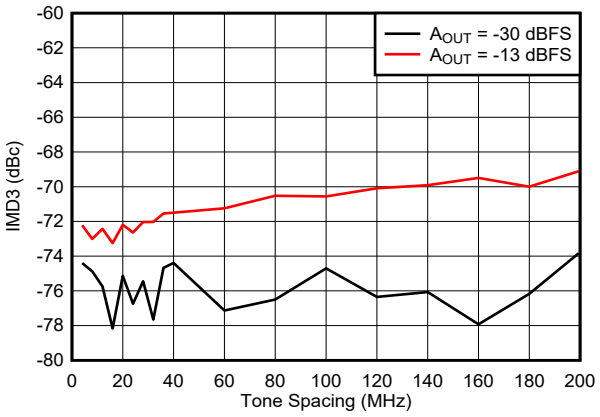
f_{DAC} = 11796.48MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = –13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

図 5-414. TX IMD3 vs Supply Voltage at 2.6 GHz



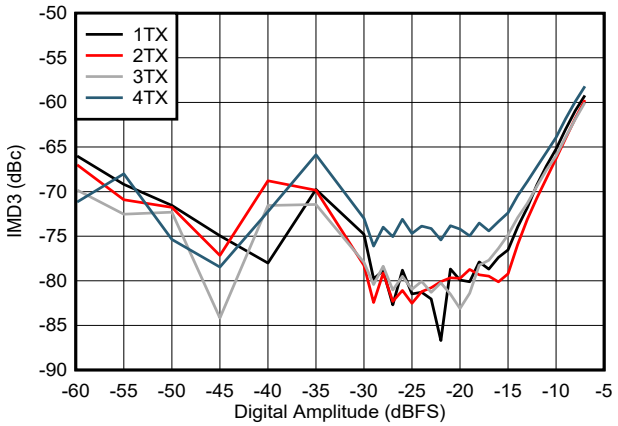
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

図 5-415. IMD3 vs Tone Spacing and Channel at 2.6 GHz



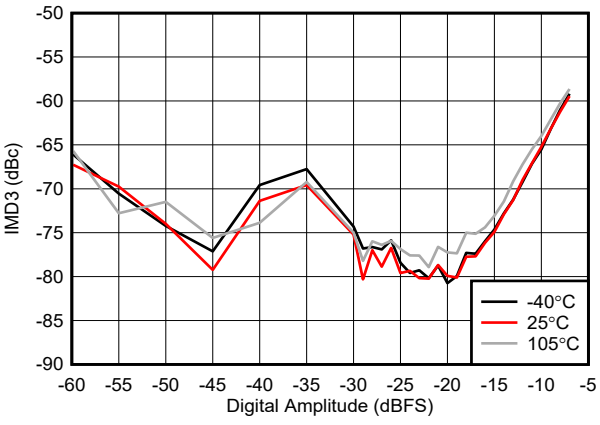
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

図 5-416. IMD3 vs Tone Spacing and Amplitude at 2.6 GHz



f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

図 5-417. IMD3 vs Digital Amplitude and Channel at 2.6 GHz

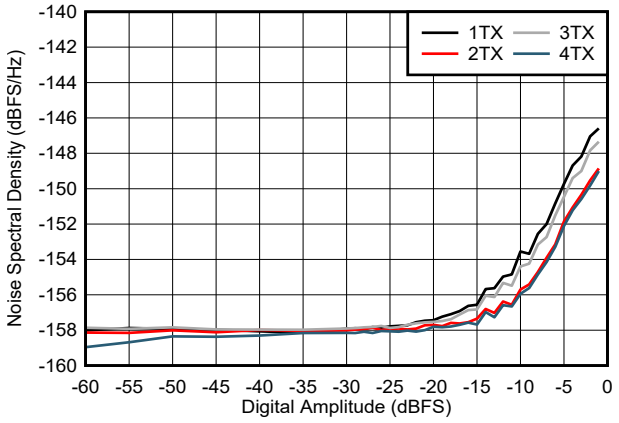


f_{DAC} = 9000MSPS, non-interleave mode, external clock mode

図 5-418. IMD3 vs Digital Amplitude and Temperature at 2.6 GHz

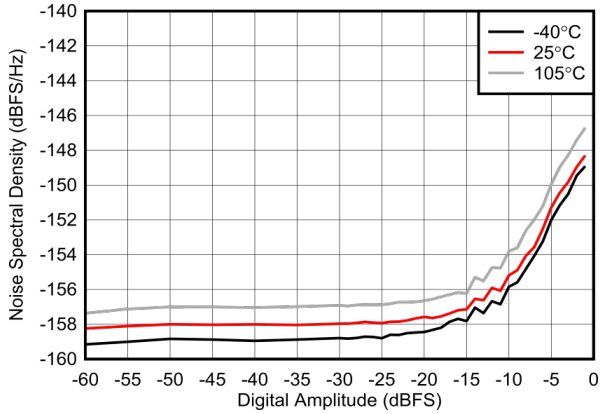
5.12.10 TX Typical Characteristics at 2.6GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



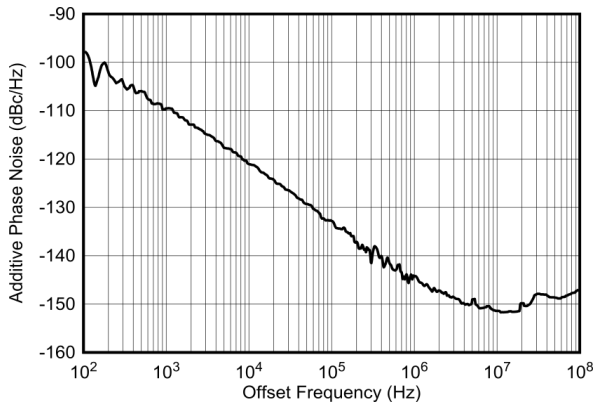
f_{DAC} = 9000MSPS, non-interleave mode, external clock mode, 50MHz offset

図 5-419. NSD vs Digital Amplitude and Channel at 2.6 GHz



f_{DAC} = 9000MSPS, non-interleave mode, external clock mode, 50MHz offset

図 5-420. NSD vs Digital Amplitude and Temperature at 2.6 GHz



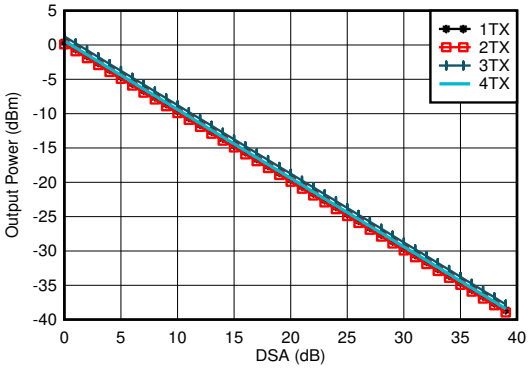
f_{DAC} = f_{CLK} = 9000MSPS, non-interleave mode

図 5-421. External Clock Additive Phase Noise at 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated

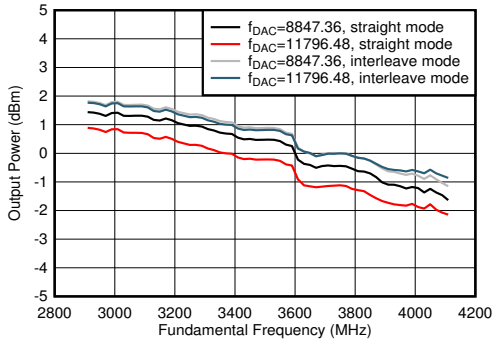
5.12.11 TX Typical Characteristics at 3.5GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



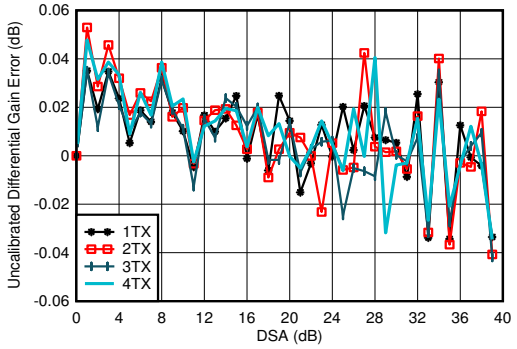
A_{out} = -0.5dFBS, 3.5 GHz Matching, included PCB and cable losses

図 5-422. TX Output Power vs DSA Setting at 3.5 GHz



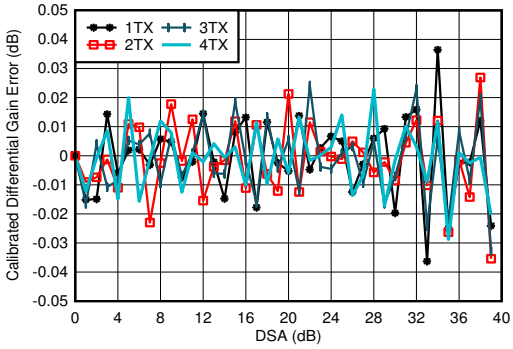
A_{out} = -0.5dFBS, 3.5 GHz Matching, included PCB and cable losses

図 5-423. TX Output Power vs Frequency



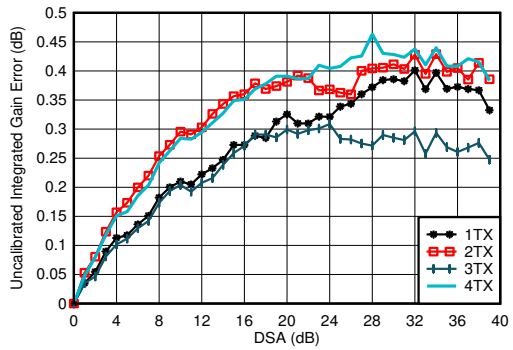
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-424. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



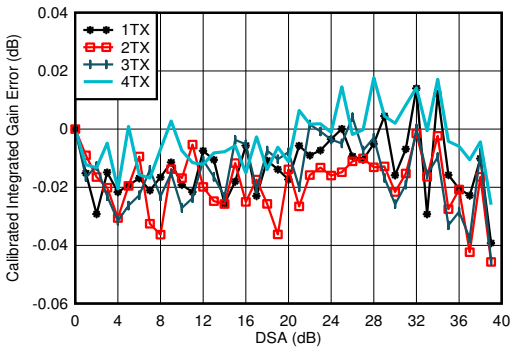
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-425. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-426. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz



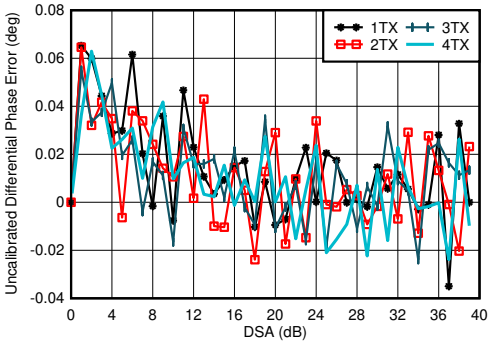
3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-427. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

Copyright © 2023 Texas Instruments Incorporated

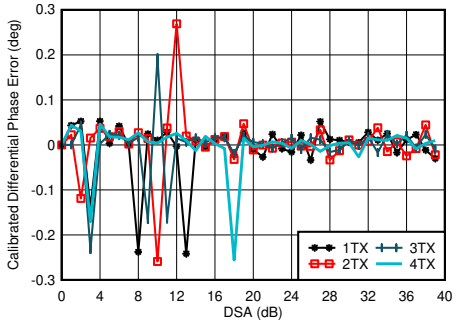
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



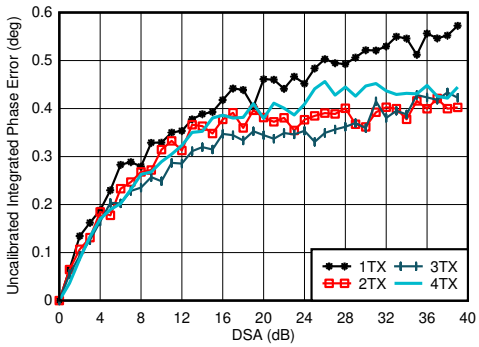
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-428. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



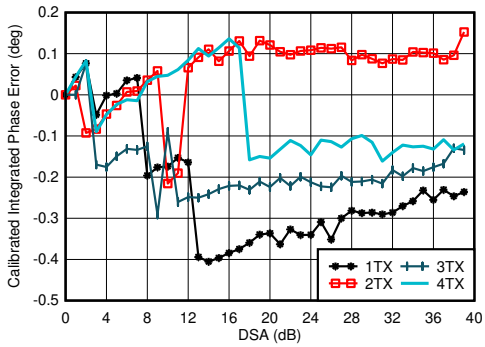
3.5 GHz Matching, included PCB and cable losses
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting). Phase DNL spike may occur at any DSA setting.

図 5-429. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



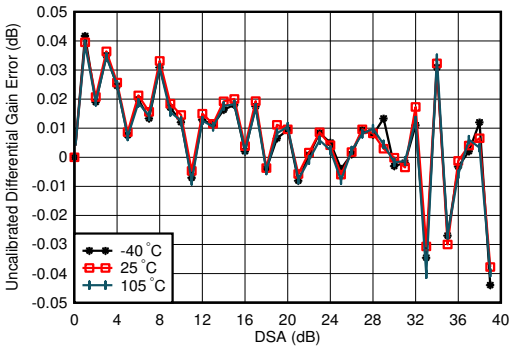
3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-430. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



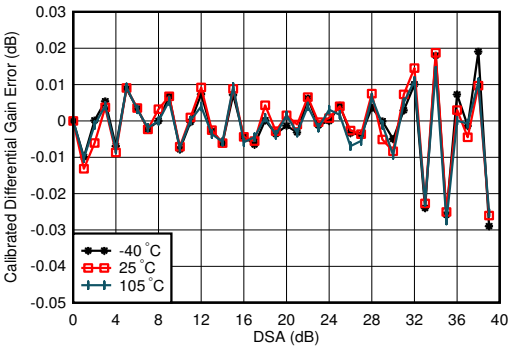
3.5 GHz Matching, included PCB and cable losses
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-431. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 1TX
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-432. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz



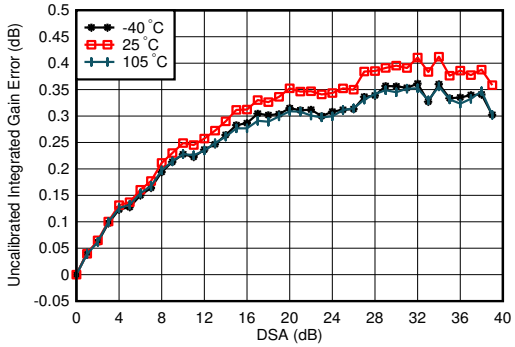
3.5 GHz Matching, 1TX, Calibrated at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-433. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

Copyright © 2023 Texas Instruments Incorporated

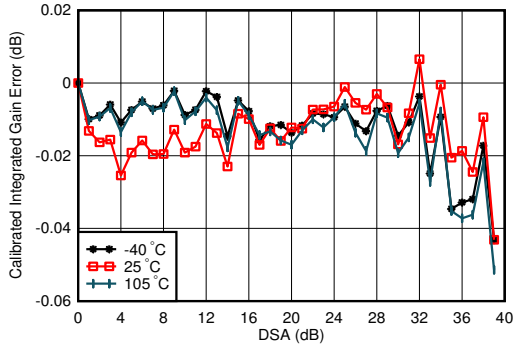
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



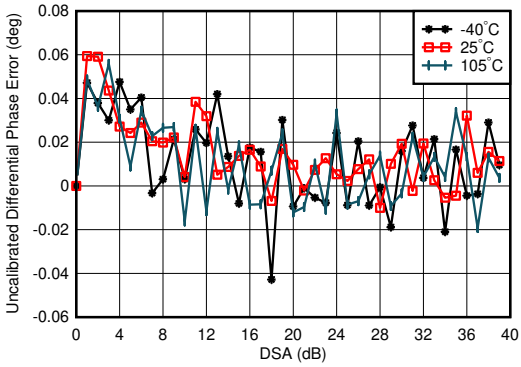
3.5 GHz Matching, 1TX
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-434. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



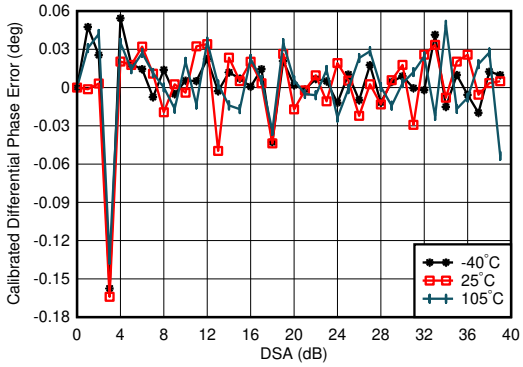
3.5 GHz Matching, 1TX, Calibrated at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-435. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-436. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



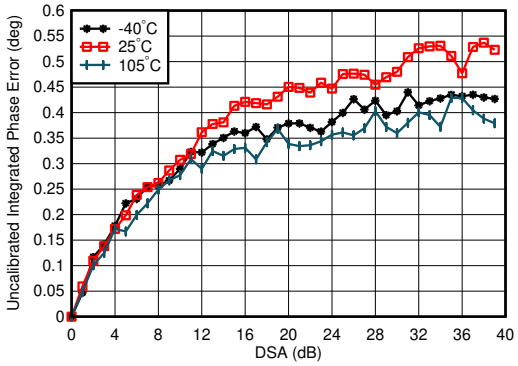
3.5 GHz Matching, 1TX, Calibrated at 25°C
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-437. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz

Copyright © 2023 Texas Instruments Incorporated

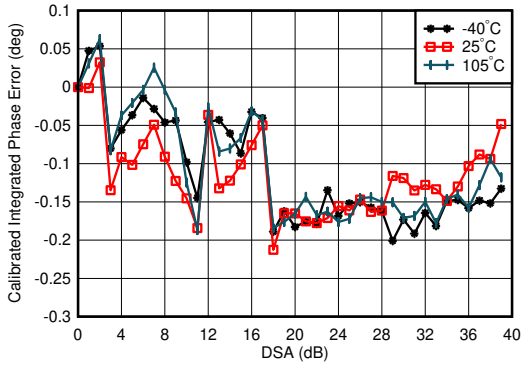
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



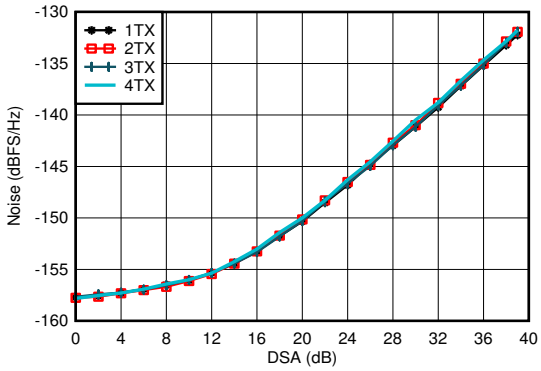
3.5 GHz Matching, 1TX
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting=0)

図 5-438. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



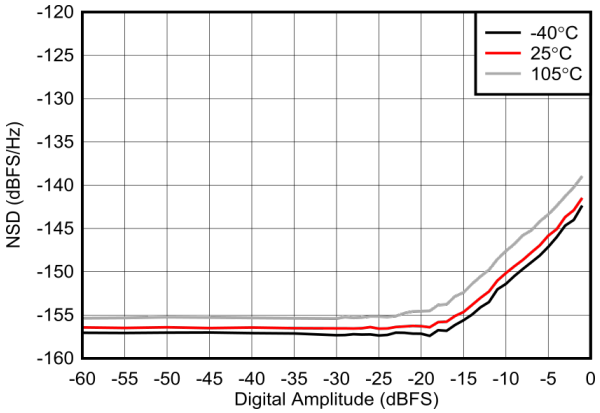
3.5 GHz Matching, 1TX, Calibrated at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-439. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



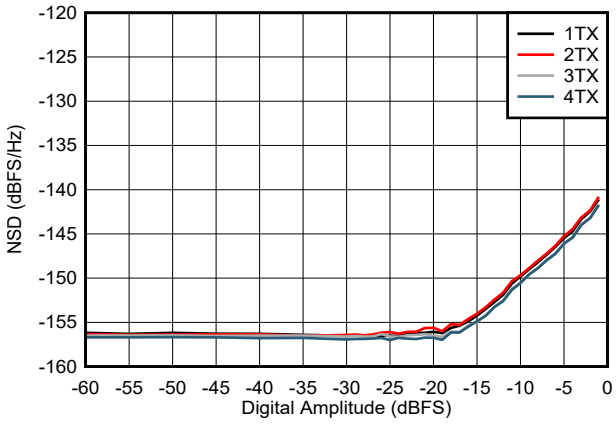
A. f_{DAC}=11796.48MSPS, interleave mode, matching at 3.5GHz, A_{out} = –13 dBFS.

図 5-440. TX NSD vs DSA Setting at 3.5 GHz



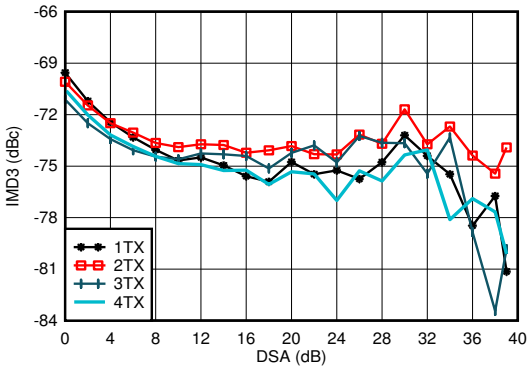
A. f_{DAC}=12MSPS, external clock mode, non-interleave mode

図 5-441. TX NSD vs Digital Amplitude and Temperature at 3.75 GHz



A. f_{DAC}=12MSPS, external clock mode, non-interleave mode

図 5-442. TX NSD vs Digital Amplitude and Channel at 3.75 GHz



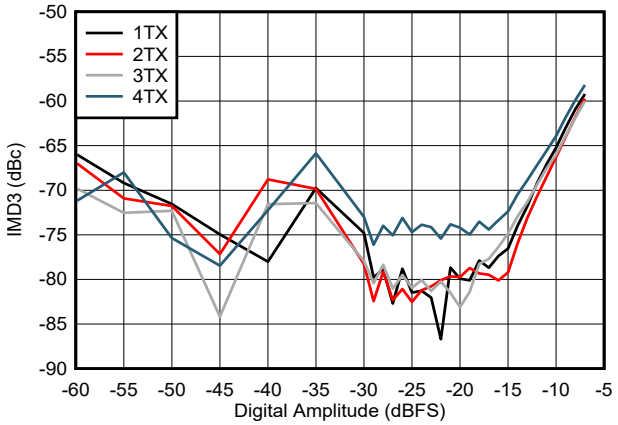
20-MHz tone spacing, 3.5 GHz Matching, –13 dBFS each tone, included PCB and cable losses

図 5-443. TX IMD3 vs DSA Setting at 3.5 GHz

Copyright © 2023 Texas Instruments Incorporated

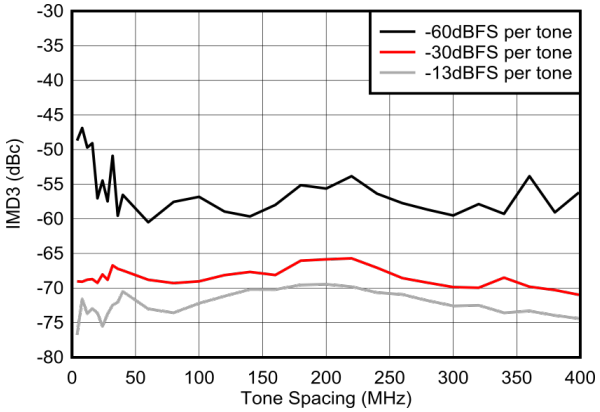
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



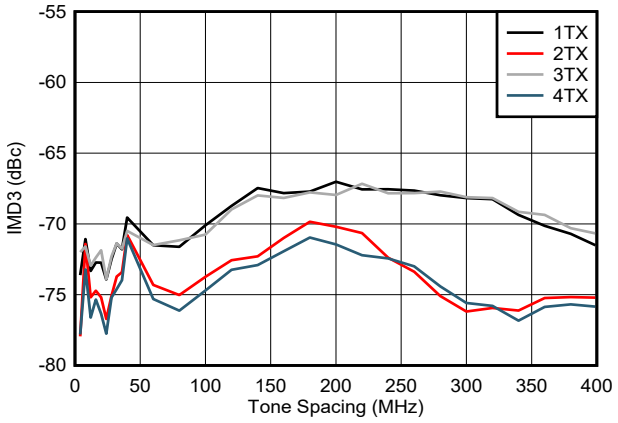
20-MHz tone spacing, 3.5 GHz Matching

図 5-444. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



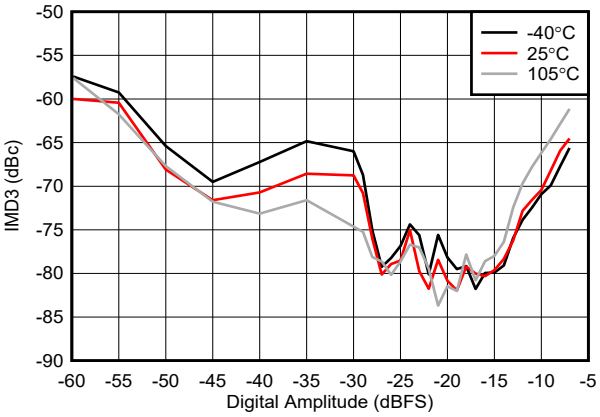
50-MHz tone spacing, external clock mode, non-interleave mode

図 5-445. TX IMD3 vs Tone Spacing and Amplitude at 3.75GHz



External clock mode, non-interleave mode

図 5-446. TX IMD3 vs Tone Spacing and Channel at 3.75GHz

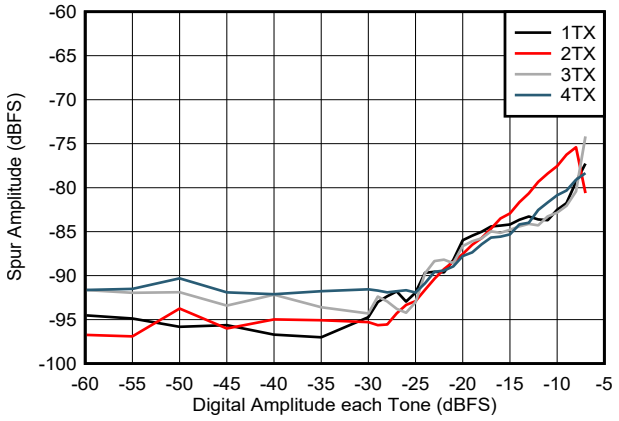


50-MHz tone spacing, external clock mode, non-interleave mode

図 5-447. TX IMD3 vs Digital Amplitude and Temperature at 3.75GHz

5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

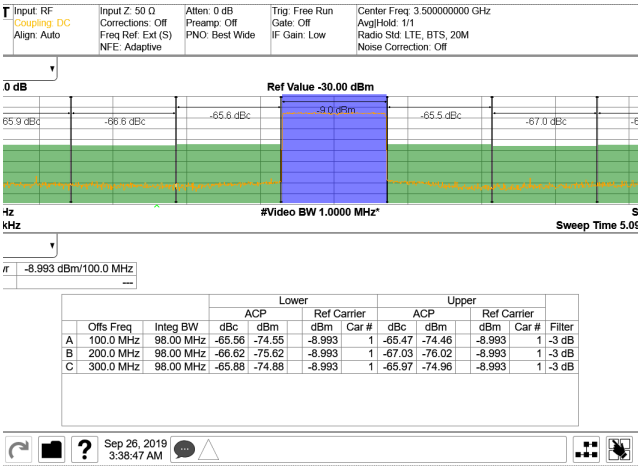


Inband = 3.75GHz ± 600MHz, f_{DAC} = 9GSPS, external clock mode, non-interleave mode.

図 5-448. Two Tone Inband SFDR vs Digital Amplitude at 3.75GHz

3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 5-449. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-450. TX 100-MHz NR Output Spectrum at 3.5 GHz (Band 42)

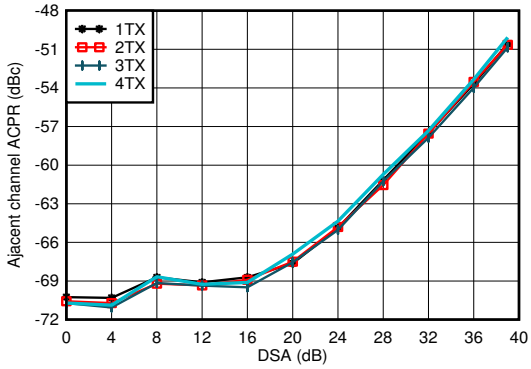
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-451. TX 2 carrier 100-MHz NR Output Spectrum at 3.45 GHz and 3.75 GHz

Copyright © 2023 Texas Instruments Incorporated

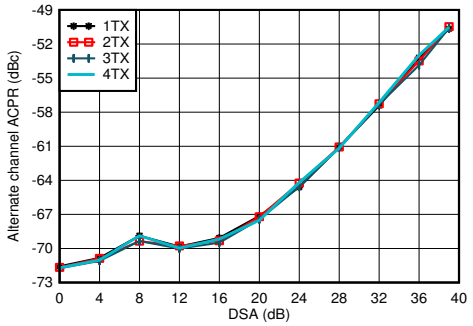
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



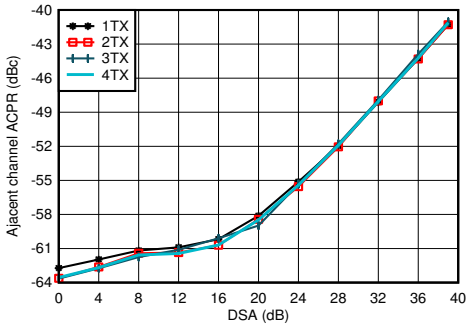
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 5-452. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz



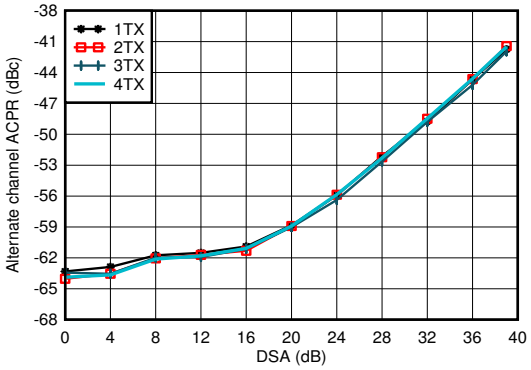
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 5-453. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz



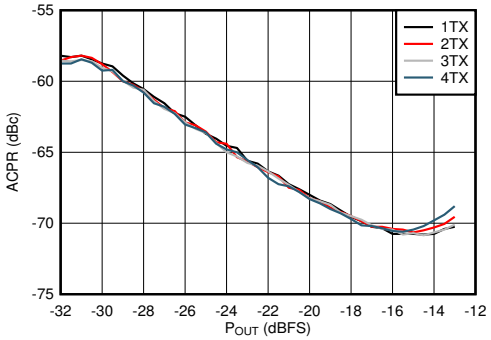
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-454. TX 100-MHz NR ACPR vs DSA Setting at 3.5 GHz



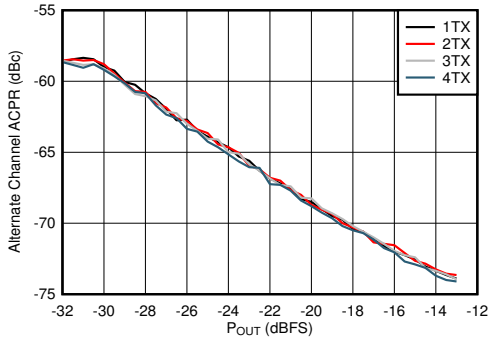
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-455. TX 100-MHz NR alt-ACPR vs DSA Setting at 3.5 GHz



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 5-456. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz

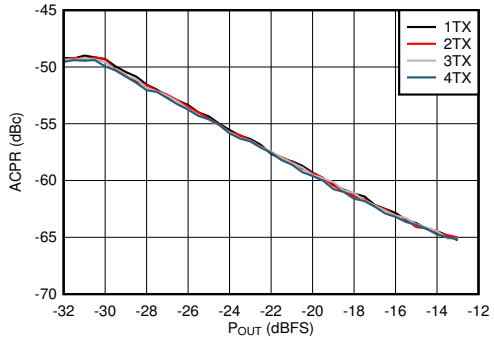


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

図 5-457. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz

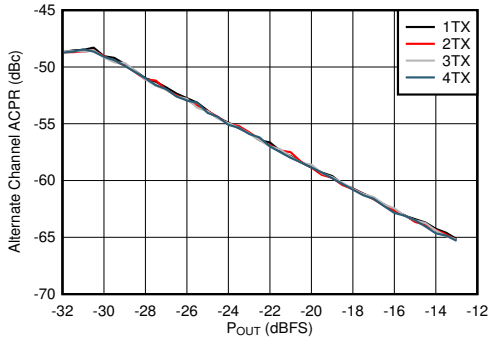
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



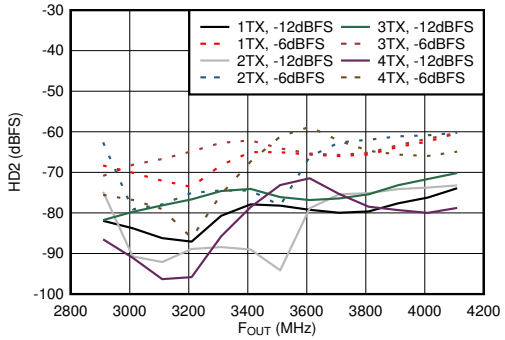
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-458. TX 100-MHz NR ACPR vs Digital Level at 3.5 GHz



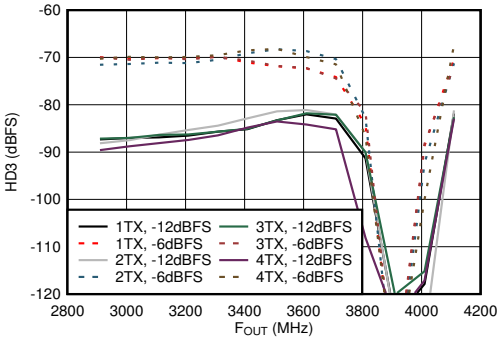
3.5 GHz Matching, single carrier 100-MHz BW NR TM1.1

図 5-459. TX 100-MHz NR alt-ACPR vs Digital Level at 3.5 GHz



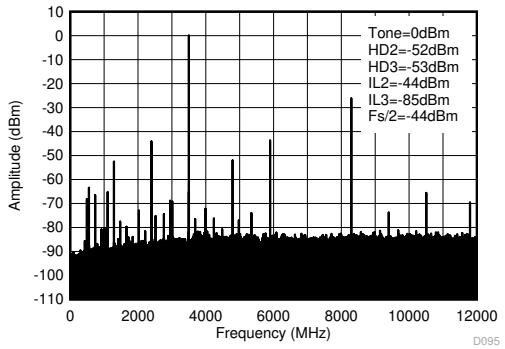
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-460. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



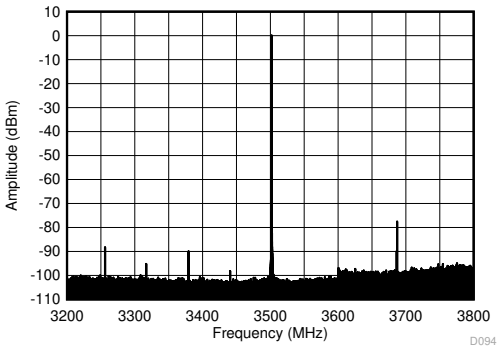
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

図 5-461. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-462. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})



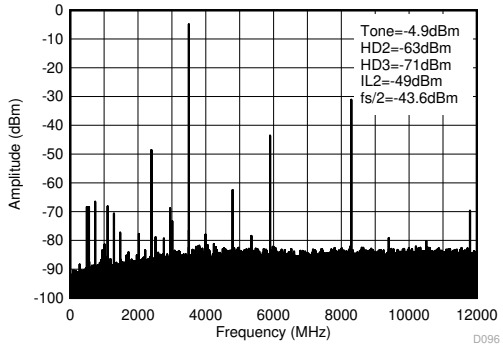
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-463. TX Single Tone (–1 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

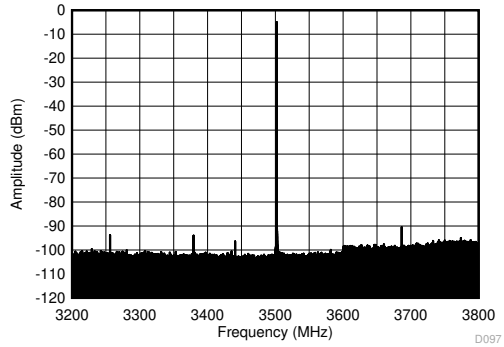
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



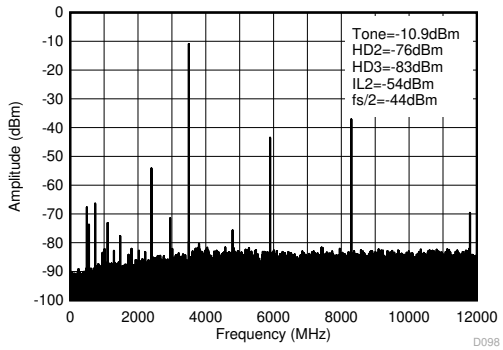
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-464. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



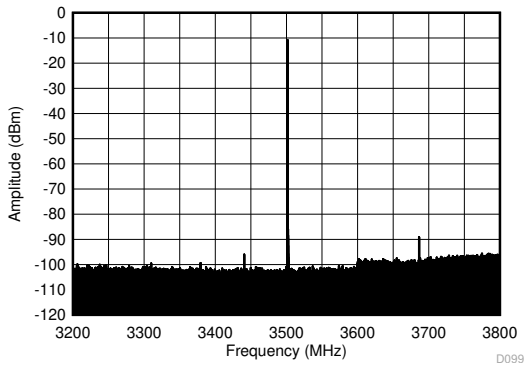
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-465. TX Single Tone (–6 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



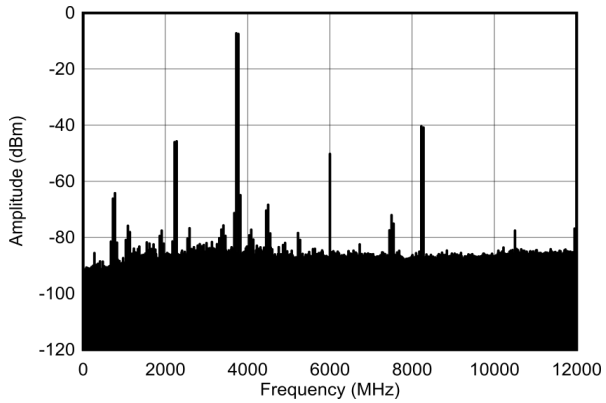
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-466. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (0-f_{DAC})



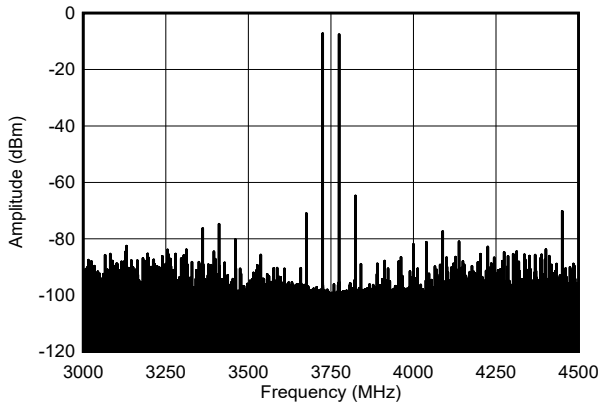
Matching at 3.5 GHz, f_{DAC} = 11.79648GSPS, interleave mode.

図 5-467. TX Single Tone (–12 dBFS) Output Spectrum at 3.5 GHz (±300 MHz)



Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-468. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each (0 - f_{DAC})



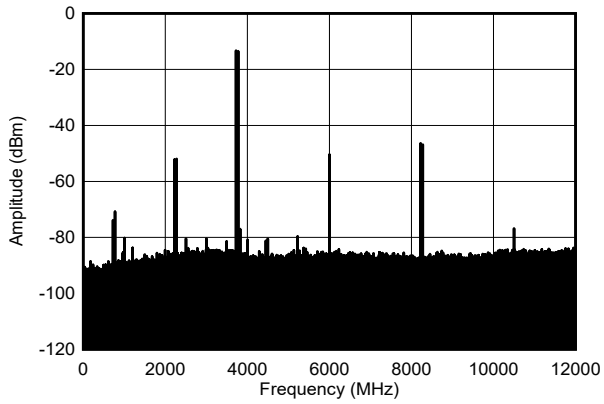
Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-469. TX Dual Tone Output Spectrum at 3.75 GHz, -7dBFS each (±600 MHz)

Copyright © 2023 Texas Instruments Incorporated

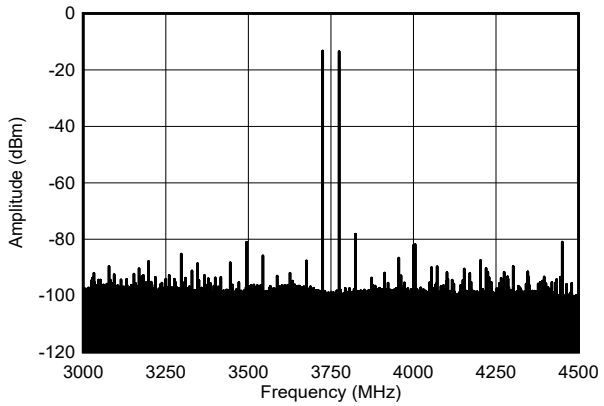
5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



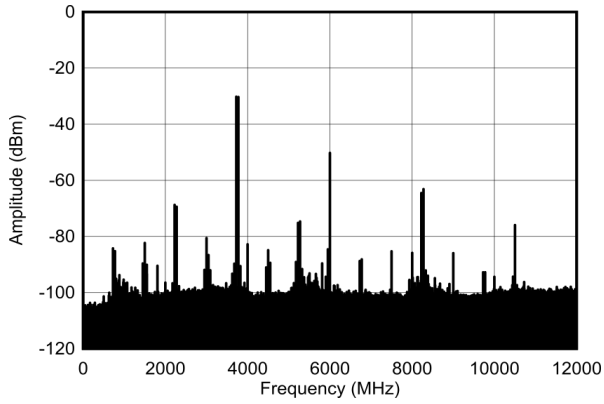
Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-470. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each (0 - f_{DAC})



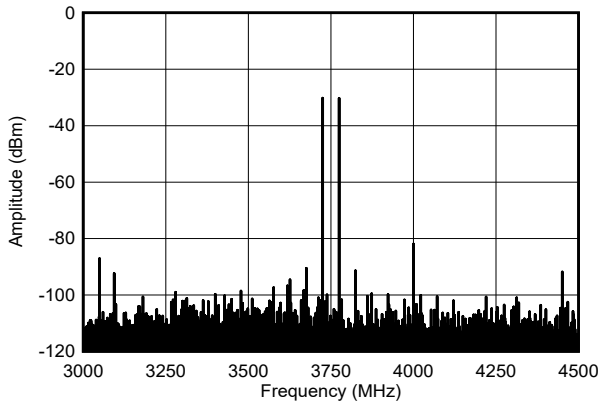
Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-471. TX Dual Tone Output Spectrum at 3.75 GHz, -13dBFS each (±600 MHz)



Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-472. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each (0 - f_{DAC})



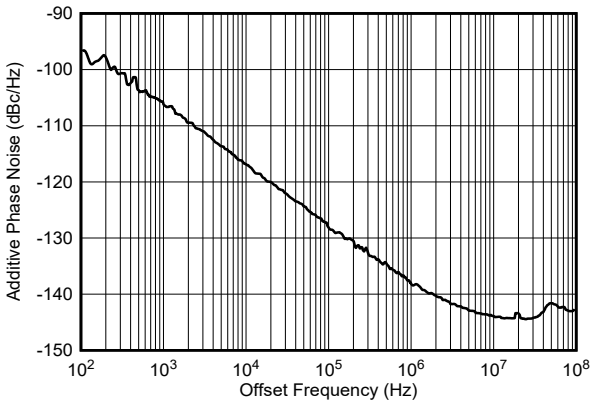
Matching at 3.5 GHz, 50MHz tone spacing, f_{DAC} = 12GSPS, non-interleave mode.

図 5-473. TX Dual Tone Output Spectrum at 3.75 GHz, -30dBFS each (±600 MHz)

Copyright © 2023 Texas Instruments Incorporated

5.12.11 TX Typical Characteristics at 3.5GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

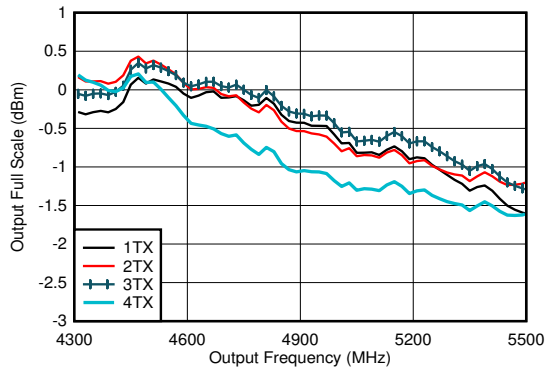


f_{DAC} = f_{CLK} = 12GSPS, non-interleave mode.

図 5-474. External Clock Additive Phase Noise at 3.7GHz

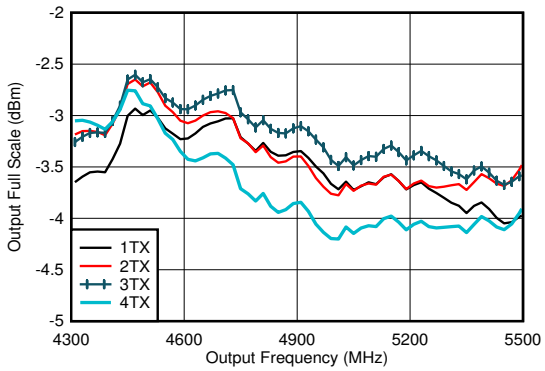
5.12.12 TX Typical Characteristics at 4.9GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



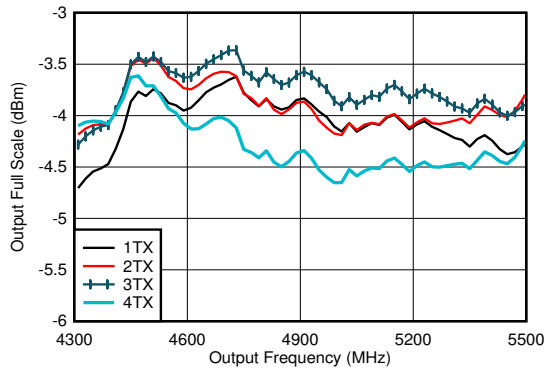
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9 GHz matching

図 5-475. TX Full Scale vs RF Frequency and Channel at 11796.48MSPS



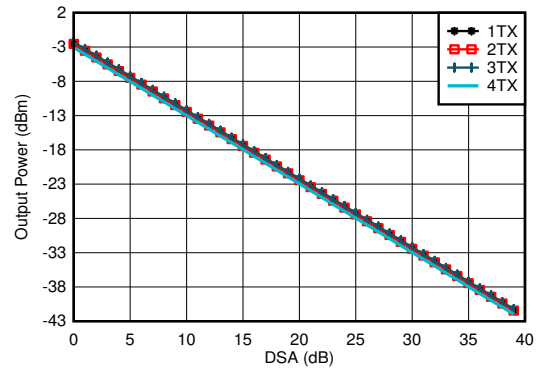
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9 GHz matching

図 5-476. TX Full Scale vs RF Frequency and Channel at 5898.24MSPS, Mix Mode, 2nd Nyquist Zone



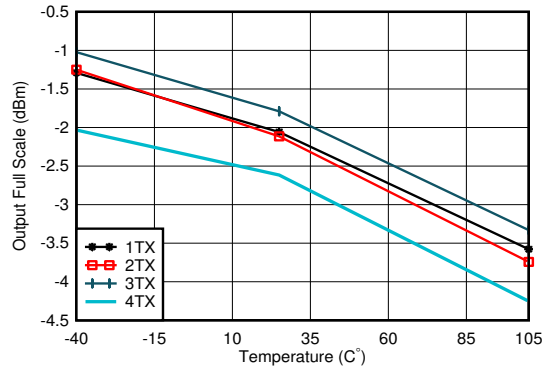
Excluding PCB and cable losses, A_{out} = -0.5dBFS, DSA = 0, 4.9 GHz matching

図 5-477. TX Full Scale vs RF Frequency and Channel at 8847.36MSPS, Mix Mode, 2nd Nyquist Zone



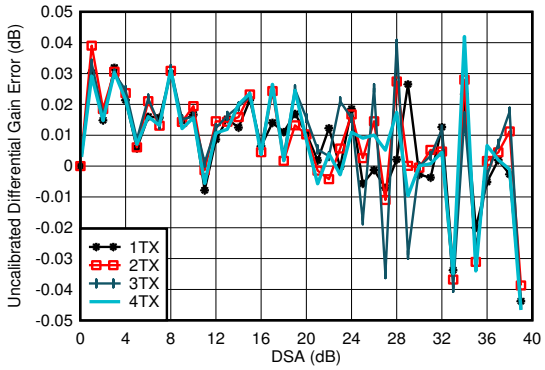
f_{DAC} = 11796.48 MSPS, A_{out} = -0.5dBFS, matching 4.9 GHz

図 5-478. TX Output Power vs DSA Setting and Channel at 4.9 GHz



A_{out} = -0.5dBFS, 4.9 GHz Matching, PCB and cable losses included.

図 5-479. TX Full Scale Output Power vs Temperature and Channel at 4.9 GHz



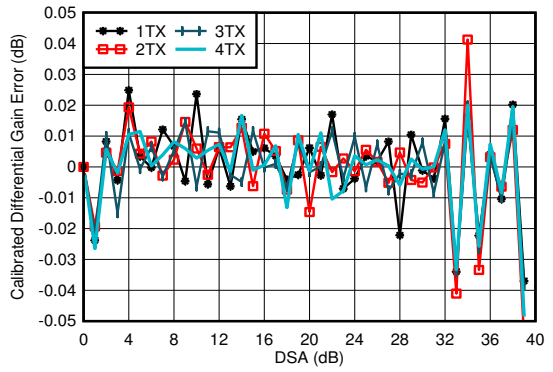
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-480. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

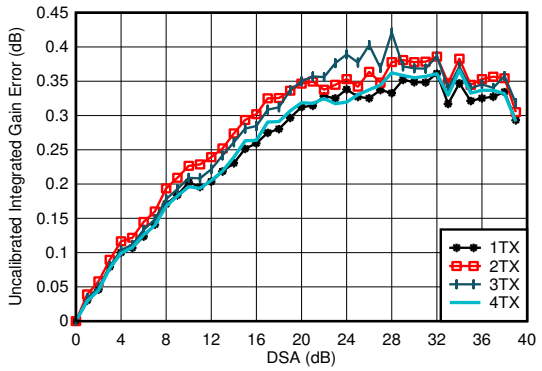
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



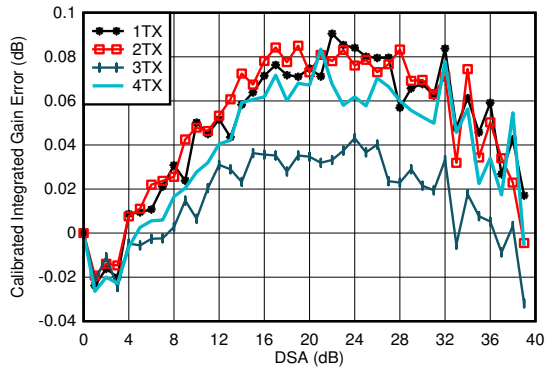
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-481. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



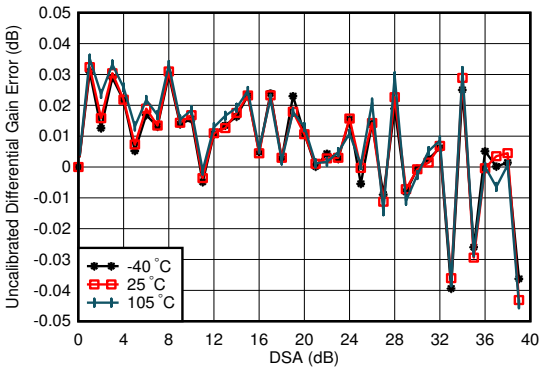
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-482. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-483. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



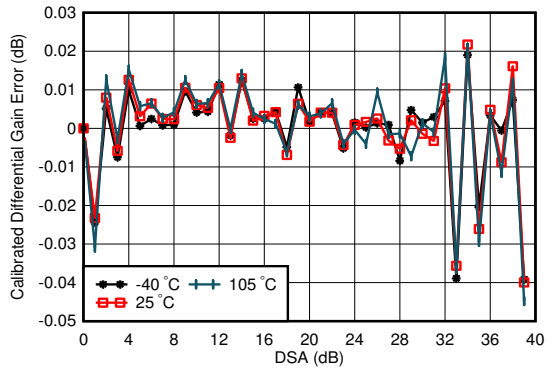
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

図 5-484. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.12 TX Typical Characteristics at 4.9GHz (continued)

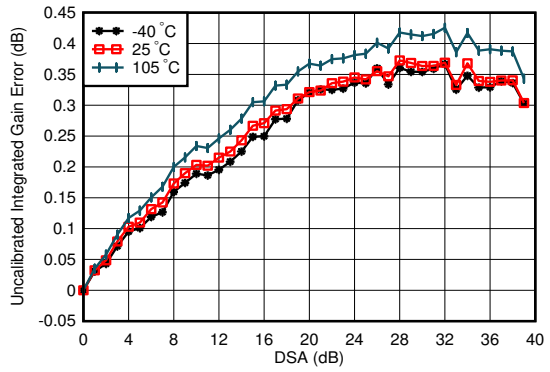
Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Differential Gain Error = P_{OUT}(DSA Setting – 1) – P_{OUT}(DSA Setting) + 1

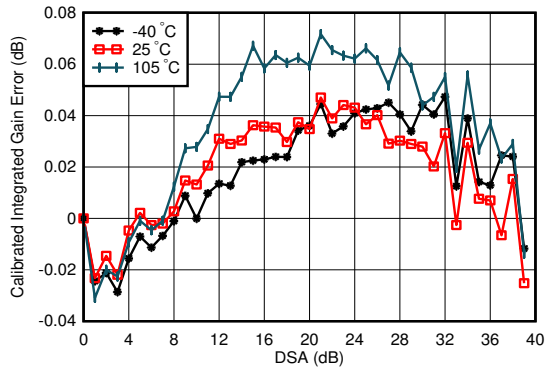
図 5-485. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

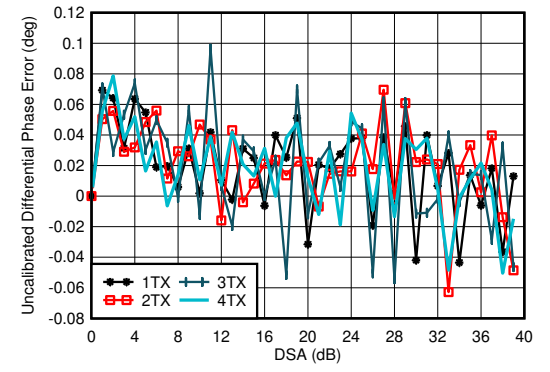
図 5-486. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error = P_{OUT}(DSA Setting) – P_{OUT}(DSA Setting = 0) + (DSA Setting)

図 5-487. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

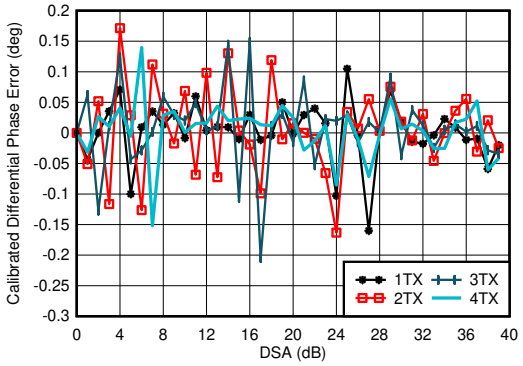
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-488. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.

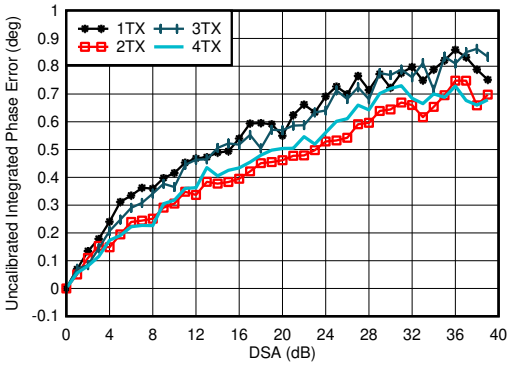


f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

Phase DNL spike may occur at any DSA setting.

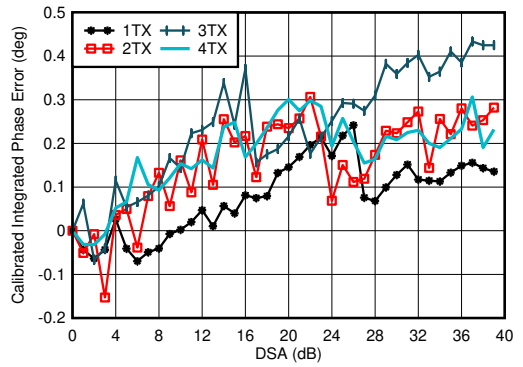
図 5-489. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

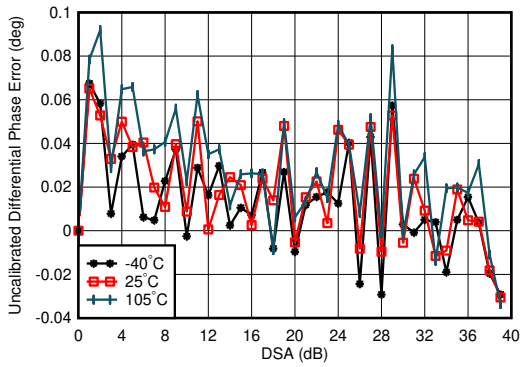
図 5-490. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-491. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



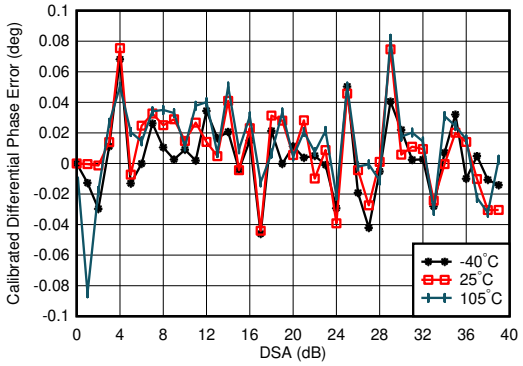
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-492. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

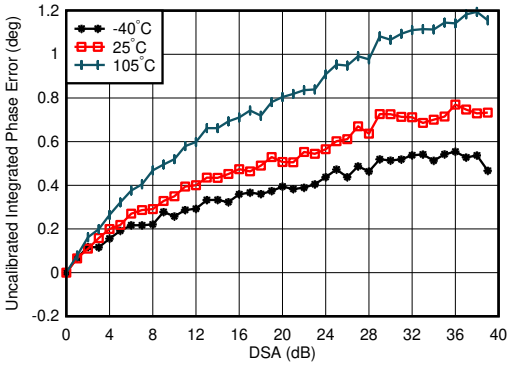
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



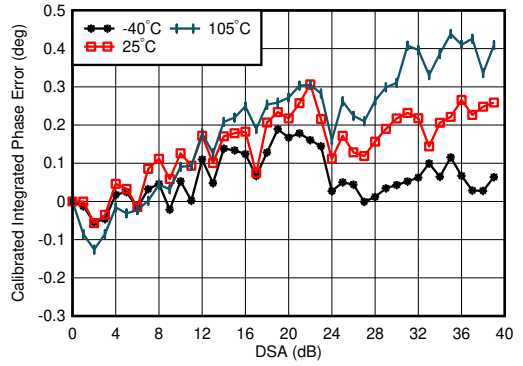
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = $Phase_{OUT}$(DSA Setting – 1) – $Phase_{OUT}$(DSA Setting)

図 5-493. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



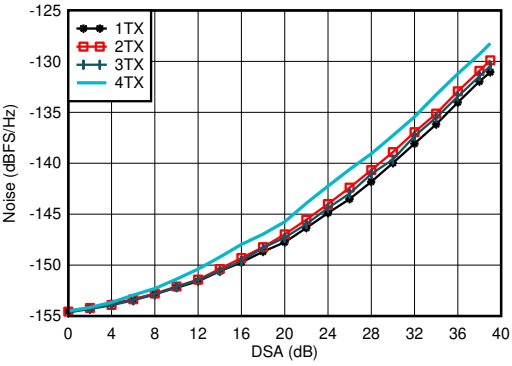
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-494. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-495. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



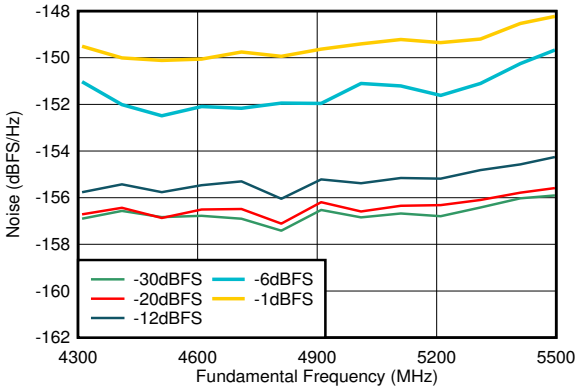
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, P_{OUT} = –13 dBFS

図 5-496. TX Output Noise vs Channel and Attenuation at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

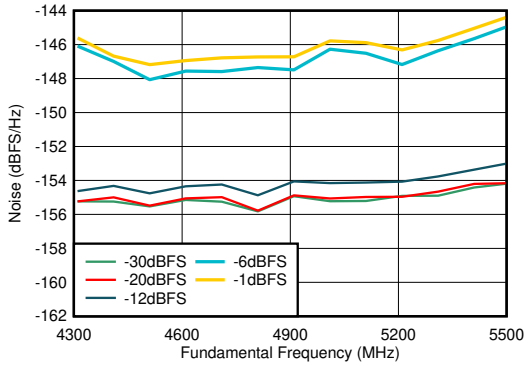
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



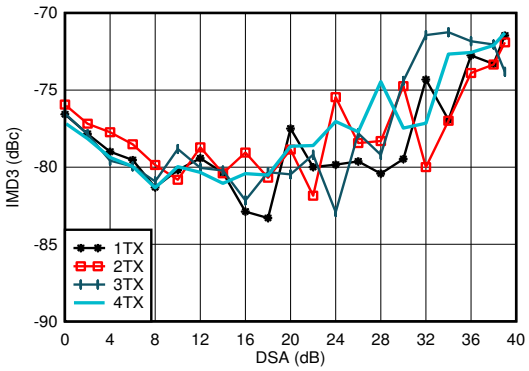
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9GHz, A_{out} = –13 dBFS.

図 5-497. TX NSD vs Output Frequency and Digital Amplitude at 4.9 GHz (DSA=0dB)



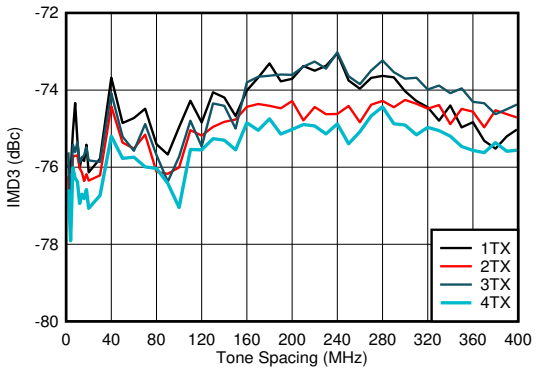
f_{DAC}=11796.48MSPS, interleave mode, matching at 4.9GHz, A_{out} = –13 dBFS.

図 5-498. TX NSD vs Output Frequency and Digital Amplitude at 4.9GHz (DSA=6dB)



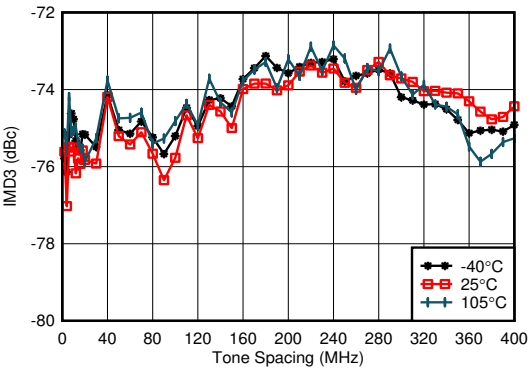
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, -13 dBFS each tone

図 5-499. TX IMD3 vs DSA Setting at 4.9 GHz



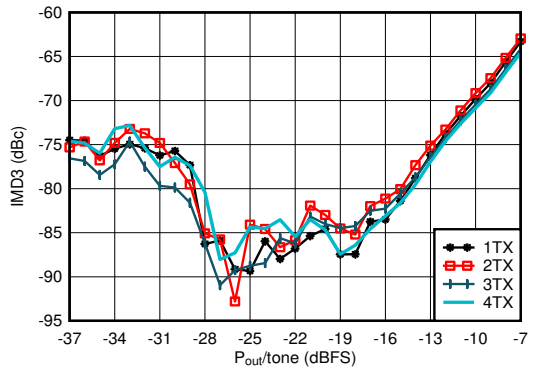
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone

図 5-500. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, –13 dBFS each tone, worst channel

図 5-501. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz



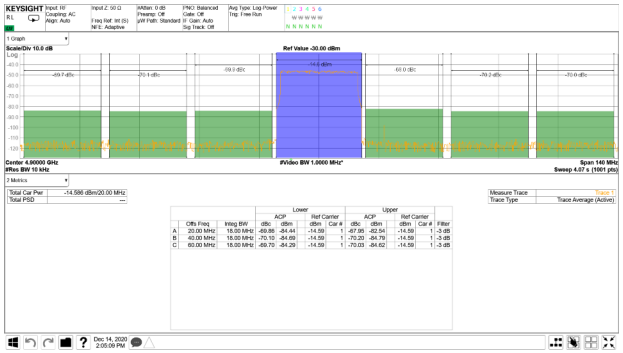
f_{DAC} = 11796.48MSPS, interleaved mode, matching at 4.9 GHz, f_{CENTER} = 4.9GHz, $f_{SPACING}$ = 20 MHz

図 5-502. TX IMD3 vs Digital Level at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

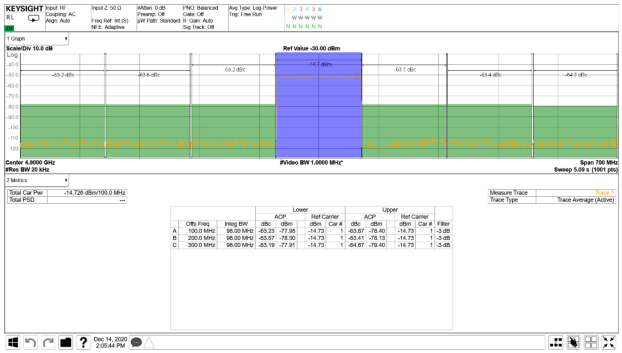
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



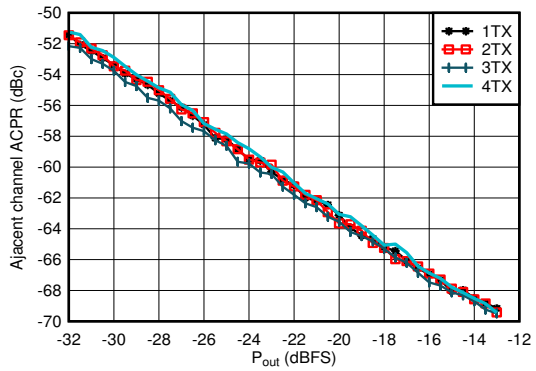
TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-503. TX 20-MHz LTE Output Spectrum at 4.9 GHz



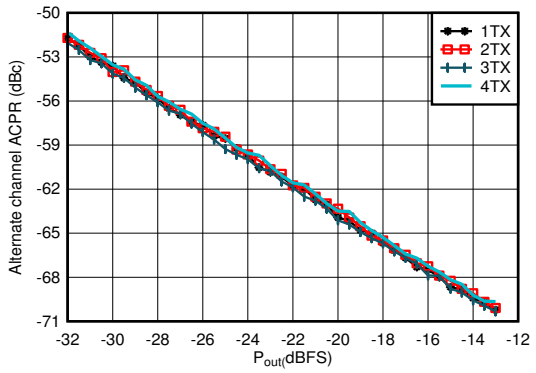
TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-504. TX 100-MHz NR Output Spectrum at 4.9 GHz



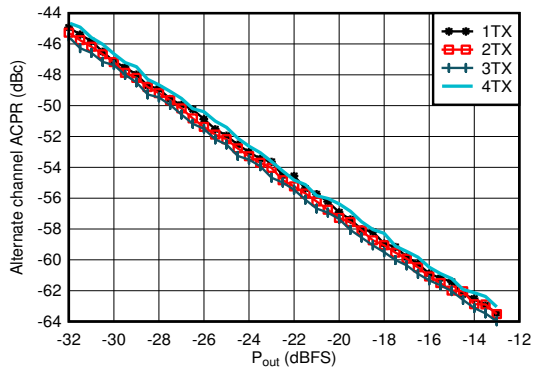
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-505. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



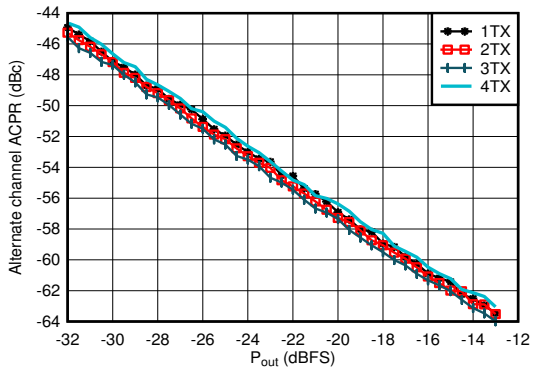
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-506. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-507. TX 100-MHz NR ACPR vs Digital Level at 4.9 GHz



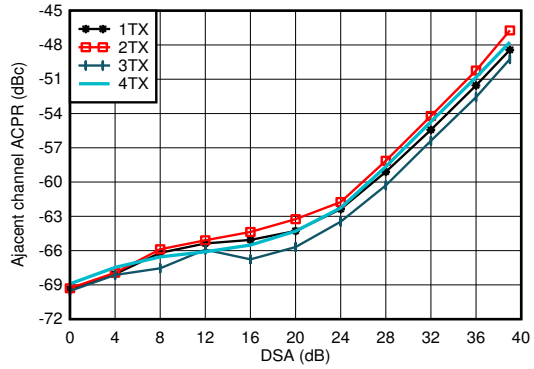
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-508. TX 100-MHz NR alt-ACPR vs Digital Level at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

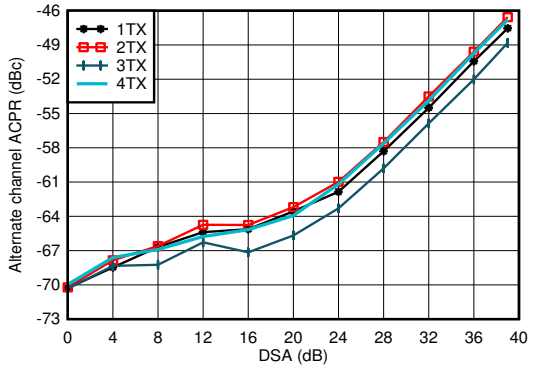
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



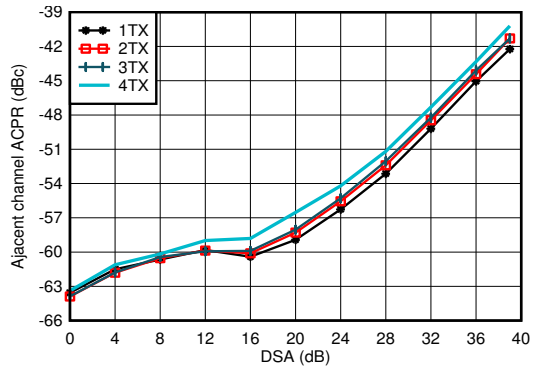
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-509. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz



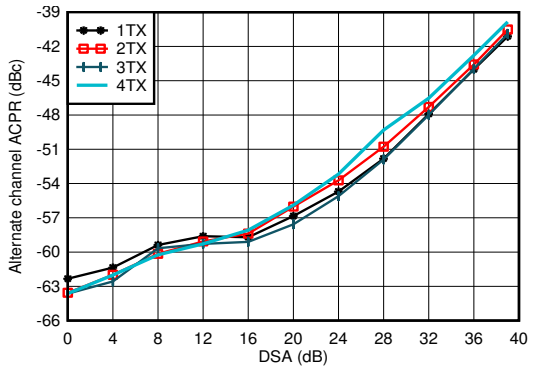
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

図 5-510. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz



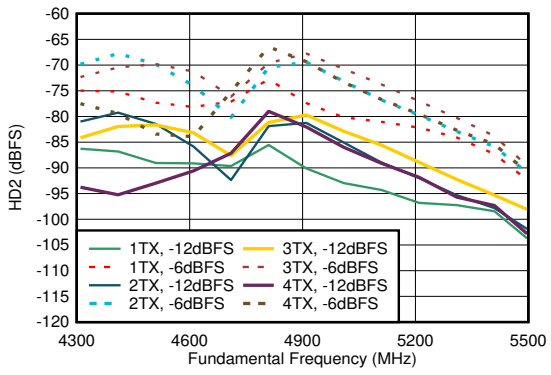
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-511. TX 100-MHz NR ACPR vs DSA at 4.9 GHz



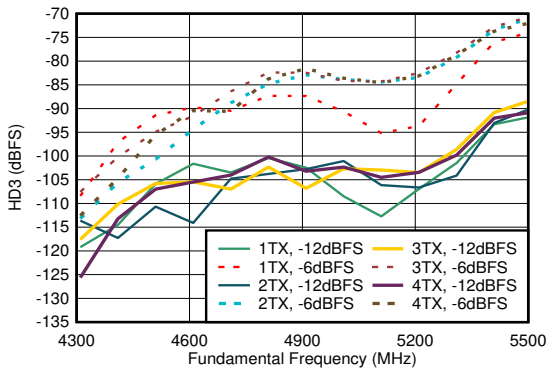
Matching at 4.9 GHz, single carrier 100-MHz BW TM1.1 NR

図 5-512. TX 100-MHz NR alt-ACPR vs DSA at 4.9 GHz



Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-513. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



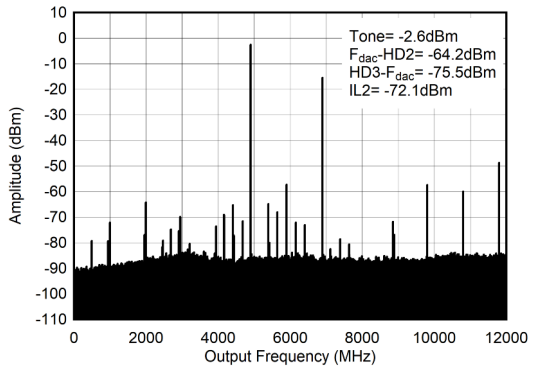
Matching at 4.9 GHz, f_{DAC} = 11.79648GSPS, interleave mode, normalized to output power at harmonic frequency

図 5-514. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz

Copyright © 2023 Texas Instruments Incorporated

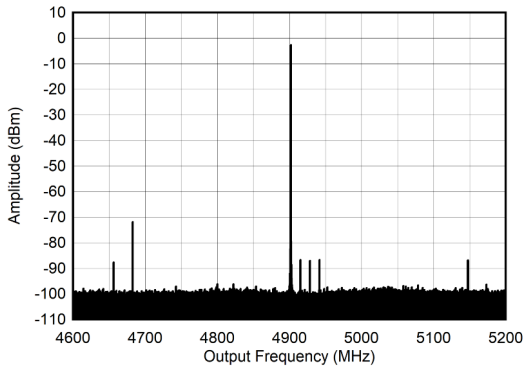
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



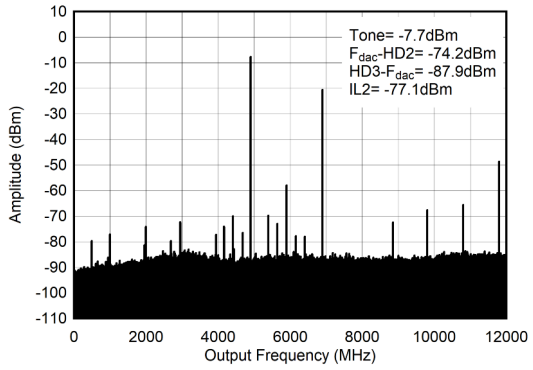
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-515. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



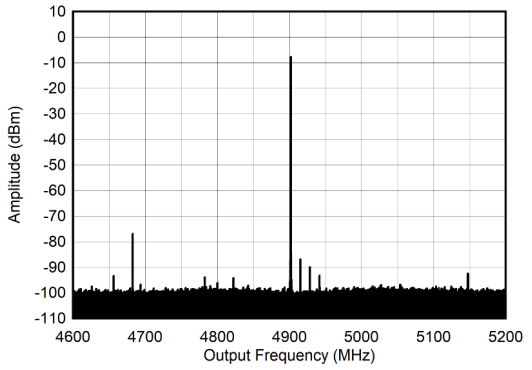
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 5-516. TX Single Tone (–1 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)



f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-517. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



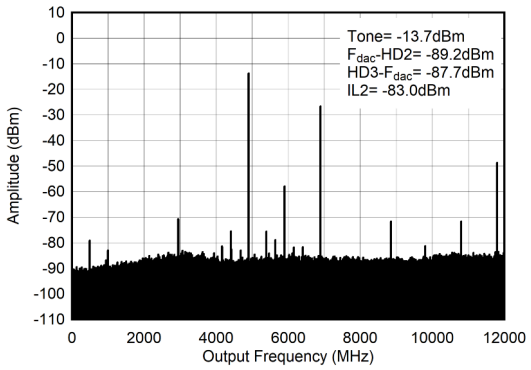
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 5-518. TX Single Tone (–6 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)

Copyright © 2023 Texas Instruments Incorporated

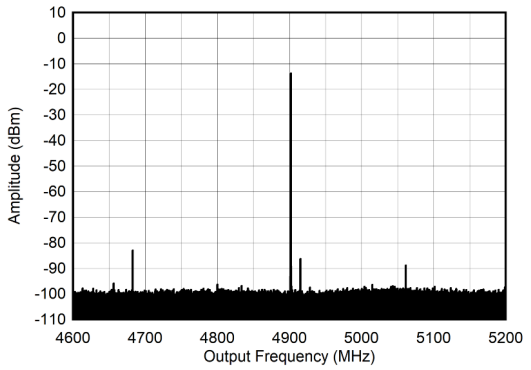
5.12.12 TX Typical Characteristics at 4.9GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 491.52MSPS, f_{DAC} = 11796.48MSPS, interleave mode, A_{OUT} = –1 dBFS, 1st Nyquist zone output, Internal PLL, f_{REF} = 491.52MSPS, 24x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated.



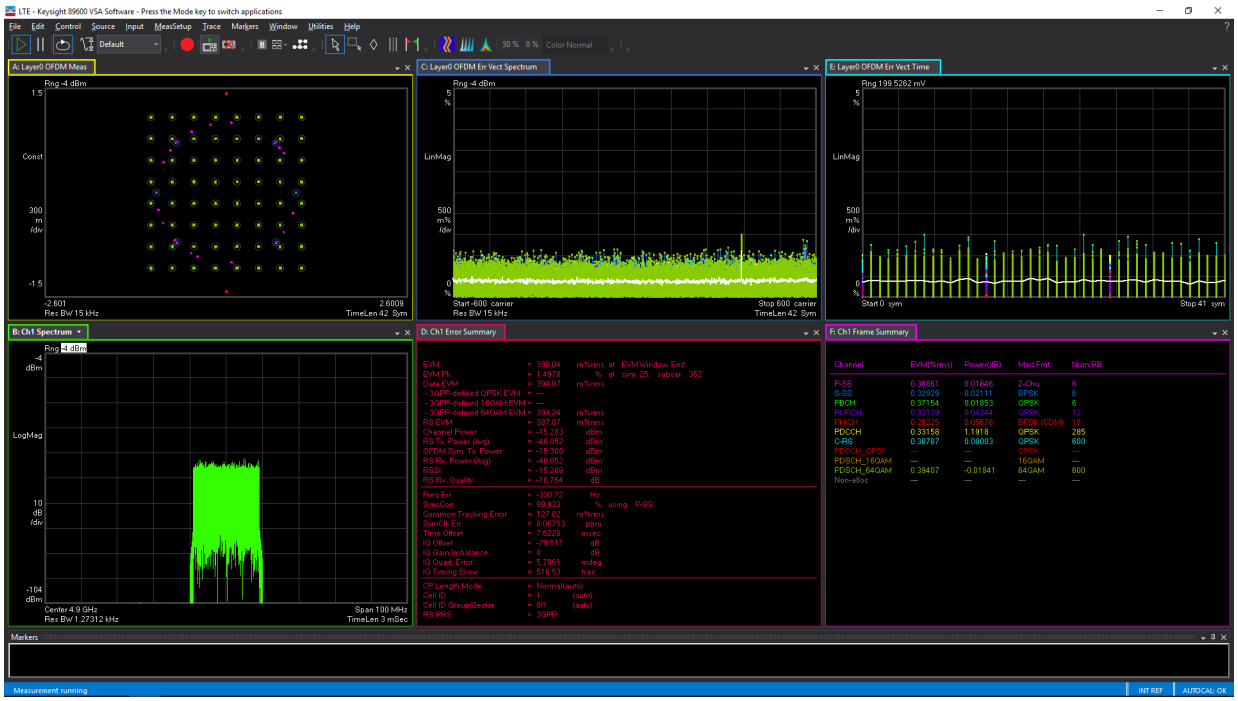
f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. ILn = $f_S/n \pm f_{OUT}$.

図 5-519. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (0-f_{DAC})



f_{DAC} = 11796.48MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses

図 5-520. TX Single Tone (–12 dBFS) Output Spectrum at 4.9 GHz (±300 MHz)

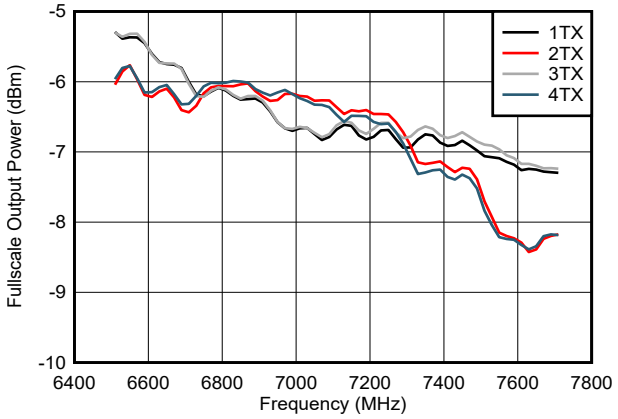


TM1.1, P_{OUT_RMS} = –13 dBFS

図 5-521. TX 20-MHz LTE Error Vector Magnitude at 4.9 GHz

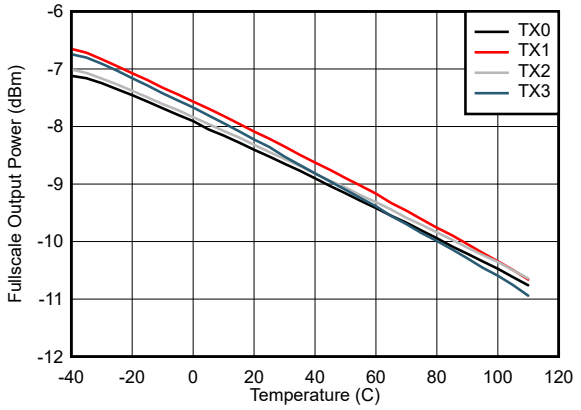
5.12.13 TX Typical Characteristics at 7.1GHz

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



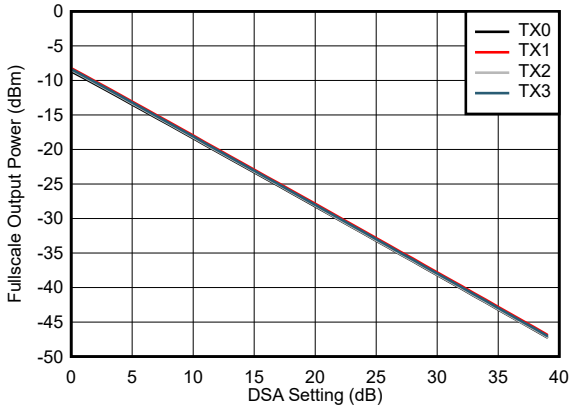
Excluding PCB and cable losses

図 5-522. TX Full Scale vs RF Frequency and Channel



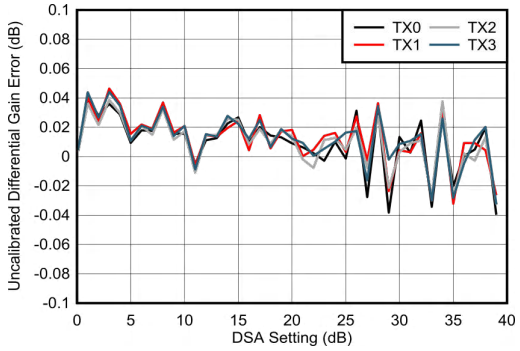
Excluding PCB and cable losses

図 5-523. TX Full Scale vs Temperature and Channel at 7.1GHz



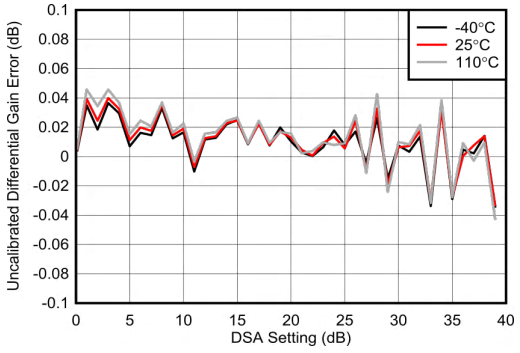
Excluding PCB and cable losses

図 5-524. TX Full Scale vs DSA Setting and Channel at 7.1 GHz



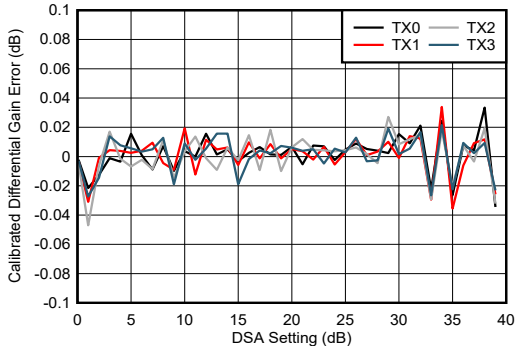
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 5-525. Uncalibrated Differential Gain Error vs Channel at 7.1 GHz



Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 5-526. Uncalibrated Differential Gain Error vs Temperature at 7.1 GHz



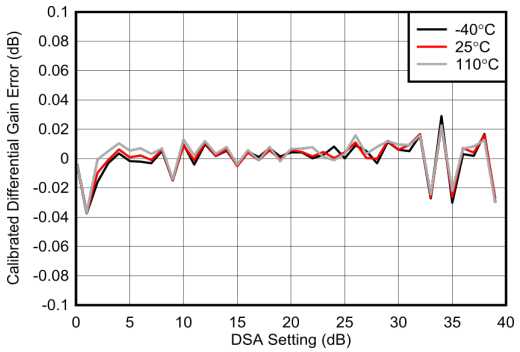
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 5-527. Calibrated Differential Gain Error vs Channel at 7.1 GHz

Copyright © 2023 Texas Instruments Incorporated

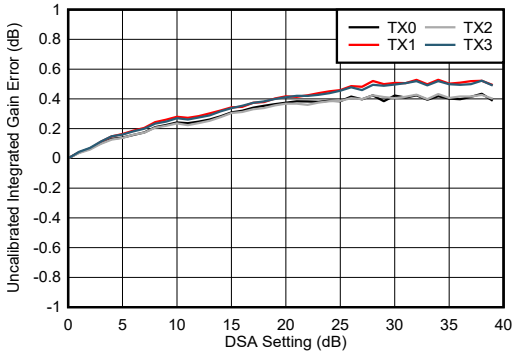
5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



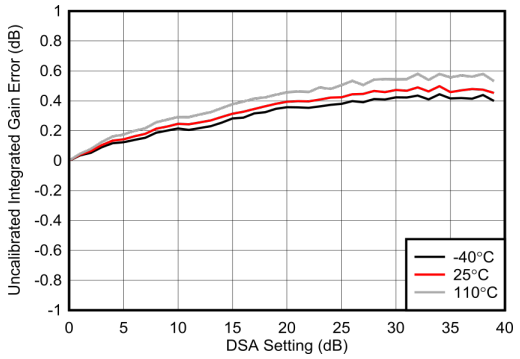
Differential Gain Error = Gain(DSA Setting – 1) – Gain(DSA Setting)

図 5-528. Calibrated Differential Gain Error vs Temperature at 7.1 GHz



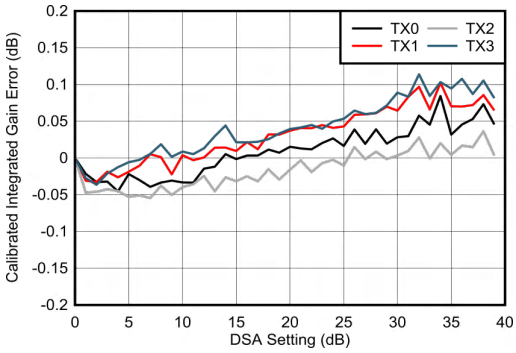
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 5-529. Uncalibrated Integrated Gain Error vs Channel at 7.1 GHz



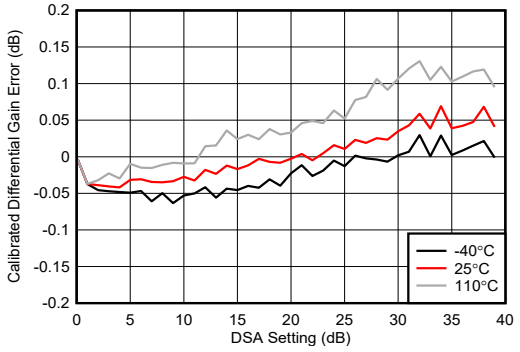
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 5-530. Uncalibrated Integrated Gain Error vs Temperature at 7.1 GHz



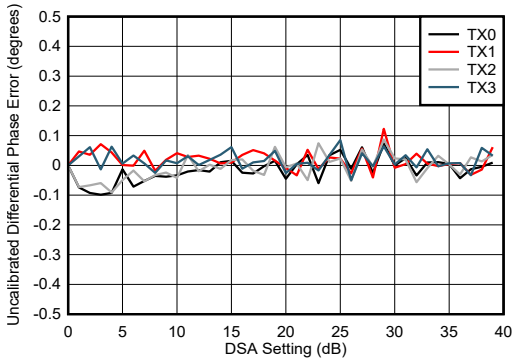
Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 5-531. Calibrated Integrated Gain Error vs Channel at 7.1 GHz



Integrated Gain Error = Gain(DSA Setting) – Gain(DSA Setting = 0).

図 5-532. Calibrated Integrated Gain Error vs Temperature at 7.1 GHz



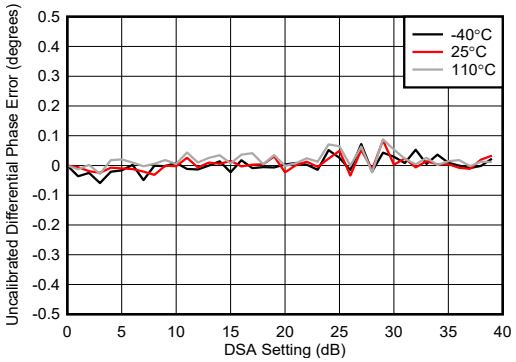
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 5-533. Uncalibrated Differential Phase Error vs Channel at 7.1 GHz

Copyright © 2023 Texas Instruments Incorporated

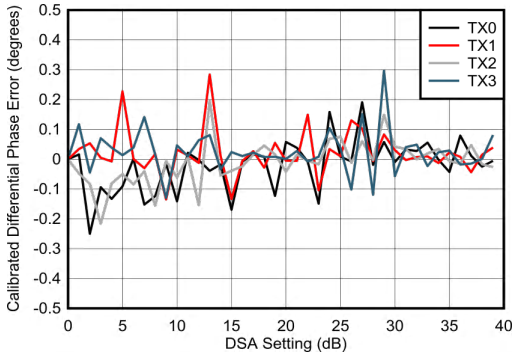
5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



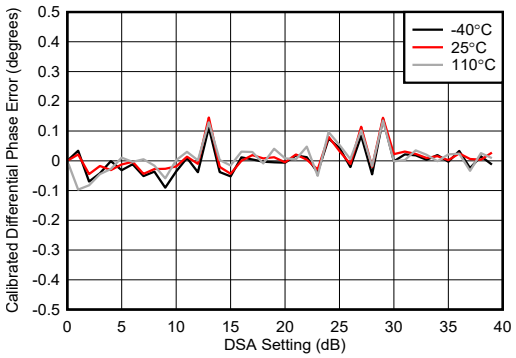
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 5-534. Uncalibrated Differential Phase Error vs Temperature at 7.1 GHz



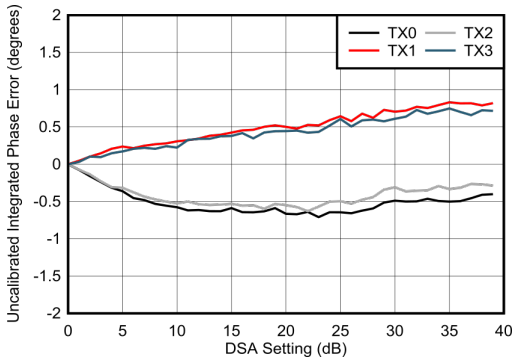
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 5-535. Calibrated Differential Phase Error vs Channel at 7.1 GHz



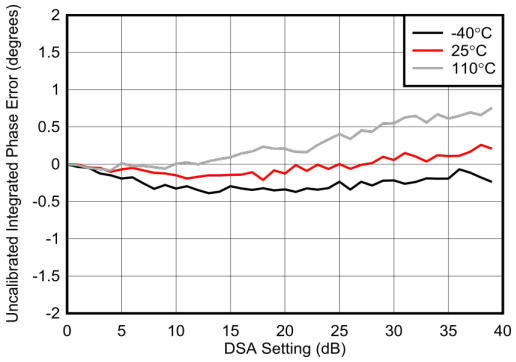
Differential Phase Error = Phase(DSA Setting – 1) – Phase(DSA Setting)

図 5-536. Calibrated Differential Phase Error vs Temperature at 7.1 GHz



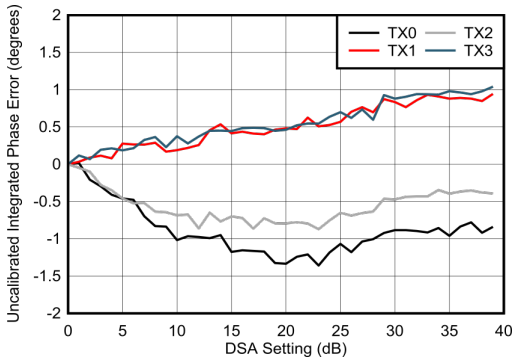
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-537. Uncalibrated Integrated Phase Error vs Channel at 7.1 GHz



Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-538. Uncalibrated Integrated Phase Error vs Temperature at 7.1 GHz



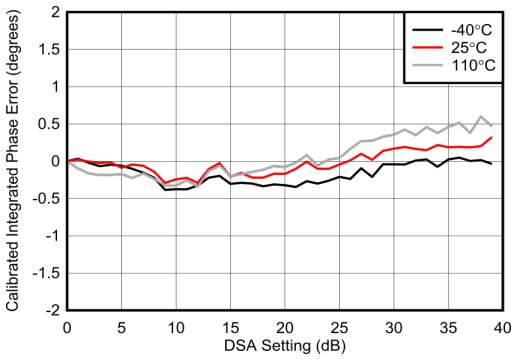
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-539. Calibrated Integrated Phase Error vs Channel at 7.1 GHz

Copyright © 2023 Texas Instruments Incorporated

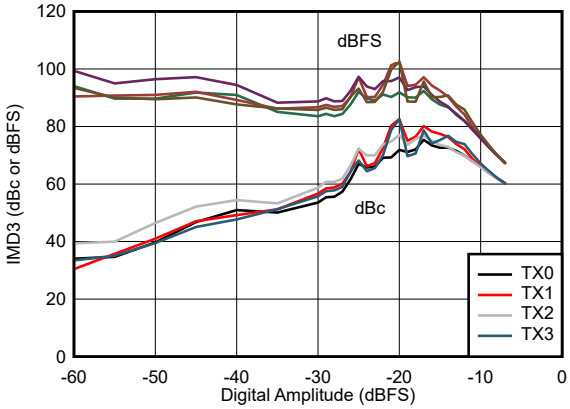
5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



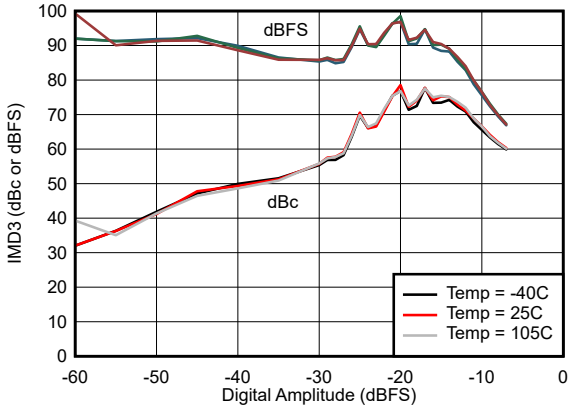
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

図 5-540. Calibrated Integrated Phase Error vs Temperature at 7.1 GHz



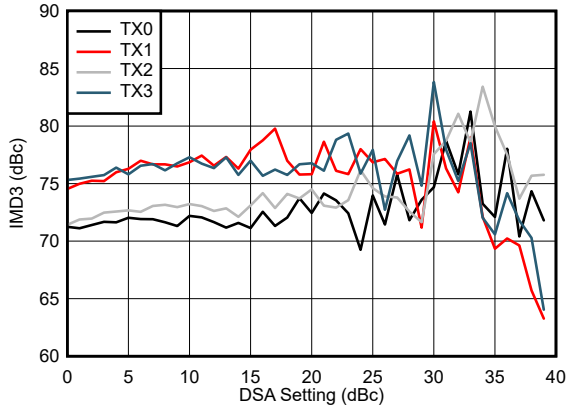
Tone spacing = 50MHz

図 5-541. IMD3 vs Digital Amplitude and Channel at 7.1 GHz



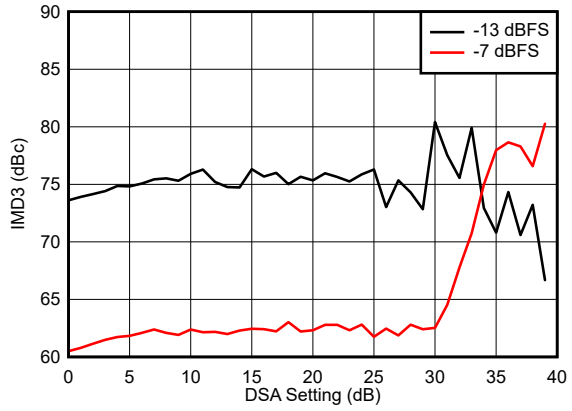
Tone spacing = 50MHz

図 5-542. IMD3 vs Digital Amplitude and Temperature at 7.1 GHz



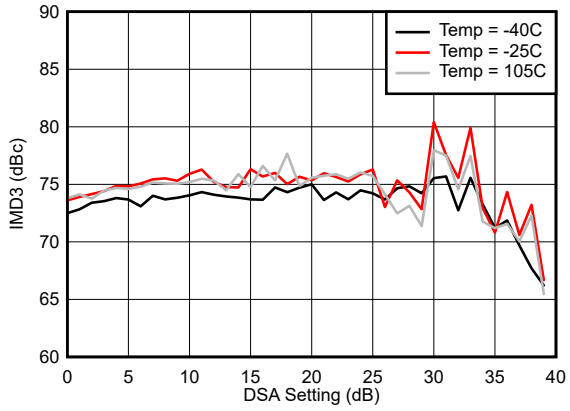
Tone spacing = 50MHz

図 5-543. IMD3 vs DSA Setting and Channel at 7.1 GHz



Tone spacing = 50MHz

図 5-544. IMD3 vs DSA Setting and Digital Amplitude at 7.1 GHz



Tone spacing = 50MHz

図 5-545. IMD3 vs DSA Setting and Temperature at 7.1 GHz

Copyright © 2023 Texas Instruments Incorporated

5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

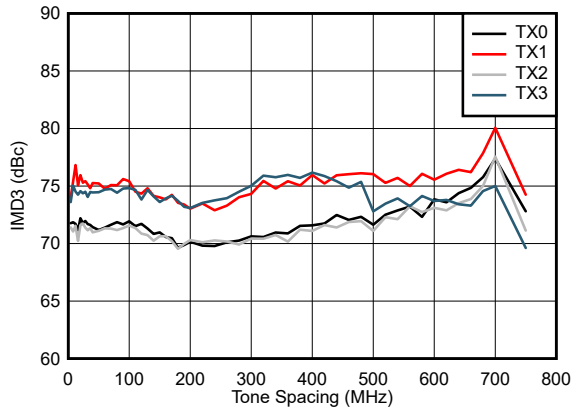


図 5-546. IMD3 vs Tone Spacing and Channel at 7.1 GHz

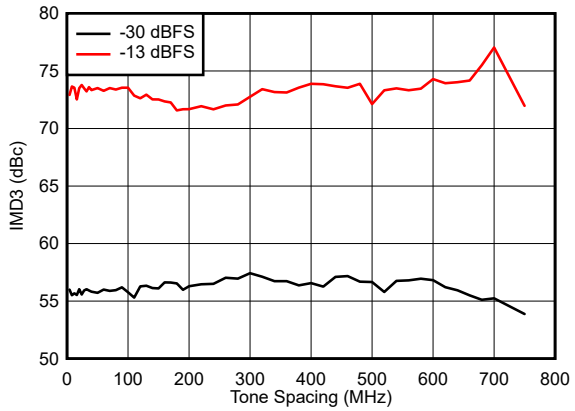


図 5-547. IMD3 vs Tone Spacing and Digital Amplitude at 7.1 GHz

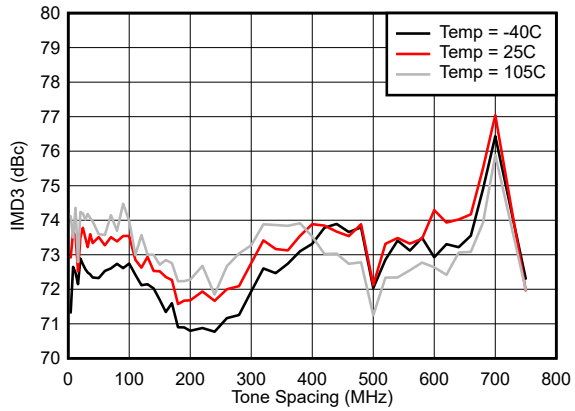
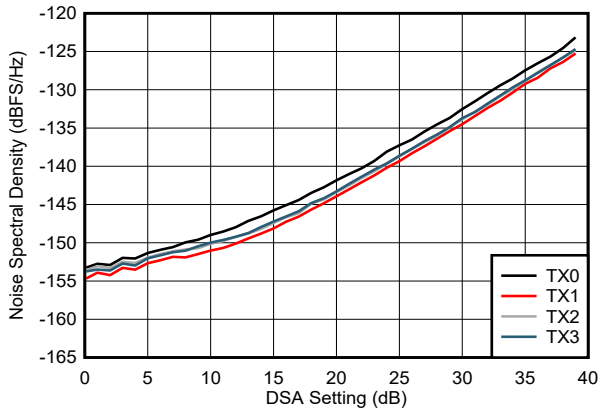
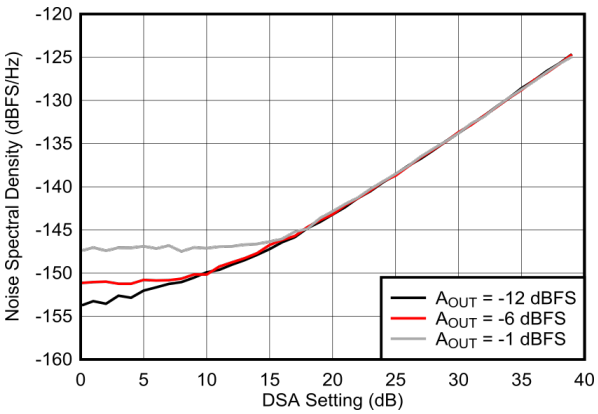


図 5-548. IMD3 vs Tone Spacing and Temperature at 7.1 GHz



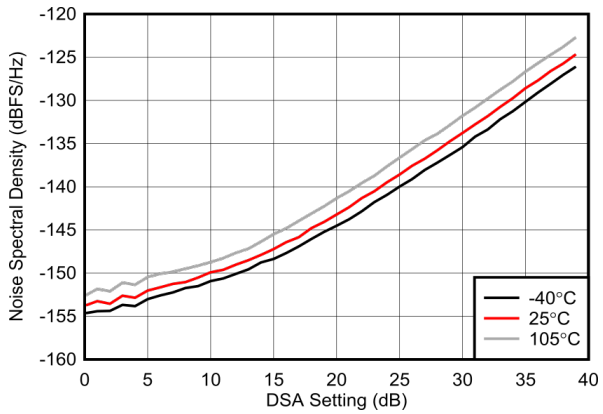
Tone at -12dBFS, 50MHz offset from tone

図 5-549. NSD vs DSA Setting and Channel at 7.1 GHz



50MHz offset from tone

図 5-550. NSD vs DSA Setting and Amplitude at 7.1 GHz



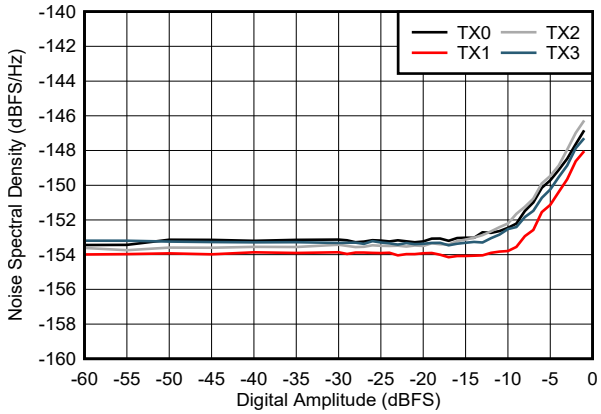
Tone at -12dBFS, 50MHz offset from tone

図 5-551. NSD vs DSA Setting and Temperature at 7.1 GHz

Copyright © 2023 Texas Instruments Incorporated

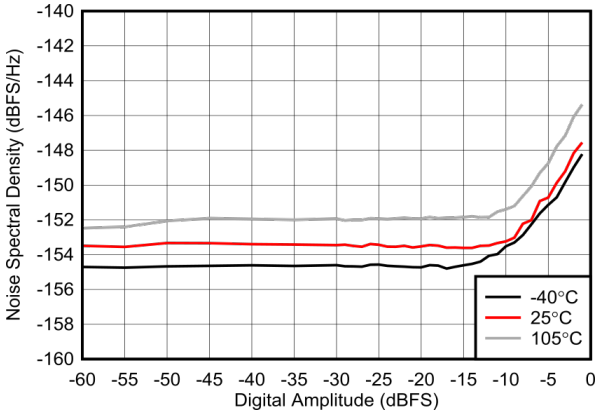
5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.



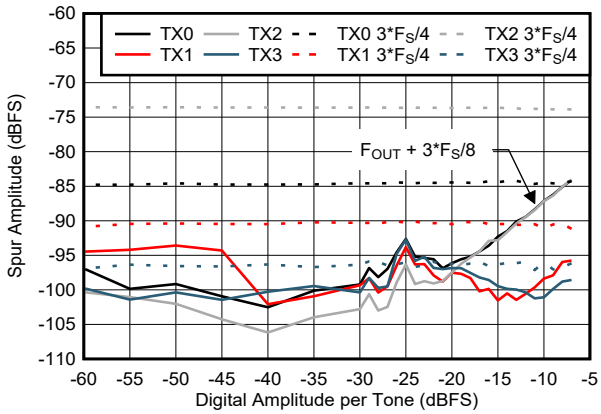
50MHz offset from tone

図 5-552. NSD vs Digital Amplitude and Channel at 7.1 GHz



50MHz offset from tone

図 5-553. NSD vs Digital Amplitude and Temperature at 7.1 GHz



Inband = 7100MHz ± 600MHz, excluding IMD3 components, 3*F_S/4 spur not included and shown separately

図 5-554. Two Tone Inband SFDR vs Digital Amplitude at 7.1 GHz

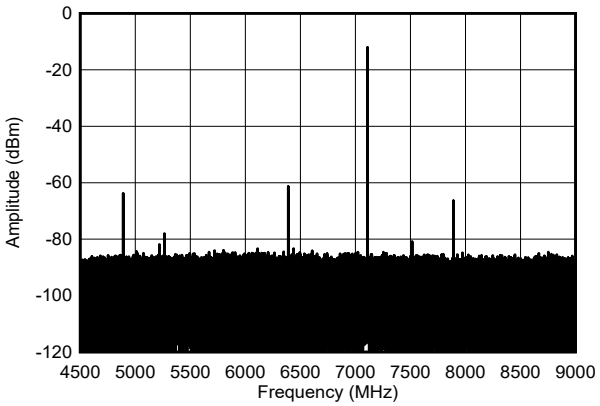


図 5-555. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Nyquist)

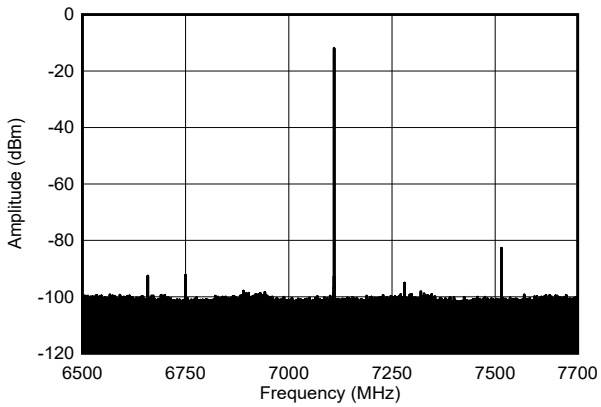


図 5-556. Single Tone Output Spectrum at 7.1GHz, -1dBFS (Inband)

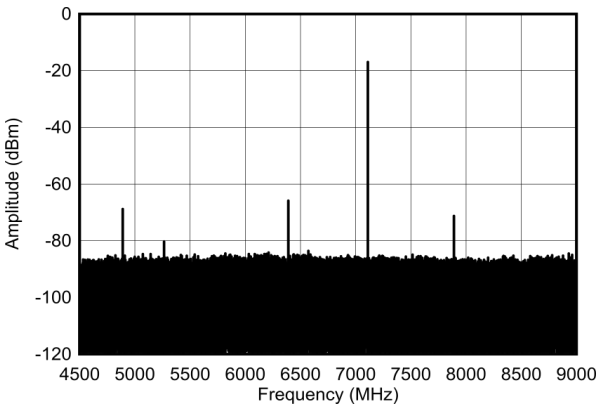


図 5-557. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Nyquist)

5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

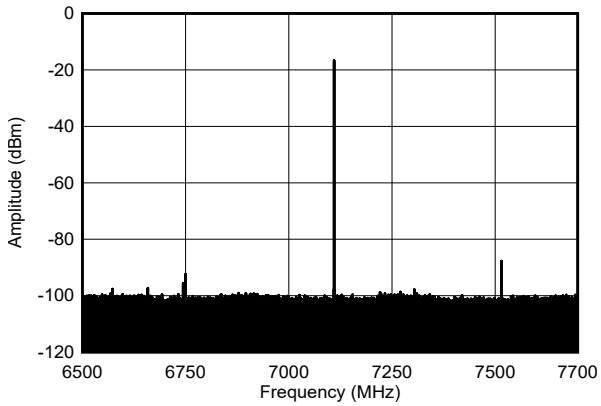


図 5-558. Single Tone Output Spectrum at 7.1GHz, -6dBFS (Inband)

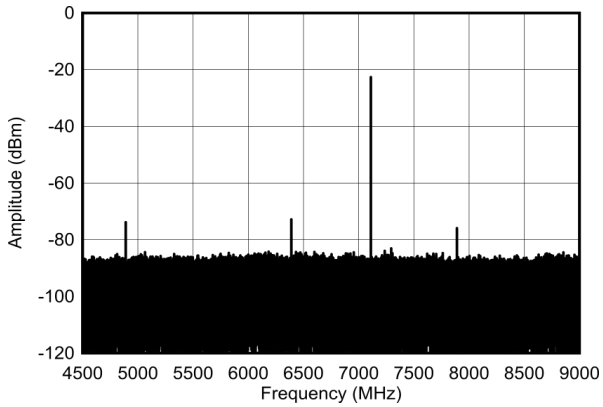


図 5-559. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Nyquist)

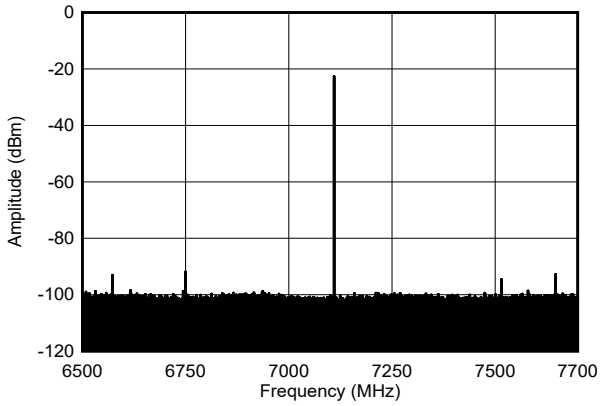
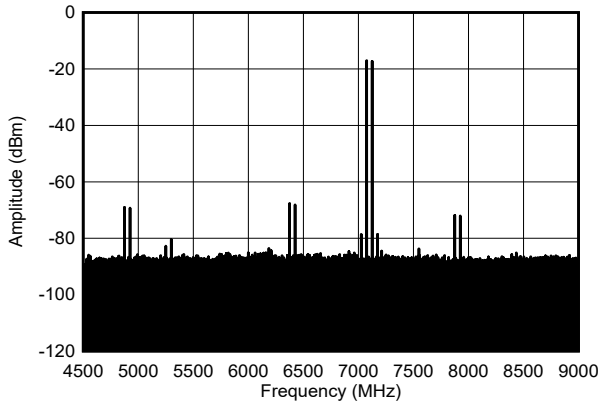
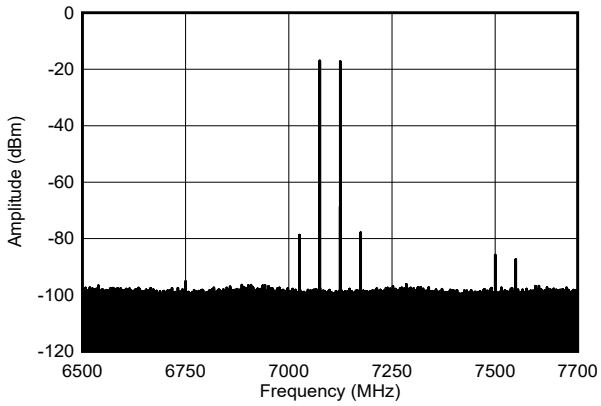


図 5-560. Single Tone Output Spectrum at 7.1GHz, -12dBFS (Inband)



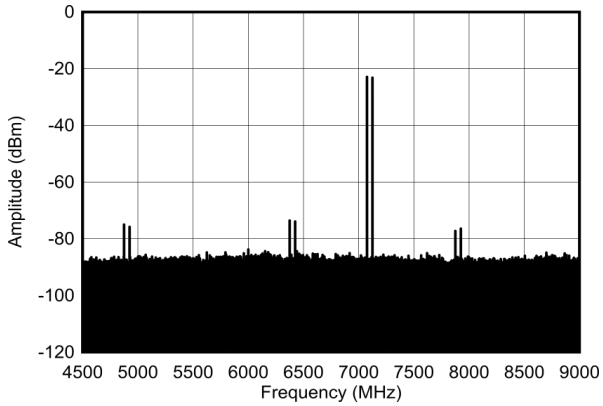
50MHz Tone Spacing

図 5-561. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Nyquist)



50MHz Tone Spacing

図 5-562. Two Tone Output Spectrum at 7.1GHz, -7dBFS each (Inband)



50MHz Tone Spacing

図 5-563. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Nyquist)

Copyright © 2023 Texas Instruments Incorporated

5.12.13 TX Typical Characteristics at 7.1GHz (continued)

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, TX input data rate = 750MSPS, f_{DAC} = 9000MSPS, non-interleave mode, A_{OUT} = –1 dBFS, 2nd Nyquist zone output, External clock mode, 12x Interpolation, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 7.1GHz matching.

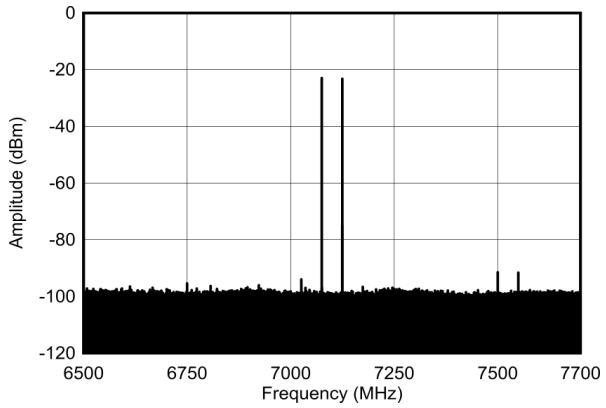


図 5-564. Two Tone Output Spectrum at 7.1GHz, -13dBFS each (Inband)

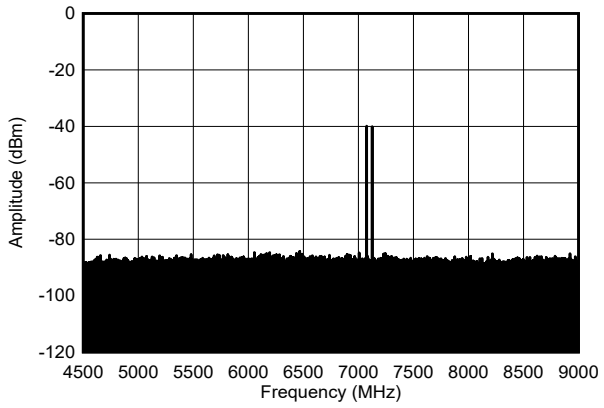


図 5-565. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Nyquist)

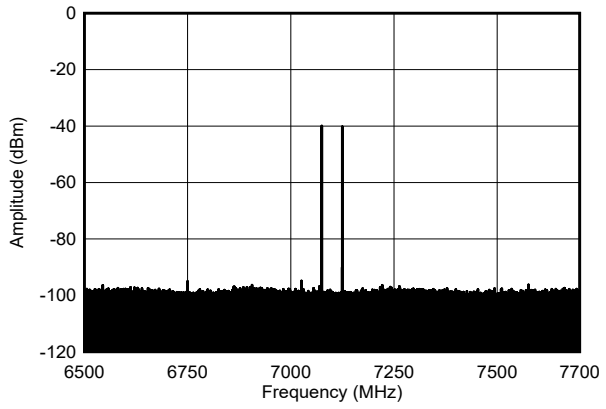


図 5-566. Two Tone Output Spectrum at 7.1GHz, -30dBFS each (Inband)

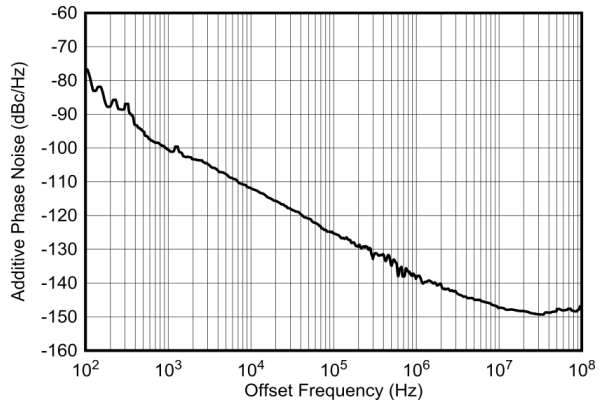
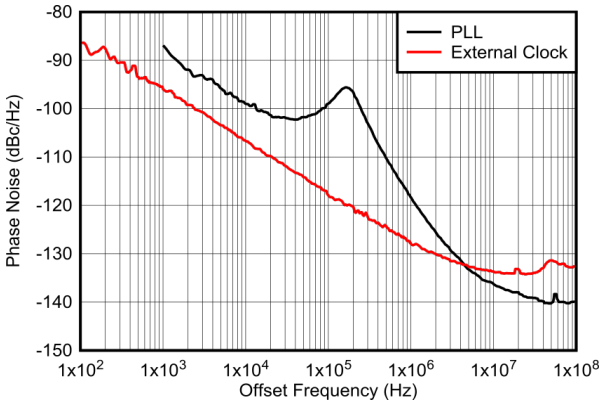


図 5-567. External Clock Additive Phase Noise at 7.1 GHz

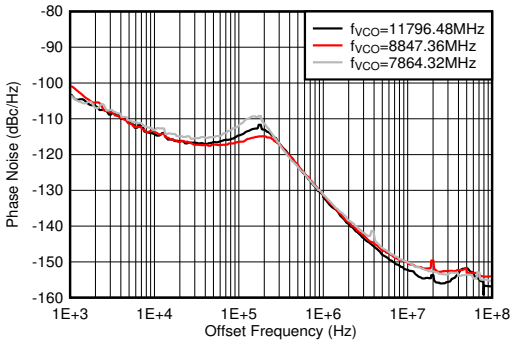
5.12.14 PLL and Clock Typical Characteristics

Typical values at T_A = +25°C with nominal supplies. Unless otherwise noted, f_{REF} = 491.52 MHz, Phase noise measured at TX output



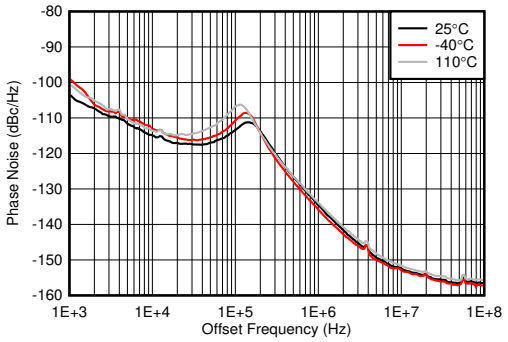
measured at TX output, normalized to 12GHz by 20*log10(12GHz/F_{OUT})

図 5-568. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz



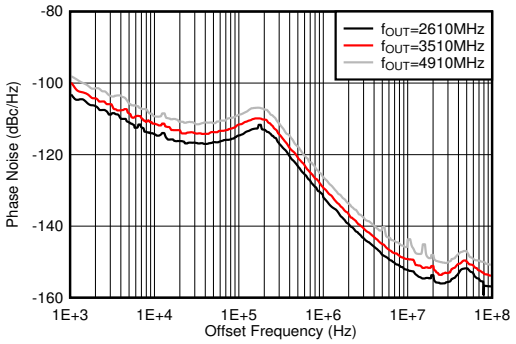
PLL enabled, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-569. Phase Noise vs Offset Frequency and f_{VCO} at f_{OUT} = 2610 MHz



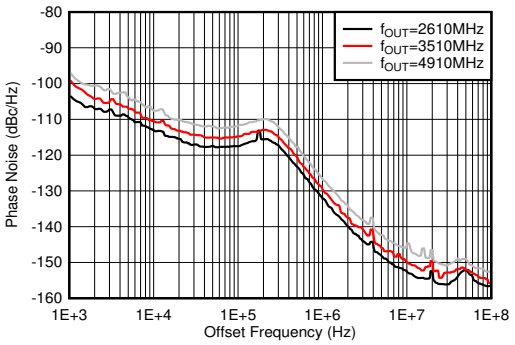
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-570. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



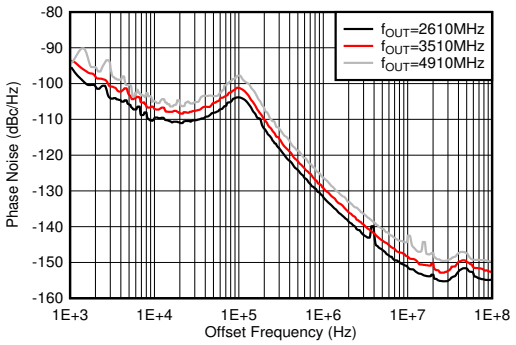
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-571. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

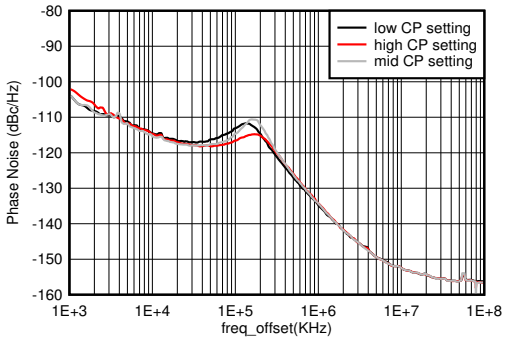
図 5-572. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

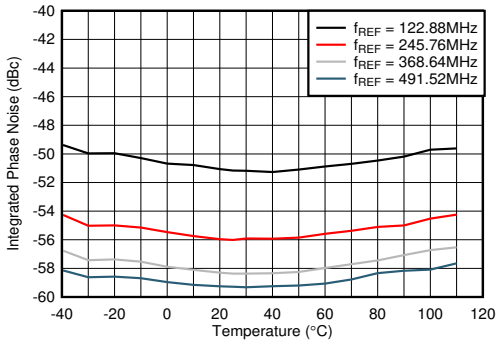
図 5-573. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C

Copyright © 2023 Texas Instruments Incorporated



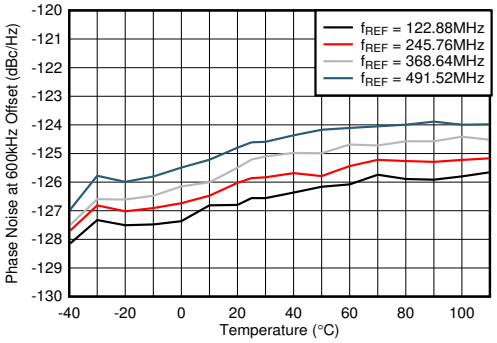
PLL enabled, f_{VCO} = 11796.48 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-574. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at f_{OUT} = 2.6 GHz



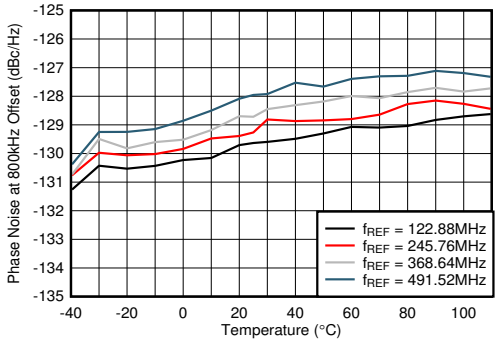
PLL enabled, f_{VCO} = 11796.48 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 5-575. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



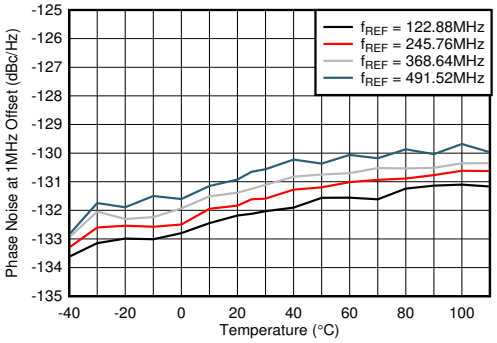
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 5-576. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



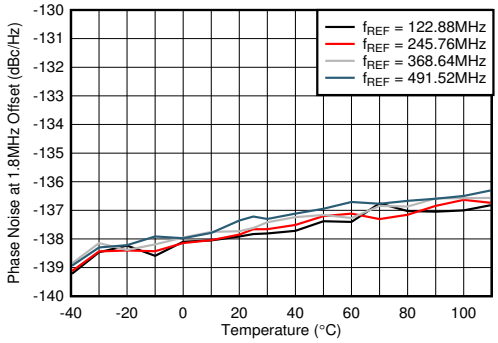
A. PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 5-577. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

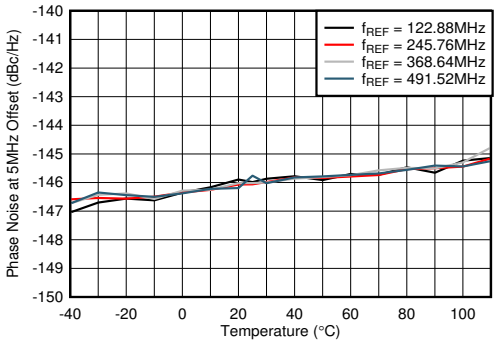
図 5-578. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

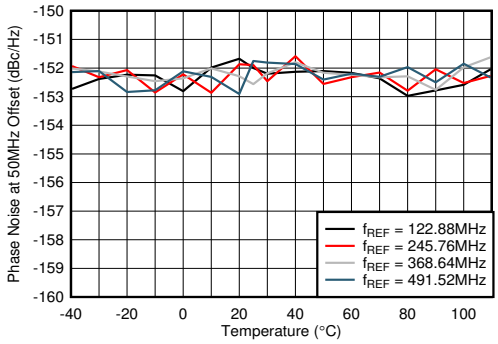
図 5-579. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated



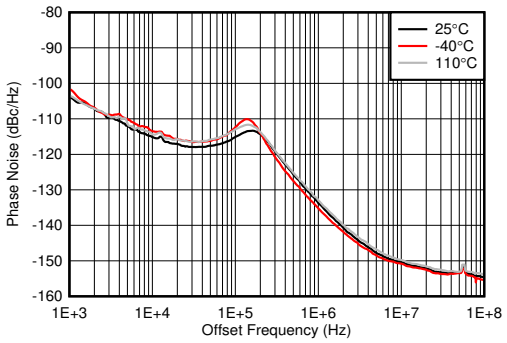
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 5-580. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



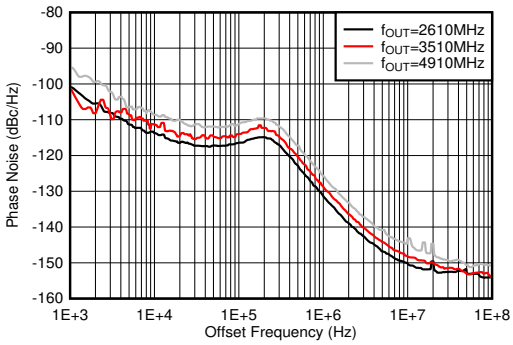
PLL enabled, f_{VCO} = 11796.48 MHz, measured at 2TXOUT

図 5-581. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



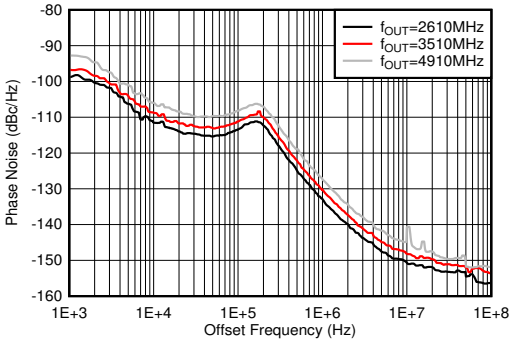
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-582. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



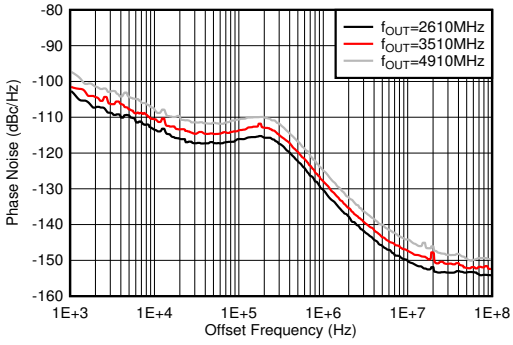
PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-583. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

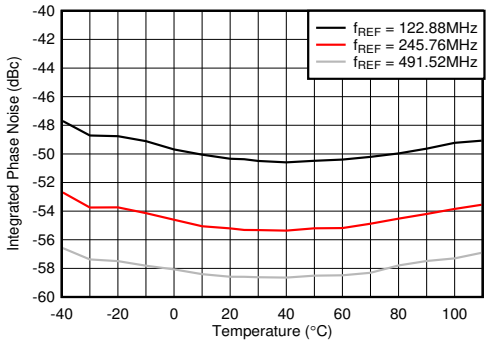
図 5-584. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



PLL enabled, f_{VCO} = 9830.4 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

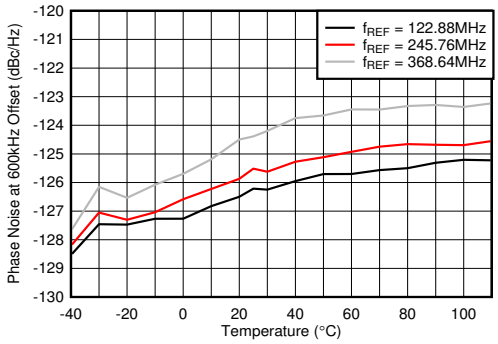
図 5-585. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C

Copyright © 2023 Texas Instruments Incorporated



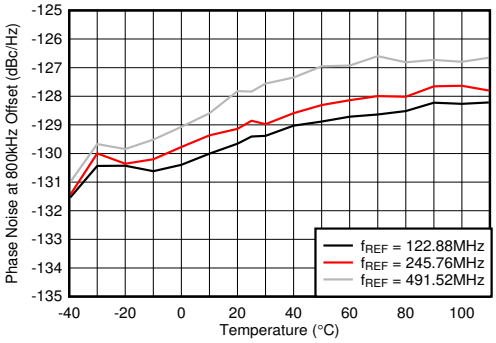
PLL enabled, f_{VCO} = 9830.4 MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

図 5-586. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



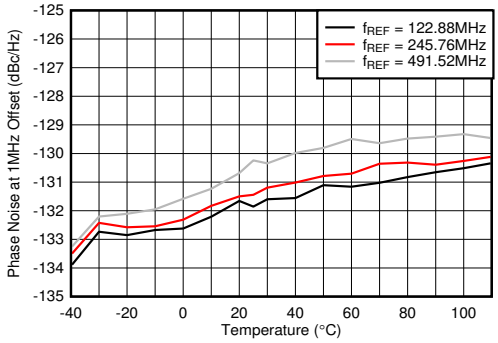
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 5-587. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



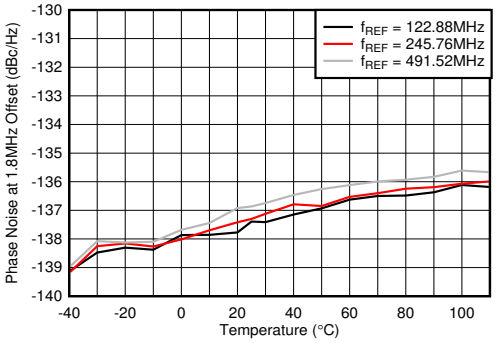
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 5-588. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



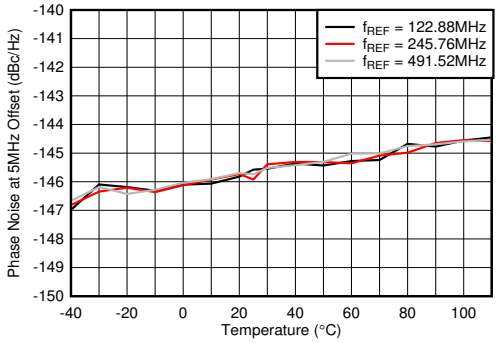
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 5-589. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

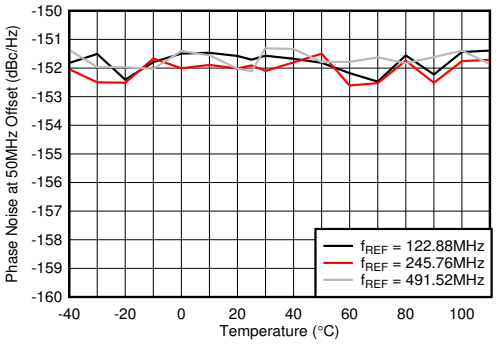
図 5-590. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

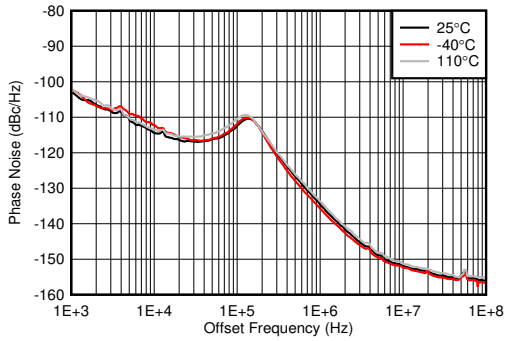
図 5-591. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated



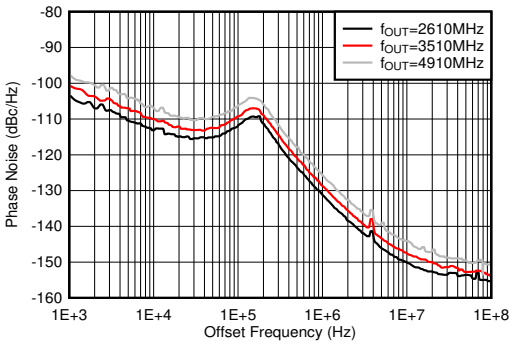
PLL enabled, f_{VCO} = 9830.4 MHz, measured at 2TXOUT

図 5-592. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at f_{OUT} = 2.6 GHz



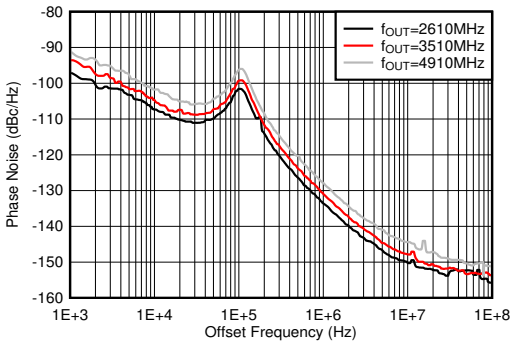
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-593. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz



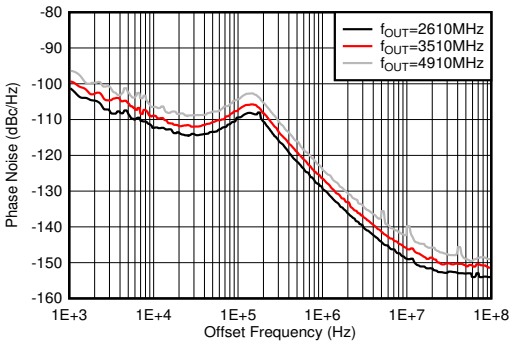
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-594. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



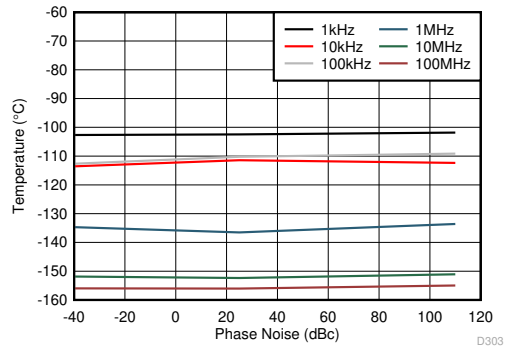
PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-595. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at –40°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

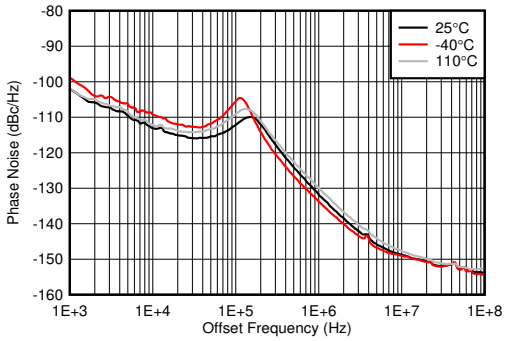
図 5-596. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, f_{VCO} = 8847.36 MHz, f_{REF} = 491.52MSPS, minimum LPF BW, measured at 2TXOUT

図 5-597. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at f_{OUT} = 2.6 GHz

Copyright © 2023 Texas Instruments Incorporated



PLL enabled, f_{VCO} = 7864.32 MHz, f_{REF} = 491.52MSPS, measured at 2TXOUT

図 5-598. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at f_{OUT} = 1910 MHz

Copyright © 2023 Texas Instruments Incorporated

6 Device and Documentation Support

6.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

6.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

6.3 商標

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

6.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

6.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2023 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7900IABJ	Active	Production	FCBGA (ABJ) | 400	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7900I
AFE7900IALK	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	SNPB	Level-3-220C-168 HR	-40 to 85	AFE7900 SNPB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

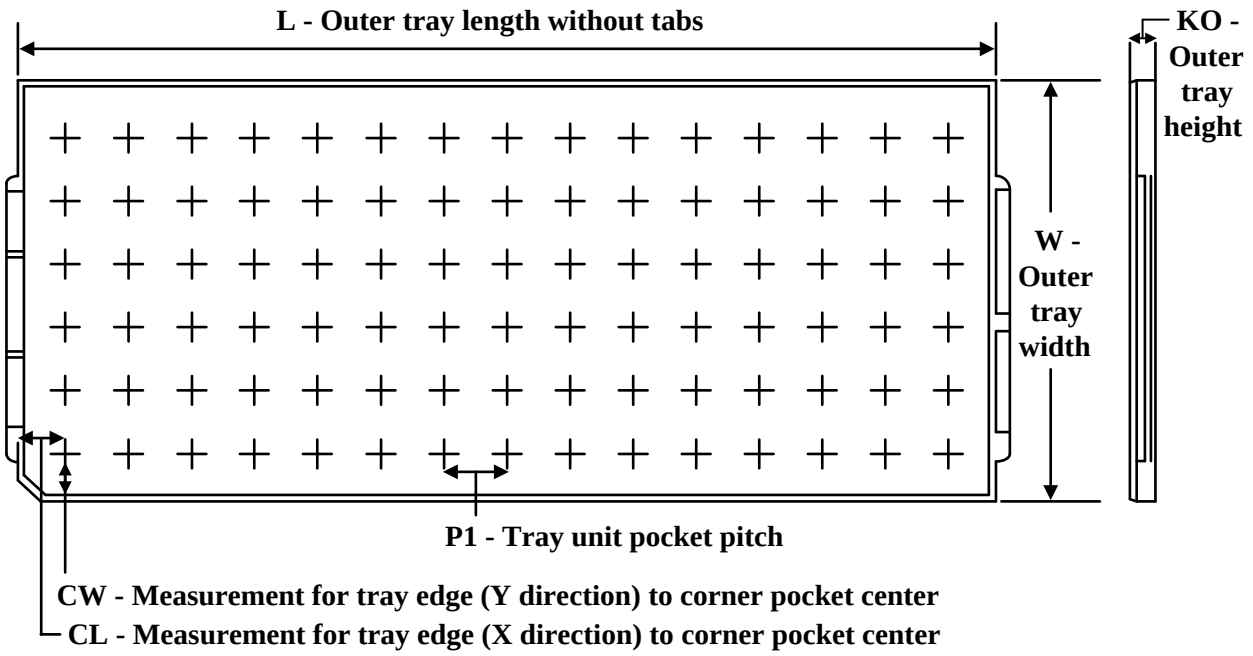
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

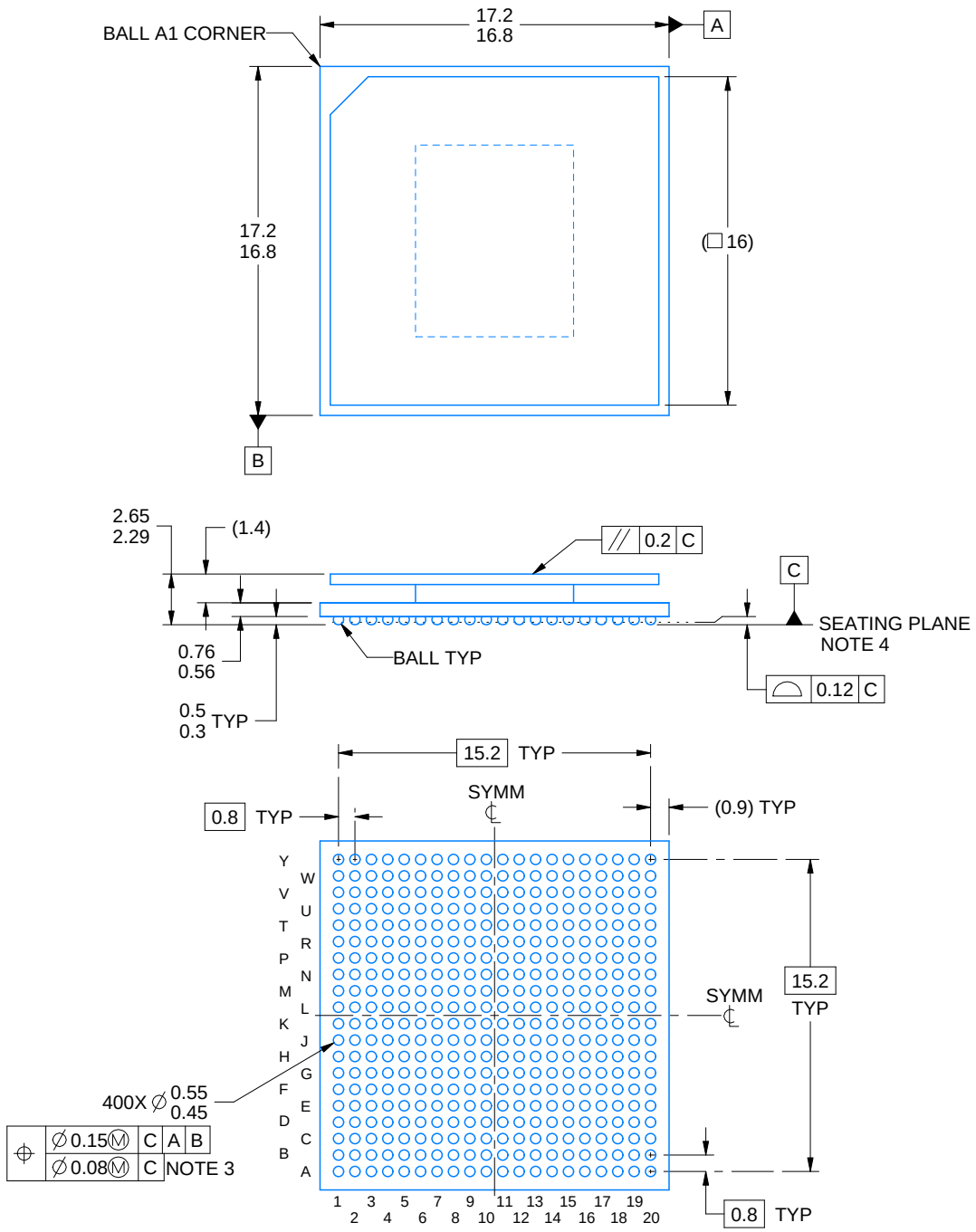
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7900IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7900IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7900IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7900IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

PACKAGE OUTLINE

ABJ0400A

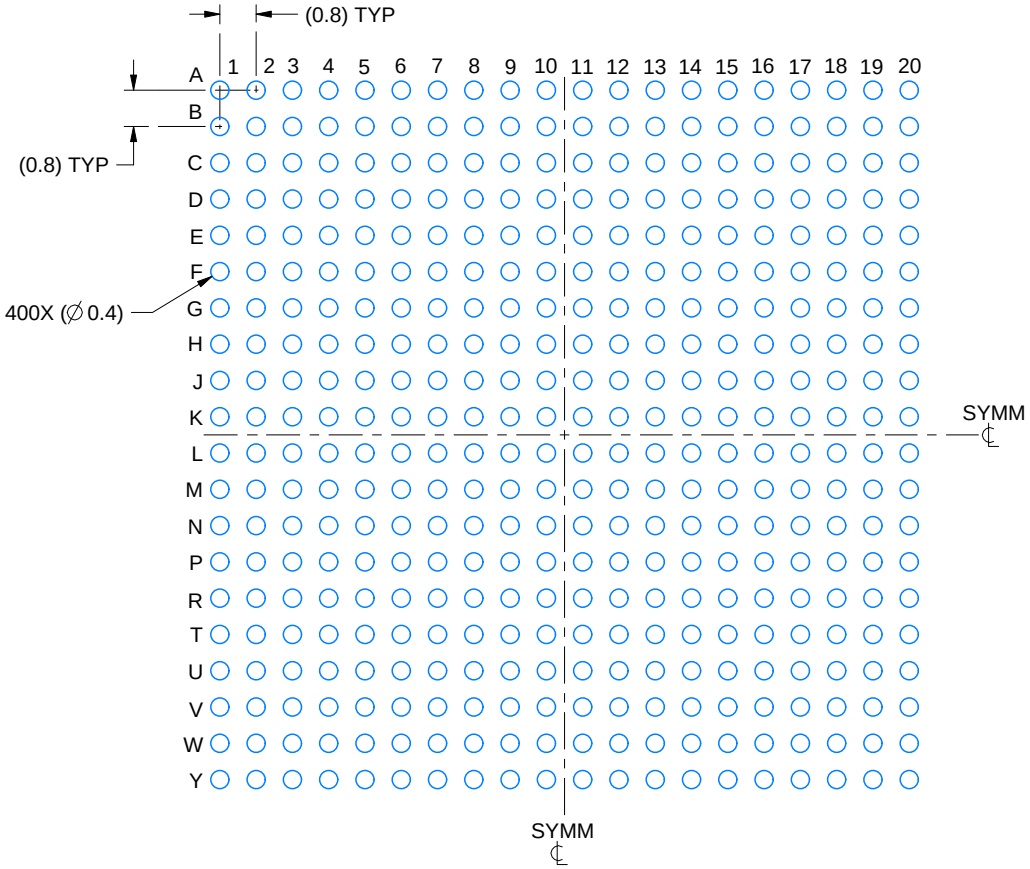
FCBGA - 2.65 mm max height

BALL GRID ARRAY

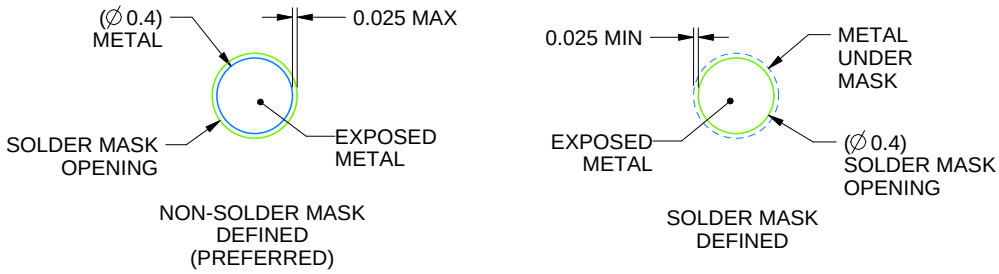


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

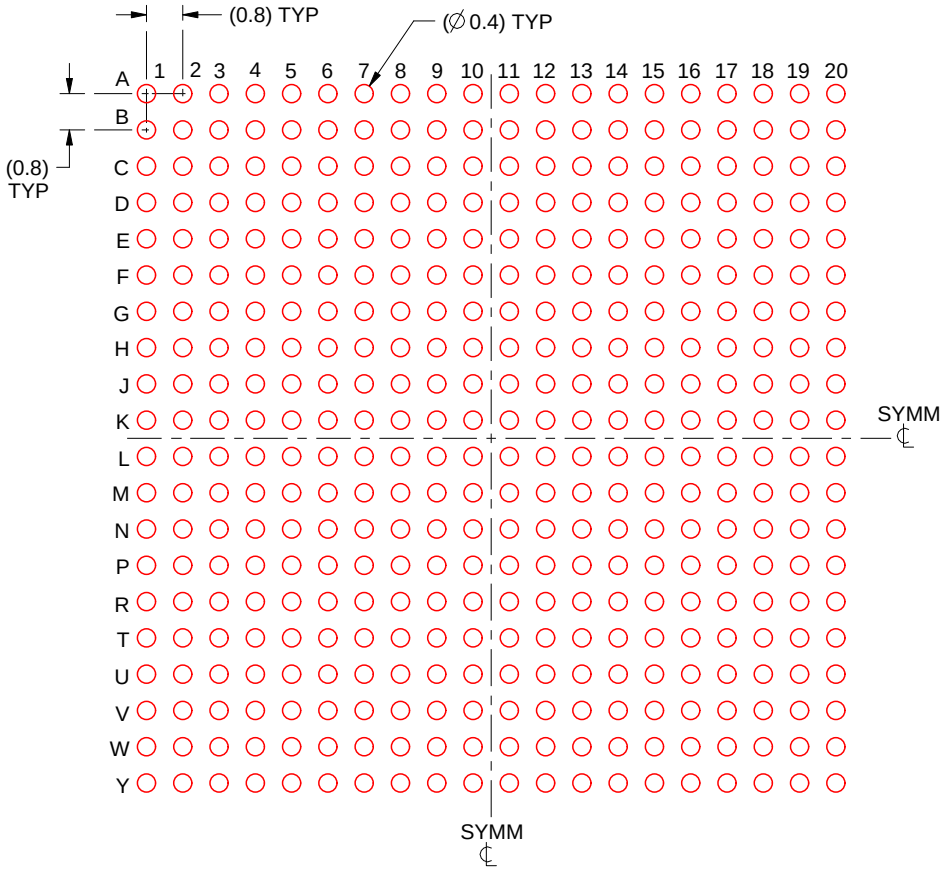


SOLDER MASK DETAILS
NOT TO SCALE

4221311/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4221311/D 03/2023

NOTES: (continued)

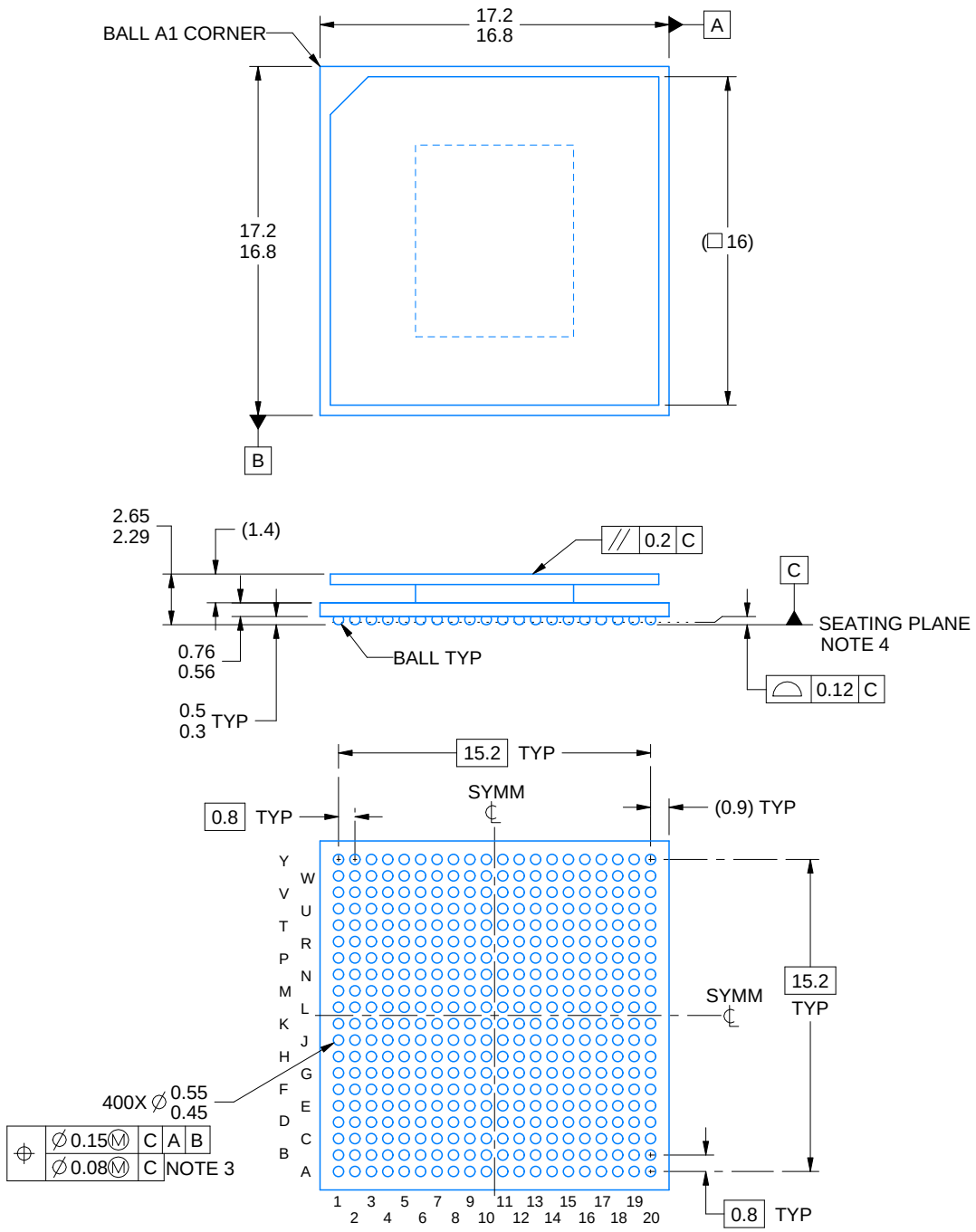
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

ALK0400A

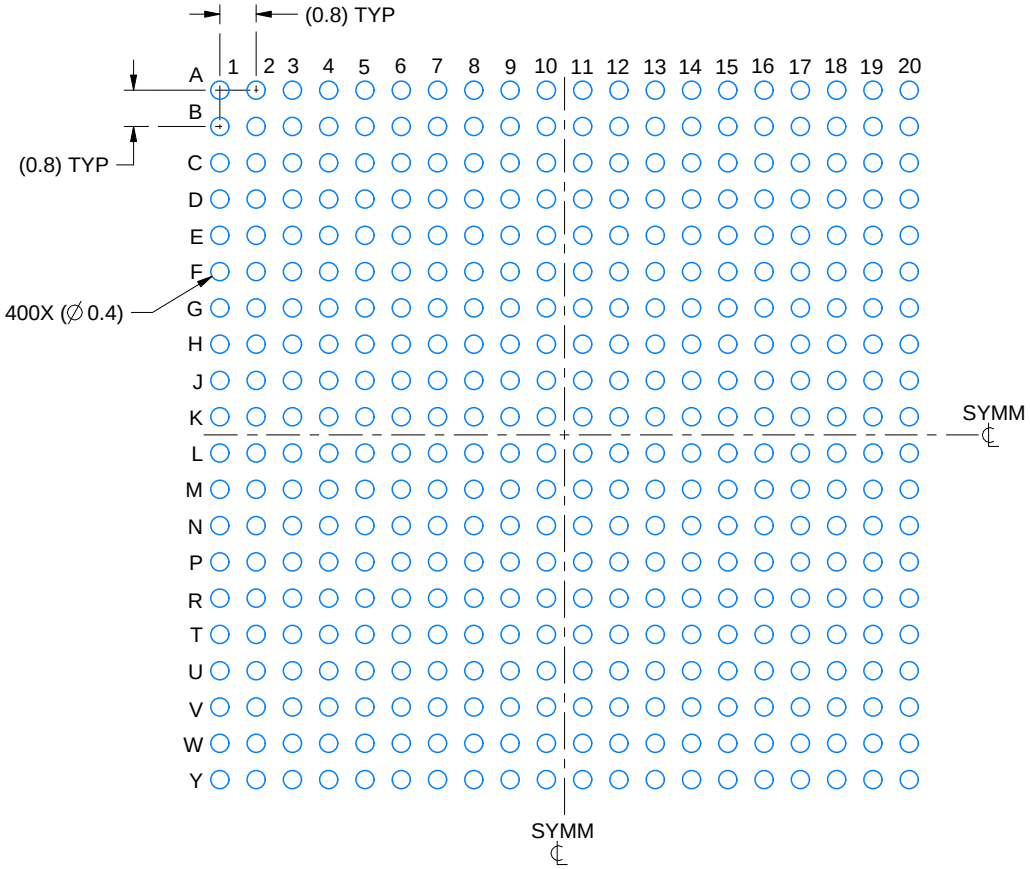
FCBGA - 2.65 mm max height

BALL GRID ARRAY

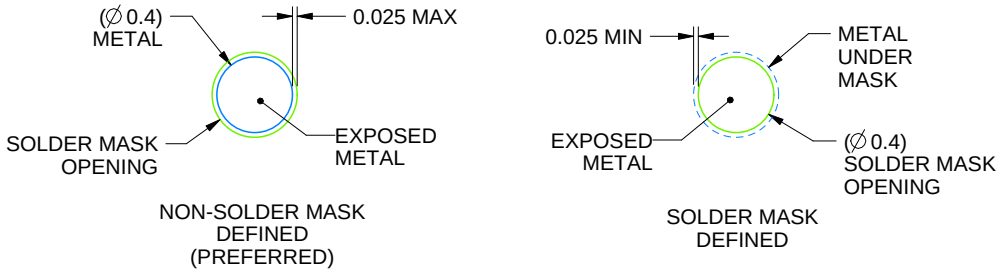


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

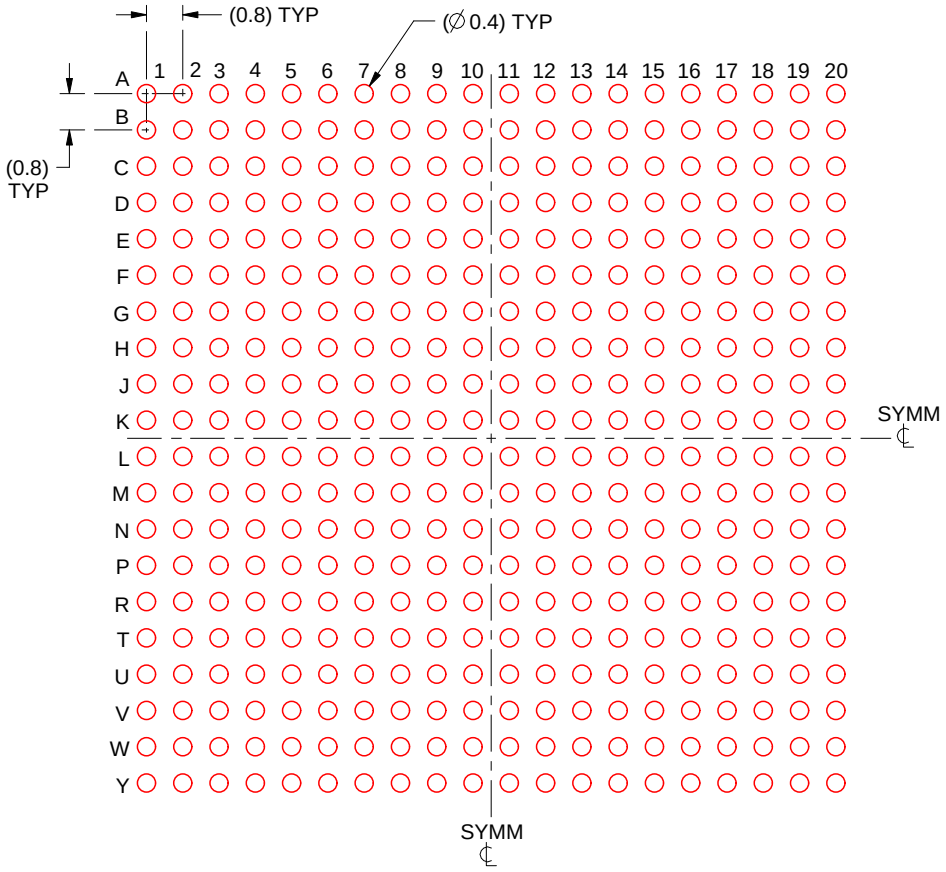


SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月