TEXAS INSTRUMENTS
AMC1035-Q1
JAJSHF7A – MAY 2019 – REVISED NOVEMBER 2019

AMC1035-Q1 デルタ・シグマ変調器 ±1V バイポーラ入力、2.5V 基準出力搭載

1 特長

- **車載アプリケーション用に AEC-Q100 認定取得済み**
  - 温度グレード 1：-40℃～+125℃、T_A
- **電圧および温度センシング用に最適化されたデルタ・シグマ変調器**
  - 入力電圧範囲：±1V
  - 高い差動入力抵抗：1.6GΩ (標準値)
  - 内蔵の 2.5V、±5mA 基準電圧によるレシオメトリック測定
- **非常に優れた DC 性能**
  - オフセット誤差：±0.5mV (最大値)
  - オフセット・ドリフト係数：±6μV/℃ (最大値)
  - ゲイン誤差：±0.25% (最大値)
  - ゲイン・ドリフト係数：±45ppm/℃ (最大値)
  - レシオメトリック・ゲイン・ドリフト係数：±15ppm/℃ (最大値)
- **マンチェスター・エンコードまたはコード化なしのビットストリーム出力を選択可能**

2 アプリケーション

- **次の用途での電圧および温度センシング**
  - トラクション・インバータ
  - オンボード充電器
  - DC/DC コンバータ
  - 集積型電源モジュール

3 概要

AMC1035-Q1 は、3.0V～5.5V の単一電源と、外部から供給される 9MHz～21MHz の範囲のクロック信号で動作する高精度デルタ・シグマ (ΔΣ) 変調器です。マンチェスター・モードでは、規定のクロック範囲は 9MHz～11MHz です。本デバイスの差動 ±1V 入力構造は、電圧および温度センシング・アプリケーション用に最適化されています。

AMC1035-Q1 のビットストリーム出力をマンチェスター符号化するよう選択すると、受信側デバイスのセットアップおよびホールド時間の要件を考慮する必要がなくなり、回路レイアウトの労力を削減できます。デジタル・フィルタ (TMS320F28004x、TMS320F2807x、TMS320F2837x マイクロコントローラ・ファミリに内蔵されているものなど) を使用して出力ビットストリームを間引くと、82kSPS の データ速度、87dB のダイナミック・レンジで、16 ビットの分解能が得られます。

AMC1035-Q1 の内部基準電圧源はレシオメトリックな回路アーキテクチャをサポートしているため、電源電圧の変動や温度ドリフトが測定精度に及ぼす悪影響を最小限に抑えられます。

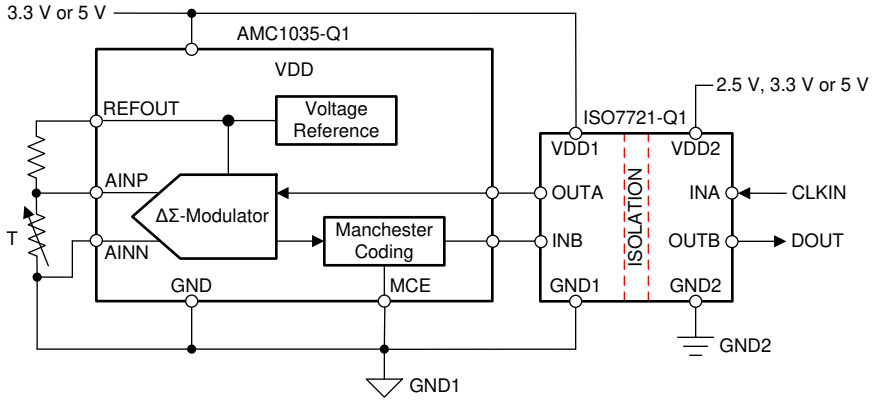
また、AMC1035-Q1 はデジタル・アイソレータと絶縁電源を使用して、高い同相 AC 電圧センシングにも使用できます。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
AMC1035-Q1	SOIC (8)	4.90mm×3.90mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーションの例



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

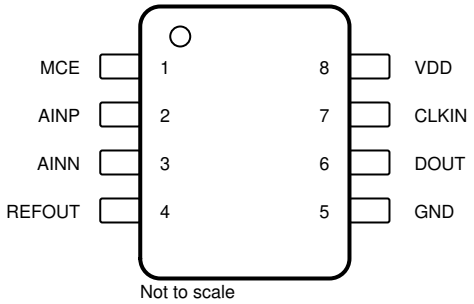
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- ドキュメント・ステータスを事前情報から量産データに 変更 ... 1

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5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MCE	I	Manchester coding enabled, active high, with internal pulldown resistor (typical value: 200 kΩ). The polarity of this signal must not be changed when the clock signal is applied.
2	AINP	I	Noninverting analog input.
3	AINN	I	Inverting analog input.
4	REFOUT	O	Reference output: 2.5 V nominal, maximum ±5-mA sink and source capability.
5	GND	—	Ground reference.
6	DOUT	O	Modulator bitstream data output, updated with the rising edge of the clock signal present on CLKIN. This pin is a Manchester coded output if MCE is pulled high. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.
7	CLKIN	I	Modulator clock input: 9 MHz to 21 MHz with an internal pulldown resistor (typical value: 200 kΩ). The clock signal must be applied continuously for proper device operation; see the *Clock Input* section for additional details.
8	VDD	—	Power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

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6 Specifications

6.1 Absolute Maximum Ratings

see(1)

PARAMETER		MIN	MAX	UNIT
Supply voltage	VDD to GND	–0.3	7	V
Analog input voltage	At AINP or AINN	GND – 5	VDD + 0.5	V
Analog output voltage	At REFOUT	GND – 0.5	VDD + 0.5	V
Digital input voltage	At CLKIN or MCE	GND – 0.5	VDD + 0.5	V
Digital output voltage	At DOUT	GND – 0.5	VDD + 0.5	V
Input current	Any pin except supply pins	–10	10	mA
Temperature	Maximum virtual junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings Automotive

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	Corner pins (1, 4, 5, and 8)	±1000	
			Other pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{AINP} – V_{AINN}$		±1.25		V
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{AINP} – V_{AINN}$	–1		1	V
	Absolute common-mode input voltage(1)	$(V_{AINP} + V_{AINN}) / 2$ to GND	–2		VDD	V
V_{CM}	Operating common-mode input voltage(2)	$(V_{AINP} + V_{AINN}) / 2$ to GND, 3.0 V ≤ VDD < 4 V, $V_{AINP} = V_{AINN}$	–1.4		VDD – 1.4	V
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 3.0 V ≤ VDD < 4.5 V, $\lvert V_{AINP} – V_{AINN} \rvert = 1.25$ V	–0.8		VDD – 2.4	
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 4 V ≤ VDD ≤ 5.5 V, $V_{AINP} = V_{AINN}$	–1.4		2.7	
		$(V_{AINP} + V_{AINN}) / 2$ to GND, 4.5 V ≤ VDD ≤ 5.5 V, $\lvert V_{AINP} – V_{AINN} \rvert = 1.25$ V	–0.8		2.1	
DIGITAL INPUT						
	Input voltage	V_{MCE} or V_{CLKIN} to GND	GND		VDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40	25	125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) See the *Analog Input* section for more details.

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6.4 Thermal Information

THERMAL METRIC[1]		AMC1035-Q1 D (SOIC) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	120	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	61	°C/W
Y_{JT}	Junction-to-top characterization parameter	10	°C/W
Y_{JB}	Junction-to-board characterization parameter	60	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

minimum and maximum specifications are at T_A = –40°C to 125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{CMuv}	Negative common-mode undervoltage detection level	(V_{AINP} + V_{AINN}) / 2 to GND, V_{AINP} = V_{AINN}			–1.45	V
		(V_{AINP} + V_{AINN}) / 2 to GND, |V_{AINP} – V_{AINN}| = 1.25 V			–0.85	
V_{CMov}	Positive common-mode overvoltage detection level	(V_{AINP} + V_{AINN}) / 2 to GND, V_{AINP} = V_{AINN}, 3.0 V ≤ VDD < 4.5 V			VDD – 1.35	V
		(V_{AINP} + V_{AINN}) / 2 to GND, |V_{AINP} – V_{AINN}| = 1.25 V, 3.0 V ≤ VDD < 4.5 V			VDD – 2.35	
		(V_{AINP} + V_{AINN}) / 2 to GND, V_{AINP} = V_{AINN}, 4.5 V ≤ VDD ≤ 5.5 V	2.75			
		(V_{AINP} + V_{AINN}) / 2 to GND, |V_{AINP} – V_{AINN}| = 1.25 V, 4.5 V ≤ VDD ≤ 5.5 V	2.15			
R_{IN}	Single-ended input resistance	AINN = GND	0.1	0.4		GΩ
R_{IND}	Differential input resistance		0.16	1.6		GΩ
C_{IN}	Single-ended input capacitance	AINN = GND		2		pF
C_{IND}	Differential input capacitance			2		pF
I_{IB}	Input bias current	AINP = AINN = GND; I_{IB} = (I_{IBP} + I_{IBN}) / 2	–10	±3	10	nA
TCI_{IB}	Input bias current drift	AINP = AINN = GND; I_{IB} = (I_{IBP} + I_{IBN}) / 2		±5		pA/°C
I_{IO}	Input offset current	I_{IO} = I_{IBP} - I_{IBN}	–5	±1	5	nA
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, V_{CMmin} ≤ V_{IN} ≤ V_{CMmax}		–104		dB
		f_{IN} from 0.1 Hz to 50 kHz, V_{CMmin} ≤ V_{IN} ≤ V_{CMmax}		–88		
DC ACCURACY						
	Resolution	Decimation filter output set to 16 bits	16			Bit
INL	Integral nonlinearity	Resolution: 16 bits	–12	±2	12	LSB
E_O	Offset error	Initial, at 25°C, AINP = AINN = GND	–0.5	±0.03	0.5	mV
TCE_O	Offset error thermal drift		–6	±0.1	6	µV/°C
E_G	Gain error	Initial, at 25°C	–0.25	±0.02	0.25	%
		Initial, at 25°C, ratiometric mode	–0.3	±0.02	0.3	
TCE_G	Gain error thermal drift		–45	±20	45	ppm/°C
		ratiometric mode	–15	±4	15	
PSRR	Power-supply rejection ratio	AINP = AINN = GND, VDD from 3.0 V to 5.5 V, at DC		–90		dB
		AINP = AINN = GND, VDD from 3.0 V to 5.5 V, 10 kHz / 100 mV ripple		–84		

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Electrical Characteristics (continued)

minimum and maximum specifications are at T_A = –40°C to 125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = 0 V, and sinc^3 filter with OSR = 256, unless otherwise noted. Typical values are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	81	87		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77	83		dB
THD	Total harmonic distortion	f_{IN} = 1 kHz		–87	–78	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	78	87		dB
REFERENCE OUTPUT						
V_{REF}	Reference output voltage	Initial, at 25°C, no load	2.495	2.5	2.505	V
TCV_{REF}	Reference output voltage drift		–50	±20	50	ppm/°C
I_{REF}	Reference output current	C_{LOAD} < 1 nF	–5		5	mA
	Load regulation	Load to GND or VDD, 0mA to 5mA		0.15	0.35	mV/mA
I_{SC}	Short-circuit current	REFOUT to GND		23		mA
		REFOUT to VDD		–21		
PSRR	Power-supply rejection ratio		–200	±30	200	µV/V
DIGITAL INPUT/OUTPUT						
I_{IN}	Input current	GND ≤ V_{IN} ≤ VDD			35	µA
C_{IN}	Input capacitance			3		pF
V_{IH}	High-level input voltage		0.7 x VDD		VDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 x VDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 21 MHz		15	30	pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	VDD – 0.1			V
		I_{OH} = –4 mA	VDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
I_{VDD}	Supply current	3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		5.2	6.8	mA
		3.0 V ≤ VDD ≤ 3.6 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF		4.6	6.1	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 0, C_{LOAD} = 15 pF		6.4	8.3	
		4.5 V ≤ VDD ≤ 5.5 V, I_{REFOUT} = 0 mA, MCE = 1, C_{LOAD} = 15 pF		5.4	7.2	

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6.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLK}	CLKIN clock frequency	MCE = 0	9	20	21	MHz
		MCE = 1	9	10	11	
$Duty_{Cycle}$	CLKIN duty cycle		40%	50%	60%	
t_{H1}	DOUT hold time after rising edge of CLKIN	MCE = 0, C_{LOAD} = 15 pF	6			ns
t_{H2}	DOUT hold time after rising edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	6		23	ns
t_{H3}	DOUT hold time after falling edge of CLKIN	MCE = 1, C_{LOAD} = 15 pF	10		26	ns
t_{D1}	Rising edge of CLKIN to DOUT valid delay	MCE = 0, C_{LOAD} = 15 pF			25	ns
t_{D2}	Rising edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	11		27	ns
t_{D3}	Falling edge of CLKIN to DOUT valid delay	MCE = 1, C_{LOAD} = 15 pF	15		30	ns
t_r	DOUT rise time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.5	3.5	
t_f	DOUT fall time	10% to 90%, 3.0 V ≤ VDD ≤ 3.6 V, C_{LOAD} = 15 pF		2.5	5.8	ns
		10% to 90%, 4.5 V ≤ VDD ≤ 5.5 V,C_{LOAD} = 15 pF		1.8	4.4	
t_{ASTART}	Analog startup time	VDD step to 3.0 V; 0.1%-settling, clock applied		0.25		ms

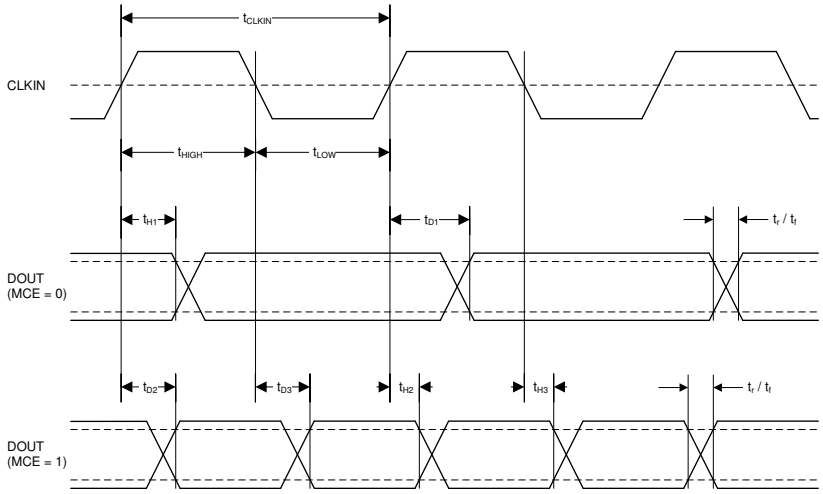


図 1. Digital Interface Timing

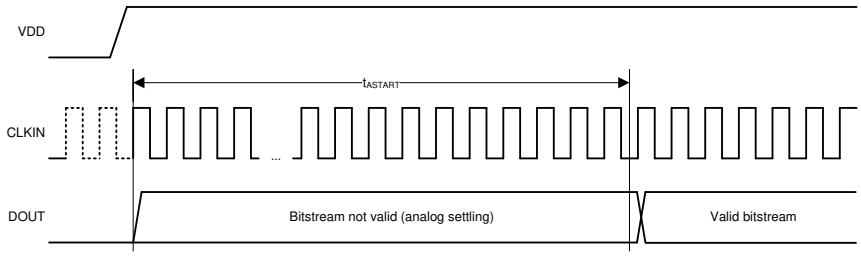


図 2. Device Startup Timing

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6.7 Typical Characteristics

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

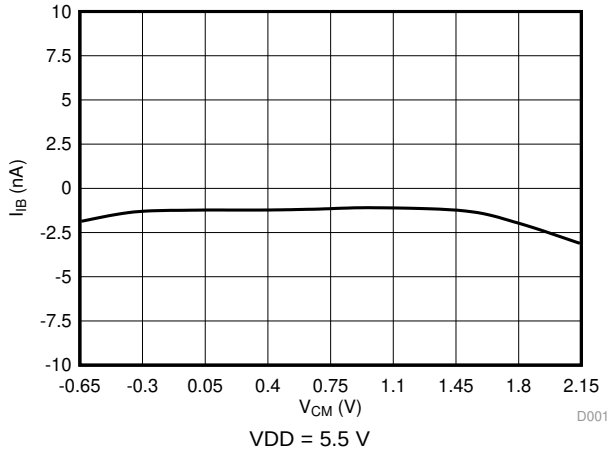


図 3. Input Bias Current vs Common-Mode Input Voltage

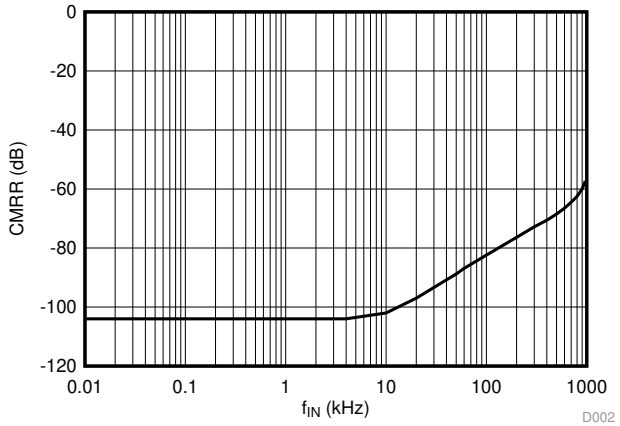


図 4. Common-Mode Rejection Ratio vs Input Signal Frequency

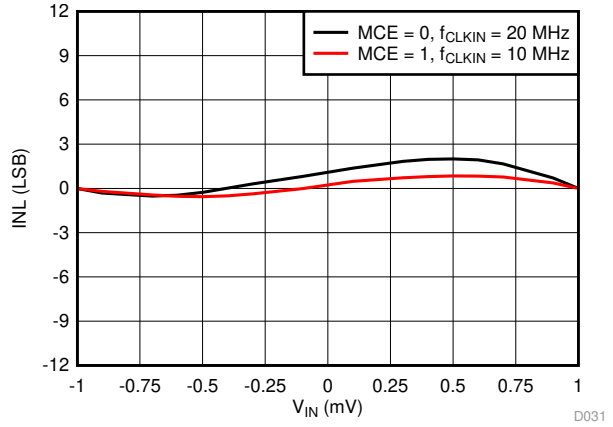


図 5. Integral Nonlinearity vs Input Voltage

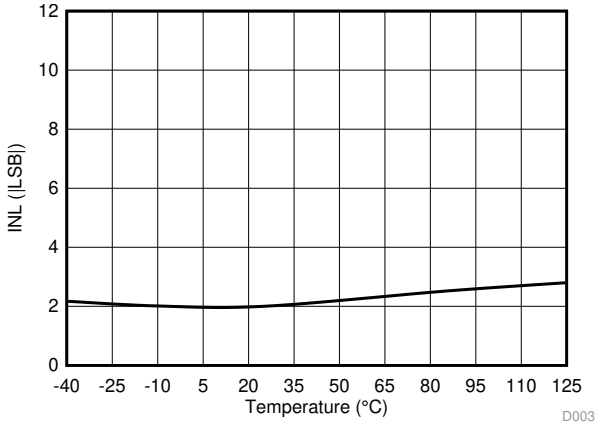


図 6. Integral Nonlinearity vs Temperature

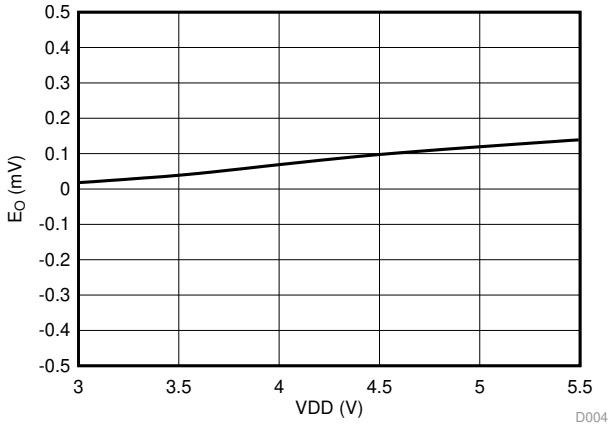


図 7. Offset Error vs Supply Voltage

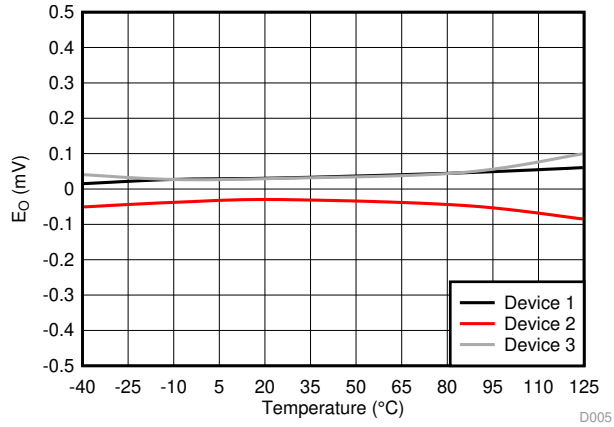


図 8. Offset Error vs Temperature

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Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

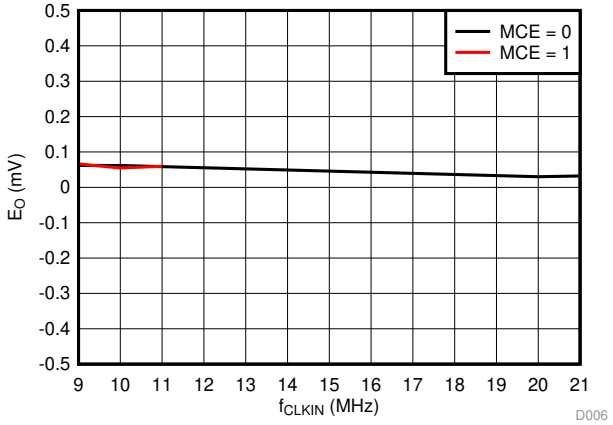


図 9. Offset Error vs Clock Frequency

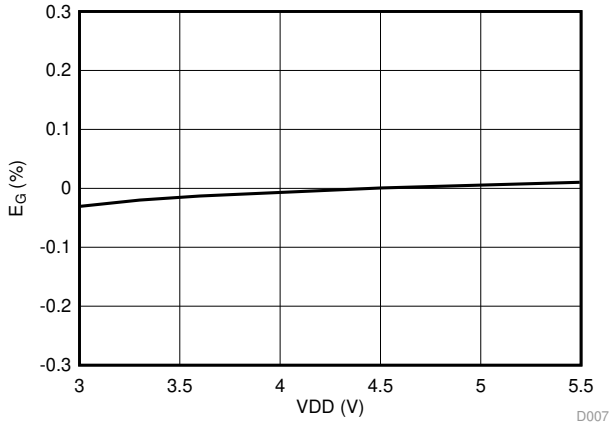


図 10. Gain Error vs Supply Voltage

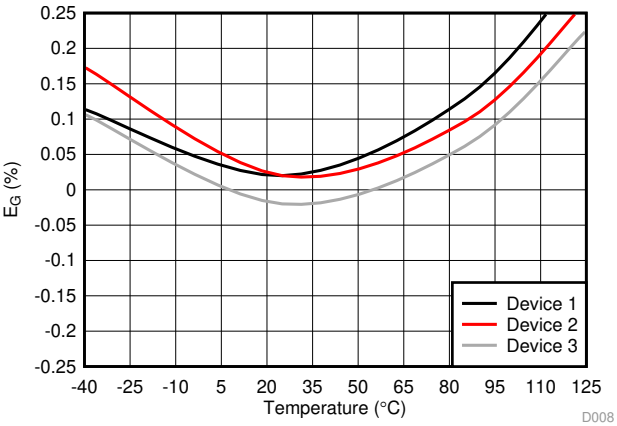


図 11. Gain Error vs Temperature

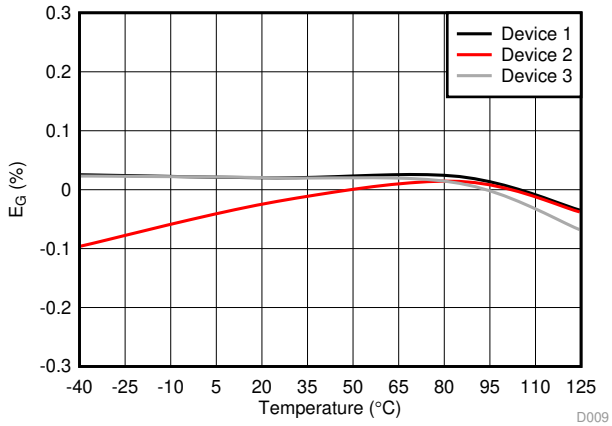


図 12. Ratiometric Gain Error vs Temperature

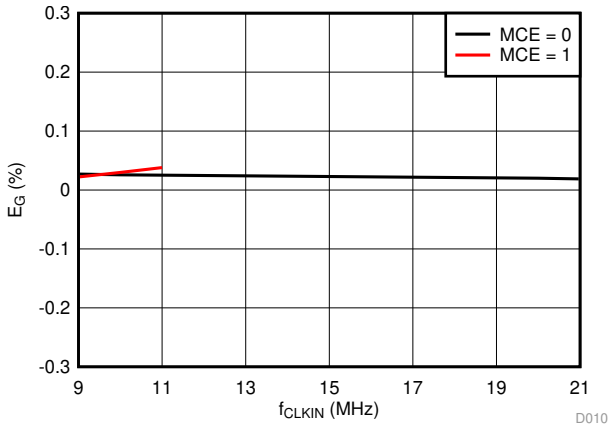


図 13. Gain Error vs Clock Frequency

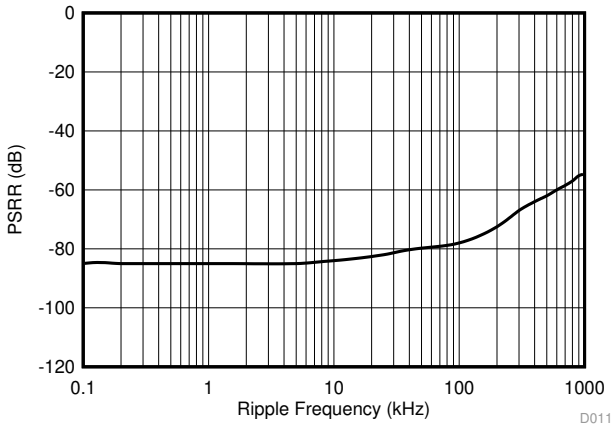


図 14. Power-Supply Rejection Ratio vs Ripple Frequency

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Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

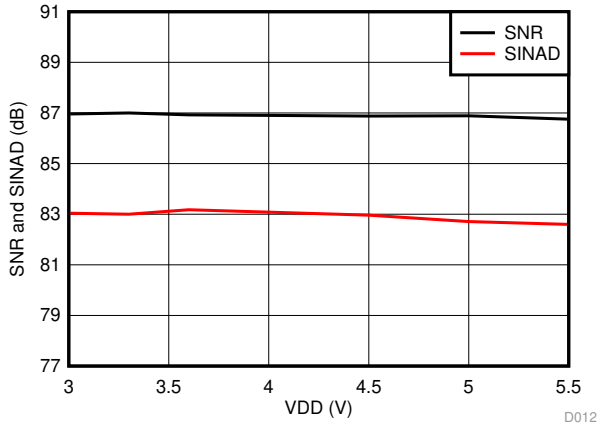


図 15. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage

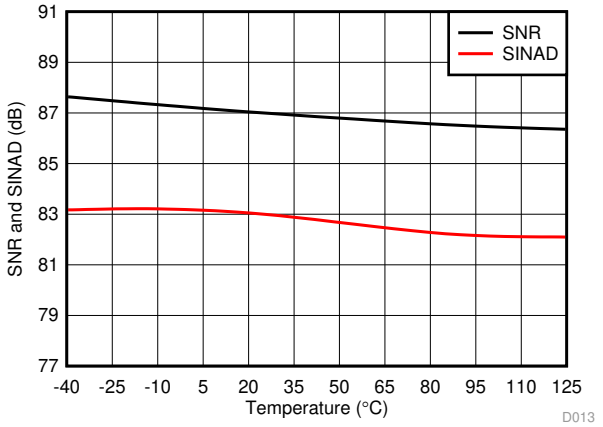


図 16. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

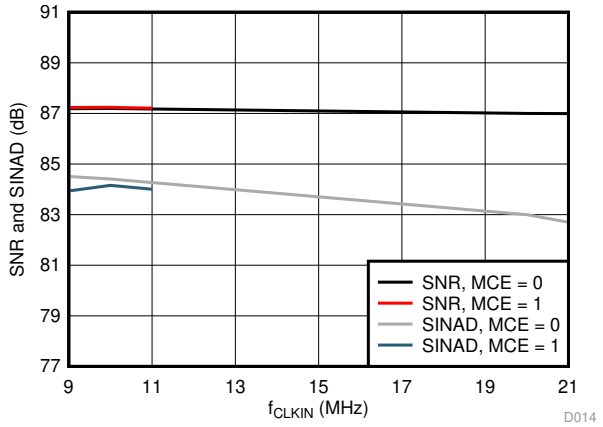


図 17. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

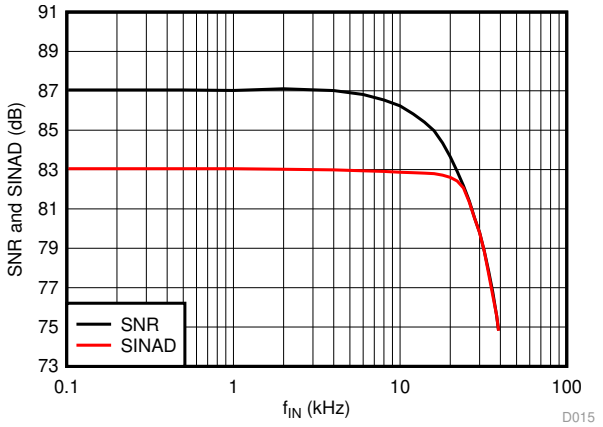


図 18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

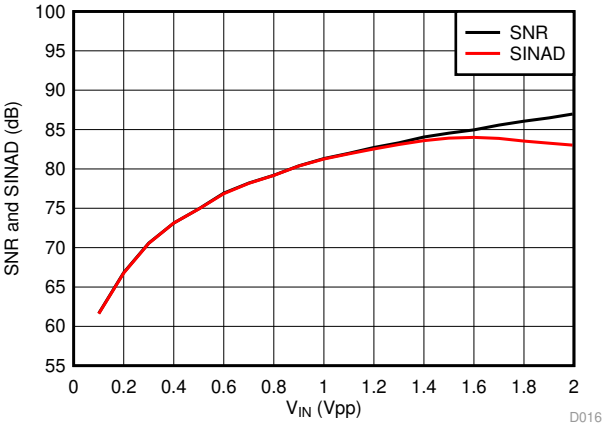


図 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Voltage

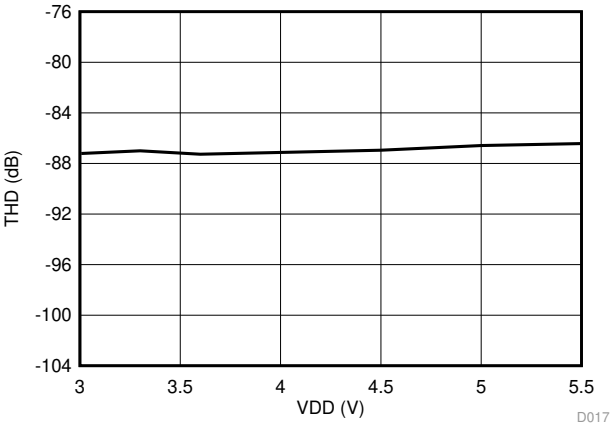


図 20. Total Harmonic Distortion vs Supply Voltage

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Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

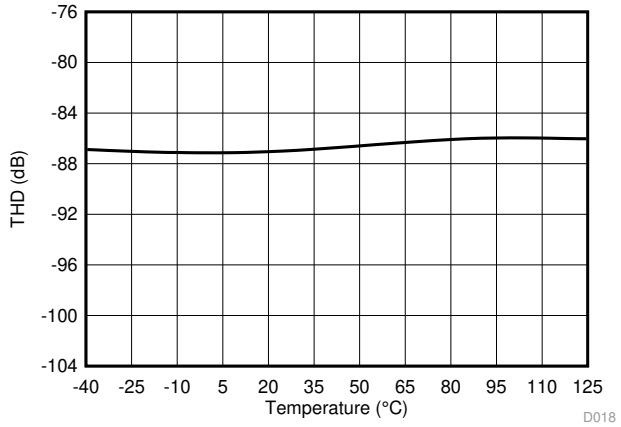


図 21. Total Harmonic Distortion vs Temperature

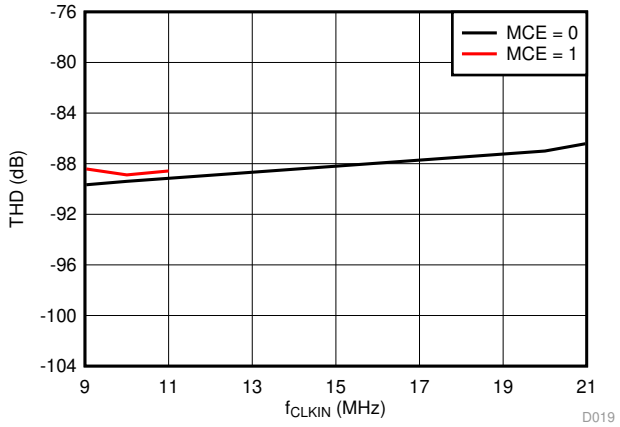


図 22. Total Harmonic Distortion vs Clock Frequency

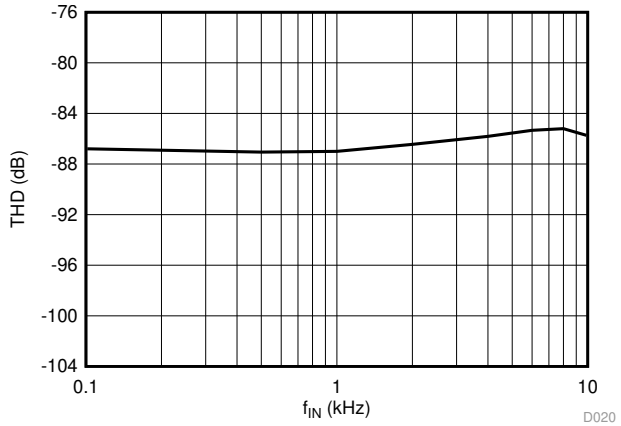


図 23. Total Harmonic Distortion vs Input Signal Frequency

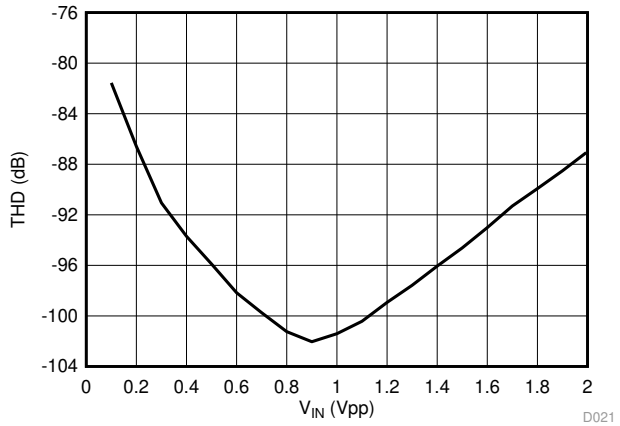


図 24. Total Harmonic Distortion vs Input Signal Voltage

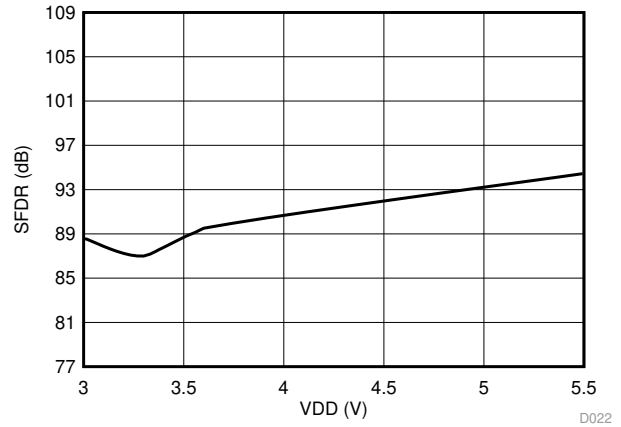


図 25. Spurious-Free Dynamic Range vs Supply Voltage

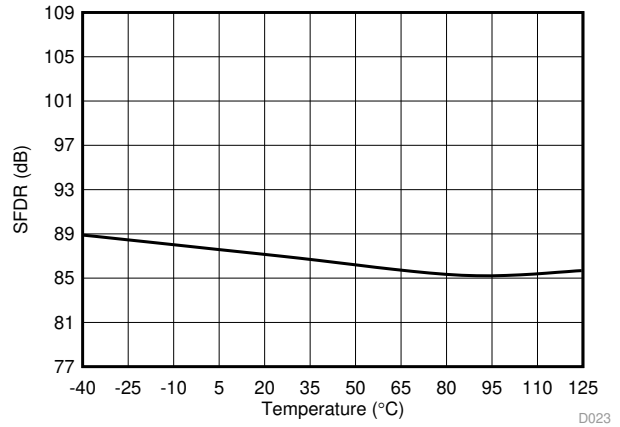


図 26. Spurious-Free Dynamic Range vs Temperature

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Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and sinc^3 filter with OSR = 256 (unless otherwise noted)

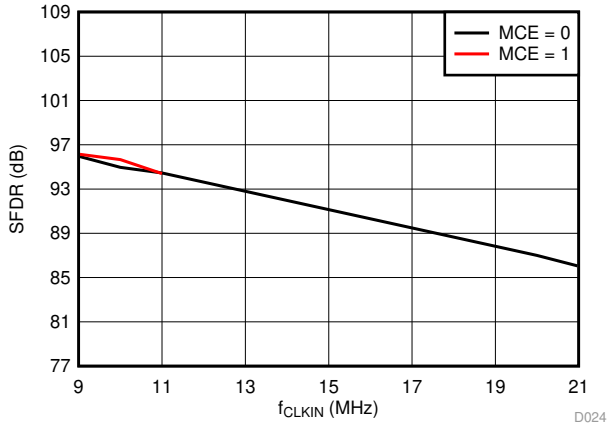


図 27. Spurious-Free Dynamic Range vs Clock Frequency

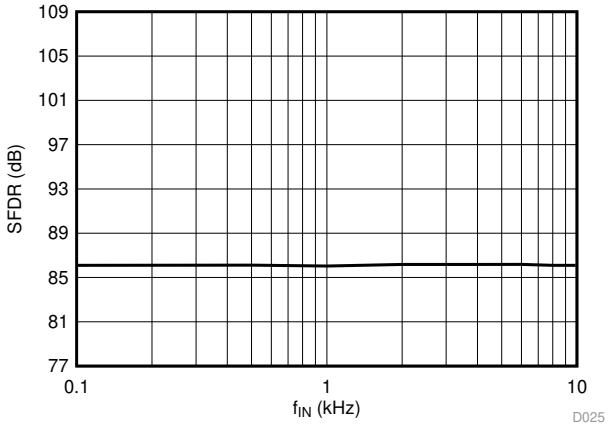


図 28. Spurious-Free Dynamic Range vs Input Signal Frequency

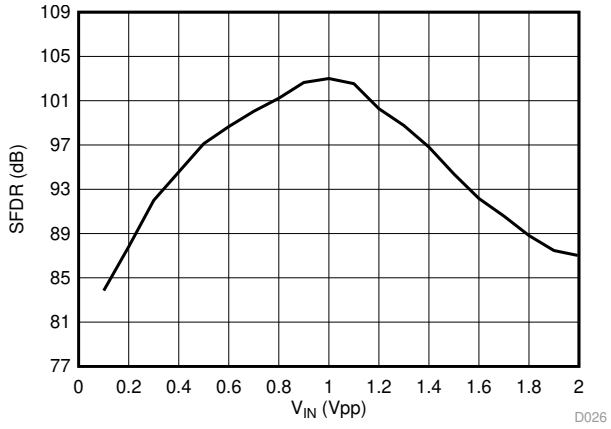
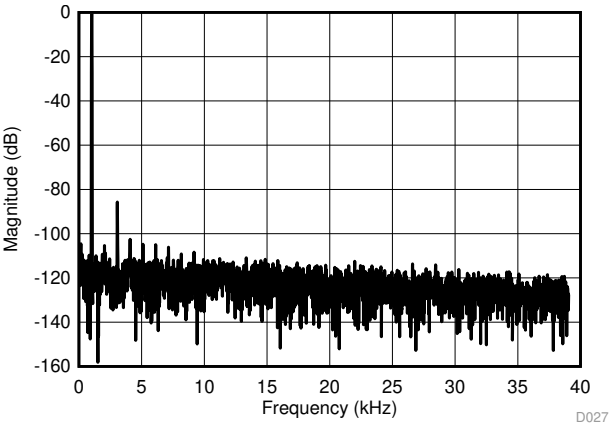
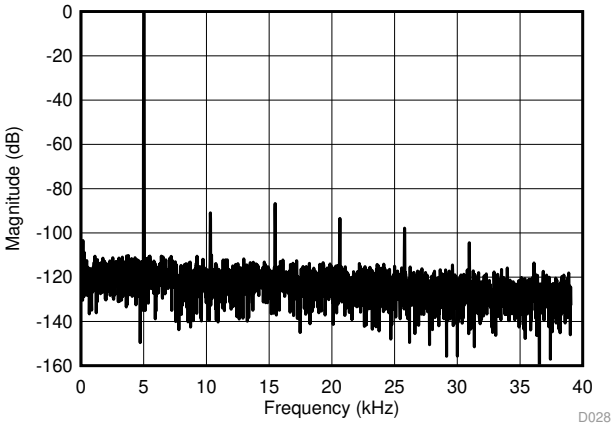


図 29. Spurious-Free Dynamic Range vs Input Signal Voltage



4096-point FFT, V_{IN} = 2 V_{PP}

図 30. Frequency Spectrum With 1-kHz Input Signal



4096-point FFT, V_{IN} = 2 V_{PP}

図 31. Frequency Spectrum With 5-kHz Input Signal

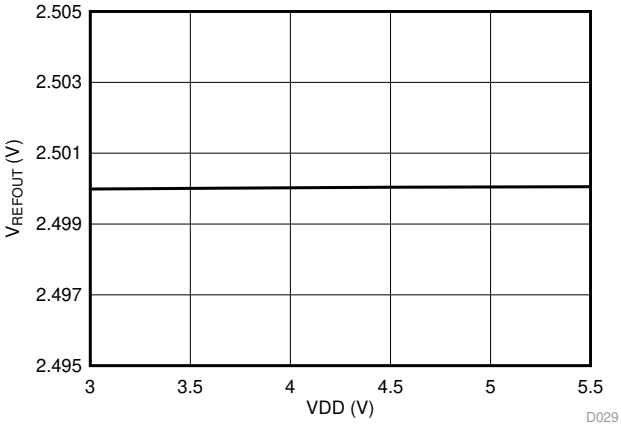


図 32. Reference Output Voltage vs Supply Voltage

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Typical Characteristics (continued)

at VDD = 3.3 V, AINP = –1 V to 1 V, AINN = GND, f_{CLKIN} = 20 MHz, MCE = 0, and $sinc^3$ filter with OSR = 256 (unless otherwise noted)

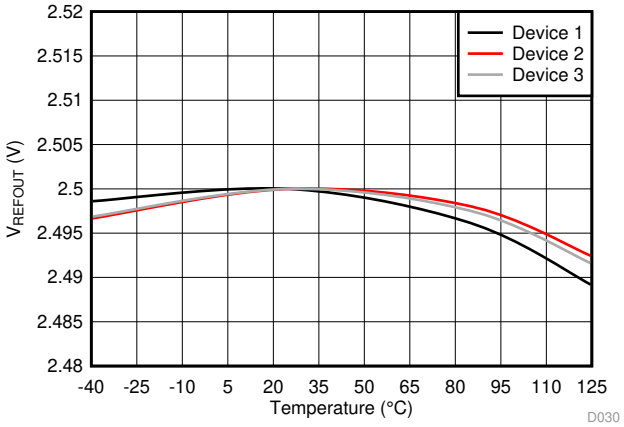


図 33. Reference Output Voltage vs Temperature

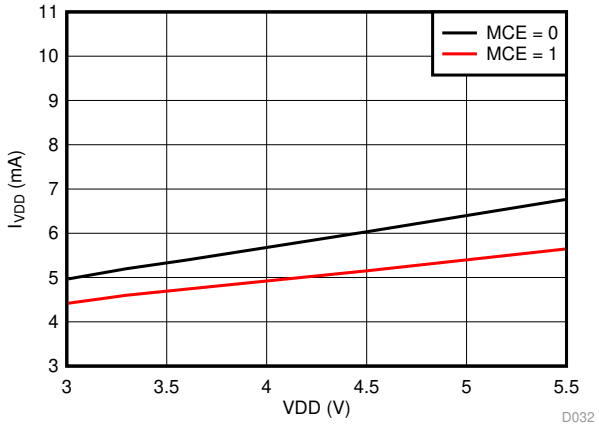


図 34. Supply Current vs Supply Voltage

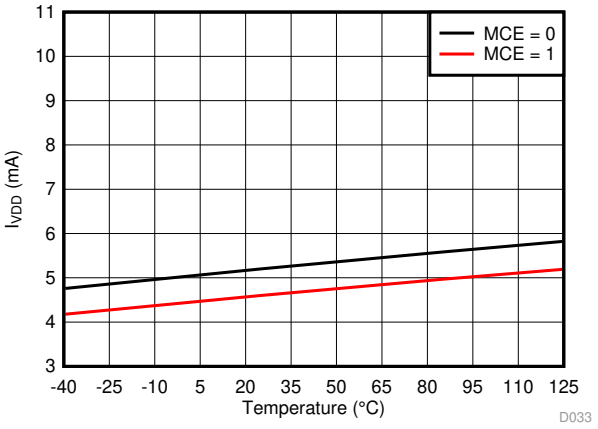


図 35. Supply Current vs Temperature

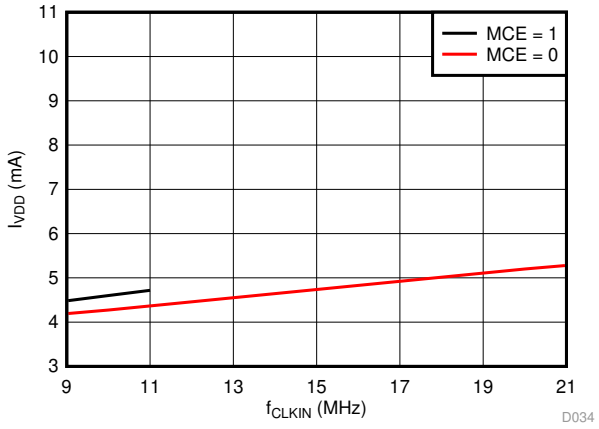


図 36. Supply Current vs Clock Frequency

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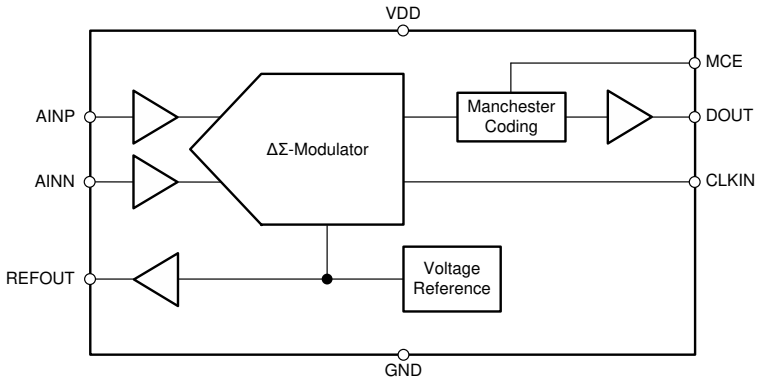
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1035-Q1 is a chopper-stabilized buffer, followed by the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 9 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1035-Q1. The 1.6-GΩ differential input resistance of the analog input stage supports low gain-error signal sensing in high-voltage applications using resistive dividers. The external clock input simplifies the synchronization of multiple measurement channels on the system level. The extended frequency range of up to 21 MHz supports higher performance levels compared to the other solutions available on the market.

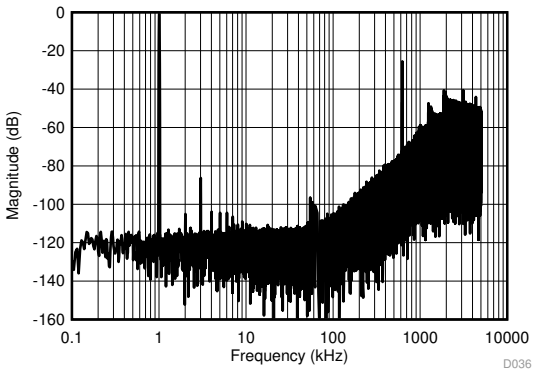
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1035-Q1 incorporates front-end circuitry that contains a buffered sampling stage, followed by a ΔΣ modulator. To support a bipolar input range, the device uses a charge pump that allows single-supply operation to simplify the overall system design and minimize the circuit cost. For reduced offset and offset drift, the input buffer is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. 図 37 shows the spur created by the switching frequency.



$sinc^3$ filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

図 37. Quantization Noise Shaping

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Feature Description (continued)

The linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±1 V, and within the specified input common-mode range.

図 38 shows the specified common-mode input voltage that applies for the full-scale input voltage range as specified in this document along with the corresponding common-mode undervoltage and overvoltage threshold levels.

If smaller input signals are used, the operational common-mode input voltage range widens. 図 39 shows the common-mode input voltage that applies with no differential input signal; that is, when the voltage applied on AINP is equal to the voltage applied on AINN. The common-mode input voltage range scales with the actual differential input voltage between this range and the range in 図 38.

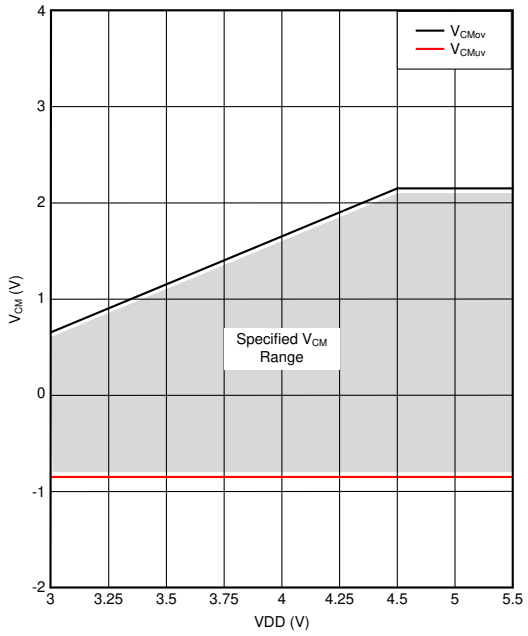


図 38. Common-Mode Input Voltage Range With a Full-Scale Differential Input Signal of ±1.25 V

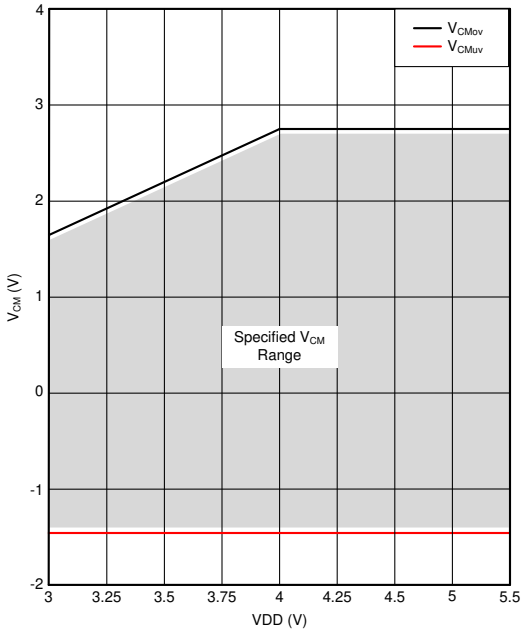


図 39. Common-Mode Input Voltage Range With a Zero Differential Input Signal

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Feature Description (continued)

7.3.2 Modulator

The modulator implemented in the AMC1035-Q1 (such as the one conceptualized in 図 40) is a second-order, switched-capacitor, feed-forward ΔΣ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

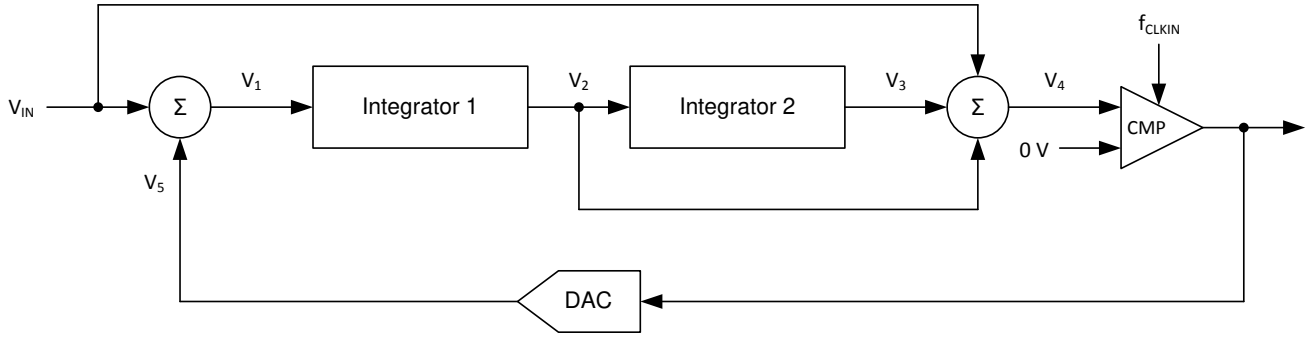


図 40. Block Diagram of a Second-Order Modulator

As depicted in 図 37, the modulator shifts the quantization noise to high frequencies. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F28004x, TMS320F2807x, and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1035-Q1. Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

7.3.3 Reference Output

The AMC1035-Q1 offers a voltage reference output that can source or sink current to significantly reduce the gain error thermal drift in ratiometric applications as specified in the *Electrical Characteristics* table. The *IGBT Temperature Sensing* section provides an example of a ratiometric use case for the AMC1035-Q1.

The reference output can drive capacitive loads less than 1 nF. Use a series resistor to avoid oscillations and degradation of performance for capacitive loads ≥ 1 nF. 表 1 lists the recommended series resistor values for given capacitor value examples. Interpolate for capacitive loads with a value between the given examples.

表 1. Series Resistor Value for Capacitive Loads ≥ 1 nF on the REFOUT Pin

CAPACITIVE LOAD ON THE REFOUT PIN	RECOMMENDED SERIES RESISTOR
1 nF	33 Ω
3.3 nF	56 Ω
10 nF	47 Ω
33 nF	33 Ω
100 nF	15 Ω
330 nF	10 Ω
1 µF	5.6 Ω
3.3 µF	3.3 Ω
10 µF	1.8 Ω

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7.3.4 Clock Input

The AMC1035-Q1 system clock is provided externally at the CLKIN pin. The clock signal must be applied continuously for proper device operation.

To support the bipolar input voltage range with a single supply, the AMC1035-Q1 includes a charge pump. This charge pump stops operating if the clock signal is below the specified frequency range or if the signal is paused or missing. Additionally, the input bias current increases beyond the specified range and significantly reduces the input resistance of the device. When the clock signal is paused or missing, the modulator stops the analog signal conversion and the digital output signal remains frozen in the last logic state. When the clock signal is applied again after a pause, the internal analog circuitry biasing must settle for proper device performance. In this case, consider the t_{ASTART} specification in the *Switching Characteristics* table.

7.3.5 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982 (an unsigned code). A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1035-Q1 with performance as specified in this document. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1035-Q1 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). 図 41 shows the input voltage versus the output modulator signal.

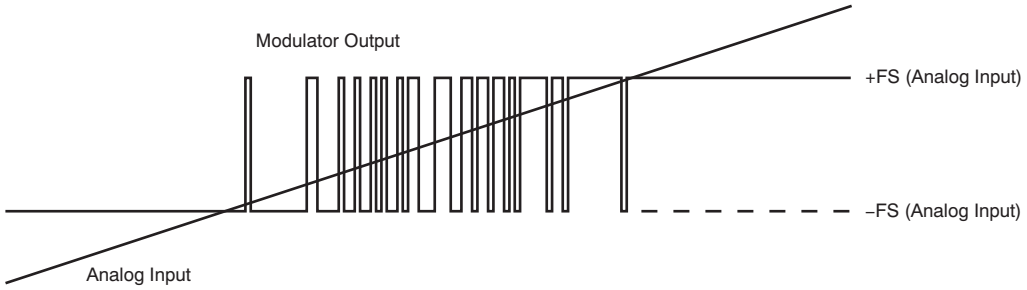


図 41. Analog Input versus the AMC1035-Q1 Modulator Output

式 1 calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section):

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The modulator bitstream on the DOUT pin changes with the rising edge of the clock signal applied on the CLKIN pin. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.

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7.3.6 Manchester Coding Feature

The AMC1035-Q1 offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. The Manchester coding combines the clock and data information using exclusive-OR (XOR) logical operation that results in a bitstream free of DC components. 図 42 shows the resulting bitstream from this coding. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN. To enable Manchester coding on the AMC1035-Q1, pull the input pin MCE high. The DOUT signal is inverted if the MCE status changes when CLKIN is high.

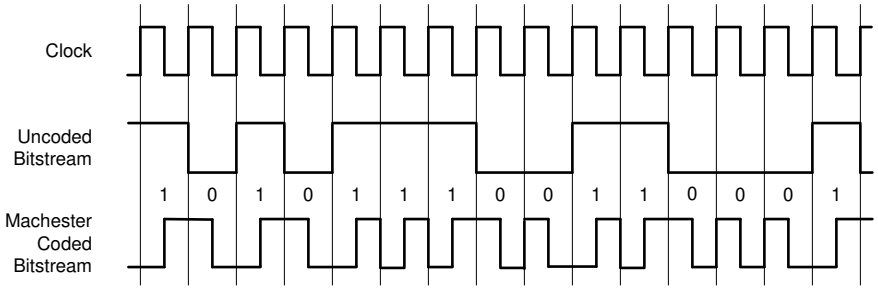


図 42. Manchester Coded Output of the AMC1035-Q1

7.4 Device Functional Modes

The AMC1035-Q1 is operational when the power supply VDD and clock signal CLKIN are applied, as specified in the *Recommended Operating Conditions* and *Switching Characteristics* tables.

7.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1035-Q1 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in 図 43, depending on the actual polarity of the signal being sensed. This feature is also supported with a Manchester coded output and allows full-scale and invalid input signals to be identified as described in the *Fail-Safe Output* section and can be used for advanced system-level diagnostics.

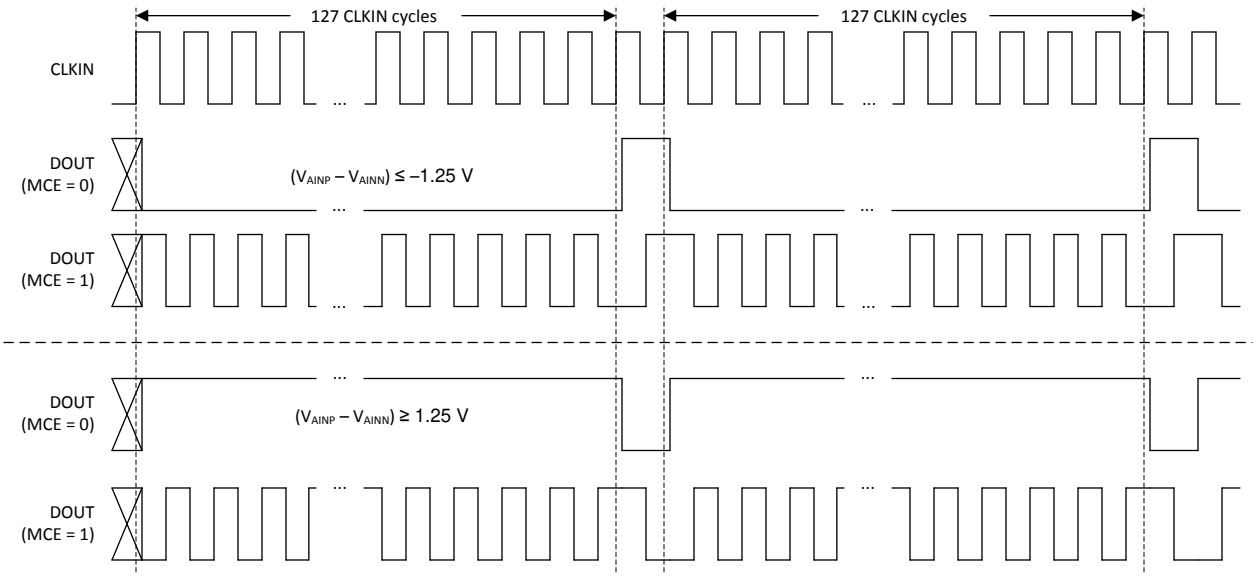


図 43. Overrange Output of the AMC1035-Q1

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Device Functional Modes (continued)

7.4.2 Fail-Safe Output

図 44 shows that if the common-mode voltage of the input reaches or exceeds the specified common-mode undervoltage, V_{CMuv}, or overvoltage detection level, V_{CMov} as defined in the *Electrical Characteristics* table, the DOUT of the AMC1035-Q1 is held at steady-state high.

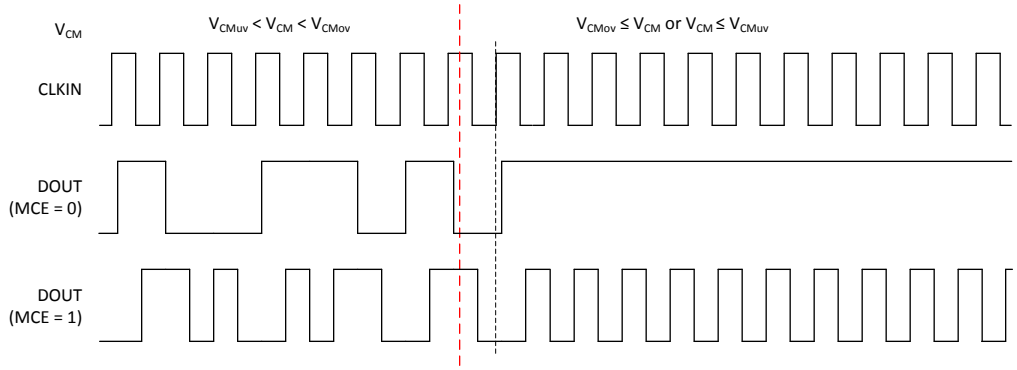


図 44. Fail-Safe Output of the AMC1035-Q1

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). 式 2 shows a $sinc^3$-type filter, which is a very simple filter, built with minimal effort and hardware:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \tag{2}$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a $sinc^3$ filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a $sinc^3$ filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

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8.2 Typical Applications

8.2.1 Voltage Sensing

ΔΣ modulators are widely used in high-efficiency systems because of their high AC and DC performance. In automotive applications, the AMC1035-Q1 can be used in traction inverters, on-board chargers, DC/DC converters, and as parts of integrated power modules.

図 45 shows a simplified schematic of a traction inverter application with the AMC1035-Q1 used for the DC-link and output phase voltage sensing. In this example, all resistive dividers reference to the negative DC-link voltage that is also used as a ground reference point for the microcontroller. An additional fifth AMC1035-Q1 can be used for temperature sensing of the insulated-gate bipolar transistor (IGBT) module; see the *IGBT Temperature Sensing* section for more details.

Current feedback is performed with shunt resistors (R_{SHUNT}) and TI's AMC1305M25-Q1 isolated modulators. Depending on the system design, either all three or only two motor phase currents are sensed.

Depending on the overall digital processing power requirements, and with a total of eight ΔΣ modulator bitstreams to be processed by the MCU, a derivate from either the low-cost single-core TMS320F2807x or the dual-core TMS320F2837x families can be used in this application.

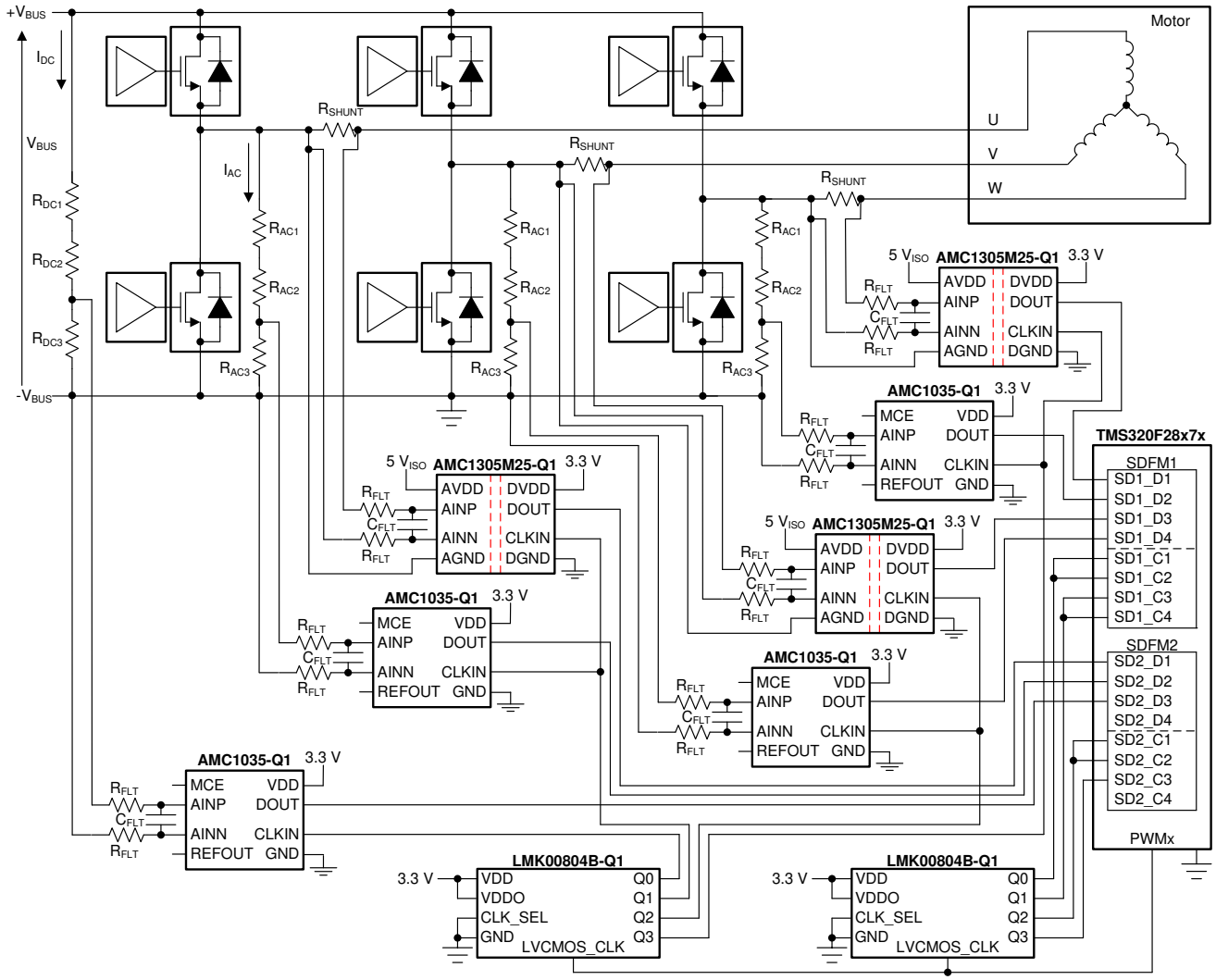


図 45. The AMC1035-Q1 in a Traction Inverter Application

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Typical Applications (continued)

8.2.1.1 Design Requirements

表 2 lists the parameters for this typical application.

表 2. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Voltage drop across the sensing resistor R_{DC1} for a linear response	1 V (maximum)
Voltage drop across the sensing resistors R_{ACx} for a linear response	±1 V (maximum)
Current through the sensing resistors R_{ACx}	±100 µV (maximum)

8.2.1.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive dividers to limit the cross current to the desired values:

- For the voltage sensing on the DC bus: $R_{DC1} + R_{DC2} + R_{DC3} = V_{BUS} / I_{DC}$
- For the voltage sensing on the output phases U, V, and W: $R_{AC1} + R_{AC2} + R_{AC3} = V_{PHASE\ (max)} / I_{AC}$

Consider the following two restrictions to choose the proper value of the resistors R_{DC3} and R_{AC3}:

- The voltage drop caused by the nominal voltage range of the system must not exceed the recommended input voltage range of the AMC1035-Q1: $V_{xC3} \leq V_{FSR}$
- The voltage drop caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{xC3} \leq V_{Clipping}$

Use similar approach for calculation of the shunt resistor values R_{SHUNT} and see the AMC1305M25-Q1 data sheet for further details.

表 3 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the DC bus.

表 3. Resistor Value Examples for DC Bus Sensing

PARAMETER	600-V DC BUS	800-V DC BUS
Resistive divider resistor R_{DC1}	3.01 MΩ	4.22 MΩ
Resistive divider resistor R_{DC2}	3.01 MΩ	4.22 MΩ
Sense resistor R_{DC3}	10 kΩ	10.5 kΩ
Resulting current through resistive divider I_{DC}	99.5 µA	94.7 µA
Resulting voltage drop on sense resistor V_{RDC3}	0.995 V	0.994 V

表 4 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 400 V and 690 V on the output phases.

表 4. Resistor Value Examples for Output Phase Voltage Sensing

PARAMETER	±400-V_{AC} PHASE	±690-V_{AC} PHASE
Resistive divider resistor R_{AC1}	2.0 MΩ	3.48 MΩ
Resistive divider resistor R_{AC2}	2.0 MΩ	3.48 MΩ
Sense resistor R_{AC3}	10.0 kΩ	10.0 kΩ
Resulting current through resistive divider I_{AC}	99.8 µA	99.0 µA
Resulting voltage drop on sense resistor V_{RAC3}	±0.998 V	±0.990 V

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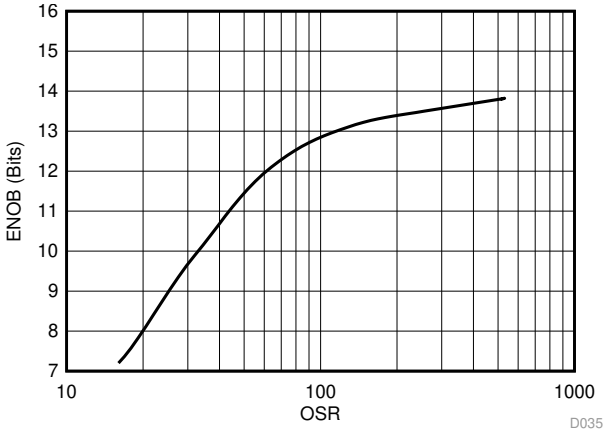
Use a power supply with a nominal voltage of 3.3 V to directly connect all modulators to the microcontroller.

For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These MCU families support up to eight channels of dedicated hardwired filter structures called *sigma-delta filter modules (SDFMs)* that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one that offers a fast response path for overcurrent detection. Use one of the pulse-width modulation (PWM) sources inside the MCU to generate the clock for the modulators and for easy synchronization of all feedback signals and the switching control of the gate drivers.

図 45 uses a clock buffer to distribute the clock reference signal generated on one of the PWM outputs of the MCU (called PWMx in 図 45) to all modulators used in the circuit and as a reference for the digital filters in the MCU. In this example, TI's LMK00804B-Q1 is used for this purpose. Each LMK00804B-Q1 output can drive two modulator or two SDFM clock inputs.

8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. 図 46 shows the ENOB of the AMC1035-Q1 with different oversampling ratios on a sinc3 filter. This number is calculated from the SINAD by using following equation: SINAD = 1.76 dB + 6.02 × ENOB.



sinc3 filter

図 46. Measured Effective Number of Bits vs Oversampling Ratio

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8.2.2 IGBT Temperature Sensing

The high input impedance of the AMC1035-Q1 is optimized for usage in voltage-sensing applications. Additionally, the internal voltage reference supports temperature sensing using a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) sensor often integrated in the IGBT module.

The same reference is internally used by the modulator, resulting in a ratiometric system solution that minimizes the overall temperature drift of the sensing path. 図 47 shows a simplified schematic of the AMC1035-Q1 used for temperature sensing of the IGBT module. See the *Application Example* on the front page of this document for an application solution that requires isolating the temperature sensor.

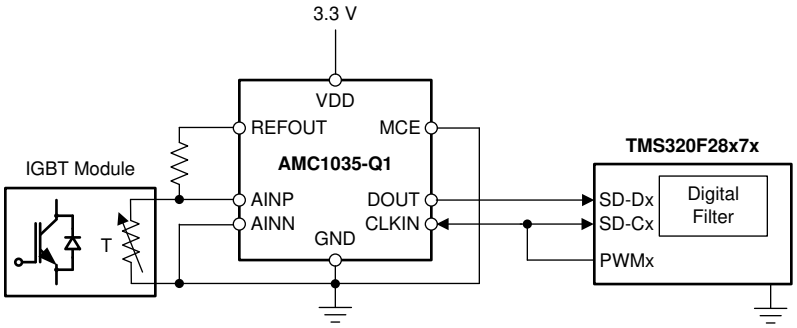


図 47. Using the AMC1035-Q1 for Temperature Sensing

8.2.3 What to Do and What Not to Do

Do not leave the analog inputs of the AMC1035-Q1 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current can drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes. In both cases, the modulator outputs a fail-safe bitstream as described in the *Fail-Safe Output* section.

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9 Power Supply Recommendations

To decouple the power supply, place a 0.1-µF capacitor as close to the VDD pin of the AMC1035-Q1 as possible, as shown in 図 48, followed by an additional capacitor in the range of 1 µF to 10 µF.

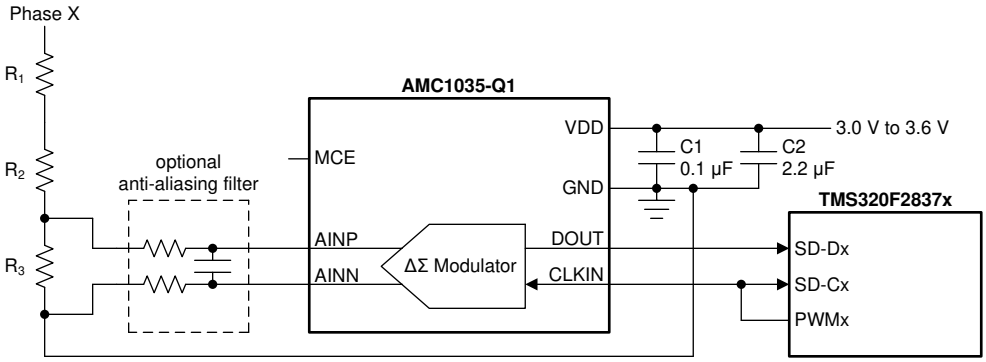


図 48. Decoupling the AMC1035-Q1

Safety considerations or high common-mode voltage levels can require the AMC1035-Q1 to be galvanically isolated from other parts of the system. 図 49 shows an example of a circuit that uses the ISO7721-Q1 to isolate the signal path and the SN6501-Q1 and a transformer are used to generate the required isolated power.

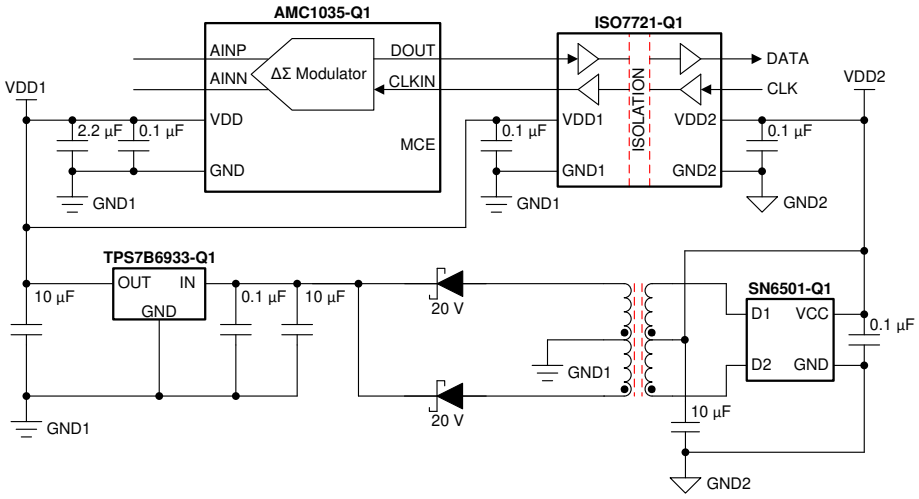


図 49. Galvanic Isolation of the AMC1035-Q1

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10 Layout

10.1 Layout Guidelines

図 50 shows two layout recommendations for designs based on 1206-SMD or 0603-SMD size decoupling capacitors placed as close as possible to the AMC1035-Q1. For best performance, place the AMC1035-Q1 as close as possible to the source of the analog signal to be converted and keep the layout of the AINP and AINN traces symmetrical.

10.2 Layout Example

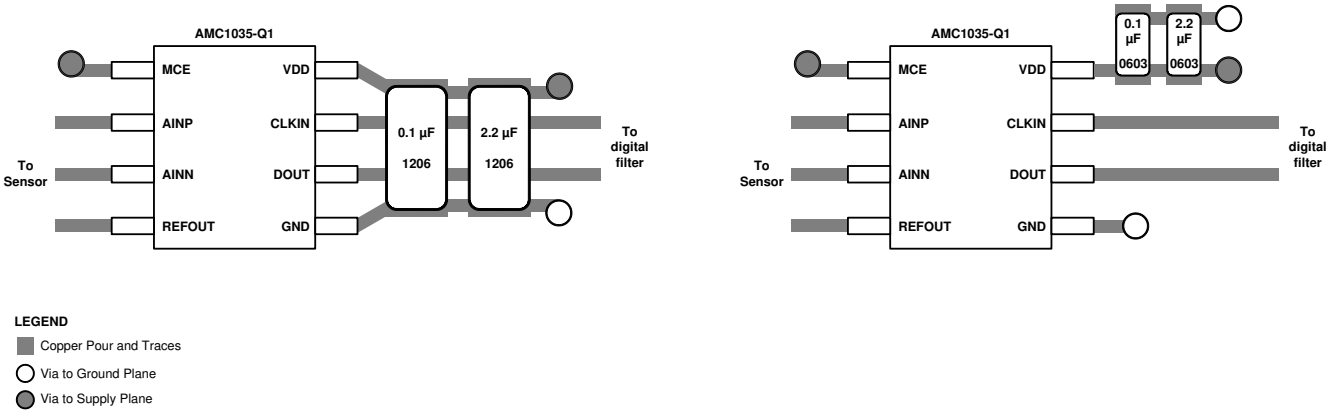


図 50. Recommended Layout of the AMC1035-Q1

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『TMS320F28004x Piccolo™ マイクロコントローラ』データシート*
- テキサス・インスツルメンツ、*『TMS320F2807x Piccolo™ マイクロコントローラ』データシート*
- テキサス・インスツルメンツ、*『TMS320F2837xD デュアル・コアDelfino™ マイクロコントローラ』データシート*
- テキサス・インスツルメンツ、*『ISO772x-Q1 高速、堅牢なEMC強化型 2 チャネル・デジタル・アイソレータ』データシート*
- テキサス・インスツルメンツ、*『ADS1202とFPGAデジタル・フィルタとの組み合わせによるモータ制御アプリケーションでの電流測定』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『AMC1305x-Q1 高精度、強化絶縁のデルタ・シグマ変調器』データシート*
- テキサス・インスツルメンツ、*『LMK00804B-Q1 1.5V～3.3V、1 入力 4 出力、高性能 LVCMOS ファンア ウト・バッファ / レベル・シフタ』データシート*
- テキサス・インスツルメンツ、*『TPS7B69xx-Q1 高電圧、超低 I_Q、低ドロップアウト・レギュレータ』データシート*
- テキサス・インスツルメンツ、*『SN6501-Q1 絶縁電源用の変圧器ドライバ』データシート*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com　　の本デバイスのプロダクト・フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1035QDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A1035Q
AMC1035QDRQ1.B	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	A1035Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AMC1035-Q1 :

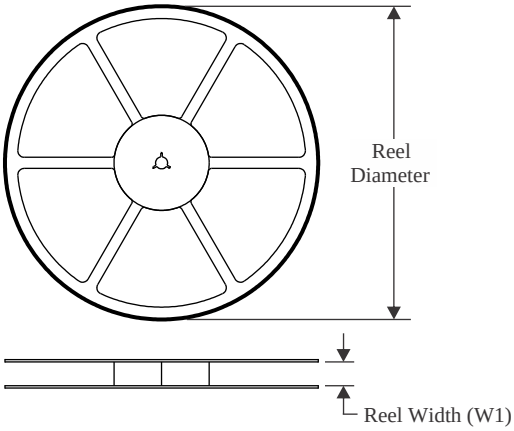
- Catalog : AMC1035

NOTE: Qualified Version Definitions:

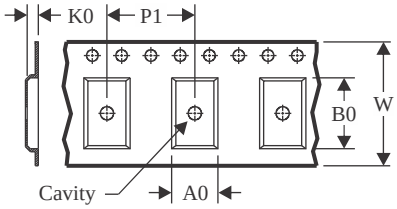
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

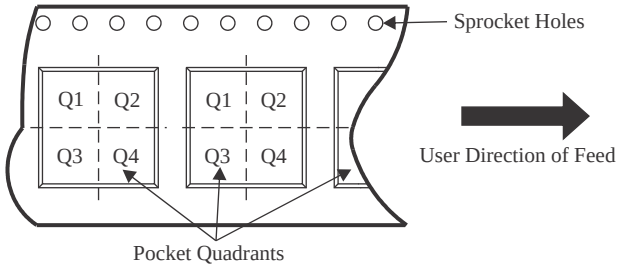


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

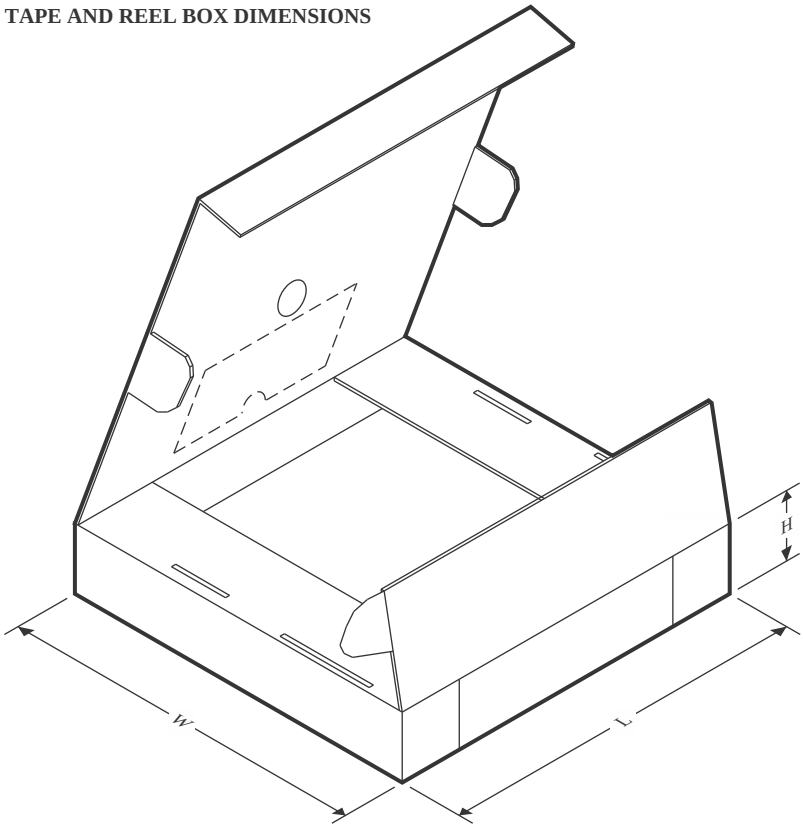
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

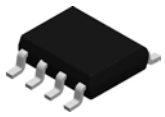
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1035QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1035QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

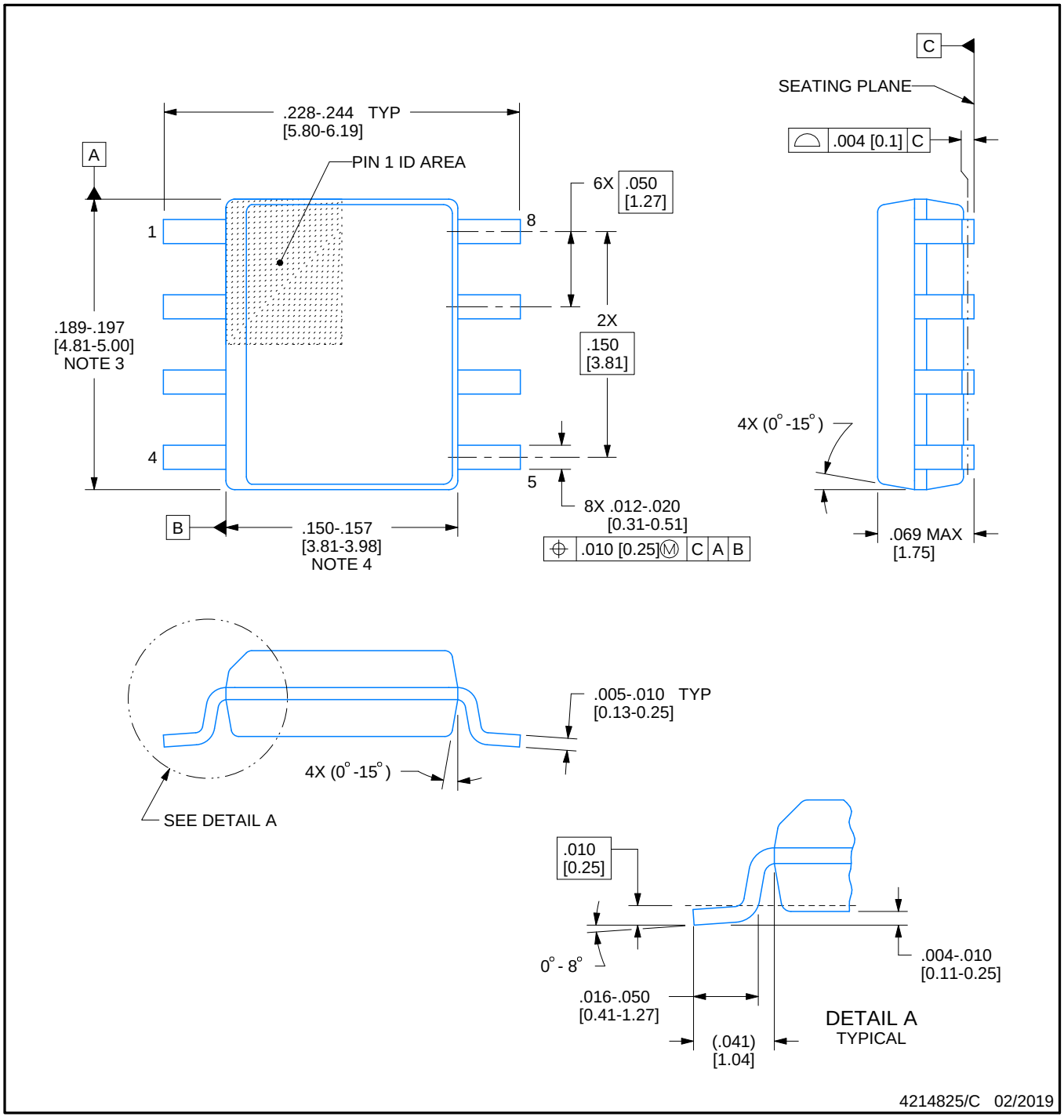


PACKAGE OUTLINE

D0008A

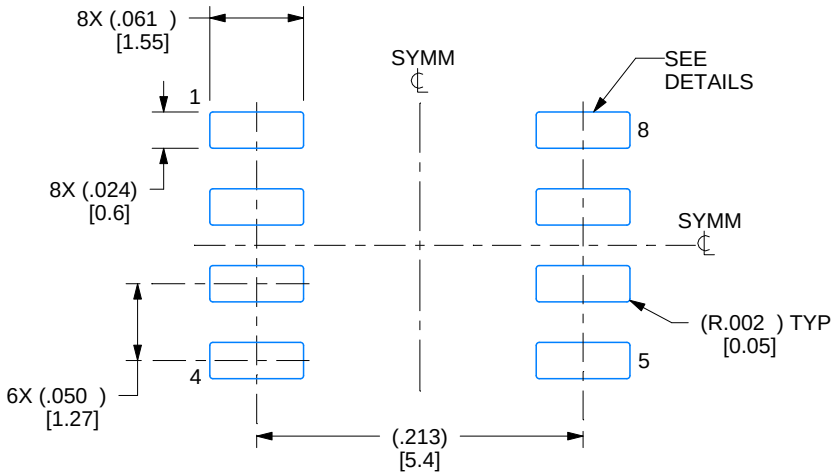
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

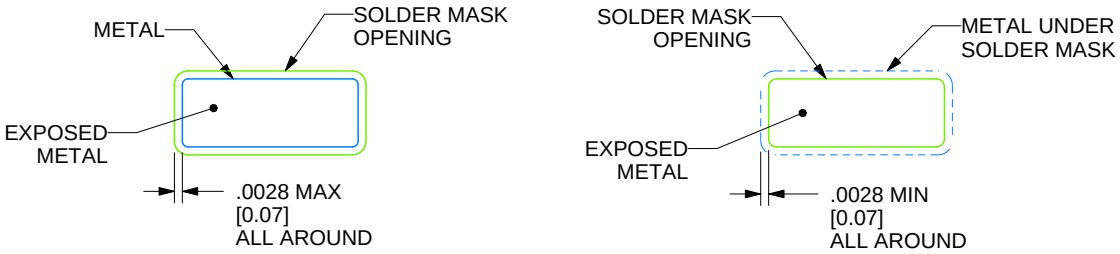


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

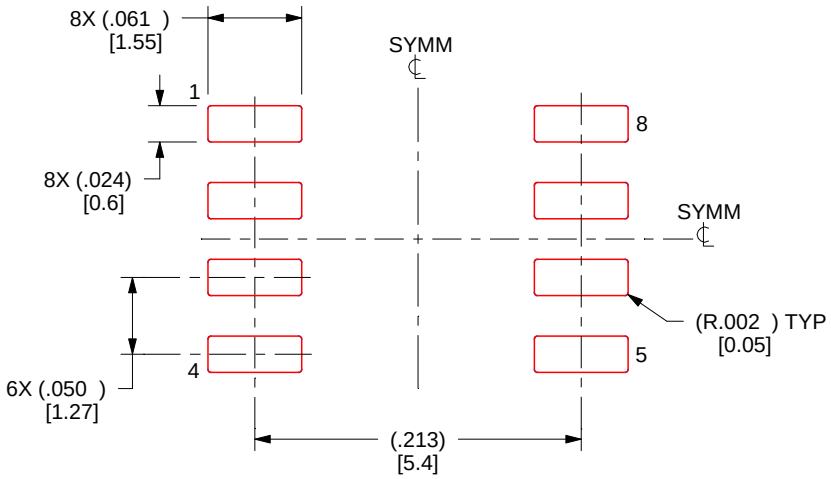
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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