AMC1300 高精度、±250mV 入力、強化絶縁型アンプ

1 特長

- シャント抵抗を用いた電流測定用に最適化された ±250mV の入力電圧範囲
- 固定ゲイン:8.2
- 小さな DC 誤差
  - AMC1300B:
    - オフセット誤差:±0.2mV (最大値)
    - オフセット・ドリフト:±0.9µV/℃ (最大値)
    - ゲイン誤差:±0.3% (最大値)
    - ゲイン・ドリフト:±30ppm/℃ (最大値)
  - AMC1300:
    - オフセット誤差:±2mV (最大値)
    - オフセット・ドリフト:±4µV/℃ (最大値)
    - ゲイン誤差:±1% (最大値)
    - ゲイン・ドリフト:±50ppm/℃ (標準値)
  - 非線形性:0.03% (最大値)
- ハイサイドの 3.3V 動作 (AMC1300B)
- 高 CMTI:100kV/µs (最小値) (AMC1300B)
- 低 EMI、CISPR-11 および CISPR-25 規格に準拠
- システム・レベル診断機能
- 安全関連の認証:
  - DIN VDE V 0884-11:2017-01 に準拠した強化絶縁耐圧 7071V_{PK}
  - UL 1577 に準拠した絶縁耐圧:5000V_{RMS} (1 分間)

2 アプリケーション

- 次のような機器で使用するシャント抵抗方式電流センシング:
  - モーター・ドライブ
  - 周波数インバータ
  - 無停電電源

3 概要

AMC1300 は高精度の絶縁型アンプで、磁気干渉に対して高い耐性のある絶縁バリアにより、入力側と出力側の回路が分離されています。この絶縁膜は、VDE V 0884-11 および UL1577 に準拠し、5kV_{RMS} までの強化ガルバニック絶縁体に認定されています。この絶縁型アンプを絶縁型電源と組み合わせて使用すると、システムの中で異なる同相電圧レベルで動作する複数のセクションを互いに分離し、低電圧セクションを損傷から保護することができます。

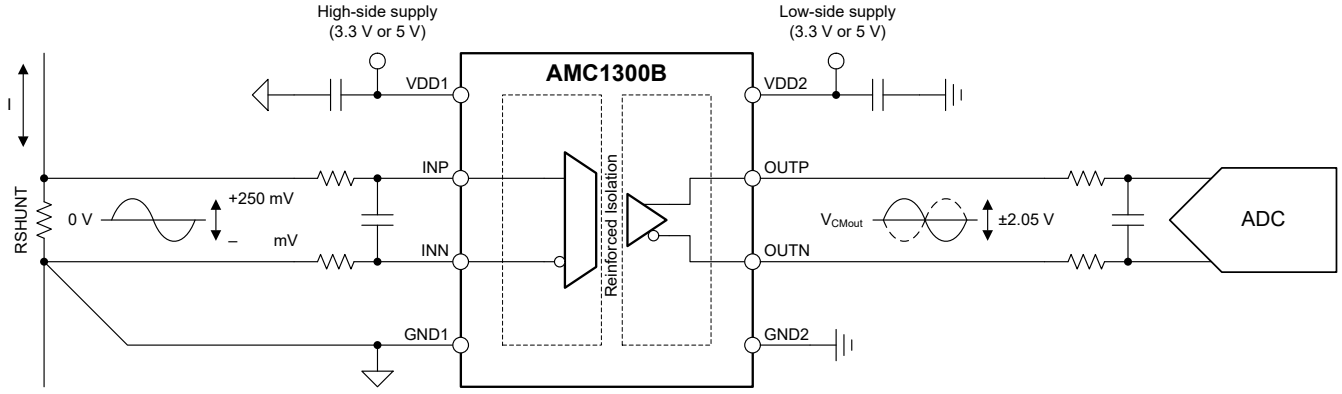
AMC1300 の入力は、シャント抵抗またはその他の低電圧レベルの信号源と直接接続するように最適化されています。デバイスの優れた性能により、電流が正確に制御され、システム・レベルで電力を削減できるほか、特にモータ制御用途でトルクのリップルを低減できます。AMC1300 には、同相モード過電圧およびハイサイド電源電圧喪失検出機能が内蔵されているため、システム・レベルの設計と診断が簡単に行えます。

AMC1300 は 2 つの性能グレード・オプションで供給されます。AMC1300B は拡張産業用温度範囲の -55℃～+125℃で動作が規定されており、AMC1300 は -40℃～+125℃で動作します。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
AMC1300	SOIC (8)	5.85mm × 7.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (June 2021) to Revision D (May 2022)	Page
• Changed CDM ESD standard from JESD22-C101 to ANSI/ESDA/JEDEC JS-002	6
• Changed T_A (max) for AMC1300 from 105 ℃ to 125 ℃.	6
• Updated VDE standard references is *Safety-Related Certifications* table	9

Changes from Revision B (April 2020) to Revision C (June 2021)	Page
• 「特長」セクションを変更	1
• ドキュメント全体を通して複数の図を変更（編集上の変更のみ）	1
• Changed TCV_{OS}, TCE_G, and CMTI values in AMC1300B column of *Device Comparison Table*	4
• Changed C_{IO} from ~1 pF to ~1.5 pF	8
• Changed V_{CMov} hysteresis from 95 mV to 60 mV	10
• Changed TCV_{OS} (AMC1300B) from ±3 to ±0.9 µV/℃ and typical value from ±1 to ±0.1 µV/℃	10
• Changed TCE_G (AMC1300B) from ±50 to ±30 ppm/℃ and typical value from ±15 to ±5 ppm/℃	10
• Changed SNR (min), f_{IN} = 1 kHz from 80 dB to 81.5 dB	10
• Added $V_{CLIPout}$ specification	10
• Changed $V_{FAILSAFE}$ from * / –2.6 V / –2.5 V to –2.63 V / –2.57 V / –2.53 V (min / typ /max)	10
• Changed output short-circuit current from ±13 mA to 14 mA (sourcing or sinking)	10
• Changed CMTI (AMC1300B) min from 75 to 100 kV/µs and typ from 140 to 150 kV/µs	10
• Changed $VDD1_{UV}$ from 1.75 V / 2.53 V / 2.7 V to 2.4 V / 2.6 V / 2.8 V (min / typ / max)	10
• Changed *Analog Input* section	21
• Changed *Analog Output* section	23
• Changed *Detailed Design Procedure* section	25
• Added *Shunt Resistor Sizing* section	25
• Added *Input Filter Design* section	25
• Added *Differential to Single-Ended Output Conversion* section	26
• Changed *Application Curves* section	27

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- Added layout recommendations to *What To Do and What Not To Do* section..... 27

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5 Device Comparison Table

PARAMETER		AMC1300B	AMC1300
High-side supply voltage, VDD1		3.0 V to 5.5 V	4.5 V to 5.5 V
Specified ambient temperature, T_A		–55°C to +125°C	–40°C to +125°C
Input offset voltage, V_{OS}	4.5 V ≤ VDD1 ≤ 5.5 V	±0.2 mV	±2 mV
	3.0 V ≤ VDD1 ≤ 4.5 V		Not applicable
Input offset drift, TCV_{OS}		±0.9 µV/°C (max)	±4 µV/°C (max)
Gain error, E_G		±0.3%	±1%
Gain error drift, TCE_G		±5 ppm/°C (typ), ±30 ppm/°C (max)	±50 ppm/°C (typ)
Common-mode transient immunity, CMTI		100 kV/µs (min), 150 kV/µs (typ)	15 kV/µs (min), 30 kV/µs (typ)
Output bandwidth, BW		250 kHz (min), 310 kHz (typ)	170 kHz (min), 230 kHz (typ)
INP, INN to OUTP, OUTN signal delay (50% – 90%)		3 µs (max)	3.4 µs (max)

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6 Pin Configuration and Functions

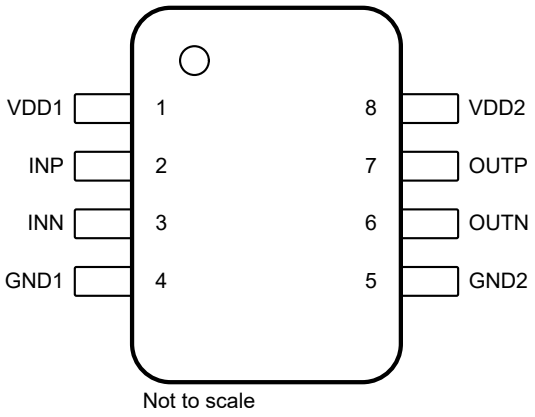


図 6-1. DWV Package, 8-Pin SOIC, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply.(1)
2	INP	Analog input	Noninverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
3	INN	Analog input	Inverting analog input. Either INP or INN must have a DC current path to GND1 to define the common-mode input voltage.(2)
4	GND1	High-side ground	High-side analog ground.
5	GND2	Low-side ground	Low-side analog ground.
6	OUTN	Analog output	Inverting analog output.
7	OUTP	Analog output	Noninverting analog output.
8	VDD2	Low-side power	Low-side power supply.(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Layout* section for details.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN	GND1 – 6	VDD1 + 0.5	V
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1300	4.5	5	5.5	V
		VDD1 to GND1, AMC1300B	3	5	5.5	
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} - V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} - V_{INN}$	–250		250	mV
	Absolute common-mode input voltage(1)	$(V_{INP}+V_{INN}) / 2$ to GND1	–2		VDD1	V
V_{CM}	Operating common-mode input voltage	$(V_{INP}+V_{INN}) / 2$ to GND1	–0.16		VDD1 – 2.1	V
TEMPERTURE RANGE						
T_A	Specified ambient temperature	AMC1300	–40		125	°C
		AMC1300B	–55		125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage VCM for normal operation. Observe analog input voltage range as specified in Absolute Maximum Ratings.

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7.4 Thermal Information

THERMAL METRIC(1)		AMC1300x DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	85.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	99	mW
		VDD1 = VDD2 = 3.6 V, AMC1300B only	57	
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5 V	54	mW
		VDD1 = 3.6 V, AMC1300B only	31	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V	45	mW
		VDD2 = 3.6 V	26	

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7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	≥ 8.5	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	≥ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance) of the double isolation (2 x 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE 0884-11 (VDE V 0884-11): 2017-01				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see Figure 4	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = V_{IOTM}$, t = 1 s (100% production test)	8485	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2 πft), f = 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Careshould be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator onthe printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases.Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

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7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: 40040142	Certificate number: E181974

7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			266	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 85.4°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C			407	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 85.4°C/W, T_J = 150°C, T_A = 25°C			1464	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

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7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1300 apply from T_A = – 40°C to+105°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; minimum and maximum specifications of the AMC1300B apply fromTA = – 55°C to+125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; typical specifications are at TA = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level	(V_{INP}+V_{INN}) / 2 to GND1	VDD1 – 2			V
	Hysteresis of common-mode overvoltage detection level			60		mV
V_{OS}	Input offset voltage(1) (2)	AMC1300, initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1	–2	±0.01	2	mV
		AMC1300B, initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1, 4.5 V ≤ VDD1 ≤ 5.5 V	–0.2	±0.01	0.2	
		AMC1300B, initial, at T_A = 25°C, V_{INP} = V_{INN} = GND1, 3.0 V ≤ VDD1 ≤ 5.5 V	–0.2	±0.01	0.2	
TCV_{OS}	Input offset drift(1) (2) (4)	AMC1300	–4	±1.3	4	uV/°C
		AMC1300B	–0.9	±0.1	0.9	
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min}$ ≤ $_{VC}$M ≤ $_{VCM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min}$ ≤ $_{VC}$M ≤ $_{VCM\ max}$		–98		
R_{IN}	Single-ended input resistance	INN = GND1		19		kΩ
R_{IND}	Differential input resistance			22		
I_{IB}	Input bias current	INP = INN = GND1; IIB = (IIBP+IIBN) / 2	–41	–30	–24	uA
I_{IO}	Input offset current	IIO = IIBP - IIBN		±5		nA
C_{IN}	Single-ended input capacitance	INN = GND1, f_{IN} = 275 kHz		2		pF
C_{IND}	Differential input capacitance	f_{IN} = 275 kHz		1		
ANALOG OUTPUT						
	Nominal gain			8.2		
E_G	Gain error(1)	AMC1300, initial, at T_A = 25°C	–1%	0.4%	1%	
		AMC1300B, initial, at T_A = 25°C	–0.3%	±0.05%	0.3%	
TCE_G	Gain error drift(1) (5)	AMC1300		±50		ppm/°C
		AMC1300B	–30	±5	30	
	Nonlinearity(1)		–0.03	±0.01	0.03	%
THD	Total harmonic distortion(3)	f_{IN} = 10 kHz		–85		dB
	Output noise	INP = INN = GND1, f_{IN} = 0 Hz, BW = 100 kHz brickwall filter		230		μV_{RMS}
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10 kHz	81.5	85		dB
		f_{IN} = 10 kHz, BW = 100 kHz		72		
PSRR	Power-supply rejection ratio(2)	PSRR vs VDD1, at DC		–103		dB
		PSRR vs VDD1, 100-mV and 10-kHz ripple		–96		
		PSRR vs VDD2, at DC		–106		
		PSRR vs VDD2, 100-mV and 10-kHz ripple		–86		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); |V_{IN}| = |V_{INP} – V_{INN}| > |$V_{Clipping}$|	–2.52	±2.49	2.52	V
$V_{FAILSAFE}$	Failsafe differential output voltage	V_{CM} ≥ $_{VCMov}$, or VDD1 missing	–2.63	–2.57	–2.53	V

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7.9 Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1300 apply from T_A = – 40°C to+105°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; minimum and maximum specifications of the AMC1300B apply fromTA = – 55°C to+125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, INP = – 250 mV to + 250 mV, and INN = GND1; typical specifications are at TA = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW_{OUT}	Output bandwidth	AMC1300	170	230		kHz
		AMC1300B	250	310		
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, INN = INP = GND1, outputs shorted to either GND2 or VDD2		14		mA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV, AMC1300	15	30		kV/µs
		|GND1 – GND2| = 1 kV, AMC1300B	100	150		
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold voltage	VDD1 falling	2.4	2.6	2.8	V
IDD1	High-side supply current	AMC1300B only, 3.0 V ≤ VDD1 ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ VDD1 ≤ 5.5 V		7.2	9.8	
IDD2	Low-side supply current	3.0 V ≤ VDD2 ≤ 3.6 V		5.3	7.2	mA
		4.5 V ≤ VDD2 ≤ 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation ("sigma") at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(5) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G\ (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

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7.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	AMC1300, unfiltered output		1.5	2.2	µs
		AMC1300B, unfiltered output		1	1.5	
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	AMC1300, unfiltered output		2	2.7	µs
		AMC1300B, unfiltered output		1.6	2.1	
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	AMC1300, unfiltered output		2.7	3.4	µs
		AMC1300B, unfiltered output		2.5	3	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		500		µs

7.11 Timing Diagram

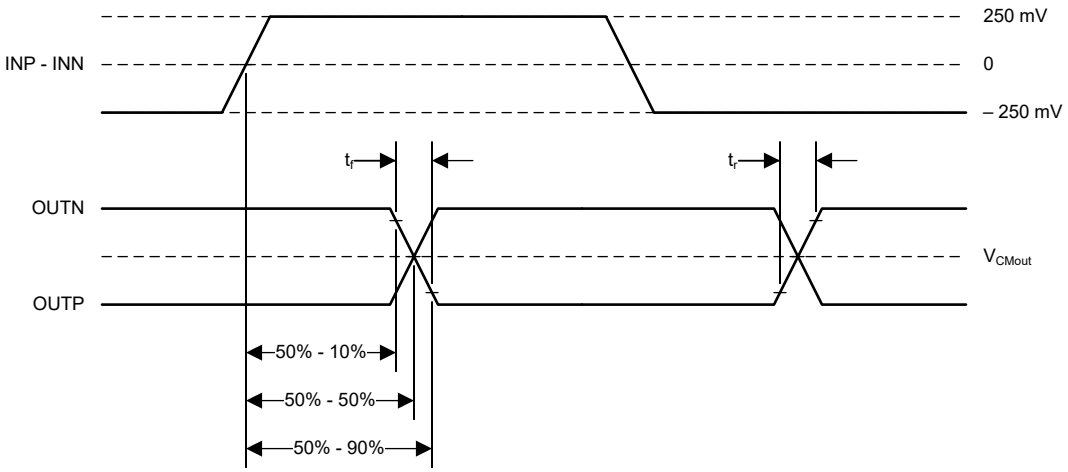


図 7-1. Rise, Fall, and Delay Time Waveforms

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7.12 Insulation Characteristics Curves

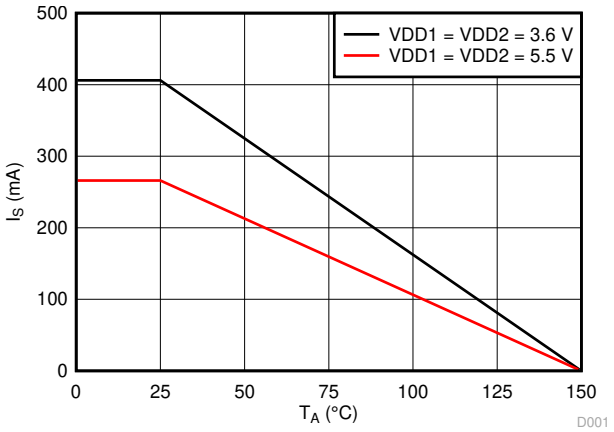


図 7-2. Thermal Derating Curve for Safety-Limiting Current per VDE

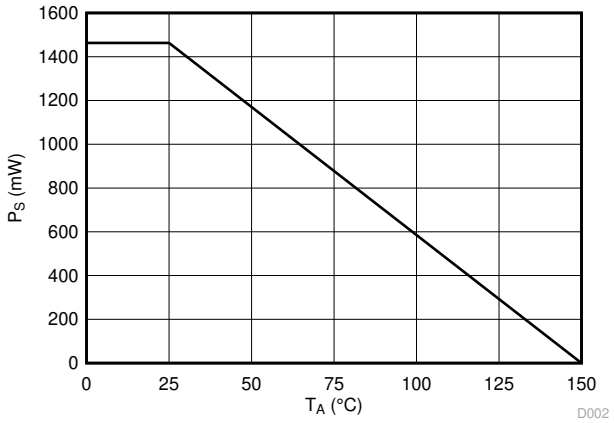
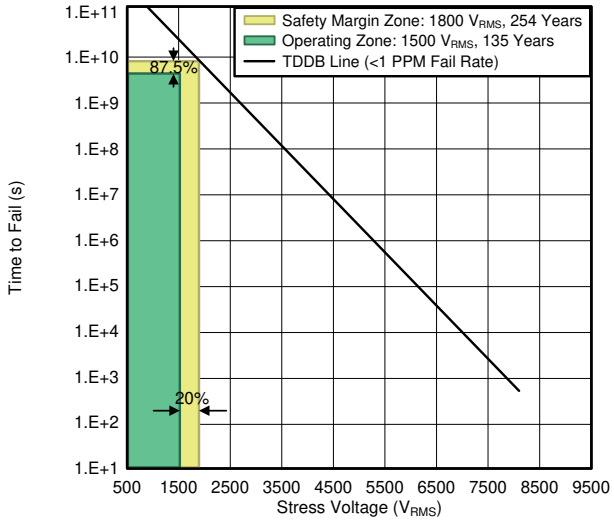


図 7-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 year

図 7-4. Reinforced Isolation Capacitor Lifetime Projection

7.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

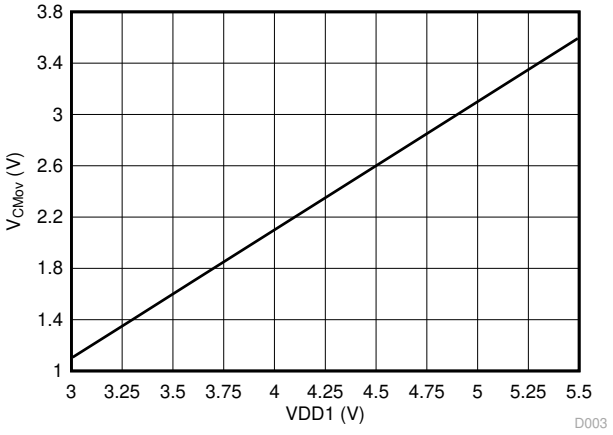
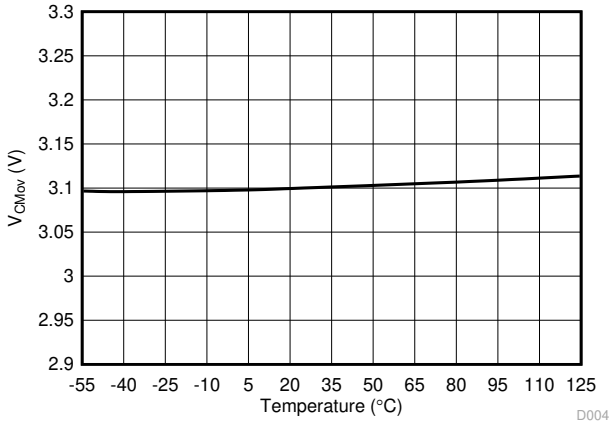
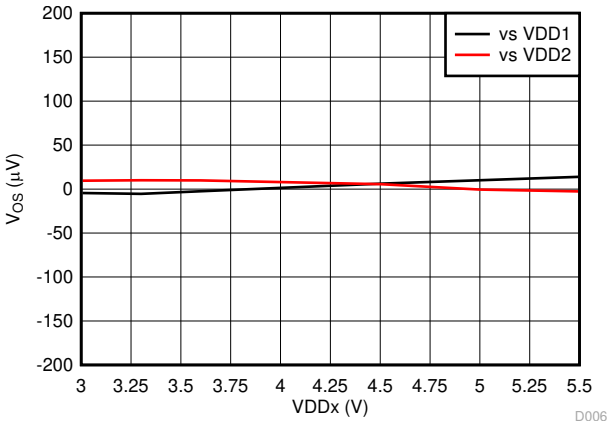


図 7-5. Common-Mode Overvoltage Detection Level vs High-Side Supply Voltage



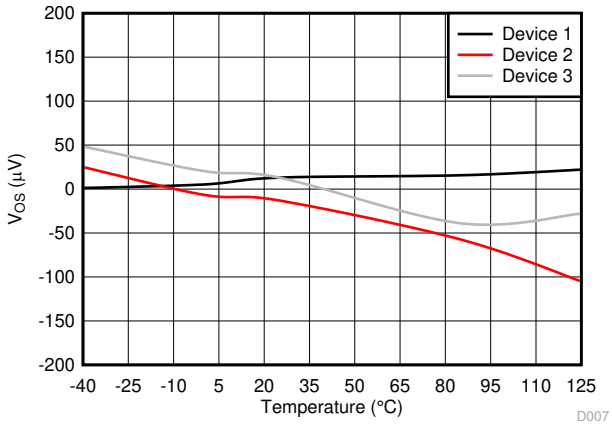
–55°C ≤ T_A < –40°C for AMC1300B only

図 7-6. Common-Mode Overvoltage Detection Level vs Temperature



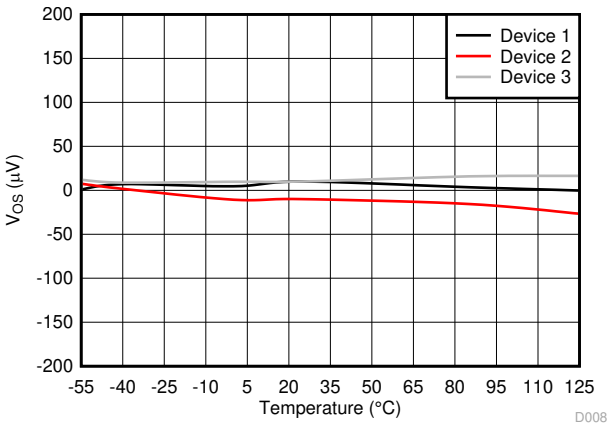
3 V ≤ VDD1 < 4.5 V for AMC1300B only

図 7-7. Input Offset Voltage vs Supply Voltage



AMC1300

図 7-8. Input Offset Voltage vs Temperature



AMC1300B

図 7-9. Input Offset Voltage vs Temperature

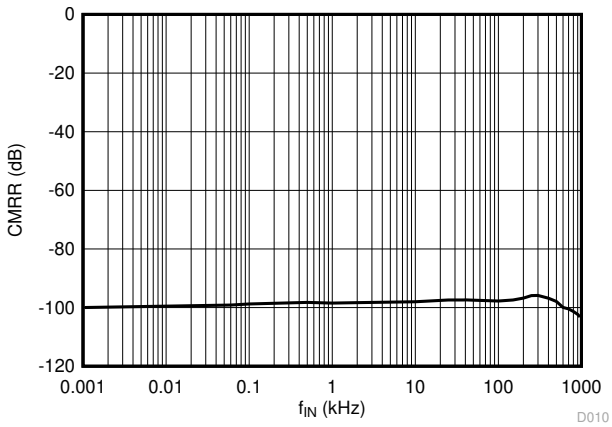
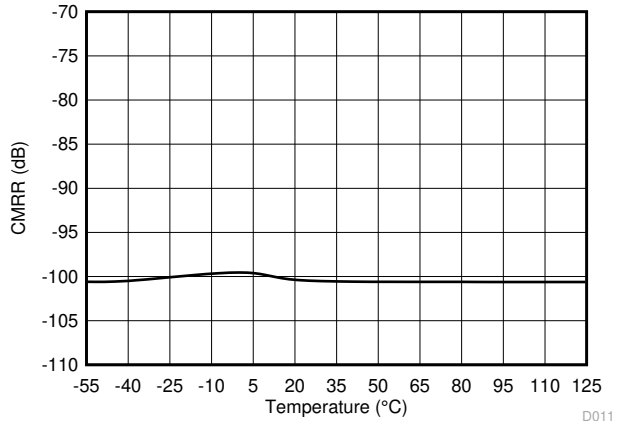


図 7-10. Common-Mode Rejection Ratio vs Input Frequency

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7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-11. Common-Mode Rejection Ratio vs Temperature

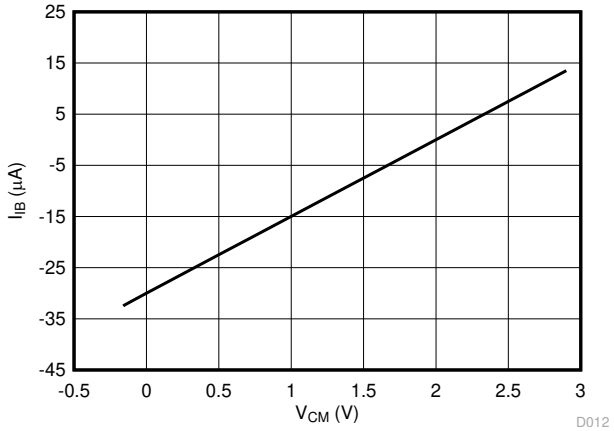


図 7-12. Input Bias Current vs Common-Mode Input Voltage

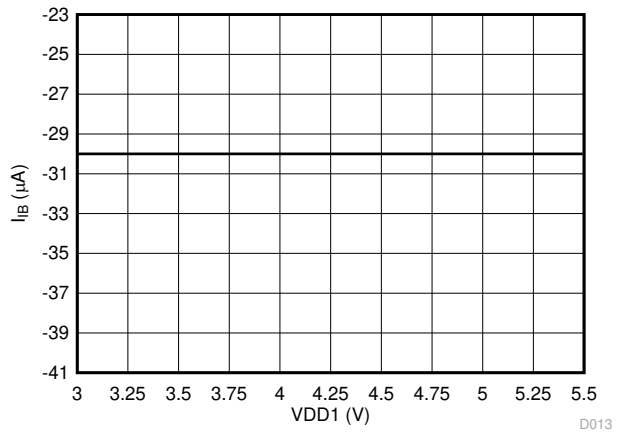
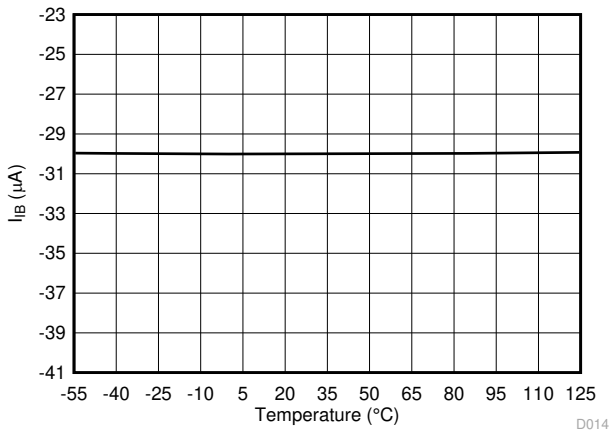


図 7-13. Input Bias Current vs High-Side Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-14. Input Bias Current vs Temperature

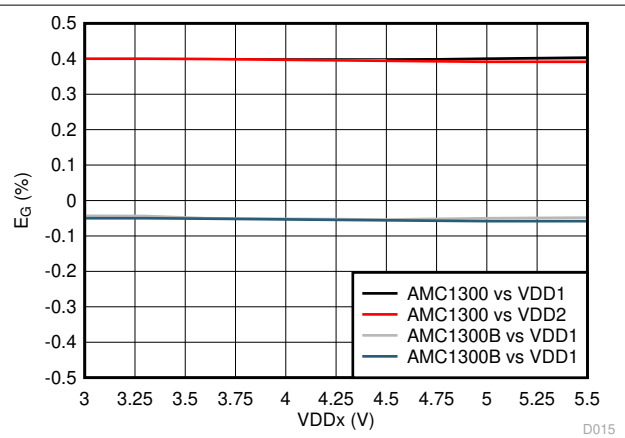
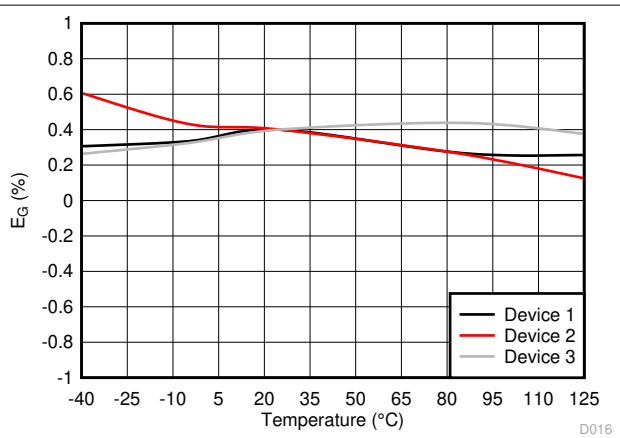


図 7-15. Gain Error vs Supply Voltage



AMC1300

図 7-16. Gain Error vs Temperature

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)

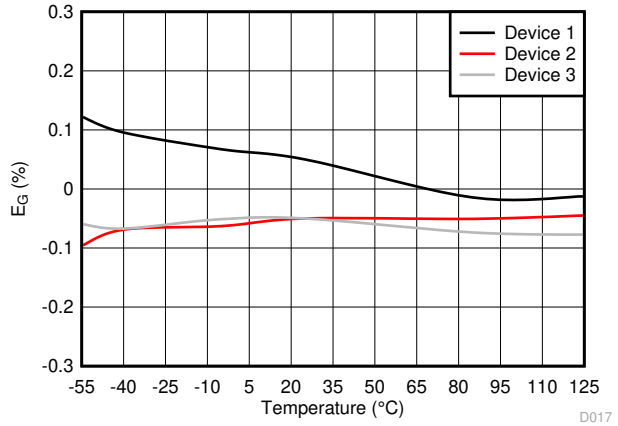


図 7-17. Gain Error vs Temperature

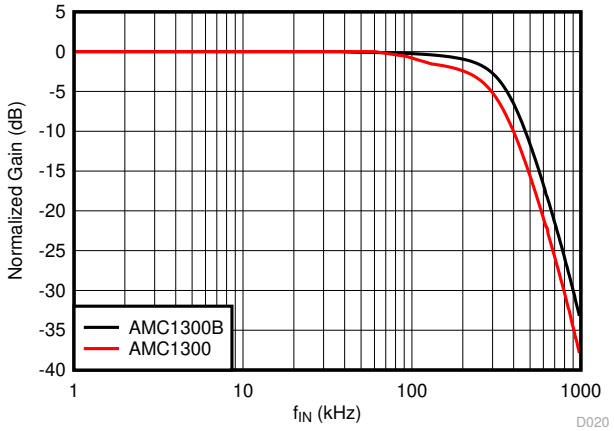


図 7-18. Normalized Gain vs Input Frequency

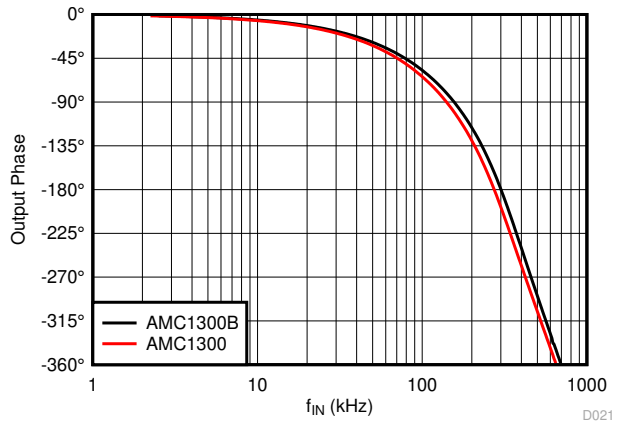


図 7-19. Output Phase vs Input Frequency

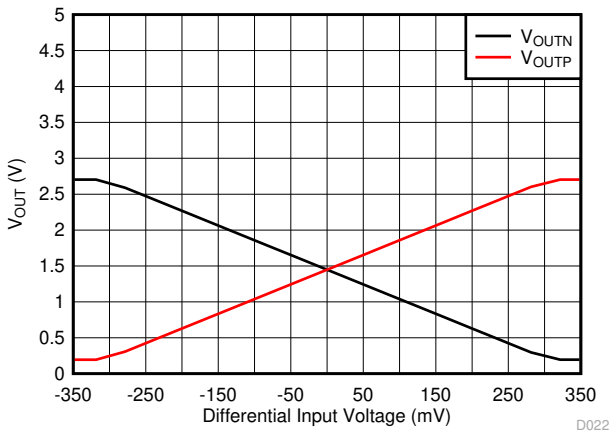


図 7-20. Output Voltage vs Input Voltage

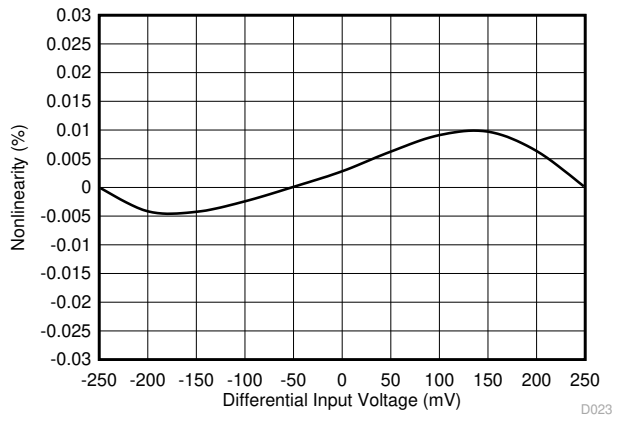


図 7-21. Nonlinearity vs Input Voltage

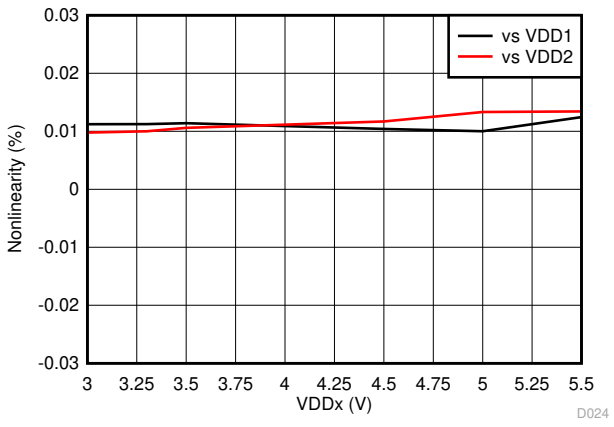
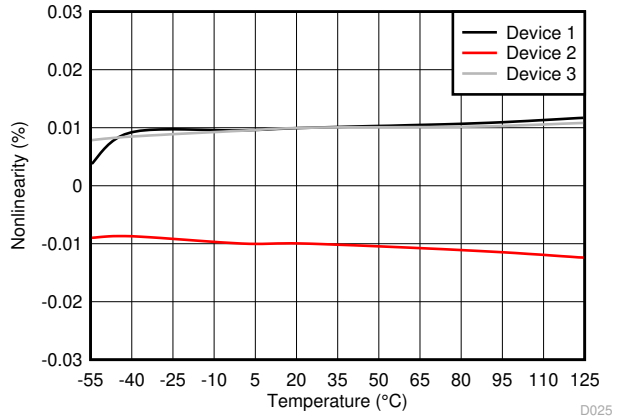


図 7-22. Nonlinearity vs Supply Voltage

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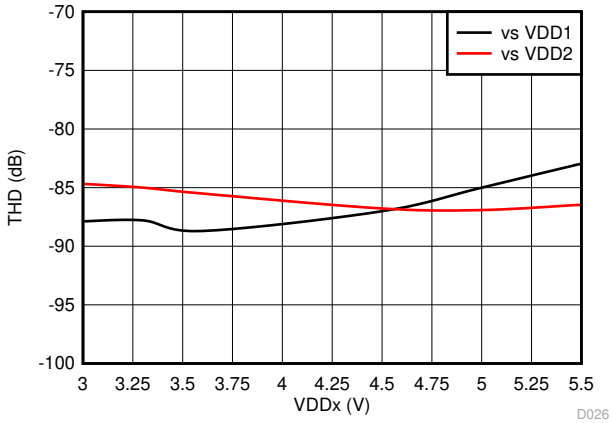
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



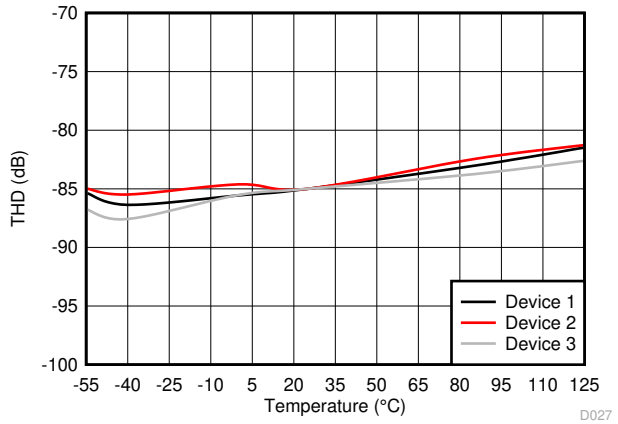
–55°C ≤ T_A < –40°C for AMC1300B only

図 7-23. Nonlinearity vs Temperature



3 V ≤ VDD1 < 4.5 V for AMC1300B only

図 7-24. Total Harmonic Distortion vs Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-25. Total Harmonic Distortion vs Temperature

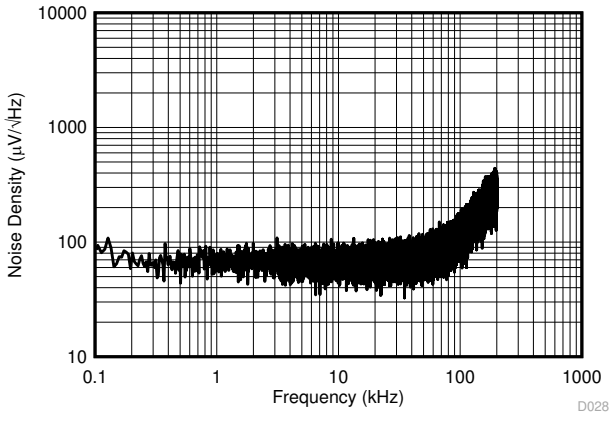


図 7-26. Input-Referred Noise Density vs Frequency

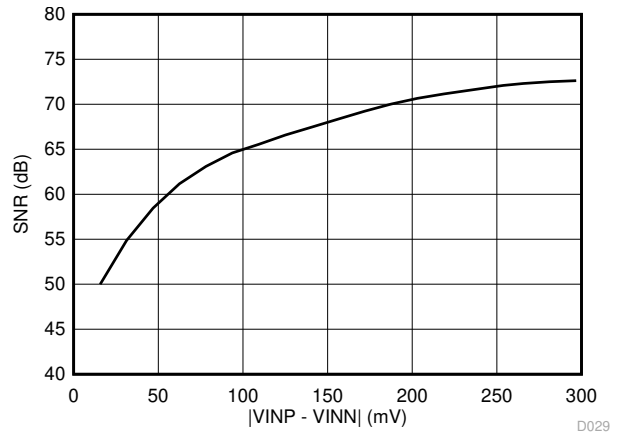
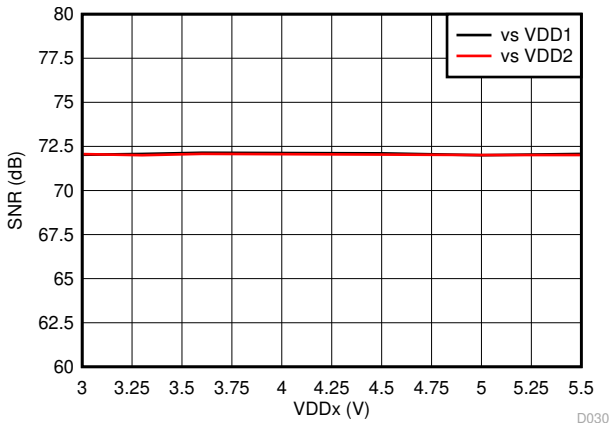


図 7-27. Signal-to-Noise Ratio vs Input Voltage



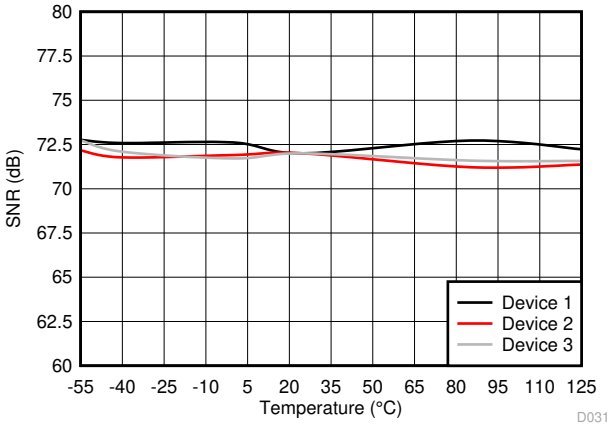
3 V ≤ VDD1 < 4.5 V for AMC1300B only

図 7-28. Signal-to-Noise Ratio vs Supply Voltage

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7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-29. Signal-to-Noise Ratio vs Temperature

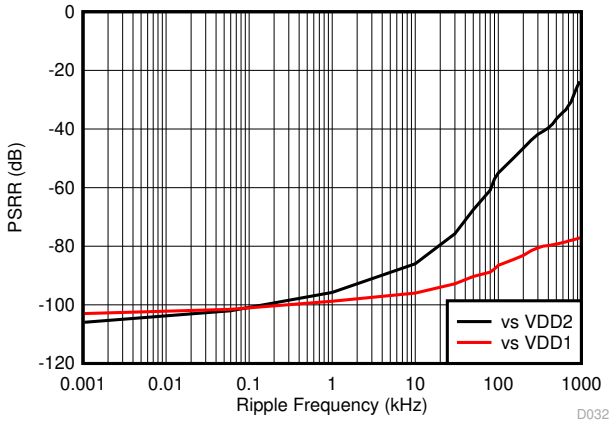


図 7-30. Power-Supply Rejection Ratio vs Ripple Frequency

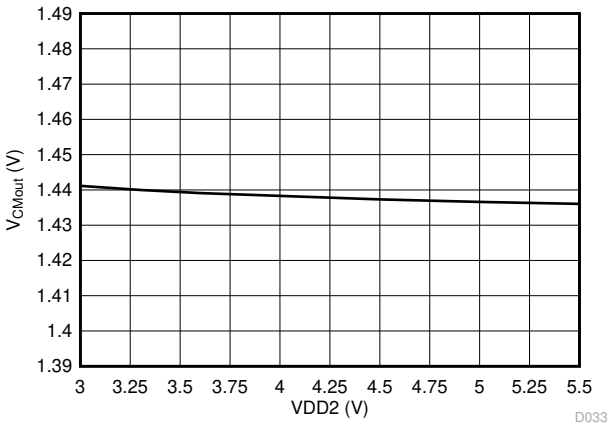
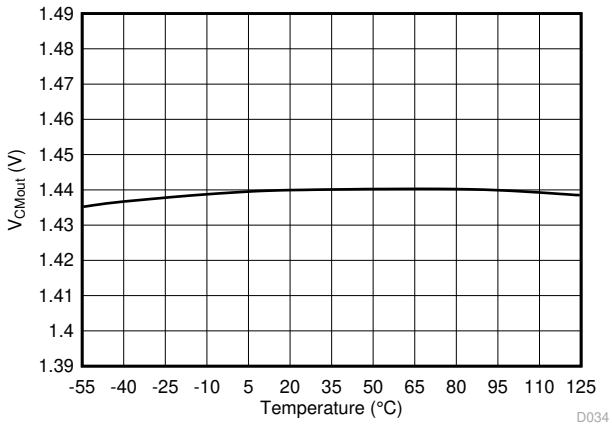


図 7-31. Output Common-Mode Voltage vs Low-Side Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-32. Output Common-Mode Voltage vs Temperature

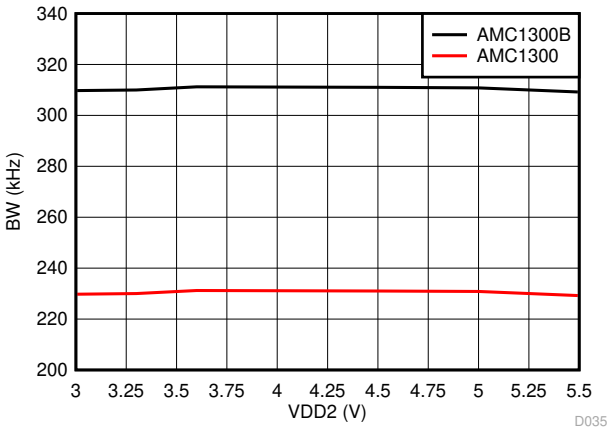


図 7-33. Output Bandwidth vs Low-Side Supply Voltage

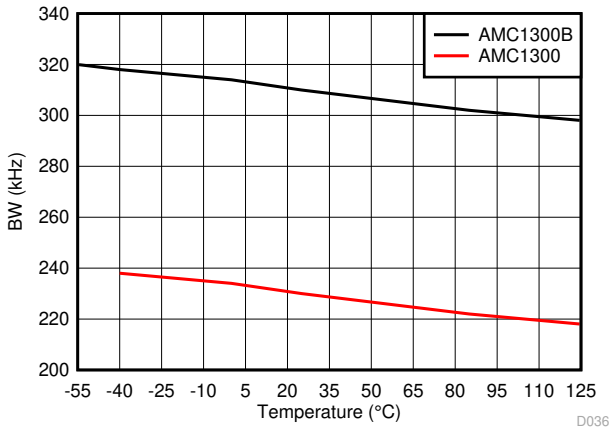
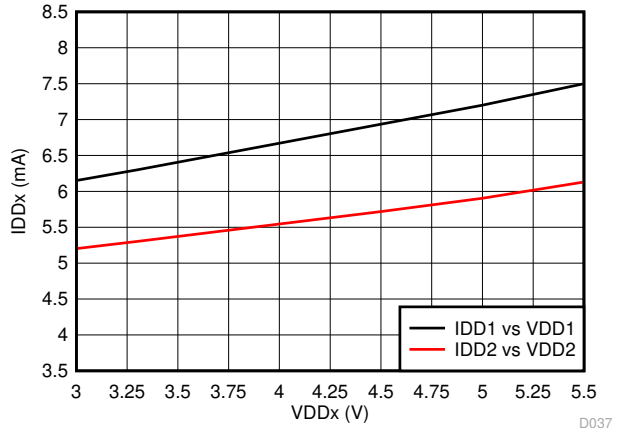


図 7-34. Output Bandwidth vs Temperature

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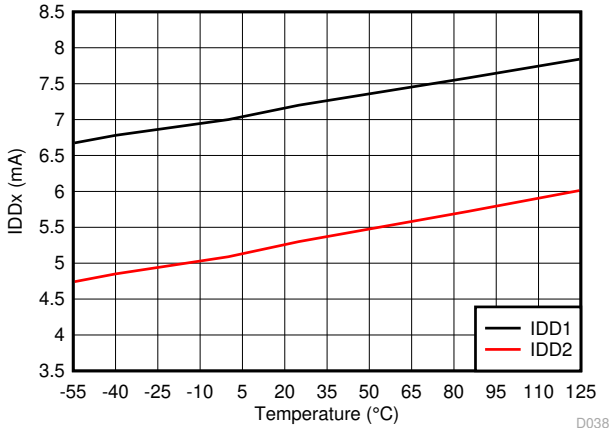
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



3 V ≤ VDD1 < 4.5 V for AMC1300B only

図 7-35. Supply Current vs Supply Voltage



–55°C ≤ T_A < –40°C for AMC1300B only

図 7-36. Supply Current vs Temperature

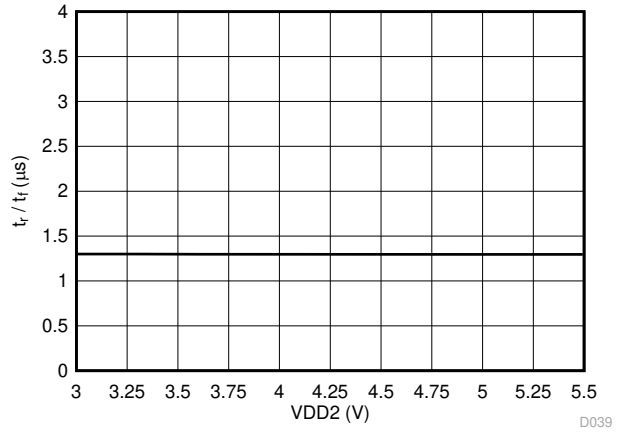
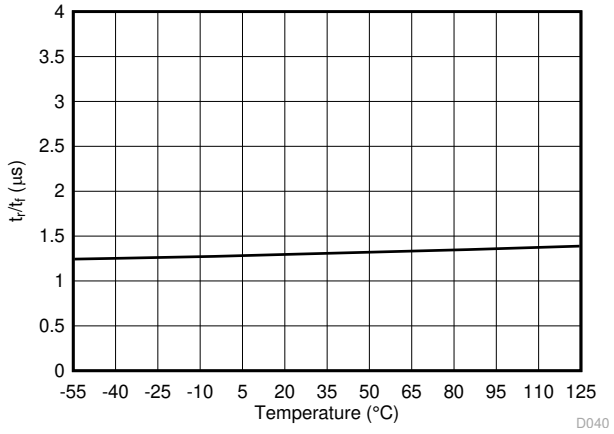
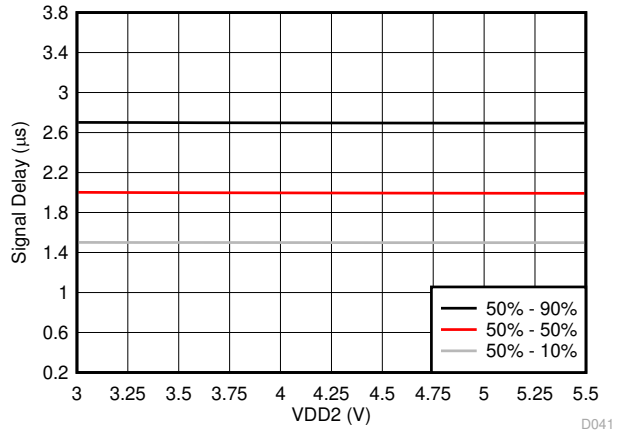


図 7-37. Output Rise and Fall Time vs Low-Side Supply



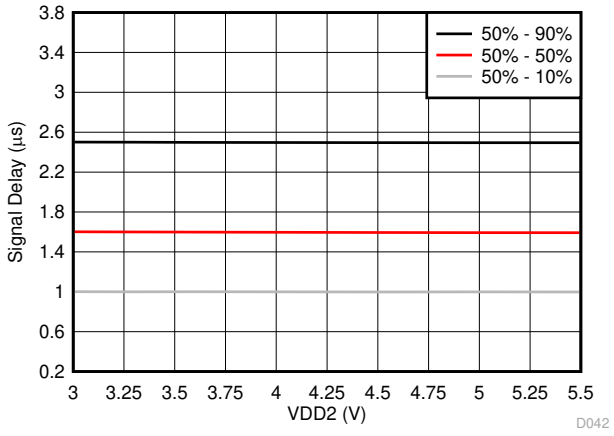
–55°C ≤ T_A < –40°C for AMC1300B only

図 7-38. Output Rise and Fall Time vs Temperature



AMC1300

図 7-39. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage



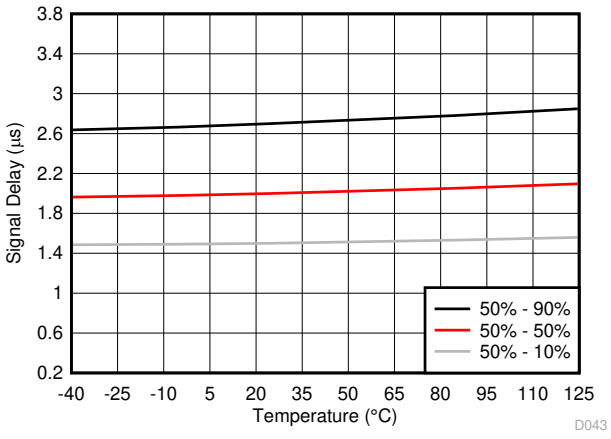
AMC1300B

図 7-40. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

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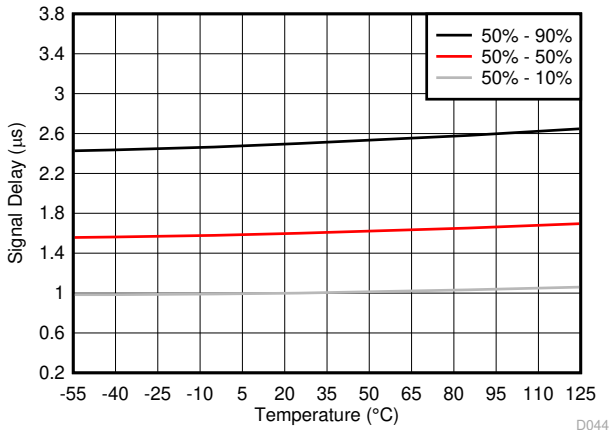
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and f_{IN} = 10 kHz (unless otherwise noted)



AMC1300

図 7-41. V_{IN} to V_{OUT} Signal Delay vs Temperature



AMC1300B

図 7-42. V_{IN} to V_{OUT} Signal Delay vs Temperature

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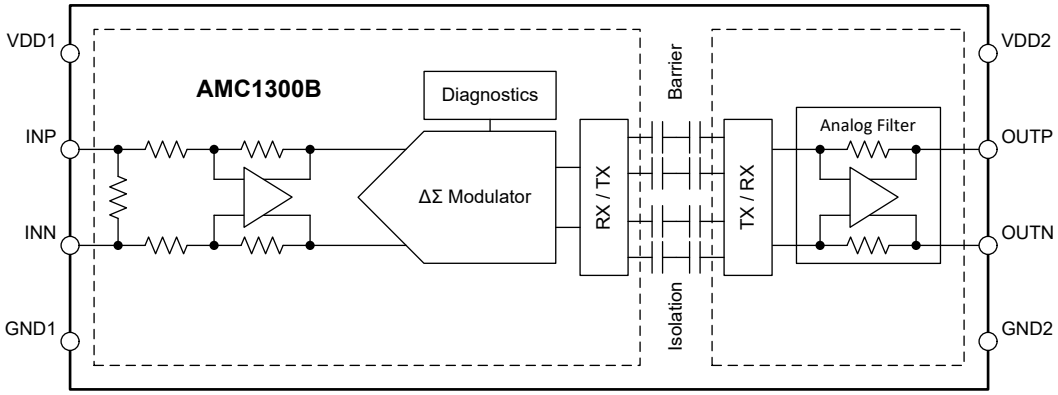
8 Detailed Description

8.1 Overview

The AMC1300 is a fully differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins that is proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1300 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The differential amplifier input stage of the AMC1300 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors with a differential input impedance of R_{IND}. The modulator converts the analog input signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals INP and INN. First, if the input voltages V_{INP} or V_{INN} exceed the range specified in the *Absolute Maximum Ratings* table, the input currents must be limited to the absolute maximum value, because the electrostatic discharge (ESD) protection turns on. In addition, the linearity and parametric performance of the device are ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) and within the common-mode input voltage range (V_{CM}) as specified in the *Recommended Operating Conditions* table.

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8.3.2 Isolation Channel Signal Transmission

The AMC1300 uses an on-off keying (OOK) modulation scheme, as shown in 図 8-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1300 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1300 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

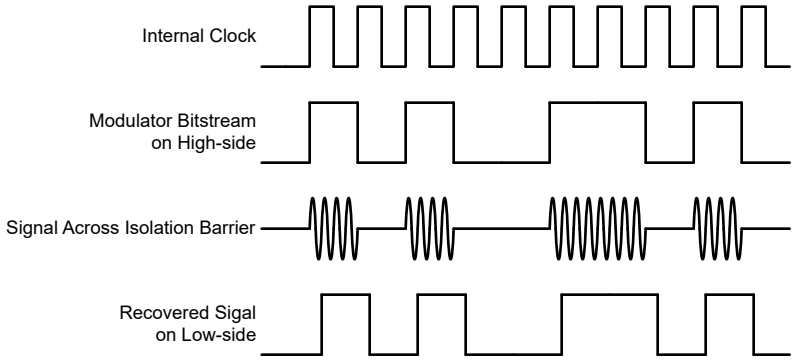


図 8-1. OOK-Based Modulation Scheme

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8.3.3 Analog Output

The AMC1300 offers a differential analog output comprised of the OUTP and OUTN pins. For differential input voltages (V_{INP} – V_{INN}) in the range from –250 mV to +250 mV, the device provides a linear response with a nominal gain of 8.2. For example, for a differential input voltage of 250 mV, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2.05 V. At zero input (INP shorted to INN), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For absolute differential input voltages greater than 250 mV but less than 320 mV, the differential output voltage continues to increase in magnitude but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 図 8-2, if the differential input voltage exceeds the $V_{Clipping}$ value.

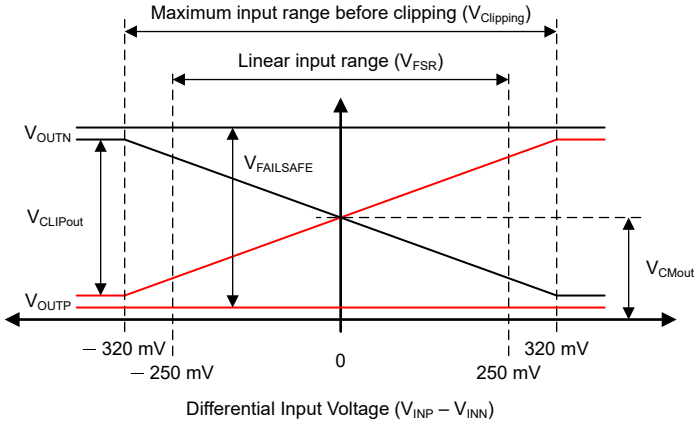


図 8-2. Output Behavior of the AMC1300

The AMC1300 offers a fail-safe feature that simplifies diagnostics on system level. 図 8-2 shows the fail-safe potential that is a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in two cases:

- When the high-side supply is missing or below the $VDD1_{UV}$ threshold
- When the common-mode input voltage, that is V_{CM} = (V_{INP} + V_{INN}) / 2, exceeds the common-mode overvoltage detection level V_{CMov}

Use the maximum $V_{FAILSAFE}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on system level.

8.4 Device Functional Modes

The AMC1300 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

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9 Application and Implementation

Note

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9.1 Application Information

The low analog input voltage range, excellent accuracy, and low temperature drift make the AMC1300 a high-performance solution for industrial applications where shunt-based current sensing in the presence of high common-mode voltage levels is required.

9.2 Typical Application

The AMC1300 is ideally suited for shunt-based current sensing applications where accurate current monitoring is required in the presence of high common-mode voltages.

図 9-1 shows the AMC1300 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop that is sensed by the AMC1300. The AMC1300 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents that signal as a differential voltage on the output pins.

The differential input, differential output, and the high common-mode transient immunity (CMTI) of the AMC1300 ensure reliable and accurate operation even in high-noise environments.

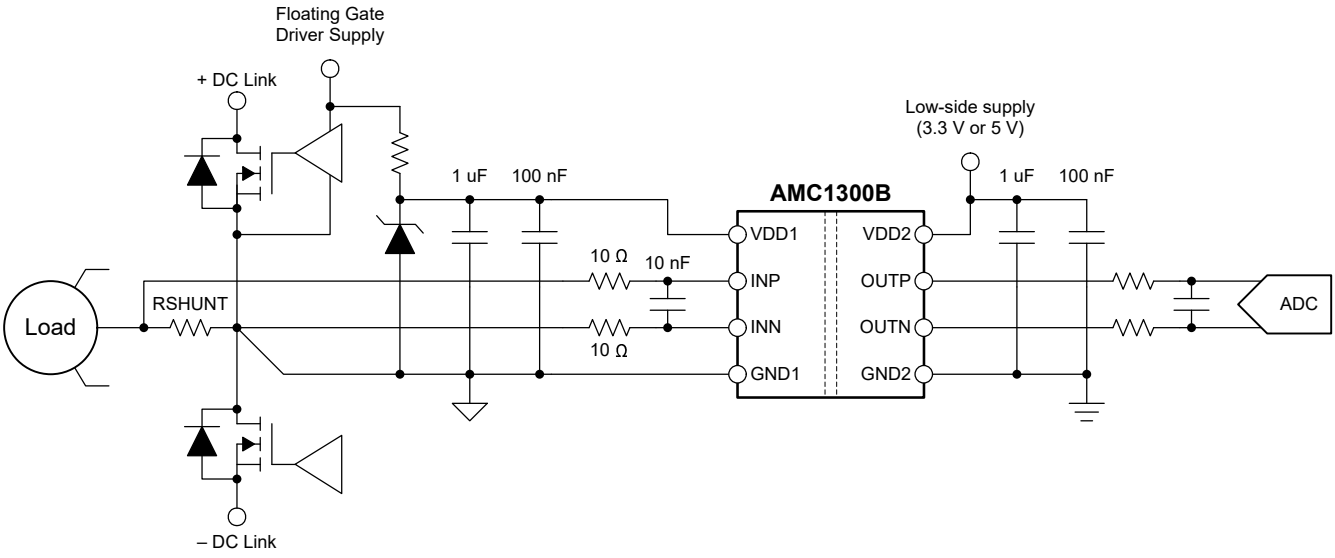


図 9-1. Using the AMC1300 for Current Sensing in a Typical Application

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9.2.1 Design Requirements

表 9-1 lists the parameters for this typical application.

表 9-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across RSHUNT for a linear response	± 250 mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	3 µs (maximum)

9.2.2 Detailed Design Procedure

In 図 9-1, the high-side power supply (VDD1) for the AMC1300 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC1300 (INN). If a four-pin shunt is used, the inputs of the AMC1300 are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

9.2.2.1 Shunt Resistor Sizing

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times RSHUNT$.

Consider the following two restrictions when selecting the value of the shunt resistor, RSHUNT:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range for a linear response: $|V_{SHUNT}| \leq |V_{FSR}|$
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

9.2.2.2 Input Filter Design

TI recommends placing an RC filter in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

For most applications, the structure shown in 図 9-2 achieves excellent performance.

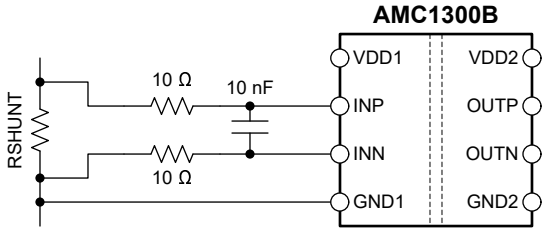


図 9-2. Differential Input Filter

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9.2.2.3 Differential-to-Single-Ended Output Conversion

図 9-3 shows an example of a TLV6001-based signal conversion and filter circuit for systems using single-ended-input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

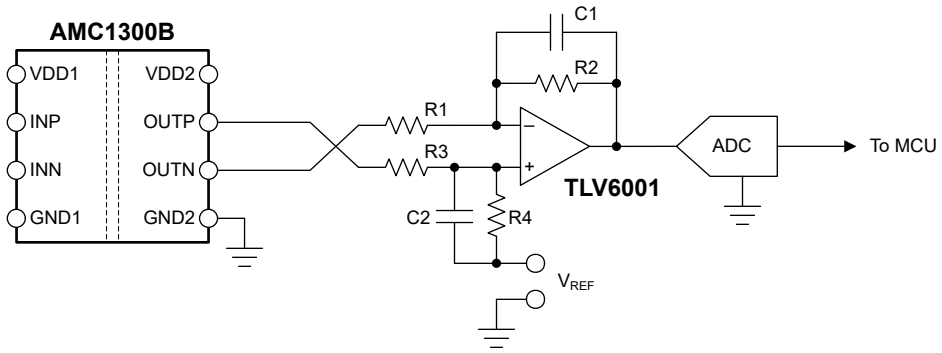


図 9-3. Connecting the AMC1300 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

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9.2.3 Application Curves

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. 図 9-4 shows the typical full-scale step response of the AMC1300.

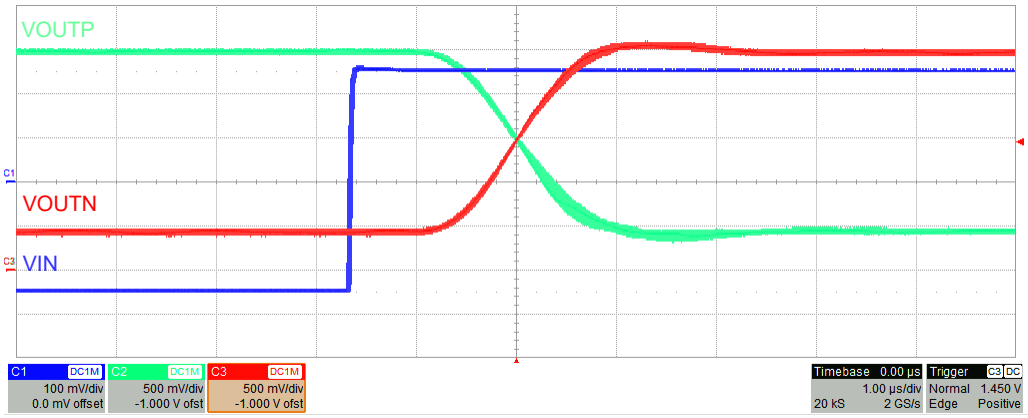


図 9-4. Step Response of the AMC1300

9.3 What To Do and What Not To Do

Do not leave the inputs of the AMC1300 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current may drive the inputs to a positive value that exceeds the operating common-mode input voltage and the device outputs the fail-safe voltage as described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Recommended Operating Conditions* table. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor rather than shorting GND1 to INN directly at the input to the device. See the *Layout* section for more details.

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10 Power Supply Recommendations

The AMC1300 does not require any specific power up sequencing. The high-side power-supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible.

The ground reference for the high-side (GND1) is derived from the end of the shunt resistor, which is connected to the negative input (INN) of the device. For best DC accuracy, use a separate trace (as shown in 図 10-1) to make this connection instead of shorting GND1 to INN directly at the device input. If a four-terminal shunt is used, the device inputs are connected to the inner leads and GND1 is connected to the outer lead on the INN-side of the shunt.

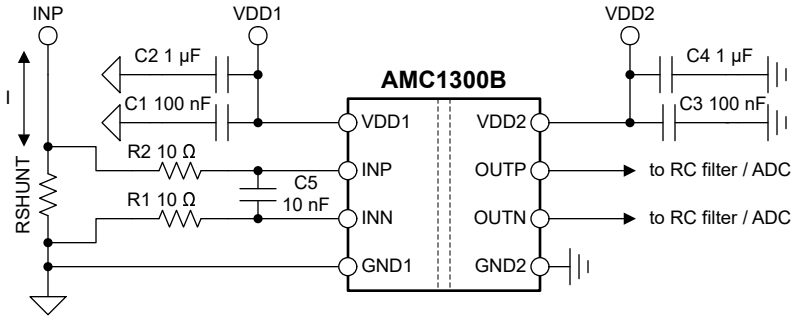


図 10-1. Decoupling of the AMC1300

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCCs) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

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11 Layout

11.1 Layout Guidelines

図 11-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1300 supply pins) and placement of the other components required by the device. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC1300 and keep the layout of both connections symmetrical.

11.2 Layout Example

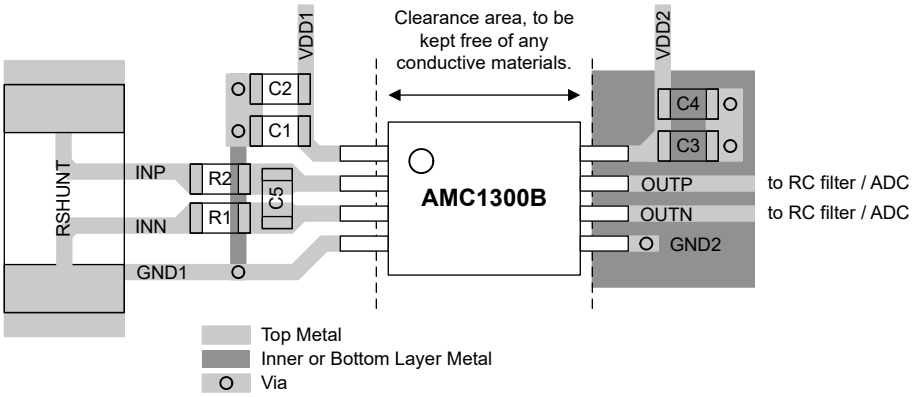


図 11-1. Recommended Layout of the AMC1300

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1300BDWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300BDWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300BDWVG4	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300BDWVG4.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300BDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300BDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	AMC1300B
AMC1300DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300
AMC1300DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300
AMC1300DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC1300

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

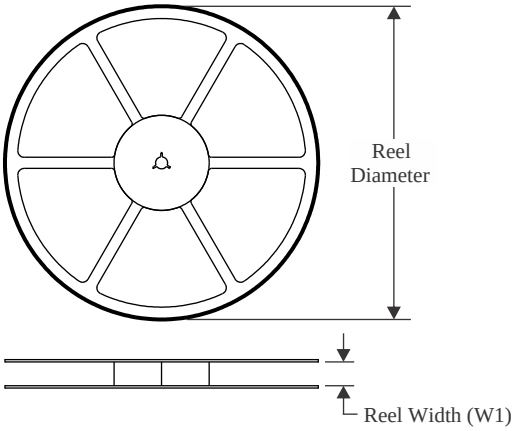
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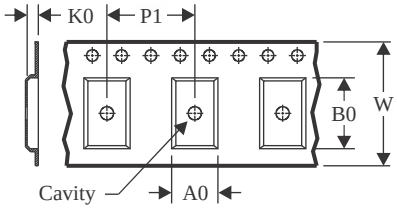
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

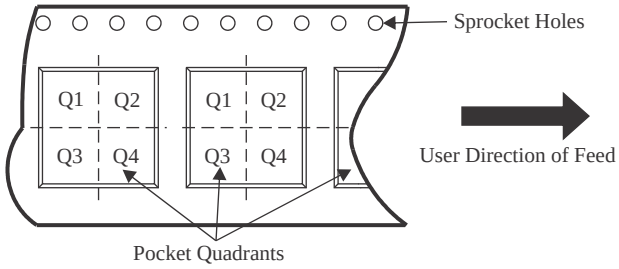


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

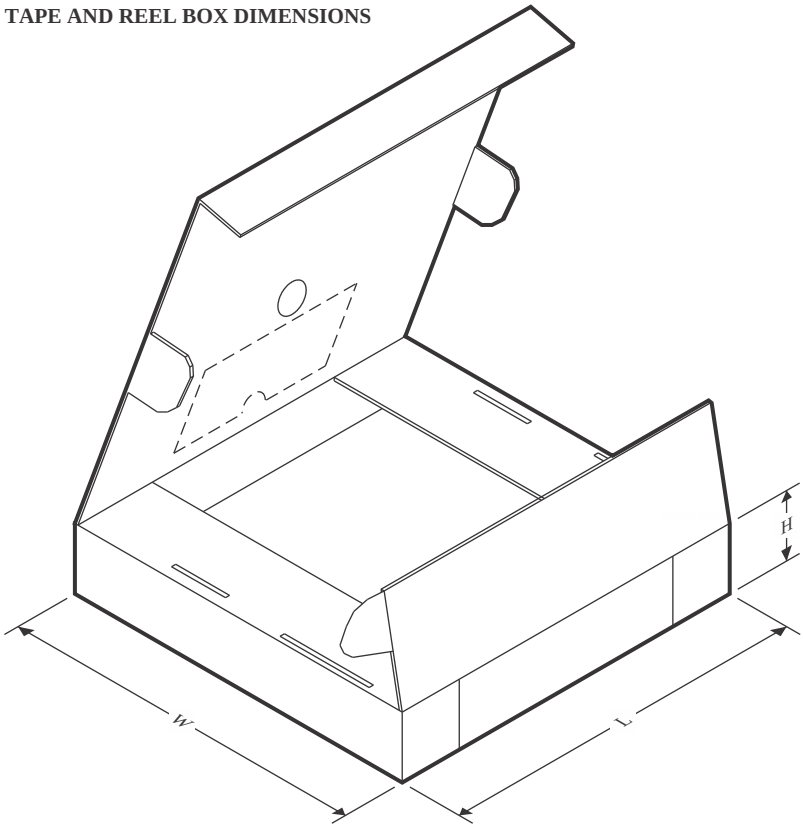
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1300BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1300DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

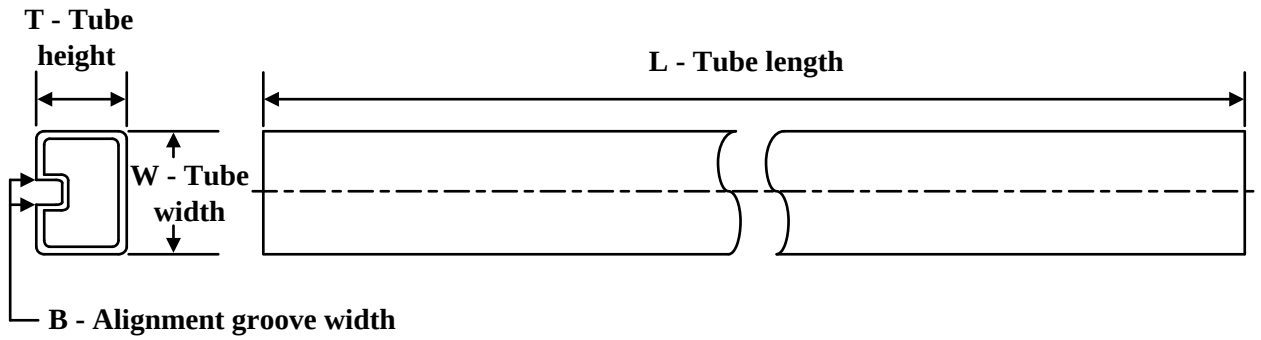
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

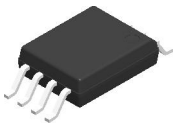
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1300BDWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1300DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

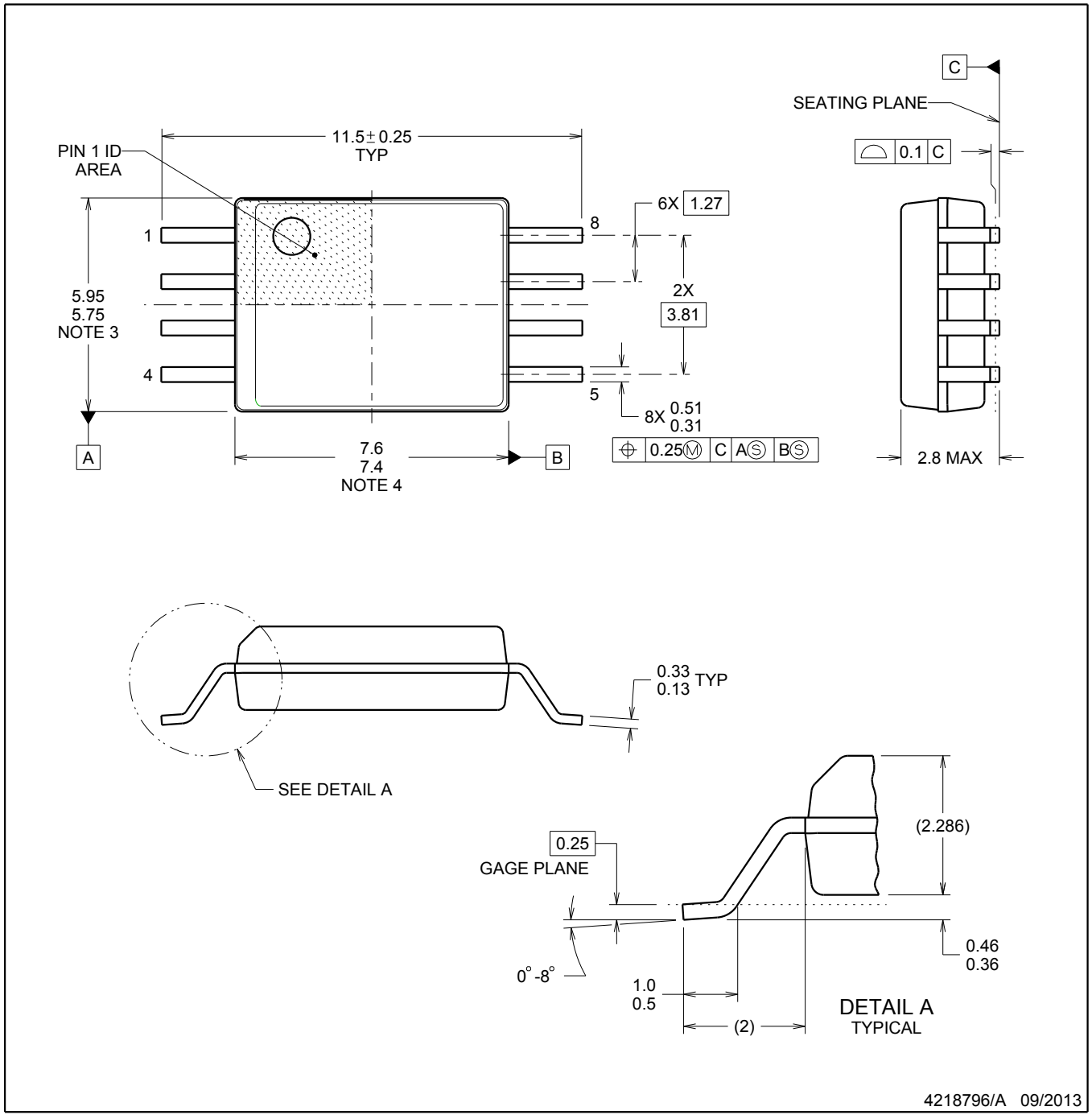
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1300BDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1300BDWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1300BDWVG4	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1300BDWVG4.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1300DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

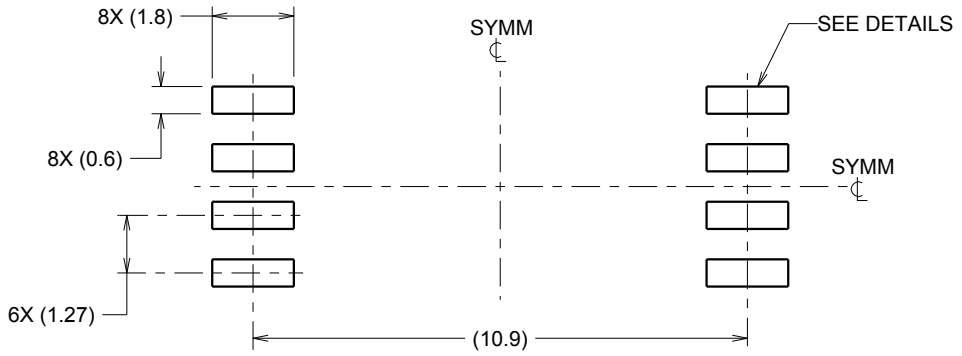
SOIC - 2.8 mm max height

SOIC

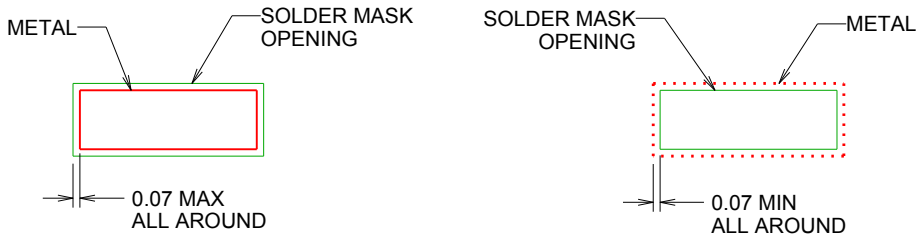


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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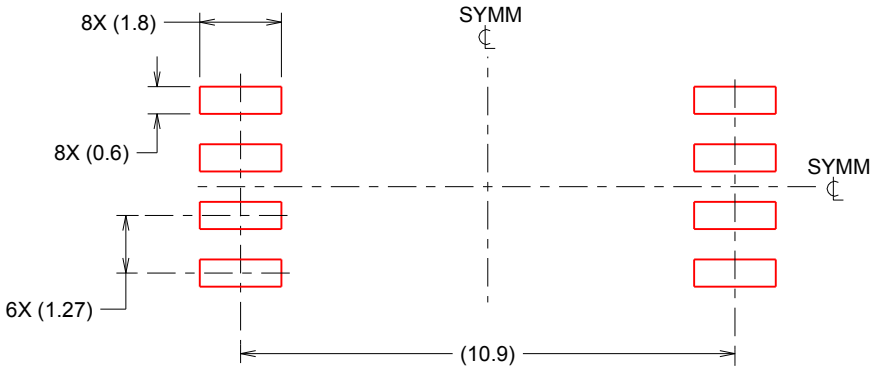
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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