TEXAS INSTRUMENTS
AMC1306E05, AMC1306E25, AMC1306M05, AMC1306M25
JAJSCZ5C – MARCH 2017 – REVISED JANAURY 2020

AMC1306x 高CMTI、小型、高精度の強化絶縁デルタ-シグマ変調器

1 特長

- シャント抵抗ベースの電流測定用に最適化されたピン互換ファミリ
  - ±50mV または ±250mV の入力電圧範囲
  - マンチェスター符号化または非符号化のビットストリーム・オプション
- 非常に優れた DC 性能
  - オフセット誤差:±50µV または ±100µV (最大値)
  - オフセット・ドリフト係数:1µV/℃ (最大値)
  - ゲイン誤差:±0.2% (最大値)
  - ゲイン・ドリフト係数:±40ppm/℃ (最大値)
- 過渡耐性：100kV/µs (標準値)
- システム・レベル診断機能
- 安全関連の認定
  - DIN VDE V 0884-11: 2017-01 に準拠した $7000V_{PEAK}$ の強化絶縁
  - UL 1577 に準拠した絶縁耐圧:$5000V_{RMS}$ (1 分間)
  - CAN/CSA No.5A-Component Acceptance Service Notice および IEC 62368-1 End Equipment Standard
- 拡張産業用温度範囲にわたって完全に動作を規定：–40°C～+125°C

2 アプリケーション

- 次の用途における、シャント抵抗を基礎にした電流センシングおよび絶縁電圧測定
  - 産業用モータ駆動
  - 太陽光発電インバータ
  - 無停電電源

3 概要

AMC1306は高精度のデルタ・シグマ(ΔΣ)変調器で、磁気干渉に対して高い耐性のある二重の静電容量性絶縁膜により、入力と出力の回路が分離されています。この絶縁バリアは、DIN VDE V 0884-11 および UL1577 規格に準拠した、7000 V_{PEAK} までの強化絶縁体に認定されています。この絶縁変調器を絶縁電源と組み合わせて使用すると、システムの中で異なる同相電圧レベルで動作する部分が分離され、低電圧部分の損傷を防ぎます。

AMC1306の入力は、シャント抵抗または他の低電圧レベルの信号源と直接接続するよう最適化されています。±50mVデバイスの独自の低い入力電圧範囲により、シャントによる消費電力が大幅に低減され、優れたACおよびDC性能が実現されます。AMC1306の出力ビットストリームには、マンチェスター符号化(AMC1306Ex)または非符号化(AMC1306Mx)のバリエーションがあります。内蔵デジタル・フィルタ(TMS320F2807xやTMS320F2837xマイクロコントローラ・ファミリで使用されているものなど)を使用してビットストリームを間引くと、78kSPSのデータ速度、85dBのダイナミック・レンジで、16ビットの分解能が得られます。

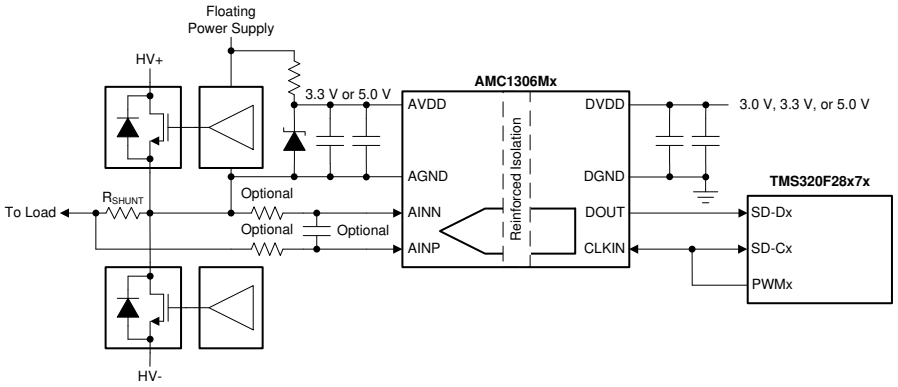
マンチェスター符号化のAMC1306Exバージョンのビットストリーム出力では、受信側デバイスのセットアップ時間やホールド時間の要件を考慮する必要なしに、単線でデータとクロックを伝送できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
AMC1306x	SOIC (8)	5.85mm×7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

Revision B (June 2018) から **Revision C** に変更 **Page**

- 「*特長*」セクションの*安全関連の認定*項目：*VDE 認定*のリビジョンを *DIN V VDE V 0884-10 (VDE V 0884-11)* から *DIN VDE V 0884-11* に変更、*IEC 60950-1*、および *IEC 60065* を *IEC 62368-1* に 変更 ... 1
- 「*概要*」セクションの *DIN V VDE V* を *DIN VDE V* に 変更 ... 1
- Changed CLR and CPG values from ≥ 9 mm to ≥ 8.5 mm in *Insulation Specifications* table ... 6
- Changed *Insulation Specifications* table header row from *DIN V VDE V 0884-11 (VDE V 0884-11): 2017-01* to *DIN VDE V 0884-11: 2017-01* ... 6
- Changed VDE certification details in *Safety-Related Certifications* table ... 7
- Changed *Safety Limiting Values* table format as per current standard ... 7
- Changed *free air* to *ambient* in condition statement of *Switching Characteristics* table ... 12
- Changed 6.05 dB to 6.02 dB in Equation 3 ... 27
- Changed input common-mode voltage from 2 V to 1.9 V for consistency with *Input Bias Current vs Common-Mode Input Voltage* figure in *What To Do and What Not To Do* section ... 32
- Changed *VINx* to *AINx* in *Layout Guidelines* section ... 34
- Changed *Recommended Layout of the AMC1306x* figure to include connection to the shunt resistor and input filter components ... 34

Revision A (July 2017) から **Revision B** に変更 **Page**

- Changed *Reinforced Isolation Capacitor Lifetime Projection* figure ... 13

2017年3月発行のものから更新 **Page**

- AMC1306E05 および AMC1306M05 を量産にリリース ... 1
- AMC1306x05 を反映するため、最初の*DC 性能*項目に ±50µV を 追加 ... 1
- 最初の*安全関連の認定*項目で規格のリビジョンを 0884-10 から 0884-11 に 変更 ... 1

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- 「概要」セクションの第 1 段落で V_{PEAK} を 8000 から 7000 に、規格のリビジョンを 0884-10 から 0884-11 に 変更 1
- Deleted Status column from *Device Comparison Table* 4
- Changed standard deviation from 0884-10 to 0884-11 in *DIN V VDE V 0884-11* section of *Insulation Specifications* table 6
- Changed standard deviation from 0884-10 to 0884-11 in *Safety-Related Certifications* table 7
- Changed *prevent* to *minimize* in condition statement of *Safety Limiting Values* table 7
- Added *Electrical Characteristics: AMC1306x05* table 8
- Changed test conditions of Analog Inputs test conditions from *(AINP – AINN) / 2 to AGND* to *(AINP + AINN) / 2 to AGND* to include all possible conditions 10
- Changed I_{IB} test condition from *Inputs shorted to AGND* to *AINP = AINN = AGND,* $I_{IB} = I_{IBP} + I_{IBN}$ 10
- Added *AINP = AINN = AGND* to E_O parameter test conditions 10
- Changed minus sign to plus or minus sign in typical specification of E_G parameter 10
- Changed *10% to 90%* to *90% to 10%* in test conditions of t_f parameter 12
- Added AMC1306x05 devices to *Typical Characteristics* section 14

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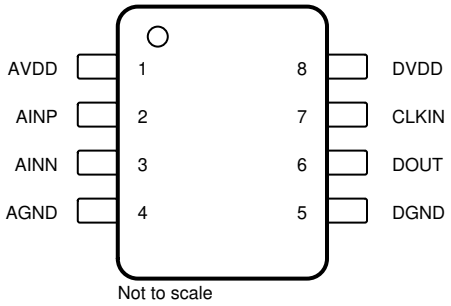
5 Device Comparison Table

PART NUMBER	INPUT VOLTAGE RANGE	DIFFERENTIAL INPUT RESISTANCE	DIGITAL OUTPUT INTERFACE
AMC1306E05	±50 mV	4.9 kΩ	Manchester coded CMOS
AMC1306E25	±250 mV	22 kΩ	Manchester coded CMOS
AMC1306M05	±50 mV	4.9 kΩ	Uncoded CMOS
AMC1306M25	±250 mV	22 kΩ	Uncoded CMOS

6 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	AVDD	—	Analog (high-side) power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.
2	AINP	I	Noninverting analog input
3	AINN	I	Inverting analog input
4	AGND	—	Analog (high-side) ground reference
5	DGND	—	Digital (controller-side) ground reference
6	DOUT	O	Modulator data output. This pin is a Manchester coded output for AMC1306Ex derivates.
7	CLKIN	I	Modulator clock input: 5 MHz to 21 MHz (5-V operation) with internal pulldown resistor (typical value: 1.5 MΩ)
8	DVDD	—	Digital (controller-side) power supply, 2.7 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

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7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage	AVDD to AGND or DVDD to DGND	–0.3	6.5	V
Analog input voltage at AINP, AINN		AGND – 6	AVDD + 0.5	V
Digital input or output voltage at CLKIN or DOUT		DGND – 0.5	DVDD + 0.5	V
Input current to any pin except supply pins		–10	10	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog (high-side) supply voltage (AVDD to AGND)	3.0	5.0	5.5	V
DVDD	Digital (controller-side) supply voltage (DVDD to DGND)	2.7	3.3	5.5	V
T_A	Operating ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		AMC1306x DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	AMC1306Ex, AVDD = DVDD = 5.5 V			91.85	mW
		AMC1306Mx, AVDD = DVDD = 5.5 V			86.90	
P_{D1}	Maximum power dissipation (high-side supply)	AVDD = 5.5 V			53.90	mW
P_{D2}	Maximum power dissipation (low-side supply)	AMC1306Ex, DVDD = 5.5 V			37.95	mW
		AMC1306Mx, DVDD = 5.5 V			33.00	

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7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation (2 × 0.0105 mm)	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11: 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	1500	V_{RMS}
		At dc voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS} or 7000 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

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7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11: 2017-01, DIN EN 62368-1: 2016-05, EN 62368-1: 2014, and IEC 62368-1: 2014	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
File number: DIN 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 5.5 V, T_J = 150°C, T_A = 25°C			202.5	mA
		$R_{\theta JA}$ = 112.2°C/W, AVDD = DVDD = 3.6 V, T_J = 150°C, T_A = 25°C			309.4	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 112.2°C/W, T_J = 150°C, T_A = 25°C			1114 (1)	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times AVDD_{max}$, where $AVDD_{max}$ is the maximum high-side supply voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

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7.9 Electrical Characteristics: AMC1306x05

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Differential input voltage before clipping output	V_{IN} = AINP – AINN		±64		mV
FSR	Specified linear differential full-scale	V_{IN} = AINP – AINN	–50		50	mV
	Absolute common-mode input voltage(1)	(AINP + AINN) / 2 to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage	(AINP + AINN) / 2 to AGND	–0.032		AVDD – 2.1	V
V_{CMov}	Common-mode overvoltage detection level(2)	(AINP + AINN) / 2 to AGND	AVDD - 2			V
C_{IN}	Single-ended input capacitance	AINN = AGND		4		pF
C_{IND}	Differential input capacitance			2		pF
I_{IB}	Input bias current	AINP = AINN = AGND, $I_{IB} = I_{IBP} + I_{IBN}$	–97	–72	–57	µA
R_{IN}	Single-ended input resistance	AINN = AGND		4.75		kΩ
R_{IND}	Differential input resistance			4.9		kΩ
I_{IO}	Input offset current			±10		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–99		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–98		
BW	Input bandwidth(3)			800		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(4)	Resolution: 16 bits, 4.5 V ≤ AVDD ≤ 5.5 V	–4	±1	4	LSB
		Resolution: 16 bits, 3.0 V ≤ AVDD ≤ 3.6 V	–5	±1.5	5	
E_O	Offset error	Initial, at 25°C, AINP = AINN = AGND	–50	±2.5	50	µV
TCE_O	Offset error thermal drift(5)		–1	±0.25	1	µV/°C
E_G	Gain error	Initial, at 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error thermal drift(6)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, at dc		–108		dB
		AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, 10 kHz, 100-mV ripple		–107		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	78	82.5		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	77.5	82.3		dB
THD	Total harmonic distortion	4.5 V ≤ AVDD ≤ 5.5 V, 5 MHz ≤ f_{CLKIN} ≤ 21 MHz, f_{IN} = 1 kHz		–98	–84	dB
		3.0 V ≤ AVDD ≤ 3.6 V, 5 MHz ≤ f_{CLKIN} ≤ 20 MHz, f_{IN} = 1 kHz		–93	–83	
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	83	100		dB

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) The common-mode overvoltage detection level has a typical hysteresis of 90 mV.
(3) This is the –3-dB, second-order roll-off frequency of the integrated differential input amplifier to consider for the antialiasing filter design.
(4) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as a number of LSBs or as a percent of the specified linear full-scale range (FSR).
(5) Offset error drift is calculated using the box method, as described by the following equation:

$$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$$

(6) Gain error drift is calculated using the box method, as described by the following equation:

$$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6$$

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Electrical Characteristics: AMC1306x05 (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –50 mV to 50 mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
CMOS Logic With Schmitt-Trigger						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance			30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
AVDD	High-side supply voltage		3.0	5.0	5.5	V
I_{AVDD}	High-side supply current	3.0 V ≤ AVDD ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ AVDD ≤ 5.5 V		7.2	9.8	
DVDD	Controller-side supply voltage		2.7	3.3	5.5	V
I_{DVDD}	Controller-side supply current	AMC1306Ex, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.1	5.5	mA
		AMC1306Mx, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.3	4.8	
		AMC1306Ex, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		5.0	6.9	
		AMC1306Mx, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.9	6.0	

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7.10 Electrical Characteristics: AMC1306x25

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
$V_{Clipping}$	Differential input voltage before clipping output	AINP – AINN		±320		mV
FSR	Specified linear differential full-scale	AINP – AINN	–250		250	mV
	Absolute common-mode input voltage(1)	(AINP + AINN) / 2 to AGND	–2		AVDD	V
V_{CM}	Operating common-mode input voltage	(AINP + AINN) / 2 to AGND	–0.16		AVDD – 2.1	V
V_{CMov}	Common-mode overvoltage detection level(2)	(AINP + AINN) / 2 to AGND	AVDD – 2			V
C_{IN}	Single-ended input capacitance	AINN = AGND		2		pF
C_{IND}	Differential input capacitance			1		pF
I_{IB}	Input bias current	AINP = AINN = AGND, $I_{IB} = I_{IBP} + I_{IBN}$	–82	–60	–48	µA
R_{IN}	Single-ended input resistance	AINN = AGND		19		kΩ
R_{IND}	Differential input resistance			22		kΩ
I_{IO}	Input offset current			±5		nA
CMTI	Common-mode transient immunity		50	100		kV/µs
CMRR	Common-mode rejection ratio	AINP = AINN, f_{IN} = 0 Hz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–95		dB
		AINP = AINN, f_{IN} from 0.1 Hz to 50 kHz, $V_{CM\ min} \le V_{IN} \le V_{CM\ max}$		–95		
BW	Input bandwidth(3)			900		kHz
DC ACCURACY						
DNL	Differential nonlinearity	Resolution: 16 bits	–0.99		0.99	LSB
INL	Integral nonlinearity(4)	Resolution: 16 bits	–4	±1	4	LSB
E_O	Offset error	Initial, at 25°C, AINP = AINN = AGND	–100	±4.5	100	µV
TCE_O	Offset error thermal drift(5)		–1	±0.15	1	µV/°C
E_G	Gain error	Initial, at 25°C	–0.2%	±0.005%	0.2%	
TCE_G	Gain error thermal drift(6)		–40	±20	40	ppm/°C
PSRR	Power-supply rejection ratio	AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, at dc		–103		dB
		AINP = AINN = AGND, 3.0 V ≤ AVDD ≤ 5.5 V, 10 kHz, 100-mV ripple		–92		
AC ACCURACY						
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz	82	86		dB
SINAD	Signal-to-noise + distortion	f_{IN} = 1 kHz	81.9	85.7		dB
THD	Total harmonic distortion	4.5 V ≤ AVDD ≤ 5.5 V, 5 MHz ≤ f_{CLKIN} ≤ 21 MHz, f_{IN} = 1 kHz		–98	–86	dB
		3.0 V ≤ AVDD ≤ 3.6 V, 5 MHz ≤ f_{CLKIN} ≤ 20 MHz, f_{IN} = 1 kHz		–93	–85	
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz	83	100		dB

(1) Steady-state voltage supported by the device in case of a system failure; see the specified common-mode input voltage V_{CM} for normal operation. Adhere to the analog input voltage range as specified in the *Absolute Maximum Ratings* table.
(2) The common-mode overvoltage detection level has a typical hysteresis of 90 mV.
(3) This parameter is the –3-dB, second-order, roll-off frequency of the integrated differential input amplifier to consider for antialiasing filter designs.
(4) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.
(5) Offset error drift is calculated using the box method, as described by the following equation: $$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}.$$
(6) Gain error drift is calculated using the box method, as described by the following equation: $$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange}\right) \times 10^6.$$

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Electrical Characteristics: AMC1306x25 (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, AVDD = 3.0 V to 5.5 V, DVDD = 2.7 V to 5.5 V, AINP = –250 mV to 250 mV, AINN = AGND, and sinc^3 filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
CMOS Logic with Schmitt-trigger						
I_{IN}	Input current	DGND ≤ V_{IN} ≤ DVDD	0		7	µA
C_{IN}	Input capacitance			4		pF
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × DVDD	V
C_{LOAD}	Output load capacitance	f_{CLKIN} = 20 MHz		30		pF
V_{OH}	High-level output voltage	I_{OH} = –20 µA	DVDD – 0.1			V
		I_{OH} = –4 mA	DVDD – 0.4			
V_{OL}	Low-level output voltage	I_{OL} = 20 µA			0.1	V
		I_{OL} = 4 mA			0.4	
POWER SUPPLY						
AVDD	High-side supply voltage		3.0	5.0	5.5	V
I_{AVDD}	High-side supply current	3.0 V ≤ AVDD ≤ 3.6 V		6.3	8.5	mA
		4.5 V ≤ AVDD ≤ 5.5 V		7.2	9.8	
DVDD	Controller-side supply voltage		2.7	3.3	5.5	V
I_{DVDD}	Controller-side supply current	AMC1306Ex, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		4.1	5.5	mA
		AMC1306Mx, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		3.3	4.8	
		AMC1306Ex, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		5.0	6.9	
		AMC1306Mx, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		3.9	6.0	

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7.11 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	4.5 V ≤ AVDD ≤ 5.5 V	5		21	MHz
		3.0 V ≤ AVDD ≤ 5.5 V	5		20	
t_{CLKIN}	CLKIN clock period	4.5 V ≤ AVDD ≤ 5.5 V	47.6		200	ns
		3.0 V ≤ AVDD ≤ 5.5 V	50		200	
t_{HIGH}	CLKIN clock high time		20	25	120	ns
t_{LOW}	CLKIN clock low time		20	25	120	ns
t_H	DOUT hold time after rising edge of CLKIN	AMC1306Mx(1), C_{LOAD} = 15 pF	3.5			ns
t_D	Rising edge of CLKIN to DOUT valid delay	AMC1306Mx(1), C_{LOAD} = 15 pF			15	ns
t_r	DOUT rise time	10% to 90%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		10% to 90%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	
t_f	DOUT fall time	90% to 10%, 2.7 V ≤ DVDD ≤ 3.6 V, C_{LOAD} = 15 pF		0.8	3.5	ns
		90% to 10%, 4.5 V ≤ DVDD ≤ 5.5 V, C_{LOAD} = 15 pF		1.8	3.9	
t_{ISTART}	Interface startup time	DVDD at 2.7 V (min) to DOUT valid with AVDD ≥ 3.0 V	32		32	CLKIN cycles
t_{ASTART}	Analog startup time	AVDD step to 3.0 V with DVDD ≥ 2.7 V, 0.1% settling		0.5		ms

(1) The output of the Manchester encoded versions of the AMC1306Ex can change with every edge of CLKIN with a typical delay of 6 ns; see the *Manchester Coding Feature* section for additional details.

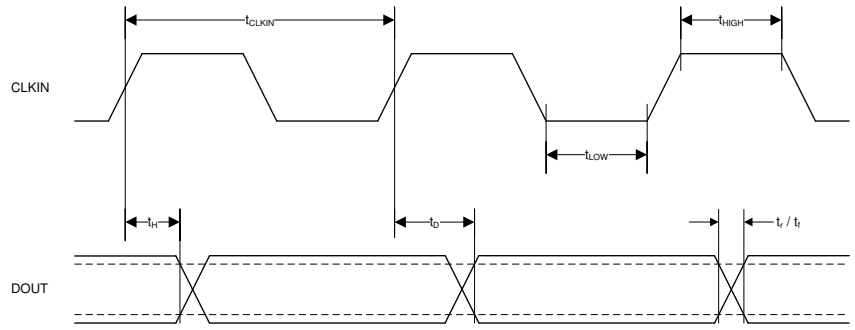

Figure 1. Digital Interface Timing

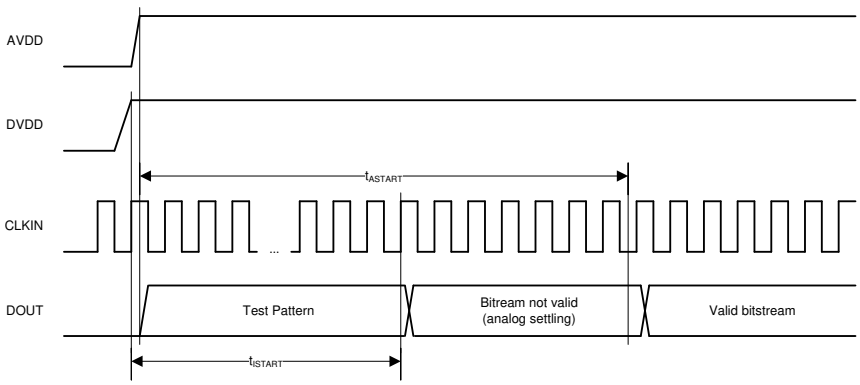

Figure 2. Device Startup Timing

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7.12 Insulation Characteristics Curves

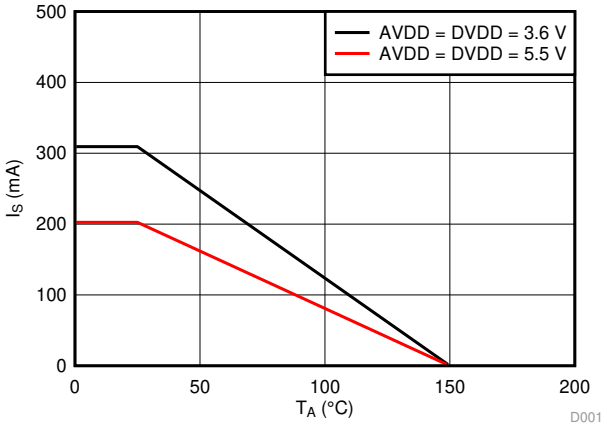


Figure 3. Thermal Derating Curve for Safety-Limiting Current per VDE

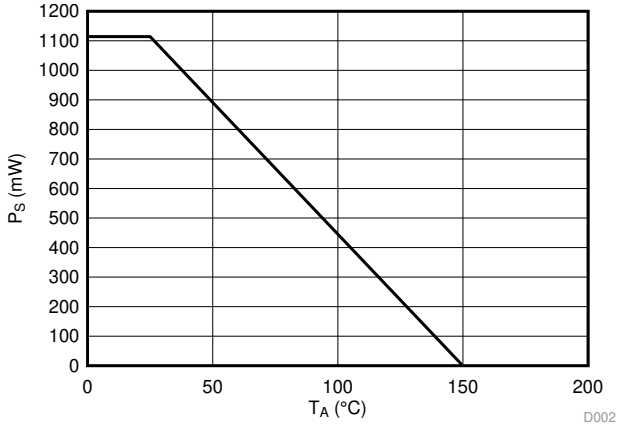
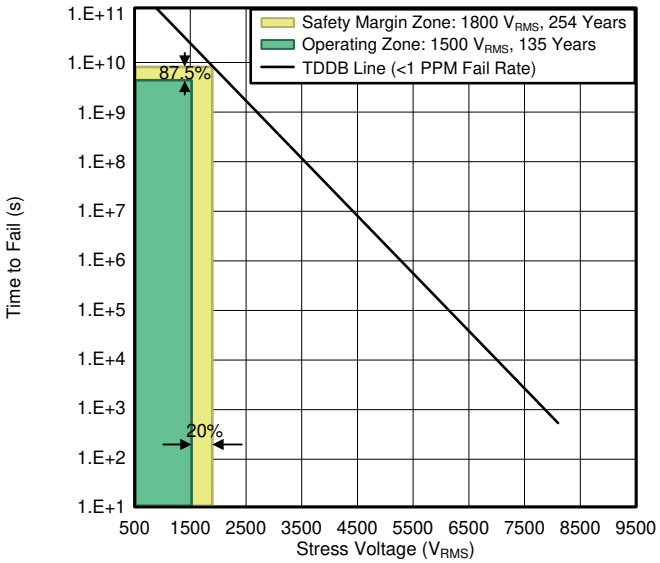


Figure 4. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

Figure 5. Reinforced Isolation Capacitor Lifetime Projection

7.13 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

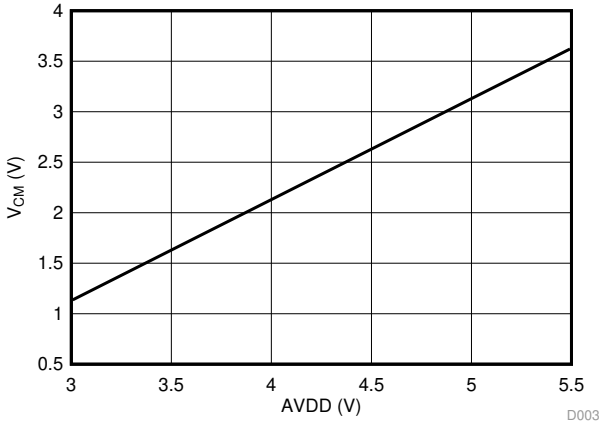


Figure 6. Maximum Operating Common-Mode Input Voltage vs High-Side Supply Voltage

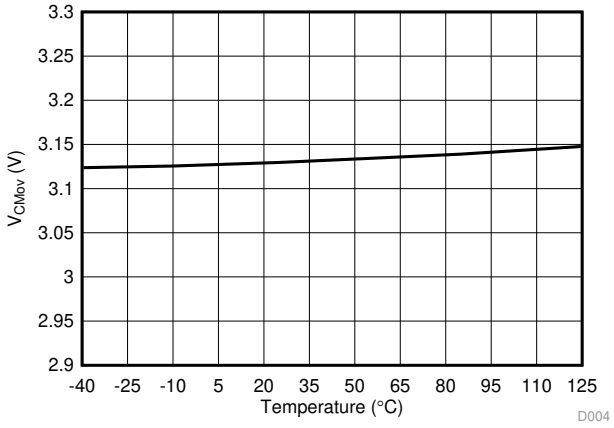


Figure 7. Common-Mode Overvoltage Detection Level vs Temperature

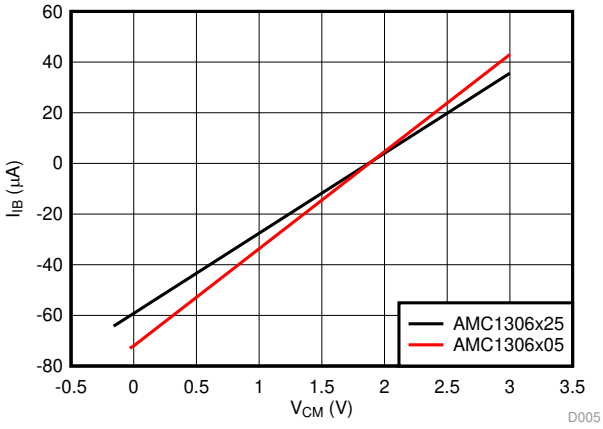


Figure 8. Input Bias Current vs Common-Mode Input Voltage

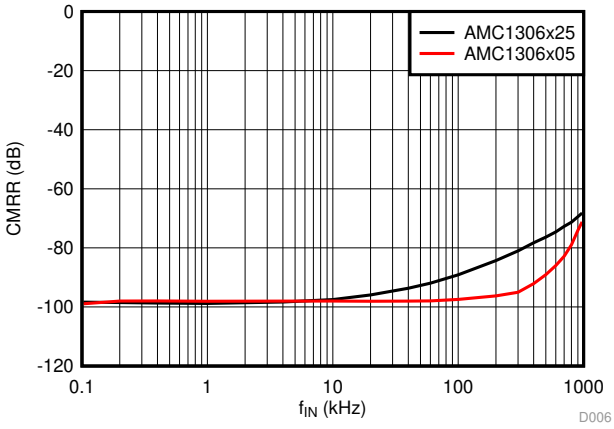


Figure 9. Common-Mode Rejection Ratio vs Input Signal Frequency

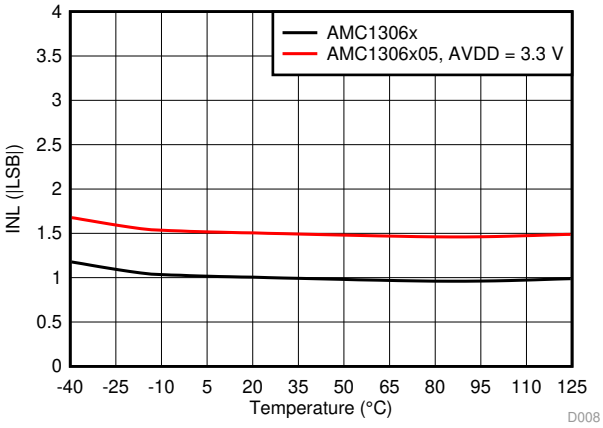


Figure 10. Integral Nonlinearity vs Temperature

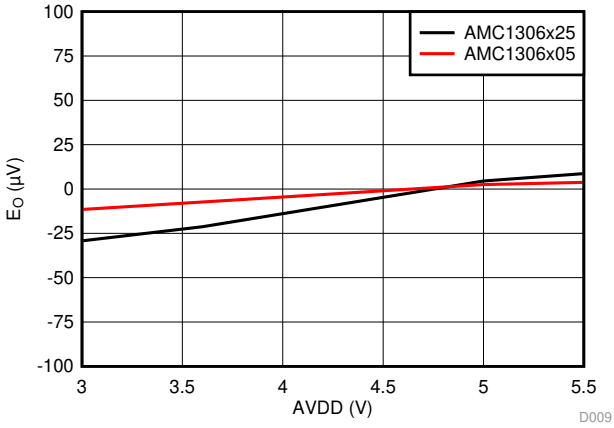


Figure 11. Offset Error vs High-Side Supply Voltage

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Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

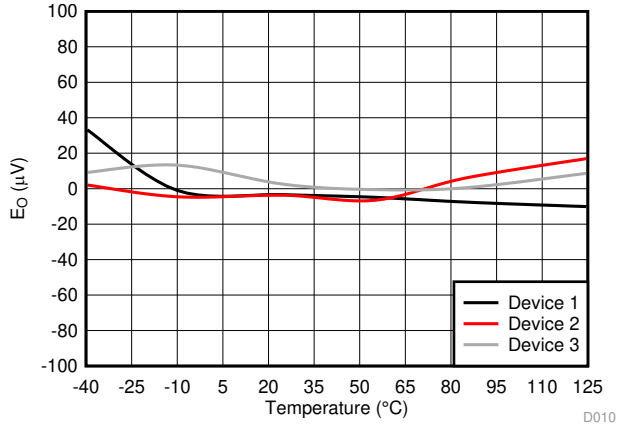

Figure 12. Offset Error vs Temperature

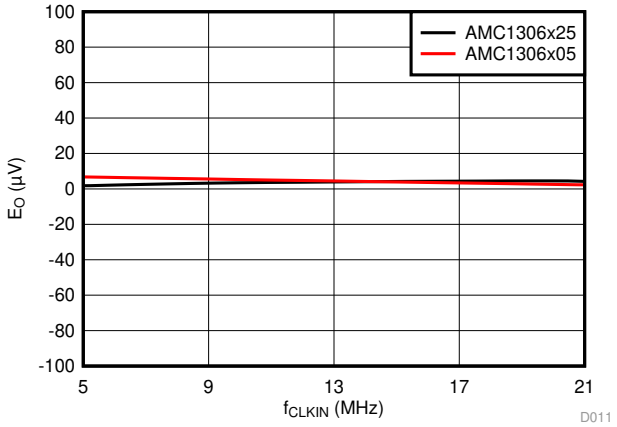

Figure 13. Offset Error vs Clock Frequency

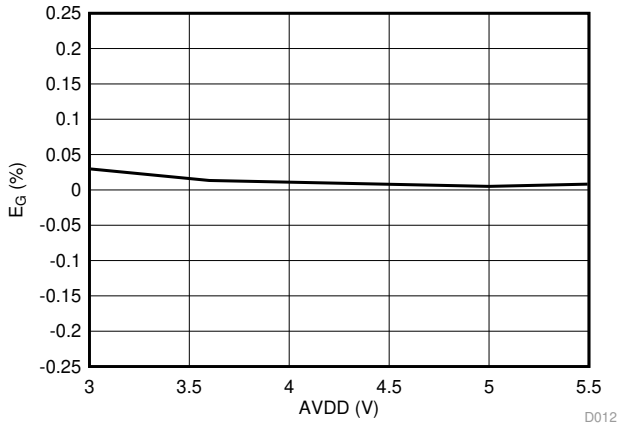

Figure 14. Gain Error vs High-Side Supply Voltage

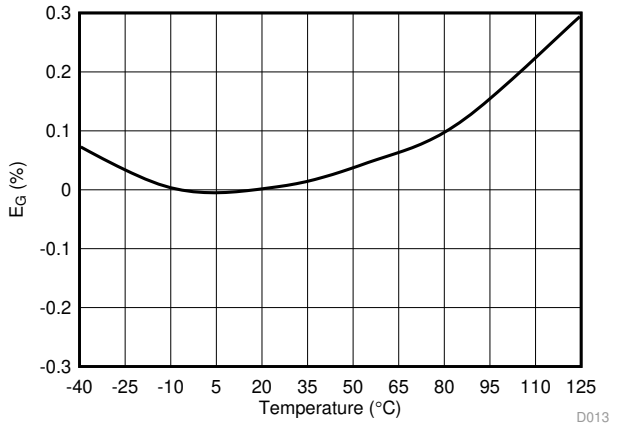

Figure 15. Gain Error vs Temperature

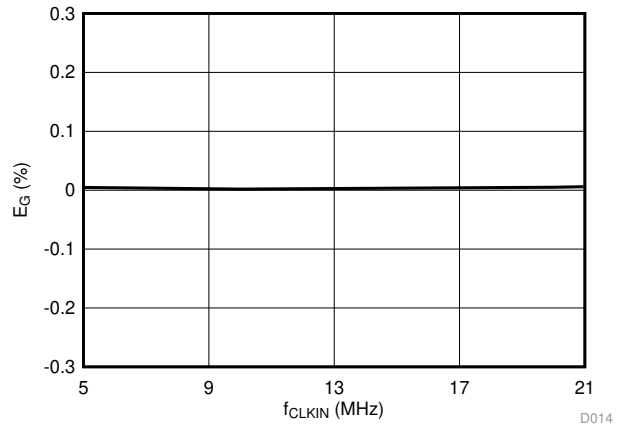

Figure 16. Gain Error vs Clock Frequency

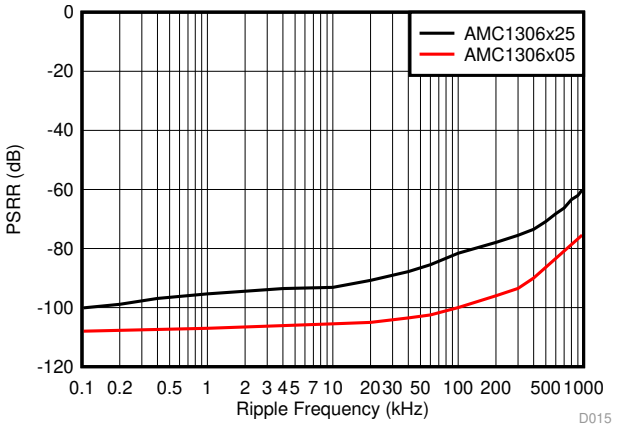

Figure 17. Power-Supply Rejection Ratio vs Ripple Frequency

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Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

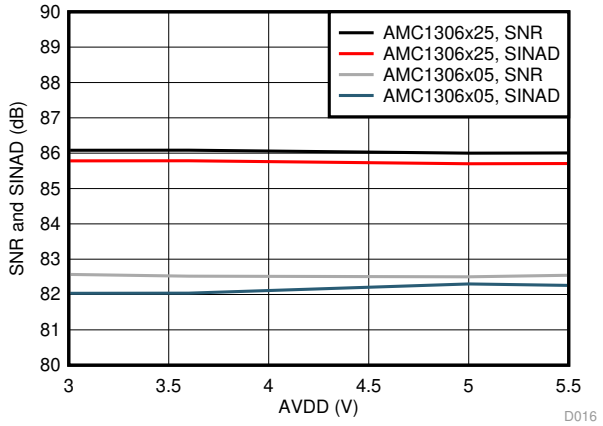

Figure 18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs High-Side Supply Voltage

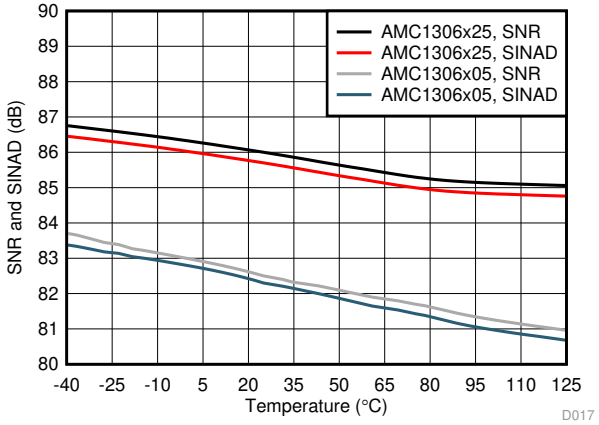

Figure 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

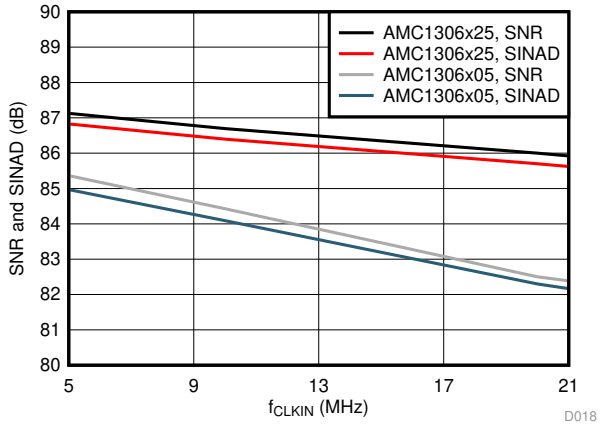

Figure 20. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

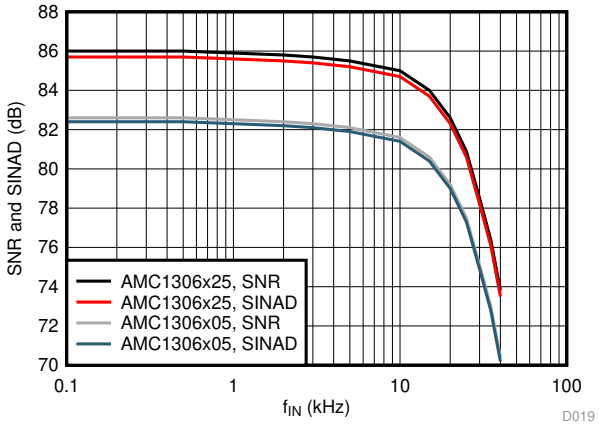

Figure 21. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

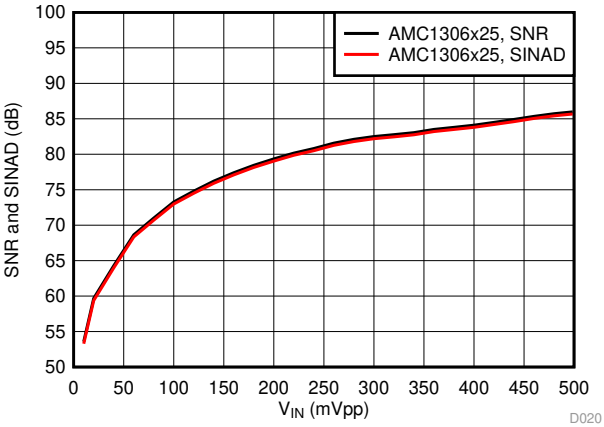

Figure 22. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

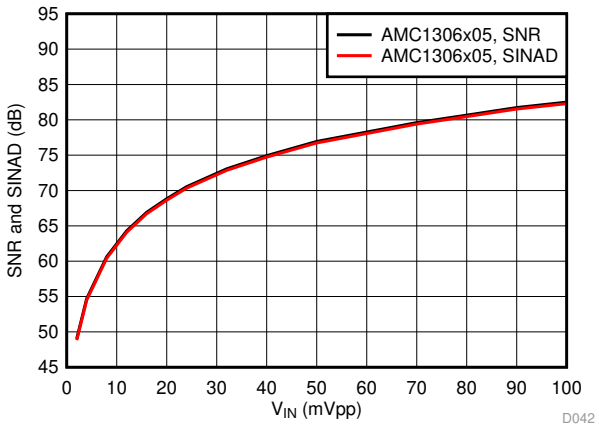

Figure 23. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

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Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

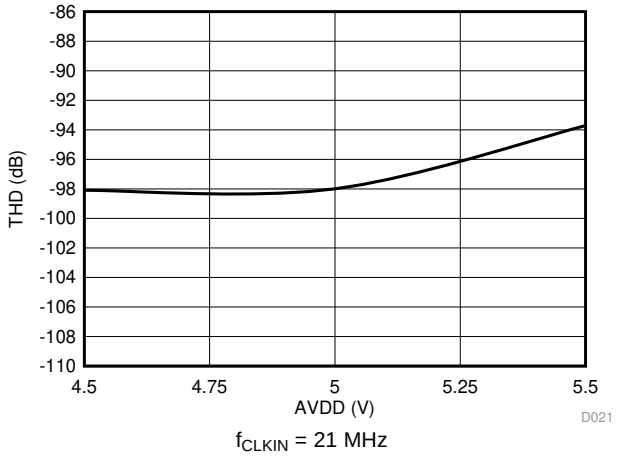

Figure 24. Total Harmonic Distortion vs High-Side Supply Voltage (5 V, nom)

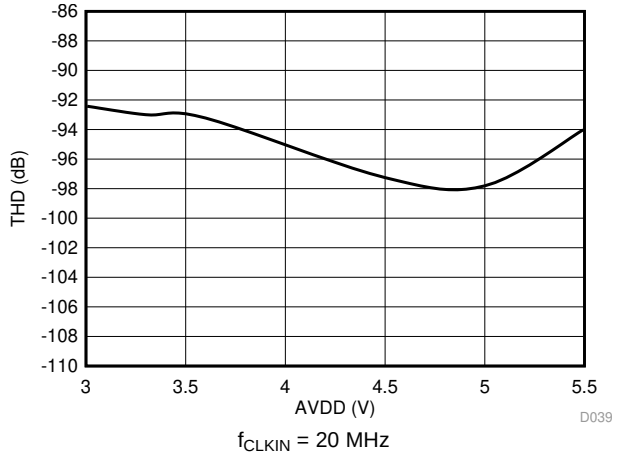

Figure 25. Total Harmonic Distortion vs High-Side Supply Voltage (3.3 V, nom)

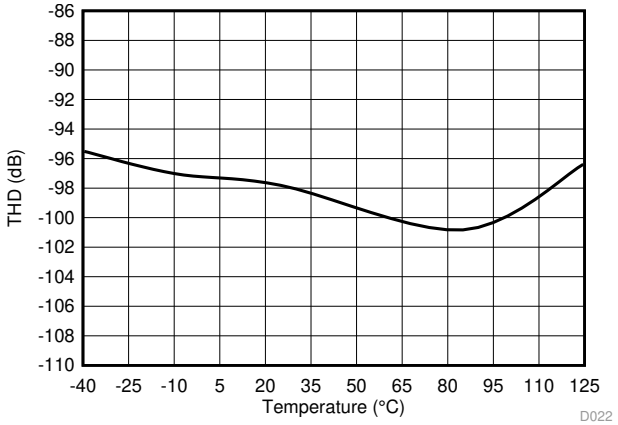

Figure 26. Total Harmonic Distortion vs Temperature

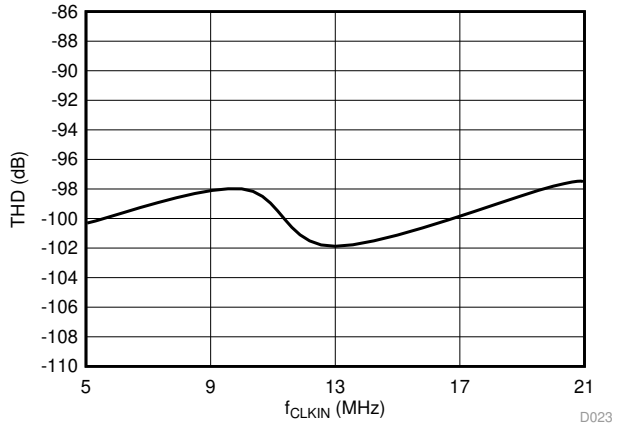

Figure 27. Total Harmonic Distortion vs Clock Frequency

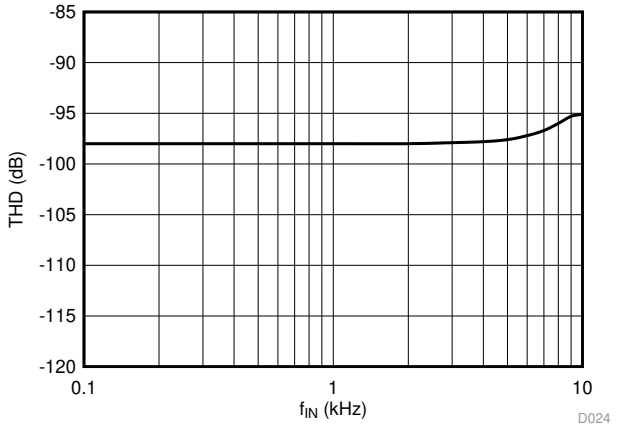

Figure 28. Total Harmonic Distortion vs Input Signal Frequency

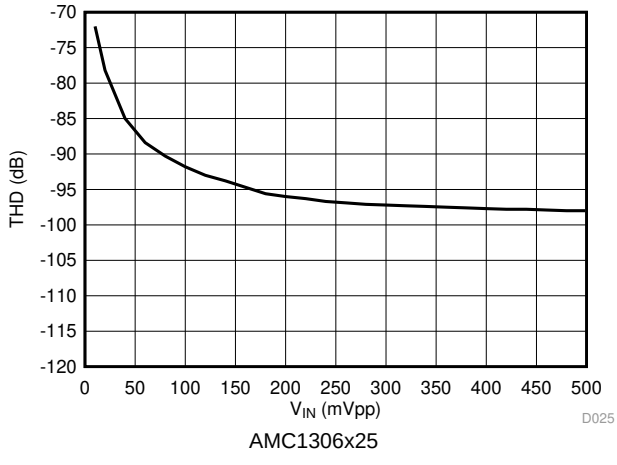

Figure 29. Total Harmonic Distortion vs Input Signal Amplitude

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Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

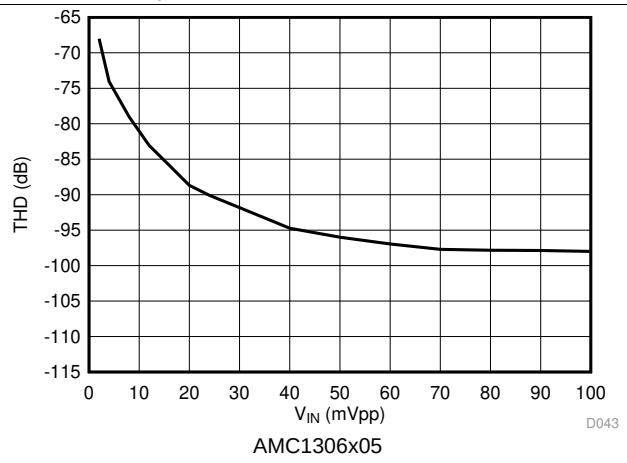

Figure 30. Total Harmonic Distortion vs Input Signal Amplitude

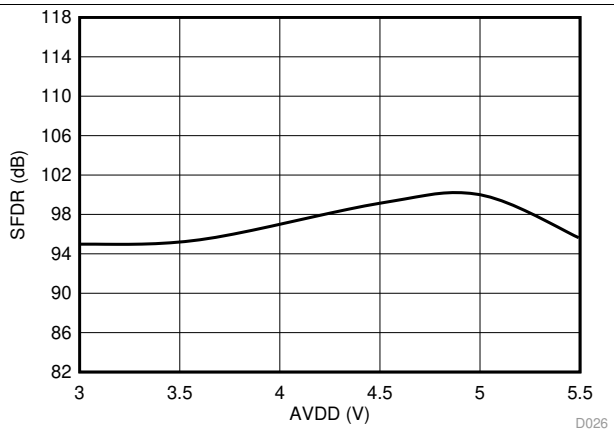

Figure 31. Spurious-Free Dynamic Range vs High-Side Supply Voltage

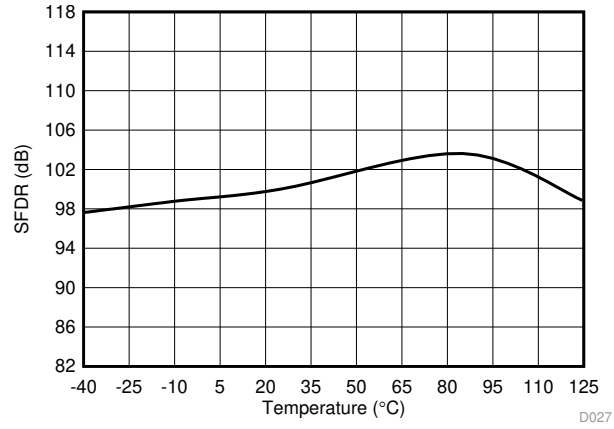

Figure 32. Spurious-Free Dynamic Range vs Temperature

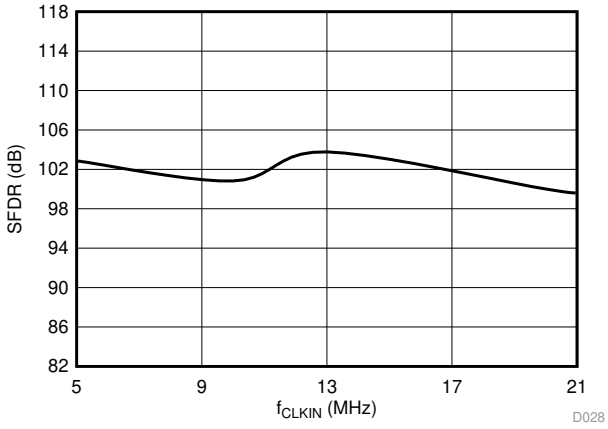

Figure 33. Spurious-Free Dynamic Range vs Clock Frequency

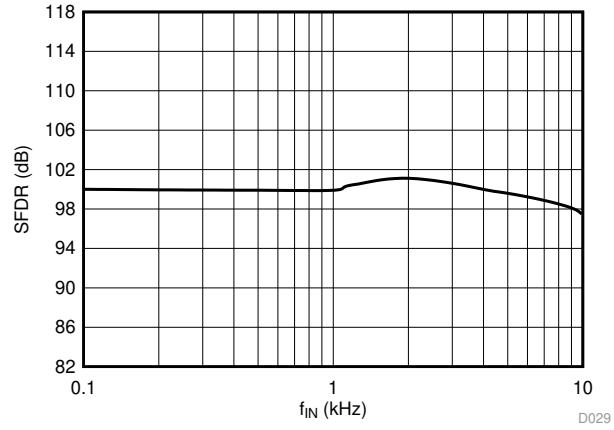

Figure 34. Spurious-Free Dynamic Range vs Input Signal Frequency

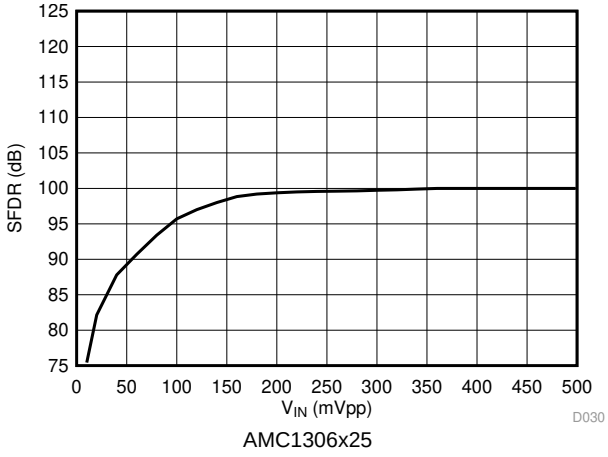

Figure 35. Spurious-Free Dynamic Range vs Input Signal Amplitude

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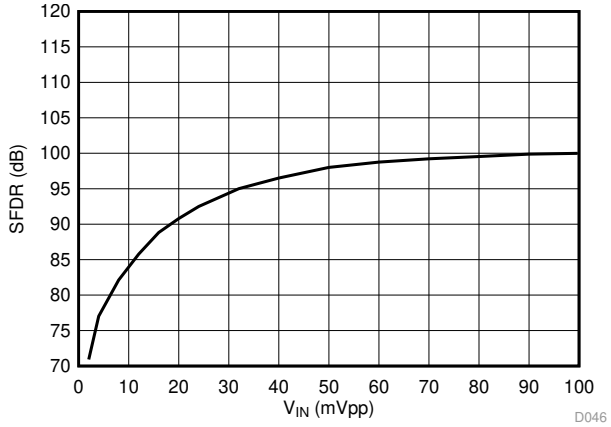
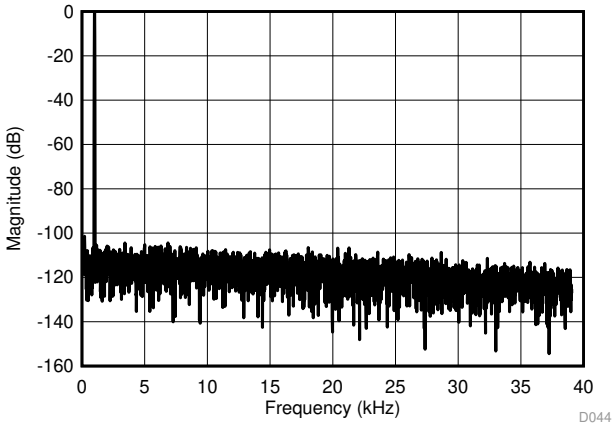
Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)



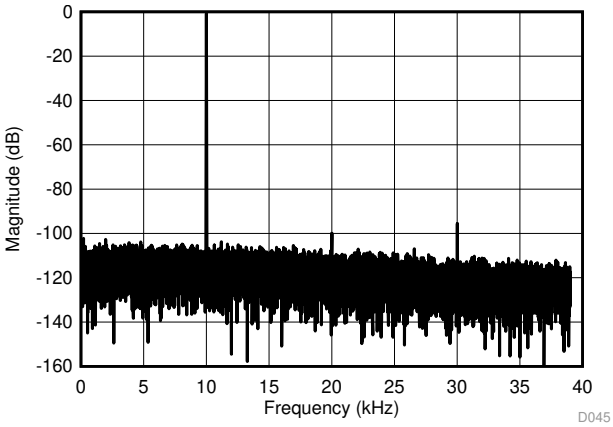
AMC1306x05

Figure 36. Spurious-Free Dynamic Range vs Input Signal Amplitude



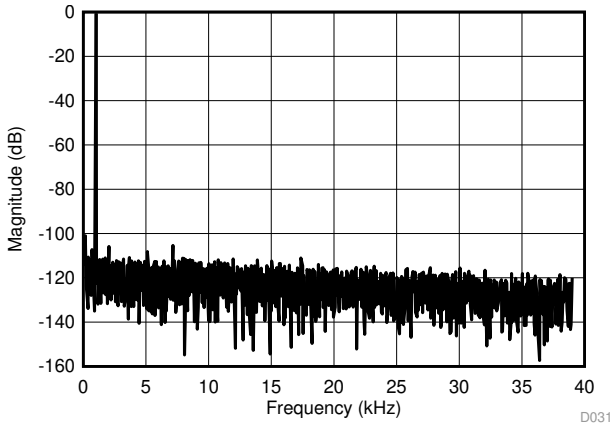
AMC1306x05, 4096-point FFT, V_{IN} = 100 mV_{PP}

Figure 37. Frequency Spectrum with 1-kHz Input Signal



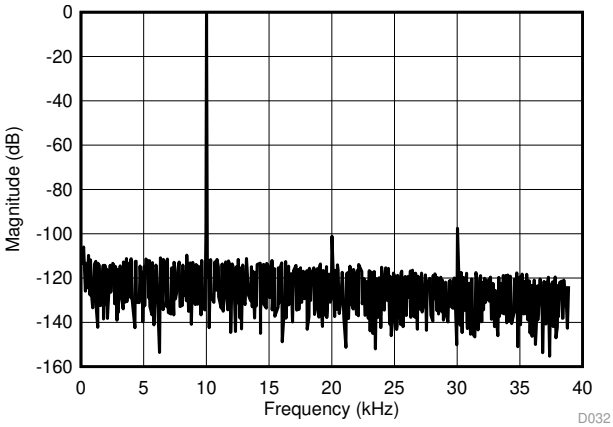
AMC1306x05, 4096-point FFT, V_{IN} = 100 mV_{PP}

Figure 38. Frequency Spectrum with 10-kHz Input Signal



AMC1306x25, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 39. Frequency Spectrum with 1-kHz Input Signal



AMC1306x25, 4096-point FFT, V_{IN} = 500 mV_{PP}

Figure 40. Frequency Spectrum with 10-kHz Input Signal

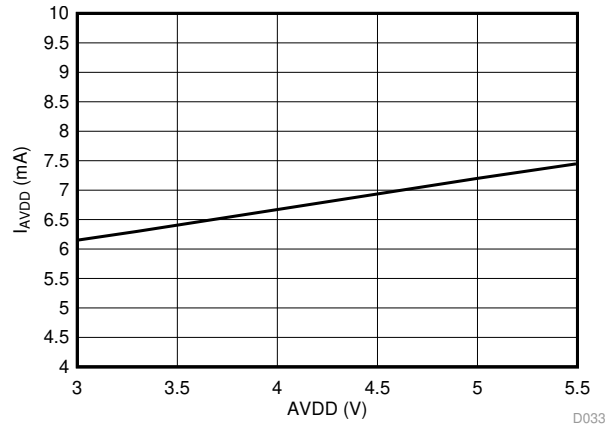


Figure 41. High-Side Supply Current vs High-Side Supply Voltage

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Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, AINP = –50 mV to 50 mV (AMC1306x05) or –250 mV to 250 mV (AMC1306x25), AINN = AGND, f_{CLKIN} = 20 MHz, and sinc^3 filter with OSR = 256 (unless otherwise noted)

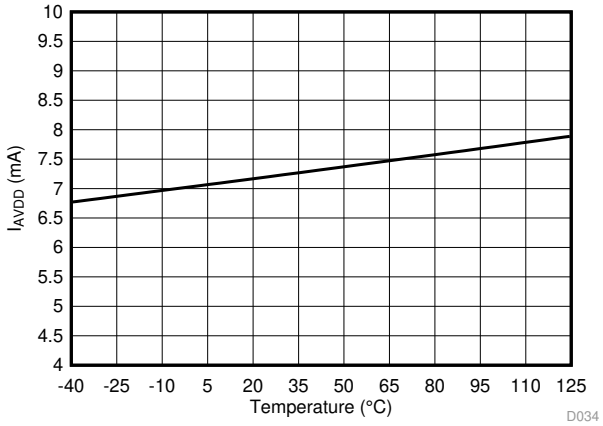

Figure 42. High-Side Supply Current vs Temperature

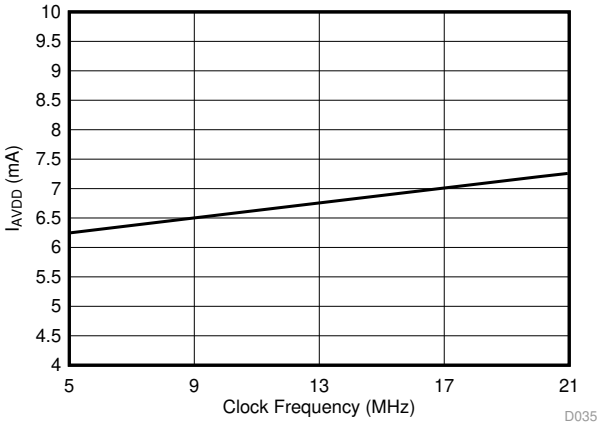

Figure 43. High-Side Supply Current vs Clock Frequency

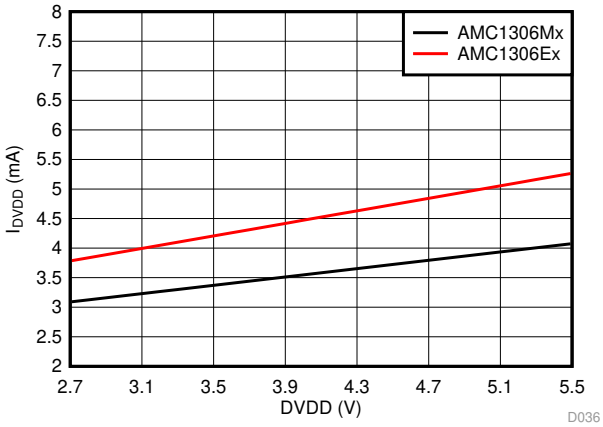

Figure 44. Controller-Side Supply Current vs Controller-Side Supply Voltage

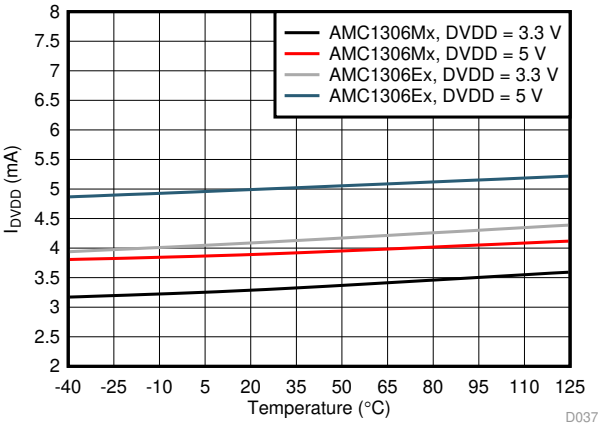

Figure 45. Controller-Side Supply Current vs Temperature

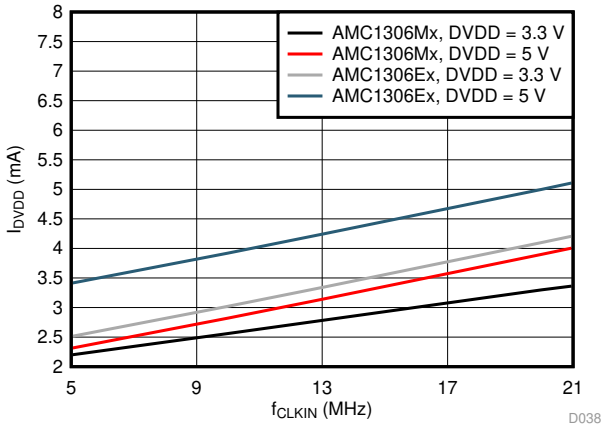

Figure 46. Controller-Side Supply Current vs Clock Frequency

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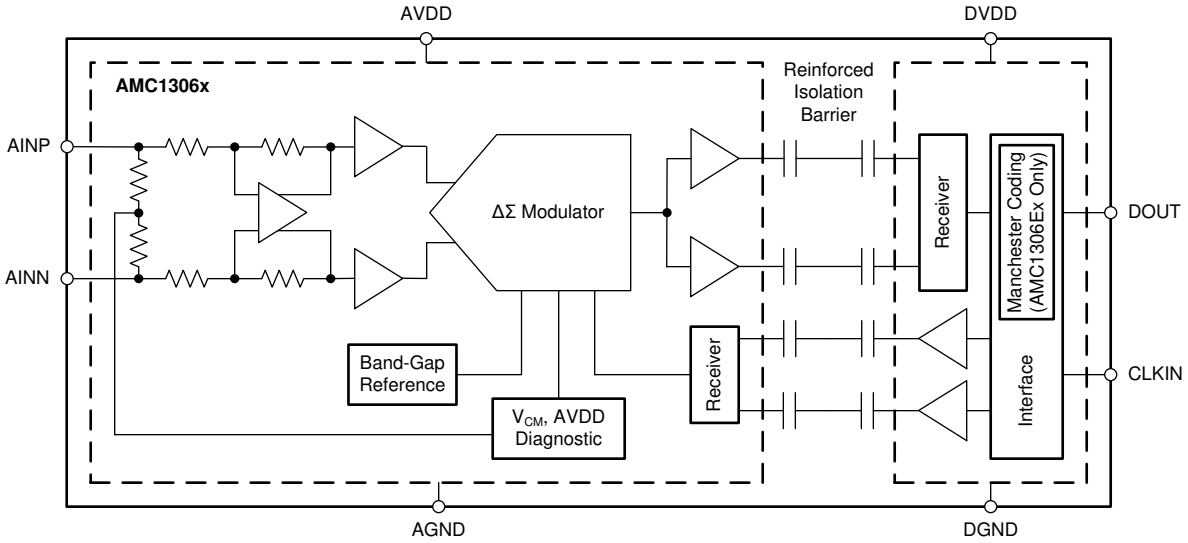
8 Detailed Description

8.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1306 is a fully-differential amplifier feeding the switched-capacitor input of a second-order, delta-sigma (ΔΣ) modulator stage that digitizes the input signal into a 1-bit output stream. The isolated data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 5 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The *Functional Block Diagram* section shows a detailed block diagram of the AMC1306. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The silicon-dioxide (SiO_2) based capacitive isolation barrier supports a high level of magnetic field immunity as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report, available for download at www.ti.com. The external clock input simplifies the synchronization of multiple current-sensing channels on the system level. The extended frequency range of up to 21 MHz supports higher performance levels compared to the other solutions available on the market.

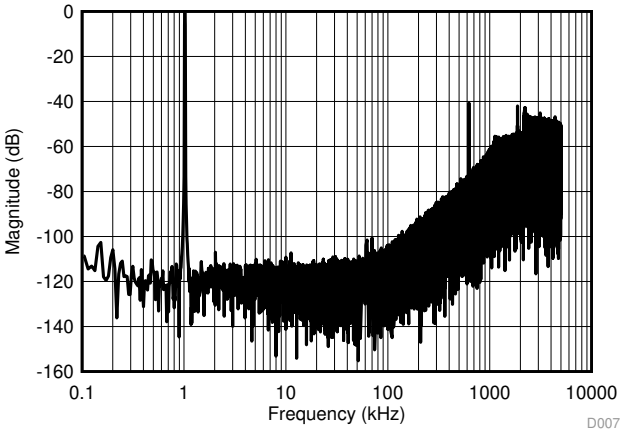
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The AMC1306 incorporates front-end circuitry that contains a differential amplifier and a sampling stage, followed by a ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 for devices with a specified input voltage range of ±250 mV (this value is for the AMC1306x25), or to a factor of 20 in devices with a ±50-mV input voltage range (for the AMC1306x05), resulting in a differential input impedance of 4.9 kΩ (for the AMC1306x05) or 22 kΩ (for the AMC1306x25). For reduced offset and offset drift, the differential amplifier is chopper-stabilized with the switching frequency set at f_{CLKIN} / 32. The switching frequency generates a spur as shown in Figure 47.



$sinc^3$ filter, OSR = 2, f_{CLKIN} = 20 MHz, f_{IN} = 1 kHz

Figure 47. Quantization Noise Shaping

Consider the input impedance of the AMC1306 in designs with high-impedance signal sources that can cause degradation of gain and offset specifications. The importance of this effect, however, depends on the desired system performance. Additionally, the input bias current caused by the internal common-mode voltage at the output of the differential amplifier is dependent on the actual amplitude of the input signal; see the *Isolated Voltage Sensing* section for more details on reducing these effects.

There are two restrictions on the analog input signals (AINP and AINN). First, if the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on. In addition, the linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ±250 mV (for the AMC1306x25) or ±50 mV (for the AMC1306x05), and within the specified input common-mode range.

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Feature Description (continued)

8.3.2 Modulator

The modulator implemented in the AMC1306 is a second-order, switched-capacitor, feed-forward ΔΣ modulator, such as the one conceptualized in Figure 48. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is differentiated with the input signal V_{IN} and the output of the first integrator V_2. Depending on the polarity of the resulting voltage V_4, the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5, causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

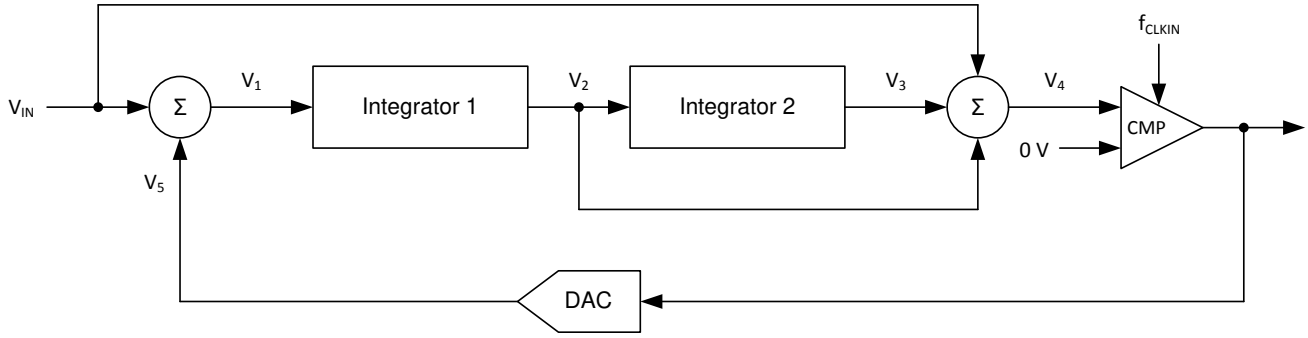

Figure 48. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 48. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families TMS320F2807x and TMS320F2837x offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1306 family. Also, SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters for a simple system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the AMC1210 (a four-channel digital sinc-filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

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Feature Description (continued)

8.3.3 Isolation Channel Signal Transmission

The AMC1306 device uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. The transmitter modulates the bitstream at TX IN in Figure 49 with an internally-generated, 480-MHz carrier across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the CMTI performance and reduces the radiated emissions caused by the high-frequency carrier. The block diagram of an isolation channel integrated in the AMC1306 is shown in Figure 49.

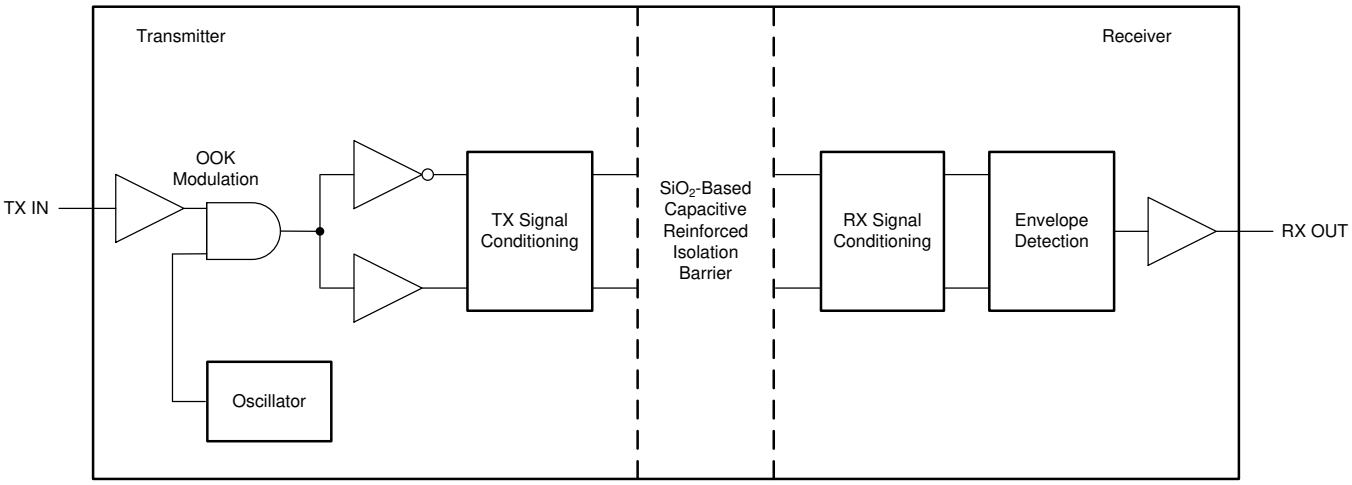

Figure 49. Block Diagram of an Isolation Channel

Figure 50 shows the concept of the on-off keying scheme.

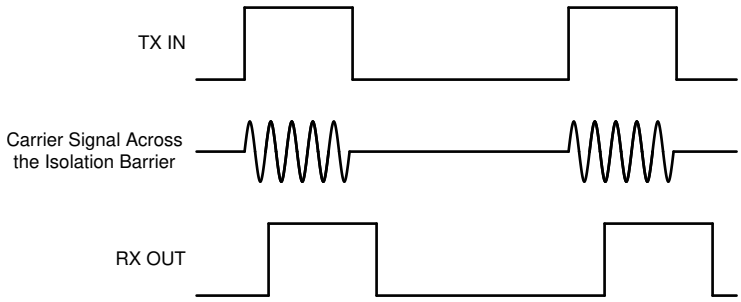

Figure 50. OOK-Based Modulation Scheme

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Feature Description (continued)

8.3.4 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 250 mV (for the AMC1306x25) or 50 mV (for the AMC1306x05) produces a stream of ones and zeros that are high 89.06% of the time. With 16 bits of resolution, that percentage ideally corresponds to the code 58368. A differential input of –250 mV (–50 mV for the AMC1306x05) produces a stream of ones and zeros that are high 10.94% of the time and ideally results in code 7168 with 16-bit resolution. These input voltages are also the specified linear ranges of the different AMC1306 versions with performance as specified in this document. If the input voltage value exceeds these ranges, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV (–64 mV for the AMC1306x05) or with a stream of only ones with an input greater than or equal to 320 mV (64 mV for the AMC1306x05). In this case, however, the AMC1306 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the *Fail-Safe Output* section for more details). The input voltage versus the output modulator signal is shown in Figure 51.

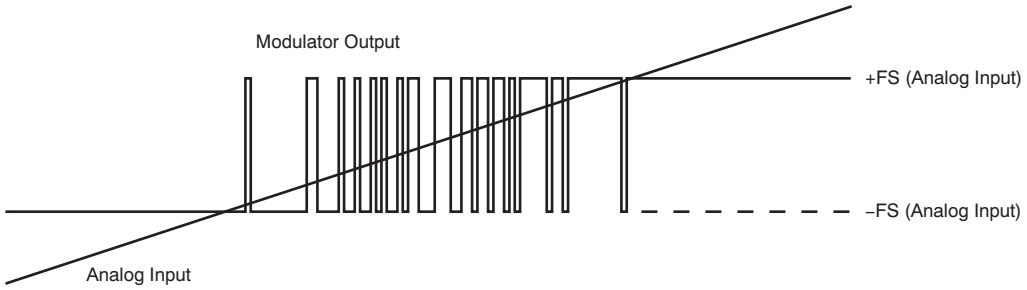

Figure 51. Analog Input versus the AMC1306 Modulator Output

The density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the *Output Behavior in Case of a Full-Scale Input* section) can be calculated using Equation 1:

$$\frac{V_{IN} + V_{Clipping}}{2 \times V_{Clipping}} \quad (1)$$

The AMC1306 system clock is provided externally at the CLKIN pin. For more details, see the *Switching Characteristics* table and the *Manchester Coding Feature* section.

8.3.5 Manchester Coding Feature

The AMC1306Ex offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. A Manchester coded bitstream is free of dc components. The Manchester coding combines the clock and data information using exclusive or (XOR) logical operation and results in a bitstream as shown in Figure 52. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN.

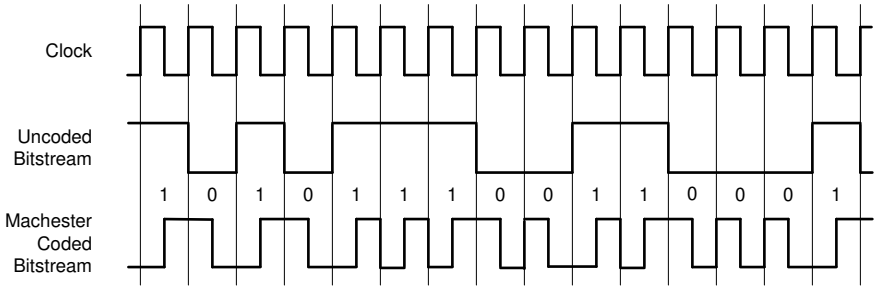

Figure 52. Manchester Coded Output of the AMC1306Ex

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8.4 Device Functional Modes

8.4.1 Fail-Safe Output

In the case of a missing high-side supply voltage AVDD, the output of a ΔΣ modulator is not defined and can cause a system malfunction. In systems with high safety requirements, this behavior is not acceptable. Therefore, the AMC1306 implements a fail-safe output function that ensures that the output DOUT of the device offers a steady-state bitstream of logic 0's in case of a missing AVDD, as shown in Figure 53.

Additionally, if the common-mode voltage of the input reaches or exceeds the specified common-mode overvoltage detection level V_{CMov} as defined in the *Electrical Characteristics* table, the AMC1306 offers a steady-state bitstream of logic 1's at the output DOUT, as also shown in Figure 53.

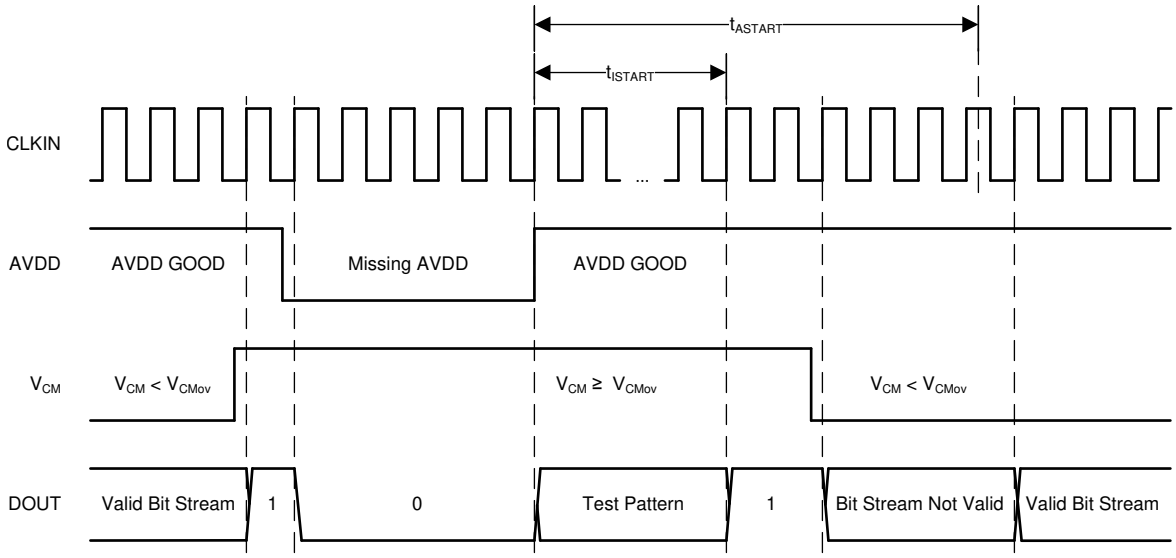

Figure 53. Fail-Safe Output of the AMC1306

8.4.2 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1306 (that is, $V_{IN} \geq V_{Clipping}$), the device generates a single one or zero every 128 bits at DOUT, depending on the actual polarity of the signal being sensed, as shown in Figure 54. In this way, differentiating between a missing AVDD and a full-scale input signal is possible on the system level.

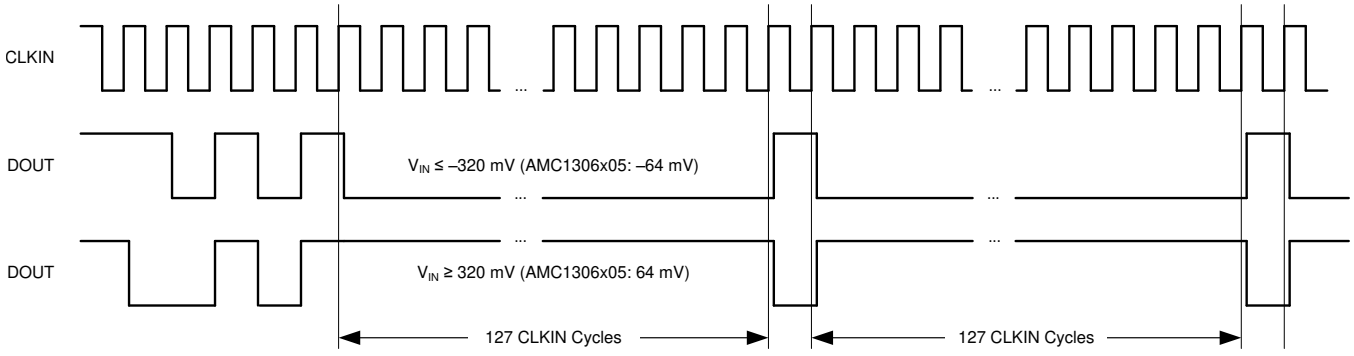

Figure 54. Overrange Output of the AMC1306

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 2:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 55 shows the ENOB of the AMC1306 with different oversampling ratios. In this document, this number is calculated from the SINAD by using Equation 3:

$$SINAD = 1.76\ dB + 6.02\ dB \times ENOB \quad (3)$$

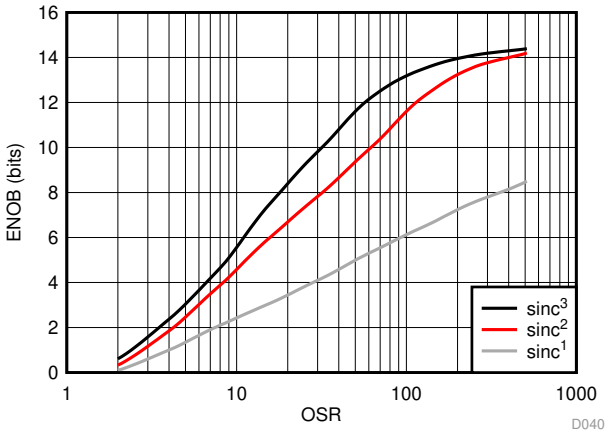

Figure 55. Measured Effective Number of Bits versus Oversampling Ratio

An example code for implementing a sinc^3 filter in an FPGA is discussed in the *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.

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9.2 Typical Applications

9.2.1 Frequency Inverter Application

Isolated ΔΣ modulators are being widely used in frequency inverter designs because of their high ac and dc performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), electrical and hybrid electrical vehicles, and other industrial applications.

Figure 56 shows a simplified schematics of the AMC1306Mx in a typical frequency inverter application as used in industrial motor drives with shunt resistors (R_{SHUNT}) used for current sensing. Depending on the system design, either all three or only two motor phase currents are sensed.

The Manchester coded bitstream output of the AMC1306Ex minimizes the wiring efforts of the connection between the power board and the control board; see Figure 57. This bitstream output also allows the clock to be generated locally on the power board without the having to adjust the propagation delay time of each DOUT connection to fulfill the setup and hold time requirements of the microcontroller.

In both examples, an additional fourth AMC1306 is used to support isolated voltage sensing of the dc link. This high voltage is reduced using a high-impedance resistive divider and is sensed by the device across a smaller resistor. The value of this resistor can degrade the performance of the measurement, as described in the *Isolated Voltage Sensing* section.

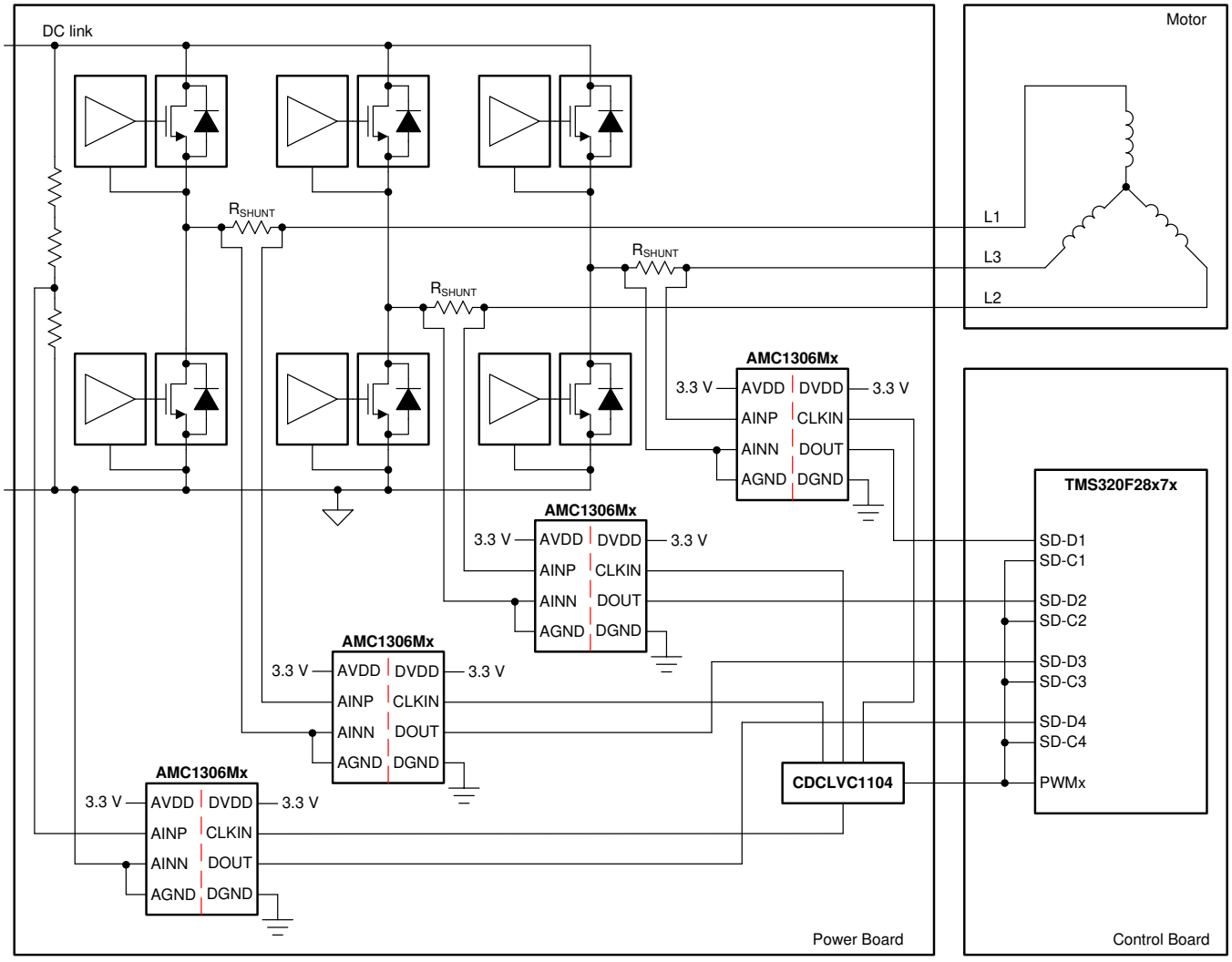

Figure 56. The AMC1306Mx in a Frequency Inverter Application

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Typical Applications (continued)

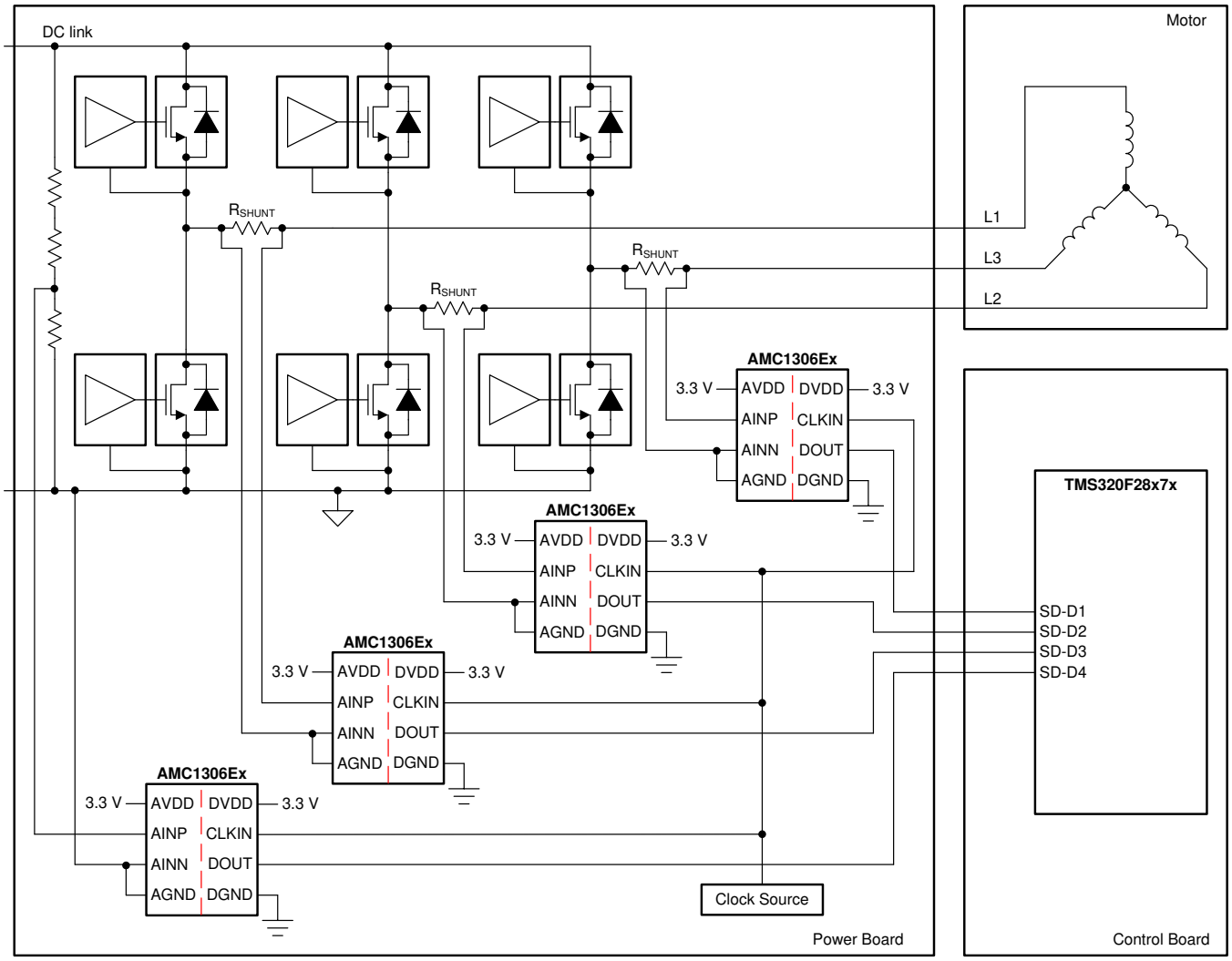

Figure 57. The AMC1306Ex in a Frequency Inverter Application

9.2.1.1 Design Requirements

Table 1 lists the parameters for the typical application in the *Frequency Inverter Application* section.

Table 1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	±250 mV (maximum)

9.2.1.2 Detailed Design Procedure

The high-side power supply (AVDD) for the AMC1306 device is derived from the power supply of the upper gate driver. Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (AGND) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC1306 (AINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and AGND is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $|V_{SHUNT}| \leq |V_{Clipping}|$

The typically recommended RC filter in front of a ΔΣ modulator to improve signal-to-noise performance of the signal path is not required for the AMC1306. By design, the input bandwidth of the analog front-end of the device is limited as specified in the *Electrical Characteristics* table.

For modulator output bitstream filtering, a device from TI's TMS320F2807x family of low-cost microcontrollers (MCUs) or TMS320F2837x family of dual-core MCUs is recommended. These families support up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.

9.2.1.3 Application Curve

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on the filter order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, filter types other than $sinc^3$ can be a better choice; an alternative is the $sinc^2$ filter. Figure 58 compares the settling times of different filter orders.

The delay time of the sinc filter with a continuous signal is half of the settling time.

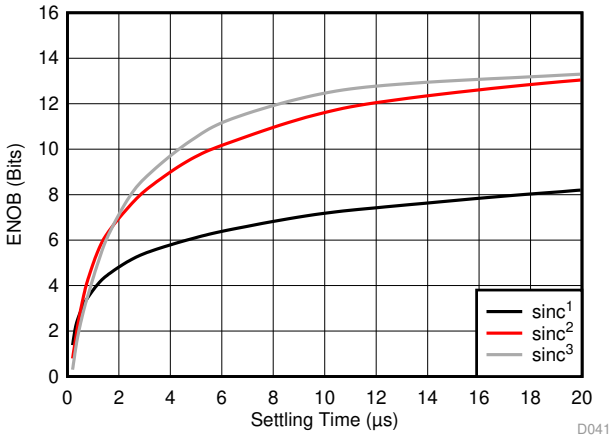

Figure 58. Measured Effective Number of Bits versus Settling Time

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9.2.2 Isolated Voltage Sensing

The AMC1306 is optimized for usage in current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the affect of the (usually higher) impedance of the resistor used in this case is considered.

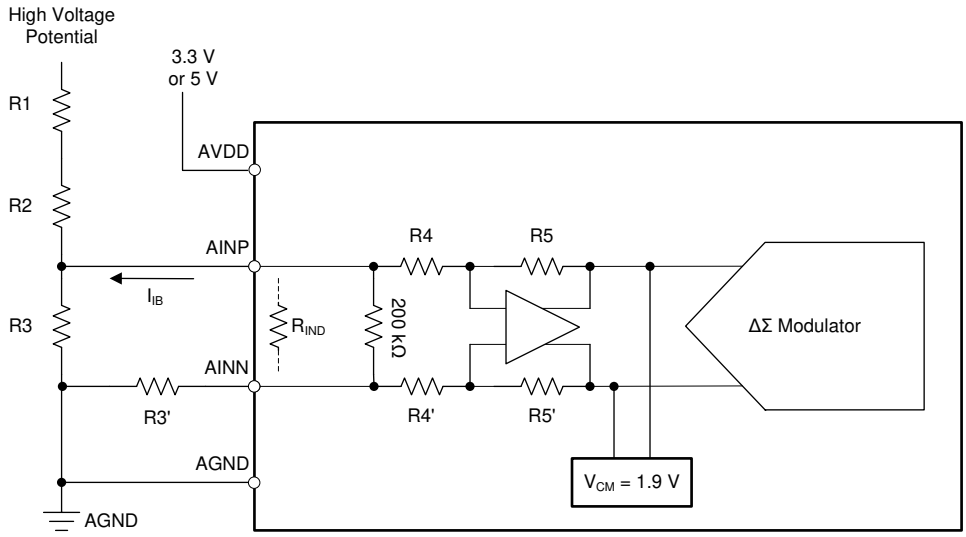

Figure 59. Using the AMC1306 for Isolated Voltage Sensing

9.2.2.1 Design Requirements

Figure 59 shows a simplified circuit typically used in high-voltage-sensing applications. The high impedance resistors (R1 and R2) are used as voltage dividers and dominate the current value definition. The resistance of the sensing resistor R3 is chosen to meet the input voltage range of the AMC1306. This resistor and the differential input impedance of the device (the AMC1306x25 is 22 kΩ, the AMC1306x05 is 4.9 kΩ) also create a voltage divider that results in an additional gain error. With the assumption of R1, R2, and R_{IN} having a considerably higher value than R3, the resulting total gain error can be estimated using Equation 4, with E_G being the gain error of the AMC1306.

$$\left|E_{Gtot}\right| = \left|E_G\right| + \frac{R3}{R_{IN}} \tag{4}$$

This gain error can be easily minimized during the initial system-level gain calibration procedure.

9.2.2.2 Detailed Design Procedure

As indicated in Figure 59, the output of the integrated differential amplifier is internally biased to a common-mode voltage of 1.9 V. This voltage results in a bias current I_{IB} through the resistive network R4 and R5 (or R4' and R5') used for setting the gain of the amplifier. The value range of this current is specified in the *Electrical Characteristics* table. This bias current generates additional offset error that depends on the value of the resistor R3. The initial system offset calibration does not minimize this effect because the value of the bias current depends on the actual common-mode amplitude of the input signal (as illustrated in Figure 60). Therefore, in systems with high accuracy requirements, a series resistor is recommended to be used at the negative input (AINN) of the AMC1306 with a value equal to the shunt resistor R3 (that is, R3' = R3 in Figure 59) to eliminate the effect of the bias current.

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This additional series resistor (R3') influences the gain error of the circuit. The effect can be calculated using Equation 5 with R5 = R5' = 50 kΩ and R4 = R4' = 2.5 kΩ (for the AMC1306x05) or 12.5 kΩ (for the AMC1306x25).

$$E_G(\%) = \left(1 - \frac{R4}{R4' + R3'}\right) \times 100\% \quad (5)$$

9.2.2.3 Application Curve

Figure 60 shows the dependency of the input bias current on the common-mode voltage at the input of the AMC1306.

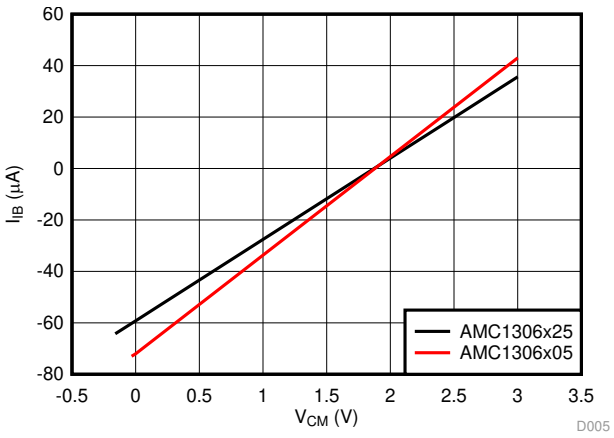

Figure 60. Input Bias Current vs Common-Mode Input Voltage

9.2.3 What To Do and What Not To Do

Do not leave the inputs of the AMC1306 unconnected (floating) when the device is powered up. If both modulator inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 1.9 V. If that voltage is above the specified input common-mode range, the front gain diminishes and the modulator outputs a bitstream resembling a zero input differential voltage.

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10 Power Supply Recommendations

In a typical frequency-inverter application, the high-side power supply (AVDD) for the device is directly derived from the floating power supply of the upper gate driver. For lowest system-level cost, a Zener diode can be used to limit the voltage to 5 V or 3.3 V (±10%). Alternatively a low-cost low-drop regulator (LDO), for example the LM317-N, can be used to adjust the supply voltage level and minimize noise on the power-supply node. A low-ESR decoupling capacitor of 0.1 µF is recommended for filtering this power-supply path. Place this capacitor (C2 in Figure 61) as close as possible to the AVDD pin of the AMC1306 for best performance. If better filtering is required, an additional 10-µF capacitor can be used.

The floating ground reference (AGND) is derived from the end of the shunt resistor that is connected to the negative input (AINN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads and AGND is connected to one of the outer leads of the shunt.

For decoupling of the digital power supply on the controller side, a 0.1-µF capacitor is recommended to be placed as close to the DVDD pin of the AMC1306 as possible, followed by an additional capacitor in the range of 1 µF to 10 µF.

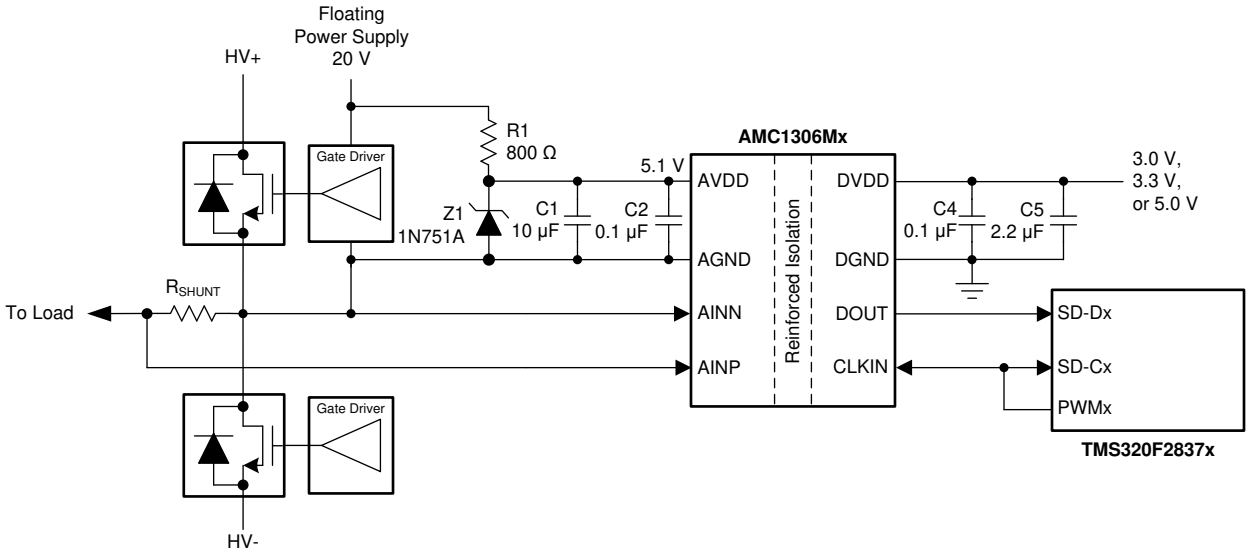

Figure 61. Decoupling the AMC1306

11 Layout

11.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors (as close as possible to the AMC1306) and placement of the other components required by the device is shown in Figure 62. For best performance, place the shunt resistor close to the AINP and AINN inputs of the AMC1306 and keep the layout of both connections symmetrical.

11.2 Layout Example

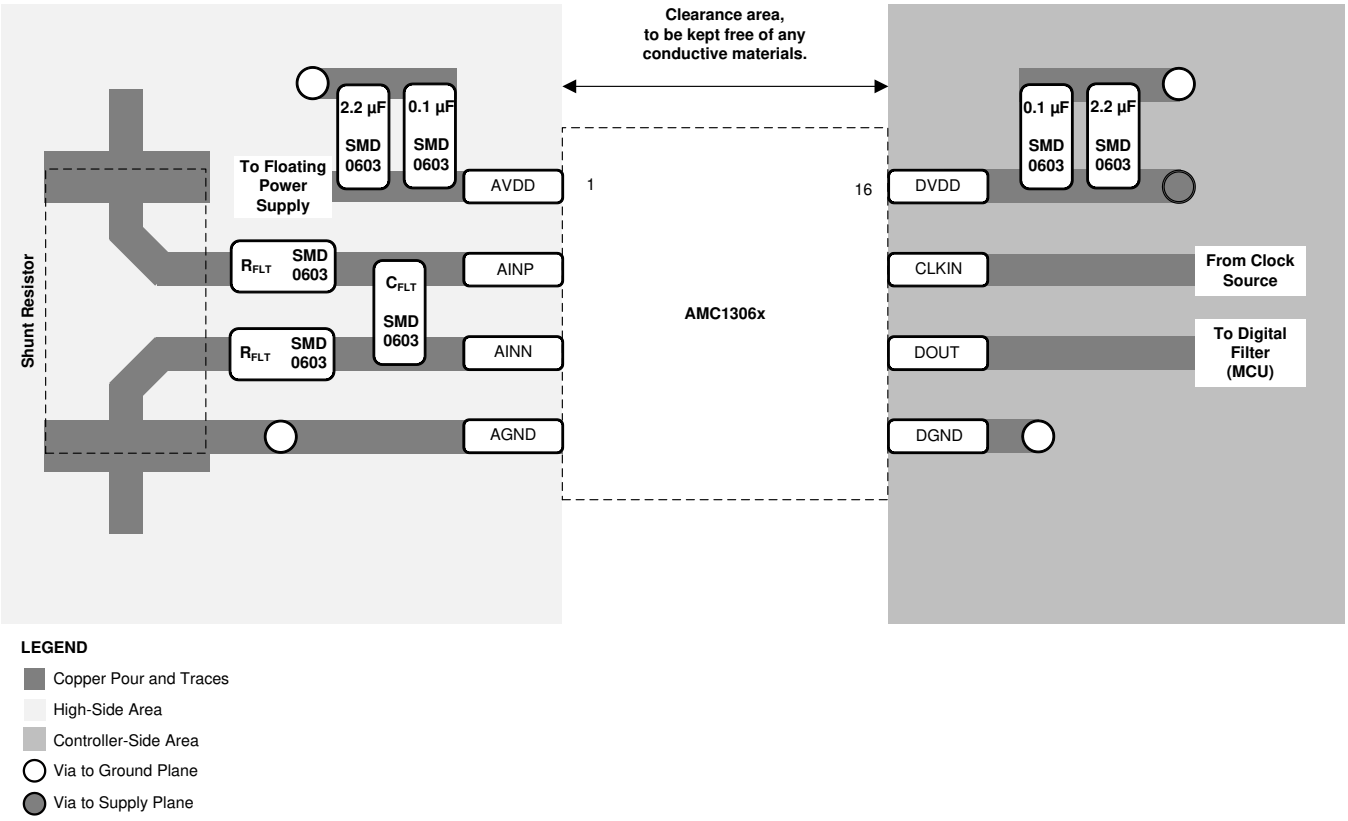

Figure 62. Recommended Layout of the AMC1306x

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

12.1.1.1 絶縁の用語集

*『絶縁の用語集』*を参照してください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『AMC1210 2次デルタ-シグマ変調器用のクワッド・デジタル・フィルタ』*
- *『MSP430F677x ポリフェーズ計量SoC』*
- *『TMS320F2807x Piccolo™ マイクロコントローラ』*
- *『TMS320F2837xD デュアルコアDelfino™ マイクロコントローラ』*
- *『ISO72x デジタル・アイソレータの磁場耐性』*
- *『ADS1202とFPGAデジタル・フィルタとの組み合わせによるモータ制御アプリケーションでの電流測定』*
- *『CDCLVC11xx 3.3Vおよび2.5V LVCMOS高性能クロック・バッファ・ファミリ』*

12.3 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
AMC1306E05	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
AMC1306E25	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
AMC1306M05	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
AMC1306M25	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1306E05DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWV.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1306E05DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E05
AMC1306E05DWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
AMC1306E25DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWV.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1306E25DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
AMC1306E25DWVRG4	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVRG4.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306E25
AMC1306E25DWVRG4.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
AMC1306M05DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWV.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1306M05DWVG4	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVG4.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVG4.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1306M05DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M05
AMC1306M05DWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
AMC1306M25DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWV.B	Active	Production	SOIC (DWV) | 8	64 | TUBE	-	Call TI	Call TI	-40 to 125	
AMC1306M25DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25
AMC1306M25DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1306M25

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1306M25DWVR.B	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AMC1306M05, AMC1306M25 :

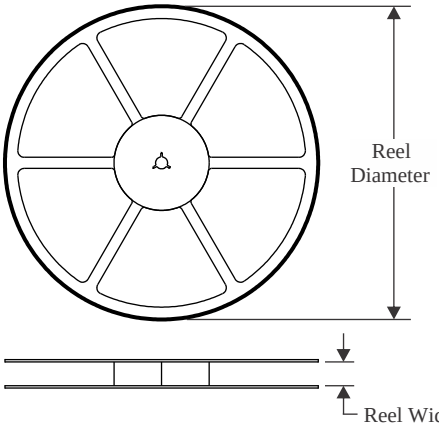
- Automotive : AMC1306M05-Q1, AMC1306M25-Q1

NOTE: Qualified Version Definitions:

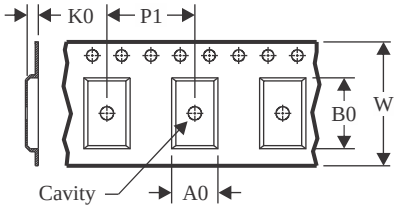
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

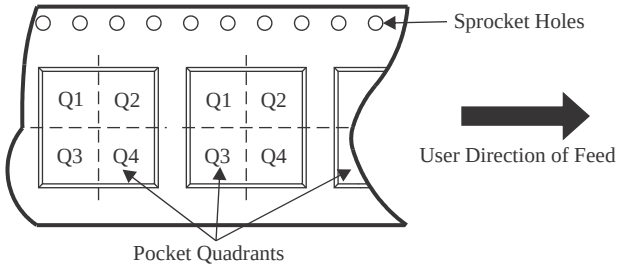


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

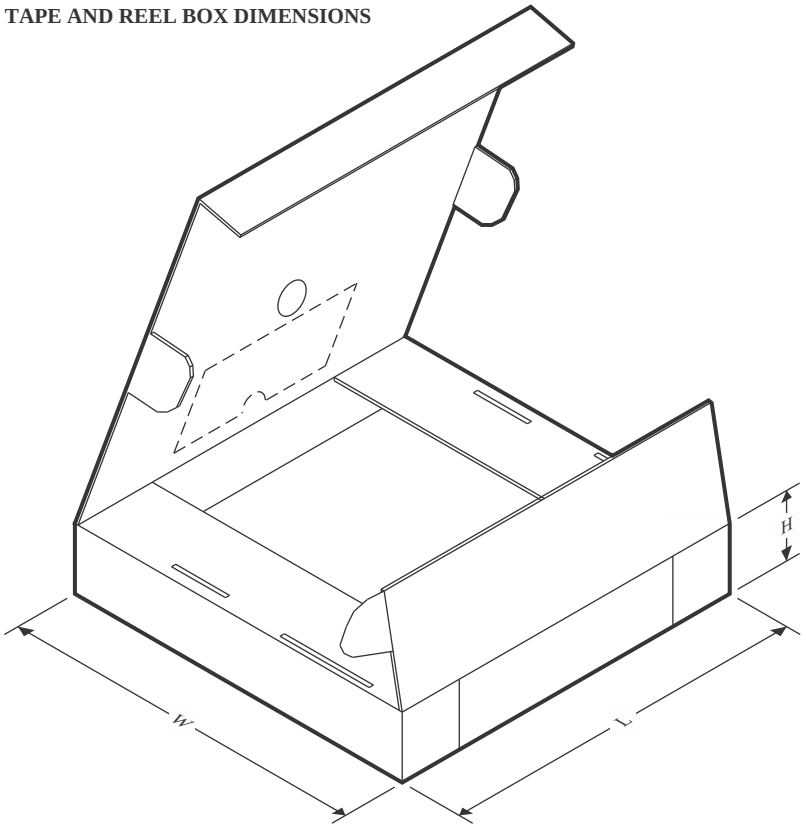
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1306E05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306E25DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306E25DWVRG4	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306M05DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
AMC1306M25DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

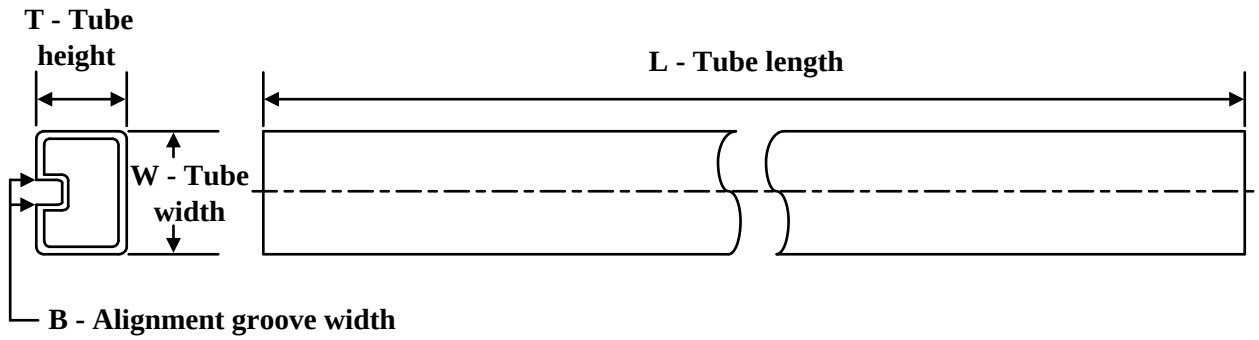
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

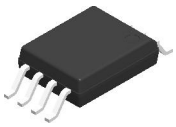
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1306E05DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306E25DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306E25DWVRG4	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306M05DWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
AMC1306M25DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

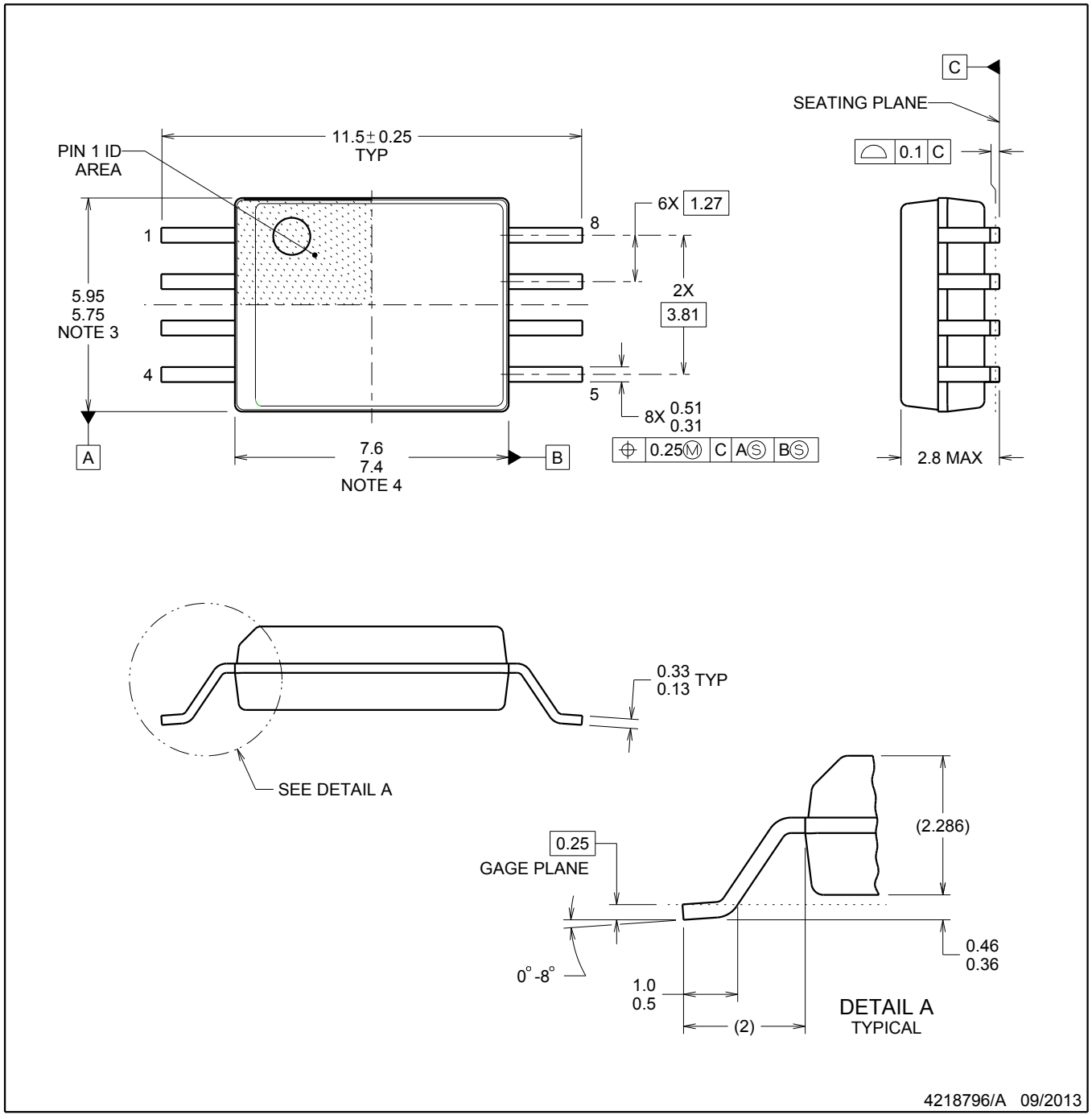
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1306E05DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E05DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E25DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306E25DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWVG4	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M05DWVG4.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M25DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1306M25DWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

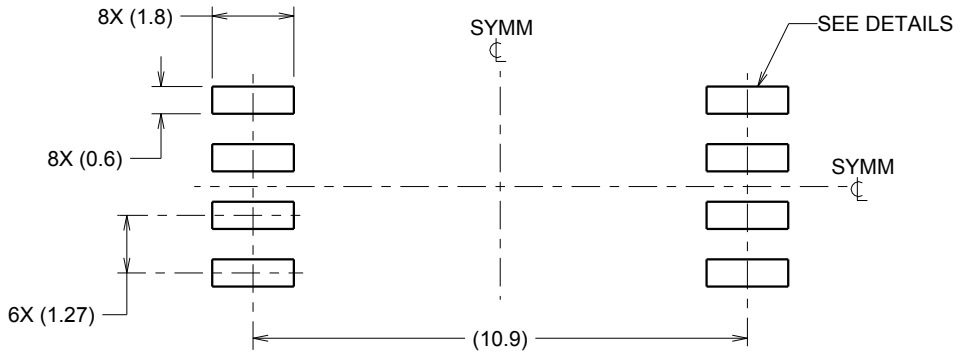
SOIC - 2.8 mm max height

SOIC

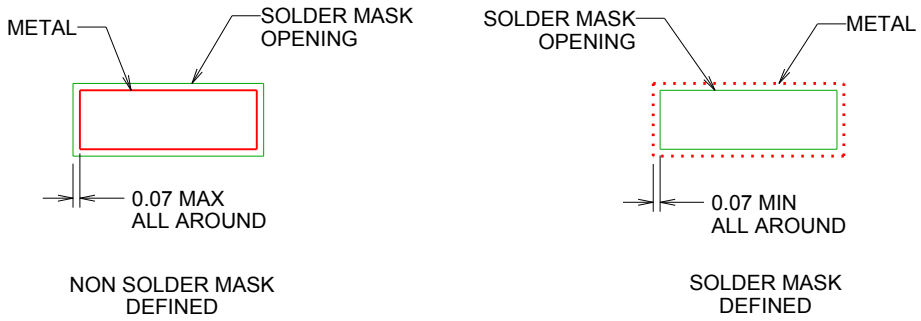


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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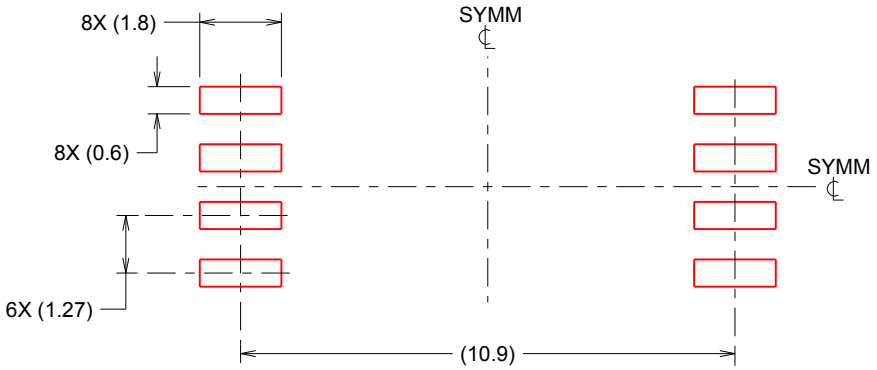
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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