AMC1311x 高インピーダンス、2V 入力、強化絶縁型アンプ

1 特長

- 絶縁電圧測定用に最適化された 2V の高インピーダンス入力電圧範囲
- 固定ゲイン:1
- 小さい DC 誤差:
  - AMC1311:
    - オフセット誤差:±9.9mV (最大値)
    - オフセット・ドリフト:±20μV/℃ (標準値)
    - ゲイン誤差:±1% (最大値)
    - ゲイン・ドリフト:±30ppm/℃ (標準値)
  - AMC1311B:
    - オフセット誤差:±1.5mV (最大値)
    - オフセット・ドリフト:±10μV/℃ (最大値)
    - ゲイン誤差:±0.2% (最大値)
    - ゲイン・ドリフト:±40ppm/℃ (最大値)
  - 非線形性:0.04% (最大値)
- ハイサイドの 3.3V 動作 (AMC1311B)
- 高 CMTI:100kV/μs (最小値) (AMC1311B)
- ハイサイド電源喪失の表示
- 安全関連認証:
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した強化絶縁耐圧:7000V_{PK}
  - UL 1577 に準拠した絶縁耐圧:5000V_{RMS} (1 分間)
  - 拡張産業用温度範囲全体にわたって仕様を完全に規定:-40℃～+125℃

2 アプリケーション

- 次の用途での絶縁型電圧センシング:
  - モーター・ドライブ
  - 周波数インバータ
  - 無停電電源

3 概要

AMC1311 は、磁気干渉に対して高い耐性を示す容量性絶縁バリアによって入力回路から分離された出力を備えた高精度の絶縁型アンプです。この絶縁バリアは、DIN EN IEC 60747-17 (VDE 0884-17) および UL1577 に従って最大 5kV_{RMS} の強化ガルバニック絶縁を達成していることが認証されており、最大 1500V_{RMS} の使用電圧に対応しています。

この絶縁バリアは、異なる同相電圧レベルで動作するシステム領域を分離し、電気的損傷を生じさせる可能性がある電圧またはオペレータに害を及ぼす可能性がある電圧から低電圧側を保護します。

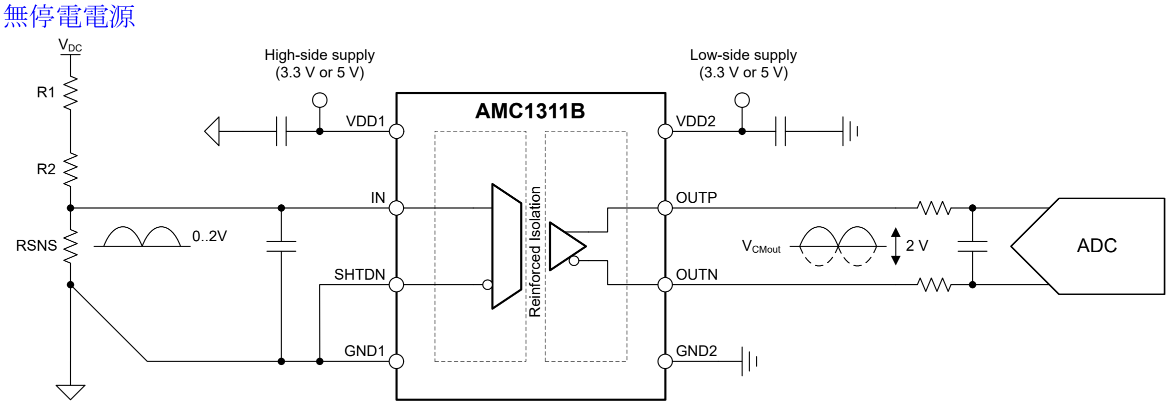
AMC1311 の高インピーダンス入力は、高インピーダンスの抵抗分圧器またはその他の高インピーダンスの電圧信号源と接続するように最適化されています。優れた DC 精度と低い温度ドリフトにより、閉ループ・システムでの高精度の絶縁電圧センシングと制御をサポートします。ハイサイド電源喪失の検出機能が内蔵されているため、システム・レベルの設計や診断が容易になります。

AMC1311 は 2 つの性能グレード・オプションで供給されます。AMC1311B は拡張産業用温度範囲の -55℃～+125℃ で動作が規定されており、AMC1311 は -40℃～+125℃ で動作します。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
AMC1311	SOIC (8)	5.85mm × 7.50mm
AMC1311B		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (May 2020) to Revision C (June 2022) — **Page**

- 絶縁規格を DIN VDE V 0884-11 (VDE V 0884-11) から DIN EN IEC 60747-17 (VDE 0884-17) に変更し、それに応じて「絶縁仕様」と「安全関連認証」の表を更新 ... 1
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- Merged V_{OS} specs for 4.5V ≤ VDD1 ≤ 5.5 V and 3.0 V ≤ VDD1 ≤ 5.5 V ranges (AMC1311B only) ... 10
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- Changed CMTI from 75 kV/µs (minimum), 140 kV/µs (typical) to 100 kV/µs (minimum), 150kV/µs (typical) (AMC1311B only) ... 10
- Changed $VDD1_{UV}$ (VDD1 falling) from 1.75 V / 2.53 V / 2.7 V to 2.4 V / 2.6 V / 2.8 V (minimum / typical / maximum) ... 10
- Changed *Rise, Fall, and Delay Time Definition* timing diagram ... 12
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- Changed functional block diagram ... 20
- Deleted *Fail-Safe Output* section, added *Analog Output* section ... 22
- Changed *Typical Application* section and subsections ... 23
- Changed *What To Do and What Not To Do* section ... 26
- Changed *Layout* section ... 28

Changes from Revision A (June 2018) to Revision B (May 2020) **Page**

- 「特長」セクションで AMC1311B のオフセットのドリフトを ±15μV/℃ (最大値) から 10μV/℃ (最大値) に変更........... 1
- 「特長」セクションで AMC1311B のゲイン誤差を ±0.3% (最大値) から ±0.2% (最大値) に変更し、AMC1311B のゲイン・ドリフトを ±45ppm/℃ (最大値) から ±40ppm/℃ (最大値) に変更....................1
- 「IEC 60950-1 および IEC60065」を「IEC 62368-1」に変更....................1
- Changed AMC1311B values for TCV_{OS}, E_G, and TCE_G in *Device Comparison Table* 4
- Changed AMC1311B values for TCV_{OS}, E_G, and TCE_G in *Device Comparison Table* 6
- Added ESD classification levels to *ESD Ratings* table....................6
- Changed CLR and CPG values from 9 mm to 8.5 mm....................6
- Changed *Insulation Specifications* table per ISO standard.................... 6
- Changed *Safety-Related Certification* table per ISO standard.................... 6
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- Changed TCV_{OS} parameter minimum value from –15 µV/°C to –10 µV/°C and maximum value from 15 µV/°C to 10µV/°C for the AMC1311B in the *Electrical Characteristics* table....................6
- Changed E_G parameter minimum value from *–0.3%* to *–0.2%* and maximum value from *0.3%* to *0.2%* for the AMC1311B in the *Electrical Characteristics* table....................6
- Changed TCE_G parameter minimum value from *–45 ppm/°C* to *–40 ppm/°C* and maximum value from *45 ppm/°C* to *40 ppm/°C* for the AMC1311B in the *Electrical Characteristics* table.................... 6
- Changed *Step Response of the AMC1311* figure....................26

5 Device Comparison Table

PARAMETER		AMC1311B	AMC1311
High-side supply voltage, VDD1		3.0 V to 5.5 V	4.5 V to 5.5 V
Specified ambient temperature, T_A		–55°C to +125°C	–40°C to +125°C
Input offset voltage, V_{OS}	4.5 V ≤ VDD1 ≤ 5.5 V	±1.5 mV	±9.9 mV
	3.0 V ≤ VDD1 ≤ 5.5 V	±2.5 mV	Not applicable
Input offset drift, TCV_{OS}		±3 µV/°C (typ), ±10 µV/°C (max)	±20 µV/°C (typ)
Gain error, E_G		±0.2%	±1%
Gain error drift, TCE_G		±5 ppm/°C (typ), ±40 ppm/°C (max)	±30 ppm/°C (typ)
Common-mode transient immunity, CMTI		100 kV/µs (min)	15 kV/µs (min)

6 Pin Configuration and Functions

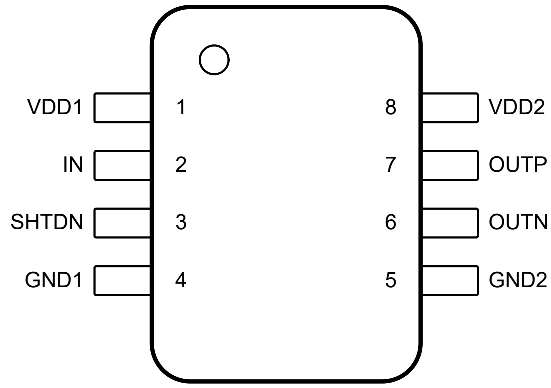


図 6-1. DWV Package, 8-Pin SOIC (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	IN	Analog input	Analog input
3	SHTDN	Digital input	Shutdown input, active high, with internal pullup resistor (typical value: 100 kΩ)
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	OUTN	Analog output	Inverting analog output
7	OUTP	Analog output	Noninverting analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings

see(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Input voltage	IN	GND1 – 6	VDD1 + 0.5	V
	SHTDN	GND1 – 0.5	VDD1 + 0.5	
Output voltage	OUTP, OUTN	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1, AMC1311	4.5	5	5.5	V
		VDD1 to GND1, AMC1311B	3	5	5.5	
	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output	IN to GND1		2.516		V
V_{FSR}	Specified linear full-scale voltage	IN to GND1	–0.1		2	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	On OUTP or OUTN to GND2			500	pF
		OUTP to OUTN			250	
R_{LOAD}	Resistive load	On OUTP or OUTN to GND2		10	1	kΩ
DIGITAL INPUT						
	Input voltage	SHTDN to GND1	0		VDD1	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature	AMC1311	–40		125	°C
		AMC1311B	–55		125	

7.4 Thermal Information

THERMAL METRIC[1]		DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V	98	mW
		VDD1 = VDD2 = 3.6V, AMC1311B only	56	
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5 V	53	mW
		VDD1 = 3.6 V, AMC1311B only	30	
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5 V	45	mW
		VDD2 = 3.6 V, AMC1311B only	26	

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage[1]	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7000	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8400	
V_{IMP}	Maximum impulse voltage[3]	Tested in air, 1.2/50-µs waveform per IEC 62368-1	9800	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[4]	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	12800	V_{PK}
q_{pd}	Apparent charge[5]	Method a, after input/output safety test subgroups 2 and 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output[6]	V_{IO} = 0.5 V_{PP} at 1 MHz	~1.5	pF
R_{IO}	Insulation resistance, input to output[6]	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition
Reinforced insulation	Single protection
Certificate number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 84.6°C/W, VDDx = 5.5 V, T_J = 150°C, T_A = 25°C			268	mA
		$R_{\theta JA}$ = 84.6°C/W, VDDx = 3.6 V, T_J = 150°C, T_A = 25°C, AMC1311B only			410	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 84.6°C/W, T_J = 150°C, T_A = 25°C			1477	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

7.9 Electrical Characteristics

minimum and maximum specifications of the AMC1311 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B apply from T_A = –55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = –0.1 V to 2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage[(1)] [(2)]	T_A = 25°C, 4.5 V ≤ VDD1 ≤ 5.5 V, AMC1311	–9.9	±0.4	9.9	mV
		T_A = 25°C, AMC1311B[(3)]	–1.5	±0.4	1.5	
TCV_{OS}	Input offset thermal drift[(1)] [(2)] [(5)]	AMC1311		±20		μV/°C
		AMC1311B	–10	±3	10	
R_{IN}	Input resistance	T_A = 25℃		1		GΩ
I_{IB}	Input bias current	IN = GND1, T_A = 25℃	–15	3.5	15	nA
C_{IN}	Input capacitance	f_{IN} = 275 kHz		7		pF
ANALOG OUTPUT						
	Nominal gain			1		V/V
E_G	Gain error[(1)]	T_A = 25℃, AMC1311	–1%	0.4%	1%	
		T_A = 25℃, AMC1311B	–0.2%	±0.05%	0.2%	
TCE_G	Gain error drift[(1)] [(6)]	AMC1311		±30		ppm/°C
		AMC1311B	–40	±5	40	
	Nonlinearity[(1)]		–0.04%	±0.01%	0.04%	
THD	Total harmonic distortion[(4)]	V_{IN} = 2 V_{PP}, V_{IN} > 0 V, f_{IN} = 10 kHz, BW = 10 kHz		–87		dB
SNR	Signal-to-noise ratio	V_{IN} = 2 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz	79	82.6		dB
		V_{IN} = 2 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz		70.9		
	Output noise	V_{IN} = GND1, BW = 100 kHz		220		μVrms
PSRR	Power-supply rejection ratio[(2)]	vs VDD1, at DC		–80		dB
		vs VDD2, at DC		–85		
		vs VDD1, 10 kHz / 100-mV ripple		–65		
		vs VDD2, 10 kHz / 100-mV ripple		–70		
V_{CMout}	Output common-mode voltage		1.39	1.44	1.49	V
$V_{CLIPout}$	Clipping differential output voltage	V_{OUT} = (V_{OUTP} – V_{OUTN}); V_{IN} > $V_{Clipping}$		2.49		V
$V_{FAILSAFE}$	Failsafe differential output voltage	SHTDN = high, or VDD1 undervoltage, or VDD1 missing		–2.6	–2.5	V
BW	Output bandwidth	AMC1311	100	220		kHz
		AMC1311B	220	275		
R_{OUT}	Output resistance	On OUTP or OUTN		<0.2		Ω
	Output short-circuit current	On OUTP or OUTN, sourcing or sinking, IN = GND1, outputs shorted to either GND or VDD2		14		mA
CMTI	Common-mode transient immunity	AMC1311	15	30		kV/μs
		AMC1311B	100	150		

7.9 Electrical Characteristics (continued)

minimum and maximum specifications of the AMC1311 apply from T_A = –40°C to +125°C, VDD1 = 4.5 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = –0.1 V to 2 V, and SHTDN = GND1 = 0 V; minimum and maximum specifications of the AMC1311B apply from T_A = –55°C to +125°C, VDD1 = 3.0 V to 5.5 V, VDD2 = 3.0 V to 5.5 V, V_{IN} = –0.1 V to 2 V, and SHTDN = GND1 = 0 V (unless otherwise noted); typical specifications are at T_A = 25°C, VDD1 = 5 V, and VDD2 = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT						
I_{IN}	Input current	SHTDN pin, GND1 ≤ SHTDN ≤ VDD1	–70		1	µA
C_{IN}	Input capacitance	SHTDN pin		5		pF
V_{IH}	High-level input voltage		0.7 × VDD1			V
V_{IL}	Low-level input voltage				0.3 × VDD1	V
POWER SUPPLY						
$VDD1_{UV}$	VDD1 undervoltage detection threshold	VDD1 rising	2.5	2.7	2.9	V
		VDD1 falling	2.4	2.6	2.8	
$VDD2_{UV}$	VDD2 undervoltage detection threshold	VDD2 rising	2.2	2.45	2.65	V
		VDD2 falling	1.85	2.0	2.2	
I_{DD1}	High-side supply current	3.0 V < VDD1 < 3.6 V, SHTDN = low, AMC1311B only		6.0	8.4	mA
		4.5 V < VDD1 < 5.5 V, SHTDN = low		7.1	9.7	
		SHTDN = VDD1		1.3		µA
I_{DD2}	Low-side supply current	3.0 V < VDD2 < 3.6 V		5.3	7.2	mA
		4.5 V < VDD2 < 5.5 V		5.9	8.1	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) The typical value is at VDD1 = 3.3 V.
(4) THD is the ratio of the rms sum of the amplitudes of first five higher harmonics to the amplitude of the fundamental.
(5) Offset error temperature drift is calculated using the box method, as described by the following equation:
$TCV_{OS} = (Value_{MAX} - Value_{MIN}) / TempRange$
(6) Gain error temperature drift is calculated using the box method, as described by the following equation:
$TCE_G (ppm) = (Value_{MAX} - Value_{MIN}) / (Value_{(T=25°C)} \times TempRange) \times 10^6$

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.3		µs
t_f	Output signal fall time			1.3		µs
	IN to OUTx signal delay (50% – 10%)	Unfiltered output, AMC1311		1.5	2.5	µs
		Unfiltered output, AMC1311B		1.0	1.5	
	IN to OUTx signal delay (50% – 50%)	Unfiltered output, AMC1311		2.1	3.1	µs
		Unfiltered output, AMC1311B		1.6	2.1	
	IN to OUTx signal delay (50% – 90%)	Unfiltered output, AMC1311		3.0	4.0	µs
		Unfiltered output, AMC1311B		2.5	3.0	
t_{AS}	Analog settling time	VDD1 step to 3.0 V with VDD2 ≥ 3.0 V, to V_{OUTP}, V_{OUTN} valid, 0.1% settling		50	100	µs
t_{EN}	Device enable time	SHTDN high to low		50	100	µs
t_{SHTDN}	Device shutdown time	SHTDN low to high		3	10	µs

7.11 Timing Diagram

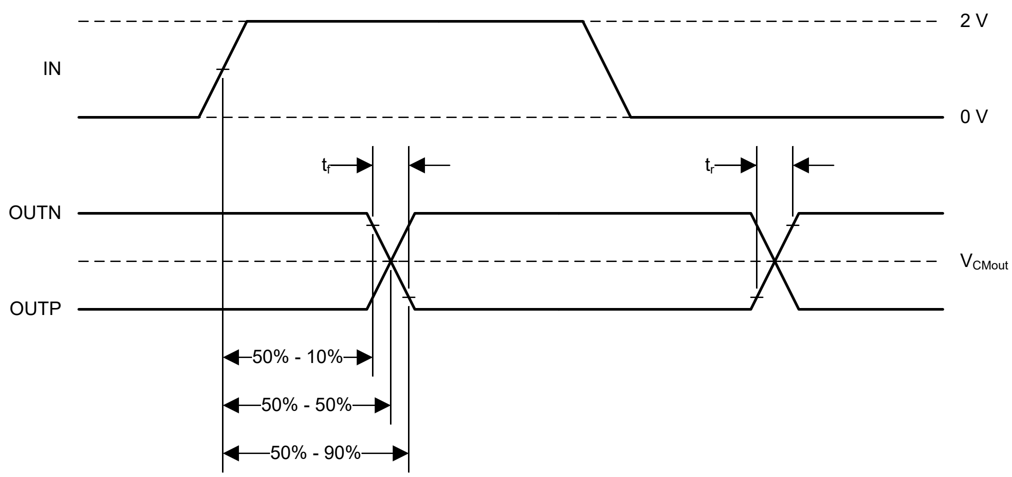


図 7-1. Rise, Fall, and Delay Time Definition

7.12 Insulation Characteristics Curves

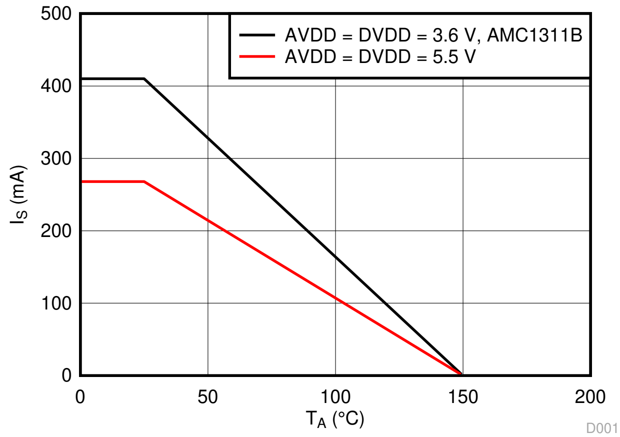


図 7-2. Thermal Derating Curve for Safety-Limiting Current per VDE

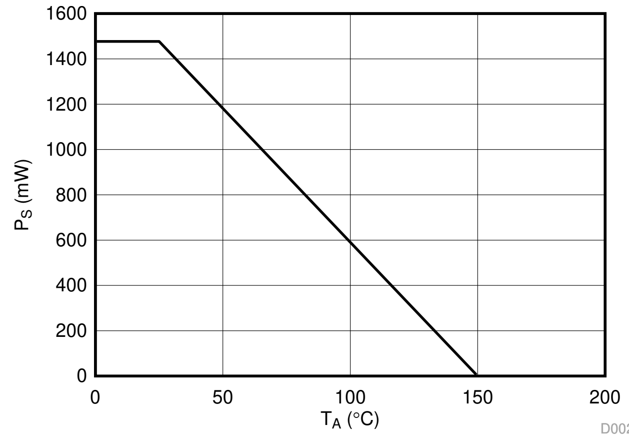
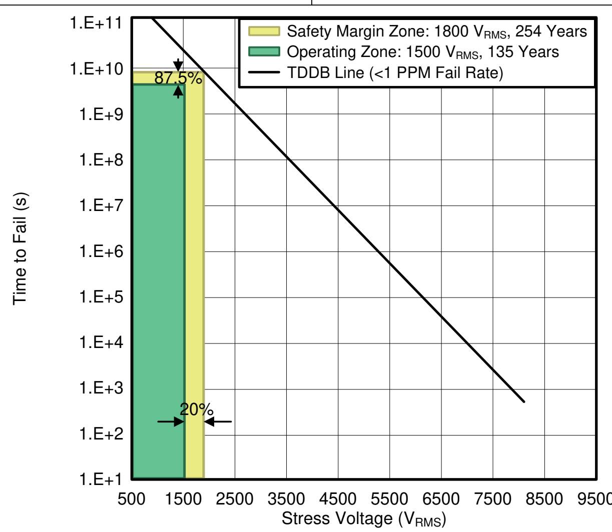


図 7-3. Thermal Derating Curve for Safety-Limiting Power per VDE

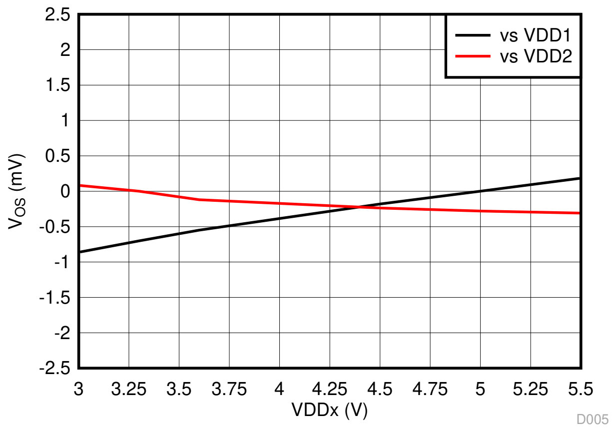


T_A up to 150°C, stress-voltage frequency = 60 Hz, isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

図 7-4. Reinforced Isolation Capacitor Lifetime Projection

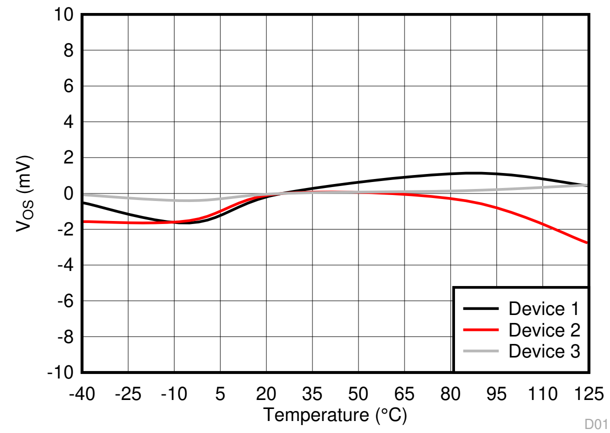
7.13 Typical Characteristics

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



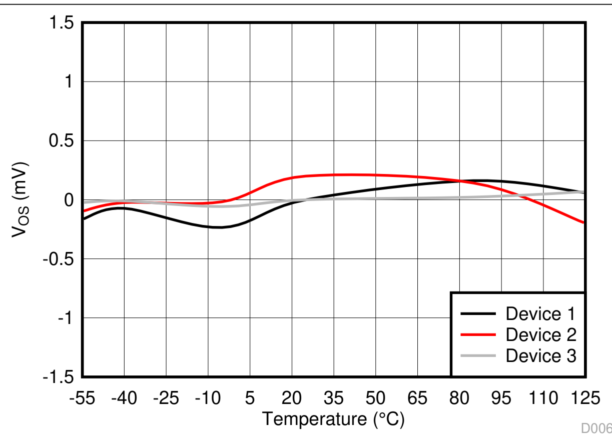
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-5. Input Offset Voltage vs Supply Voltage



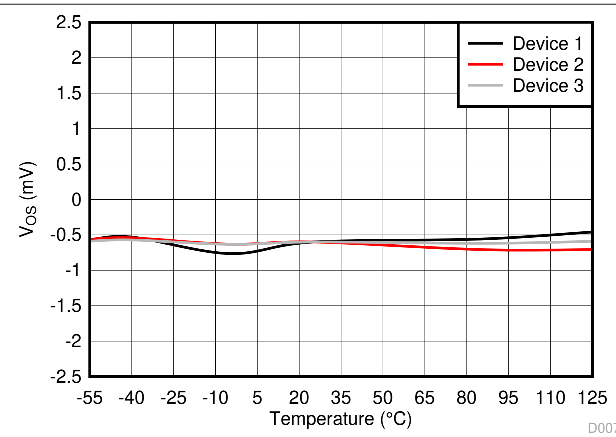
AMC1311

図 7-6. Input Offset Voltage vs Temperature



VDD1 = 5 V, AMC1311B

図 7-7. Input Offset Voltage vs Temperature



VDD1 = 3.3 V, AMC1311B

図 7-8. Input Offset Voltage vs Temperature

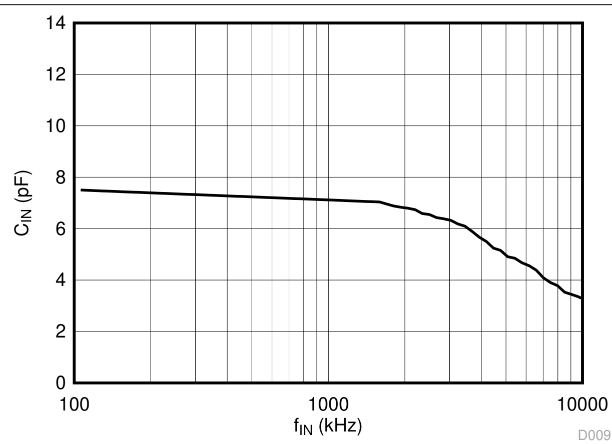
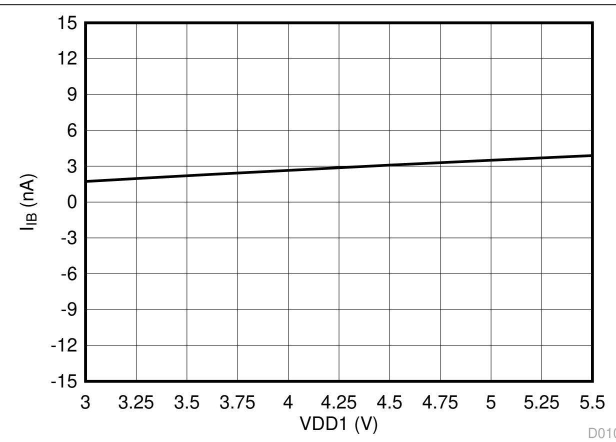


図 7-9. Input Capacitance vs Input Signal Frequency

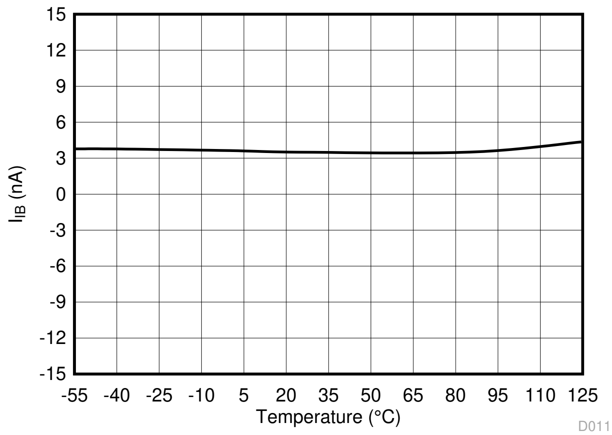


3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-10. Input Bias Current vs High-Side Supply Voltage

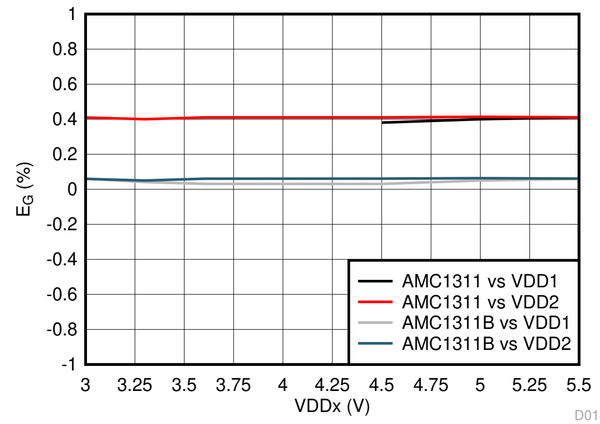
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



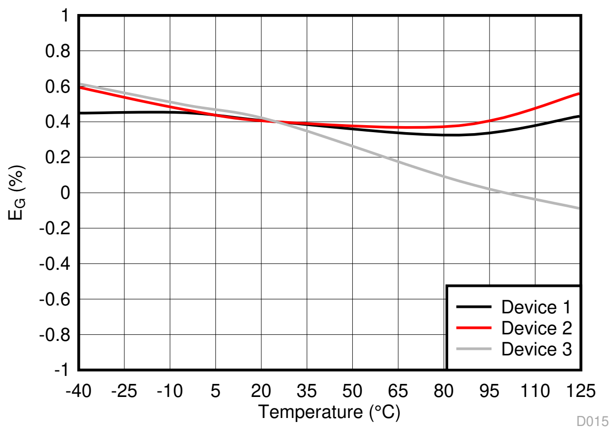
–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-11. Input Bias Current vs Temperature



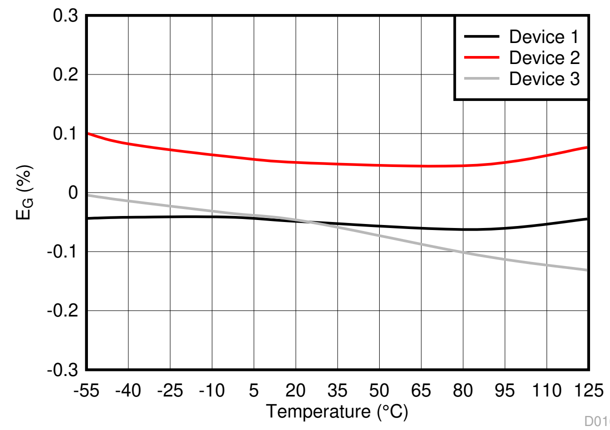
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-12. Gain Error vs Supply Voltage



AMC1311

図 7-13. Gain Error vs Temperature



AMC1311B

図 7-14. Gain Error vs Temperature

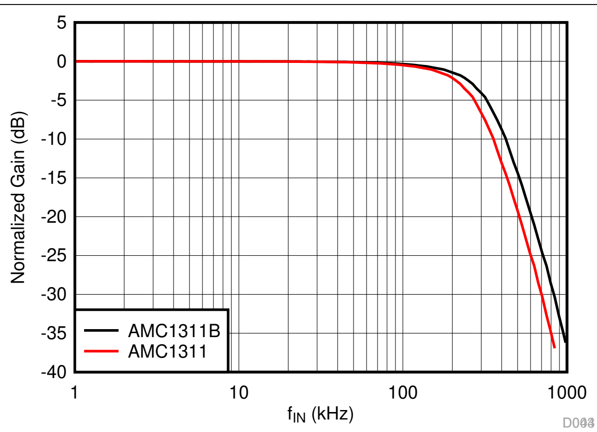


図 7-15. Normalized Gain vs Input Frequency

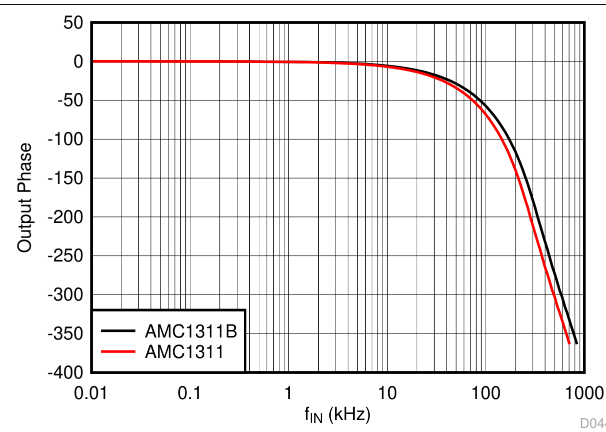


図 7-16. Output Phase vs Input Frequency

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

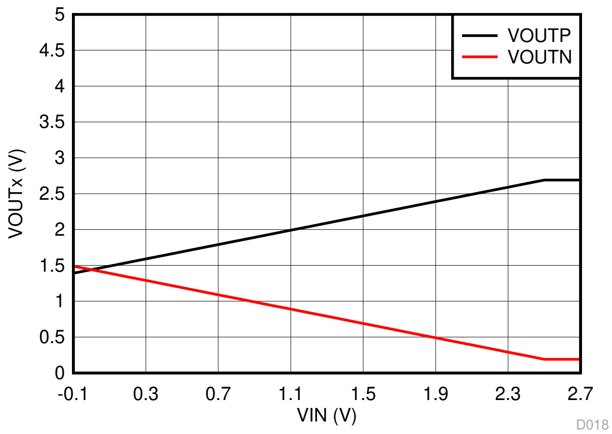


図 7-17. Output Voltage vs Input Voltage

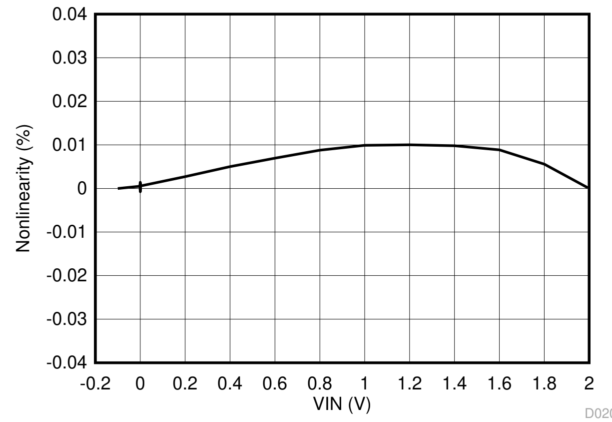
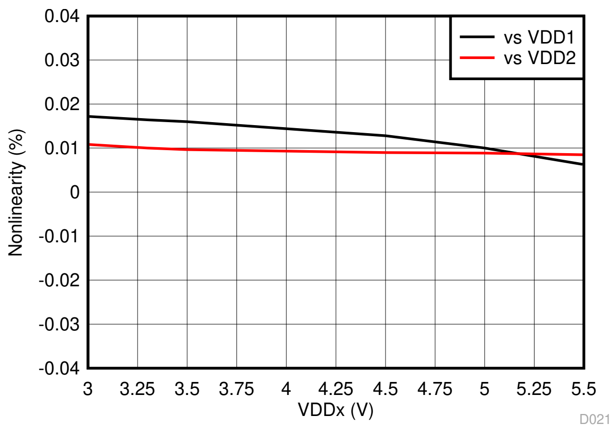
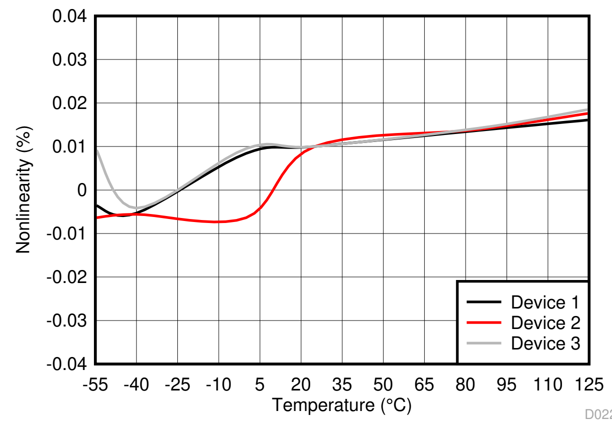


図 7-18. Nonlinearity vs Input Voltage



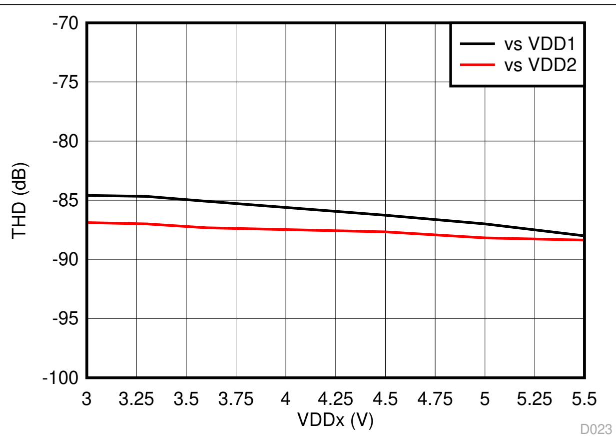
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-19. Nonlinearity vs Supply Voltage



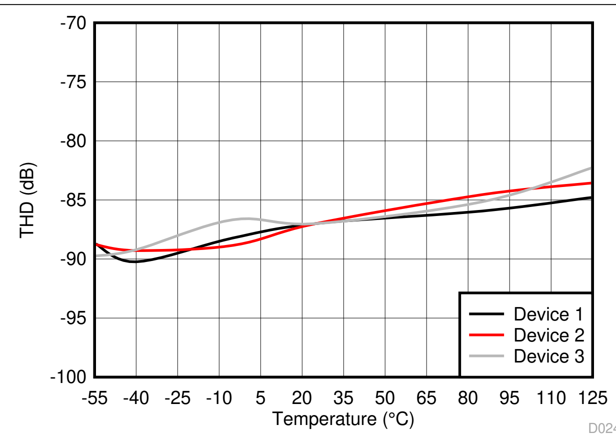
–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-20. Nonlinearity vs Temperature



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-21. Total Harmonic Distortion vs Supply Voltage



–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-22. Total Harmonic Distortion vs Temperature

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)

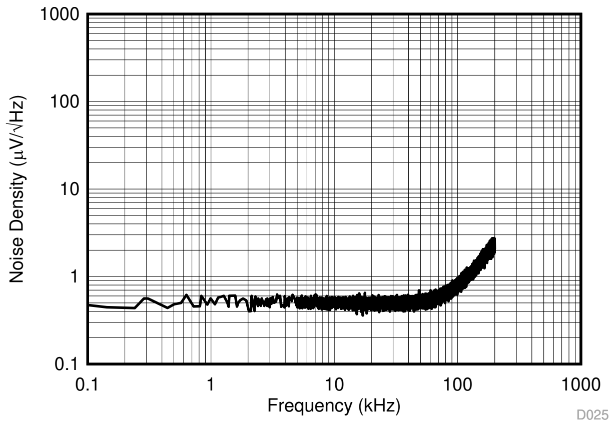


図 7-23. Input-Referred Noise Density vs Frequency

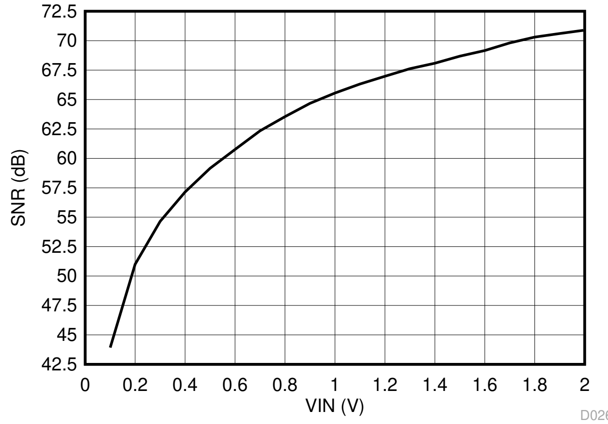
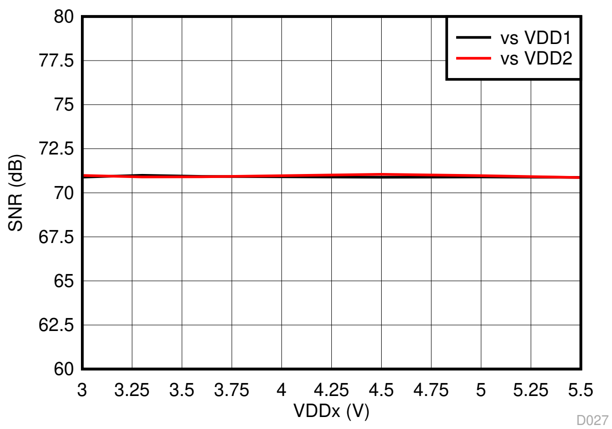
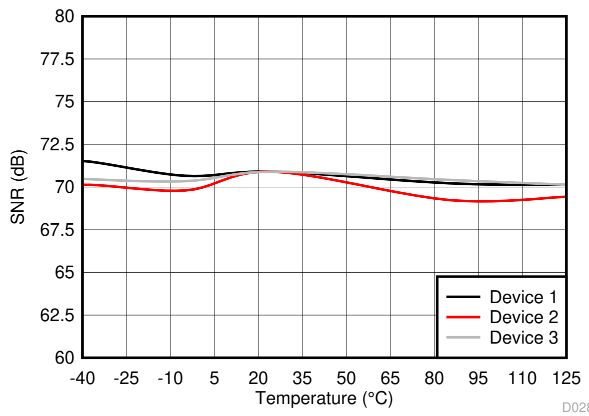


図 7-24. Signal-to-Noise Ratio vs Input Voltage



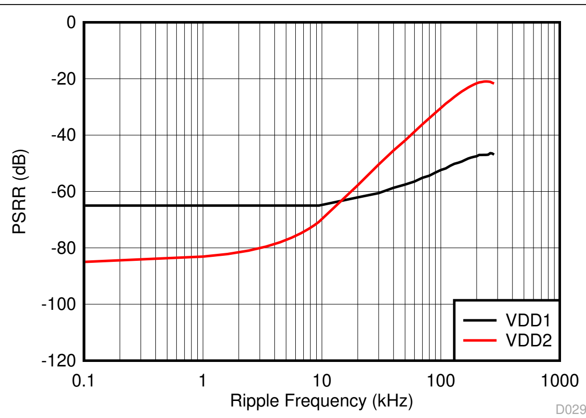
3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-25. Signal-to-Noise Ratio vs Supply Voltage



–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-26. Signal-to-Noise Ratio vs Temperature



100-mV ripple

図 7-27. Power-Supply Rejection Ratio vs Ripple Frequency

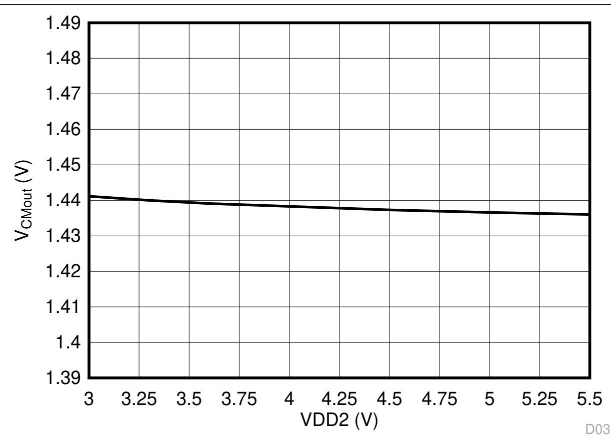
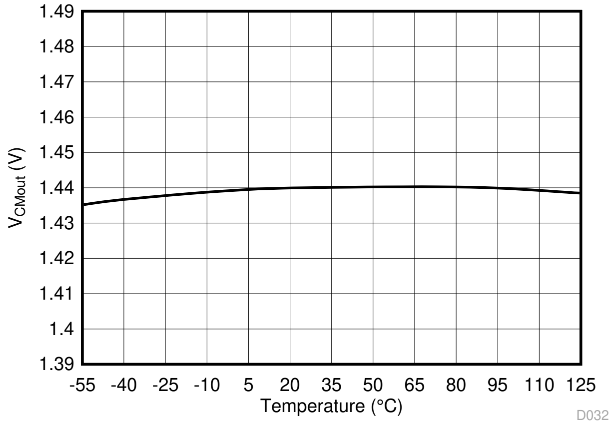


図 7-28. Output Common-Mode Voltage vs Low-Side Supply Voltage

7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-29. Output Common-Mode Voltage vs Temperature

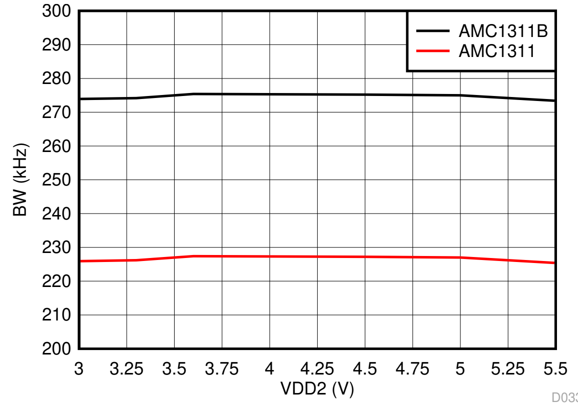


図 7-30. Output Bandwidth vs Low-Side Supply Voltage

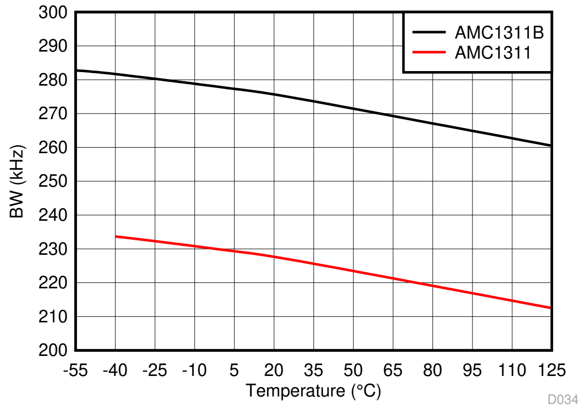
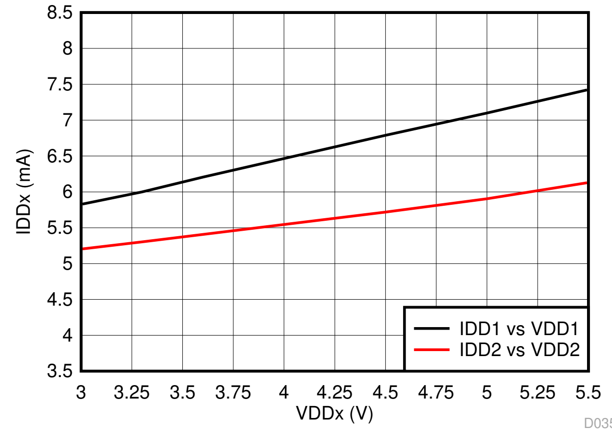
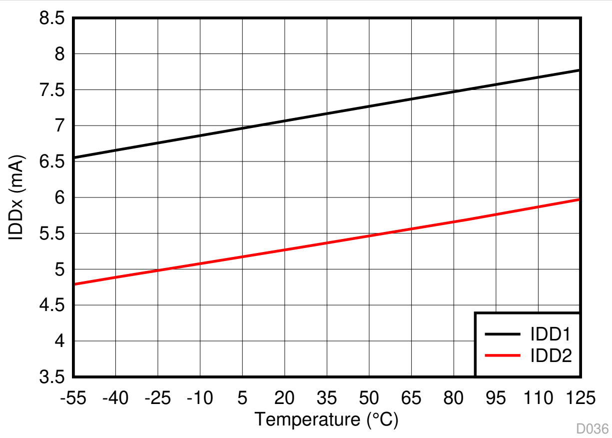


図 7-31. Output Bandwidth vs Temperature



3.0 V ≤ VDD1 < 4.5 V for the AMC1311B only

図 7-32. Supply Current vs Supply Voltage



–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-33. Supply Current vs Temperature

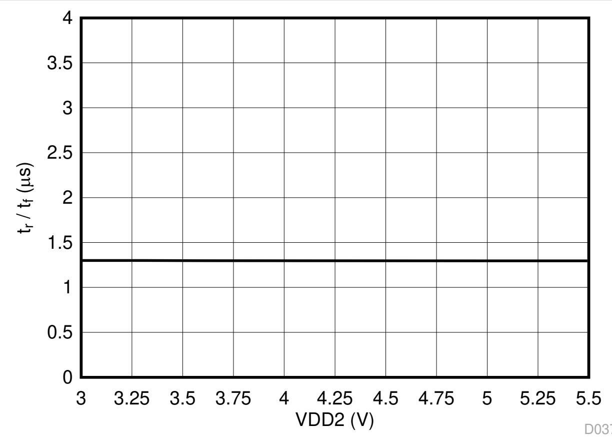
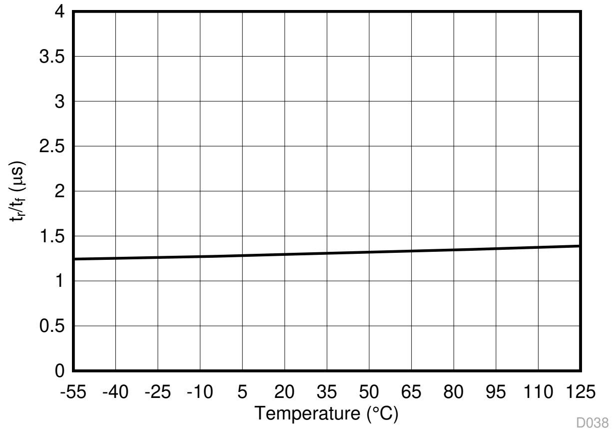


図 7-34. Output Rise and Fall Time vs Low-Side Supply Voltage

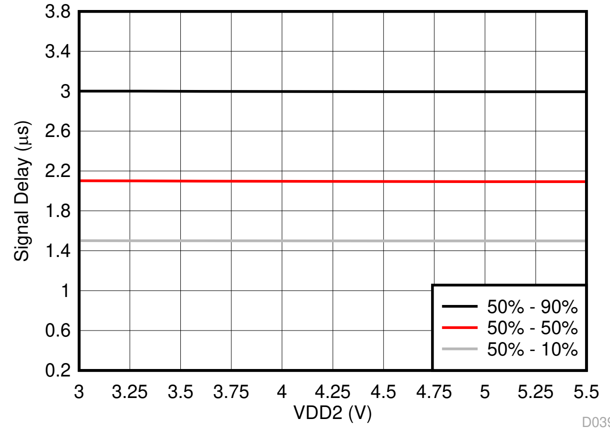
7.13 Typical Characteristics (continued)

at VDD1 = 5 V, VDD2 = 3.3 V, SHTDN = 0 V, f_{IN} = 10 kHz, and BW = 100 kHz (unless otherwise noted)



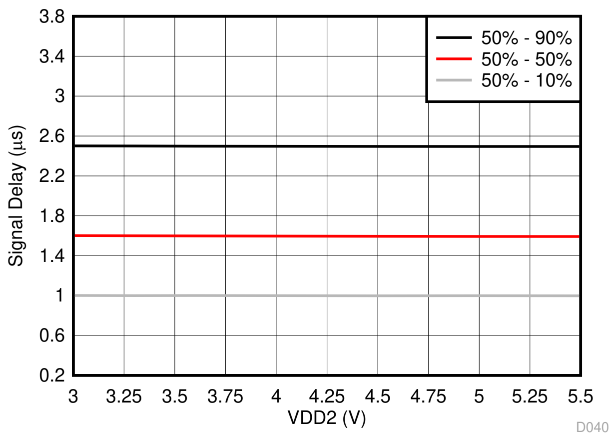
–55°C ≤ T_A < –40°C for the AMC1311B only

図 7-35. Output Rise and Fall Time vs Temperature



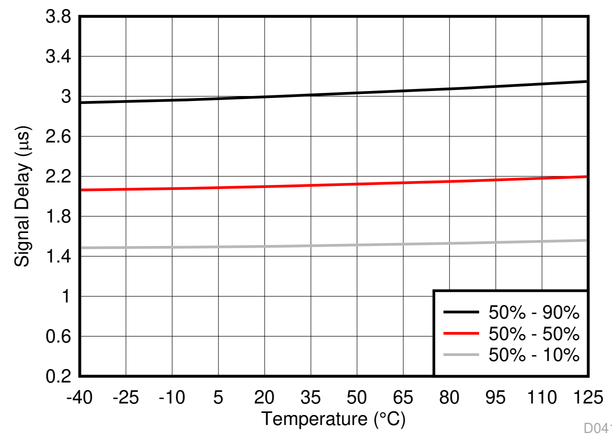
AMC1311

図 7-36. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage



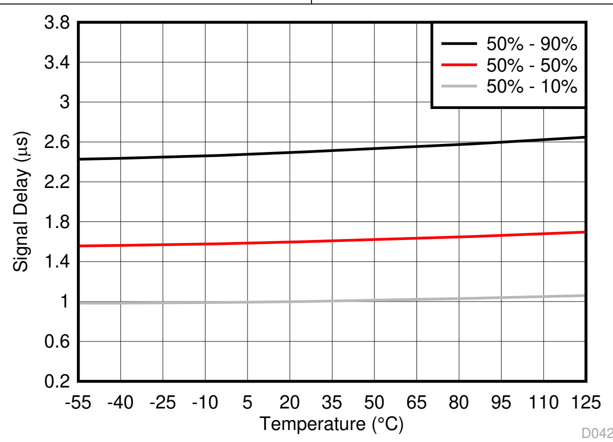
AMC1311B

図 7-37. IN to OUTP, OUTN Signal Delay vs Low-Side Supply Voltage



AMC1311

図 7-38. IN to OUTP, OUTN Signal Delay vs Temperature



AMC1311B

図 7-39. IN to OUTP, OUTN Signal Delay vs Temperature

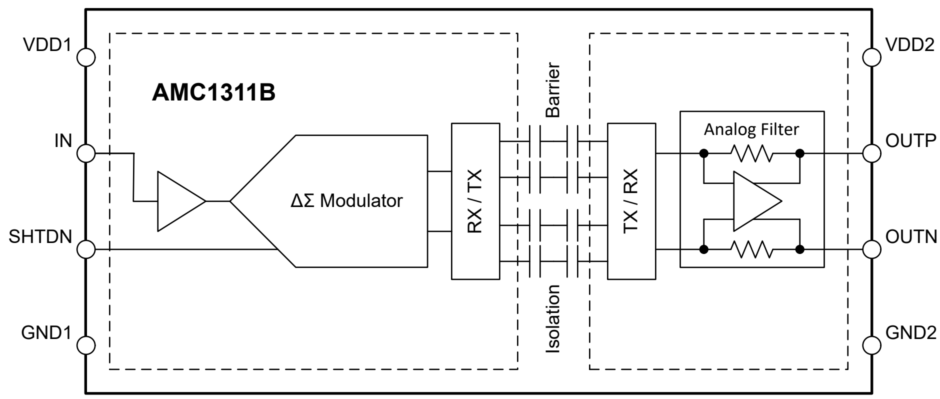
8 Detailed Description

8.1 Overview

The AMC1311 is a precision, single-ended input, isolated amplifier with a high input impedance and wide input voltage range. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier and separates the high-side from the low-side. On the low-side, the received bitstream is processed by a fourth-order analog filter that outputs a differential signal at the OUTP and OUTN pins proportional to the input signal.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The digital modulation used in the AMC1311 to transmit data across the isolation barrier, and the isolation barrier characteristics itself, result in high reliability and high common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The single-ended, high-impedance input stage of the AMC1311 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred across the isolation barrier, as described in the *Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signal IN. First, if the input voltage V_{IN} exceeds the range specified in the *Absolute Maximum Ratings* table, the input current must be limited to the absolute maximum value because the electrostatic discharge (ESD) protection turns on. Secondly, the linearity and parametric performance of the device is ensured only when the analog input voltage remains within the linear full-scale range (V_{FSR}) as specified in the *Recommended Operating Conditions* table.

8.3.2 Isolation Channel Signal Transmission

The AMC1311 uses an on-off keying (OOK) modulation scheme, as shown in 図 8-1, to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) shown in the *Functional Block Diagram* transmits an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC1311 is 480 MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the fourth-order analog filter. The AMC1311 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and lowest level of radiated emissions caused by the high-frequency carrier and RX/TX buffer switching.

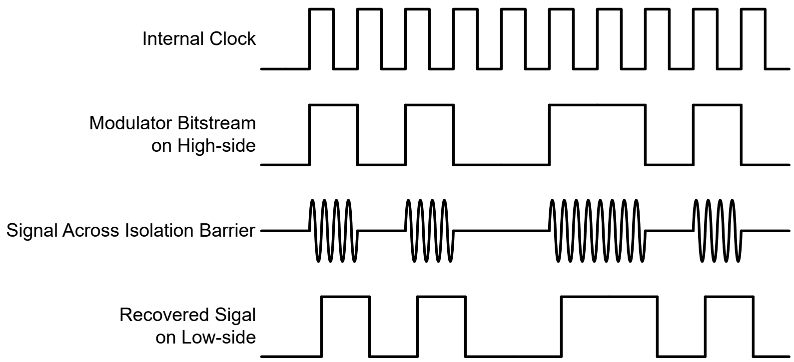


図 8-1. OOK-Based Modulation Scheme

8.3.3 Analog Output

The AMC1311 provides a differential analog output on the OUTP and OUTN pins. For input voltages of V_{IN} in the range from –0.1 V to +2 V, the device provides a linear response with a nominal gain of 1. For example, for an input voltage of 2 V, the differential output voltage (V_{OUTP} – V_{OUTN}) is 2 V. At zero input (IN shorted to GND1), both pins output the same common-mode output voltage V_{CMout}, as specified in the *Electrical Characteristics* table. For input voltages greater than 2 V but less than approximately 2.5 V, the differential output voltage continues to increase but with reduced linearity performance. The outputs saturate at a differential output voltage of $V_{CLIPout}$, as shown in 図 8-2, if the input voltage exceeds the $V_{Clipping}$ value.

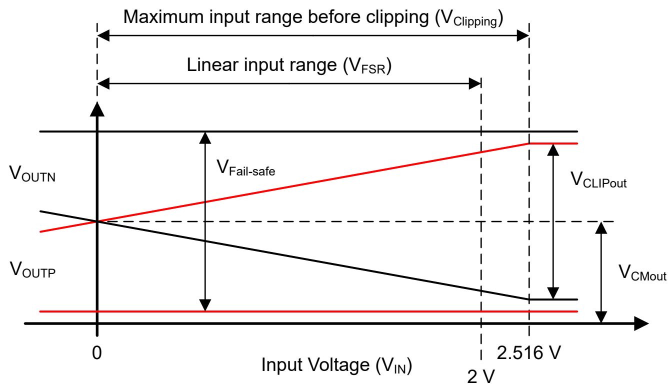


図 8-2. Output Behavior of the AMC1311

The AMC1311 output offers a fail-safe feature that simplifies diagnostics on a system level. 図 8-2 shows the fail-safe mode, in which the AMC1311 outputs a negative differential output voltage that does not occur under normal operating conditions. The fail-safe output is active in three cases:

- When the high-side supply VDD1 of the AMC1311 device is missing
- When the high-side supply VDD1 falls below the undervoltage threshold $VDD1_{UV}$
- When the SHTDN pin is pulled high

Use the maximum $V_{Fail\text{-}safe}$ voltage specified in the *Electrical Characteristics* table as a reference value for fail-safe detection on a system level.

8.4 Device Functional Modes

The AMC1311 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The high input impedance, low input bias current, low AC and DC errors, and low temperature drift make the AMC1311 a high-performance solution for industrial applications where voltage sensing in the presence of high common-mode voltage levels is required.

9.2 Typical Application

図 9-1 shows the AMC1311 in a typical application. The DC bus voltage is divided down to an approximate 2-V level across the bottom resistor (RSNS) of a high-impedance resistive divider that is sensed by the AMC1311. The AMC1311 digitizes the analog input signal on the high-side, transfers the data across the isolation barrier to the low-side, reconstructs the analog signal, and presents this signal as a differential voltage signal on the output pins.

The high-impedance input and the high common-mode transient immunity (CMTI) of the AMC1311 ensure reliable and accurate operation even in high-noise environments.

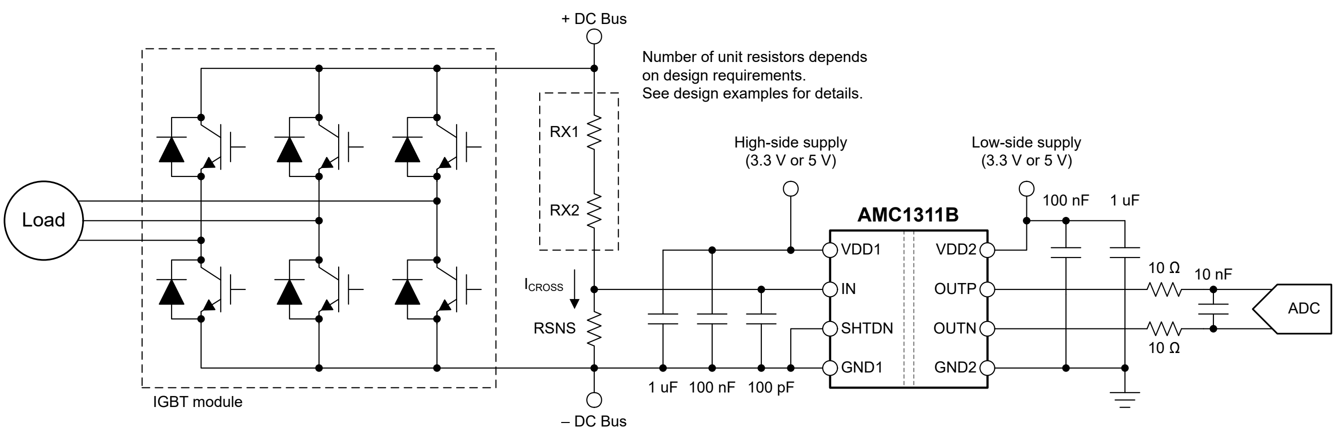


図 9-1. Using the AMC1311 for DC Link Voltage Sensing in Frequency Inverters

9.2.1 Design Requirements

表 9-1 lists the parameters for this typical application.

表 9-1. Design Requirements

PARAMETER	VALUE
System input voltage	Single phase, 230 V, 50 Hz
Maximum DC link voltage	400 V
High-side supply voltage	3.3 V or 5 V
Low-side supply voltage	3.3 V or 5 V
Maximum resistor operating voltage	75 V
Voltage drop across the sense resistor (RSNS) for a linear response	2 V (maximum)
Current through the resistive divider, I_{CROSS}	100 µA (maximum)

9.2.2 Detailed Design Procedure

The 100-µA, cross-current requirement at the maximum DC link voltage (400 V) determines that the total impedance of the resistive divider is 4 MΩ. The impedance of the resistive divider is dominated by the top portion (shown exemplary as RX1 and RX2 in 図 9-1) and the voltage drop across RSNS can be neglected for a moment. The maximum allowed voltage drop per unit resistor is specified as 75 V; therefore, the minimum number of unit resistors in the top portion of the resistive divider is 400 V / 75 V = 6. The calculated unit value is 4 MΩ / 6 = 666 kΩ and the next closest value from the E96 series is 665 kΩ.

RSNS is sized such that the voltage drop across the resistor at the maximum DC link voltage (400 V) equals the linear full-scale range input voltage (V_{FSR}) of the AMC1311, which is 2 V. This voltage is calculated as RSNS = V_{FSR} / ($V_{DC\text{-}link,\ max}$ – V_{FSR}) × R_{TOP}, where R_{TOP} is the total value of the top resistor string (6 × 665 kΩ = 3990 kΩ). RSNS is calculated as 20.05 kΩ and matches a value from the E96 series.

表 9-2. Resistor Value Example

PARAMETER	VALUE
Unit resistor R_X	665 kΩ
Number of unit resistors	6
Sense resistor RSNS	20.05 kΩ
Resulting current through resistive divider I_{CROSS}	99.7 µA
Resulting voltage drop across sense resistor	2.000 V
Power dissipated in unit resistor RX	6.6 mW
Total power dissipated in resistive divider	39.9 mW

9.2.2.1 Input Filter Design

Placing an RC filter in front of the isolated amplifier improves signal-to-noise performance of the signal path. In practice, however, the impedance of the resistor divider is high and only a small-value filter capacitor can be used to not limit the signal bandwidth to an unacceptable low value. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20 MHz) of the internal ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter

Most voltage-sensing applications use high-impedance resistor dividers in front of the isolated amplifier to scale down the input voltage. In this case, a single capacitor (as shown in 図 9-2) is sufficient to filter the input signal.

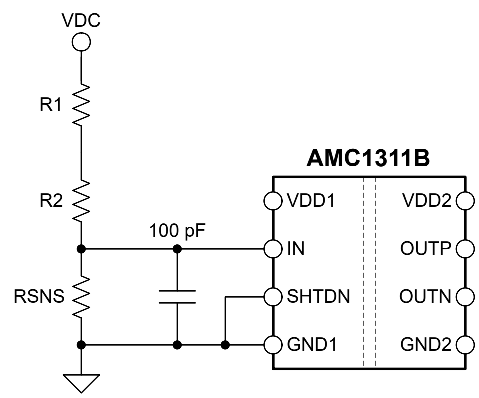


図 9-2. Input Filter

9.2.2.2 Differential to Single-Ended Output Conversion

図 9-3 shows an example of a TLV900x-based signal conversion and filter circuit for systems using single-ended input ADCs to convert the analog output voltage into digital. With R1 = R2 = R3 = R4, the output voltage equals (V_{OUTP} – V_{OUTN}) + V_{REF}. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance. For most applications, R1 = R2 = R3 = R4 = 3.3 kΩ and C1 = C2 = 330 pF yields good performance.

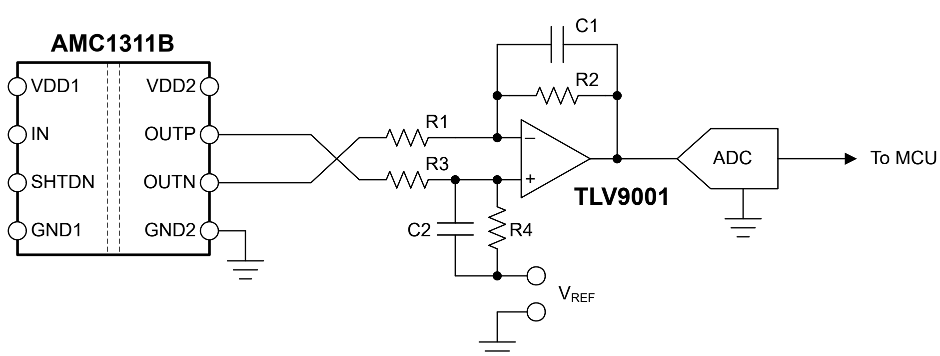


図 9-3. Connecting the AMC1311 Output to a Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guides, available for download at www.ti.com.

9.2.3 Application Curve

One important aspect of system design is the effective detection of an overvoltage condition to protect switching devices and passive components from damage. To power off the system quickly in the event of an overvoltage condition, a low delay caused by the isolated amplifier is required. 図 9-4 shows the typical full-scale step response of the AMC1311.

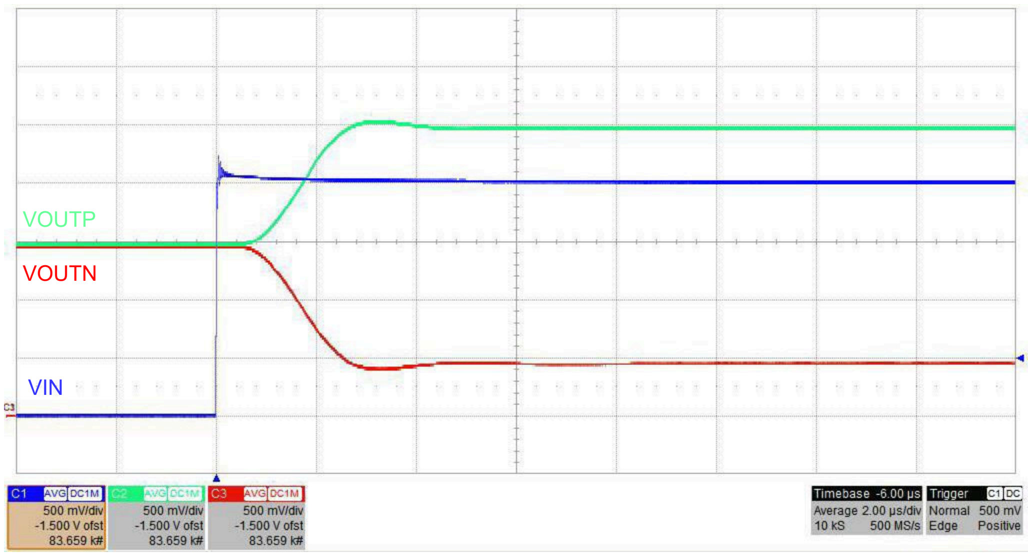


図 9-4. Step Response of the AMC1311

9.3 What To Do and What Not To Do

Do not leave the analog input (IN pin) of the AMC1311 unconnected (floating) when the device is powered up on the high-side. If the device input is left floating, the bias current may generate a negative input voltage that exceeds the specified input voltage range, causing the output of the device to be invalid.

Do not connect protection diodes to the input (IN pin) of the AMC1311. Diode leakage current can introduce significant measurement error especially at high temperatures. The input pin is protected against high voltages by its ESD protection circuit and the high impedance of the external restive divider.

10 Power Supply Recommendations

In a typical application, the high-side (VDD1) of the AMC1311 is powered from an already existing, high-side, ground-referenced, 3.3-V or 5-V power supply in the system. Alternatively, the high-side supply can be generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings.

The AMC1311 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100-nF capacitor (C1) parallel to a low-ESR, 1-µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100-nF capacitor (C3) parallel to a low-ESR, 1-µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. 図 10-1 shows the proper decoupling layout for the AMC1311.

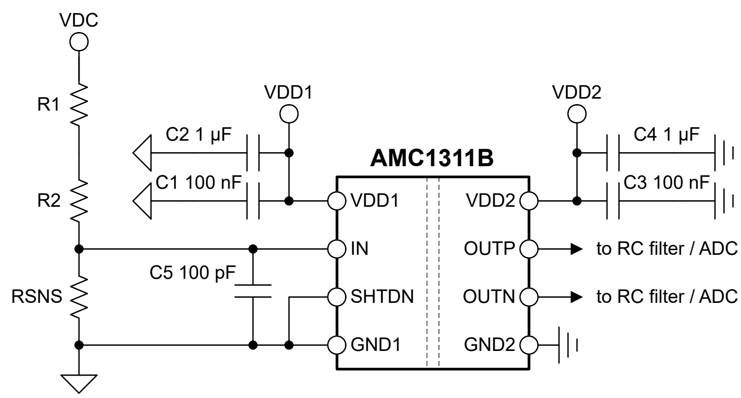


図 10-1. Decoupling of the AMC1311

Capacitors must provide adequate effective capacitance under the applicable DC bias conditions they experience in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of their nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

11 Layout

11.1 Layout Guidelines

図 11-1 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC1311 supply pins) and placement of the other components required by the device. For best performance, place the sense resistor close to the device input pin (IN).

11.2 Layout Example

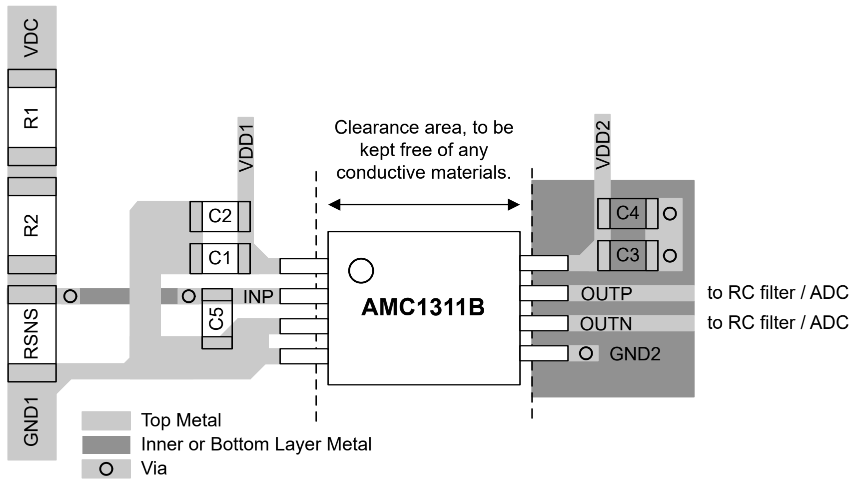


図 11-1. Recommended Layout of the AMC1311

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instruments, *TLV900x Low-Power, RRIO, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *SN6501 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *AMC1311EVM Users Guide*
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC1311BDWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311BDWV.A	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311BDWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311BDWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311BDWVRG4	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311BDWVRG4.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311B
AMC1311DWV	Active	Production	SOIC (DWV) | 8	64 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311
AMC1311DWVR	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311
AMC1311DWVR.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	1311
AMC1311DWVRG4	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311
AMC1311DWVRG4.A	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-55 to 125	1311

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF AMC1311 :

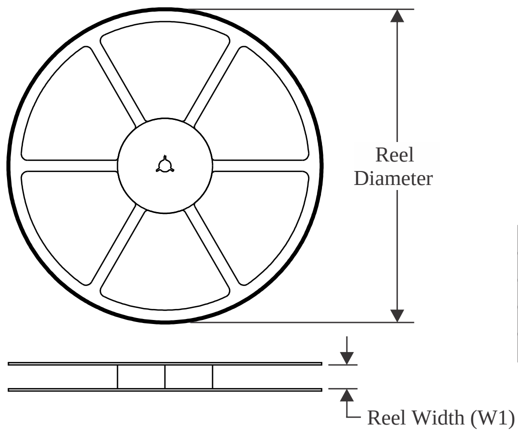
- Automotive : AMC1311-Q1

NOTE: Qualified Version Definitions:

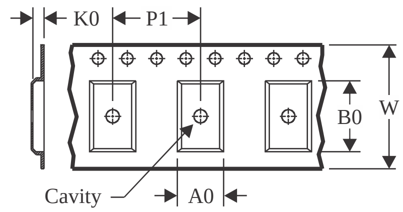
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

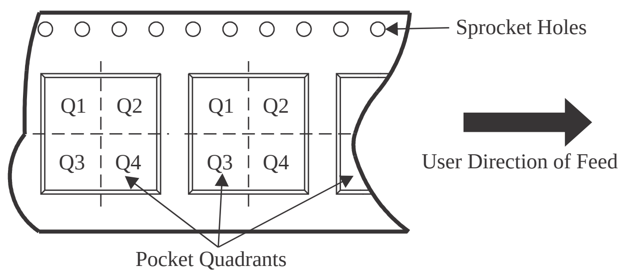


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

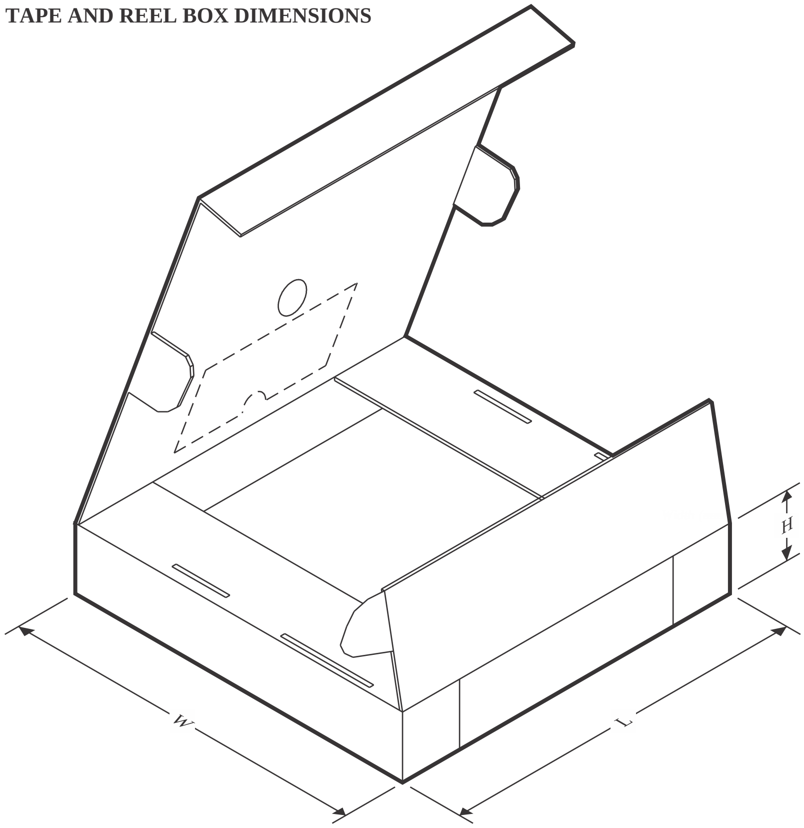
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1311BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1311BDWVRG4	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1311DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1
AMC1311DWVRG4	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

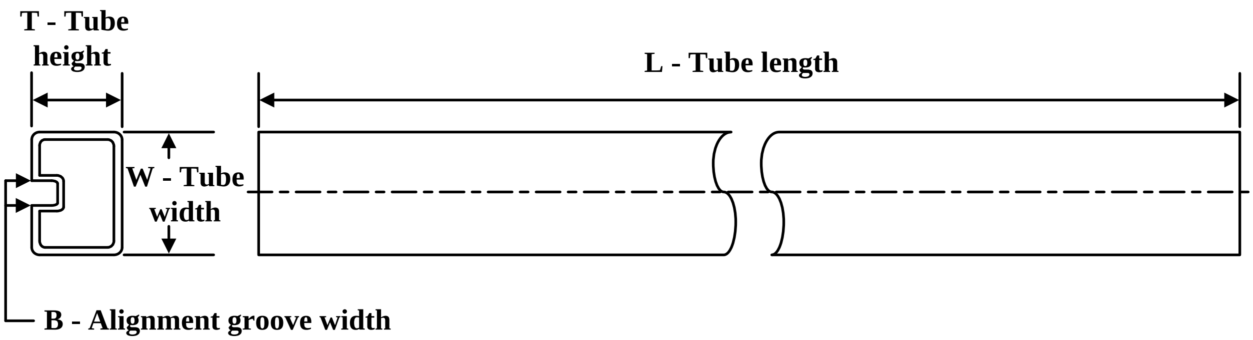
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

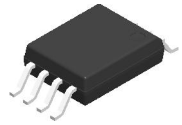
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1311BDWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1311BDWVRG4	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1311DWVR	SOIC	DWV	8	1000	353.0	353.0	32.0
AMC1311DWVRG4	SOIC	DWV	8	1000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

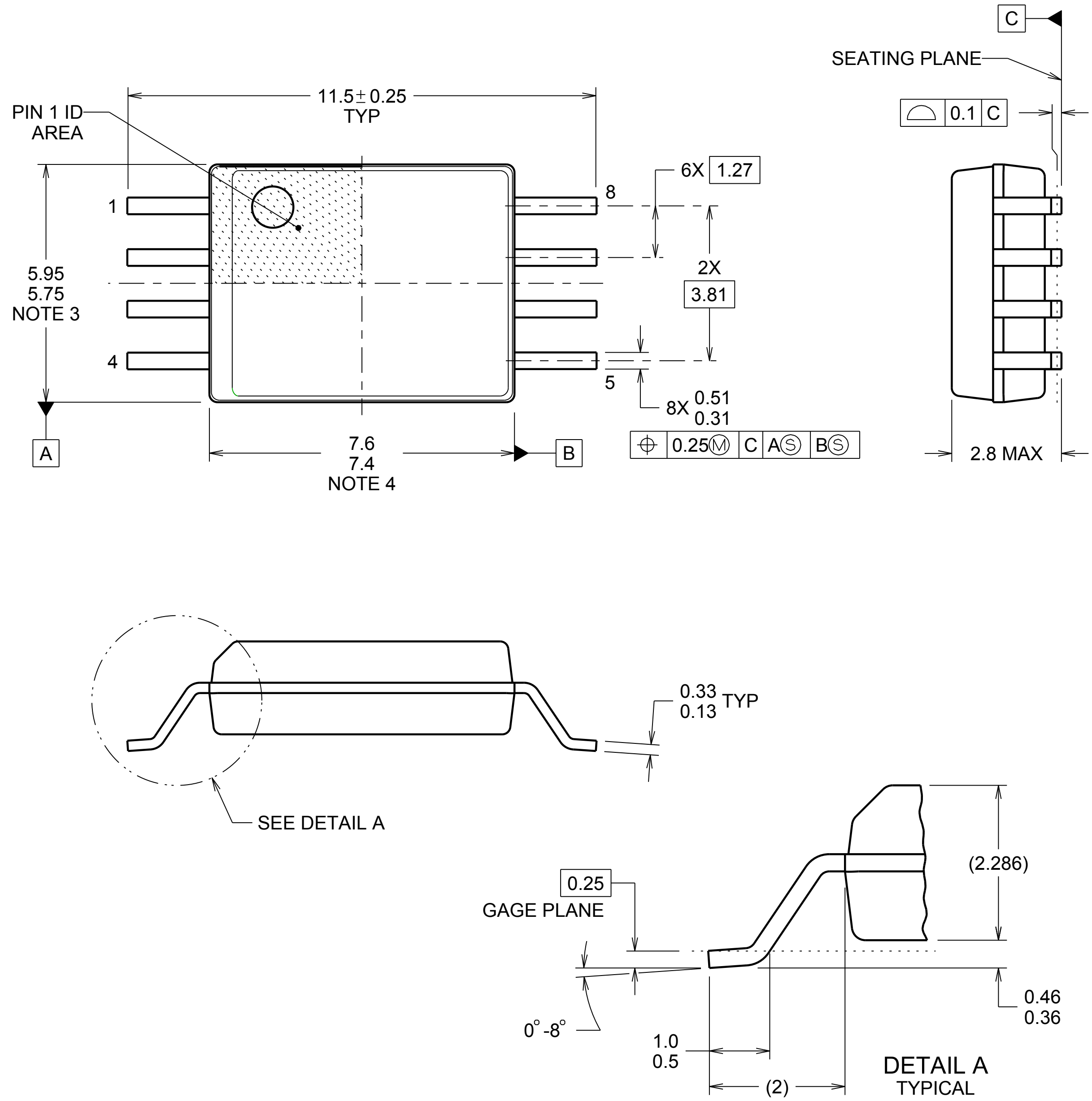
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
AMC1311BDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1311BDWV.A	DWV	SOIC	8	64	505.46	13.94	4826	6.6
AMC1311DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6



DWV0008A

SOIC - 2.8 mm max height

SOIC



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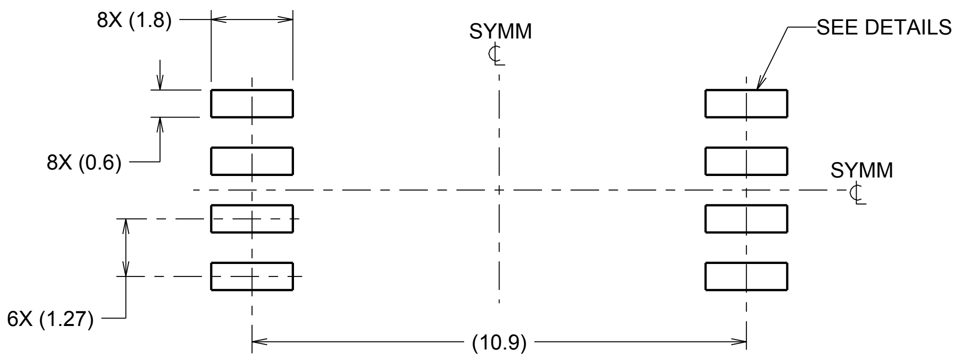
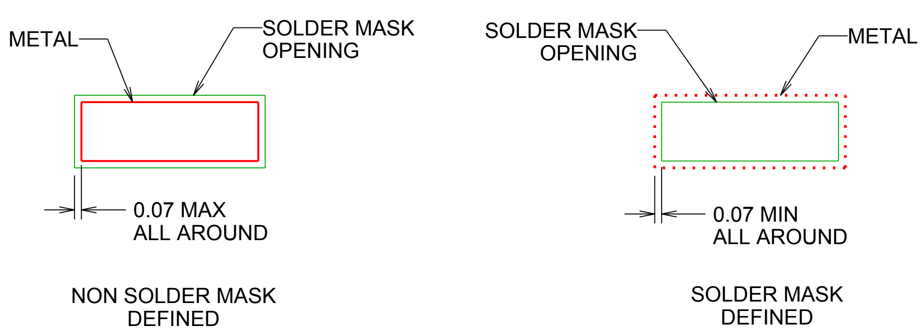
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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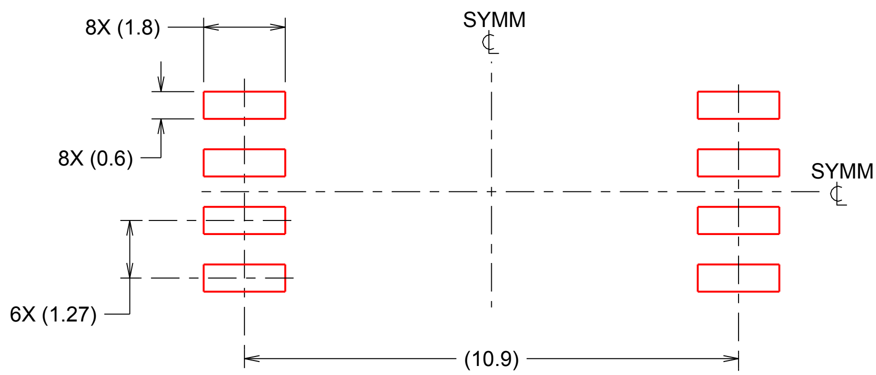
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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