bq25700A SMBusマルチケミストリ・バッテリ昇降圧型充電コントローラ、システム電力モニタおよびプロセッサ過熱モニタ搭載

1 特長

- 1～4セルのバッテリを広範囲の入力電源から充電
  - 3.5V～24Vの入力動作電圧範囲
  - USB2.0、USB 3.0、USB 3.1 (Type C)、USB_PD入力電流設定に対応
  - 降圧と昇圧の動作間のシームレスな移行
  - ソース過負荷に対する入力電流および電圧のレギュレーション(IDPMおよびVDPM)
- 電力/電流モニタによるCPUスロットル処理
  - 包括的なPROCHOTプロファイル、IMVP8準拠
  - 入力およびバッテリ電流モニタ
  - システム電力モニタ、IMVP8準拠
- Narrow-VDC (NVDC)電力パスの管理
  - バッテリ未接続または深放電状態でも即時オン
  - アダプタの過負荷時にバッテリでシステムを補完
- バッテリからUSBポートへの電源供給(USB OTG)
  - 4.48V～20.8VでUSB PD互換の出力
  - 最大6.35Aの出力電流制限
- 800kHzまたは1.2MHzに設定可能なスイッチング周波数により1µH～3.3µHのインダクタに対応
- ホスト制御インターフェイスによる柔軟なシステム構成
  - SMBus (bq25700A)ポートによる最適なシステム性能およびステータス・レポート
  - EC制御なしでハードウェア・ピンにより入力電流制限を設定
- 内蔵されたADCにより電圧、電流、電力を監視
- 高精度のレギュレーションと監視
  - ±0.5%の充電電圧レギュレーション
  - ±2%の入力/充電電流レギュレーション
  - ±2%の入力/充電電流監視
  - ±5%の電力監視
- 安全性
  - サーマル・シャットダウン
  - 入力、システム、バッテリの過電圧保護
  - MOSFETインダクタの過電流保護
- バッテリの低い静止電流
- 入力電流最適化(ICO)により最大の入力電力を抽出
- 任意の化学方式のバッテリを充電: Li+、LiFePO4、NiCd、NiMH、鉛蓄電池
- パッケージ: 32ピン4×4 WQFN

2 アプリケーション

- ウルトラブック、ノートブックPC、脱着可能PC、タブレットPC、パワー・バンク
- 産業用および医療用機器
- 充電式バッテリ搭載の携帯機器

3 概要

bq25700Aは同期整流NVDCバッテリ昇降圧型充電コントローラで、スペースに制約があり多種類のバッテリに対応する充電アプリケーション向けに、部品数が少なく、効率の高いソリューションを構築できます。

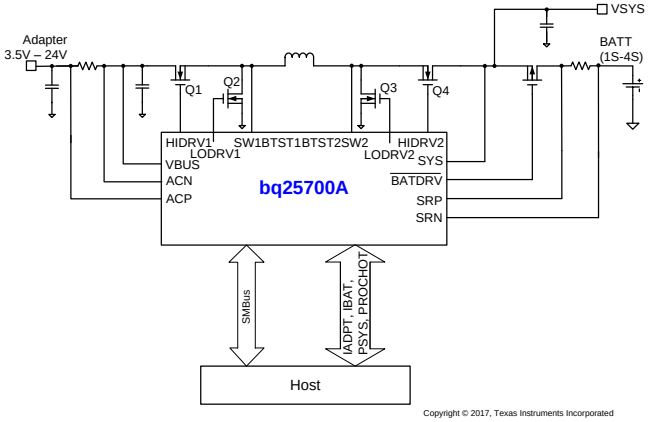
NVDC-1構成により、システムをバッテリの電圧にレギュレートしながら、システムの最低電圧を下回らないように維持できます。バッテリが完全に放電した場合や取り外された場合でも、システムは動作を続けられます。負荷電力が入力電源の定格を超過すると、バッテリが補完モードに移行し、システムの故障を防止します。

製品情報 (1)

型番	パッケージ	本体サイズ(公称)
bq25700A	WQFN (32)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

アプリケーション図



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2017年5月発行のものから更新 **Page**

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- 「概要」の「入力電源の過負荷」を「システムの故障」に 変更 ... 1
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- Changed $V_{(IADP)}$ to $V_{(IADPT)}$ in IADPT description ... 6
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- Changed REG0x3D to REG0x3B in $V_{OTG_REG_ACC}$ Test Conditions in Electrical Characteristics ... 11
- Changed REG0x12[15] = 0 to REG0x12[15] = 1 in Test Conditions for $I_{BAT_BATFET_ON}$ ... 11
- Changed REG0x12[15] = 0 to REG0x12[15] = 1 in Test Conditions for $I_{BAT_BATFET_ON}$ ... 11
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- 変更 18.5V to 19.5V in 3S row SYSOVP column in 表 1 ... 23
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改訂履歴 (continued)

- 変更 subscript of I_{LIM2_VTH} in Input Overcurrent Protection (ACOC) 28
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- 追加 REG to Battery Charging 29
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- 変更 Device Address to DeviceID for FFh in 表 6 33
- 追加 <default at POR> to PWM_FREQ description in 表 7 35
- 追加 sentence to IBAT_GAIN description in 表 8 35
- 変更 LDO to internal resistor in EN_LDO description in 表 8 35
- 削除 Independent Comparator Reference in 表 10 36
- 削除 Independent Comparator Polarity in 表 10 37
- 削除 Independent Comparator Deglitch Time in 表 10 37
- 追加 independent to FORCE_LATCHOFF description in 表 10 37
- 追加 <default at POR> to BATFETOFF_ HIZ description in 表 14 40
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- 追加 $\overline{\text{PROCHOT}}$ Pulse Extension Enable to EN_PROCHOT_EXT description in 表 16 41
- 追加 There is a 128 mA offset. to IDCHG_VTH description in 表 17 43
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- 追加 paragraph to IIN_HOST Register With 10-mΩ Sense Resistor (SMBus address = 3Fh) [reset = 4000h] 55
- 変更 Minimum System Voltage from 614 mV to 6144 mV in Design Requirements 66
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5 概要（続き）

bq25700AはUSBアダプタ、高電圧USB PDソース、従来型のアダプタなど、広範な入力電源からバッテリを充電します。

電源投入時に、充電器は電源およびバッテリの状況に基づいてコンバータを降圧、昇圧、昇降圧型のいずれかの構成に設定します。充電器はホストの制御なしに、降圧、昇圧、昇降圧型の構成間を自動的に遷移します。

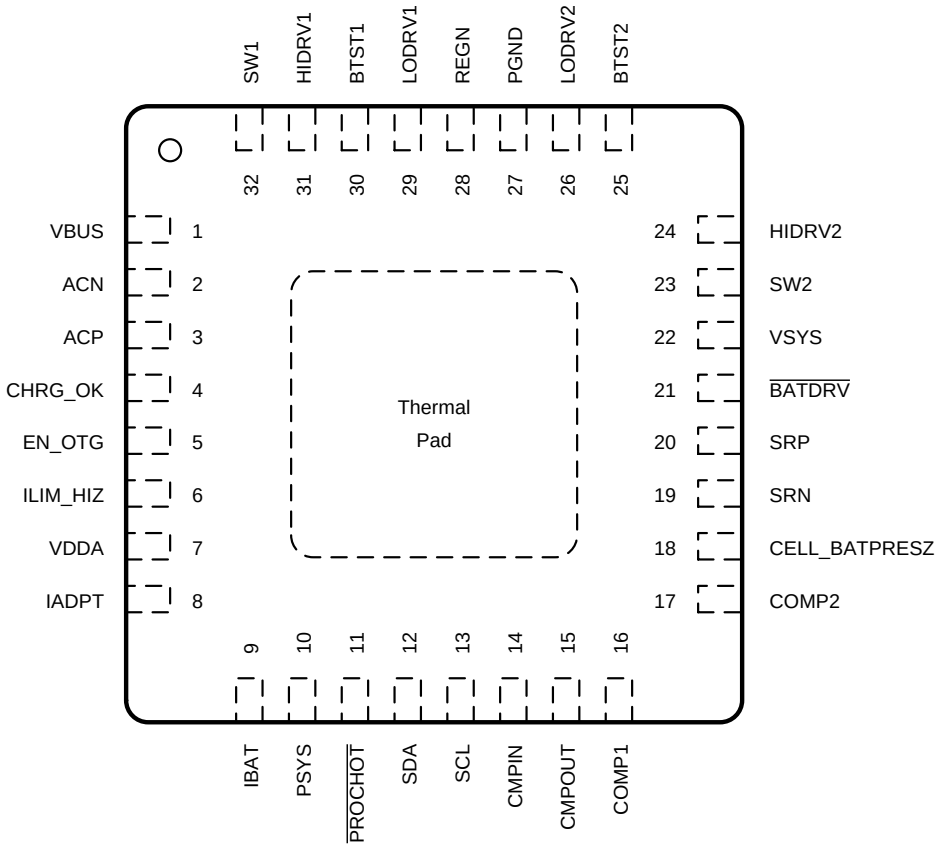
入力電源が存在しないとき、bq25700Aは1～4セルのバッテリからのOn-the-Go (OTG)機能をサポートし、VBUS上に4.48V～20.8Vを出力します。OTGモードでは、充電器は出力電圧と出力電流をレギュレートします。

bq25700Aはアダプタの電流、バッテリの電流、システムの電力を監視します。柔軟にプログラムされる$\overline{\text{PROCHOT}}$出力は、必要に応じてスロットル・バックのためCPUへ直接接続できます。

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6 Pin Configuration and Functions

RSN Package
32-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
ACN	2	PWR	Input current sense resistor negative input. The leakage on ACP and ACN are matched. The series resistors on the ACP and ACN pins are placed between sense resistor and filter cap. Refer to *Application and Implementation* for ACP/ACN filter design.
ACP	3	PWR	Input current sense resistor positive input. The leakage on ACP and ACN are matched. The series resistors on the ACP and ACN pins are placed between sense resistor and filter cap. Refer to *Application and Implementation* for ACP/ACN filter design.
$\overline{\text{BATDRV}}$	21	O	P-channel battery FET (BATFET) gate driver output. It is shorted to VSYS to turn off the BATFET. It goes 10 V below VSYS to fully turn on BATFET. BATFET is in linear mode to regulate VSYS at minimum system voltage when battery is depleted. BATFET is fully on during fast charge and supplement mode.
BTST1	30	PWR	Buck mode high side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW1 and BTST1. The bootstrap diode between REGN and BTST1 is integrated.
BTST2	25	PWR	Boost mode high side power MOSFET driver power supply. Connect a 0.047-µF capacitor between SW2 and BTST2. The bootstrap diode between REGN and BTST2 is integrated.
CELL_BATPRESZ	18	I	Battery cell selection pin for 1–4 cell battery setting. CELL_BATPRESZ pin is biased from VDDA. CELL_BATPRESZ pin also sets SYSOVP threshold to 5 V for 1-cell, 12 V for 2-cell, and 19.5 V for 3-cell/4-cell. CELL_BATPRESZ pin is pulled below $V_{CELL_BATPRESZ_FALL}$ to indicate battery removal. The device exits LEARN mode, and disables charge. REG0x15() goes back to default.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
CHRG_OK	4	O	Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via 10-kΩ resistor. When VBUS rises above 3.5V or falls below 24.5V, CHRG_OK is HIGH after 50ms deglitch time. When VBUS is falls below 3.2 V or rises above 26 V, CHRG_OK is LOW. When fault occurs, CHRG_OK is asserted LOW.
CMPIN	14	I	Input of independent comparator. The independent comparator compares the voltage sensed on CMPIN pin to internal reference, and its output is on CMPOUT pin. Internal reference, output polarity and deglitch time is selectable by SMBus. With polarity HIGH (REG0x30[6] = 1), place a resistor between CMPIN and CMPOUT to program hysteresis. With polarity LOW (REG0x30[6] = 0), the internal hysteresis is 100 mV. If the independent comparator is not in use, tie CMPIN to ground.
CMPOUT	15	O	Open-drain output of independent comparator. Place pullup resistor from CMPOUT to pullup supply rail. Internal reference, output polarity and deglitch time are selectable by SMBus.
COMP2	17	I	Buck boost converter compensation pin 2. Refer to bq25700 EVM schematic for COMP2 pin RC network.
COMP1	16	I	Buck boost converter compensation pin 1. Refer to bq25700 EVM schematic for COMP1 pin RC network.
EN_OTG	5	I	Active HIGH to enable OTG mode. When EN_OTG pin is HIGH and REG0x32[13] is HIGH, OTG can be enabled, refer to *USB On-The-Go (OTG)* for details of how to enable OTG function
HIDRV1	31	O	Buck mode high side power MOSFET (Q1) driver. Connect to high side n-channel MOSFET gate.
HIDRV2	24	O	Boost mode high side power MOSFET(Q4) driver. Connect to high side n-channel MOSFET gate.
IADPT	8	I/O	Buffered adapter current output. $V_{(IADPT)}$ = 20 or 40 × ($V_{(ACP)}$ – $V_{(ACN)}$). With ratio selectable in REG0x12[4]. Place a resistor from the IADPT pin to ground corresponding to inductor in use. For 2.2 µH, the resistor is 137 kΩ. Place 100-pF or less ceramic decoupling capacitor from IADPT pin to ground. IADPT output voltage is clamped below 3.3 V.
IBAT	9	O	Buffered battery current selected by SMBus. $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRP)}$ – $V_{(SRN)}$) for charge current, or $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRN)}$ – $V_{(SRP)}$) for discharge current, with ratio selectable in REG0x12[3]. Place 100-pF or less ceramic decoupling capacitor from IBAT pin to ground. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V.
ILIM_HIZ	6	I	Input current limit input. Program ILIM_HIZ voltage by connecting a resistor divider from supply rail to ILIM_HIZ pin to ground. The pin voltage is calculated as: $V_{(ILIM_HIZ)}$ = 1 V + 40 × IDPM × RAC, in which IDPM is the target input current. The input current limit used by the charger is the lower setting of ILIM_HIZ pin and REG0x3F(). When the pin voltage is below 0.4 V, the device enters Hi-Z mode with low quiescent current. When the pin voltage is above 0.8 V, the device is out of Hi-Z mode.
LODRV1	29	O	Buck mode low side power MOSFET (Q2) driver. Connect to low side n-channel MOSFET gate.
LODRV2	26	O	Boost mode low side power MOSFET (Q3) driver. Connect to low side n-channel MOSFET gate.
PGND	27	GND	Device power ground.
$\overline{\text{PROCHOT}}$	11	O	Active low open drain output of processor hot indicator. It monitors adapter input current, battery discharge current, and system voltage. After any event in the $\overline{\text{PROCHOT}}$ profile is triggered, a pulse is asserted. The minimum pulse width is adjustable in REG0x33[5:2].
PSYS	10	O	Current mode system power monitor. The output current is proportional to the total power from the adapter and battery. The gain is selectable through SMBus. Place a resistor from PSYS to ground to generate output voltage. This pin can be floating if not in use. Its output voltage is clamped below 3.3 V. Place a capacitor in parallel with the resistor for filtering.
REGN	28	PWR	6-V linear regulator output supplied from VBUS or VSYS. The LDO is active when VBUS above V_{VBUS_CONVEN}. Connect a 2.2- or 3.3-µF ceramic capacitor from REGN to power ground. REGN pin output is for power stage gate drive.
SCL	13	I	SMBus clock input. Connect to clock line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to SMBus specifications.
SDA	12	I/O	SMBus open-drain data I/O. Connect to data line from the host controller or smart battery. Connect a 10-kΩ pullup resistor according to SMBus specifications.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NUMBER		
SRN	19	PWR	Charge current sense resistor negative input. SRN pin is for battery voltage sensing as well. Connect SRN pin with optional 0.1-μF ceramic capacitor to GND for common-mode filtering. Connect a 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched. For reverse battery plug-in protection, 10-Ω series resistors are placed on SRP and SRN.
SRP	20	PWR	Charge current sense resistor positive input. Connect 0.1-μF ceramic capacitor from SRP to SRN to provide differential mode filtering. The leakage current on SRP and SRN are matched. For reverse battery plug-in protection, 10-Ω series resistors are placed on SRP and SRN. Connect SRP pin with optional 0.1-uF ceramic capacitor to GND for common-mode filtering.
SW1	32	PWR	Buck mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
SW2	23	PWR	Boost mode high side power MOSFET driver source. Connect to the source of the high side n-channel MOSFET.
VBUS	1	PWR	Charger input voltage. An input low pass filter of 1Ω and 0.47 μF (minimum) is recommended.
VDDA	7	PWR	Internal reference bias pin. Connect a 10-Ω resistor from REGN to VDDA and a 1-μF ceramic capacitor from VDDA to power ground.
VSYS	22	PWR	Charger system voltage sensing. The system voltage regulation limit is programmed in REG0x15() and REG0x3E().
Thermal pad	–	–	Exposed pad beneath the IC. Analog ground and power ground star-connected near the IC's ground. Always solder thermal pad to the board, and have vias on the thermal pad plane connecting to power ground planes. It also serves as a thermal pad to dissipate the heat.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Voltage	SRN, SRP, ACN, ACP, VBUS, VSYS, $\overline{\text{BATDRV}}$	–0.3	30	V
	SW1, SW2	–2.0	30	
	BTST1, BTST2, HIDRV1, HIDRV2	–0.3	36	
	LODRV1, LODRV2 (2% duty cycle)	–4.0	7	
	HIDRV1, HIDRV2 (2% duty cycle)	–4.0	36	
	SW1, SW2 (2% duty cycle)	–4.0	30	
	SDA, SCL, REGN, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT, EN_OTG	–0.3	7	
	$\overline{\text{PROCHOT}}$	–0.3	5.5	
	IADPT, IBAT, PSYS	–0.3	3.6	
Differential voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	–0.3	7	V
	SRP-SRN, ACP-ACN	–0.5	0.5	
Junction temperature range, T_J		–40	155	°C
Storage temperature, T_{stg}		–40	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage	ACN, ACP, VBUS	0	24	V
	SRN, SRP, VSYS, $\overline{\text{BATDRV}}$	0	19.2	
	SW1, SW2	–2	24	
	BTST1, BTST2, HIDRV1, HIDRV2	0	30	
	SDA, SCL, REGN, CHRG_OK, CELL_BATPRESZ, ILIM_HIZ, LODRV1, LODRV2, VDDA, COMP1, COMP2, CMPIN, CMPOUT	0	6.5	
	$\overline{\text{PROCHOT}}$	0	5.3	
	IADPT, IBAT, PSYS	0	3.3	
Differential voltage	BTST1-SW1, BTST2-SW2, HIDRV1-SW1, HIDRV2-SW2	0	6.5	V
	SRP-SRN, ACP-ACN	–0.35	0.35	
Junction temperature, T_J		–40	125	°C
Operating free-air temperature, T_A		–40	85	°C

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7.4 Thermal Information

THERMAL METRIC[1]		bq25700A RSN (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INPUT_OP}	Input voltage operating range		3.5		26	V
REGULATION ACCURACY						
MAX SYSTEM VOLTAGE REGULATION						
V_{SYSMAX_RNG}	System voltage regulation, measured on V_{SYS}		1.024		19.2	V
V_{SYSMAX_ACC}	System voltage regulation accuracy (charge disable)	REG0x15() = 0x41A0H (16.800 V)		V_{SRN} + 160 mV		V
			–2%		2%	
		REG0x15() = 0x3130H (12.592 V)		V_{SRN} + 160 mV		V
			–2%		2%	
		REG0x15() = 0x20D0H (8.400 V)		V_{SRN} + 160 mV		V
			–3%		3%	
		REG0x15() = 0x1060H (4.192 V)		V_{SRN} + 160 mV		V
			–3%		3%	
MINIMUM SYSTEM VOLTAGE REGULATION						
V_{SYSMIN_RNG}	System voltage regulation, measured on V_{SYS}		1.024		19.2	V
$V_{SYSMIN_REG_ACC}$	Minimum system voltage regulation accuracy (charge enable, VBAT below REG0x3E() setting)	REG0x3E() = 0x3000H		12.288		V
			–2%		2%	
		REG0x3E() = 0x2400H		9.216		V
			–2%		2%	
		REG0x3E() = 0x1800H		6.144		V
			–3%		3%	
		REG0x3E() = 0x0E00H		3.584		V
			–3%		4%	
CHARGE VOLTAGE REGULATION						
V_{BAT_RNG}	Battery voltage regulation		1.024		19.2	V
$V_{BAT_REG_ACC}$	Battery voltage regulation accuracy (charge enable) (0°C to 85°C)	REG0x15() = 0x41A0H		16.8		V
			–0.5%		0.5%	
		REG0x15() = 0x3130H		12.592		V
			–0.5%		0.5%	
		REG0x15() = 0x20D0H		8.4		V
			–0.6%		0.6%	
		REG0x15() = 0x1060H		4.192		V
			–1.1%		1.2%	

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CHARGE CURRENT REGULATION IN FAST CHARGE						
$V_{IREG_CHG_RNG}$	Charge current regulation differential voltage range	VIREG_CHG = VSRP – VSRN	0		81.28	mV
$I_{CHRG_REG_ACC}$	Charge current regulation accuracy 10-mΩ current sensing resistor, VBAT above 0x3E() setting (0°C to 85°C)	REG0x14() = 0x1000H		4096		mA
			–3%		2%	
		REG0x14() = 0x0800H		2048		mA
			–4%		3%	
		REG0x14() = 0x0400H		1024		mA
			–5%		6%	
		REG0x14() = 0x0200H		512		mA
			–12%		12%	
CHARGE CURRENT REGULATION IN LDO MODE						
I_{CLAMP}	Pre-charge current clamp	CELL 2s-4s		384		mA
		CELL 1 s, V_{SRN} < 3 V		384		mA
		CELL 1 s, 3 V < V_{SRN} < VSYSMIN		2		A
$I_{PRECHRG_REG_ACC}$	Pre-charge current regulation accuracy with 10-Ω SRP/SRN series resistor, VBAT below REG0x3E() setting (0°C to 85°C)	REG0x14() = 0x0180H		384		mA
		2S-4S	–15%		15%	
		1S	–25%		25%	
		REG0x14() = 0x0100H		256		mA
		2S-4S	–20%		20%	
		1S	–35%		35%	
		REG0x14() = 0x00C0H		192		mA
		2S-4S	–25%		25%	
		1S	–50%		50%	
		REG0x14() = 0x0080H		128		mA
		2S-4S	–30%		30%	
$I_{LEAK_SRP_SRN}$	SRP, SRN leakage current mismatch (0°C to 85°C)		–12		10	µA
INPUT CURRENT REGULATION						
$V_{IREG_DPM_RNG}$	Input current regulation differential voltage range	$V_{IREG_DPM} = V_{ACP} – V_{ACN}$	0.5		64	mV
$I_{DPM_REG_ACC}$	Input current regulation accuracy (–40°C to 105°C) with 10-Ω ACP/ACN series resistor	REG0x3F() = 0x4FFFH	3820		4000	mA
		REG0x3F() = 0x3BFFH	2830		3000	mA
		REG0x3F() = 0x1DFFH	1350		1500	mA
		REG0x3F() = 0x09FFH	340		500	mA
$I_{LEAK_ACP_ACN}$	ACP, ACN leakage current mismatch		–16		10	µA
$V_{IREG_DPM_RNG_ILIM}$	Voltage Range for input current regulation		1		4	V
$I_{DPM_REG_ACC_ILIM}$	Input Current Regulation Accuracy on ILIM_HIZ pin V_{ILIM_HIZ} = 1 V + 40 × IDPM × R_{AC}, with 10-Ω ACP/ACN series resistor	V_{ILIM_HIZ} = 2.6 V	3800	4000	4200	mA
		V_{ILIM_HIZ} = 2.2 V	2800	3000	3200	mA
		V_{ILIM_HIZ} = 1.6 V	1300	1500	1700	mA
		V_{ILIM_HIZ} = 1.2 V	300	500	700	mA
I_{LEAK_ILIM}	I_{LIM_HIZ} pin leakage		–1		1	µA
INPUT VOLTAGE REGULATION						
$V_{IREG_DPM_RNG}$	Input voltage regulation range	Voltage on VBUS	3.2		19.52	V

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DPM_REG_ACC}$	Input voltage regulation accuracy	REG0x3D()=0x3C80H		18688		mV
			–2%		2%	
		REG0x3D()=0x1E00H		10880		mV
			–2.5%		2.5%	
		REG0x3D()=0x0500H		4480		mV
			–3%		5%	
OTG CURRENT REGULATION						
$V_{IOTG_REG_RNG}$	Input current regulation differential voltage range	$V_{IREG_DPM} = V_{ACP} – V_{ACN}$	0		81.28	mV
I_{OTG_ACC}	Input current regulation accuracy with 50-mA LSB, with 10-Ω ACP/ACN series resistor	REG0x3C() = 0x3C00H	2800	3000	3200	mA
		REG0x3C() = 0x1E00H	1300	1500	1700	mA
		REG0x3C() = 0x0A00H	300	500	700	mA
OTG VOLTAGE REGULATION						
$V_{IREG_DPM_RNG}$	Input voltage regulation range	Voltage on VBUS	4.48		20.8	V
$V_{OTG_REG_ACC}$	OTG voltage regulation accuracy	REG0x3B()=0x3CC0H		20.032		V
			–2%		2%	
		REG0x3B()=0x1D80H		12.032		V
			–2%		2%	
		REG0x3B()=0x0240H		5.056		V
			–3%		3%	
REFERENCE AND BUFFER						
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage (0 mA–60 mA)	V_{VBUS} = 10 V	5.7	6	6.3	V
$V_{DROPOUT}$	REGN voltage in drop out mode	V_{VBUS} = 5 V, I_{LOAD} = 20 mA	3.8	4.3	4.6	V
$I_{REGN_LIM_Charging}$	REGN current limit when converter is enabled	V_{VBUS} = 10 V, force V_{REGN} = 4 V	50	65		mA
C_{REGN}	REGN output capacitor required for stability	I_{LOAD} = 100 µA to 50 mA	2.2			µF
C_{VDDA}	REGN output capacitor required for stability	I_{LOAD} = 100 µA to 50 mA	1			µF
QUIESCENT CURRENT						
$I_{BAT_BATFET_ON}$	System powered by battery. BATFET on. I_{SRN} + I_{SRP} + I_{SW2}+ I_{BTST2} + I_{SW1} + I_{BTST1}+ $_{ACP}$ + I_{ACN} + I_{VBUS} + I_{VSYS}	VBAT = 18 V, REG0x12[15] = 1, in low power mode		22	45	µA
		VBAT = 18 V, REG0x12[15] = 1, REG0x30[14:13] = 01, REGN off		105	175	µA
		VBAT=18 V, REG0x12[15] = 1, REG0x30[14:13] = 10, REGN off		60	90	µA
		VBAT = 18 V, REG0x12[15] = 0, REG0x30[12] = 0, REGN on, EN_PSYS		860	1150	µA
		VBAT = 18 V, REG0x12[15] = 0, REG0x30[12] = 1, REGN on		960	1250	
$I_{AC_SW_LIGHT_buck}$	Input current during PFM in buck mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST} + I_{SW2} + I_{BTST2}	VIN = 20 V, VBAT = 12.6 V, 3 s, REG0x12[10] = 0; MOSFET Qg = 4 nC		2.2		mA

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{AC_SW_LIGHT_boost}$	Input current during PFM in boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VIN = 5 V, VBAT = 8.4 V, 2 s, REG0x12[10] = 0; MOSFET Qg = 4 nC		2.7		mA
$I_{AC_SW_LIGHT_buckboost}$	Input current during PFM in buck boost mode, no load, I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST1} + I_{SW2} + I_{BTST2}	VIN = 12 V, VBAT = 12 V, REG0x12[10] = 0; MOSFET Qg = 4 nC		2.4		mA
$I_{OTG_STANDBY}$	Quiescent current during PFM in OTG mode I_{VBUS} + I_{ACP} + I_{ACN} + I_{VSYS} + I_{SRP} + I_{SRN} + I_{SW1} + I_{BTST2} + I_{SW2} + I_{BTST2}	VBAT = 8.4 V, VBUS = 5 V, 800-kHz switching frequency, MOSFET Qg = 4 nC		3		mA
		VBAT = 8.4 V, VBUS = 12 V, 800-kHz switching frequency, MOSFET Qg = 4 nC		4.2		
		VBAT = 8.4 V, VBUS = 20 V, 800-kHz switching frequency, MOSFET Qg = 4 nC		6.2		
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	3.8		26	V
V_{IADPT_CLAMP}	I_{ADPT} output clamp voltage		3.1	3.2	3.3	V
I_{IADPT}	I_{ADPT} output current				1	mA
A_{IADPT}	Input current sensing gain	$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x12[4] = 0		20		V/V
		$V_{(IADPT)}$ / $V_{(ACP-ACN)}$, REG0x12[4] = 1		40		V/V
V_{IADPT_ACC}	Input current monitor accuracy	$V_{(ACP-ACN)}$ = 40.96 mV	–2%		2%	
		$V_{(ACP-ACN)}$ = 20.48 mV	–3%		3%	
		$V_{(ACP-ACN)}$ =10.24 mV	–6%		6%	
		$V_{(ACP-ACN)}$ = 5.12 mV	–10%		10%	
C_{IADPT_MAX}	Maximum output load capacitance				100	pF
V_{SRP/N_OP}	Battery common mode range	Voltage on SRP/SRN	2.5		18	V
V_{IBAT_CLAMP}	IBAT output clamp voltage		3.05	3.2	3.3	V
I_{IBAT}	IBAT output current				1	mA
A_{IBAT}	Charge and discharge current sensing gain on IBAT pin	$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x12[3] = 0,		8		V/V
		$V_{(IBAT)}$ / $V_{(SRN-SRP)}$, REG0x12[3] = 1,		16		V/V
$I_{IBAT_CHG_ACC}$	Charge and discharge current monitor accuracy on IBAT pin	$V_{(SRN-SRP)}$ = 40.96 mV	–2%		2%	
		$V_{(SRN-SRP)}$ = 20.48 mV	–3%		4%	
		$V_{(SRN-SRP)}$ =10.24 mV	–6%		6%	
		$V_{(SRN-SRP)}$ = 5.12 mV	–12%		12%	
C_{IBAT_MAX}	Maximum output load capacitance				100	pF
SYSTEM POWER SENSE AMPLIFIER						
V_{PSYS}	PSYS output voltage range		0		3.3	V
I_{PSYS}	PSYS output current		0		160	µA
A_{PSYS}	PSYS system gain	$V_{(PSYS)}$ / ($P_{(IN)}$+ $P_{(BAT)}$), REG0x30[9] = 1		1		µA/W

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PSYS_ACC}	PSYS gain accuracy (REG0x30[9] = 1)	Adapter only with system power = 19.5 V / 45 W, T_A = 0 to 85°C	–5%		5%	
		Adapter only with system power = 19.5 V / 45 W, T_A = –40 to 125°C	–7%		6%	
		Battery only with system power = 11 V / 44 W, T_A = 0 to 85°C	–5%		5%	
		Battery only with system power = 11 V / 44 W, T_A = –40 to 125°C	–6%		6%	
V_{PSYS_CLAMP}	PSYS clamp voltage		3		3.3	V
COMPARATOR						
VBUS UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBUS_UVLOZ}	VBUS undervoltage rising threshold	VBUS rising	2.34	2.55	2.77	V
V_{VBUS_UVLO}	VBUS undervoltage falling threshold	VBUS falling	2.2	2.4	2.6	V
$V_{VBUS_UVLO_HYST}$	VBUS undervoltage hysteresis			150		mV
V_{VBUS_CONVEN}	VBUS converter enable rising threshold	VBUS rising	3.2	3.5	3.9	V
$V_{VBUS_CONVENZ}$	VBUS converter enable falling threshold	VBUS falling	2.9	3.2	3.5	V
$V_{VBUS_CONVEN_HYST}$	VBUS converter enable hysteresis			400		mV
BATTERY UNDER VOLTAGE LOCKOUT COMPARATOR						
V_{VBAT_UVLOZ}	VBAT undervoltage rising threshold	VSRN rising	2.35	2.55	2.75	V
V_{VBAT_UVLO}	VBAT undervoltage falling threshold	VSRN falling	2.2	2.4	2.6	V
$V_{VBAT_UVLO_HYST}$	VBAT undervoltage hysteresis			150		mV
V_{VBAT_OTGEN}	VBAT OTG enable rising threshold	VSRN rising	3.3	3.55	3.75	V
V_{VBAT_OTGENZ}	VBAT OTG enable falling threshold	VSRN falling	3	3.2	3.4	V
$V_{VBAT_OTGEN_HYST}$	VBAT OTG enable hysteresis			350		mV
VBUS UNDER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS_OTG_UV}$	VBUS undervoltage falling threshold	As percentage of REG0x3B()		85.0%		
$t_{VBUS_OTG_UV}$	VBUS undervoltage deglitch time			7		ms
VBUS OVER VOLTAGE COMPARATOR (OTG MODE)						
$V_{VBUS_OTG_OV}$	VBUS overvoltage rising threshold	As percentage of REG0x3B()		105%		
$t_{VBUS_OTG_OV}$	VBUS Over-Voltage Deglitch Time			10		ms
$V_{BAT_SYSMIN_RISE}$	LDO mode to fast charge mode threshold, VSRN rising	as percentage of 0x3E()	98%	100%	102%	
$V_{BAT_SYSMIN_FALL}$	LDO mode to fast charge mode threshold, VSRN falling	as percentage of 0x3E()		97.5%		

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BAT_SYSMIN_HYST}$	Fast charge mode to LDO mode threshold hysteresis	as percentage of 0x3E()		2.5%		
BATTERY LOWV COMPARATOR (Pre-charge to Fast Charge Thresold for 1S)						
V_{BATLV_FALL}	BATLOWV falling threshold	1 s		2.80		V
V_{BATLV_RISE}	BATLOWV rising threshold			3.00		V
V_{BATLV_RHYST}	BATLOWV hysteresis			200		mV
INPUT OVER-VOLTAGE COMPARATOR (ACOVP)						
V_{ACOV_RISE}	VBUS overvoltage rising threshold	VBUS rising	25	26	27	V
V_{ACOV_FALL}	VBUS overvoltage falling threshold	VBUS falling	24	24.5	25	V
V_{ACOV_HYST}	VBUS overvoltage hysteresis			1.5		V
$t_{ACOV_RISE_DEG}$	VBUS overvoltage rising deglitch	VBUS rising to stop converter		100		µs
$t_{ACOV_FALL_DEG}$	VBUS overvoltage falling deglitch	VBUS falling to start converter		1		ms
INPUT OVER CURRENT COMPARATOR (ACOC)						
V_{ACOC}	ACP to ACN rising threshold, w.r.t. ILIM2 in REG0x33[15:11]	Voltage across input sense resistor rising, Reg0x31[2] = 1	195%	210%	225%	
V_{ACOC_FLOOR}	Measure between ACP and ACN	Set IDPM to minimum	44	50	56	mV
$V_{ACOC_CEILING}$	Measure between ACP and ACN	Set IDPM to maximum	172	180	188	mV
$t_{ACOC_DEG_RISE}$	Rising deglitch time	Deglitch time to trigger ACOC		250		µs
t_{ACOC_RELAX}	Relax time	Relax time before converter starts again		250		ms
SYSTEM OVER-VOLTAGE COMPARATOR (SYSOVP)						
V_{SYSOVP_RISE}	System overvoltage rising threshold to turn off converter	1 s	4.85	5	5.1	V
		2 s	11.7	12	12.2	
		3 s	19	19.5	20	
		4 s	19	19.5	20	
V_{SYSOVP_FALL}	System overvoltage falling threshold	1 s		4.8		V
		2 s		11.5		
		3 s		19		
		4 s		19		
I_{SYSOVP}	Discharge current when SYSOVP stop switching was triggered	on SYS		20		mA
BAT OVER-VOLTAGE COMPARATOR (BATOVP)						
V_{BATOVP_RISE}	Overvoltage rising threshold as percentage of V_{BAT_REG} in REG0x15()	1 s, 4.2 V	102.5%	104%	106%	
		2 s - 4 s	102.5%	104%	105%	
V_{BATOVP_FALL}	Overvoltage falling threshold as percentage of VBAT_REG in REG0x15()	1 s	100%	102%	104%	
		2 s - 4 s	100%	102%	103%	
V_{BATOVP_HYST}	Overvoltage hysteresis as percentage of V_{BAT_REG} in REG0x15()	1 s		2%		
		2 s - 4 s		2%		
I_{BATOVP}	Discharge current during BATOVP	on VSYS pin		20		mA

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BATOVP_RISE}	Overvoltage rising deglitch to turn off $\overline{BATDRV}$ to disable charge			20		ms
CONVERTER OVER-CURRENT COMPARATOR (Q2)						
VOCP_limit_Q2	Converter Over-Current Limit	Reg0x31[5]=1		150		mV
		Reg0x31[5]=0		210		
VOCP_limit_SYSSHORT_Q2	System Short or SRN<2.5 V	Reg0x31[5]=1		45		mV
		Reg0x31[5]=0		60		
CONVERTER OVER-CURRENT COMPARATOR (ACX)						
VOCP_limit_ACX	Converter Over-Current Limit	Reg0x31[4]=1		150		mV
		Reg0x31[4]=0		280		
VOCP_limit_SYSSHORT_ACX	System Short or SRN<2.5 V	Reg0x31[4]=1		90		mV
		Reg0x31[4]=0		150		
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT_RISE}	Thermal shutdown rising temperature	Temperature increasing		155		°C
T_{SHUTF_FALL}	Thermal shutdown falling temperature	Temperature reducing		135		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			20		°C
t_{SHUT_RDEG}	Thermal shutdown rising deglitch			100		µs
t_{SHUT_FHYS}	Thermal shutdown falling deglitch			12		ms
VSYS PROCHOT COMPARATOR						
$V_{SYS_\overline{PROCHOT}}$	V_{SYS} threshold falling threshold	Reg0x33[7:6] = 00, 1 s		2.85		V
		Reg0x33[7:6] = 00, 2–4 s		5.75		V
		Reg0x33[7:6] = 01, 1 s	2.95	3.1	3.25	V
		Reg0x33[7:6] = 01, 2–4 s	5.8	5.95	6.1	V
		Reg0x33[7:6] = 10, 1 s		3.3		V
		Reg0x33[7:6] = 10, 2–4 s		6.25		V
		Reg0x33[7:6] = 11, 1 s		3.5		V
		Reg0x33[7:6] = 11, 2–4 s		6.5		V
$t_{SYS_PRO_RISE_DEG}$	V_{SYS} rising deglitch for throttling			8		µs
ICRIT PROCHOT COMPARATOR						
V_{ICRIT_PRO}	Input current rising threshold for throttling as 10% above ILIM2 (REG0x33[15:11])	Reg0x33[15:11] = 00000	105%	110%	116%	
		Reg0x33[15:11] = 01001	142%	150%	156%	
INOM PROCHOT COMPARATOR						
V_{INOM_PRO}	INOM rising threshold as 10% above IIN (REG0x3F())		105%	110%	116%	
IDCHG PROCHOT COMPARATOR						
V_{IDCHG_PRO}	IDCHG threshold for throttling for IDSCHG of 6 A	Reg0x34[15:10] =001100		6272		mA
			95%		102%	
INDEPENDENT COMPARATOR						
V_{INDEP_CMP}	Independent comparator threshold	Reg0x30[7] = 1, CMPIN falling	1.17	1.2	1.23	V
		Reg0x30[7] = 0, CMPIN falling	2.27	2.3	2.33	V

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{INDEP_CMP_HYS}$	Independent comparator hysteresis	Reg0x3B[6] = 0, CMPIN falling		100		mV
POWER MOSFET DRIVER						
PWM OSCILLATOR AND RAMP						
F_{SW}	PWM switching frequency	Reg0x12[9] = 0	1020	1200	1380	kHz
		Reg0x12[9] = 1	680	800	920	kHz
BATFET GATE DRIVER ($\overline{BATDRV}$)						
V_{BATDRV_ON}	Gate drive voltage on BATFET		8.5	10	11.5	V
V_{BATDRV_DIODE}	Drain-source voltage on BATFET during ideal diode operation			30		mV
R_{BATDRV_ON}	Measured by sourcing 10-µA current to $\overline{BATDRV}$		3	4	6	kΩ
R_{BATDRV_OFF}	Measured by sinking 10-µA current from $\overline{BATDRV}$			1.2	2.1	kΩ
PWM HIGH SIDE DRIVER (HIDRV Q1)						
$R_{DS_HI_ON_Q1}$	High side driver (HSD) turnon resistance	$V_{BTST1} – V_{SW1}$ = 5 V		6		Ω
$R_{DS_HI_OFF_Q1}$	High side driver turnoff resistance	$V_{BTST1} – V_{SW1}$ = 5 V		1.3	2.2	Ω
$V_{BTST1_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	$V_{BTST1} – V_{SW1}$ when low side refresh pulse is requested	3.2	3.7	4.6	V
PWM HIGH SIDE DRIVER (HIDRV Q4)						
$R_{DS_HI_ON_Q4}$	High side driver (HSD) turnon resistance	$V_{BTST2} – V_{SW2}$ = 5 V		6		Ω
$R_{DS_HI_OFF_Q4}$	High side driver turnoff resistance	$V_{BTST2} – V_{SW2}$ = 5 V		1.5	2.4	Ω
$V_{BTST2_REFRESH}$	Bootstrap refresh comparator falling threshold voltage	$V_{BTST2} – V_{SW2}$ when low side refresh pulse is requested	3.3	3.7	4.6	V
PWM LOW SIDE DRIVER (LODRV Q2)						
$R_{DS_LO_ON_Q2}$	Low side driver (LSD) turnon resistance	$V_{BTST1} – V_{SW1}$ = 5.5 V		6		Ω
$R_{DS_LO_OFF_Q2}$	Low side driver turnoff resistance	$V_{BTST1} – V_{SW1}$ = 5.5 V		1.7	2.6	Ω
PWM LOW SIDE DRIVER (LODRV Q3)						
$R_{DS_LO_ON_Q3}$	Low side driver (LSD) turnon resistance	$V_{BTST2} – V_{SW2}$ = 5.5 V		7.6		Ω
$R_{DS_LO_OFF_Q3}$	Low side driver turnoff resistance	$V_{BTST2} – V_{SW2}$ = 5.5 V		2.9	4.6	Ω
INTERNAL SOFT START During Charge Enable						
SSSTEP_DAC	Soft Start Step Size			64		mA
SSSTEP_DAC	Soft Start Step Time			8		µs
INTEGRATED BTST DIODE (D1)						
V_{F_D1}	Forward bias voltage	I_F = 20 mA at 25°C		0.8		V
V_{R_D1}	Reverse breakdown voltage	I_R = 2 µA at 25°C			20	V
INTEGRATED BTST DIODE (D2)						
V_{F_D2}	Forward bias voltage	I_F = 20 mA at 25°C		0.8		V
V_{R_D2}	Reverse breakdown voltage	I_R = 2 µA at 25°C			20	V
PWM DRIVERS TIMING						

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Electrical Characteristics (continued)

over T_J = –40 to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERFACE						
LOGIC INPUT (SDA, SCL, EN_OTG)						
V_{IN_LO}	Input low threshold	SMBus			0.8	V
V_{IN_HI}	Input high threshold	SMBus (bq25700A)	2.1			V
LOGIC OUTPUT OPEN DRAIN (SDA, CHRG_OK, CMPOUT)						
V_{OUT_LO}	Output saturation voltage	5-mA drain current			0.4	V
V_{OUT_LEAK}	Leakage current	V = 7 V	–1		1	mA
LOGIC OUTPUT OPEN DRAIN SDA						
$V_{OUT_LO_SDA}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_SDA}$	Leakage Current	V = 7V	–1		1	mA
LOGIC OUTPUT OPEN DRAIN CHRG_OK						
$V_{OUT_LO_CHRG_OK}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_CHRG_OK}$	Leakage Current	V = 7V	–1		1	mA
LOGIC OUTPUT OPEN DRAIN CMPOUT						
$V_{OUT_LO_CMPOUT}$	Output Saturation Voltage	5 mA drain current			0.4	V
$V_{OUT_LEAK_CMPOUT}$	Leakage Current	V = 7V	–1		1	mA
LOGIC OUTPUT OPEN DRAIN ($\overline{\text{PROCHOT}}$)						
$V_{OUT_LO_PROCHOT}$	Output saturation voltage	50-Ω pullup to 1.05 V / 5-mA load			300	mV
$V_{OUT_LEAK_PROCHOT}$	Leakage current	V = 5.5 V	–1		1	mA
ANALOG INPUT (ILIM_HIZ)						
V_{HIZ_LO}	Voltage to get out of HIZ mode	ILIM_HIZ pin rising	0.8			V
V_{HIZ_HIGH}	Voltage to enable HIZ mode	ILIM_HIZ pin falling			0.4	V
ANALOG INPUT (CELL_BATPRESZ)						
V_{CELL_4S}	4S	REGN = 6 V, as percentage of REGN	68.4%	75%		
V_{CELL_3S}	3S	REGN = 6 V, as percentage of REGN	51.7%	55%	65%	
V_{CELL_2S}	2S	REGN = 6 V, as percentage of REGN	35%	40%	49.1%	
V_{CELL_1S}	1S	REGN = 6 V, as percentage of REGN	18.4%	25%	31.6%	
$V_{CELL_BATPRESZ_RISE}$	Battery is present		18%			
$V_{CELL_BATPRESZ_FALL}$	Battery is removed	CELL_BATPRESZ falling			15%	
ANALOG INPUT (COMP1, COMP2)						
I_{LEAK_COMP1}	COMP1 Leakage		–120		120	nA
I_{LEAK_COMP2}	COMP2 Leakage		–120		120	nA

7.6 Timing Requirements

		MIN	TYP	MAX	UNIT
SMBus TIMING CHARACTERISTICS					
t_r	SCLK/SDATA rise time			1	µs
t_f	SCLK/SDATA fall time			300	ns
$t_{W(H)}$	SCLK pulse width high	4		50	µs
$t_{W(L)}$	SCLK Pulse Width Low	4.7			µs
$t_{SU(STA)}$	Setup time for START condition	4.7			µs
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated	4			µs

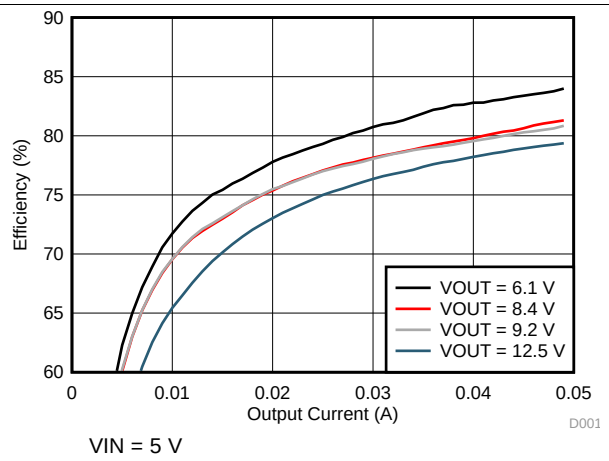
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Timing Requirements (continued)

		MIN	TYP	MAX	UNIT
$t_{SU(DAT)}$	Data setup time	250			ns
$t_{H(DTA)}$	Data hold time	300			ns
$t_{SU(STOP)}$	Setup time for STOP condition	4			µs
$t_{(BUF)}$	Bus free time between START and STOP condition	4.7			µs
$F_{S(CL)}$	Clock Frequency	10		100	KHz
HOST COMMUNICATION FAILURE					
$t_{timeout}$	SMBus bus release timeout(1)	25		35	ms
t_{BOOT}	Deglitch for watchdog reset signal	10			ms
t_{WDI}	Watchdog timeout period, ChargeOption() bit [14:13] = 01(2)	35	44	53	s
	Watchdog timeout period, ChargeOption() bit bit [14:13] = 10(2)	70	88	105	s
	Watchdog timeout period, ChargeOption() bit bit [14:13] = 11(2) (default)	140	175	210	s

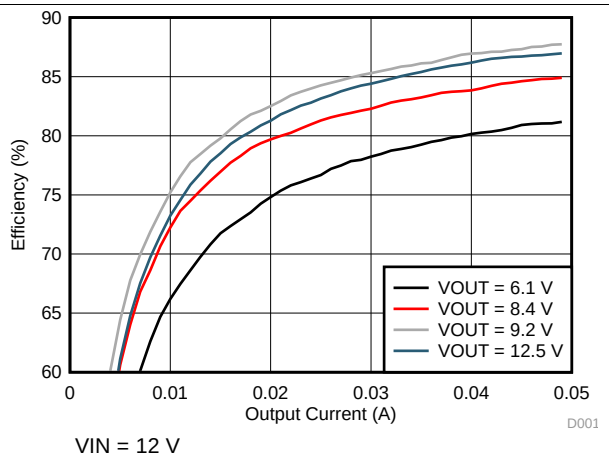
(1) Devices participating in a transfer will timeout when any clock low exceeds the 25ms minimum timeout period. Devices that have detected a timeout condition must reset the communication no later than the 35 ms maximum timeout period. Both a master and a slave must adhere to the maximum value specified as it incorporates the cumulative stretch limit for both a master (10 ms) and a slave (25 ms).
(2) User can adjust threshold via SMBus ChargeOption() REG0x12.

7.7 Typical Characteristics



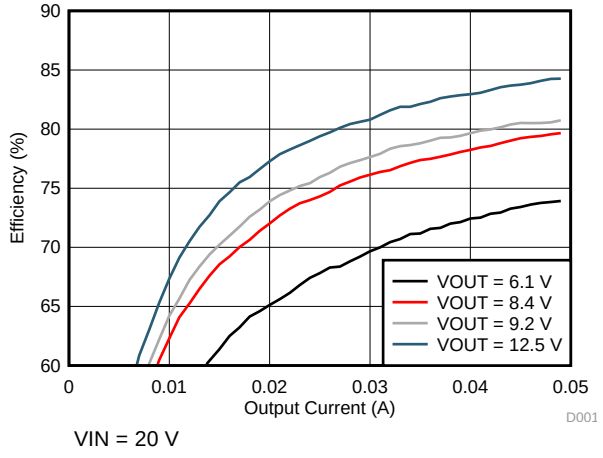
VIN = 5 V

図 1. Light Load Efficiency



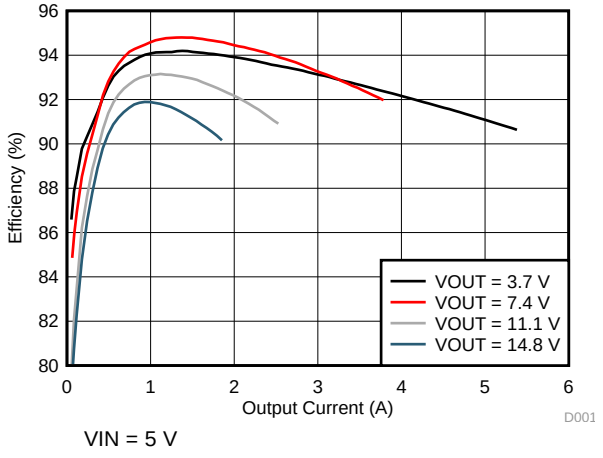
VIN = 12 V

図 2. Light Load Efficiency



VIN = 20 V

図 3. Light Load Efficiency

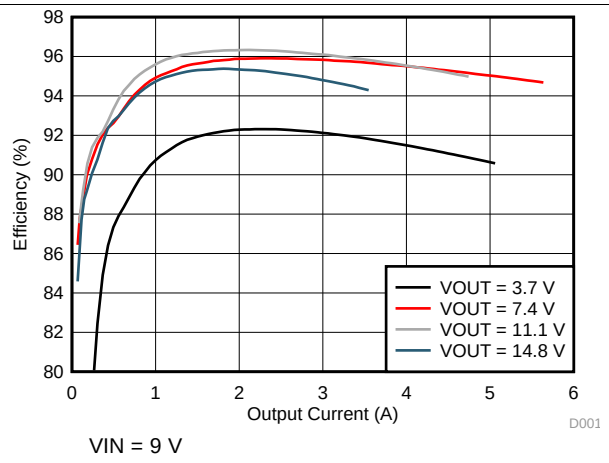


VIN = 5 V

図 4. System Efficiency

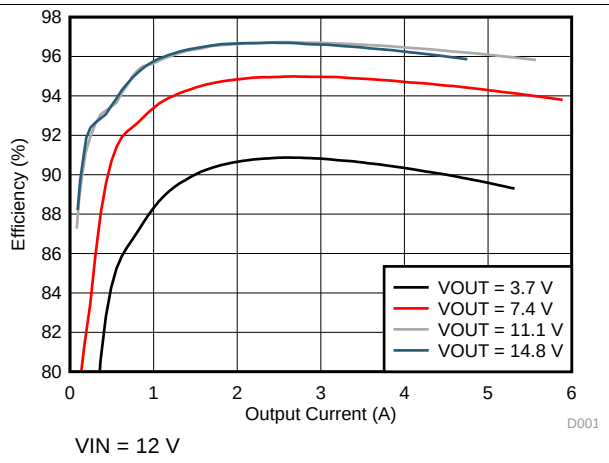
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Typical Characteristics (continued)



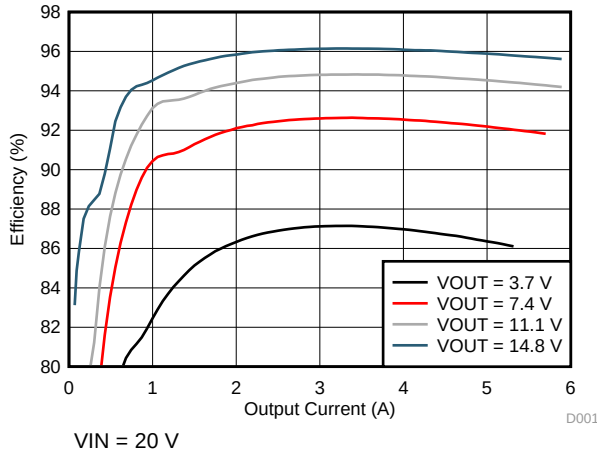
VIN = 9 V

図 5. System Efficiency



VIN = 12 V

図 6. System Efficiency



VIN = 20 V

図 7. System Efficiency

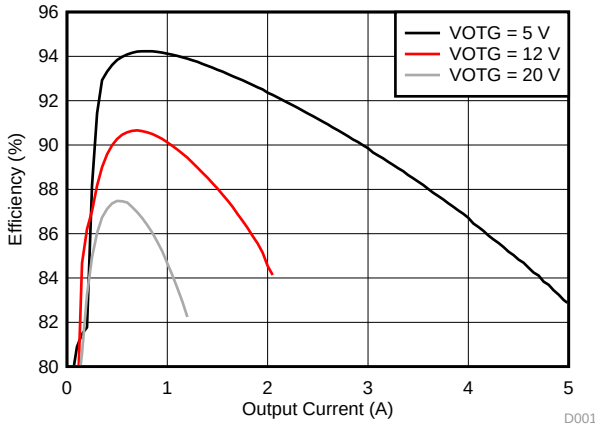


図 8. OTG Efficiency with 1S Battery

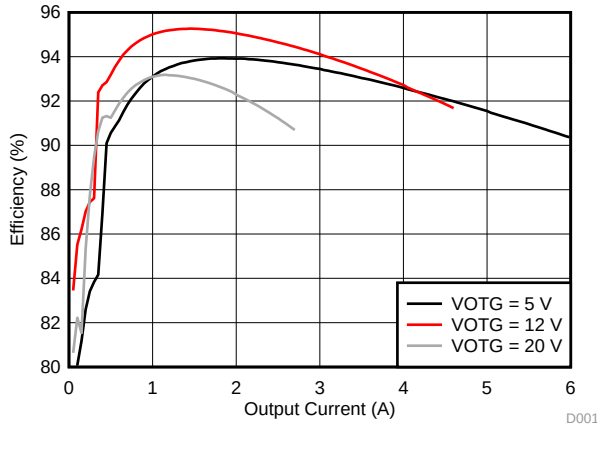


図 9. OTG Efficiency with 2S Battery

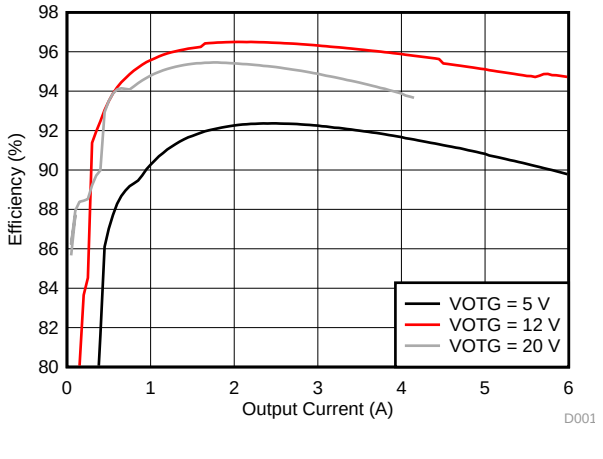


図 10. OTG Efficiency with 3S Battery

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Typical Characteristics (continued)

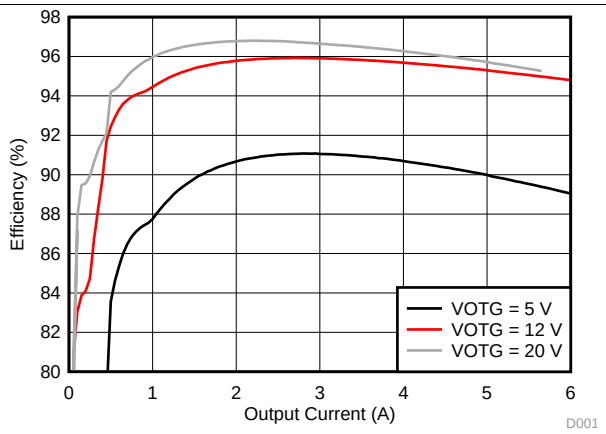


図 11. OTG Efficiency with 4S Battery

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8 Detailed Description

8.1 Overview

The bq25700A is a buck boost NVDC (narrow voltage DC) charge controller for multi-chemistry portable applications such as notebook, detachable, ultrabook, tablet and other mobile devices with rechargeable batteries. It provides seamless transition between converter operation modes (buck, boost, or buck boost), fast transient response, and high light load efficiency.

The bq25700A supports wide range of power sources, including USB PD ports, legacy USB ports, traditional AC-DC adapters, etc. It takes input voltage from 3.5 V to 24 V, and charges battery of 1-4 series. It also supports USB On-The-Go (OTG) to provide 4.48V to 20.8V output at USB port.

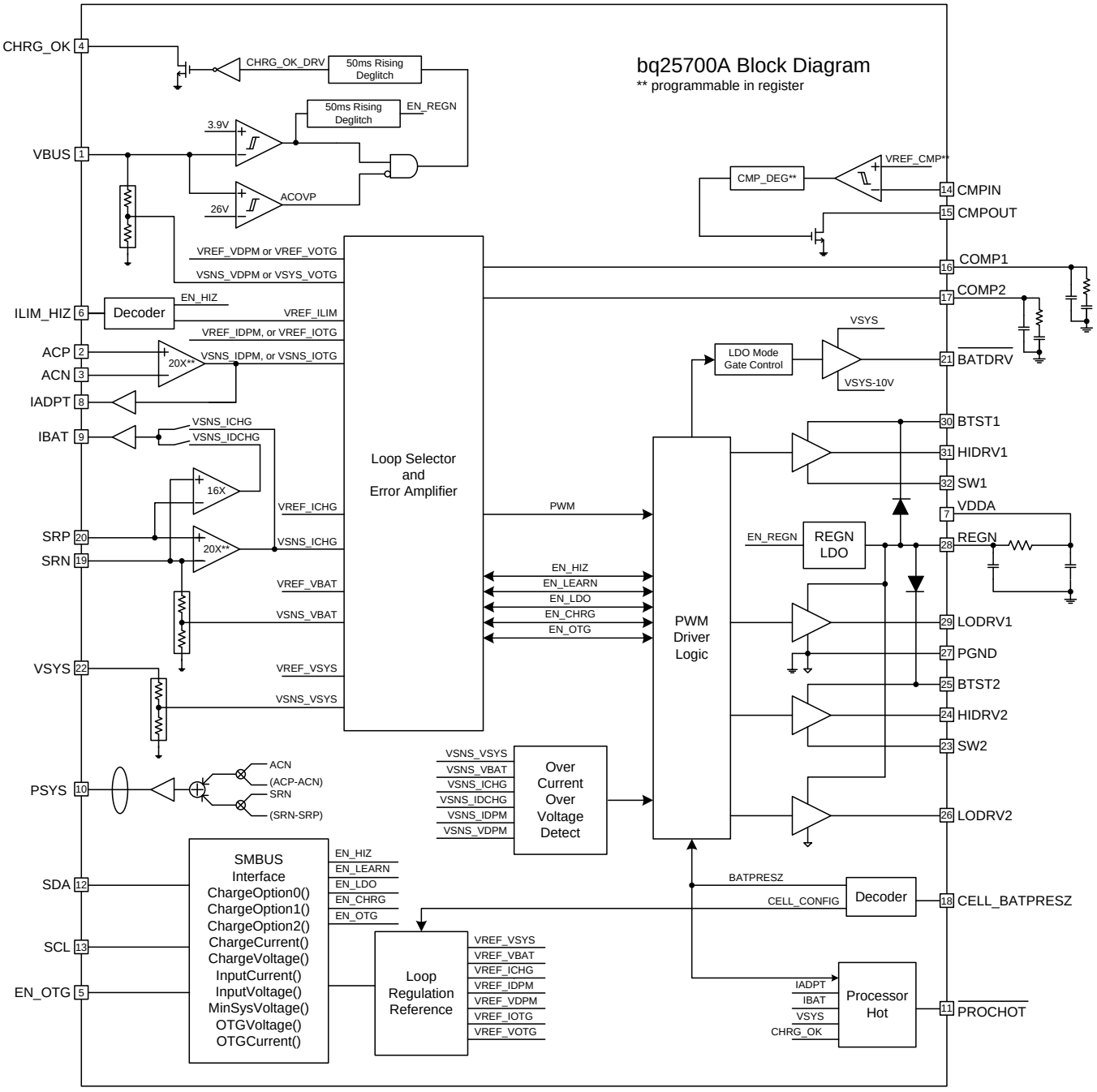
The bq25700A features Dynamic Power Management (DPM) to limit the input power and avoid AC adapter overloading. During battery charging, as the system power increases, the charging current will reduce to maintain total input current below adapter rating. If system power demand temporarily exceeds adapter rating, the bq25700A supports NVDC architecture to allow battery discharge energy to supplement system power. For details, refer to *System Voltage Regulation* section.

In order to be compliant with an Intel IMVP8 compliant system, the bq25700A includes PSYS function to monitor the total platform power from adapter and battery. Besides PSYS, it provides both an independent input current buffer (IADPT) and a battery current buffer (IBAT) with highly accurate current sense amplifiers. If the platform power exceeds the available power from adapter and battery, a PROCHOT signal is asserted to CPU so that the CPU optimizes its performance to the power available to the system.

The SMBus controls input current, charge current and charge voltage registers with high resolution, high accuracy regulation limits. It also sets the PROCHOT timing and threshold profile to meet system requirements.

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8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Power-Up from Battery Without DC Source

If only battery is present and the voltage is above V_{VBAT_UVLOZ}, the BATFET turns on and connects battery to system. By default, the charger is in low power mode (REG0x12[15] = 1) with lowest quiescent current. The LDO stays off. When device moves to performance mode (REG0x12[15] = 0), The host enables IBAT buffer through SMBus to monitor discharge current. For PSYS, PROCHOT or independent comparator, REGN LDO is enabled for an accurate reference.

8.3.2 Power-Up From DC Source

When an input source plugs in, the charger checks the input source voltage to turn on LDO and all the bias circuits. It sets the input current limit before the converter starts.

The power-up sequence from DC source is as follows:

1. 50 ms after VBUS above V_{VBUS_CONVEN}, enable 6 V LDO and CHRG_OK goes HIGH
2. Input voltage and current limit setup
3. Battery CELL configuration
4. 150 ms after VBUS above V_{VBUS_CONVEN}, converter powers up.

8.3.2.1 CHRG_OK Indicator

CHRG_OK is an active HIGH open drain indicator. It indicates the charger is in normal operation when the following conditions are valid:

- VBUS is above V_{VBUS_CONVEN}
- VBUS is below V_{ACOV}
- No MOSFET/inductor, or over-voltage, over-current, thermal shutdown fault

8.3.2.2 Input Voltage and Current Limit Setup

After CHRG_OK goes HIGH, the charger sets default input current limit in REG0x3F() to 3.30 A. The actual input current limit is the lower setting of REG0x3F() and ILIM_HIZ pin.

Charger initiates a VBUS voltage measurement without any load (VBUS at no load). The default VINDPM threshold is VBUS at no load – 1.28 V.

After input current and voltage limits are set, the charger device is ready to power up. The host can always update input current and voltage limit based on input source type.

8.3.2.3 Battery Cell Configuration

CELL_BATPRESZ pin is biased with resistors from REGN to CELL_BATPRESZ to GND. After VDDA LDO is activated, the device detects the battery configuration through CELL_BATPRESZ pin bias voltage. Refer to *Electrical Characteristics* for CELL setting thresholds.

表 1. Battery Cell Configuration

CELL COUNT	PIN VOLTAGE w.r.t. VDDA	BATTERY VOLTAGE (REG0x15)	SYSOVP
4S	75%	16.800V	19.5V
3S	55%	12.592V	19.5V
2S	40%	8.400V	12V
1S	25%	4.192V	5V

8.3.2.4 Device Hi-Z State

The charger enters Hi-Z mode when ILIM_HIZ pin voltage is below 0.4 V or REG0x32[15] is set to 1. During Hi-Z mode, the input source is present, and the charger is in the low quiescent current mode with REGN LDO enabled.

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8.3.3 USB On-The-Go (OTG)

The device supports USB OTG operation to deliver power from the battery to other portable devices through USB port. The OTG mode output voltage is set in REG0x3B(). The OTG mode output current is set in REG0x3C(). The OTG operation can be enabled if the conditions are valid:

- Valid battery voltage is set REG0x15()
- OTG output voltage is set in REG0x3B() and output current is set in REG0x3C()
- EN_OTG pin is HIGH and REG0x32[12] = 1
- VBUS is below V_{VBUS_UVLO}
- 10 ms after the above conditions are valid, converter starts and VBUS ramps up to target voltage. CHRG_OK pin goes HIGH if REG0x12[11] = 1.

8.3.4 Converter Operation

The charger employs a synchronous buck-boost converter that allows charging from a standard 5-V or a high-voltage power source. The charger operates in buck, buck-boost and boost mode. The buck-boost can operate uninterruptedly and continuously across the three operation modes.

表 2. MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
Q1	Switching	Switching	ON
Q2	Switching	Switching	OFF
Q3	OFF	Switching	Switching
Q4	ON	Switching	Switching

8.3.4.1 Inductor Setting through IADPT Pin

The charger reads the inductor value through the IADPT pin.

表 3. Inductor Setting on IADPT Pin

INDUCTOR IN USE	RESISTOR ON IADPT PIN
1 µH	93 kΩ
2.2 µH	137 kΩ
3.3 µH	169 kΩ

8.3.4.2 Continuous Conduction Mode (CCM)

With sufficient charge current, the inductor current does not cross 0 A, which is defined as CCM. The controller starts a new cycle with ramp coming up from 200 mV. As long as error amplifier output voltage is above the ramp voltage, the high-side MOSFET (HSFET) stays on. When the ramp voltage exceeds error amplifier output voltage, HSFET turns off and low-side MOSFET (LSFET) turns on. At the end of the cycle, ramp gets reset and LSFET turns off, ready for the next cycle. There is always break-before-make logic during transition to prevent cross-conduction and shoot-through. During the dead time when both MOSFETs are off, the body-diode of the low-side power MOSFET conducts the inductor current.

During CCM, the inductor current always flows and creates a fixed two-pole system. Having the LSFET turn-on when the HSFET is off keeps the power dissipation low and allows safe charging at high currents.

8.3.4.3 Pulse Frequency Modulation (PFM)

In order to improve converter light-load efficiency, the bq25700A switches to PFM control at light load. The effective switching frequency will decrease accordingly when system load decreases. The minimum frequency can be limit to 25 kHz (ChargeOption0() bit[10]=1).

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8.3.5 Current and Power Monitor

8.3.5.1 High-Accuracy Current Sense Amplifier (IADPT and IBAT)

As an industry standard, a high-accuracy current sense amplifier (CSA) is used to monitor the input current during forward charging, or output current during OTG (IADPT) and the charge/discharge current (IBAT). IADPT voltage is 20× or 40× the differential voltage across ACP and ACN. IBAT voltage is 8x/16× (during charging), or 8×/16× (during discharging) of the differential across SRP and SRN. After input voltage or battery voltage is above UVLO, IADPT output becomes valid. To lower the voltage on current monitoring, a resistor divider from CSA output to GND can be used and accuracy over temperature can still be achieved.

- $V_{(IADPT)}$ = 20 or 40 × ($V_{(ACP)}$ – $V_{(ACN)}$) during forward mode, or 20 or 40 × ($V_{(ACN)}$ – $V_{(ACP)}$) during reverse OTG mode.
- $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRP)}$ – $V_{(SRN)}$) during forward mode.
- $V_{(IBAT)}$ = 8 or 16 × ($V_{(SRN)}$ – $V_{(SRP)}$) during forward supplement mode, or reverse OTG mode.

A maximum 100-pF capacitor is recommended to connect on the output for decoupling high-frequency noise. An additional RC filter is optional, if additional filtering is desired. Note that adding filtering also adds additional response delay. The CSA output voltage is clamped at 3.3 V.

8.3.5.2 High-Accuracy Power Sense Amplifier (PSYS)

The charger monitors total system power. During forward mode, the input adapter powers system. During reverse OTG mode, the battery powers the system and VBUS output. The ratio of PSYS current and total power K_{PSYS} can be programmed in REG0x30[9] with default 1 μA/W. The input and charge sense resistors (RAC and RSR) are programmed in REG0x30[11:10]. PSYS voltage can be calculated with 式 1 where IIN>0 when adapter is in forward charging, and IBAT>0 when the battery is in discharge when the battery is in discharge.

$$V_{PSYS} = R_{PSYS} \times K_{PSYS} (V_{ACP} \times I_{IN} + V_{BAT} \times I_{BAT}) \quad (1)$$

For proper PSYS functionality, RAC and RSR values are limited to 10 mΩ and 20 mΩ.

8.3.6 Input Source Dynamic Power Manage

Refer to *Input Current and Input Voltage Registers for Dynamic Power Management*.

8.3.7 Two-Level Adapter Current Limit (Peak Power Mode)

Usually adapter can supply current higher than DC rating for a few milliseconds to tens of milliseconds. The charger employs two-level input current limit, or peak power mode, to fully utilize the overloading capability and minimize battery discharge during CPU turbo mode. Peak power mode is enabled in REG0x31[13](EN_PKPWR_IDPM) or REG0x31[12(EN_PKPWR_VSYS)]. The DC current limit, or I_{LIM1}, is the same as adapter DC current, set in REG0x3F(). The overloading current, or I_{LIM2}, is set in REG0x33[15:11], as a percentage of $I_{LIM1.}$

When the charger detects input current surge and battery discharge due to load transient, it applies I_{LIM2} for T_{OVLD} in REG0x31[15:14], first, and then I_{LIM1} for up to T_{MAX} – T_{OVLD} time. T_{MAX} is programmed in REG0x31[9:8]. After $T_{MAX,}$ if the load is still high, another peak power cycle starts. Charging is disabled during $T_{MAX,}$; once $T_{MAX,}$ expires, charging continues. If T_{OVLD} is programmed higher than T_{MAX}, then peak power mode is always on.

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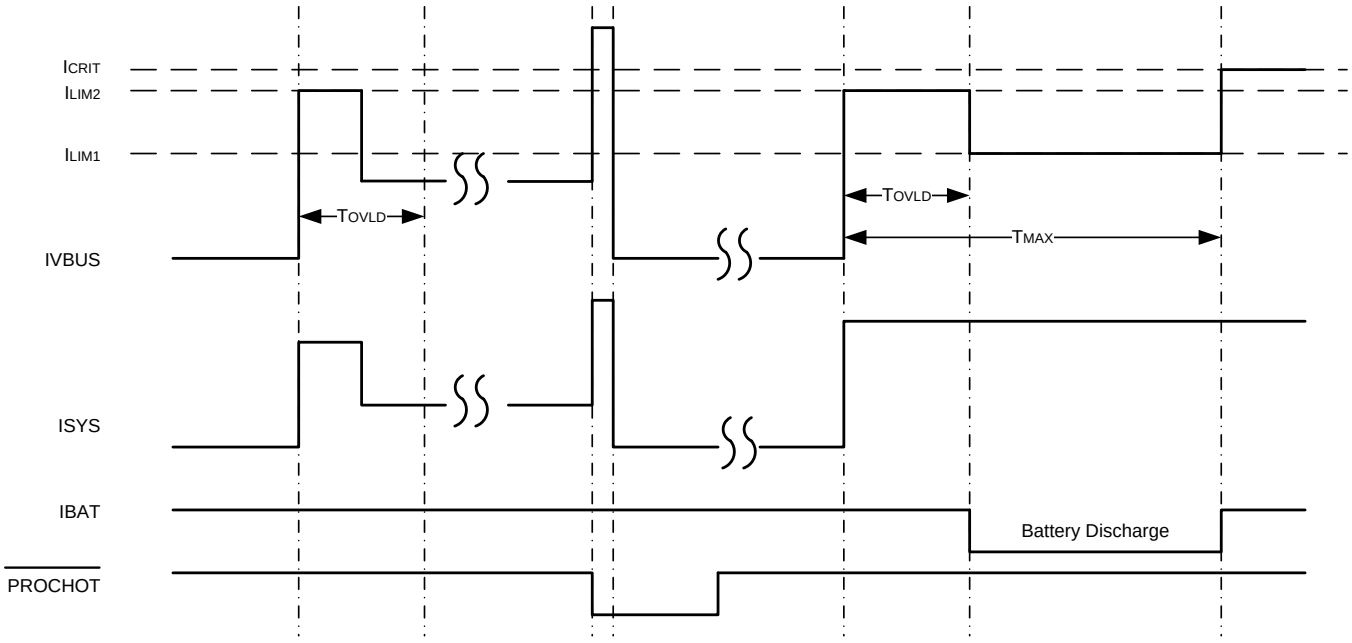


図 12. Two-Level Adapter Current Limit Timing Diagram

8.3.8 Processor Hot Indication

When CPU is running turbo mode, the system peak power may exceed available power from adapter and battery together. The adapter current and battery discharge peak current, or system voltage drop is indication that system power is too high. The charger processor hot function monitors these events, and PROCHOT pulse is asserted. Once CPU receives PROCHOT pulse from charger, it slows down to reduce system power. The processor hot function monitors these events, and PROCHOT pulse is asserted.

The PROCHOT triggering events include:

- ICRIT: adapter peak current, as 110% of I_{LIM2}
- INOM: adapter average current (110% of input current limit)
- IDCHG: battery discharge current
- VSYS: system voltage on VSYS
- Adapter Removal: upon adapter removal (CHRG_OK pin HIGH to LOW)
- Battery Removal: upon battery removal (CELL_BATPRESZ pin goes LOW)
- CMPOUT: Independent comparator output (CMPOUT pin HIGH to LOW)

The threshold of ICRIT, IDCHG or VSYS, and the deglitch time of ICRIT, INOM, IDCHG or CMPOUT are programmable through SMBus. Each triggering event can be individually enabled in REG0x34[6:0]. When any event in PROCHOT profile is triggered, PROCHOT is asserted low for minimum 10 ms programmable in 0x33[4:3]. At the end of the 10 ms, if the PROCHOT event is still active, the pulse gets extended.

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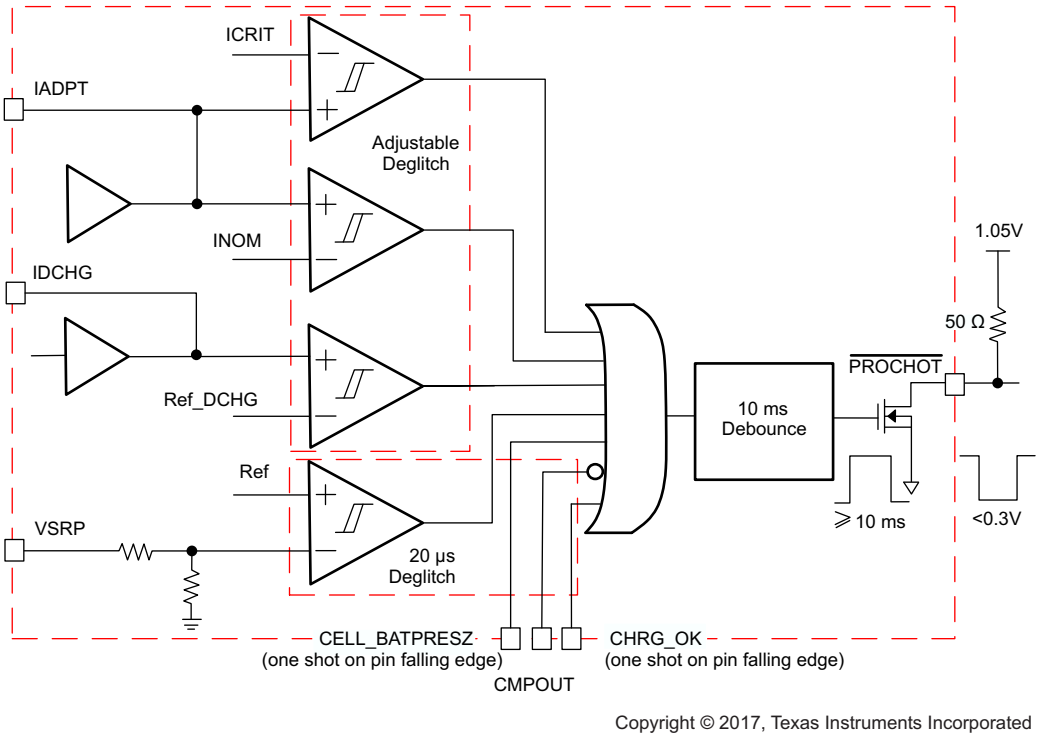


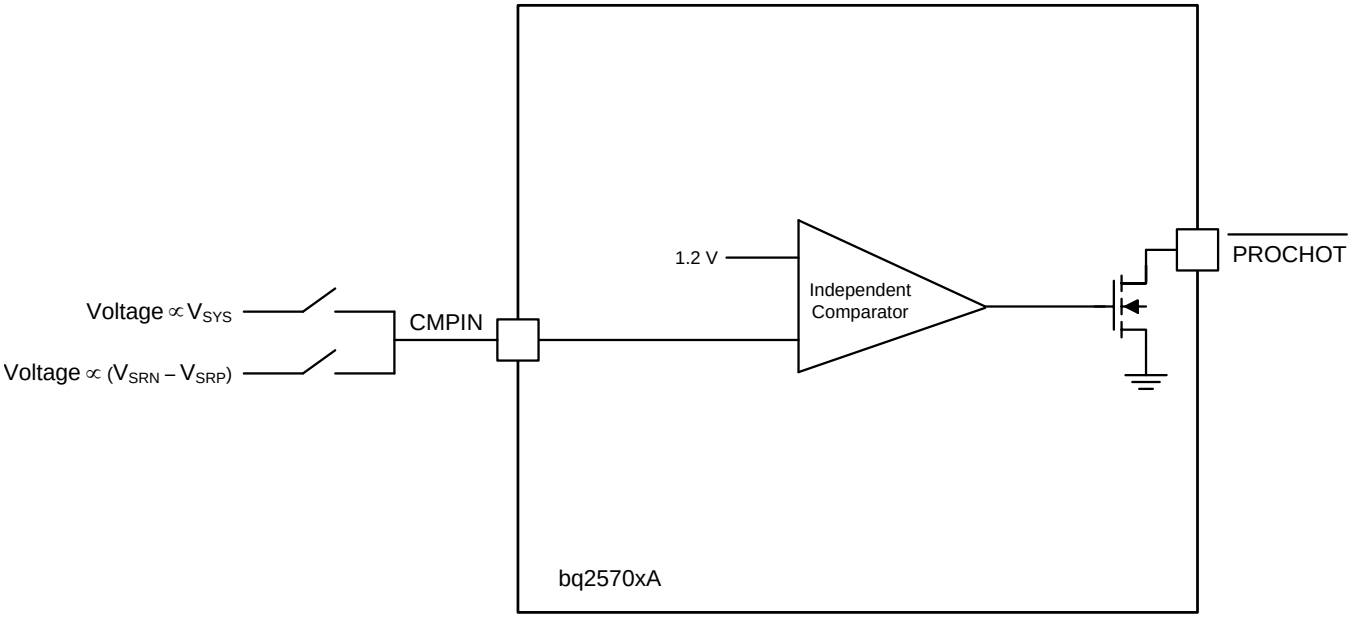
図 13. $\overline{\text{PROCHOT}}$ Profile

8.3.8.1 $\overline{\text{PROCHOT}}$ During Low Power Mode

During low power mode (REG0x12[15] = 1), the charger offers a low quiescent current (~150 µA). Low power $\overline{\text{PROCHOT}}$ function uses the independent comparator to monitor battery discharge current and system voltage, and assert $\overline{\text{PROCHOT}}$ to CPU.

Below lists the register setting to enable $\overline{\text{PROCHOT}}$ during low power mode.

- REG0x12[15] = 1
- REG0x34[5:0] = 000000
- REG0x30[6:4] = 100
- Independent comparator threshold is always 1.2 V
- When REG0x30[14] = 1, charger monitors discharge current. Connect CMPIN to voltage proportional to IBAT pin. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when CMPIN voltage falls below 1.2 V.
- When REG0x30[13] = 1, charger monitors system voltage. Connect CMPIN to voltage proportional to system. $\overline{\text{PROCHOT}}$ triggers from HIGH to LOW when CMPIN voltage rises above 1.2 V.



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図 14. $\overline{\text{PROCHOT}}$ Low Power Mode Implementation

8.3.8.2 $\overline{\text{PROCHOT}}$ Status

REG0x21[6:0] reports which event in the profile triggers $\overline{\text{PROCHOT}}$ by setting the corresponding bit to 1. The status bit can be reset back to 0 after it is read by host, and current $\overline{\text{PROCHOT}}$ event is no longer active.

Assume there are two $\overline{\text{PROCHOT}}$ events, event A and event B. Event A triggers $\overline{\text{PROCHOT}}$ first, but event B is also active. Both status bits will be HIGH. At the end of the 10 ms $\overline{\text{PROCHOT}}$ pulse, if $\overline{\text{PROCHOT}}$ is still active (either by A or B), the $\overline{\text{PROCHOT}}$ pulse is extended.

8.3.9 Device Protection

8.3.9.1 Watchdog Timer

The charger includes watchdog timer to terminate charging if the charger does not receive a write MaxChargeVoltage() or write ChargeCurrent() command within 175 s (adjustable via REG0x12[14:13]). When watchdog timeout occurs, all register values are kept unchanged except ChargeCurrent() resets to zero. Battery charging is suspended. Write MaxChargeVoltage() or write ChargeCurrent() commands must be re-sent to reset watchdog timer and resume charging. Writing REG0x12[14:13] = 00 to disable watchdog timer also resumes charging.

8.3.9.2 Input Overvoltage Protection (ACOV)

The charger has fixed ACOV voltage. When VBUS pin voltage is higher than ACOV, it is considered as adapter over voltage. CHRG_OK will be pulled low, and converter will be disabled. As system falls below battery voltage, BATFET will be turned on. When VBUS pin voltage falls below ACOV, it is considered as adapter voltage returns back to normal voltage. CHRG_OK is pulled high by external pull up resistor. The converter resumes if enable conditions are valid.

8.3.9.3 Input Overcurrent Protection (ACOC)

If the input current exceeds the 1.25× or 2× (REG0x31[2]) of I_{LIM2_VTH} (REG0x33[15:11]) set point, converter stops switching. After 300 ms, converter starts switching again.

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8.3.9.4 System Overvoltage Protection (SYSOVP)

When the converter starts up, the bq25700A reads CELL pin configuration and sets MaxChargeVoltage() and SYSOVP threshold (1s – 5 V, 2s – 12 V, 3s/4s – 19.5 V). Before REGx15() is written by the host, the battery configuration will change with CELL pin voltage. When SYSOVP happens, the device latches off the converter. REG20[4] is set as 1. The user can clear latch-off by either writing 0 to the SYSOVP bit or removing and plugging in the adapter again. After latch-off is cleared, the converter starts again.

8.3.9.5 Battery Overvoltage Protection (BATOVP)

Battery over-voltage may happen when battery is removed during charging or the user plugs in a wrong battery. The BATOVP threshold is 104% (1 s) or 102% (2 s to 4 s) of regulation voltage set in REG0x15().

8.3.9.6 Battery Short

If BAT voltage falls below SYSMIN during charging, the maximum current is limited to 384 mA.

8.3.9.7 Thermal Shutdown (TSHUT)

The WQFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As added level of protection, the charger converter turns off for self-protection whenever the junction temperature exceeds the 155°C. The charger stays off until the junction temperature falls below 135°C. During thermal shut down, the LDO current limit is reduced to 16 mA and REGN LDO stays off. When the temperature falls below 135°C, charge can be resumed with soft start.

8.4 Device Functional Modes

8.4.1 Forward Mode

When input source is connected to VBUS, bq25700A is in forward mode to regulate system and charge battery.

8.4.1.1 System Voltage Regulation with Narrow VDC Architecture

The bq25700A employs Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by MinSystemVoltage(). Even with a deeply depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode).

As the battery voltage rises above the minimum system voltage, BATFET is fully on when charging or in supplement mode and the voltage difference between the system and battery is the VDS of BATFET. System voltage is regulated 160 mV above battery voltage when BATFET is off (no charging or no supplement current).

See *System Voltage Regulation* for details on system voltage regulation and register programming.

8.4.1.2 Battery Charging

The bq25700A charges 1-4 cell battery in constant current (CC), and constant voltage (CV) mode. Based on CELL_BATPREZ pin setting, the charger sets default battery voltage 4.2V/cell to ChargeVoltage(), or REG0x15(). According to battery capacity, the host programs appropriate charge current to ChargeCurrent(), or REG0x14(). When battery is full or battery is not in good condition to charge, host terminates charge by setting REG0x12[0] to 1, or setting ChargeCurrent() to zero.

See *Feature Description* for details on register programming.

8.4.2 USB On-The-Go

The bq25700A supports USB OTG functionality to deliver power from the battery to other portable devices through USB port (reverse mode). The OTG output voltage is compliant with USB PD specification, including 5 V, 9 V, 15 V, and 20 V (REG0x3B()). The output current regulation is compliant with USB type C specification, including 500 mA, 1.5 A, 3 A and 5 A (REG0x3C()).

Similar to forward operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

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8.5 Programming

The charger supports battery-charger commands that use either Write-Word or Read-Word protocols, as summarized in 表 6. The SMBUS address is 12h (0001001_X), where X is the read/write bit. The ManufacturerID and DeviceID registers are assigned identify the charger device. The ManufacturerID register command always returns 40h.

8.5.1 SMBus Interface

The bq25700A device operates as a slave, receiving control inputs from the embedded controller host through the SMBus interface. The bq25700A device uses a simplified subset of the commands documented in *System Management Bus Specification V1.1*, which can be downloaded from www.smbus.org. The bq25700A device uses the SMBus read-word and write-word protocols (shown in 表 4 and 表 5) to communicate with the smart battery. The device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus. In addition, the device has two identification registers, a 16-bit device ID register (0xFFH) and a 16-bit manufacturer ID register (0xFEH).

SMBus communication starts when VCC is above $V_{(UVLO)}$.

The data (SDA) and clock (SCL) pins have Schmitt-trigger inputs that can accommodate slow edges. Choose pullup resistors (10 kΩ) for SDA and SCL to achieve rise times according to the SMBus specifications. Communication starts when the master signals a start condition, which is a high-to-low transition on SDA, while SCL is high. When the master has finished communicating, the master issues a stop condition, which is a low-to-high transition on SDA, while SCL is high. The bus is then free for another transmission. 図 15 and 図 16 show the timing diagram for signals on the SMBus interface. The address byte, command byte, and data bytes are transmitted between the start and stop conditions. The SDA state changes only while SCL is low, except for the start and stop conditions. Data is transmitted in 8-bit bytes and is sampled on the rising edge of SCL. Nine clock cycles are required to transfer each byte in or out of the device because either the master or the slave acknowledges the receipt of the correct byte during the ninth clock cycle. The bq25700A supports the charger commands listed in 表 4.

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Programming (continued)

8.5.1.1 SMBus Write-Word and Read-Word Protocols

表 4. Write-Word Format

S (1)(2)	SLAVE ADDRESS (1)	W (1)(3)	ACK (4)(5)	COMMAND BYTE (1)	ACK (4)(5)	LOW DATA BYTE (1)	ACK (4)(5)	HIGH DATA BYTE (1)	ACK (4)(5)	P (1)(6)
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	

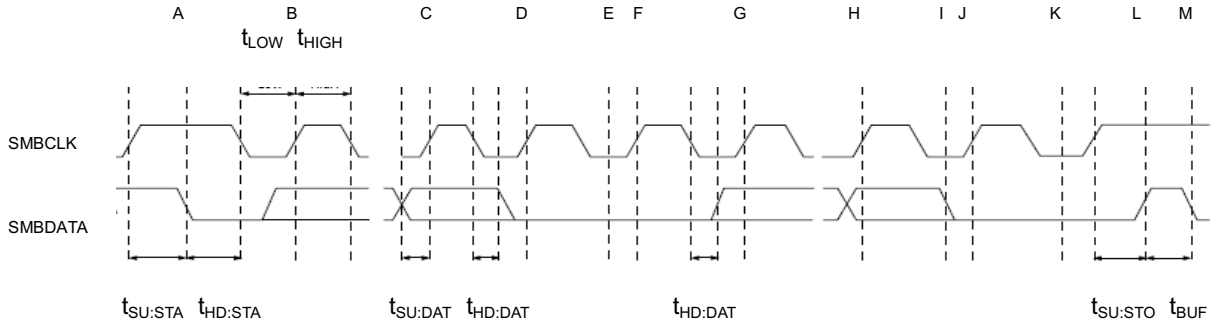
(1) Master to slave
(2) S = Start condition or repeated start condition
(3) W = Write bit (logic-low)
(4) Slave to master (shaded gray)
(5) ACK = Acknowledge (logic-low)
(6) P = Stop condition

表 5. Read-Word Format

S (1) (2)	SLAVE ADDRESS (1)	W (1)(3)	ACK (4)(5)	COMMAND BYTE (1)	ACK (4)(5)	S (1) (2)	SLAVE ADDRESS (1)	R (1) (6)	ACK (4)(5)	LOW DATA BYTE (4)	ACK (1)(5)	HIGH DATA BYTE (4)	NACK (1)(7)	P (1)(8)
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	

(1) Master to slave
(2) S = Start condition or repeated start condition
(3) W = Write bit (logic-low)
(4) Slave to master (shaded gray)
(5) ACK = Acknowledge (logic-low)
(6) R = Read bit (logic-high)
(7) NACK = Not acknowledge (logic-high)
(8) P = Stop condition

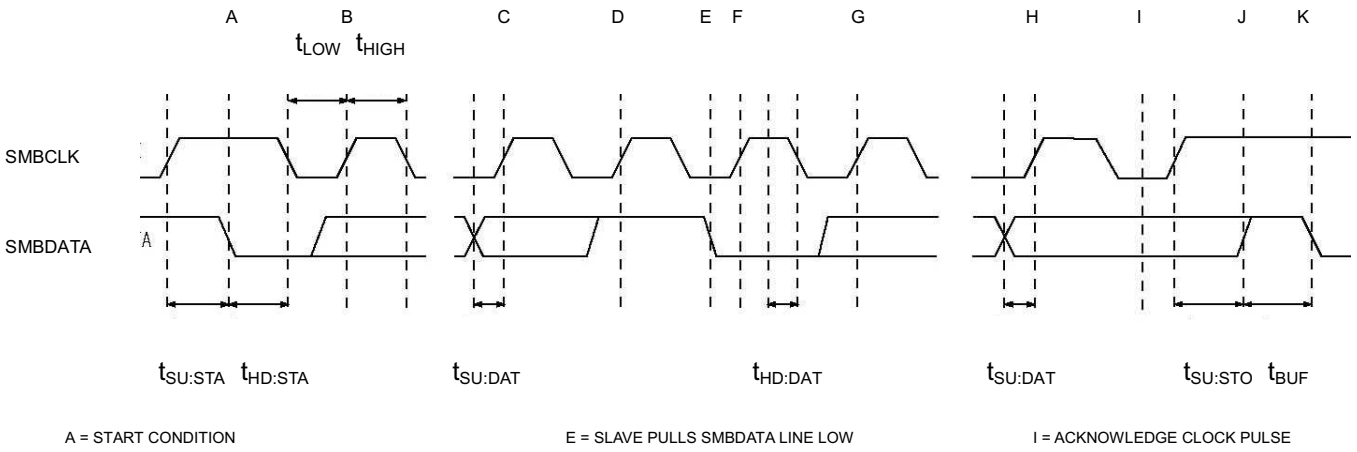
8.5.1.2 Timing Diagrams



A = Start condition
B = MSB of address clocked into slave
C = LSB of address clocked into slave
D = R/W bit clocked into slave
E = Slave pulls SMBDATA line low
F = ACKNOWLEDGE bit clocked into master
G = MSB of data clocked into slave
H = LSB of data clocked into slave
I = Slave pulls SMBDATA line low
J = Acknowledge clocked into master
K = Acknowledge clock pulse
L = Stop condition, data executed by slave
M = New start condition

図 15. SMBus Write Timing

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A = Start condition
B = MSB of address clocked into slave
C = LSB of address clocked into slave
D = R/W bit clocked into slave
E = Slave pulls SMBDATA line low
F = ACKNOWLEDGE bit clocked into master
G = MSB of data clocked into master
H = LSB of data clocked into master
I = Acknowledge clock pulse
J = Stop condition
K = New start condition

図 16. SMBus Read Timing

8.6 Register Map

表 6. Charger Command Summary

SMBus ADDR	REGISTER NAME	TYPE	DESCRIPTION	LINKS
12h	ChargeOption0()	R/W	Charge Option 0	Go
14h	ChargeCurrent()	R/W	7-bit charge current setting LSB 64 mA, Range 8128 mA	Go
15h	MaxChargeVoltage()	R/W	11-bit charge voltage setting LSB 16 mV, Default: 1S-4192mV, 2S-8400mV, 3S-12592mV, 4S-16800mV	Go
30h	ChargeOption1()	R/W	Charge Option 1	Go
31h	ChargeOption2()	R/W	Charge Option 2	Go
32h	ChargeOption3()	R/W	Charge Option 3	Go
33h	ProchotOption0()	R/W	$\overline{\text{PROCHOT}}$ Option 0	Go
34h	ProchotOption1()	R/W	$\overline{\text{PROCHOT}}$ Option 1	Go
35h	ADCOption()	R/W	ADC Option	Go
20h	ChargerStatus()	R	Charger Status	Go
21h	ProchotStatus()	R	Prochot Status	Go
22h	IIN_DPM()	R	7-bit input current limit in use LSB: 50 mA, Range: 50 mA - 6400 mA	Go
23h	ADCVBUS/PSYS()	R	8-bit digital output of input voltage, 8-bit digital output of system power PSYS: Full range: 3.06 V, LSB: 12 mV VBUS: Full range: 3.2 V - 19.52 V, LSB 64 mV	Go
24h	ADCIBAT()	R	8-bit digital output of battery charge current, 8-bit digital output of battery discharge current ICHG: Full range 8.128 A, LSB 64 mA IDCHG: Full range: 32.512 A, LSB: 256 mA	Go

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Register Map (continued)

表 6. Charger Command Summary (continued)

SMBus ADDR	REGISTER NAME	TYPE	DESCRIPTION	LINKS
25h	ADCIINCMPIN()	R	8-bit digital output of input current, 8-bit digital output of CMPIN voltage POR State - IIN: Full range: 12.75 A, LSB 50 mA CMPIN: Full range 3.06 V, LSB: 12 mV	Go
26h	ADCVSYSVBAT()	R	8-bit digital output of system voltage, 8-bit digital output of battery voltage VSYS: Full range: 2.88 V - 19.2 V, LSB: 64 mV VBAT: Full range : 2.88 V - 19.2 V, LSB 64 mV	Go
3Bh	OTGVoltage()	R/W	8-bit OTG voltage setting LSB 64 mV, Range: 4480 – 20800 mV	Go
3Ch	OTGCurrent()	R/W	7-bit OTG output current setting LSB 50 mA, Range: 0 A – 6350 mA	Go
3Dh	InputVoltage()	R/W	8-bit input voltage setting LSB 64 mV, Range: 3200 mV – 19520 mV	Go
3Eh	MinSystemVoltage()	R/W	6-Bit minimum system voltage setting LSB: 256 mV, Range: 1024 mV - 16182 mV Default: 1S-3.584V, 2S-6.144V, 3S-9.216V, 4S-12.288V	Go
3Fh	IIN_HOST()	R/W	6-bit Input current limit set by host LSB: 50 mA, Range: 50 mA - 6400 mA	Go
FEh	ManufacturerID()	R	Manufacturer ID - 0x0040H	Go
FFh	DeviceID()	R	Device ID	Go

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8.6.1 Setting Charge and PROCHOT Options

8.6.1.1 ChargeOption0 Register (SMBus address = 12h) [reset = E20Eh]

図 17. ChargeOption0 Register (SMBus address = 12h) [reset = E20Eh]

15	14	13	12	11	10	9	8
EN_LWPWR	WDTMR_ADJ		IDPM_AUTO_ DISABLE	OTG_ON_ CHRGOK	EN_OOA	PWM_FREQ	Reserved
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved		EN_LEARN	IADPT_GAIN	IBAT_GAIN	EN_LDO	EN_IDPM	CHRG_INHIBIT
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7. ChargeOption0 Register (SMBus address = 12h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	EN_LWPWR	R/W	1b	Low Power Mode Enable 0b: Disable Low Power Mode. Device in performance mode with battery only. The PROCHOT, current/power monitor buffer and comparator follow register setting. 1b: Enable Low Power Mode. Device in low power mode with battery only for lowest quiescent current. PROCHOT, discharge current monitor buffer, power monitor buffer and independent comparator are disabled. ADC is not available in Low Power Mode. Independent comparator can be enabled by setting either REG0X30()[14] or [13] to 1. <default at POR>
14-13	WDTMR_ADJ	R/W	11b	WATCHDOG Timer Adjust Set maximum delay between consecutive SMBus write of charge voltage or charge current command. If device does not receive a write on the REG0x15() or the REG0x14() within the watchdog time period, the charger will be suspended by setting the REG0x14() to 0 mA. After expiration, the timer will resume upon the write of REG0x14(), REG0x15() or REG0x12[14:13]. The charger will resume if the values are valid. 00b: Disable Watchdog Timer 01b: Enabled, 5 sec 10b: Enabled, 88 sec 11b: Enable Watchdog Timer, 175 sec <default at POR>
12	IDPM_AUTO_ DISABLE	R/W	0b	IDPM Auto Disable When CELL_BATPRESZ pin is LOW, the charger automatically disables the IDPM function by setting EN_IDPM (REG0x12[1]) to 0. The host can enable IDPM function later by writing EN_IDPM bit (REG0x12[1]) to 1. 0b: Disable this function. IDPM is not disabled when CELL_BATPRESZ goes LOW. <default at POR> 1b: Enable this function. IDPM is disabled when CELL_BATPRESZ goes LOW.
11	OTG_ON_ CHRGOK	R/W	0b	Add OTG to CHRG_OK Drive CHRG_OK to HIGH when the device is in OTG mode. 0b: Disable <default at POR> 1b: Enable
10	EN_OOA	R/W	0b	Out-of-Audio Enable 0b: No limit of PFM burst frequency <default at POR> 1b: Set minimum PFM burst frequency to above 25 kHz to avoid audio noise

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表 7. ChargeOption0 Register (SMBus address = 12h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
9	PWM_FREQ	R/W	1b	Switching Frequency Two converter switching frequencies. One for small inductor and the other for big inductor. Recommend 800 kHz with 2.2 µH or 3.3 µH, and 1.2 MHz with 1 µH or 1.5 µH. 0b: 1200 kHz 1b: 800 kHz <default at POR>
8	Reserved	R/W	0b	Reserved

表 8. ChargeOption0 Register (SMBus address = 12h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	Reserved	R/W	00b	Reserved
5	EN_LEARN	R/W	0b	LEARN function allows the battery to discharge while the adapter is present. It calibrates the battery gas gauge over a complete discharge/charge cycle. When the battery voltage is below battery depletion threshold, the system switches back to adapter input by the host. When CELL_BATPRESZ pin is LOW, the device exits LEARN mode and this bit is set back to 0. 0b: Disable LEARN Mode <default at POR> 1b: Enable LEARN Mode
4	IADPT_GAIN	R/W	0b	IADPT Amplifier Ratio The ratio of voltage on IADPT and voltage across ACP and ACN. 0b: 20× <default at POR> 1b: 40×
3	IBAT_GAIN	R/W	1b	IBAT Amplifier Ratio The ratio of voltage on IBAT and voltage across SRP and SRN 0b: 8× 1b: 16× <default at POR>
2	EN_LDO	R/W	1b	LDO Mode Enable When battery voltage is below minimum system voltage (REG0x3E()), the charger is in pre-charge with LDO mode enabled. 0b: Disable LDO mode, BATFET fully ON. Precharge current is set by battery pack internal resistor. The system is regulated by the MaxChargeVoltage register. 1b: Enable LDO mode, Precharge current is set by the ChargeCurrent register and clamped below 384 mA (2 cell – 4 cell) or 2A (1 cell). The system is regulated by the MinSystemVoltage register. <default at POR>
1	EN_IDPM	R/W	1b	IDPM Enable Host writes this bit to enable IDPM regulation loop. When the IDPM is disabled by the charger (refer to IDPM_AUTO_DISABLE), this bit goes LOW. 0b: IDPM disabled 1b: IDPM enabled <default at POR>
0	CHRG_INHIBIT	R/W	0b	Charge Inhibit When this bit is 0, battery charging will start with valid values in the MaxChargeVoltage register and the ChargeCurrent register. 0b: Enable Charge <default at POR> 1b: Inhibit Charge

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8.6.1.2 ChargeOption1 Register (SMBus address = 30h) [reset = 211h]

図 18. ChargeOption1 Register (SMBus address = 30h) [reset = 211h]

15	14	13	12	11	10	9	8
EN_IBAT	EN_PROCHOT_LPWR		EN_PSYS	RSNS_RAC	RSNS_RSR	PSYS_RATIO	Reserved
R/W	R/W		R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
CMP_REF	CMP_POL	CMP_DEG		FORCE_ LATCHOFF	Reserved	EN_SHIP_ DCHG	AUTO_ WAKEUP_EN
R/W	R/W	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. ChargeOption1 Register (SMBus address = 30h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	EN_IBAT	R/W	0b	IBAT Enable Enable the IBAT output buffer. In low power mode (REG0x12[15] = 1), IBAT buffer is always disabled regardless of this bit value. 0b Turn off IBAT buffer to minimize Iq <default at POR> 1b: Turn on IBAT buffer
14-13	EN_PROCHOT _LPWR	R/W	00b	Enable $\overline{\text{PROCHOT}}$ during battery only low power mode With battery only, enable IDCHG or VSYS in $\overline{\text{PROCHOT}}$ with low power consumption. Do not enable this function with adapter present. Refer to *$\overline{\text{PROCHOT}}$ During Low Power Mode* for more details. 00b: Disable low power $\overline{\text{PROCHOT}}$ <default at POR> 01b: Enable IDCHG low power $\overline{\text{PROCHOT}}$ 10b: Enable VSYS low power $\overline{\text{PROCHOT}}$ 11b: Reserved
12	EN_PSYS	R/W	0b	PSYS Enable Enable PSYS sensing circuit and output buffer (whole PSYS circuit). In low power mode (REG0x12[15] = 1), PSYS sensing and buffer are always disabled regardless of this bit value. 0b: Turn off PSYS buffer to minimize Iq <default at POR> 1b: Turn on PSYS buffer
11	RSNS_RAC	R/W	0b	Input sense resistor RAC 0b: 10 mΩ <default at POR> 1b: 20 mΩ
10	RSNS_RSR	R/W	0b	Charge sense resistor RSR 0b: 10 mΩ <default at POR> 1b: 20 mΩ
9	PSYS_RATIO	R/W	1b	PSYS Gain Ratio of PSYS output current vs total input and battery power with 10-mΩ sense resistor. 0b: 0.25 µA/W 1b: 1 µA/W <default at POR>
8	Reserved	R/W	0b	Reserved

表 10. ChargeOption1 Register (SMBus address = 30h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CMP_REF	R/W	0b	Independent Comparator internal Reference 0b: 2.3 V <default at POR> 1b: 1.2 V

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表 10. ChargeOption1 Register (SMBus address = 30h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
6	CMP_POL	R/W	0b	Independent Comparator output Polarity 0b: When CMPIN is above internal threshold, CMPOUT is LOW (internal hysteresis) <default at POR> 1b: When CMPIN is below internal threshold, CMPOUT is LOW (external hysteresis)
5-4	CMP_DEG	R/W	01b	Independent comparator deglitch time, only applied to the falling edge of CMPOUT (HIGH → LOW). 00b: Independent comparator is disabled 01b: Independent comparator is enabled with output deglitch time 1 µs <default at POR> 10b: Independent comparator is enabled with output deglitch time of 2 ms 11b: Independent comparator is enabled with output deglitch time of 5 sec
3	FORCE_LATCHOFF	R/W	0b	Force Power Path Off When independent comparator triggers, charger turns off Q1 and Q4 (same as disable converter) so that the system is disconnected from the input source. At the same time, CHRG_OK signal goes to LOW to notify the system. 0b: Disable this function <default at POR> 1b: Enable this function
2	Reserved	R/W	0b	Reserved
1	EN_SHIP_DCHG	R/W	0b	Discharge SRN for Shipping Mode When this bit is 1, discharge SRN pin down below 3.8 V in 140 ms. When 140 ms is over, this bit is reset to 0. 0b: Disable shipping mode <default at POR> 1b: Enable shipping mode
0	AUTO_WAKEUP_EN	R/W	1b	Auto Wakeup Enable When this bit is HIGH, if the battery is below minimum system voltage (REG0x3E()), the device will automatically enable 128 mA charging current for 30 mins. When the battery is charged up above minimum system voltage, charge will terminate and the bit is reset to LOW. 0b: Disable 1b: Enable <default at POR>

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8.6.1.3 ChargeOption2 Register (SMBus address = 31h) [reset = 2B7]

図 19. ChargeOption2 Register (SMBus address = 31h) [reset = 2B7]

15	14	13	12	11	10	9	8
PKPWR_TOVLD_DEG		EN_PKPWR_IDPM	EN_PKPWR_VSYS	PKPWR_OVLD_STAT	PKPWR_RELAX_STAT	PKPWR_TMAX[1:0]	
R/W		R/W	R/W	R/W	R/W	R/W	
7	6	5	4	3	2	1	0
EN_EXTILIM	EN_ICHG_IDCHG	Q2_OCP	ACX_OCP	EN_ACOC	ACOC_VTH	EN_BATOC	BATOC_VTH
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. ChargeOption2 Register (SMBus address = 31h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	PKPWR_TOVLD_DEG	R/W	00b	Input Overload time in Peak Power Mode 00b: 1 ms <default at POR> 01b: 2 ms 10b: 10 ms 11b: 20 ms
13	EN_PKPWR_IDPM	R/W	0b	Enable Peak Power Mode triggered by input current overshoot If REG0x31[13:12] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by input current overshoot <default at POR> 1b: Enable peak power mode triggered by input current overshoot.
12	EN_PKPWR_VSYS	R/W	0b	Enable Peak Power Mode triggered by system voltage under-shoot If REG0x31[13:12] are 00b, peak power mode is disabled. Upon adapter removal, the bits are reset to 00b. 0b: Disable peak power mode triggered by system voltage under-shoot <default at POR> 1b: Enable peak power mode triggered by system voltage under-shoot.
11	PKPWR_OVLD_STAT	R/W	0b	Indicator that the device is in overloading cycle. Write 0 to get out of overloading cycle. 0b: Not in peak power mode. <default at POR> 1b: In peak power mode.
10	PKPWR_RELAX_STAT	R/W	0b	Indicator that the device is in relaxation cycle. Write 0 to get out of relaxation cycle. 0b: Not in relaxation cycle. <default at POR> 1b: In relaxation mode.
9-8	PKPWR_TMAX[1:0]	R/W	10b	Peak power mode overload and relax cycle time. When REG0x31[15:14] is programmed longer than REG0x31[9:8], there is no relax time. 00b: 5 ms 01b: 10 ms 10b: 20 ms <default at POR> 11b: 40 ms

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表 12. ChargeOption2 Register (SMBus address = 31h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_EXTILIM	R/W	1b	Enable ILIM_HIZ pin to set input current limit 0b: Input current limit is set by REG0x3F. 1b: Input current limit is set by the lower value of ILIM_HIZ pin and REG0x3F. <default at POR>
6	EN_ICHG _IDCHG	R/W	0b	0b: IBAT pin as discharge current. <default at POR> 1b: IBAT pin as charge current.
5	Q2_OCP	R/W	1b	Q2 OCP threshold by sensing Q2 VDS 0b: 210 mV 1b: 150 mV <default at POR>
4	ACX_OCP	R/W	1b	Input current OCP threshold by sensing ACP-ACN. 0b: 280 mV 1b: 150 mV <default at POR>
3	EN_ACOC	R/W	0b	ACOC Enable Input overcurrent (ACOC) protection by sensing the voltage across ACP and ACN. Upon ACOC (after 100-µs blank-out time), converter is disabled. 0b: Disable ACOC <default at POR> 1b: ACOC threshold 125% or 200% ICRIT
2	ACOC_VTH	R/W	1b	ACOC Limit Set MOSFET OCP threshold as percentage of IDPM with current sensed from $R_{AC.}$ 0b: 125% of ICRIT 1b: 200% of ICRIT <default at POR>
1	EN_BATOC	R/W	1b	BATOC Enable Battery discharge overcurrent (BATOC) protection by sensing the voltage across SRN and SRP. Upon BATOC, converter is disabled. 0b: Disable BATOC 1b: BATOC threshold 125% or 200% $\overline{\text{PROCHOT}}$ IDCHG <default at POR>
0	BATOC_VTH	R/W	1b	Set battery discharge overcurrent threshold as percentage of $\overline{\text{PROCHOT}}$ battery discharge current limit. 0b: 125% of $\overline{\text{PROCHOT}}$ IDCHG 1b: 200% of $\overline{\text{PROCHOT}}$ IDCHG <default at POR>

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8.6.1.4 ChargeOption3 Register (SMBus address = 32h) [reset = 0h]

図 20. ChargeOption3 Register (SMBus address = 32h) [reset = 0h]

15	14	13	12	11	10	9	8
EN_HIZ	RESET_REG	RESET_ VINDPM	EN_OTG	EN_ICO_MOD E	Reserved		
R/W	R/W	R/W	R/W	R/W	R/W		
7	6	5	4	3	2	1	0
Reserved						BATFETOFF_ HIZ	PSYS_OTG_ IDCHG
R/W						R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. ChargeOption3 Register (SMBus address = 32h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	EN_HIZ	R/W	0b	Device Hi-Z Mode Enable When the charger is in Hi-Z mode, the device draws minimal quiescent current. With VBUS above UVLO. REGN LDO stays on, and system powers from battery. 0b: Device not in Hi-Z mode <default at POR> 1b: Device in Hi-Z mode
14	RESET_REG	R/W	0b	Reset Registers All the registers go back to the default setting except the VINDPM register. 0b: Idle <default at POR> 1b: Reset all the registers to default values. After reset, this bit goes back to 0.
13	RESET_VINDPM	R/W	0b	Reset VINDPM Threshold 0b: Idle 1b: Converter is disabled to measure VINDPM threshold. After VINDPM measurement is done, this bit goes back to 0 and converter starts.
12	EN_OTG	R/W	0b	OTG Mode Enable Enable device in OTG mode when EN_OTG pin is HIGH. 0b: Disable OTG <default at POR> 1b: Enable OTG mode to supply VBUS from battery.
11	EN_ICO_MODE	R/W	0b	Enable ICO Algorithm 0b: Disable ICO algorithm. <default at POR> 1b: Enable ICO algorithm.
10-8	Reserved	R/W	000b	Reserved

表 14. ChargeOption3 Register (SMBus address = 32h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-2	Reserved	R/W	000000b	Reserved
1	BATFETOFF_ HIZ	R/W	0b	Control BATFET during HIZ mode. 0b: BATFET on during Hi-Z <default at POR> 1b: BATFET off during Hi-Z
0	PSYS_OTG_ IDCHG	R/W	0b	PSYS function during OTG mode. 0b: PSYS as battery discharge power minus OTG output power <default at POR> 1b: PSYS as battery discharge power only

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8.6.1.5 ProchotOption0 Register (SMBus address = 33h) [reset = 04A54h]

図 21. ProchotOption0 Register (SMBus address = 33h) [reset = 04A54h]

15-11			10-9		8
ILIM2_VTH			ICRIT_DEG		Reserved
R/W			R/W		R/W
7-6	5	4-3	2	1	0
VSYS_VTH	EN_PROCHOT_EXT	PROCHOT_WIDTH	PROCHOT_CLEAR	INOM_DEG	Reserved
R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. ProchotOption0 Register (SMBus address = 33h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-11	ILIM2_VTH	R/W	01001b	I_{LIM2} Threshold 5 bits, percentage of IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold: 00001b - 11001b: 110% - 230%, step 5% 11010b - 11110b: 250% - 450%, step 50% 11111b: Out of Range (Ignored) Default 150%, or 01001
10-9	ICRIT_DEG	R/W	01b	ICRIT Deglitch time ICRIT threshold is set to be 110% of $_{ILIM2}$. Typical ICRIT deglitch time to trigger $\overline{\text{PROCHOT}}$. 00b: 15 µs 01b: 100 µs <default at POR> 10b: 400 µs (max 500 us) 11b: 800 µs (max 1 ms)
8	Reserved	R/W	0b	Reserved

表 16. ProchotOption0 Register (SMBus address = 33h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	VSYS_VTH	R/W	01b	VSYS Threshold Measure on VSYS with fixed 20-µs deglitch time. Trigger when SYS pin voltage is below the threshold. 00b: 5.75 V (2-4 s) or 2.85 V (1 s) 01b: 6 V (2-4 s) or 3.1 V (1 s) <default at POR> 10b: 6.25 V (2-4 s) or 3.35 V (1 s) 11b: 6.5 V (2-4 s) or 3.6 V (1 s)
5	EN_PROCHOT_EXT	R/W	0b	$\overline{\text{PROCHOT}}$ Pulse Extension Enable When pulse extension is enabled, keep the $\overline{\text{PROCHOT}}$ pin voltage LOW until host writes 0x33[2] = 0. 0b: Disable pulse extension <default at POR> 1b: Enable pulse extension
4-3	PROCHOT_WIDTH	R/W	10b	$\overline{\text{PROCHOT}}$ Pulse Width Minimum $\overline{\text{PROCHOT}}$ pulse width when REG0x33[5] = 0 00b: 100 µs 01b: 1 ms 10b: 10 ms <default at POR> 11b: 5 ms

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表 16. ProchotOption0 Register (SMBus address = 33h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
2	PROCHOT _CLEAR	R/W	1b	$\overline{\text{PROCHOT}}$ Pulse Clear Clear $\overline{\text{PROCHOT}}$ pulse when 0x33[5] = 1. 0b: Clear $\overline{\text{PROCHOT}}$ pulse and drive $\overline{\text{PROCHOT}}$ pin HIGH. 1b: Idle <default at POR>
1	INOM_DEG	R/W	0b	INOM Deglitch Time INOM is always 10% above IDPM in 0x3FH. Measure current between ACP and ACN. Trigger when the current is above this threshold. 0b: 1 ms (must be max) <default at POR> 1b: 50 ms (max 60 ms)
0	Reserved	R/W	0b	Reserved

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8.6.1.6 ProchotOption1 Register (SMBus address = 34h) [reset = 8120h]

図 22. ProchotOption1 Register (SMBus address = 34h) [reset = 8120h]

15-10							9-8
IDCHG_VTH							IDCHG_DEG
R/W							R/W
7	6	5	4	3	2	1	0
Reserved	PROCHOT_PROFILE_IC	PP_ICRIT	PP_INOM	PP_IDCHG	PP_VSYS	PP_BATPRES	PP_ACOK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. ProchotOption1 Register (SMBus address = 34h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-10	IDCHG_VTH	R/W	100000b	IDCHG Threshold 6 bit, range, range 0 A to 32256 mA, step 512 mA. There is a 128 mA offset Measure current between SRN and SRP. Trigger when the discharge current is above the threshold. If the value is programmed to 000000b $\overline{\text{PROCHOT}}$ is always triggered. Default: 16384 mA or 100000b
9-8	IDCHG_DEG	R/W	01b	IDCHG Deglitch Time 00b: 1.6 ms 01b: 100 µs <default at POR> 10b: 6 ms 11b: 12 ms

表 18. ProchotOption1 Register (SMBus address = 34h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R/W	0b	Reserved
6	PROCHOT _PROFILE_COMP	R/W	0b	$\overline{\text{PROCHOT}}$ Profile When all the REG0x34[6:0] bits are 0, $\overline{\text{PROCHOT}}$ function is disabled. Bit6 Independent comparator 0b: disable <default at POR> 1b: enable
5	PROCHOT _PROFILE_ICRIT	R/W	1b	0b: disable 1b: enable <default at POR>
4	PROCHOT _PROFILE_INOM	R/W	0b	0b: disable <default at POR> 1b: enable
3	PROCHOT _PROFILE_IDCHG	R/W	0b	0b: disable <default at POR> 1b: enable
2	PROCHOT _PROFILE_VSYS	R/W	0b	0b: disable <default at POR> 1b: enable
1	PROCHOT _PROFILE_BATPRES	R/W	0b	0b: disable <default at POR> 1b: enable (one-shot falling edge triggered) If BATPRES is enabled in $\overline{\text{PROCHOT}}$ after the battery is removed, it will immediately send out one-shot $\overline{\text{PROCHOT}}$ pulse.

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表 18. ProchotOption1 Register (SMBus address = 34h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
0	PROCHOT _PROFILE_ACOK	R/W	0b	0b: disable <default at POR> 1b: enable ChargeOption0[15] = 0 to assert $\overline{\text{PROCHOT}}$ pulse after adapter removal. If PROCHOT_PROFILE_ACOK is enabled in $\overline{\text{PROCHOT}}$ after the adapter is removed, it will be pulled low.

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8.6.1.7 ADCOption Register (SMBus address = 35h) [reset = 2000h]

図 23. ADCOption Register (SMBus address = 35h) [reset = 2000h]

15	14	13	12-8				
ADC_CONV	ADC_START	ADC_ FULLSCALE	Reserved				
R/W	R/W	R/W	R/W				
7	6	5	4	3	2	1	0
EN_ADC_ CMPIN	EN_ADC_ VBUS	EN_ADC_ PSYS	EN_ADC_ IIN	EN_ADC_ IDCHG	EN_ADC_ ICHG	EN_ADC_ VSYS	EN_ADC_ VBAT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

The ADC registers are read in the following order: VBAT, VSYS, ICHG, IDCHG, IIN, PSYS, VBUS, CMPIN. ADC is disabled in low power mode. When enabling ADC, the device exit low power mode at battery only.

表 19. ADCOption Register (SMBus address = 35h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	ADC_CONV	R/W	0b	Typical ADC conversion time is 10 ms. 0b: One-shot update. Do one set of conversion updates to registers REG0x23(), REG0x24(), REG0x25(), and REG0x26() after ADC_START = 1. 1b: Continuous update. Do a set of conversion updates to registers REG0x23(), REG0x24(), REG0x25(), and REG0x26() every 1 sec.
14	ADC_START	R/W	0b	0b: No ADC conversion 1b: Start ADC conversion. After the one-shot update is complete, this bit automatically resets to zero
13	ADC_ FULLSCALE	R/W	1b	ADC input voltage range. When input voltage is below 5 V, or battery is 1S, full scale 2.04 V is recommended. 0b: 2.04 V 1b: 3.06 V <default at POR>
12-8	Reserved	R/W	00000b	Reserved

表 20. ADCOption Register (SMBus address = 35h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	EN_ADC_CMPIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
6	EN_ADC_VBUS	R/W	0b	0b: Disable <default at POR> 1b: Enable
5	EN_ADC_PSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
4	EN_ADC_IIN	R/W	0b	0b: Disable <default at POR> 1b: Enable
3	EN_ADC_IDCHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
2	EN_ADC_ICHG	R/W	0b	0b: Disable <default at POR> 1b: Enable
1	EN_ADC_VSYS	R/W	0b	0b: Disable <default at POR> 1b: Enable
0	EN_ADC_VBAT	R/W	0b	0b: Disable <default at POR> 1b: Enable

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8.6.2 Charge and $\overline{\text{PROCHOT}}$ Status

8.6.2.1 ChargerStatus Register (SMBus address = 20h) [reset = 0000h]

図 24. ChargerStatus Register (SMBus address = 20h) [reset = 0000h]

15	14	13	12	11	10	9	8
AC_STAT	ICO_DONE	Reserved	IN_VINDPM	IN_IINDPM	IN_FCHRG	IN_PCHRG	IN_OTG
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Fault ACOV	Fault BATOC	Fault ACOC	SYSOVP_ STAT	Reserved	Fault Latchoff	Fault_OTG_ OVP	Fault_OTG_ OCP
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. ChargerStatus Register (SMBus address = 20h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	AC_STAT	R	0b	Input source status, same as CHRG_OK pin 0b: Input not present 1b: Input is present
14	ICO_DONE	R	0b	After the ICO routine is successfully executed, the bit goes 1. 0b: ICO is not complete 1b: ICO is complete
13	Reserved	R	0b	Reserved
12	IN_VINDPM	R	0b	0b: Charger is not in VINDPM during forward mode, or voltage regulation during OTG mode 1b: Charger is in VINDPM during forward mode, or voltage regulation during OTG mode
11	IN_IINDPM	R	0b	0b: Charger is not in IINDPM 1b: Charger is in IINDPM
10	IN_FCHRG	R	0b	0b: Charger is not in fast charge 1b: Charger is in fast charger
9	IN_PCHRG	R	0b	0b: Charger is not in pre-charge 1b: Charger is in pre-charge
8	IN_OTG	R	0b	0b: Charger is not in OTG 1b: Charge is in OTG

表 22. ChargerStatus Register (SMBus address = 20h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Fault ACOV	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOV
6	Fault BATOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: BATOC
5	Fault ACOC	R	0b	The faults are latched until a read from host. 0b: No fault 1b: ACOC

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表 22. ChargerStatus Register (SMBus address = 20h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
4	SYSOVP_STAT	R	0b	SYSOVP Status and Clear When the SYSOVP occurs, this bit is HIGH. During the SYSOVP, the converter is disabled. After the SYSOVP is removed, the user must write a 0 to this bit or unplug the adapter to clear the SYSOVP condition to enable the converter again. 0b: Not in SYSOVP <default at POR> 1b: In SYSOVP. When SYSOVP is removed, write 0 to clear the SYSOVP latch.
3	Reserved	R	0b	Reserved
2	Fault Latchoff	R	0b	The faults are latched until a read from host. 0b: No fault 1b: Latch off (REG0x30[3])
1	Fault_OTG_OVP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG OVP
0	Fault_OTG_UCP	R	0b	The faults are latched until a read from host. 0b: No fault 1b: OTG OCP

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8.6.2.2 ProchotStatus Register (SMBus address = 21h) [reset = 0h]

図 25. ProchotStatus Register (SMBus address = 21h) [reset = 0h]

15-8							
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved	STAT_COMP	STAT_ICRIT	STAT_INOM	STAT_IDCHG	STAT_VSYS	STAT_Battery_Removal	STAT_Adapter_Removal
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. ProchotStatus Register (SMBus address = 21h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8	Reserved	R	00000000b	Reserved

表 24. ProchotStatus Register (SMBus address = 21h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Reserved	R	0b	Reserved
6	STAT_COMP	R	0b	0b: Not triggered 1b: Triggered
5	STAT_ICRIT	R	0b	0b: Not triggered 1b: Triggered
4	STAT_INOM	R	0b	0b: Not triggered 1b: Triggered
3	STAT_IDCHG	R	0b	0b: Not triggered 1b: Triggered
2	STAT_VSYS	R	0b	0b: Not triggered 1b: Triggered
1	STAT_Battery_Removal	R	0b	0b: Not triggered 1b: Triggered
0	STAT_Adapter_Removal	R	0b	0b: Not triggered 1b: Triggered

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8.6.3 ChargeCurrent Register (SMBus address = 14h) [reset = 0h]

To set the charge current, write a 16-bit ChargeCurrent() command (REG0x14h()) using the data format listed in 表 25 and 表 26.

With 10-mΩ sense resistor, the charger provides charge current range of 64 mA to 8.128 A, with a 64-mA step resolution. Upon POR, ChargeCurrent() is 0 A. Any conditions for CHRG_OK low except ACOV will reset ChargeCurrent() to zero. CELL_BATPRESZ going LOW (battery removal) will reset the ChargeCurrent() register to 0 A.

Charge current is not reset in ACOC, TSHUT, power path latch off (REG0x30[1]), and SYSOVP.

A 0.1-µF capacitor between SRP and SRN for differential mode filtering is recommended; an optional 0.1-µF capacitor between SRN and ground, and an optional 0.1-µF capacitor between SRP and ground for common mode filtering. Meanwhile, the capacitance on SRP should not be higher than 0.1 µF in order to properly sense the voltage across SRP and SRN for cycle-by-cycle current detection.

The SRP and SRN pins are used to sense voltage drop across RSR with default value of 10 mΩ. However, resistors of other values can also be used. For a larger sense resistor, a larger sense voltage is given, and a higher regulation accuracy; but, at the expense of higher conduction loss. A current sensing resistor value no more than 20 mΩ is suggested.

図 26. ChargeCurrent Register With 10-mΩ Sense Resistor (SMBus address = 14h) [reset = 0h]

15	14	13	12	11	10	9	8
Reserved			Charge Current, bit 6	Charge Current, bit 5	Charge Current, bit 4	Charge Current, bit 3	Charge Current, bit 2
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Charge Current, bit 1	Charge Current, bit 0	Reserved	Reserved				
R/W	R/W	R/W	R/W				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 25. Charge Current Register (14h) With 10-mΩ Sense Resistor (SMBus address = 14h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-13	Reserved	R/W	000b	Not used. 1 = invalid write.
12	Charge Current, bit 6	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 4096 mA of charger current.
11	Charge Current, bit 5	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 2048 mA of charger current.
10	Charge Current, bit 4	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 1024 mA of charger current.
9	Charge Current, bit 3	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 512 mA of charger current.
8	Charge Current, bit 2	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 256 mA of charger current.

表 26. Charge Current Register (14h) With 10-mΩ Sense Resistor (SMBus address = 14h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Charge Current, bit 1	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 128 mA of charger current.
6	Charge Current, bit 0	R/W	0b	0 = Adds 0 mA of charger current. 1 = Adds 64 mA of charger current.

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表 26. Charge Current Register (14h) With 10-mΩ Sense Resistor (SMBus address = 14h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

8.6.3.1 Battery Pre-Charge Current Clamp

During pre-charge, BATFET works in linear mode or LDO mode (default REG0x12[2] = 1). For 2-4 cell battery, the system is regulated at minimum system voltage in REG0x3E() and the pre-charge current is clamped at 384 mA. For 1 cell battery, the pre-charge to fast charge threshold is 3 V, and the pre-charge current is clamped at 384 mA. However, the BATFET stays in LDO mode operation till battery voltage is above minimum system voltage (~3.6 V). During battery voltage from 3 V to 3.6 V, the fast charge current is clamped at 2 A.

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8.6.4 MaxChargeVoltage Register (SMBus address = 15h) [reset value based on CELL_BATPRESZ pin setting]

To set the output charge voltage, write a 16-bit ChargeVoltage register command (REG0x15()) using the data format listed in 表 27 and 表 28. The charger provides charge voltage range from 1.024 V to 19.200 V, with 16-mV step resolution. Any write below 1.024 V or above 19.200 V is ignored. Upon POR or when charge is disabled, the system is regulated at the MaxChargeVoltage register.

Upon POR, REG0x15() is by default set as 4192 mV for 1 s, 8400 mV for 2 s, 12592 mV for 3 s or 16800 mV for 4 s. After CHRG_OK, if host writes REG0x14() before REG0x15(), the charge will start after the write to REG0x14().If the battery is different from 4.2 V/cell, the host has to write to REG0x15() before REG0x14() for correct battery voltage setting. Writing REG0x15() to 0 will set REG0x15() to default value on CELL_BATPRESZ pin, and force REG0x14() to zero to disable charge.

The SRN pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, and directly place a decoupling capacitor (0.1 µF recommended) as close to the device as possible to decouple high frequency noise.

図 27. MaxChargeVoltage Register (SMBus address = 15h) [reset value based on CELL_BATPRESZ pin setting]

15	14	13	12	11	10	9	8
Reserved	Max Charge Voltage, bit 10	Max Charge Voltage, bit 9	Max Charge Voltage, bit 8	Max Charge Voltage, bit 7	Max Charge Voltage, bit 6	Max Charge Voltage, bit 5	Max Charge Voltage, bit 4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Max Charge Voltage, bit 3	Max Charge Voltage, bit 2	Max Charge Voltage, bit 1	Max Charge Voltage, bit 0	Reserved			
R/W	R/W	R/W	R/W	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 27. MaxChargeVoltage Register (SMBus address = 15h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	Reserved	R/W	0b	Not used. 1 = invalid write.
14	Max Charge Voltage, bit 10	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16384 mV of charger voltage.
13	Max Charge Voltage, bit 9	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 8192 mV of charger voltage
12	Max Charge Voltage, bit 8	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 4096 mV of charger voltage.
11	Max Charge Voltage, bit 7	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 2048 mV of charger voltage.
10	Max Charge Voltage, bit 6	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 1024 mV of charger voltage.
9	Max Charge Voltage, bit 5	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 512 mV of charger voltage.
8	Max Charge Voltage, bit 4	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 256 mV of charger voltage.

表 28. MaxChargeVoltage Register (SMBus address = 15h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Max Charge Voltage, bit 3	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 128 mV of charger voltage.

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表 28. MaxChargeVoltage Register (SMBus address = 15h) Field Descriptions (continued)

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
6	Max Charge Voltage, bit 2	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 64 mV of charger voltage.
5	Max Charge Voltage, bit 1	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 32 mV of charger voltage.
4	Max Charge Voltage, bit 0	R/W	0b	0 = Adds 0 mV of charger voltage. 1 = Adds 16 mV of charger voltage.
3-0	Reserved	R/W	0000b	Not used. Value Ignored.

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8.6.5 MinSystemVoltage Register (SMBus address = 3Eh) [reset value based on CELL_BATPRESZ pin setting]

To set the minimum system voltage, write a 16-bit MinSystemVoltage register command (REG0x3E()) using the data format listed in 表 29 and 表 30. The charger provides minimum system voltage range from 1.024 V to 16.128 V, with 256-mV step resolution. Any write below 1.024 V or above 16.128 V is ignored. Upon POR, the MinSystemVoltage register is 3.584 V for 1 S, 6.144 V for 2 S and 9.216 V for 3 S, and 12.288 V for 4 S.

図 28. MinSystemVoltage Register (SMBus address = 3Eh) [reset value based on CELL_BATPRESZ pin setting]

15	14	13	12	11	10	9	8
Reserved		Min System Voltage, bit 5	Min System Voltage, bit 4	Min System Voltage, bit 3	Min System Voltage, bit 2	Min System Voltage, bit 1	Min System Voltage, bit 0
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 29. MinSystemVoltage Register (SMBus address = 3Eh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	Reserved	R/W	00b	Not used. 1 = invalid write.
13	Min System Voltage, bit 5	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 8192 mV of system voltage.
12	Min System Voltage, bit 4	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 4096mV of system voltage.
11	Min System Voltage, bit 3	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 2048 mV of system voltage.
10	Min System Voltage, bit 2	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 1024 mV of system voltage.
9	Min System Voltage, bit 1	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 512 mV of system voltage.
8	Min System Voltage, bit 0	R/W	0b	0 = Adds 0 mV of system voltage. 1 = Adds 256 mV of system voltage.

表 30. MinSystemVoltage Register (SMBus address = 3Eh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

8.6.5.1 System Voltage Regulation

The device employs Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG0x3E(). Even with a deeply depleted battery, the system is regulated above the minimum system voltage with BATFET.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is regulated above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on when charging or in supplement mode and the voltage difference between the system and battery is the VDS of BATFET. System voltage is regulated 160 mV above battery voltage when BATFET is off (no charging or no supplement current).

When BATFET is removed, the system node VSYS is shorted to SRP. Before the converter starts operation, LDO mode needs to be disabled. The following sequence is required to configure charger without BATFET.

1. Before adapter plugs in, put the charger into HIZ mode. (either pull pin 6 ILIM_HIZ to ground, or set

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REG0x32[15] to 1)

2. Set 0x12[2] to 0 to disable LDO mode.
3. Set 0x30[0] to 0 to disable auto-wakeup mode.
4. Check if battery voltage is properly programmed (REG0x15)
5. Set pre-charge/charge current (REG0x14)
6. Put the device out of HIZ mode. (Release ILIM_HIZ from ground and set REG0x32[15]=0).

In order to prevent any accidental SW mistakes, the host sets low input current limit (a few hundred milliamps) when device is out of HIZ.

8.6.6 Input Current and Input Voltage Registers for Dynamic Power Management

The charger supports Dynamic Power Management (DPM). Normally, the input power source provides power for the system load or to charge the battery. When the input current exceeds the input current setting, or the input voltage falls below the input voltage setting, the charger decreases the charge current to provide priority to the system load. As the system current rises, the available charge current drops accordingly towards zero. If the system load keeps increasing after the charge current drops down to zero, the system voltage starts to drop. As the system voltage drops below the battery voltage, the battery will discharge to supply the heavy system load.

8.6.6.1 Input Current Registers

To set the maximum input current limit, write a 16-bit IIN_HOST register command (REG0x3F()) using the data format listed in 表 31 and 表 32. When using a 10-mΩ sense resistor, the charger provides an input-current limit range of 50 mA to 6400 mA, with 50-mA resolution. The default current limit is 3.3 A. Due to the USB current setting requirement, the register setting specifies the maximum current instead of the typical current. Upon adapter removal, the input current limit is reset to the default value of 3.3 A. The register offset is 50 mA. With code 0, the input current limit is 50 mA.

The ACP and ACN pins are used to sense R_{AC} with the default value of 10 mΩ. For a 20-mΩ sense resistor, a larger sense voltage is given and a higher regulation accuracy, but at the expense of higher conduction loss.

Instead of using the internal DPM loop, the user can build up an external input current regulation loop and have the feedback signal on the ILIM_HIZ pin.

$$V_{ILIM_HIZ} = 1V + 40 \times (V_{ACP} - V_{ACN}) = 1 + 40 \times I_{DPM} \times R_{AC} \quad (2)$$

In order to disable ILIM_HIZ pin, the host can write to 0x31[7] to disable ILIM_HIZ pin, or pull ILIM_HIZ pin above 4.0 V.

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8.6.6.1.1 IIN_HOST Register With 10-mΩ Sense Resistor (SMBus address = 3Fh) [reset = 4000h]

The register offset is 50 mA. With code 0, the input current limit readback is 50 mA.

図 29. IIN_HOST Register With 10-mΩ Sense Resistor (SMBus address = 3Fh) [reset = 4100h]

15	14	13	12	11	10	9	8
Reserved	Input Current set by host, bit 6	Input Current set by host, bit 5	Input Current set by host, bit 4	Input Current set by host, bit 3	Input Current set by host, bit 2	Input Current set by host, bit 1	Input Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 31. IIN_HOST Register With 10-mΩ Sense Resistor (SMBus address = 3Fh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	Reserved	R/W	0b	Not used. 1 = invalid write.
14	Input Current set by host, bit 6	R/W	1b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
13	Input Current set by host, bit 5	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
12	Input Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 800 mA of input current.
11	Input Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
10	Input Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
9	Input Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
8	Input Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

表 32. IIN_HOST Register With 10-mΩ Sense Resistor (SMBus address = 3Fh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

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8.6.6.1.2 IIN_DPM Register With 10-mΩ Sense Resistor (SMBus address = 022h) [reset = 0h]

IIN_DPM register reflects the actual input current limit programmed in the register, either from host or from ICO.

After ICO, the current limit used by DPM regulation may differ from the IIN_HOST register settings. The actual DPM limit is reported in REG0x22(). The register offset is 50 mA. With code 0, the input current limit read-back is 50 mA.

図 30. IIN_DPM Register With 10-mΩ Sense Resistor (SMBus address = 022h) [reset = 0h]

15	14	13	12	11	10	9	8
Reserved	Input Current in DPM, bit 6	Input Current in DPM, bit 5	Input Current in DPM, bit 4	Input Current in DPM, bit 3	Input Current in DPM, bit 2	Input Current in DPM, bit 1	Input Current in DPM, bit 0
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 33. IIN_DPM Register With 10-mΩ Sense Resistor (SMBus address = 022h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	Reserved	R	0b	Not used. 1 = invalid write.
14	Input Current in DPM, bit 6	R	0b	0 = Adds 0 mA of input current. 1 = Adds 3200 mA of input current.
13	Input Current in DPM, bit 5	R	0b	0 = Adds 0 mA of input current. 1 = Adds 1600 mA of input current.
12	Input Current in DPM, bit 4	R	0b	0 = Adds 0 mA of input current. 1 = Adds 800mA of input current
11	Input Current in DPM, bit 3	R	0b	0 = Adds 0 mA of input current. 1 = Adds 400 mA of input current.
10	Input Current in DPM, bit 2	R	0b	0 = Adds 0 mA of input current. 1 = Adds 200 mA of input current.
9	Input Current in DPM, bit 1	R	0b	0 = Adds 0 mA of input current. 1 = Adds 100 mA of input current.
8	Input Current in DPM, bit 0	R	0b	0 = Adds 0 mA of input current. 1 = Adds 50 mA of input current.

表 34. IIN_DPM Register With 10-mΩ Sense Resistor (SMBus address = 022h) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R	00000000b	Not used. Value Ignored.

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8.6.6.1.3 InputVoltage Register (SMBus address = 3Dh) [reset = VBUS-1.28V]

To set the input voltage limit, write a 16-bit InputVoltage register command (REG0x3D()) using the data format listed in 表 35 and 表 36.

If the input voltage drops more than the InputVoltage register allows, the device enters DPM and reduces the charge current. The default offset voltage is 1.28 V below the no-load VBUS voltage. The DC offset is 3.2 V (0000000).

図 31. InputVoltage Register (SMBus address = 3Dh) [reset = VBUS-1.28V]

15	14	13	12	11	10	9	8
Reserved		Input Voltage, bit 7	Input Voltage, bit 6	Input Voltage, bit 5	Input Voltage, bit 4	Input Voltage, bit 3	Input Voltage, bit 2
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Input Voltage, bit 1	Input Voltage, bit 0	Reserved					
R/W	R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 35. InputVoltage Register (SMBus address = 3Dh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	Reserved	R/W	00b	Not used. 1 = invalid write.
13	Input Voltage, bit 7	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 8192 mV of input voltage.
12	Input Voltage, bit 6	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 4096mV of input voltage.
11	Input Voltage, bit 5	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 2048 mV of input voltage.
10	Input Voltage, bit 4	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 1024 mV of input voltage.
9	Input Voltage, bit 3	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 512 mV of input voltage.
8	Input Voltage, bit 2	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 256 mV of input voltage.

表 36. InputVoltage Register (SMBus address = 3Dh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	Input Voltage, bit 1	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 128 mV of input voltage.
6	Input Voltage, bit 0	R/W	0b	0 = Adds 0 mV of input voltage. 1 = Adds 64 mV of input voltage
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

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8.6.7 OTGVoltage Register (SMBus address = 3Bh) [reset = 0h]

To set the OTG output voltage limit, write to REG0x3B() using the data format listed in 表 37 and 表 38. The DC offset is 4.48 V (0000000).

図 32. OTGVoltage Register (SMBus address = 3Bh) [reset = 0h]

15	14	13	12	11	10	9	8
Reserved		OTG Voltage, bit 7	OTG Voltage, bit 6	OTG Voltage, bit 5	OTG Voltage, bit 4	OTG Voltage, bit 3	OTG Voltage, bit 2
R/W		R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
OTG Voltage, bit 1	OTG Voltage, bit 0	Reserved					
R/W	R/W	R/W					

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 37. OTGVoltage Register (SMBus address = 3Bh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15-14	Reserved	R/W	00b	Not used. 1 = invalid write.
13	OTG Voltage, bit 7	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 8192 mV of OTG voltage.
12	OTG Voltage, bit 6	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 4096 mV of OTG voltage.
11	OTG Voltage, bit 5	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 2048 mV of OTG voltage.
10	OTG Voltage, bit 4	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 1024 mV of OTG voltage.
9	OTG Voltage, bit 3	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 512 mV of OTG voltage.
8	OTG Voltage, bit 2	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 256 mV of OTG voltage.

表 38. OTGVoltage Register (SMBus address = 3Bh) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7	OTG Voltage, bit 1	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 128 mV of OTG voltage.
6	OTG Voltage, bit 0	R/W	0b	0 = Adds 0 mV of OTG voltage. 1 = Adds 64 mV of OTG voltage.
5-0	Reserved	R/W	000000b	Not used. Value Ignored.

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8.6.8 OTGCurrent Register (SMBus address = 3Ch) [reset = 0h]

To set the OTG output current limit, write to REG0x3C() using the data format listed in 表 39 and 表 40.

図 33. OTGCurrent Register (SMBus address = 3Ch) [reset = 0h]

15	14	13	12	11	10	9	8
Reserved	OTG Current set by host, bit 6	OTG Current set by host, bit 5	OTG Current set by host, bit 4	OTG Current set by host, bit 3	OTG Current set by host, bit 2	OTG Current set by host, bit 1	OTG Current set by host, bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 39. OTGCurrent Register (SMBus address = 3Ch) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
15	Reserved	R/W	0b	Not used. 1 = invalid write.
14	OTG Current set by host, bit 6	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 3200 mA of OTG current.
13	OTG Current set by host, bit 5	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 1600mA of OTG current.
12	OTG Current set by host, bit 4	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 800 mA of OTG current.
11	OTG Current set by host, bit 3	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 400 mA of OTG current.
10	OTG Current set by host, bit 2	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 200 mA of OTG current.
9	OTG Current set by host, bit 1	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 100 mA of OTG current.
8	OTG Current set by host, bit 0	R/W	0b	0 = Adds 0 mA of OTG current. 1 = Adds 50 mA of OTG current.

表 40. OTGCurrent Register (SMBus address = 3Ch) Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION
7-0	Reserved	R/W	00000000b	Not used. Value Ignored.

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8.6.9 ADCVBUS/PSYS Register (SMBus address = 23h)

- PSYS: Full range: 3.06 V, LSB: 12 mV
- VBUS: Full range: 3200 mV to 19520 mV, LSB: 64 mV

図 34. ADCVBUS/PSYS Register (SMBus address = 23h)

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 41. ADCVBUS/PSYS Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8		R		8-bit Digital Output of Input Voltage
7-0		R		8-bit Digital Output of System Power

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8.6.10 ADCIBAT Register (SMBus address = 24h)

- ICHG: Full range: 8.128 A, LSB: 64 mA
- IDCHG: Full range: 32.512 A, LSB: 256 mA

図 35. ADCIBAT Register (SMBus address = 24h)

15	14	13	12	11	10	9	8
Reserved	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
Reserved	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 42. ADCIBAT Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15	Reserved	R		Not used. Value ignored.
14-8		R		7-bit Digital Output of Battery Charge Current
7	Reserved	R		Not used. Value ignored.
6-0		R		7-bit Digital Output of Battery Discharge Current

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8.6.11 ADCIINCMPIN Register (SMBus address = 25h)

- IIN: Full range: 12.75 A, LSB: 50 mA
- CMPIN: Full range: 3.06 V, LSB: 12 mV

図 36. ADCIINCMPIN Register (SMBus address = 25h)

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 43. ADCIINCMPIN Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8		R		8-bit Digital Output of Input Current
7-0		R		8-bit Digital Output of CMPIN voltage

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8.6.12 ADCVSYSVBAT Register (SMBus address = 26h)

- VSYS: Full range: 2.88 V to 19.2 V, LSB: 64 mV
- VBAT: Full range: 2.88 V to 19.2 V, LSB: 64 mV

図 37. ADCVSYSVBAT Register (SMBus address = 26h) (reset =)

15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 44. ADCVSYSVBAT Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
15-8		R		8-bit Digital Output of System Voltage
7-0		R		8-bit Digital Output of Battery Voltage

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8.6.13 ID Registers

8.6.13.1 ManufactureID Register (SMBus address = FEh) [reset = 0040h]

図 38. ManufactureID Register (SMBus address = FEh) [reset = 0040h]

15-0
MANUFACTURE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 45. ManufactureID Register Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
15-0	MANUFACTURE_ID	R		40h

8.6.13.2 Device ID (DeviceAddress) Register (SMBus address = FFh) [reset = 0h]

図 39. Device ID (DeviceAddress) Register (SMBus address = FFh) [reset = 0h]

15-8
Reserved
R
7-0
DEVICE_ID
R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 46. Device ID (DeviceAddress) Register Field Descriptions

SMBus BIT	FIELD	TYPE	RESET	DESCRIPTION (READ ONLY)
15-8	Reserved	R	0b	Reserved
7-0	DEVICE_ID	R	0b	SMBus: 79h

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9 Application and Implementation

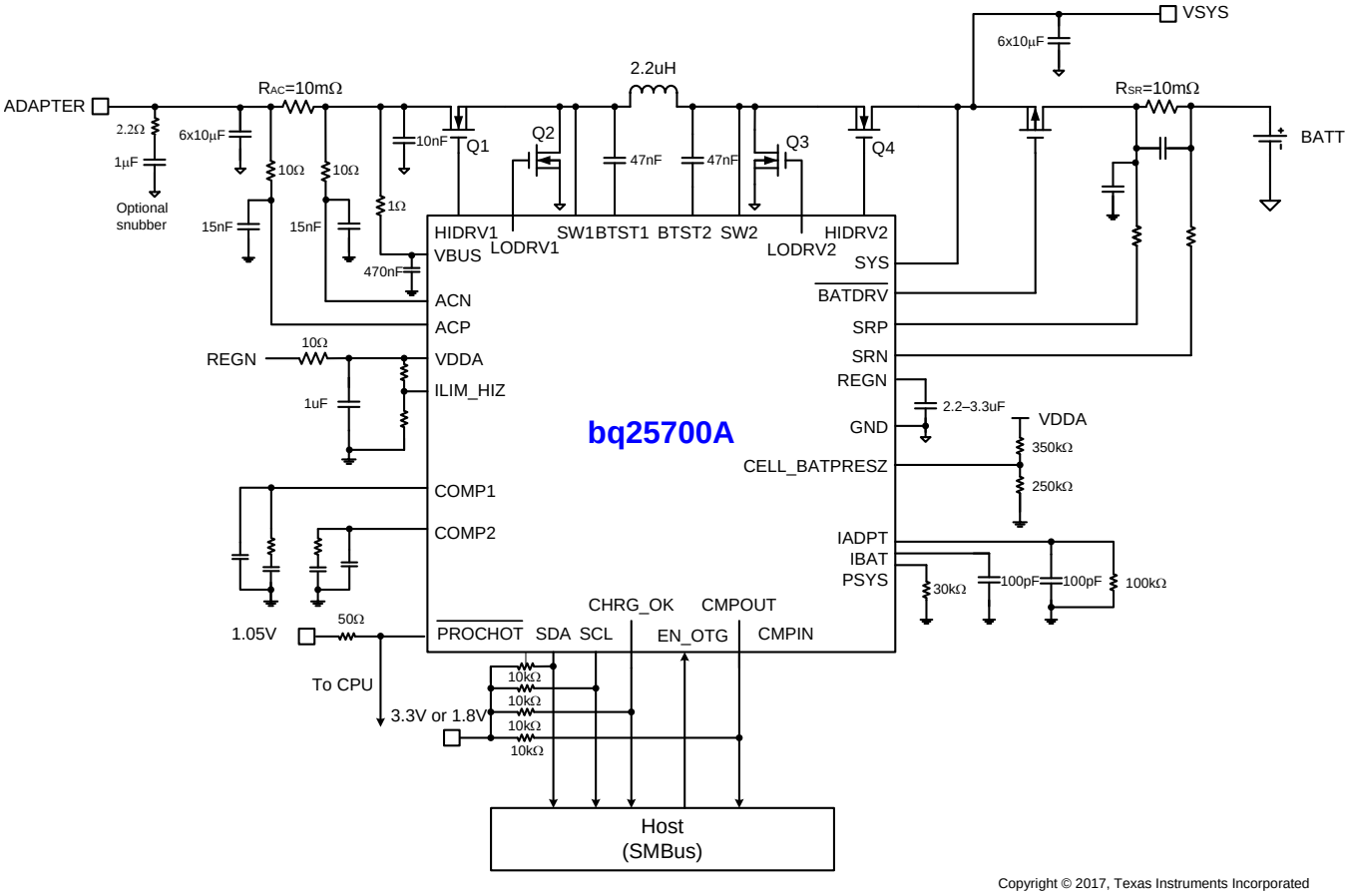
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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The bq2570xEVM-732 evaluation module (EVM) is a complete charger module for evaluating the bq25700A. The application curves were taken using the bq2570xEVM-732. Refer to the EVM user's guide (SLUUBG6) for EVM information.

9.2 Typical Application



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図 40. Application Diagram

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (1)	3.5 V < Adapter Voltage < 24 V
Input Current Limit (1)	3.2 A for 65 W adapter
Battery Charge Voltage (2)	8400 mV for 2s battery

(1) Refer to adapter specification for settings for Input Voltage and Input Current Limit.
(2) Refer to battery specification for settings.

Typical Application (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Battery Charge Current(2)	3072 mA for 2s battery
Minimum System Voltage(2)	6144 mV for 2s battery

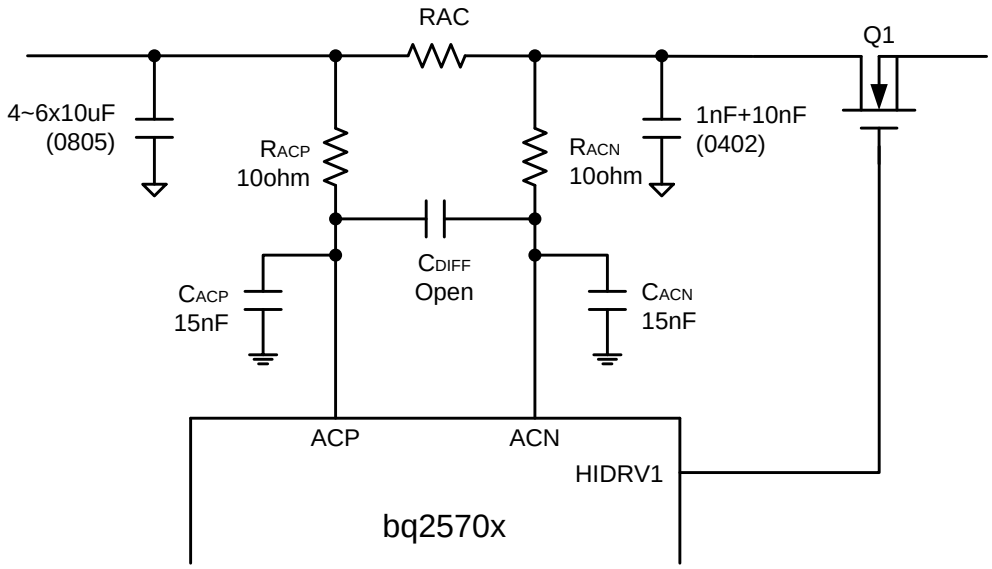
9.2.2 Detailed Design Procedure

The parameters are configurable using the evaluation software. The simplified application circuit (see 図 40, as the application diagram) shows the minimum component requirements. Inductor, capacitor, and MOSFET selection are explained in the rest of this section. Refer to the EVM user's guide (SLUUBG6) for the complete application schematic.

9.2.2.1 ACP-ACN Input Filter

The bq25700A has average current mode control. The input current sensing through ACP/ACN is critical to recover inductor current ripple. Parasitic inductance on board will generate high frequency ringing on ACP-ACN which overwhelms converter sensed inductor current information, so it is difficult to manage parasitic inductance created based on different PCB layout. Bigger parasitic inductance will generate bigger sense current ringing which will cause the average current control loop to go into oscillation.

For real system board condition, we suggest to use below circuit design to get best result and filter noise induced from different PCB parasitic factor. With time constant of filter from 47 nsec to 200 nsec, the filtering on ringing is effective and in the meantime, the delay of on the sensed signal is small and therefore poses no concern for average current mode control.



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図 41. ACN-ACP Input Filter

9.2.2.2 Inductor Selection

The bq25700A has two selectable fixed switching frequency. Higher switching frequency allows the use of smaller inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (3)$$

The inductor ripple current in buck operation depends on input voltage (V_{IN}), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$) and inductance (L):

$$I_{RIPPLE_BUCK} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (4)$$

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During boost operation, the duty cycle is:

$$D_{BOOST} = 1 – (V_{IN}/V_{BAT})$$

and the ripple current is:

$$I_{RIPPLE_BOOST} = (VIN \times D_{BOOST}) / (f_S \times L)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5 in buck mode. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current occurs where the duty cycle is closest to 50% and can be estimated by 式 5:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \quad (5)$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25 V rating or higher capacitor is preferred for 19 V - 20 V input voltage. Minimum 4 - 6 pcs of 10-µF 0805 size capacitor is suggested for 45 - 65 W adapter design.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the input capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high input voltages and small capacitor packages. See the manufacturer's datasheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.4 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. In buck mode the output capacitor RMS current is given:

To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 10 kHz and 20 kHz. The preferred ceramic capacitor is 25-V X7R or X5R for output capacitor. Minimum 6 pcs of 10-µF 0805 size capacitor is suggested to be placed by the inductor. Place the capacitors after Q4 drain. Place minimum 10 µF after the charge current sense resistor for best stability.

Ceramic capacitors show a dc-bias effect. This effect reduces the effective capacitance when a dc-bias voltage is applied across a ceramic capacitor, as on the output capacitor of a charger. The effect may lead to a significant capacitance drop, especially for high output voltages and small capacitor packages. See the manufacturer's data sheet about the performance with a dc bias voltage applied. It may be necessary to choose a higher voltage rating or nominal capacitance value in order to get the required value at the operating point.

9.2.2.5 Power MOSFETs Selection

Four external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. 30 V or higher voltage rating MOSFETs are preferred for 19 V - 20 V input voltage.

Figure-of-merit (FOM) is usually used for selecting proper MOSFET based on a tradeoff between the conduction loss and switching loss. For the top side MOSFET, FOM is defined as the product of a MOSFET's on-resistance, $R_{DS(ON)}$, and the gate-to-drain charge, Q_{GD}. For the bottom side MOSFET, FOM is defined as the product of the MOSFET's on-resistance, $R_{DS(ON)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD}; \; FOM_{bottom} = R_{DS(on)} \times Q_G \quad (6)$$

The lower the FOM value, the lower the total power loss. Usually lower $R_{DS(ON)}$ has higher cost with the same package size.

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The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D=V_{OUT}/V_{IN}$), charging current (I_{CHG}), MOSFET's on-resistance ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn on time (t_{on}) and turn off time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times (t_{on} + t_{off}) \times f_s \quad (7)$$

The first item represents the conduction loss. Usually MOSFET $R_{DS(ON)}$ increases by 50% with 100°C junction temperature rise. The second term represents the switching loss. The MOSFET turn-on and turn-off times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \quad t_{off} = \frac{Q_{SW}}{I_{off}} \quad (8)$$

where Q_{sw} is the switching charge, I_{on} is the turn-on gate driving current and I_{off} is the turn-off gate driving current. If the switching charge is not given in MOSFET datasheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (9)$$

Gate driving current can be estimated by REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turn-on gate resistance (R_{on}) and turn-off gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \quad I_{off} = \frac{V_{plt}}{R_{off}} \quad (10)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous continuous conduction mode:

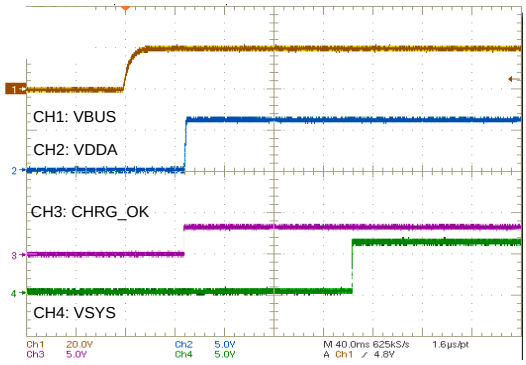
$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (11)$$

When charger operates in non-synchronous mode, the bottom-side MOSFET is off. As a result all the freewheeling current goes through the body-diode of the bottom-side MOSFET. The body diode power loss depends on its forward voltage drop (V_F), non-synchronous mode charging current ($I_{NONSYNC}$), and duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D) \quad (12)$$

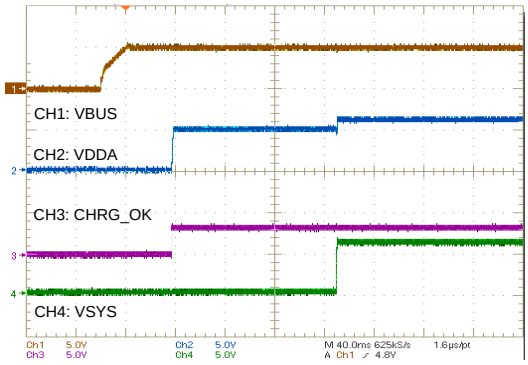
The maximum charging current in non-synchronous mode can be up to 0.25 A for a 10-mΩ charging current sensing resistor or 0.5 A if battery voltage is below 2.5 V. The minimum duty cycle happens at lowest battery voltage. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum non-synchronous mode charging current.

9.2.3 Application Curves



2-cell without battery

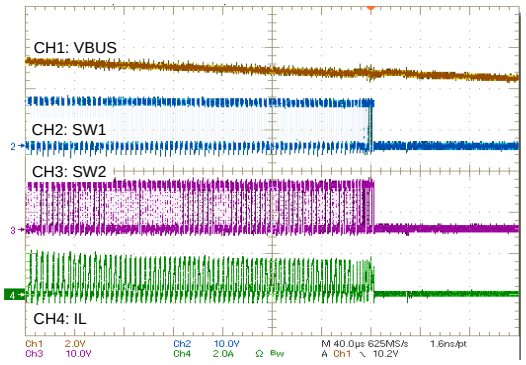
図 42. Power Up from 20 V



2-cell without battery

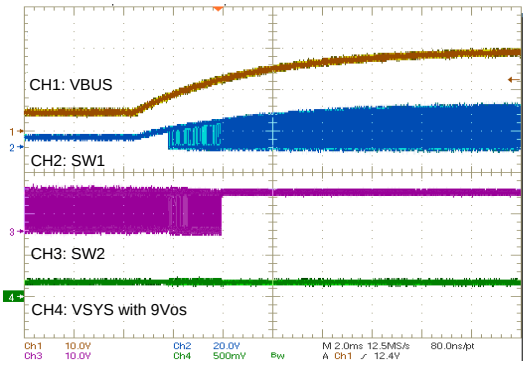
図 43. Power Up from 5 V

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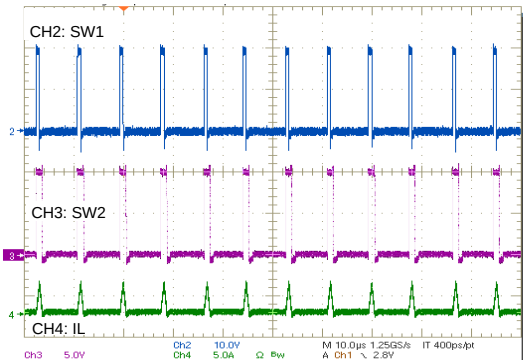
3-cell VBAT = 10 V

図 44. Power Off from 12 V



VBUS 5 V to 20 V

図 45. System Regulation



VBUS = 20 V, VSYS = 10 V, ISYS = 200 mA

図 46. PFM Operation

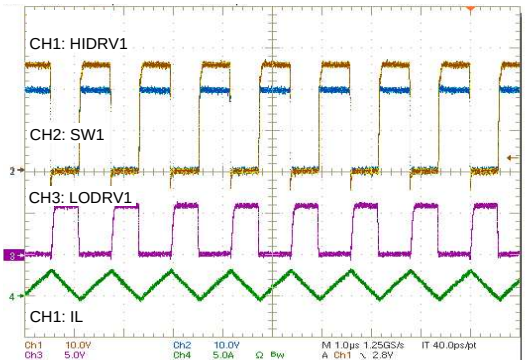
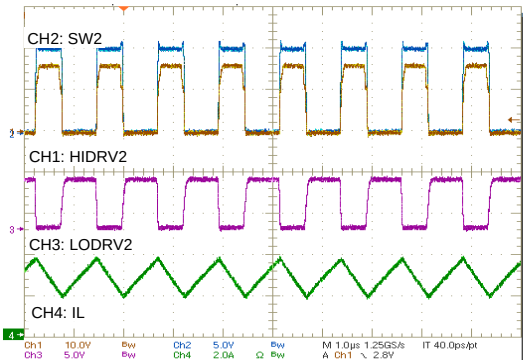
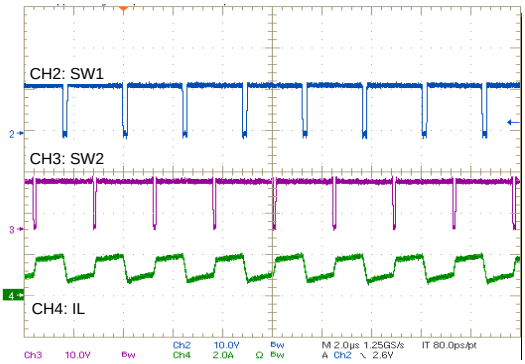


図 47. PWM Operation



VBUS = 5 V, VBAT = 10 V

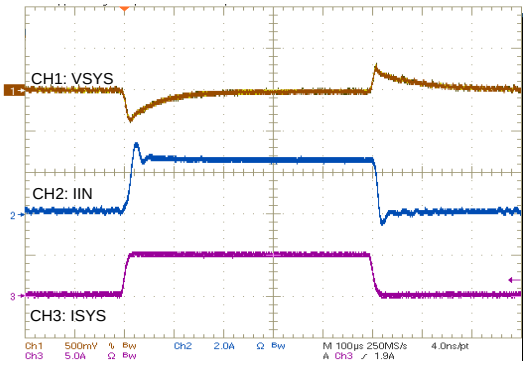
図 48. Switching During Boost Mode



VBUS = 12 V, VBAT = 12 V

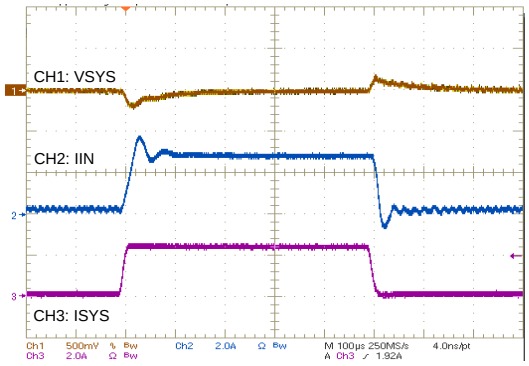
図 49. Switching During Buck Boost Mode

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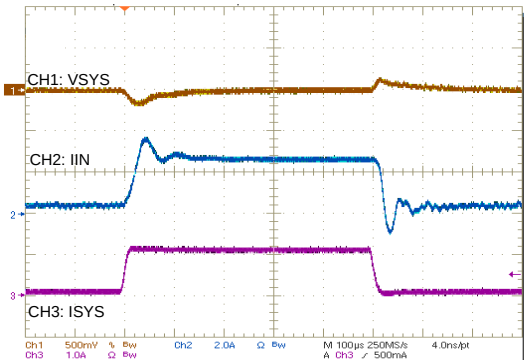
VBUS = 12 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

図 50. System Regulation in Buck Mode



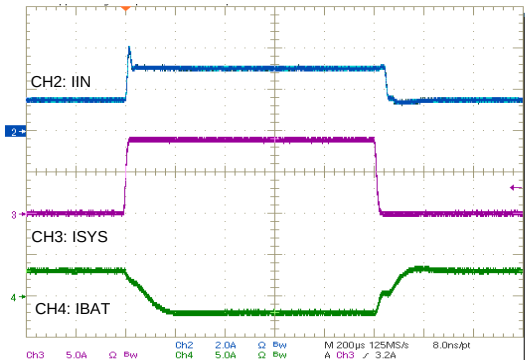
VBUS = 9 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

図 51. System Regulation in Buck Boost Mode



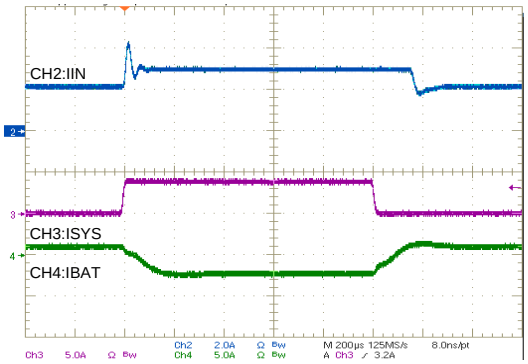
VBUS = 5 V/3.3 A, 3-cell, VSYS = 9 V, Without battery

図 52. System Regulation in Boost Mode



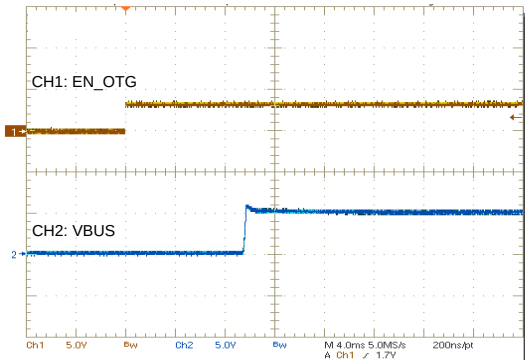
VBUS = 20 V/3.3 V, VBAT = 7.5 V

図 53. Input Current Regulation in Buck Mode



VBUS = 5 V/3.3 V, VBAT = 7.5 V

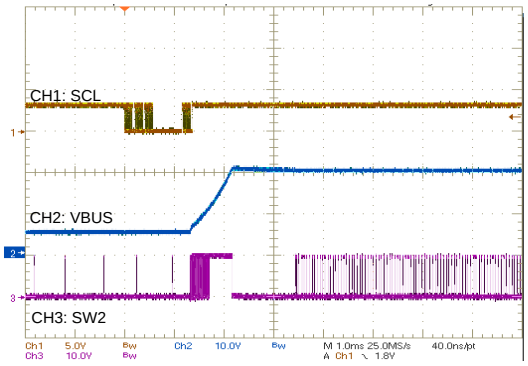
図 54. Input Current in Boost Mode



VBUS = 5 V

図 55. OTG Power Up from 8 V Battery

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VBAT = 10 V, VBUS 5 V to 20 V, IOTG = 500 mA

図 56. OTG Voltage Ramp Up

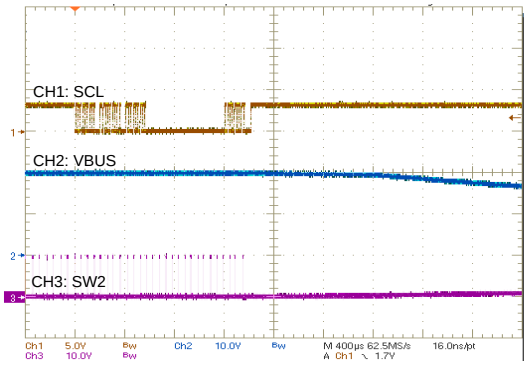
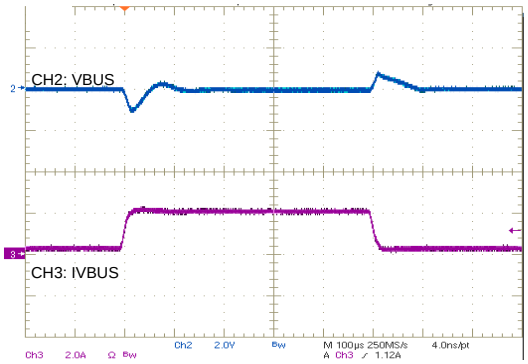


図 57. OTG Power Off



VBAT = 10 V, VBUS = 20 V

図 58. OTG Load Transient

10 Power Supply Recommendations

The valid adapter range is from 3.5 V (V_{VBUS_CONVEN}) to 24 V (ACOV) with at least 500-mA current rating. When CHRG_OK goes HIGH, the system is powered from adapter through the charger. When adapter is removed, the system is connected to battery through BATFET. Typically the battery depletion threshold should be greater than the minimum system voltage so that the battery capacity can be fully utilized for maximum battery life.

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11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see *Layout Example* section) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to the supply of the switching MOSFET and ground connections. Use a short copper trace connection. These parts must be placed on the same layer of PCB using vias to make this connection.
2. The device must be placed close to the gate pins of the switching MOSFET. Keep the gate drive signal traces short for a clean MOSFET drive. The device can be placed on the other side of the PCB of switching MOSFETs.
3. Place an inductor input pin as close as possible to the output pin of the switching MOSFET. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the device in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see 図 60 for Kelvin connection for best current accuracy). Place a decoupling capacitor on these traces next to the device.
5. Place an output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Use a single ground connection to tie the charger power ground to the charger analog ground. Just beneath the device, use analog ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
8. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground (power pad should tie to analog ground in this case if possible).
9. Decoupling capacitors must be placed next to the device pins. Make trace connection as short as possible.
10. It is critical that the exposed power pad on the backside of the device package be soldered to the PCB ground.
11. The via size and number should be enough for a given current path. See the EVM design (SLUUBG6) for the recommended component placement with trace and via locations. For WQFN information, see SLUA271.

11.2 Layout Example

11.2.1 Layout Consideration of Current Path

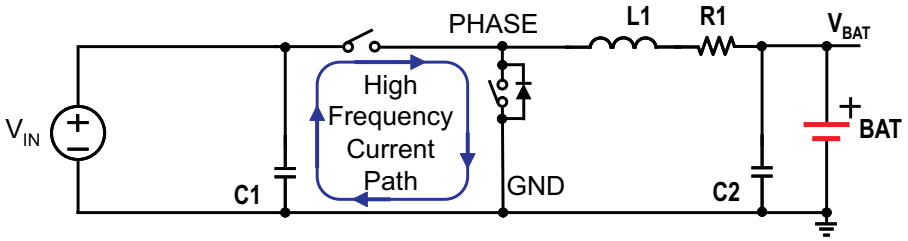


図 59. High Frequency Current Path

Layout Example (continued)

11.2.2 Layout Consideration of Short Circuit Protection

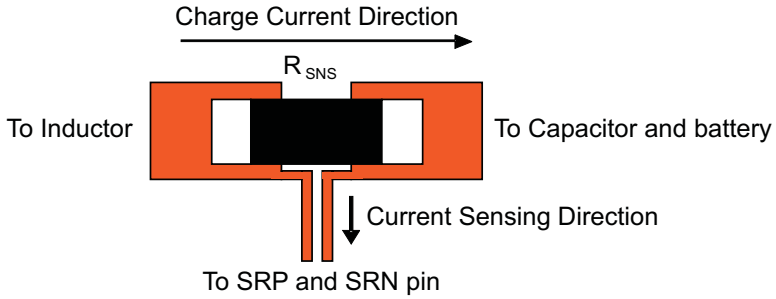


図 60. Sensing Resistor PCB Layout

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12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『半導体およびICパッケージの熱指標』*アプリケーション・レポートSPRA953
- *『bq2570x評価モジュール・ユーザー・ガイド』*SLUUBG6
- *『QFN/SONのPCB実装』*アプリケーション・レポートSLUA271

12.3 ドキュメントの更新通知を受け取る方法

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12.4 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25700ARSNR	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	BQ 25700A
BQ25700ARSNR.A	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25700A
BQ25700ARSNRG4	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25700A
BQ25700ARSNRG4.A	Active	Production	QFN (RSN) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25700A
BQ25700ARSNT	Active	Production	QFN (RSN) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25700A
BQ25700ARSNT.A	Active	Production	QFN (RSN) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25700A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

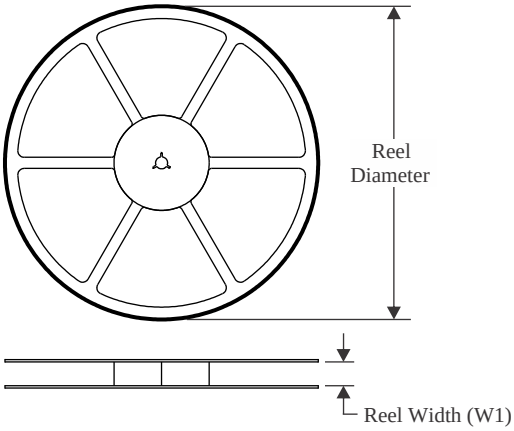
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

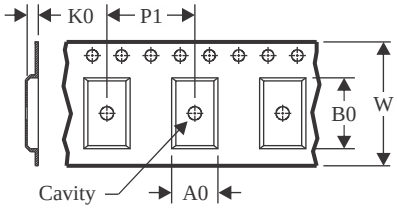
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

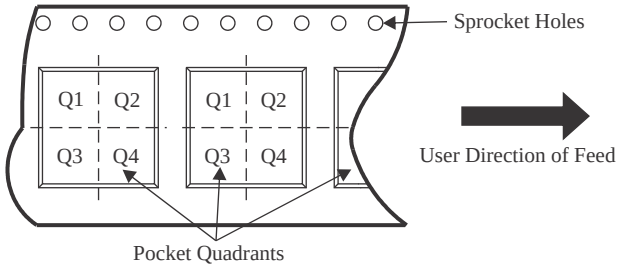


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

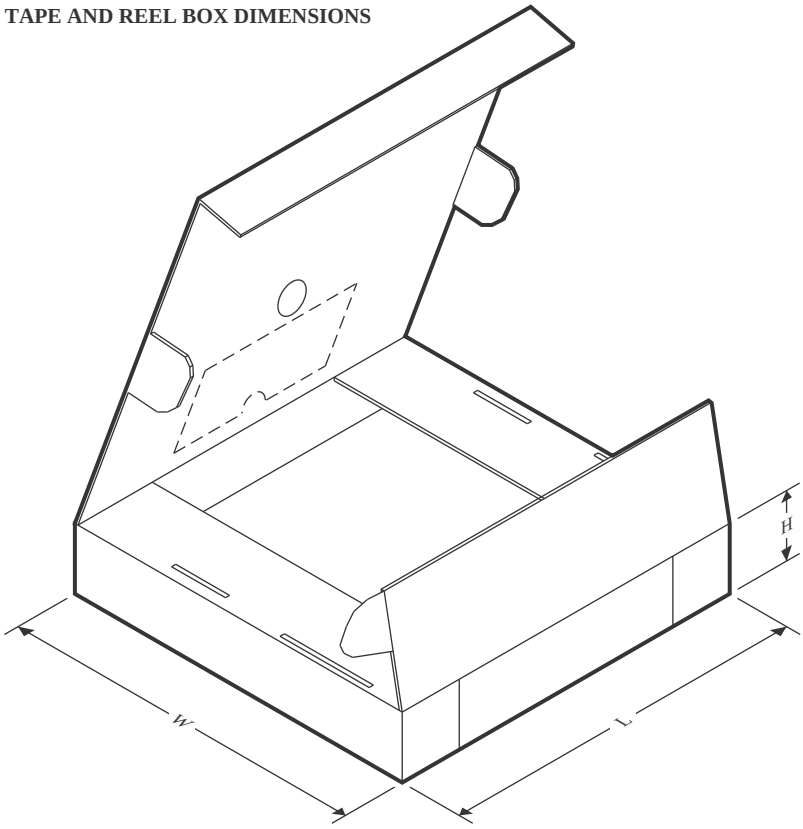
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25700ARSNR	QFN	RSN	32	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2
BQ25700ARSNRG4	QFN	RSN	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25700ARSNT	QFN	RSN	32	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25700ARSNR	QFN	RSN	32	3000	353.0	353.0	32.0
BQ25700ARSNRG4	QFN	RSN	32	3000	367.0	367.0	35.0
BQ25700ARSNT	QFN	RSN	32	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

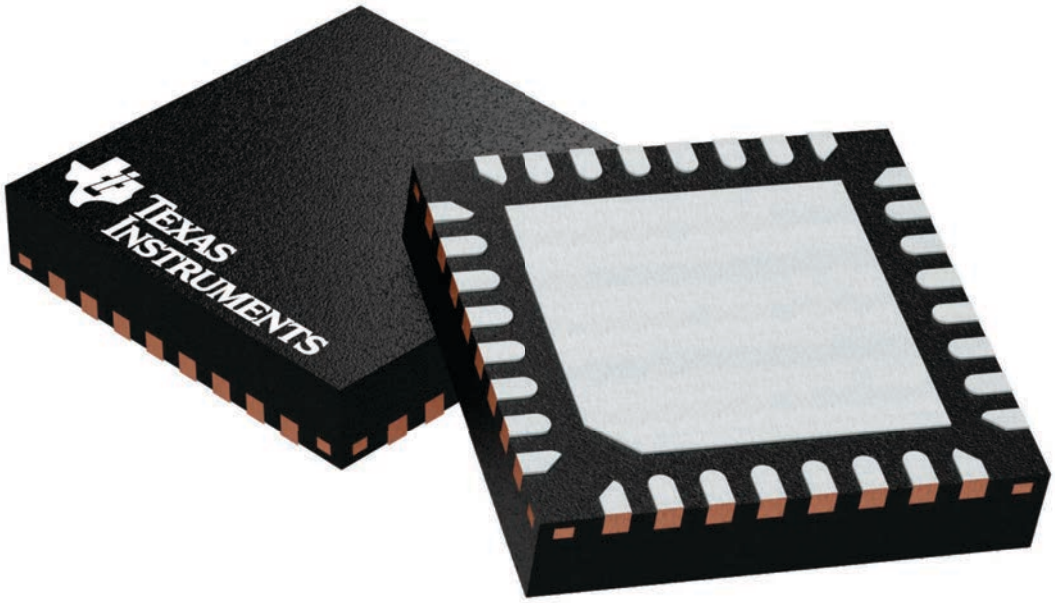
RSN 32

WQFN - 0.8 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



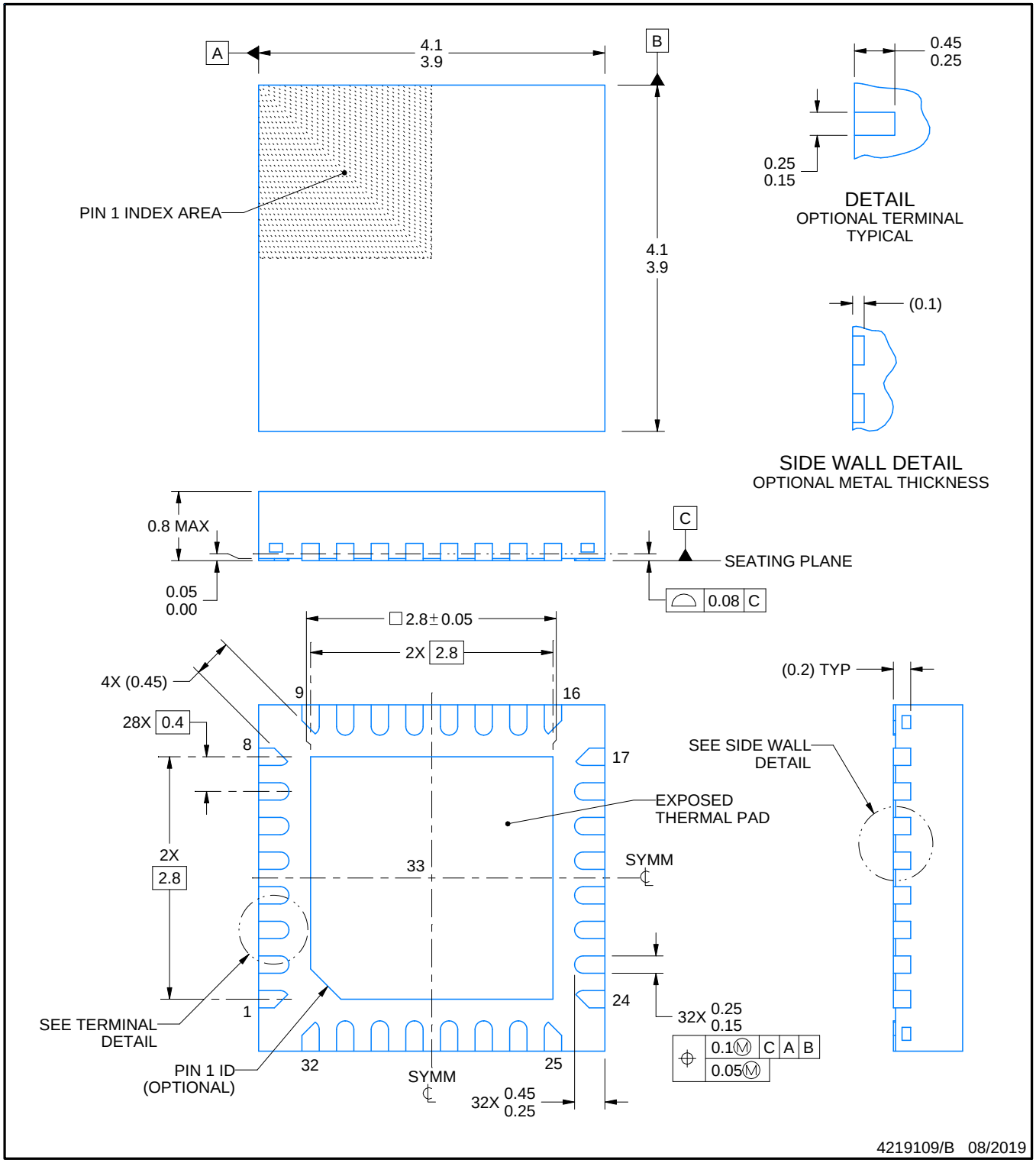
4225265/A

PACKAGE OUTLINE

RSN0032B

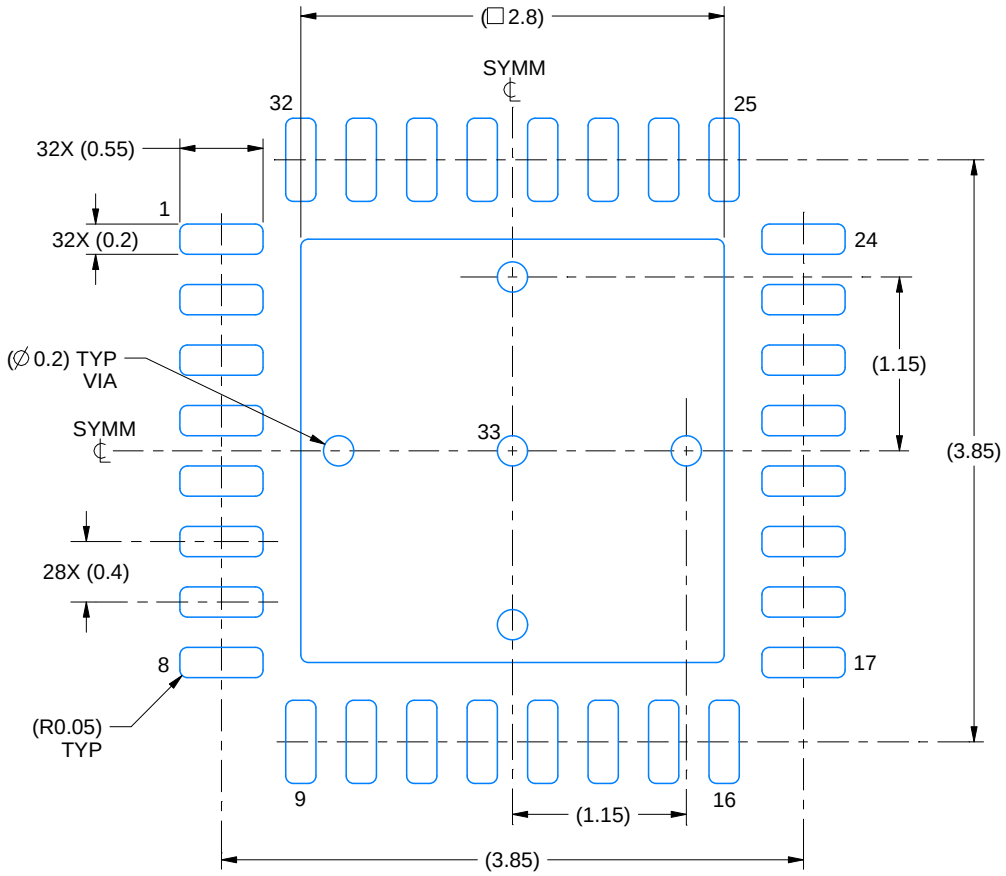
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

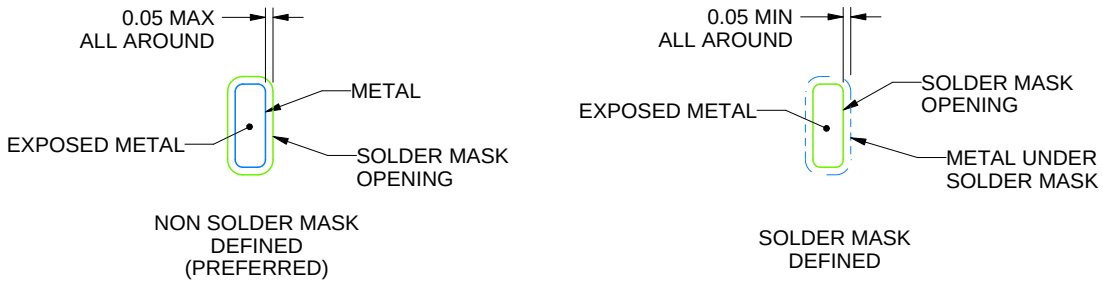


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

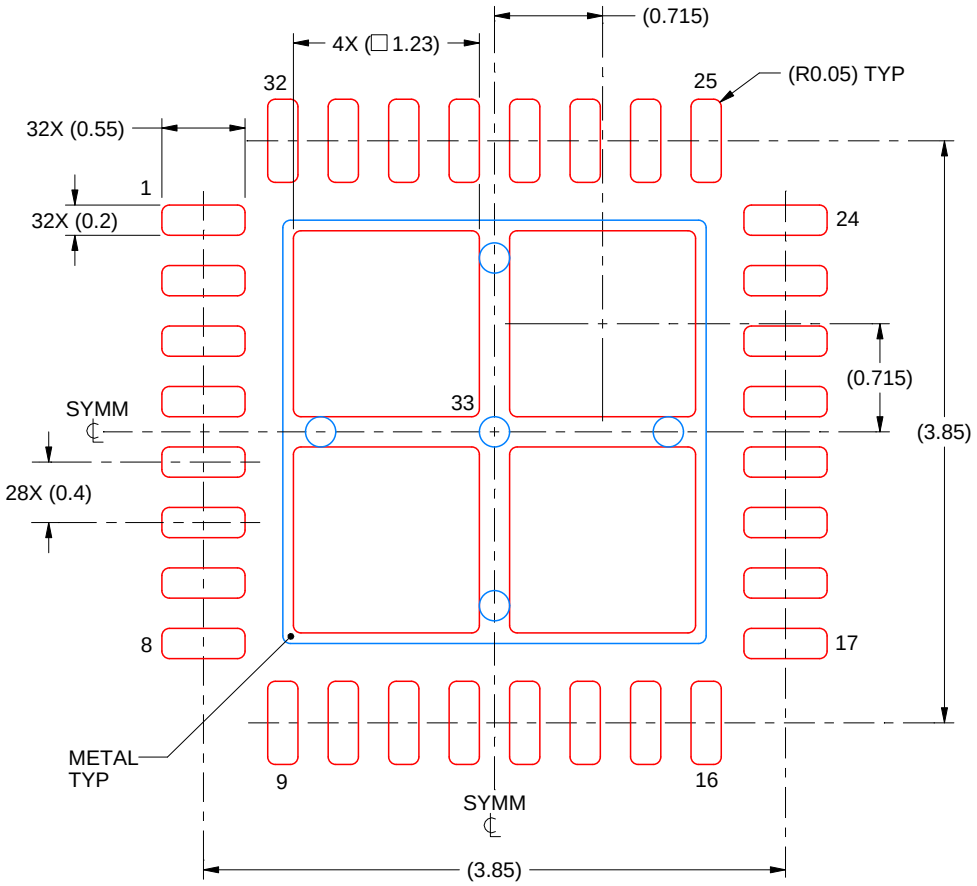


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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