# CC2652R SimpleLink™ マルチプロトコル 2.4GHz ワイヤレス MCU

## 1 特長

- マイクロコントローラ
  - 強力な 48MHz Arm® Cortex®-M4F プロセッサ
  - EEMBC CoreMark® スコア：148
  - 352kB のインシステム プログラマブル フラッシュ
  - プロトコルおよびライブラリ機能用の 256kB ROM
  - 8kB のキャッシュ SRAM (汎用 RAM としても使用可能)
  - 80kB の超低リーク SRAM。SRAM は動作の信頼性を高めるためパリティで保護。
  - 2 ピン cJTAG および JTAG デバッグ
  - OTA (Over-the-air) 更新をサポート
- 4kB の SRAM を搭載した超低消費電力センサ コントローラ
  - センサ・データのサンプリング、保存、処理
  - システム CPU から独立して動作
  - 高速ウェイクアップにより低消費電力動作を実現
- TI-RTOS、ドライバ、ブートローダ、Bluetooth® 5.2 Low Energy コントローラ、IEEE 802.15.4 MAC を ROM に配置してアプリケーション・サイズを最適化
- RoHS 準拠のパッケージ
  - 7mm × 7mm RGZ VQFN48 (31GPIO)
- ペリフェラル
  - デジタル・ペリフェラルを任意の GPIO に接続可能
  - 4× 32 ビットまたは 8× 16 ビットの汎用タイマ
  - 12 ビット ADC、200k サンプル / 秒、8 チャネル
  - 内部リファレンス DAC を搭載した 2 つのコンパレータ
    (連続時間 ×1、超低消費電力 ×1)
  - プログラマブル電流ソース
  - UART ×2
  - SSI ×2 (SPI、MICROWIRE、TI)
  - $I^2C$ および $I^2S$
  - リアルタイム・クロック (RTC)
  - AES 128 および 256 ビット暗号化アクセラレータ
  - ECC および RSA 公開鍵ハードウェア・アクセラレータ
  - SHA2 アクセラレータ (SHA-512 までのフル・スイート)
  - 真性乱数生成器 (TRNG)
  - 静電容量式センシング、最大 8 チャネル
  - 温度およびバッテリ監視を内蔵
- 外部システム
  - オンチップの降圧型 DC/DC コンバータ
- 低消費電力
  - アクティブ・モードの RX：6.9mA
  - アクティブ・モードの TX (0dBm)：7.0mA
  - アクティブ・モードの TX (+5dBm)：9.2mA
  - アクティブ・モードの MCU 48MHz (CoreMark)：3.4mA (71µA/MHz)
  - センサ・コントローラ、低消費電力モード、2MHz、無限ループ動作：30.1µA
  - センサ・コントローラ、アクティブ・モード、24MHz、無限ループ動作：808µA
  - スタンバイ：0.94µA (RTC 動作、80kB RAM および CPU を保持)
  - シャットダウン：150nA (外部イベントでウェークアップ)
- 無線部
  - Bluetooth 5.2 Low Energy およびそれ以前の LE 仕様、IEEE 802.15.4 PHY および MAC と互換性がある 2.4GHz RF トランシーバ
  - 3 線式、2 線式、1 線式 PTA の共存メカニズム
  - 優れたレシーバ感度：
    802.15.4 (2.4GHz) で -100dBm、
    Bluetooth 125kbps (LE Coded PHY) で -105dBm
  - 温度補償付きで最大 +5dBm の出力電力
  - 国際的な無線周波数規制への準拠を目標としたシステムに最適
    - EN 300 328、(欧州)
    - EN 300 440 カテゴリ 2
    - FCC CFR47 Part 15
    - ARIB STD-T66 (日本)
- ワイヤレス・プロトコル
  - Thread、Zigbee®、Bluetooth® 5.2 Low Energy、IEEE 802.15.4、IPv6 対応スマート・オブジェクト (6LoWPAN)、独自システム、SimpleLink™ TI 15.4 スタック (2.4GHz)、DMM (ダイナミック・マルチプロトコル・マネージャ) ドライバ。
- 開発ツールとソフトウェア
  - CC26x2R LaunchPad™ 開発キット
  - SimpleLink™ LOWPOWER F2 ソフトウェア開発キット (SDK)
  - SmartRF™ Studio による簡素な無線構成
  - Sensor Controller Studio により低消費電力のセンシング・アプリケーションを構築

## 2 アプリケーション

- 2400～2480MHz の ISM および SRD システム [1]
  (最小 4kHz の受信帯域幅)

[1] サポートしているプロトコル規格、変調フォーマット、データ・レートの詳細については、RF コアを参照してください。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

- ビルディング・オートメーション
  - ビルディングのセキュリティ・システム – モーション検出器、電子スマート・ロック、ドアおよび窓センサ、ガレージ・ドア・システム、ゲートウェイ
  - HVAC – サーモスタット、ワイヤレス環境センサ、HVAC システム・コントローラ、ゲートウェイ
  - 防火システム – 煙および熱感知器、火災警報制御パネル (FACP)
  - ビデオ監視 – IP ネットワーク・カメラ
  - エレベータとエスカレータ – エレベータとエスカレータのエレベータ・メイン制御パネル
- グリッド・インフラストラクチャ
  - スマート・メータ – 水道メータ、ガス・メータ、電気メータ、ヒート・コスト・アロケータ
  - グリッド通信 – 無線通信 – 長距離センサ・アプリケーション
  - その他の代替エネルギー – 環境発電
- 産業用輸送 – アセット・トラッキング
- ファクトリ・オートメーションおよび制御
- 医療用
- 電子 POS (EPOS) – 電子棚札 (ESL)
- 通信機器
  - 有線ネットワーク – 無線 LAN または Wi-Fi アクセス・ポイント、エッジ・ルータ 、小規模企業向けルータ
- パーソナル・エレクトロニクス
  - 携帯型電子機器 – RF スマート遠隔制御
  - ホーム・シアターおよびエンターテインメント – スマート・スピーカ、スマート・ディスプレイ、セット・トップ・ボックス
  - ネットワーク接続の周辺機器 – 民生用ワイヤレス・モジュール、ポインティング・デバイス、キーボードとキーパッド
  - ゲーム – 電子玩具とロボット玩具
  - ウェアラブル (非医療用) – スマート・トラッカー、スマート衣料

## 3 概要

SimpleLink™ CC2652R デバイスはマルチプロトコルの 2.4GHz ワイヤレス マイコン (MCU) です。本デバイスは Thread、Zigbee®、Bluetooth® 5.2 Low Energy、IEEE 802.15.4、IPv6 対応スマート・オブジェクト (6LoWPAN)、TI 15.4 スタック (2.4GHz) を含む独自システム、DMM (ダイナミック マルチプロトコル マネージャ) ドライバを使った同時マルチプロトコルをサポートしています。このデバイスは、ビルディングのセキュリティ・システム、HVAC、医療、有線ネットワーク、ポータブル電子機器、ホーム・シアターおよびエンターテインメント、ネットワーク接続の周辺機器市場の低消費電力の無線通信および高度なセンシングに最適化されています。このデバイスの主な特長を以下に示します

- SimpleLink™ LOWPOWER F2 ソフトウェア開発キット (SDK) で幅広いプロトコル スタックを柔軟にサポート。
- 0.94µA の小さいスタンバイ電流 (全 RAM 保持) によるバッテリ駆動時間が長いワイヤレス アプリケーション。
- 産業用温度に対応し、105℃で 11µA の最小スタンバイ電流。
- 高速ウェイクアップ機能を備えたプログラマブルな自律型超低消費電力センサ・コントローラ CPU による高度なセンシング。たとえば、このセンサ コントローラは、1µA のシステム電流で 1Hz の ADC サンプリングが可能です。
- 潜在的な放射線イベントによるデータ破損を防止する常時オン SRAM パリティを備え、低い SER (ソフト・エラー・レート) FIT (Failure-in-time、故障率) により、産業用市場向けに中断のない長い動作寿命を実現。
- 柔軟性の高い低消費電力 RF トランシーバ機能を備えた専用のソフトウェア制御無線コントローラ (Arm® Cortex®-M0) により、複数の物理層および RF 規格をサポート。
- Bluetooth® Low Energy (125kbps の LE Coded PHY で -105dBm) に対応する優れた無線感度および堅牢 (選択度、ブロッキング) 性能。

CC2652R デバイスは SimpleLink™ MCU プラットフォームの一部です。このプラットフォームは Wi-Fi®、Bluetooth Low Energy、Thread、Zigbee、Sub-1GHz MCU、ホスト MCU で構成されます。 CC2652R は、ピン互換のパッケージ オプションを備えた、32kB～704kB のフラッシュ サイズに対応するスケーラブルな製品ラインアップの一部であり、シングル コア ソフトウェア開発キット (SDK) と豊富なツール セットを備えた、共通の使いやすい開発環境を共有しています。SimpleLink™ プラットフォームを 1 回統合すれば、製品ラインアップのどのデバイスの組み合わせでも設計に追加できるので、設計要件変更の際もコードを高度に再利用できます。詳細については、SimpleLink™ MCU プラットフォームを参照してください。


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**製品情報**

| 部品番号 (1) | パッケージ | 本体サイズ (公称) |
|---|---|---|
| CC2652R1FRGZ | VQFN (48) | 7.00mm × 7.00mm |

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については、セクション 12 のパッケージ・オプションに関する付録、またはテキサス・インスツルメンツの Web サイトを参照してください。

## 4 機能ブロック図

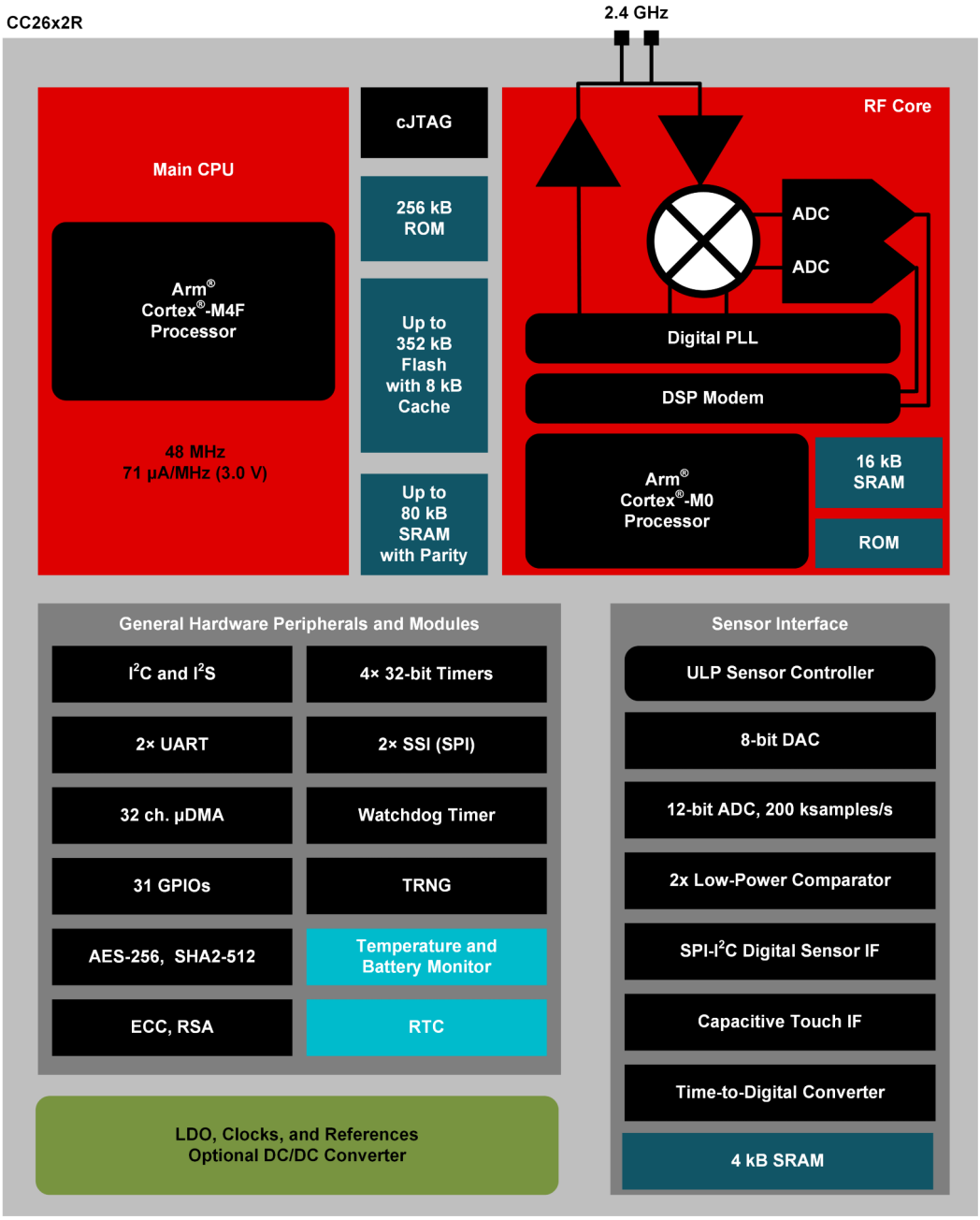



**図 4-1. CC2652R ブロック図**

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## 5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from June 12, 2023 to November 28, 2023 (from Revision I (June 2023) to Revision J (November 2023))** **Page**

- 無線消費電流 (TX 電流) を更新 ... 1
- SDK を新しい命名規則に更新し、ドキュメント全体を通して URL を更新。 ... 1
- ドキュメント全体を通して単位のフォーマットを更新 ... 1
- セクション 3 に、メモリのスケーラビリティに関する詳細を追加 ... 2
- Updated Device Comparison table ... 5
- Updated typical Tx currents in セクション 8.6, *Power Consumption - Radio Modes* ... 9
- Added footnote about DAC output impedance in セクション 8.15.2.1, *Digital-to-Analog Converter (DAC) Characteristics* ... 9
- Updated *Typical TX Current and Output Power* ... 32
- Added EnergyTrace information to セクション 9.11 ... 42


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# 6 Device Comparison

| Device | RADIO SUPPORT | | | | | | | | | | | FLASH (kB) | RAM + Cache (kB) | GPIO | PACKAGE SIZE | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Sub-1 GHz Prop. | 2.4GHz Prop. | Wireless M-Bus | mioty | Wi-SUN® | Sidewalk | *Bluetooth*® LE | ZigBee | Thread | Multiprotocol | +20 dBm PA | | | | 4 × 4 mm VQFN (24) | 4 × 4 mm VQFN (32) | 5 × 5 mm VQFN (32) | 5 × 5 mm VQFN (40) | 7 × 7 mm VQFN (48) | 8 × 8 mm VQFN (64) |
| CC1310 | √ | | √ | √ | | | | | | | | 32-128 | 16-20 + 8 | 10-30 | | √ | √ | | √ | |
| CC1311R3 | √ | | √ | √ | | | | | | | | 352 | 32 + 8 | 22-30 | | | | √ | √ | |
| CC1311P3 | √ | | √ | √ | | | | | | | √ | 352 | 32 + 8 | 26 | | | | | √ | |
| CC1312R | √ | | √ | √ | √ | | | | | | | 352 | 80 + 8 | 30 | | | | | √ | |
| CC1312R7 | √ | | √ | √ | √ | √ | | | | √ | | 704 | 144 + 8 | 30 | | | | | √ | |
| CC1314R10 | √ | | √ | √ | √ | √ | | | | √ | | 1024 | 256 + 8 | 30-46 | | | | | √ | √ |
| CC1352R | √ | √ | √ | √ | √ | | √ | √ | √ | √ | | 352 | 80 + 8 | 28 | | | | | √ | |
| CC1354R10 | √ | √ | √ | √ | √ | | √ | √ | √ | √ | | 1024 | 256 + 8 | 28-42 | | | | | √ | √ |
| CC1352P | √ | √ | √ | √ | √ | | √ | √ | √ | √ | √ | 352 | 80 + 8 | 26 | | | | | √ | |
| CC1352P7 | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | 704 | 144 + 8 | 26 | | | | | √ | |
| CC1354P10 | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | 1024 | 256 + 8 | 26-42 | | | | | √ | √ |
| CC2340R5[(1)] | | √ | | | | | √ | √ | √ | | | 512 | 36 | 12-26 | √ | | | √ | | |
| CC2640R2F | | | | | | | √ | | | | | 128 | 20 + 8 | 10-31 | | √ | √ | | √ | |
| CC2642R | | | | | | | √ | | | | | 352 | 80 + 8 | 31 | | | | | √ | |
| CC2642R-Q1 | | | | | | | √ | | | | | 352 | 80 + 8 | 31 | | | | | √ | |
| CC2651R3 | | √ | | | | | √ | √ | | | | 352 | 32 + 8 | 23-31 | | | | √ | √ | |
| CC2651P3 | | √ | | | | | √ | √ | | | √ | 352 | 32 + 8 | 22-26 | | | | √ | √ | |
| CC2652R | | √ | | | | | √ | √ | √ | √ | | 352 | 80 + 8 | 31 | | | | | √ | |
| CC2652RB | | √ | | | | | √ | √ | √ | √ | | 352 | 80 + 8 | 31 | | | | | √ | |
| CC2652R7 | | √ | | | | | √ | √ | √ | √ | | 704 | 144 + 8 | 31 | | | | | √ | |
| CC2652P | | √ | | | | | √ | √ | √ | √ | √ | 352 | 80 + 8 | 26 | | | | | √ | |
| CC2652P7 | | √ | | | | | √ | √ | √ | √ | √ | 704 | 144 + 8 | 26 | | | | | √ | |
| CC2674R10 | | √ | | | | | √ | √ | √ | √ | | 1024 | 256 + 8 | 31-45 | | | | | √ | √ |
| CC2674P10 | | √ | | | | | √ | √ | √ | √ | √ | 1024 | 256 + 8 | 26-45 | | | | | √ | √ |

(1) ZigBee and Thread support enabled by future software update

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# 7 Terminal Configuration and Functions

## 7.1 Pin Diagram – RGZ Package (Top View)

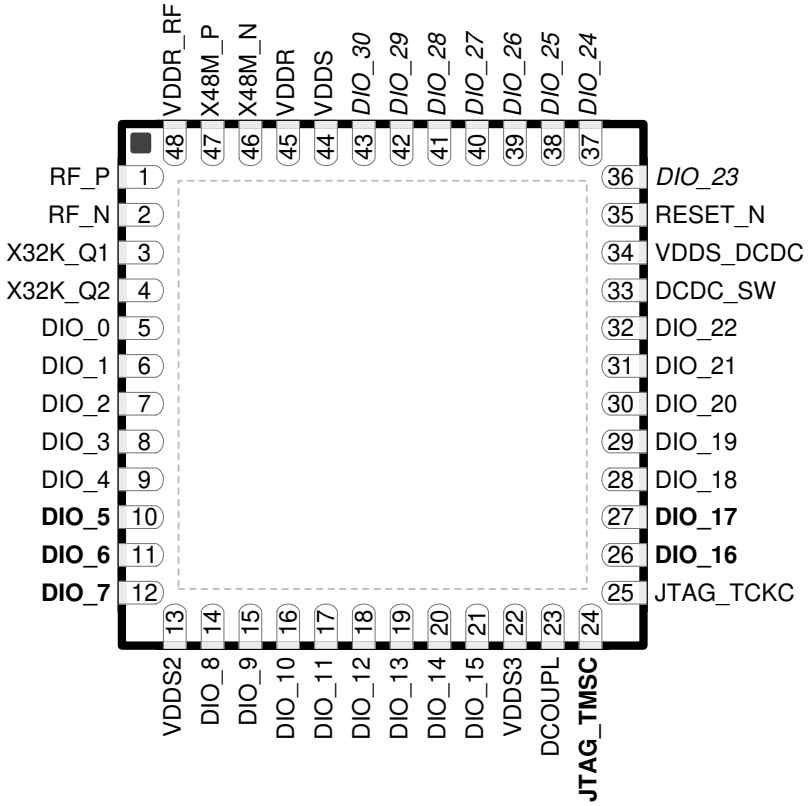



**図 7-1. RGZ (7 mm × 7 mm) Pinout, 0.5 mm Pitch (Top View)**

The following I/O pins marked in 図 7-1 in **bold** have high-drive capabilities:

- Pin 10, DIO_5
- Pin 11, DIO_6
- Pin 12, DIO_7
- Pin 24, JTAG_TMSC
- Pin 26, DIO_16
- Pin 27, DIO_17

The following I/O pins marked in 図 7-1 in *italics* have analog capabilities:

- Pin 36, DIO_23
- Pin 37, DIO_24
- Pin 38, DIO_25
- Pin 39, DIO_26
- Pin 40, DIO_27
- Pin 41, DIO_28
- Pin 42, DIO_29
- Pin 43, DIO_30


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## 7.2 Signal Descriptions – RGZ Package

表 7-1. Signal Descriptions – RGZ Package

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| DCDC_SW | 33 | — | Power | Output from internal DC/DC converter(1) |
| DCOUPL | 23 | — | Power | For decoupling of internal 1.27 V regulated digital-supply (2) |
| DIO_0 | 5 | I/O | Digital | GPIO |
| DIO_1 | 6 | I/O | Digital | GPIO |
| DIO_2 | 7 | I/O | Digital | GPIO |
| DIO_3 | 8 | I/O | Digital | GPIO |
| DIO_4 | 9 | I/O | Digital | GPIO |
| DIO_5 | 10 | I/O | Digital | GPIO, high-drive capability |
| DIO_6 | 11 | I/O | Digital | GPIO, high-drive capability |
| DIO_7 | 12 | I/O | Digital | GPIO, high-drive capability |
| DIO_8 | 14 | I/O | Digital | GPIO |
| DIO_9 | 15 | I/O | Digital | GPIO |
| DIO_10 | 16 | I/O | Digital | GPIO |
| DIO_11 | 17 | I/O | Digital | GPIO |
| DIO_12 | 18 | I/O | Digital | GPIO |
| DIO_13 | 19 | I/O | Digital | GPIO |
| DIO_14 | 20 | I/O | Digital | GPIO |
| DIO_15 | 21 | I/O | Digital | GPIO |
| DIO_16 | 26 | I/O | Digital | GPIO, JTAG_TDO, high-drive capability |
| DIO_17 | 27 | I/O | Digital | GPIO, JTAG_TDI, high-drive capability |
| DIO_18 | 28 | I/O | Digital | GPIO |
| DIO_19 | 29 | I/O | Digital | GPIO |
| DIO_20 | 30 | I/O | Digital | GPIO |
| DIO_21 | 31 | I/O | Digital | GPIO |
| DIO_22 | 32 | I/O | Digital | GPIO |
| DIO_23 | 36 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_24 | 37 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_25 | 38 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_26 | 39 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_27 | 40 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_28 | 41 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_29 | 42 | I/O | Digital or Analog | GPIO, analog capability |
| DIO_30 | 43 | I/O | Digital or Analog | GPIO, analog capability |
| EGP | — | — | GND | Ground – exposed ground pad(3) |
| JTAG_TMSC | 24 | I/O | Digital | JTAG TMSC, high-drive capability |
| JTAG_TCKC | 25 | I | Digital | JTAG TCKC |
| RESET_N | 35 | I | Digital | Reset, active low. No internal pullup resistor |
| RF_P | 1 | — | RF | Positive RF input signal to LNA during RX<br>Positive RF output signal from PA during TX |
| RF_N | 2 | — | RF | Negative RF input signal to LNA during RX<br>Negative RF output signal from PA during TX |
| VDDR | 45 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (4) (6) |

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**表 7-1. Signal Descriptions – RGZ Package (続き)**

| PIN | | I/O | TYPE | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| VDDR_RF | 48 | — | Power | Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (5) (6) |
| VDDS | 44 | — | Power | 1.8 V to 3.8 V main chip supply(1) |
| VDDS2 | 13 | — | Power | 1.8 V to 3.8 V DIO supply(1) |
| VDDS3 | 22 | — | Power | 1.8 V to 3.8 V DIO supply(1) |
| VDDS_DCDC | 34 | — | Power | 1.8 V to 3.8 V DC/DC converter supply |
| X48M_N | 46 | — | Analog | 48 MHz crystal oscillator pin 1 |
| X48M_P | 47 | — | Analog | 48 MHz crystal oscillator pin 2 |
| X32K_Q1 | 3 | — | Analog | 32 kHz crystal oscillator pin 1 |
| X32K_Q2 | 4 | — | Analog | 32 kHz crystal oscillator pin 2 |

(1) For more details, see technical reference manual listed in セクション 11.2.
(2) Do not supply external circuitry from this pin.
(3) EGP is the only ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(4) If internal DC/DC converter is not used, this pin is supplied internally from the main LDO.
(5) If internal DC/DC converter is not used, this pin must be connected to VDDR for supply from the main LDO.
(6) Output from internal DC/DC and LDO is trimmed to 1.68 V.

## 7.3 Connections for Unused Pins and Modules

**表 7-2. Connections for Unused Pins – RGZ Package**

| FUNCTION | SIGNAL NAME | PIN NUMBER | ACCEPTABLE PRACTICE(1) | PREFERRED PRACTICE(1) |
|---|---|---|---|---|
| GPIO | DIO_n | 5–12<br>14–21<br>26–32<br>36–43 | NC or GND | NC |
| 32.768 kHz crystal | X32K_Q1 | 3 | NC or GND | NC |
| | X32K_Q2 | 4 | | |
| DC/DC converter(2) | DCDC_SW | 33 | NC | NC |
| | VDDS_DCDC | 34 | VDDS | VDDS |

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC_SW and VDDR can be removed. VDDR and VDDR_RF must still be connected and the 22 µF DCDC capacitor must be kept on the VDDR net.


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# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| VDDS(3) | Supply voltage | | –0.3 | 4.1 | V |
| | Voltage on any digital pin(4) (5) | | –0.3 | VDDS + 0.3, max 4.1 | V |
| | Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2, X48M_N and X48M_P | | –0.3 | VDDR + 0.3, max 2.25 | V |
| $V_{in}$ | Voltage on ADC input | Voltage scaling enabled | –0.3 | VDDS | V |
| | | Voltage scaling disabled, internal reference | –0.3 | 1.49 | |
| | | Voltage scaling disabled, VDDS as reference | –0.3 | VDDS / 2.9 | |
| | Input level, RF pins | | | 5 | dBm |
| $T_{stg}$ | Storage temperature | | –40 | 150 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.
(5) Injection current is not supported on any GPIO pin

## 8.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | All pins | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2) | All pins | ±500 | V |

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Operating junction temperature(2) | –40 | 105 | °C |
| Operating supply voltage (VDDS) | 1.8 | 3.8 | V |
| Rising supply voltage slew rate | 0 | 100 | mV/µs |
| Falling supply voltage slew rate(1) | 0 | 20 | mV/µs |

(1) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 22 µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(2) For thermal resistance characteristics refer to Thermal Resistance Characteristics. For application considerations, refer to Junction Temperature.

## 8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDDS Power-on-Reset (POR) threshold | | | 1.1 - 1.55 | | V |
| VDDS Brown-out Detector (BOD) (1) | Rising threshold | | 1.77 | | V |
| VDDS Brown-out Detector (BOD), before initial boot (2) | Rising threshold | | 1.70 | | V |
| VDDS Brown-out Detector (BOD) (1) | Falling threshold | | 1.75 | | V |

(1) For boost mode (VDDR =1.95 V), TI drivers software initialization will trim VDDS BOD limits to maximum (approximately 2.0 V)
(2) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

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## 8.5 Power Consumption - Power Modes

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V with DC/DC enabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Core Current Consumption** | | | | | | |
| $I_{core}$ | Reset and Shutdown | Reset. RESET_N pin asserted or VDDS below power-on-reset threshold | | 150 | | nA |
| | | Shutdown. No clocks running, no retention | | 150 | | |
| | Standby without cache retention | RTC running, CPU, 80 kB RAM and (partial) register retention. RCOSC_LF | | 0.94 | | µA |
| | | RTC running, CPU, 80 kB RAM and (partial) register retention XOSC_LF | | 1.09 | | µA |
| | Standby with cache retention | RTC running, CPU, 80 kB RAM and (partial) register retention. RCOSC_LF | | 3.2 | | µA |
| | | RTC running, CPU, 80 kB RAM and (partial) register retention. XOSC_LF | | 3.3 | | µA |
| | Idle | Supply Systems and RAM powered RCOSC_HF | | 675 | | µA |
| | Active | MCU running CoreMark at 48 MHz RCOSC_HF | | 3.39 | | mA |
| **Peripheral Current Consumption,** (1), (2) | | | | | | |
| $I_{peri}$ | Peripheral power domain | Delta current with domain enabled | | 97.7 | | µA |
| | Serial power domain | Delta current with domain enabled | | 7.2 | | |
| | RF Core | Delta current with power domain enabled, clock enabled, RF core idle | | 210.9 | | |
| | µDMA | Delta current with clock enabled, module is idle | | 63.9 | | |
| | Timers | Delta current with clock enabled, module is idle(5) | | 81.0 | | |
| | I2C | Delta current with clock enabled, module is idle | | 10.1 | | |
| | I2S | Delta current with clock enabled, module is idle | | 26.3 | | |
| | SSI | Delta current with clock enabled, module is idle | | 82.9 | | |
| | UART | Delta current with clock enabled, module is idle(3) | | 167.5 | | |
| | CRYPTO (AES) | Delta current with clock enabled, module is idle(4) | | 25.6 | | |
| | PKA | Delta current with clock enabled, module is idle | | 84.7 | | |
| | TRNG | Delta current with clock enabled, module is idle | | 35.6 | | |
| **Sensor Controller Engine Consumption** | | | | | | |
| $I_{SCE}$ | Active mode | 24 MHz, infinite loop | | 808.5 | | µA |
| | Low-power mode | 2 MHz, infinite loop | | 30.1 | | |

(1) Adds to core current $I_{core}$ for each peripheral unit activated.
(2) $I_{peri}$ is not supported in Standby or Shutdown modes.
(3) Only one UART running
(4) Only one SSI running
(5) Only one GPTimer running


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## 8.6 Power Consumption - Radio Modes

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V with DC/DC enabled unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Radio receive current | 2440 MHz | | 6.9 | | mA |
| | Radio transmit current 2.4 GHz PA (BLE) | 0 dBm output power setting 2440 MHz | | 7.0 | | mA |
| | | +5 dBm output power setting 2440 MHz | | 9.2 | | mA |

## 8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and $V_{DDS}$ = 3.0 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Flash sector size | | | 8 | | KB |
| Supported flash erase cycles before failure, full bank(1) (5) | | 30 | | | k Cycles |
| Supported flash erase cycles before failure, single sector(2) | | 60 | | | k Cycles |
| Maximum number of write operations per row before sector erase(3) | | | | 83 | Write Operations |
| Flash retention | 105 °C | 11.4 | | | Years at 105 °C |
| Flash sector erase current | Average delta current | | 10.7 | | mA |
| Flash sector erase time(4) | Zero cycles | | 10 | | ms |
| Flash write current | Average delta current, 4 bytes at a time | | 6.2 | | mA |
| Flash write time(4) | 4 bytes at a time | | 21.6 | | µs |

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

## 8.8 Thermal Resistance Characteristics

| THERMAL METRIC(1) | | PACKAGE: RGZ (VQFN) 48 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 23.4 | °C/W(2) |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 13.3 | °C/W(2) |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 8.0 | °C/W(2) |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W(2) |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 7.9 | °C/W(2) |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.7 | °C/W(2) |

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
(2) °C/W = degrees Celsius per watt.

## 8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency bands | 2360 | | 2500 | MHz |

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## 8.10 Bluetooth Low Energy - Receive (RX)

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **125 kbps (LE Coded)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | –105 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | >5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37 byte packets) | | > (–320 / 240) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255 byte packets) | | > (–125 / 100) | | ppm |
| Co-channel rejection(1) | Wanted signal at –79 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –1.5 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 8 / 4.5(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = $10^{-3}$ | | 44 / 37 (2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 46 / 44(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 44 / 46(2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = $10^{-3}$ | | 48 / 44(2) | | dB |
| Selectivity, ±7 MHz | Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = $10^{-3}$ | | 51 / 45(2) | | dB |
| Selectivity, Image frequency(1) | Wanted signal at –79 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 37 | | dB |
| Selectivity, Image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4.5 / 44 (2) | | dB |
| **500 kbps (LE Coded)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | –100 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–300 / 300) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37 byte packets) | | > (–450 / 450) | | ppm |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (255 byte packets) | | > (–150/ 175) | | ppm |
| Co-channel rejection(1) | Wanted signal at –72 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –3.5 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 8 / 4(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = $10^{-3}$ | | 43 / 35 (2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 46 / 46(2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 45 / 47(2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –72 dBm, modulated interferer at ≥ ±6 MHz, BER = $10^{-3}$ | | 46 / 45(2) | | dB |
| Selectivity, ±7 MHz | Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = $10^{-3}$ | | 49 / 45(2) | | dB |
| Selectivity, Image frequency(1) | Wanted signal at –72 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 35 | | dB |


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## 8.10 Bluetooth Low Energy - Receive (RX) (続き)

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Selectivity, Image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4 / 46(2) | | dB |
| **1 Mbps (LE 1M)** | | | | | |
| Receiver sensitivity | Differential mode. BER = $10^{-3}$ | | –97 | | dBm |
| Receiver saturation | Differential mode. BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–350 / 350) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37 byte packets) | | > (–650 / 750) | | ppm |
| Co-channel rejection(1) | Wanted signal at –67 dBm, modulated interferer in channel, BER = $10^{-3}$ | | –6 | | dB |
| Selectivity, ±1 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = $10^{-3}$ | | 7 / 4(2) | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = $10^{-3}$ | | 39 / 33(2) | | dB |
| Selectivity, ±3 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = $10^{-3}$ | | 36 / 40 (2) | | dB |
| Selectivity, ±4 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 36 / 45(2) | | dB |
| Selectivity, ±5 MHz or more(1) | Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = $10^{-3}$ | | 40 | | dB |
| Selectivity, image frequency(1) | Wanted signal at –67 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 33 | | dB |
| Selectivity, image frequency ±1 MHz(1) | Note that Image frequency + 1 MHz is the Co- channel – 1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = $10^{-3}$ | | 4 / 41(2) | | dB |
| Out-of-band blocking(3) | 30 MHz to 2000 MHz | | –10 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | –18 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | –12 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | –2 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level | | –42 | | dBm |
| Spurious emissions, 30 to 1000 MHz(4) | Measurement in a 50 Ω single-ended load. | | < –59 | | dBm |
| Spurious emissions, 1 to 12.75 GHz(4) | Measurement in a 50 Ω single-ended load. | | < –47 | | dBm |
| RSSI dynamic range | | | 70 | | dB |
| RSSI accuracy | | | ±4 | | dB |
| **2 Mbps (LE 2M)** | | | | | |
| Receiver sensitivity | Differential mode. Measured at SMA connector, BER = $10^{-3}$ | | –91 | | dBm |
| Receiver saturation | Differential mode. Measured at SMA connector, BER = $10^{-3}$ | | > 5 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > (–500 / 500) | | kHz |
| Data rate error tolerance | Difference between incoming data rate and the internally generated data rate (37 byte packets) | | > (–700 / 750) | | ppm |
| Co-channel rejection(1) | Wanted signal at –67 dBm, modulated interferer in channel,BER = $10^{-3}$ | | –7 | | dB |
| Selectivity, ±2 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = $10^{-3}$ | | 8 / 4(2) | | dB |

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## 8.10 Bluetooth Low Energy - Receive (RX) (続き)

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Selectivity, ±4 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = $10^{-3}$ | | 36 / 34 (2) | | dB |
| Selectivity, ±6 MHz(1) | Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = $10^{-3}$ | | 37 / 36(2) | | dB |
| Selectivity, image frequency(1) | Wanted signal at –67 dBm, modulated interferer at image frequency, BER = $10^{-3}$ | | 4 | | dB |
| Selectivity, image frequency ±2 MHz(1) | Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = $10^{-3}$ | | –7 / 36(2) | | dB |
| Out-of-band blocking(3) | 30 MHz to 2000 MHz | | –16 | | dBm |
| Out-of-band blocking | 2003 MHz to 2399 MHz | | –21 | | dBm |
| Out-of-band blocking | 2484 MHz to 2997 MHz | | –15 | | dBm |
| Out-of-band blocking | 3000 MHz to 12.75 GHz | | –12 | | dBm |
| Intermodulation | Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level | | –38 | | dBm |

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at $F_{wanted}$ / 2, per Bluetooth Specification
(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)


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## 8.11 Bluetooth Low Energy - Transmit (TX)

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| Max output power | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 5 | | dBm |
| Output power programmable range | Differential mode, delivered to a single-ended 50 Ω load through a balun | | | 26 | | dB |
| **Spurious emissions and harmonics** | | | | | | |
| Spurious emissions (1) | f < 1 GHz, outside restricted bands | +5 dBm setting | | < –36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < –54 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < –55 | | dBm |
| | f > 1 GHz, including harmonics | | | < –42 | | dBm |
| Harmonics (1) | Second harmonic | | | < –42 | | dBm |
| | Third harmonic | | | < –42 | | dBm |

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

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## 8.12 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **General Parameters** | | | | | |
| Receiver sensitivity | PER = 1% | | –99 | | dBm |
| Receiver saturation | PER = 1% | | > 5 | | dBm |
| Adjacent channel rejection | Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1% | | 36 | | dB |
| Alternate channel rejection | Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1% | | 57 | | dB |
| Channel rejection, ±15 MHz or more | Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1% | | 59 | | dB |
| Blocking and desensitization, 5 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 57 | | dB |
| Blocking and desensitization, 10 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 62 | | dB |
| Blocking and desensitization, 20 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 62 | | dB |
| Blocking and desensitization, 50 MHz from upper band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Blocking and desensitization, –5 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 59 | | dB |
| Blocking and desensitization, –10 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 59 | | dB |
| Blocking and desensitization, –20 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 63 | | dB |
| Blocking and desensitization, –50 MHz from lower band edge | Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1% | | 65 | | dB |
| Spurious emissions, 30 MHz to 1000 MHz(1) | Measurement in a 50 Ω single-ended load | | –66 | | dBm |
| Spurious emissions, 1 GHz to 12.75 GHz(1) | Measurement in a 50 Ω single-ended load | | –53 | | dBm |
| Frequency error tolerance | Difference between the incoming carrier frequency and the internally generated carrier frequency | | > 350 | | ppm |
| Symbol rate error tolerance | Difference between incoming symbol rate and the internally generated symbol rate | | > 1000 | | ppm |
| RSSI dynamic range | | | 95 | | dB |
| RSSI accuracy | | | ±4 | | dB |

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)


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## 8.13 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

When measured on the CC26x2REM-7ID reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, $f_{RF}$= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| Max output power | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 5 | | dBm |
| Output power programmable range | Differential mode, delivered to a single-ended 50-Ω load through a balun | | | 26 | | dB |
| **Spurious emissions and harmonics** | | | | | | |
| Spurious emissions (1) (2) | f < 1 GHz, outside restricted bands | +5 dBm setting | | < -36 | | dBm |
| | f < 1 GHz, restricted bands ETSI | | | < -47 | | dBm |
| | f < 1 GHz, restricted bands FCC | | | < -55 | | dBm |
| | f > 1 GHz, including harmonics | | | < –42 | | dBm |
| Harmonics (1) | Second harmonic | | | < -42 | | dBm |
| | Third harmonic | | | < -42 | | dBm |
| **IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)** | | | | | | |
| Error vector magnitude | +5 dBm setting | | | 2 | | % |

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).
(2) To ensure margins for passing FCC band edge requirements at 2483.5 MHz, a lower than maximum output-power setting or less than 100% duty cycle may be used when operating at 2480 MHz.

## 8.14 Timing and Switching Characteristics

### 8.14.1 Reset Timing

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| RESET_N low duration | 1 | | | µs |

### 8.14.2 Wakeup Timing

Measured over operating free-air temperature with $V_{DDS}$ = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| MCU, Reset to Active(1) | | | 850 - 4000 | | µs |
| MCU, Shutdown to Active(1) | | | 850 - 4000 | | µs |
| MCU, Standby to Active | | | 160 | | µs |
| MCU, Active to Standby | | | 36 | | µs |
| MCU, Idle to Active | | | 14 | | µs |

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again. The wake up time increases with a higher capacitor value.

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## 8.14.3 Clock Specifications

### 8.14.3.1 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.(1)

| | PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | Crystal frequency | | 48 | | MHz |
| ESR | Equivalent series resistance<br>6 pF < $C_L$ ≤ 9 pF | | 20 | 60 | Ω |
| ESR | Equivalent series resistance<br>5 pF < $C_L$ ≤ 6 pF | | | 80 | Ω |
| $L_M$ | Motional inductance, relates to the load capacitance that is used for the crystal ($C_L$ in Farads)(5) | | < 3 × $10^{-25}$ / $C_L$ $^2$ | | H |
| $C_L$ | Crystal load capacitance(4) | 5 | 7(3) | 9 | pF |
| | Start-up time(2) | | 200 | | µs |

(1) Probing or otherwise stopping the crystal while the DC/DC converter is enabled may cause permanent damage to the device.
(2) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(3) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(4) Adjustable load capacitance is integrated into the device.
(5) The crystal manufacturer's specification must satisfy this requirement for proper operation.

### 8.14.3.2 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Frequency | | 48 | | MHz |
| Uncalibrated frequency accuracy | | ±1 | | % |
| Calibrated frequency accuracy(1) | | ±0.25 | | % |
| Start-up time | | 5 | | µs |

(1) Accuracy relative to the calibration source (XOSC_HF)

### 8.14.3.3 2 MHz RC Oscillator (RCOSC_MF)

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Calibrated frequency | | 2 | | MHz |
| Start-up time | | 5 | | µs |

### 8.14.3.4 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| | Crystal frequency | | 32.768 | | kHz |
| ESR | Equivalent series resistance | | 30 | 100 | kΩ |
| $C_L$ | Crystal load capacitance | 6 | 7(1) | 12 | pF |

(1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

### 8.14.3.5 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Calibrated frequency | | 32.8 (1) | | kHz |


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### *8.14.3.5 32 kHz RC Oscillator (RCOSC_LF) (続き)*

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Temperature coefficient. | | 50 | | ppm/°C |

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

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## 8.14.4 Synchronous Serial Interface (SSI) Characteristics

### *8.14.4.1 Synchronous Serial Interface (SSI) Characteristics*

over operating free-air temperature range (unless otherwise noted)

| PARAMETER NO. | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| S1 | $t_{clk_per}$ | SSIClk cycle time | 12 | | 65024 | System Clocks (2) |
| S2(1) | $t_{clk_high}$ | SSIClk high time | | 0.5 | | $t_{clk_per}$ |
| S3(1) | $t_{clk_low}$ | SSIClk low time | | 0.5 | | $t_{clk_per}$ |

(1) Refer to SSI timing diagrams Diagram 1, Diagram 2, Diagram 3
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

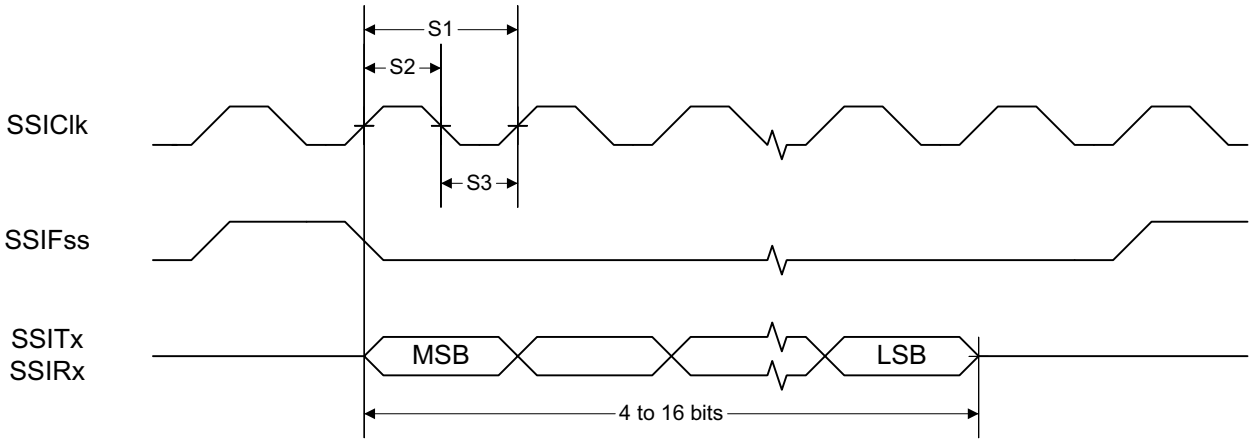



**図 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement**

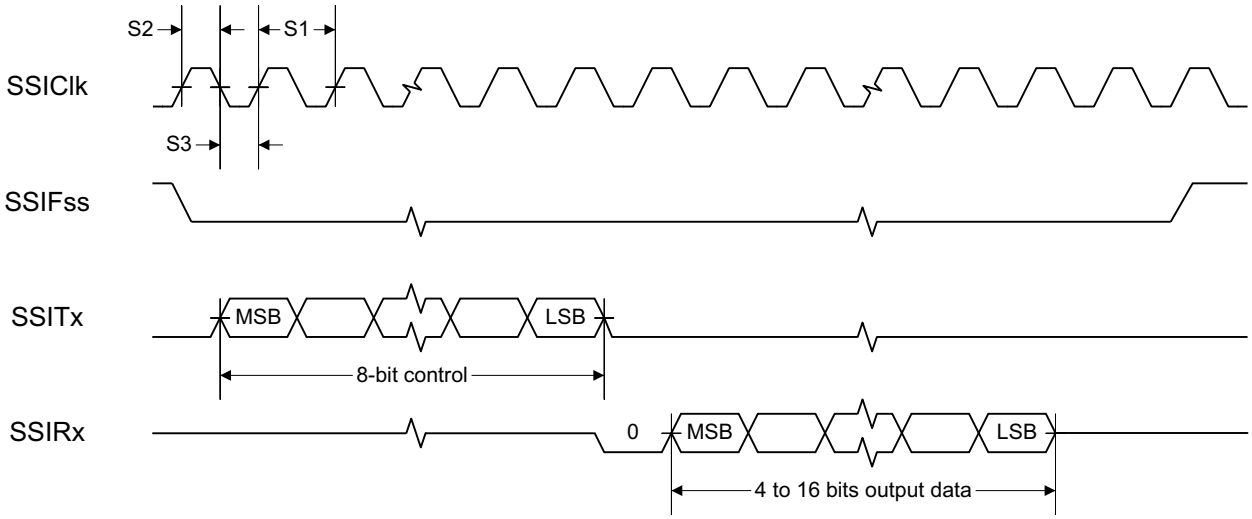



**図 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer**


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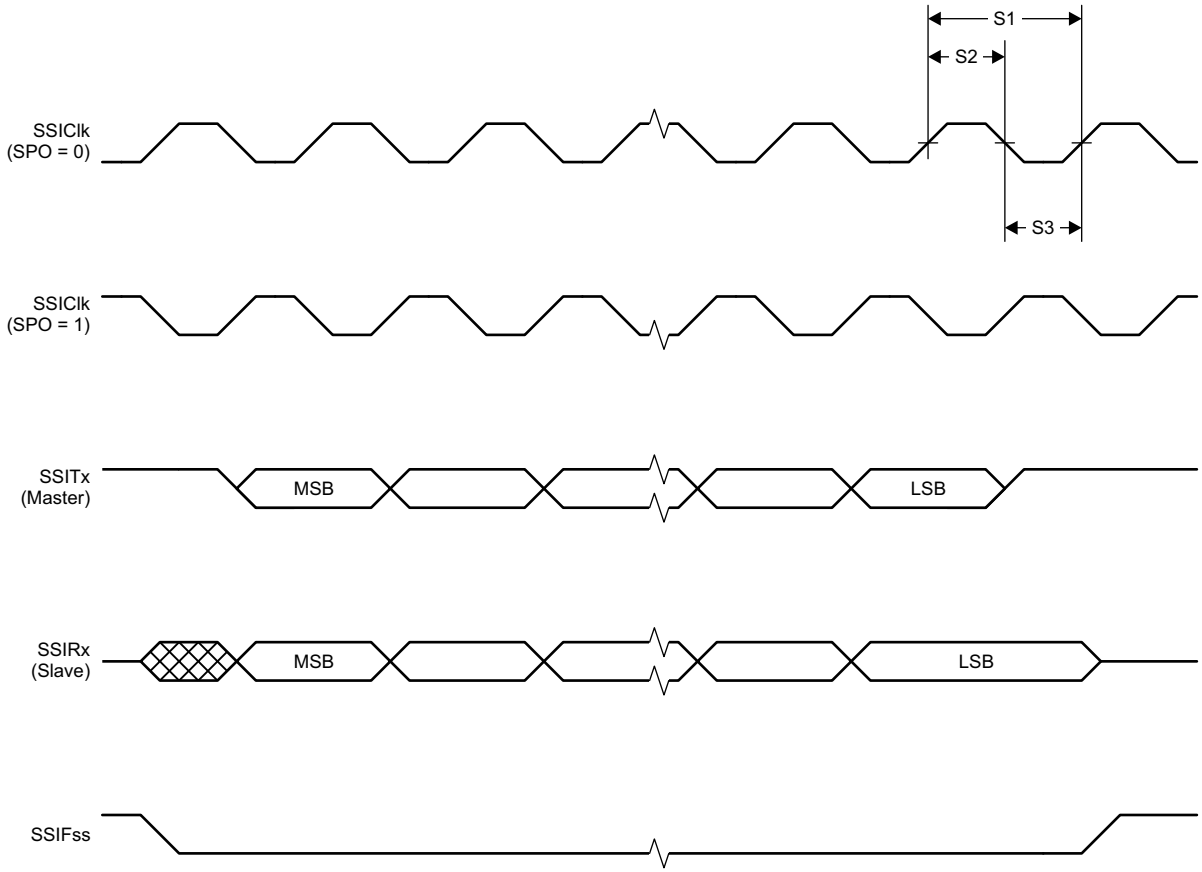



**図 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1**

## 8.14.5 UART

### *8.14.5.1 UART Characteristics*

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| UART rate | | | 3 | MBaud |

# 8.15 Peripheral Characteristics

## 8.15.1 ADC

### *8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics*

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input voltage range | | 0 | | VDDS | V |
| | Resolution | | | 12 | | Bits |
| | Sample Rate | | | | 200 | ksps |
| | Offset | Internal 4.3 V equivalent reference(2) | | –0.24 | | LSB |
| | Gain error | Internal 4.3 V equivalent reference(2) | | 7.14 | | LSB |
| DNL(4) | Differential nonlinearity | | | >–1 | | LSB |
| INL | Integral nonlinearity | | | ±4 | | LSB |
| ENOB | Effective number of bits | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 9.8 | | Bits |
| | | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled | | 9.8 | | |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 10.1 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 11.1 | | |
| | | Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 600 Hz input tone (5) | | 11.3 | | |
| | | Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 150 Hz input tone (5) | | 11.6 | | |
| THD | Total harmonic distortion | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | –65 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | –70 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | –72 | | |
| SINAD, SNDR | Signal-to-noise and distortion ratio | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 60 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 63 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 68 | | |
| SFDR | Spurious-free dynamic range | Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone | | 70 | | dB |
| | | VDDS as reference, 200 kSamples/s, 9.6 kHz input tone | | 73 | | |
| | | Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone | | 75 | | |
| | Conversion time | Serial conversion, time-to-output, 24 MHz clock | | 50 | | Clock Cycles |
| | Current consumption | Internal 4.3 V equivalent reference(2) | | 0.42 | | mA |
| | Current consumption | VDDS as reference | | 0.6 | | mA |
| | Reference voltage | Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1 | | 4.3(2) (3) | | V |
| | Reference voltage | Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: $V_{ref}$ = 4.3 V × 1408 / 4095 | | 1.48 | | V |
| | Reference voltage | VDDS as reference, input voltage scaling enabled | | VDDS | | V |
| | Reference voltage | VDDS as reference, input voltage scaling disabled | | VDDS / 2.82(3) | | V |


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### 8.15.1.1 Analog-to-Digital Converter (ADC) Characteristics (続き)

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input impedance | 200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time | | >1 | | MΩ |

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings (see セクション 8.1) at all times
(4) No missing codes
(5) ADC_output = Σ($4^n$ samples ) >> n, n = desired extra bits

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## 8.15.2 DAC

### *8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics*

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **General Parameters** | | | | | | |
| | Resolution | | | 8 | | Bits |
| $V_{DDS}$ | Supply voltage | Any load, any $V_{REF}$, pre-charge OFF, DAC charge-pump ON | 1.8 | | 3.8 | V |
| | | External Load[4], any $V_{REF}$, pre-charge OFF, DAC charge-pump OFF | 2.0 | | 3.8 | |
| | | Any load, $V_{REF}$ = DCOUPL, pre-charge ON | 2.6 | | 3.8 | |
| $F_{DAC}$ | Clock frequency | Buffer ON (recommended for external load) | 16 | | 250 | kHz |
| | | Buffer OFF (internal load) | 16 | | 1000 | |
| | Voltage output settling time | $V_{REF}$ = VDDS, buffer OFF, internal load | | 13 | | 1 / $F_{DAC}$ |
| | | $V_{REF}$ = VDDS, buffer ON, external capacitive load = 20 pF[3] | | 13.8 | | |
| | External capacitive load | | | 20 | 200 | pF |
| | External resistive load | | 10 | | | MΩ |
| | Short circuit current | | | | 400 | µA |
| $Z_{MAX}$ | Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz [5] | VDDS = 3.8 V, DAC charge-pump OFF | | 50.8 | | kΩ |
| | | VDDS = 3.0 V, DAC charge-pump ON | | 51.7 | | |
| | | VDDS = 3.0 V, DAC charge-pump OFF | | 53.2 | | |
| | | VDDS = 2.0 V, DAC charge-pump ON | | 48.7 | | |
| | | VDDS = 2.0 V, DAC charge-pump OFF | | 70.2 | | |
| | | VDDS = 1.8 V, DAC charge-pump ON | | 46.3 | | |
| | | VDDS = 1.8 V, DAC charge-pump OFF | | 88.9 | | |
| **Internal Load - Continuous Time Comparator / Low Power Clocked Comparator** | | | | | | |
| DNL | Differential nonlinearity | $V_{REF}$ = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC}$ = 250 kHz | | ±1 | | LSB[1] |
| | Differential nonlinearity | $V_{REF}$ = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator $F_{DAC}$ = 16 kHz | | ±1.2 | | |
| | Offset error[2] Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V | | ±0.64 | | LSB[1] |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±0.81 | | |
| | | $V_{REF}$ = VDDS = 1.8 V | | ±1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.43 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±2.88 | | |
| | | $V_{REF}$ = ADCREF | | ±2.37 | | |
| | Offset error[2] Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS= 3.8 V | | ±0.78 | | LSB[1] |
| | | $V_{REF}$ = VDDS = 3.0 V | | ±0.77 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±3.46 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.44 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±4.70 | | |
| | | $V_{REF}$ = ADCREF | | ±4.11 | | |
| | Max code output voltage variation[2] Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V | | ±1.53 | | LSB[1] |
| | | $V_{REF}$ = VDDS = 3.0 V | | ±1.71 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±2.10 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±6.00 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±3.85 | | |
| | | $V_{REF}$ = ADCREF | | ±5.84 | | |


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### 8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (続き)

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Max code output voltage variation[2] Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS= 3.8 V | | ±2.92 | | LSB[1] |
| | | $V_{REF}$ =VDDS= 3.0 V | | ±3.06 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±3.91 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±7.84 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±4.06 | | |
| | | $V_{REF}$ = ADCREF | | ±6.94 | | |
| | Output voltage range[2] Load = Continuous Time Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS = 3.8 V, code 255 | | 3.62 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.86 | | |
| | | $V_{REF}$ = VDDS= 1.8 V, code 1 | | 0.01 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.71 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.41 | | |
| | Output voltage range[2] Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS= 3.8 V, code 255 | | 3.61 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.85 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 1 | | 0.01 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.71 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.21 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.01 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.41 | | |
| **External Load (Keysight 34401A Multimeter)** | | | | | | |
| INL | Integral nonlinearity | $V_{REF}$ = VDDS, $F_{DAC}$ = 250 kHz | | ±1 | | LSB[1] |
| | | $V_{REF}$ = DCOUPL, $F_{DAC}$ = 250 kHz | | ±1 | | |
| | | $V_{REF}$ = ADCREF, $F_{DAC}$ = 250 kHz | | ±1 | | |
| DNL | Differential nonlinearity | $V_{REF}$ = VDDS, $F_{DAC}$ = 250 kHz | | ±1 | | LSB[1] |
| | Offset error | $V_{REF}$ = VDDS= 3.8 V | | ±0.40 | | LSB[1] |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±0.50 | | |
| | | $V_{REF}$ = VDDS = 1.8 V | | ±0.75 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±1.55 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±1.30 | | |
| | | $V_{REF}$ = ADCREF | | ±1.10 | | |
| | Max code output voltage variation | $V_{REF}$ = VDDS= 3.8 V | | ±1.00 | | LSB[1] |
| | | $V_{REF}$ = VDDS= 3.0 V | | ±1.00 | | |
| | | $V_{REF}$ = VDDS= 1.8 V | | ±1.00 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON | | ±3.45 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF | | ±2.10 | | |
| | | $V_{REF}$ = ADCREF | | ±1.90 | | |

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### 8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics (続き)

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Output voltage range<br>Load = Low Power Clocked Comparator | $V_{REF}$ = VDDS = 3.8 V, code 1 | | 0.03 | | V |
| | | $V_{REF}$ = VDDS = 3.8 V, code 255 | | 3.61 | | |
| | | $V_{REF}$ = VDDS = 3.0 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS= 3.0 V, code 255 | | 2.85 | | |
| | | $V_{REF}$ = VDDS= 1.8 V, code 1 | | 0.02 | | |
| | | $V_{REF}$ = VDDS = 1.8 V, code 255 | | 1.71 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 1 | | 0.02 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge OFF, code 255 | | 1.20 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 1 | | 1.27 | | |
| | | $V_{REF}$ = DCOUPL, pre-charge ON, code 255 | | 2.46 | | |
| | | $V_{REF}$ = ADCREF, code 1 | | 0.02 | | |
| | | $V_{REF}$ = ADCREF, code 255 | | 1.42 | | |

(1) 1 LSB ($V_{REF}$ 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter
(5) When using lower levels of VDDS with the charge pump OFF, care must be taken to adapt the surrounding circuit to the increase in impedance.


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## 8.15.3 Temperature and Battery Monitor

### *8.15.3.1 Temperature Sensor*

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 2 | | °C |
| Accuracy | -40 °C to 0 °C | | ±4.0 | | °C |
| Accuracy | 0 °C to 105 °C | | ±2.5 | | °C |
| Supply voltage coefficient(1) | | | 3.6 | | °C/V |

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

### *8.15.3.2 Battery Monitor*

Measured on a Texas Instruments reference design with $T_c$ = 25 °C, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 25 | | mV |
| Range | | 1.8 | | 3.8 | V |
| Integral nonlinearity (max) | | | 23 | | mV |
| Accuracy | VDDS = 3.0 V | | 22.5 | | mV |
| Offset error | | | -32 | | mV |
| Gain error | | | -1 | | % |

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## 8.15.4 Comparators

### 8.15.4.1 Low-Power Clocked Comparator

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range | | 0 | | $V_{DDS}$ | V |
| Clock frequency | | | SCLK_LF | | |
| Internal reference voltage(1) | Using internal DAC with VDDS as reference voltage, DAC code = 0 - 255 | | 0.024 - 2.865 | | V |
| Offset | Measured at $V_{DDS}$ / 2, includes error from internal DAC | | ±5 | | mV |
| Decision time | Step from –50 mV to 50 mV | | 1 | | Clock Cycle |

(1) The comparator can use an internal 8 bits DAC as its reference. The DAC output voltage range depends on the reference voltage selected. See セクション 8.15.2.1

### 8.15.4.2 Continuous Time Comparator

$T_c$ = 25°C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltage range(1) | | 0 | | $V_{DDS}$ | V |
| Offset | Measured at $V_{DDS}$ / 2 | | ±5 | | mV |
| Decision time | Step from –10 mV to 10 mV | | 0.78 | | µs |
| Current consumption | Internal reference | | 8.6 | | µA |

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

## 8.15.5 Current Source

### 8.15.5.1 Programmable Current Source

$T_c$ = 25 °C, $V_{DDS}$ = 3.0 V, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Current source programmable output range (logarithmic range) | | | 0.25 - 20 | | µA |
| Resolution | | | 0.25 | | µA |


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## 8.15.6 GPIO

### *8.15.6.1 GPIO DC Characteristics*

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **$T_A$ = 25 °C, $V_{DDS}$ = 1.8 V** | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 1.56 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.24 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 1.59 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.21 | | V |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 73 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 19 | | µA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.08 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 0.73 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.35 | | V |
| **$T_A$ = 25 °C, $V_{DDS}$ = 3.0 V** | | | | | |
| GPIO VOH at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 2.59 | | V |
| GPIO VOL at 8 mA load | IOCURR = 2, high-drive GPIOs only | | 0.42 | | V |
| GPIO VOH at 4 mA load | IOCURR = 1 | | 2.63 | | V |
| GPIO VOL at 4 mA load | IOCURR = 1 | | 0.40 | | V |
| **$T_A$ = 25 °C, $V_{DDS}$ = 3.8 V** | | | | | |
| GPIO pullup current | Input mode, pullup enabled, Vpad = 0 V | | 282 | | µA |
| GPIO pulldown current | Input mode, pulldown enabled, Vpad = VDDS | | 110 | | µA |
| GPIO low-to-high input transition, with hysteresis | IH = 1, transition voltage for input read as 0 → 1 | | 1.97 | | V |
| GPIO high-to-low input transition, with hysteresis | IH = 1, transition voltage for input read as 1 → 0 | | 1.55 | | V |
| GPIO input hysteresis | IH = 1, difference between 0 → 1 and 1 → 0 points | | 0.42 | | V |
| **$T_A$ = 25 °C** | | | | | |
| VIH | Lowest GPIO input voltage reliably interpreted as a *High* | $0.8*V_{DDS}$ | | | V |
| VIL | Highest GPIO input voltage reliably interpreted as a *Low* | | | $0.2*V_{DDS}$ | V |

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## 8.16 Typical Characteristics

All measurements in this section are done with $T_c$ = 25 °C and $V_{DDS}$ = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions* for device limits. Values exceeding these limits are for reference only.

### 8.16.1 MCU Current

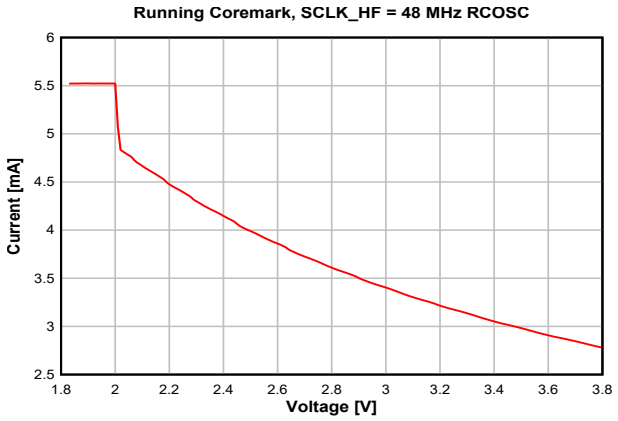



**図 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)**

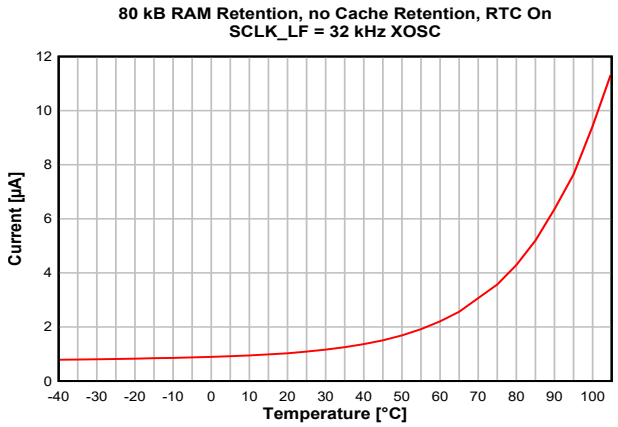



**図 8-5. Standby Mode (MCU) Current vs. Temperature**


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### 8.16.2 RX Current

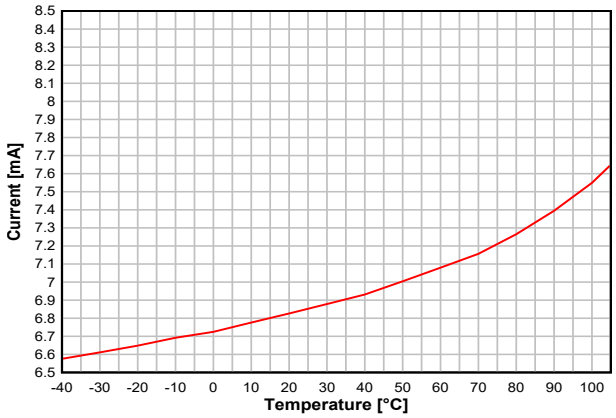



**図 8-6. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)**

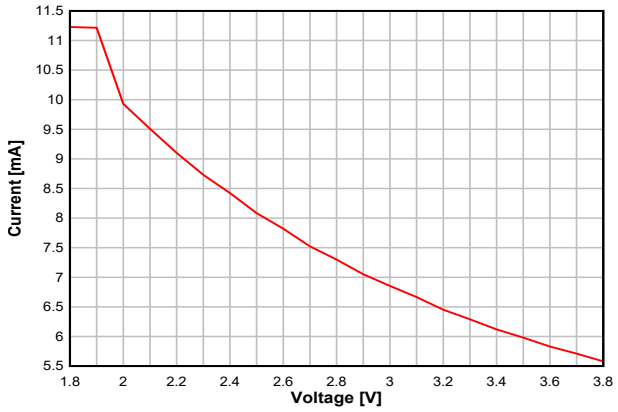



**図 8-7. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)**

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### 8.16.3 TX Current

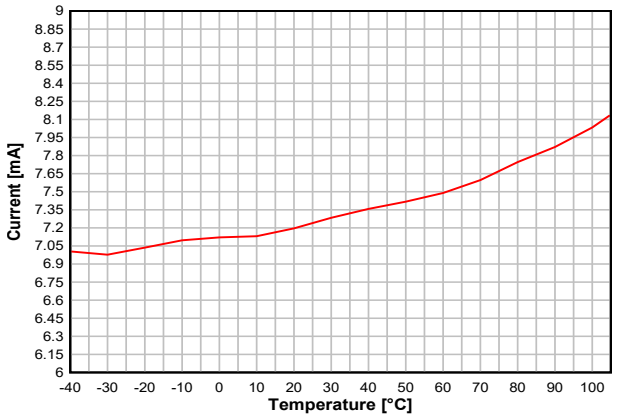



**図 8-8. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)**

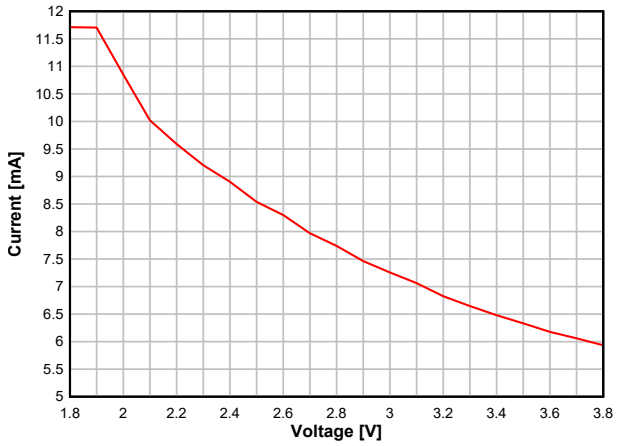



**図 8-9. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)**

shows typical TX current and output power for different output power settings.

**表 8-1. Typical TX Current and Output Power**

| CC2652R at 2.4 GHz, VDDS = 3.0 V (Measured on CC26x2REM-7ID-Q1) | | | |
|---|---|---|---|
| **txPower** | **TX Power Setting (SmartRF Studio)** | **Typical Output Power [dBm]** | **Typical Current Consumption [mA]** |
| 0x8623 | 5 | 5.0 | 9.2 |
| 0x5E1A | 4 | 4.1 | 8.6 |
| 0x4867 | 3 | 3.2 | 8.2 |
| 0x3860 | 2 | 2.0 | 7.6 |
| 0x2E5C | 1 | 1.2 | 7.3 |
| 0x2E59 | 0 | 0.3 | 7.0 |
| 0x10D9 | -5 | -5.0 | 5.9 |
| 0x0AD1 | -10 | -9.5 | 5.3 |
| 0x0ACC | -15 | -13.7 | 4.9 |
| 0x0AC8 | -20 | -18.6 | 4.6 |


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### 8.16.4 RX Performance

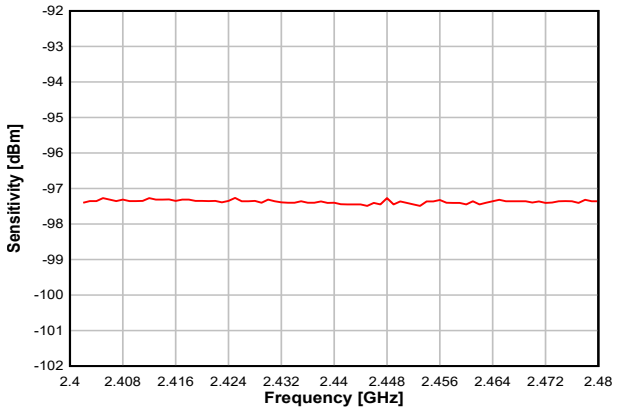



**図 8-10. Sensitivity vs. Frequency (BLE 1 Mbps, 2.44 GHz)**

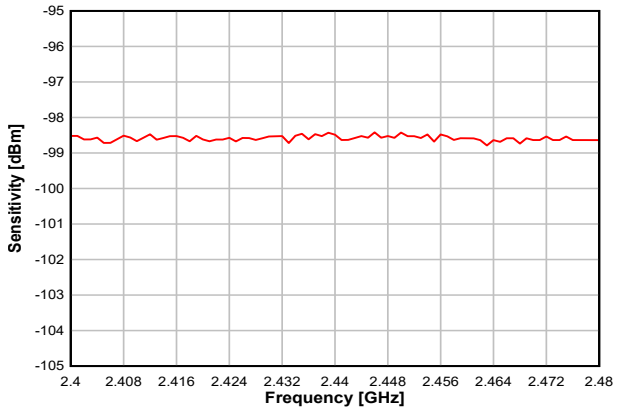



**図 8-11. Sensitivity vs. Frequency (IEEE 802.15.4-2006, 250 kbps, OQPSK DSSS 1:8, 2.44 GHz)**

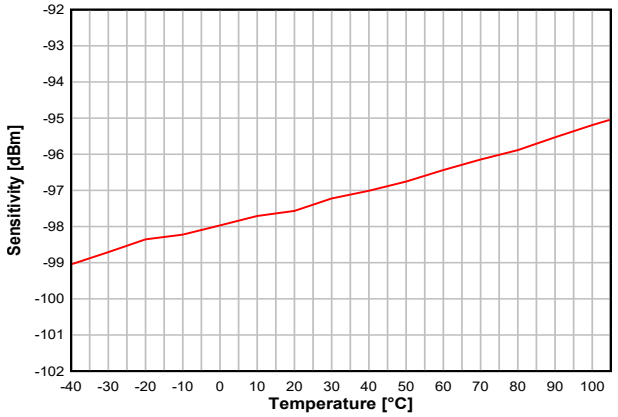



**図 8-12. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)**

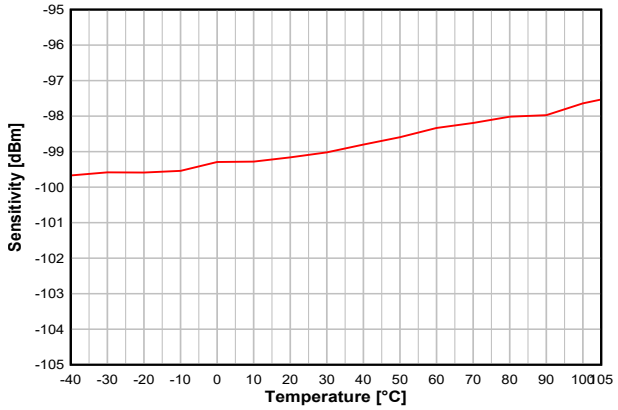



**図 8-13. Sensitivity vs. Temperature (IEEE 802.15.4-2006, 250 kbps, OQPSK DSSS 1:8, 2.44 GHz)**

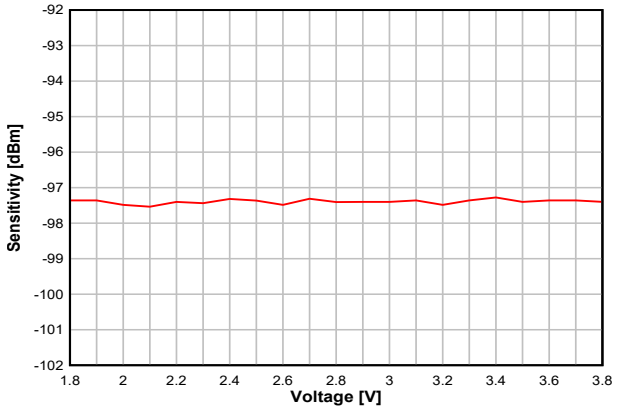



**図 8-14. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)**

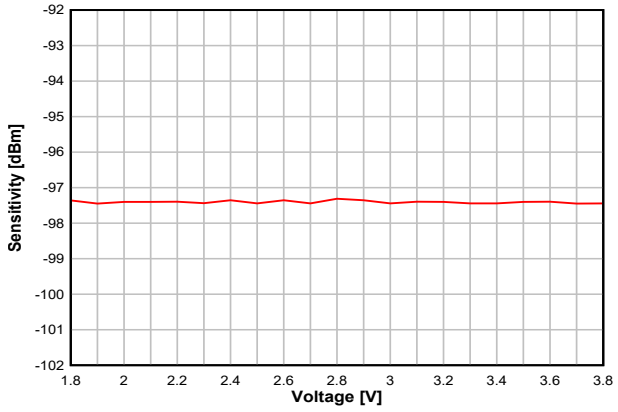



**図 8-15. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)**

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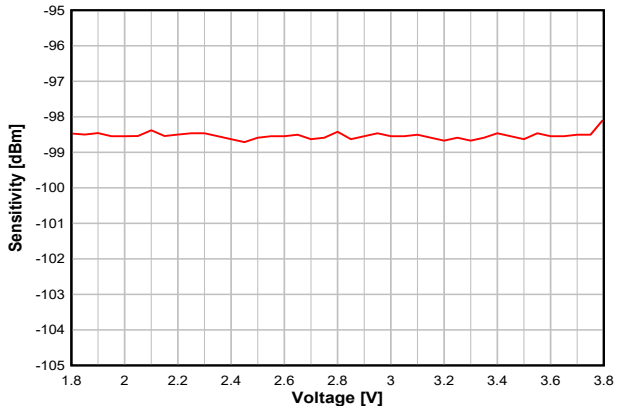



**図 8-16. Sensitivity vs. Supply Voltage (VDDS) (IEEE 802.15.4-2006, 250 kbps, OQPSK DSSS 1:8, 2.44 GHz)**


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### 8.16.5 TX Performance

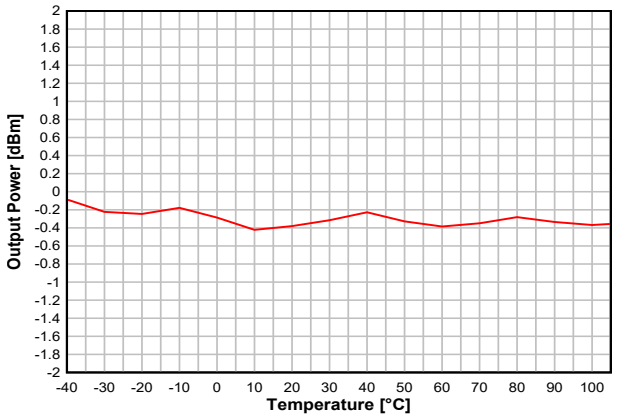



**図 8-17. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)**

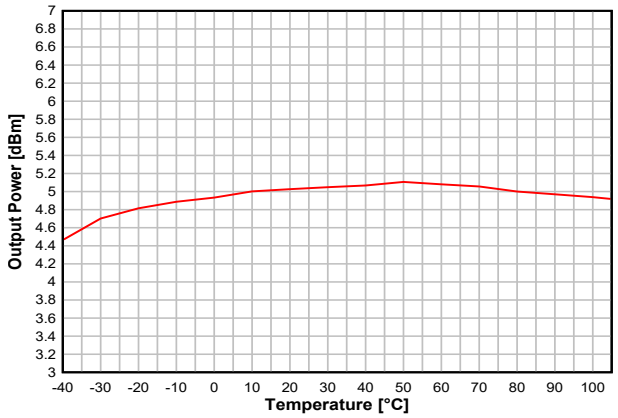



**図 8-18. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)**

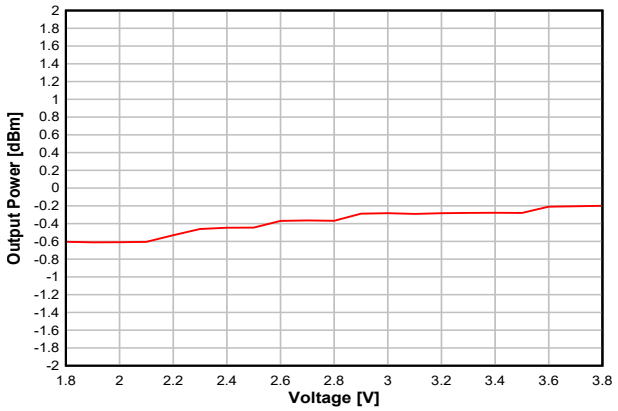



**図 8-19. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)**

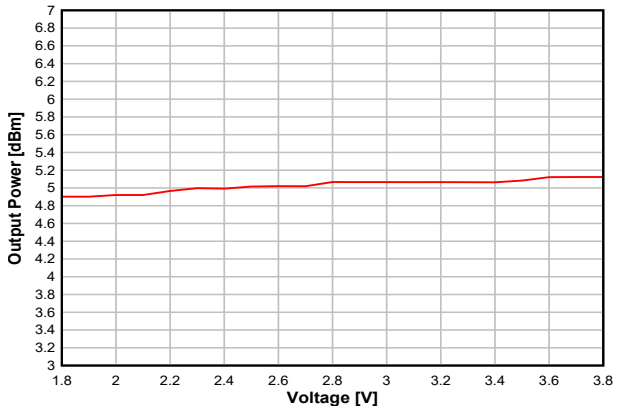



**図 8-20. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)**

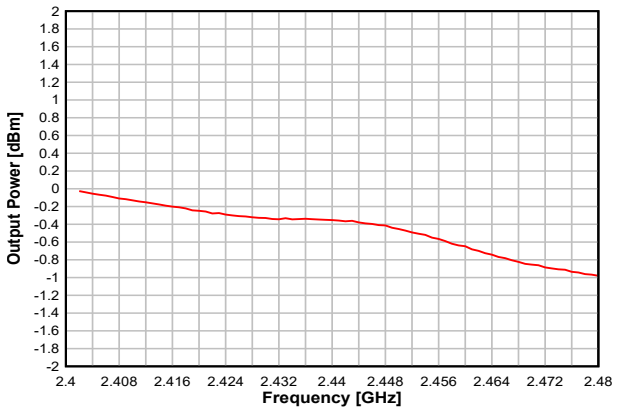



**図 8-21. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, 0 dBm)**

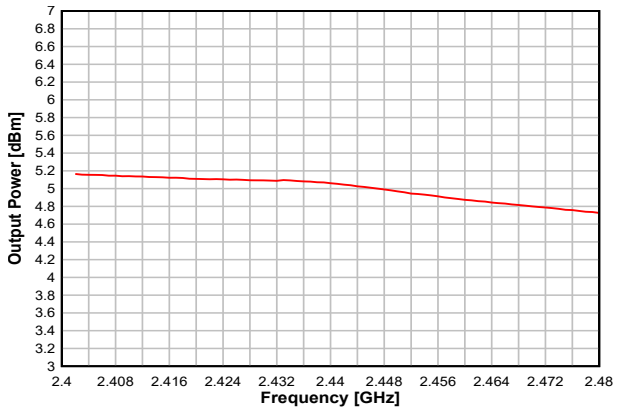



**図 8-22. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +5 dBm)**

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### 8.16.6 ADC Performance

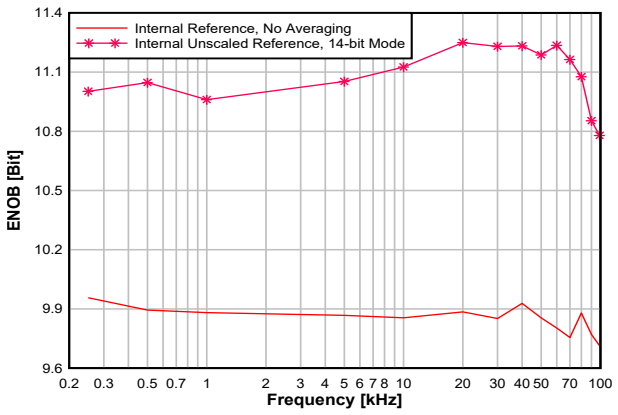



**図 8-23. ENOB vs. Input Frequency**

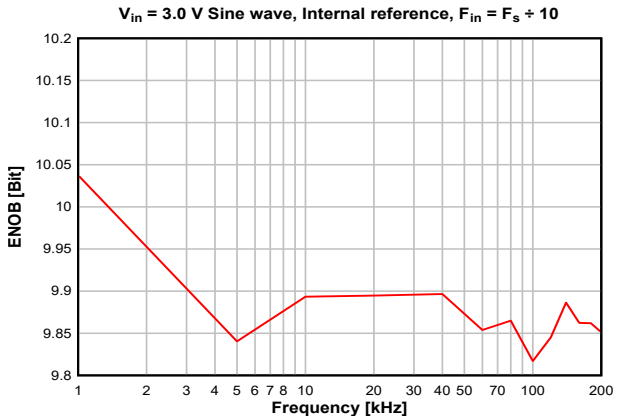



**図 8-24. ENOB vs. Sampling Frequency**

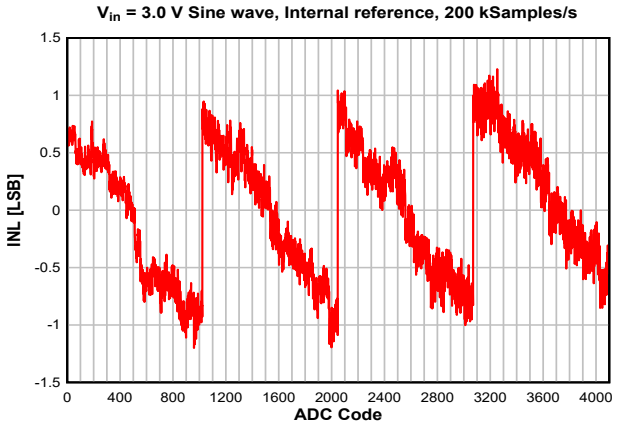



**図 8-25. INL vs. ADC Code**

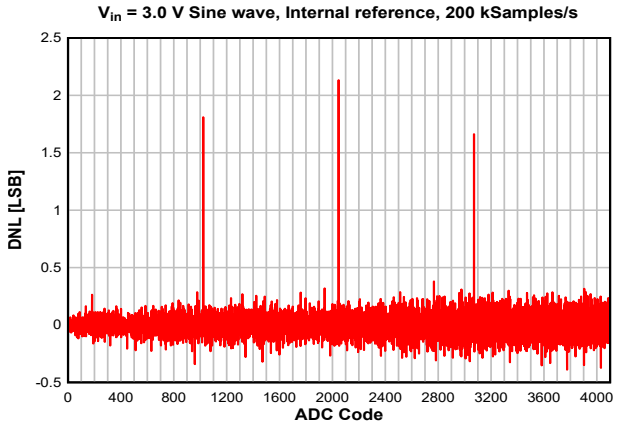



**図 8-26. DNL vs. ADC Code**

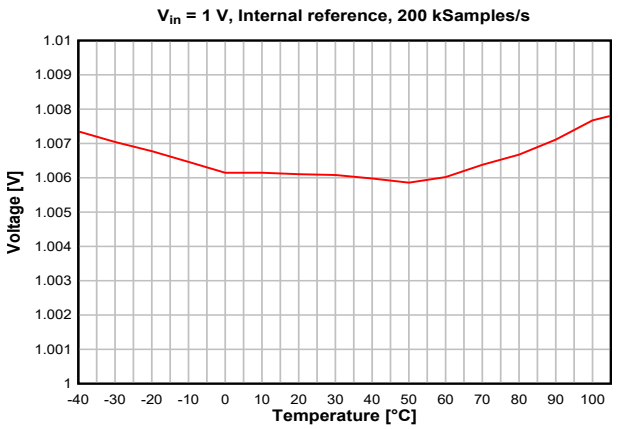



**図 8-27. ADC Accuracy vs. Temperature**

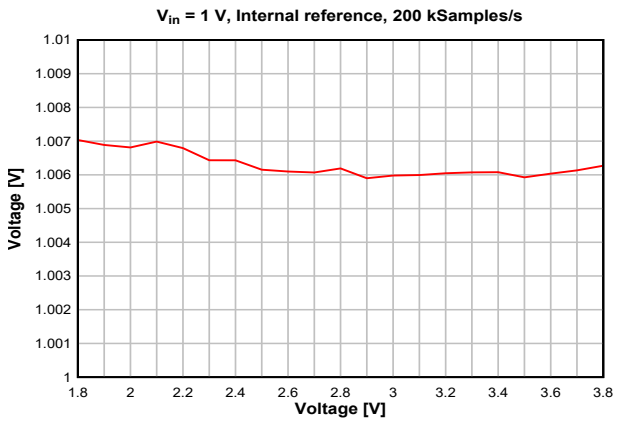



**図 8-28. ADC Accuracy vs. Supply Voltage (VDDS)**


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# 9 Detailed Description

## 9.1 Overview

セクション 4 shows the core modules of the CC2652R device.

## 9.2 System CPU

The CC2652R SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4F system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- IEEE 754-compliant single-precision Floating Point Unit (FPU)
- Memory Protection Unit (MPU) for safety-critical applications
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8 kB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

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## 9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

Multiprotocol solutions are enabled through time-sliced access of the radio, handled transparently for the application through the TI-provided RF driver and dual-mode manager.

A Packet Traffic Arbitrator (PTA) scheme is available for the managed coexistence of BLE and a co-located 2.4 GHz radio. This is based on 802.15.2 recommendations and common industry standards. The 3-wire coexistence interface has multiple modes of operation, encompassing different use cases and number of lines used for signaling. The radio acting as a slave is able to request access to the 2.4 GHz ISM band, and the master to grant it. Information about the request priority and TX or RX operation can also be conveyed.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

### 9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-speed 2 Mbps physical layer and the 500 kbps and 125 kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API. The Bluetooth 5.2 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

### 9.3.2 802.15.4 (Thread, Zigbee, 6LoWPAN)

Through a dedicated IEEE radio API, the RF Core supports the 2.4 GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread, Zigbee, and 6LoWPAN protocols. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

## 9.4 Memory

Up to 352 kB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is split into up to five 16 kB blocks and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by


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default and included in Standby mode power consumption numbers. Parity checking for detection of bit errors in memory is built-in, which reduces chip-level soft errors and thereby increases reliability. System SRAM is always initialized to zeroes upon code execution from boot.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8 kB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

There is a 4 kB ultra-low leakage SRAM available for use with the Sensor Controller Engine which is typically used for storing Sensor Controller programs, data and configuration parameters. This RAM is also accessible by the system CPU. The Sensor Controller RAM is not cleared to zeroes between system resets.

The ROM includes a TI-RTOS kernel and low-level drivers, as well as significant parts of selected radio stacks, which frees up flash memory for the application. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

### 9.5 Sensor Controller

The Sensor Controller contains circuitry that can be selectively enabled in both Standby and Active power modes. The peripherals in this domain can be controlled by the Sensor Controller Engine, which is a proprietary power-optimized CPU. This CPU can read and monitor sensors or perform other tasks autonomously; thereby significantly reducing power consumption and offloading the system CPU.

The Sensor Controller Engine is user programmable with a simple programming language that has syntax similar to C. This programmability allows for sensor polling and other tasks to be specified as sequential algorithms rather than static configuration of complex peripheral modules, timers, DMA, register programmable state machines, or event routing.

The main advantages are:

- Flexibility - data can be read and processed in unlimited manners while still ensuring ultra-low power
- 2 MHz low-power mode enables lowest possible handling of digital sensors
- Dynamic reuse of hardware resources
- 40-bit accumulator supporting multiplication, addition and shift
- Observability and debugging options

Sensor Controller Studio is used to write, test, and debug code for the Sensor Controller. The tool produces C driver source code, which the System CPU application uses to control and exchange data with the Sensor Controller. Typical use cases may be (but are not limited to) the following:

- Read analog sensors using integrated ADC or comparators
- Interface digital sensors using GPIOs, SPI, UART, or $I^2C$ ($I^2C$ and $I^2C$ are bit-banged)
- Capacitive sensing
- Waveform generation
- Very low-power pulse counting (flow metering)
- Key scan

The peripherals in the Sensor Controller include the following:

- The low-power clocked comparator can be used to wake the system CPU from any state in which the comparator is active. A configurable internal reference DAC can be used in conjunction with the comparator. The output of the comparator can also be used to trigger an interrupt or the ADC.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time-to-digital converter, and a comparator. The continuous time comparator in this block can also be used as a higher-accuracy alternative to the low-power clocked comparator. The Sensor Controller takes care of baseline tracking, hysteresis, filtering, and other related functions when these modules are used for capacitive sensing.
- The ADC is a 12-bit, 200 ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources including timers, I/O pins, software, and comparators.

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- The analog modules can connect to up to eight different GPIOs
- Dedicated SPI master with up to 6 MHz clock speed

The peripherals in the Sensor Controller can also be controlled from the main application processor.

## 9.6 Cryptography

The CC2652R device comes with a wide set of modern cryptography-related hardware accelerators, drastically reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations runs in a background hardware thread.
Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Secure Hash Algorithm 2 (SHA-2)** with support for SHA224, SHA256, SHA384, and SHA512
- **Advanced Encryption Standard (AES)** with 128 and 256 bit key lengths
- **Public Key Accelerator** - Hardware accelerator supporting mathematical operations needed for elliptic curves up to 512 bits and RSA key pair generation up to 1024 bits.

Through use of these modules and the TI provided cryptography drivers, the following capabilities are available for an application or stack:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **SHA2 based MACs**
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, can also be implemented using the provided hardware accelerators but are not part of the TI SimpleLink SDK for the CC2652R device.


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## 9.7 Timers

A large selection of timers are available as part of the CC2652R device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF). This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. The real time clock can also be read by the Sensor Controller Engine to timestamp sensor data and also has dedicated capture channels. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Sensor Controller Timers**

  The Sensor Controller contains 3 timers:

  AUX Timer 0 and 1 are 16-bit timers with a $2^N$ prescaler. Timers can either increment on a clock or on each edge of a selected tick source. Both one-shot and periodical timer modes are available.

  AUX Timer 2 is a 16-bit timer that can operate at 24 MHz, 2 MHz or 32 kHz independent of the Sensor Controller functionality. There are 4 capture or compare channels, which can be operated in one-shot or periodical modes. The timer can be used to generate events for the Sensor Controller Engine or the ADC, as well as for PWM output or waveform generation.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

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## 9.8 Serial Peripherals and I/O

The SSIs are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI master and slave up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The $I^2S$ interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The $I^2C$ interface is also used to communicate with devices compatible with the $I^2C$ standard. The $I^2C$ interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in セクション 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x2, CC26x2 SimpleLink™ Wireless MCU Technical Reference Manual.

## 9.9 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2652R device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

## 9.10 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

## 9.11 Debug

The debug subsystem implements two IEEE standards for debug and test purposes:

IEEE 1149.7 Class 4: Reduced-pin and Enhanced-functionality Test Access port and Boundary-scan Architecture. This is known by the acronym cJTAG (compact JTAG) and this device uses only two pins to communicate to the target: TMS (JTAG_TMSC) and TCK (JTAG_TCKC). This is the default mode of operation

IEEE standard 1149.1: Test Access Port and Boundary Scan Architecture Test Access Port (TAP). This standard is known by the acronym JTAG and this device uses four pins to communicate to the target: TMS (JTAG_TMSC), TCK (JTAG_TCKC), TDI (JTAG_TDI) and TDO (JTAG_TDO).

The debug subsystem also implements a user-configurable firewall to control unauthorized access to debug/test ports.


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Also featured is **EnergyTrace**/**EnergyTrace++**. This technology implements an improved method for measuring MCU current consumption, which features a very high dynamic range (from sub-µA to hundreds of mA), high sample rate (up to 256 kSamples/s) and the ability to track the CPU and peripheral power states.

Two modes of operation can be configured. **EnergyTrace** measures the overall MCU current consumption and allows maximum accuracy and speed to track ultra low-power states as well as the fast power transitions during radio transmission and reception. **EnergyTrace++** tracks the various power states of both the CPU and its Peripherals as well as the system clocks, allowing a close monitoring of the overall device activity.

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## 9.12 Power Management

To minimize power consumption, the CC2652R supports a number of power modes and power management features (see 表 9-1).

**表 9-1. Power Modes**

| MODE | SOFTWARE CONFIGURABLE POWER MODES | | | | RESET PIN HELD |
|---|---|---|---|---|---|
| | ACTIVE | IDLE | STANDBY | SHUTDOWN | |
| **CPU** | Active | Off | Off | Off | Off |
| **Flash** | On | Available | Off | Off | Off |
| **SRAM** | On | On | Retention | Off | Off |
| **Supply System** | On | On | Duty Cycled | Off | Off |
| Register and CPU retention | Full | Full | Partial | No | No |
| SRAM retention | Full | Full | Full | No | No |
| 48 MHz high-speed clock (SCLK_HF) | XOSC_HF or RCOSC_HF | XOSC_HF or RCOSC_HF | Off | Off | Off |
| 2 MHz medium-speed clock (SCLK_MF) | RCOSC_MF | RCOSC_MF | Available | Off | Off |
| 32 kHz low-speed clock (SCLK_LF) | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | XOSC_LF or RCOSC_LF | Off | Off |
| Peripherals | Available | Available | Off | Off | Off |
| Sensor Controller | Available | Available | Available | Off | Off |
| Wake-up on RTC | Available | Available | Available | Off | Off |
| Wake-up on pin edge | Available | Available | Available | Available | Off |
| Wake-up on reset pin | On | On | On | On | On |
| Brownout detector (BOD) | On | On | Duty Cycled | Off | Off |
| Power-on reset (POR) | On | On | On | Off | Off |
| Watchdog timer (WDT) | Available | Available | Paused | Off | Off |

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see 表 9-1).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or Sensor Controller event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain and Sensor Controller), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.


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The Sensor Controller is an autonomous processor that can control the peripherals in the Sensor Controller independently of the system CPU. This means that the system CPU does not have to wake up, for example to perform an ADC sampling or poll a digital sensor over SPI, thus saving both current and wake-up time that would otherwise be wasted. The Sensor Controller Studio tool enables the user to program the Sensor Controller, control its peripherals, and wake up the system CPU as needed. All Sensor Controller peripherals can also be controlled by the system CPU.

注

The power, RF and clock management for the CC2652R device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2652R software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

## 9.13 Clock Systems

The CC2652R device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or an external 48 MHz crystal (XOSC_HF). Radio operation requires an external 48 MHz crystal.

SCLK_MF is an internal 2 MHz clock that is used by the Sensor Controller in low-power mode and also for internal power management circuitry. The SCLK_MF clock is always driven by the internal 2 MHz RC Oscillator (RCOSC_MF).

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used by the Sensor Controller for ultra-low-power operation and is also used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digital IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

## 9.14 Network Processor

Depending on the product configuration, the CC2652R device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

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# 10 Application, Implementation, and Layout

注

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For general design guidelines and hardware configuration guidelines, refer to the *CC13xx/CC26xx Hardware Configuration and PCB Design Considerations Application Report*.

## 10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2652R device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

Integrated matched filter-balun devices can be used both at sub-1 GHz frequencies and at 2.4 GHz for the low-power RF outputs. Refer to the "Integrated Passive Component" section in CC13xx/CC26xx Hardware Configuration and PCB Design Considerations for further information.

| | |
|---|---|
| CC26x2REM-7ID Design Files | The CC26x2REM-7ID reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document. |
| LAUNCHXL-CC26X2R1 Design Files | The CC26X2R LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2652R device. This design applies to both the CC2642R and CC2652R devices. |
| Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad ™ Development Kit and SensorTag | The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including:<br>• PCB antennas<br>• Helical antennas<br>• Chip antennas<br>• Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz<br>The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad development kits and SensorTags. |


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## 10.2 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are three recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \quad (2)$$

3. From ambient temperature:

$$T_J = R_{\theta\mathrm{JA}} \times P + T_A \quad (3)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in *Thermal Resistance Characteristics*.

**Example:**

Using 式 3, the temperature difference between ambient temperature and junction temperature is calculated. In this example, we assume a simple use case where the radio is transmitting continuously at 0 dBm output power. Let us assume the ambient temperature is 85 °C and the supply voltage is 3 V. To calculate P, we need to look up the current consumption for Tx at 85 °C in セクション 8.16 . From the plot, we see that the current consumption is 7.8 mA. This means that P is 7.8 mA × 3 V = 23.4 mW.

The junction temperature is then calculated as:

$$T_J = 23.4^{°C}/_{W} \times 23.4mW + T_A = 0.6°C + T_A \quad (4)$$

As can be seen from the example, the junction temperature is 0.6 °C higher than the ambient temperature when running continuous Tx at 85 °C and, thus, well within the recommended operating conditions.

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, etc. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in Measuring CC13xx and CC26xx current consumption.

# 11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

## 11.1 Tools and Software

The CC2652R device is supported by a variety of software and hardware development tools.

**Development Kit**

| | |
|---|---|
| CC26x2 LaunchPad™ Development Kit | The CC26x2R LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2652R SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4 GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more. The built-in EnergyTrace™ software is an energy-based code analysis tool that measures and displays the application's energy |

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profile and helps to optimize it for ultra-low-power consumption. See セクション 6 for guidance in selecting the correct device for single-protocol products.

TMDSEMU110-U Debug Probe

The TMDSEMU110-U Debug Probe enables development of high-performance wireless applications in the entire family of SimpleLink LaunchPad™ development boards. Featuring a convenient enclosure, which grants the proper mechanical robustness for field and production environments, it supports not only multiple standards such as JTAG/cJTAG/SWD but also a UART backchannel and four GPIOs for maximum debugging flexibility. In addition, the expansion connector allows using the TMDSEMU110-ETH add-on (sold separately), which adds the full featured XDS110 EnergyTrace™ technology with variable supply voltage from 1.8V to 3.6V and up to 800 mA of supply current. The XDS110 EnergyTrace™ technology is a new method for measuring the current consumption that captures the complete operational profile of the wireless MCU.

### Software

SimpleLink™ LOWPOWER F2 SDK

The SimpleLink LOWPOWER F2 Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC2652R device, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz
- EasyLink - a large set of building blocks for building proprietary RF software stacks
- Multiprotocol support - concurrent operation between stacks using the Dynamic Multiprotocol Manager (DMM)

The SimpleLink LOWPOWER F2 SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.


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## Development Tools

**Code Composer Studio™ Integrated Development Environment (IDE)**

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

**Code Composer Studio™ Cloud IDE**

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

**IAR Embedded Workbench® for Arm®**

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 kB size-limited version is available through iar.com.

**SmartRF™ Studio**

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

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| | |
|---|---|
| Sensor Controller Studio | Sensor Controller Studio is used to write, test and debug code for the Sensor Controller peripheral. The tool generates a Sensor Controller Interface driver, which is a set of C source files that are compiled into the System CPU application. These source files also contain the Sensor Controller binary image and allow the System CPU application to control and exchange data with the Sensor Controller. Features of the Sensor Controller Studio include:<br>• Ready-to-use examples for several common use cases<br>• Full toolchain with built-in compiler and assembler for programming in a C-like programming language<br>• Provides rapid development by using the integrated sensor controller task testing and debugging functionality, including visualization of sensor data and verification of algorithms |
| CCS UniFlash | CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge. |

### 11.1.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

## 11.2 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2652R. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

**TI Resource Explorer**

| | |
|---|---|
| TI Resource Explorer | Software examples, libraries, executables, and documentation are available for your device and development board. |

**Errata**

| | |
|---|---|
| *CC2652R Silicon Errata* | The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision. |

**Application Reports**

All application reports for the CC2652R device are found on the device product folder at: ti.com/product/CC2652R/technicaldocuments.

**Technical Reference Manual (TRM)**

| | |
|---|---|
| *CC13x2, CC26x2 SimpleLink™ Wireless MCU TRM* | The TRM provides a detailed description of all modules and peripherals available in the device family. |


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## 11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

# 12 Mechanical, Packaging, and Orderable Information

## 12.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| CC2652R1FRGZR | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU \| NIPDAUAG | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZR.A | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZR.B | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZRG4 | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZRG4.A | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZRG4.B | Active | Production | VQFN (RGZ) \| 48 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZT | Active | Production | VQFN (RGZ) \| 48 | 250 \| SMALL T&R | Yes | NIPDAU \| NIPDAUAG | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZT.A | Active | Production | VQFN (RGZ) \| 48 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |
| CC2652R1FRGZT.B | Active | Production | VQFN (RGZ) \| 48 | 250 \| SMALL T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 105 | CC2652 R1F |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

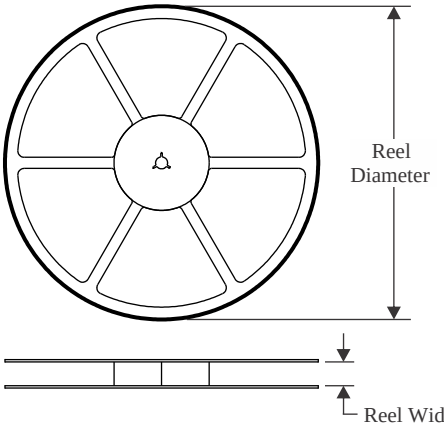
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

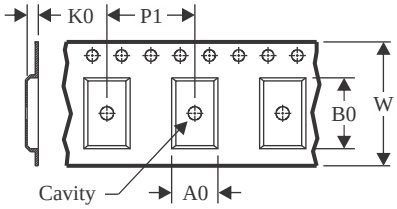
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

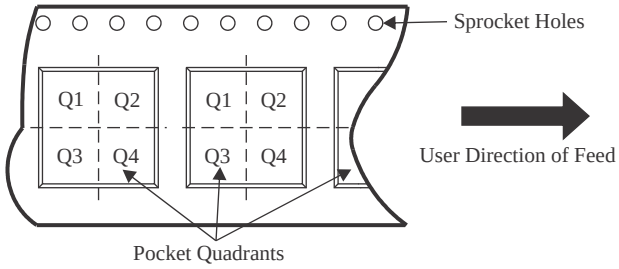



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

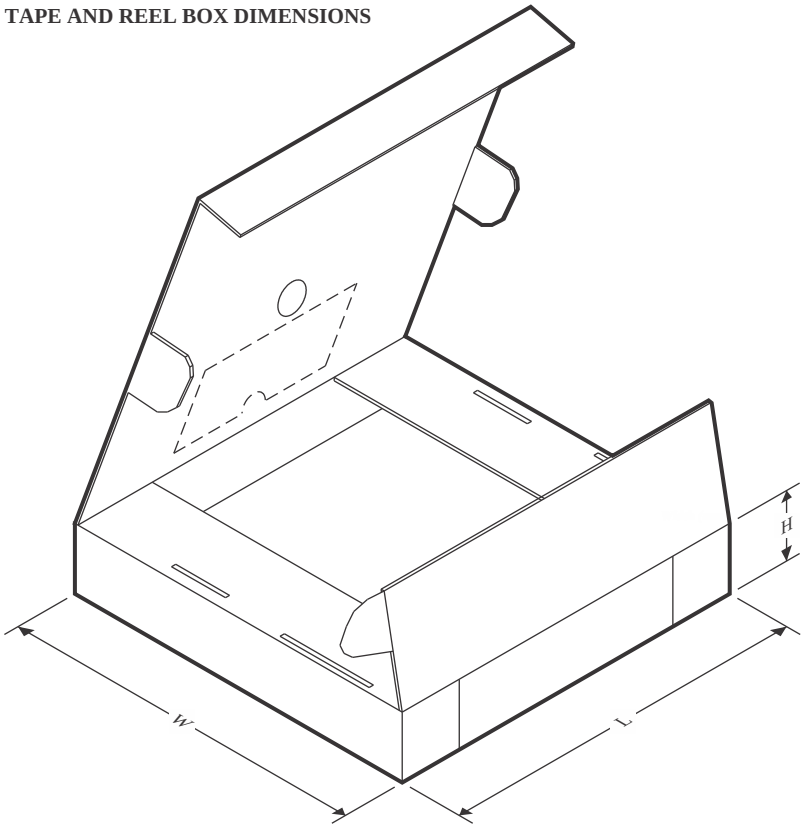
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZRG4 | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZRG4 | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZT | VQFN | RGZ | 48 | 250 | 180.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| CC2652R1FRGZT | VQFN | RGZ | 48 | 250 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 353.0 | 353.0 | 32.0 |
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 35.0 |
| CC2652R1FRGZR | VQFN | RGZ | 48 | 2500 | 360.0 | 360.0 | 36.0 |
| CC2652R1FRGZRG4 | VQFN | RGZ | 48 | 2500 | 353.0 | 353.0 | 32.0 |
| CC2652R1FRGZRG4 | VQFN | RGZ | 48 | 2500 | 367.0 | 367.0 | 35.0 |
| CC2652R1FRGZT | VQFN | RGZ | 48 | 250 | 210.0 | 185.0 | 35.0 |
| CC2652R1FRGZT | VQFN | RGZ | 48 | 250 | 353.0 | 353.0 | 32.0 |

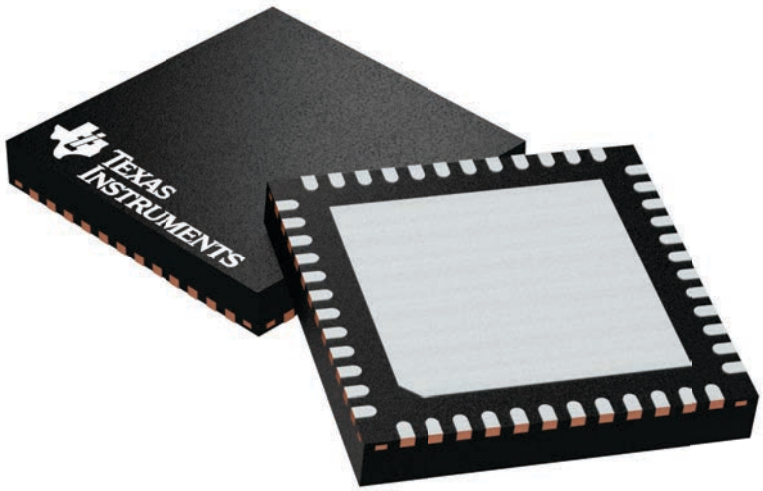
# GENERIC PACKAGE VIEW

## RGZ 48

## VQFN - 1 mm max height

**7 x 7, 0.5 mm pitch**

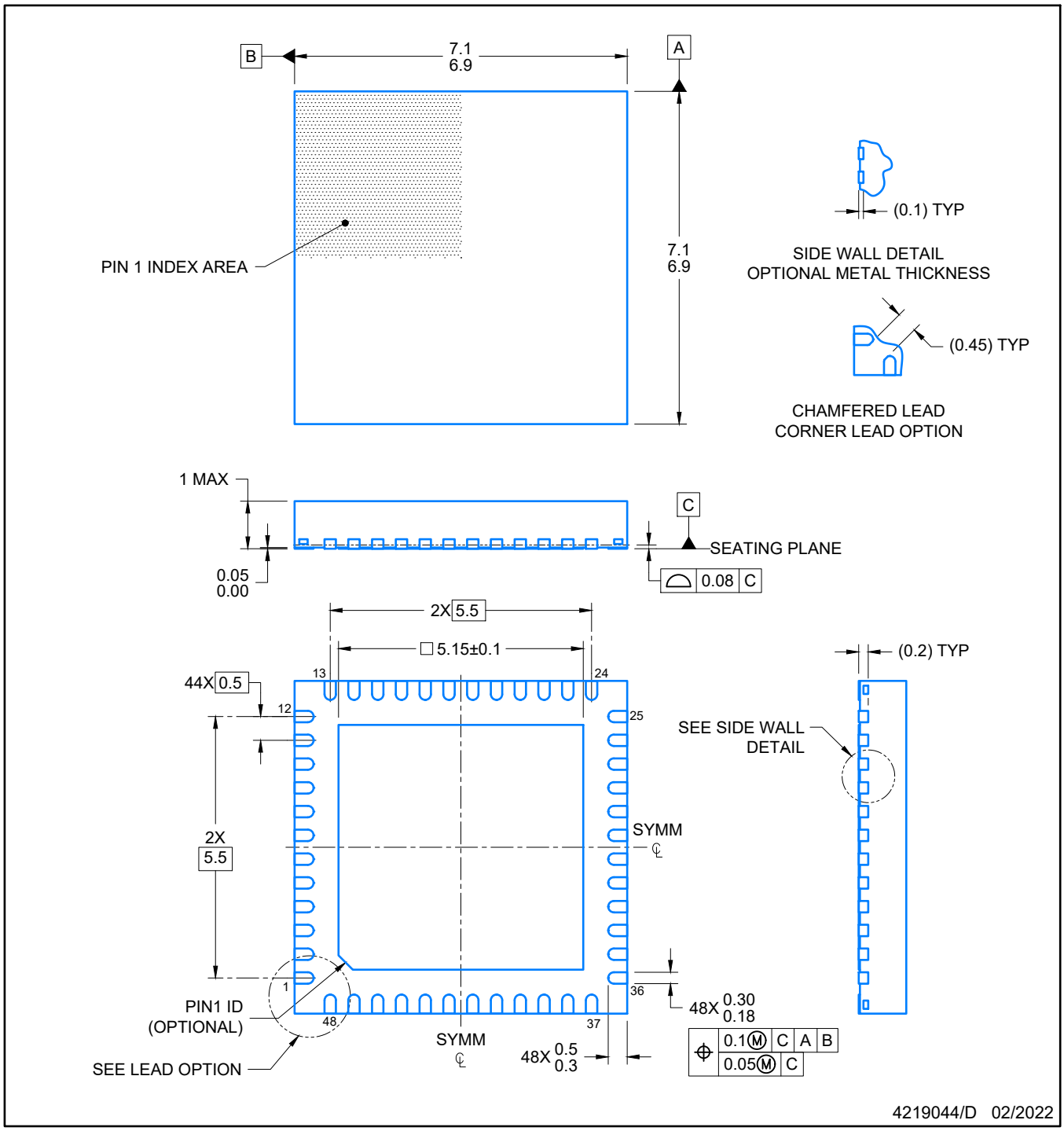
PLASTIC QUADFLAT PACK- NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

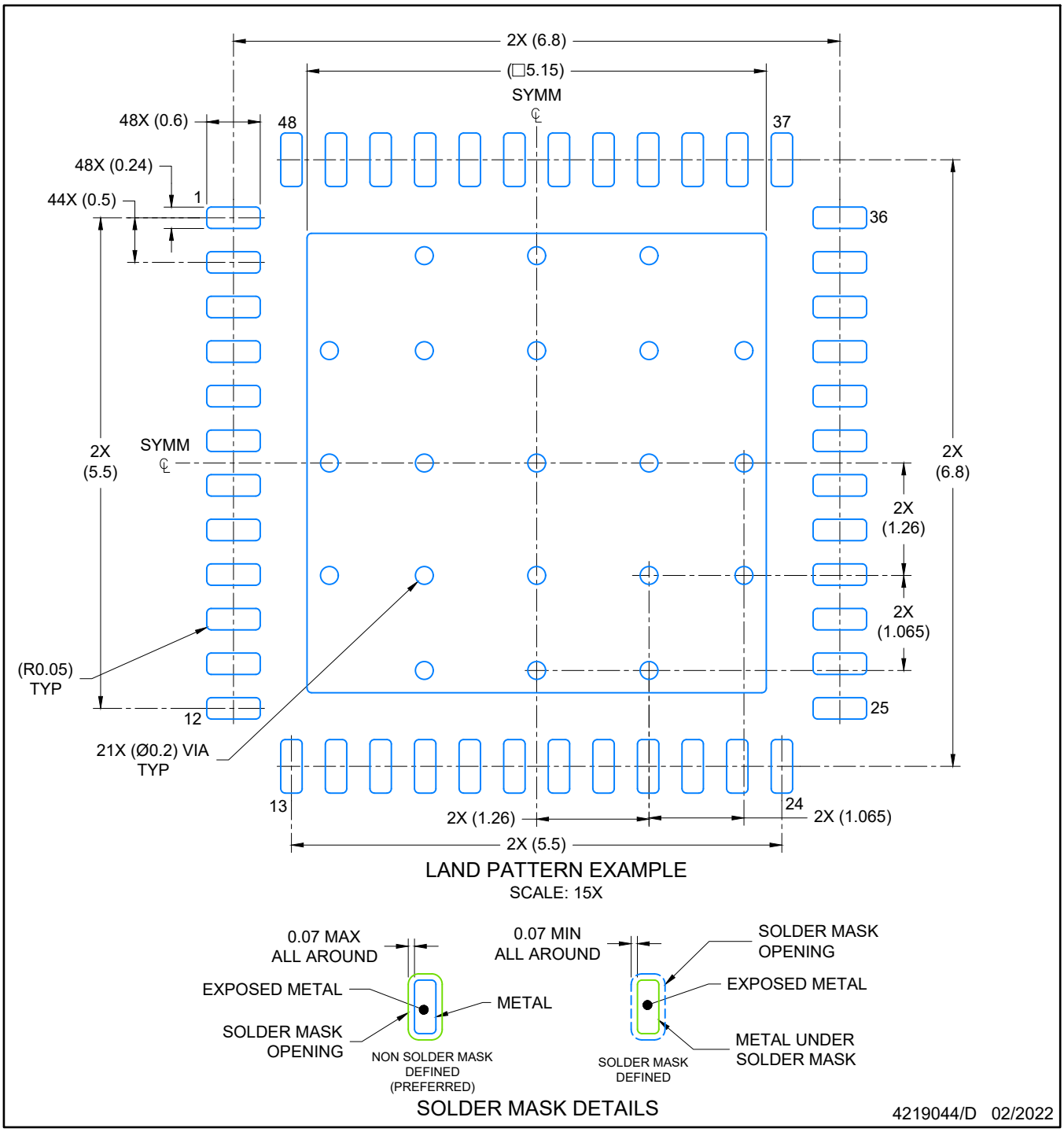
4224671/A

PLASTIC QUADFLAT PACK- NO LEAD



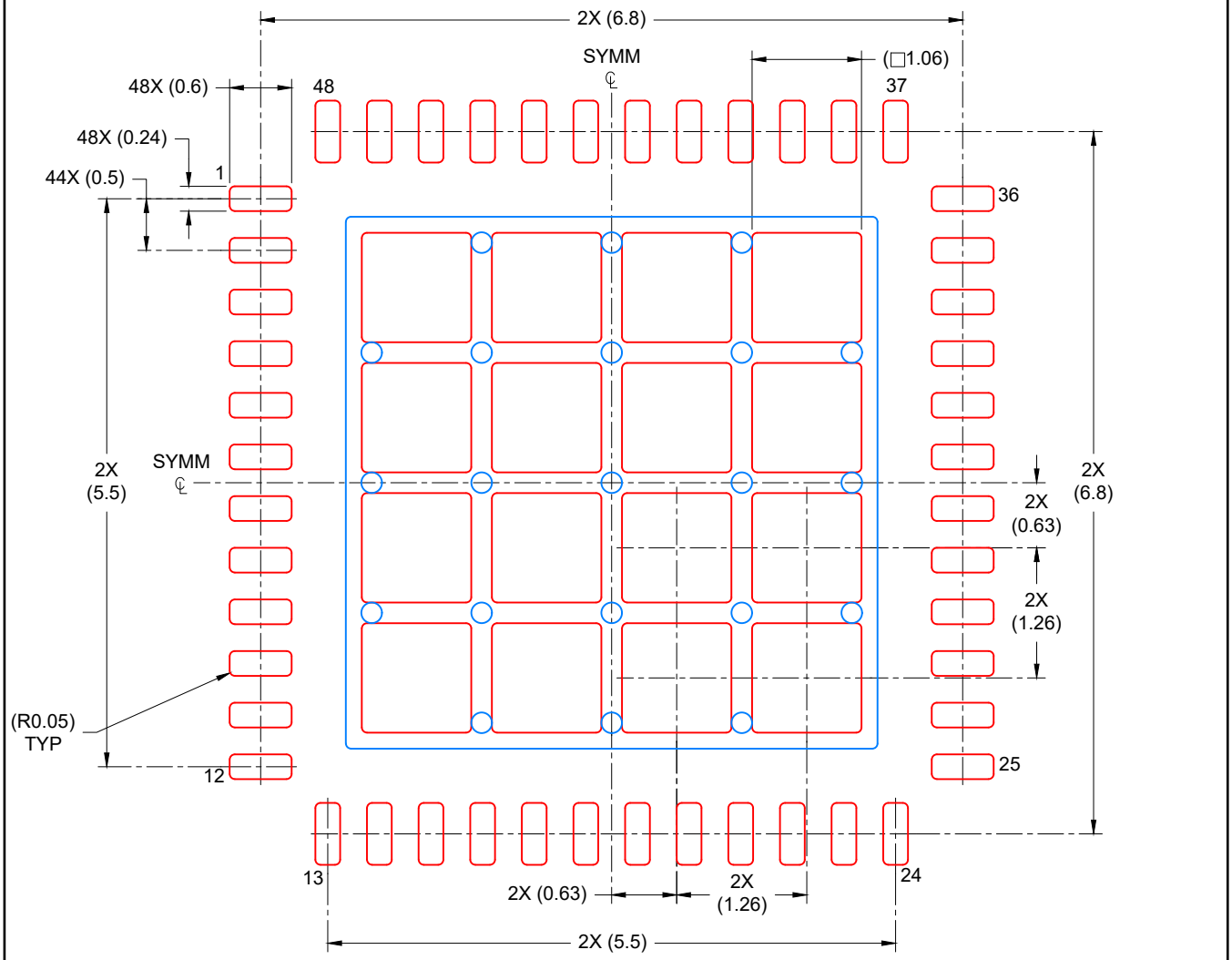

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/D 02/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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