CDx4HC4002 高速 CMOS ロジックのデュアル 4 入力 NOR ゲート

1 特長

- 標準伝搬遅延 = 8ns (V_{CC} = 5V、C_L = 15pF、T_A = 25℃時)
- ファンアウト (全温度範囲にわたって)
  - 標準出力:10 個の LSTTL 負荷
  - バス・ドライバ出力:15 の LSTTL 負荷
- 広い動作温度範囲:-55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:V_{cc} の N_{IL} = 30%、N_{IH} = 30% (V_{CC} = 5V 時)

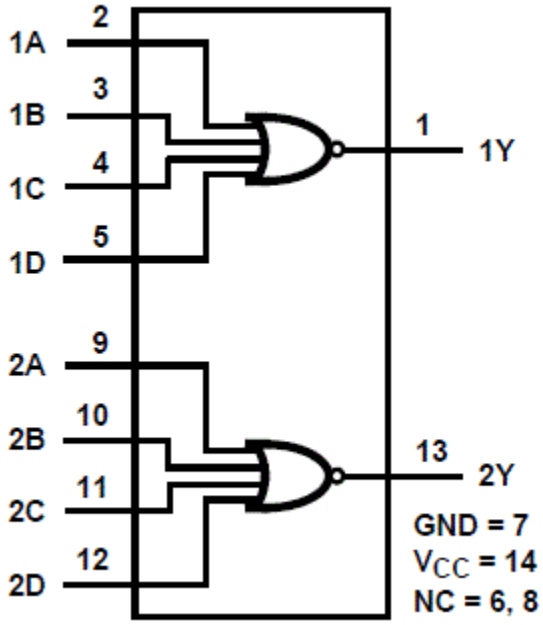
2 概要

HC4002 ロジックゲートはシリコンゲート CMOS 技術を利用して、標準 CMOS IC の低消費電力で LSTTL ゲートと同様の動作速度を実現しています。すべてのデバイスに、10 の LSTTL 負荷を駆動する機能があります。HC4002 ロジック・ファミリの機能およびピン配置は、標準の LS ロジック・ファミリと互換性があります。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
CD74HC4002M	SOIC (14)	8.65mm × 3.9mm
CD54HC4002F3A	CDIP (14)	19.55mm × 6.71mm
CD74HC4002E	PDIP (14)	19.31mm × 6.35mm
CD74HC4002PW	TSSOP (14)	5.0mm × 4.4mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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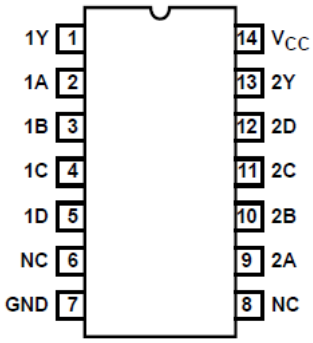
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (October 2003) to Revision F (February 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新	1

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4 Pin Configuration and Functions



J, N, D, or PW package
14-Pin CDIP, PDIP, SOIC, or TSSOP
Top View

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5 V or V_I > V_{CC} + 0.5 V		± 20	mA
I_{OK}	Output diode current	For V_O < -0.5 V or V_O > V_{CC} + 0.5 V		± 20	mA
I_O	Output source or sink current per output pin	For V_O > -0.5 V or V_O < V_{CC} + 0.5 V		± 25	mA
	Continuous current V_{CC} or ground current			± 50	mA
T_J	Junction temperature			150	
T_{stg}	Storage temperature range		– 65	150	
	Lead temperature (Soldering 10s) (SOIC - lead tips only)			300	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	V
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	ns
		6 V		400	ns
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		D (SOIC) 14 PINS	N (PDIP) 14 PINS	NS (SO) 14 PINS	PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	86	80	76	113	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.

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5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	25 o C			-40℃ to 85℃		-55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20 μA	6			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			2		20		40	μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

Input t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	V_{CC} (V)	25℃		-40℃ to 85℃	-55℃ to 125℃	UNIT
				TYP	MAX	MAX	MAX	
HC TYPES								
t_{PLH}, t_{PHL}	Propagation delay, nA, nB, nC, nD to nY	C_L = 50 pF	2		100	125	150	ns
			4.5		20	25	30	ns
			6		17	21	26	ns
		C_L = 15 pF	5	8				ns
t_{TLH}, t_{THL}	Output transition times (see Figure 1)	C_L = 50 pF	2		75	95	110	ns
			4.5		15	19	22	ns
			6		13	16	19	ns
C_{IN}	Input capacitance				10	10	10	pF
C_{PD}	Power dissipation capacitance[1] [2]	C_L = 15 pF	5	22				pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.
(2) P_D = V_{CC} ^{2} f_i (C_{PD} + C_L) where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

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6 Parameter Measurement Information

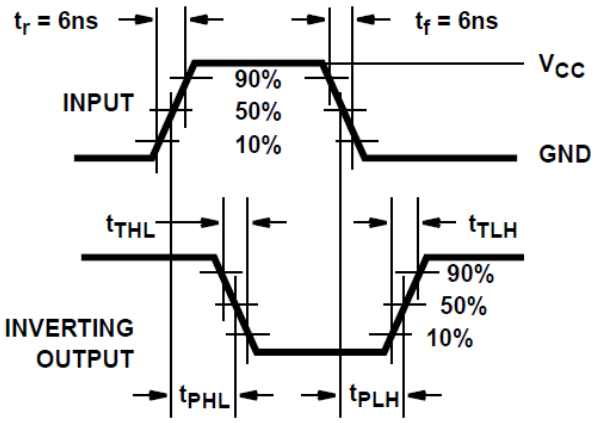


図 6-1. HC and HCU Transition Times and Propagation Delay Times, Combination Logic

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7 Detailed Description

7.1 Overview

The ’HC4002 logic gate utilizes silicon gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The ’HC4002 logic family is functional as well as pin compatible with the standard LS logic family.

7.2 Functional Block Diagram

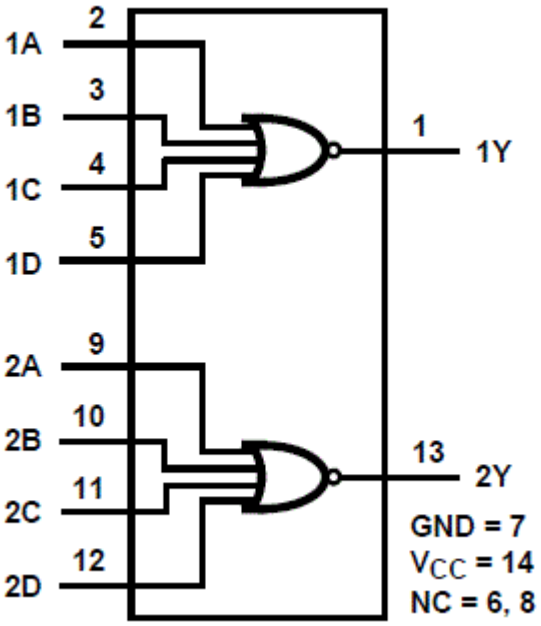


図 7-1. Functional Diagram

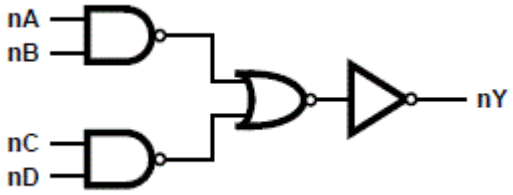


図 7-2. Logic Symbol

7.3 Device Functional Modes

表 7-1. Truth Table(1)

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Irrelevant

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC4002F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404401CA CD54HC4002F3A
CD54HC4002F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8404401CA CD54HC4002F3A
CD74HC4002E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4002E
CD74HC4002E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4002E
CD74HC4002M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4002M
CD74HC4002M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC4002M
CD74HC4002M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4002M
CD74HC4002MT	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC4002M
CD74HC4002PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HJ4002
CD74HC4002PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4002
CD74HC4002PWRG4	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4002

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF CD54HC4002, CD74HC4002 :

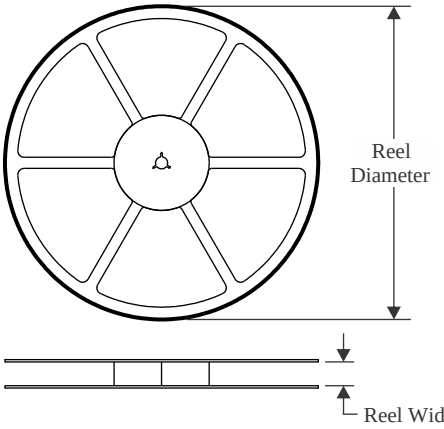
- Catalog : CD74HC4002
- Military : CD54HC4002

NOTE: Qualified Version Definitions:

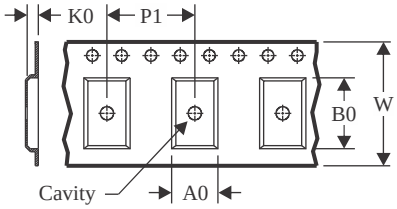
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

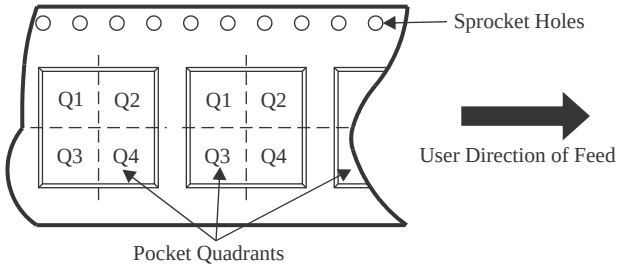


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

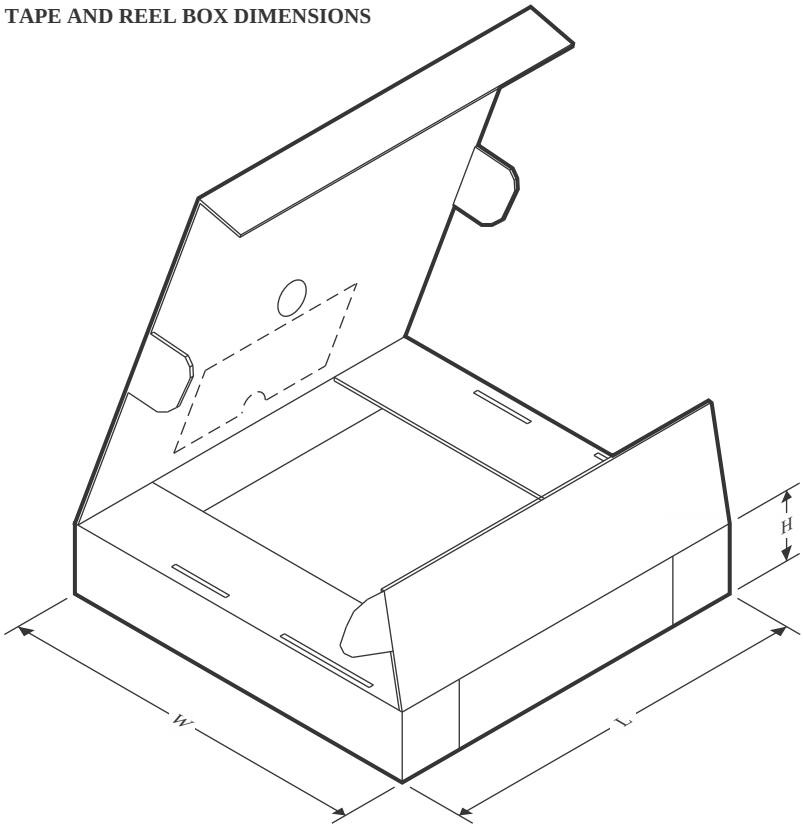
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4002M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4002PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4002PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4002PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

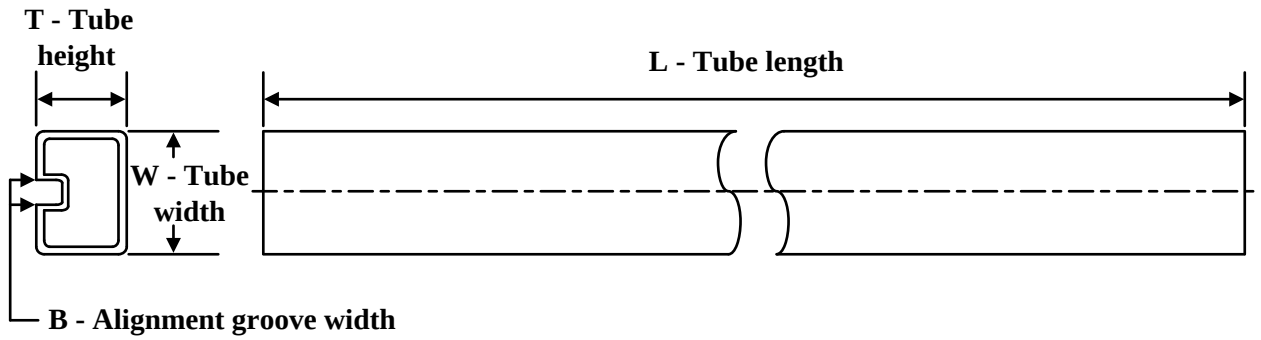
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4002M96	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC4002PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4002PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4002PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



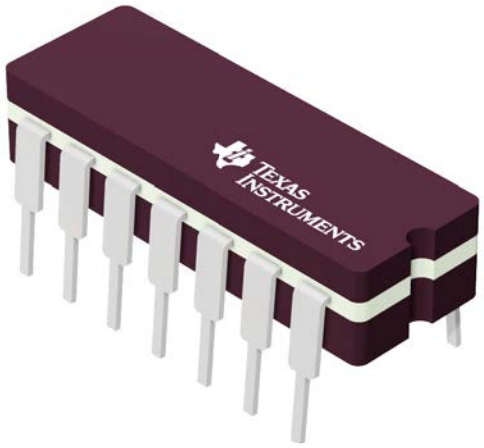
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC4002E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4002E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4002E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4002E.A	N	PDIP	14	25	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

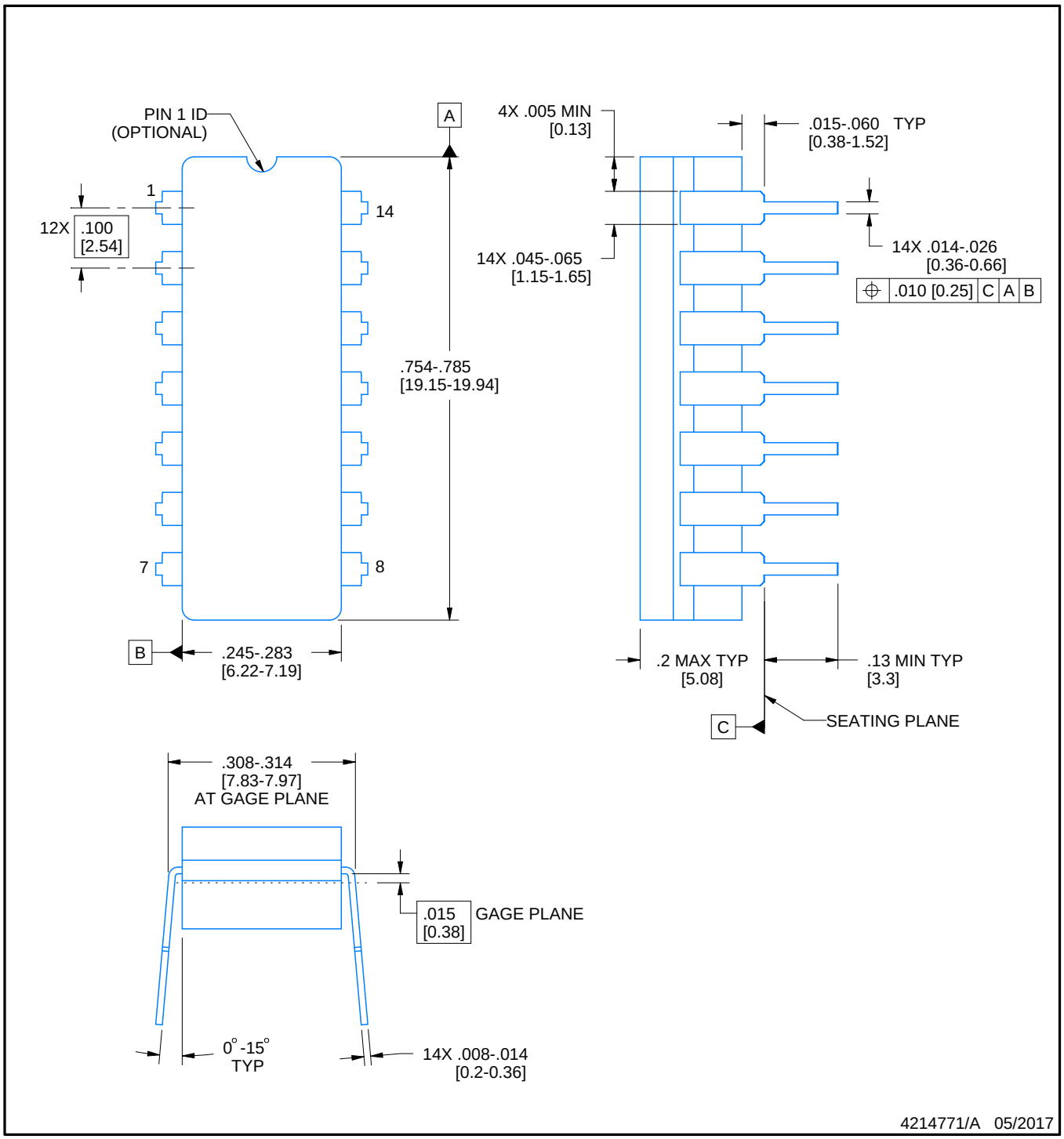


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

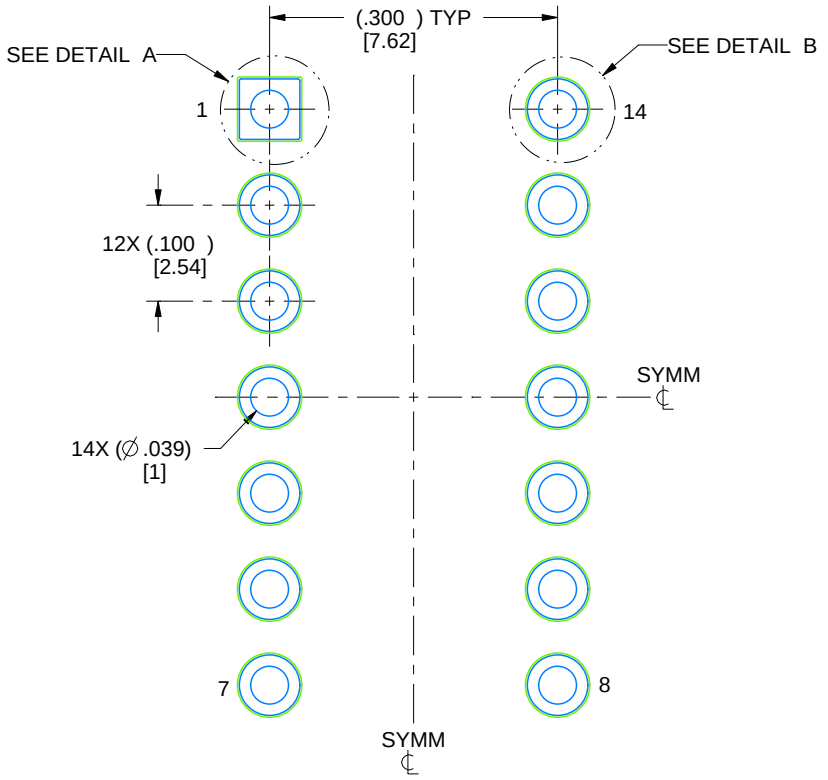
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

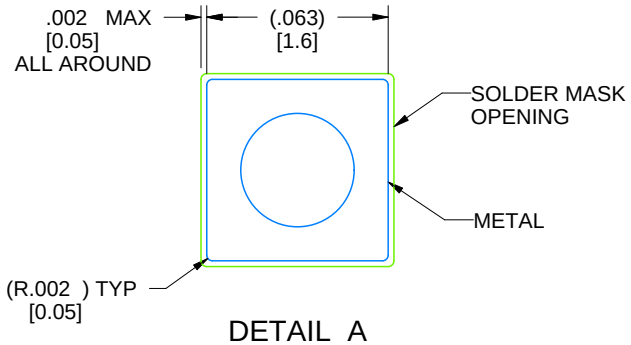
J0014A

CDIP - 5.08 mm max height

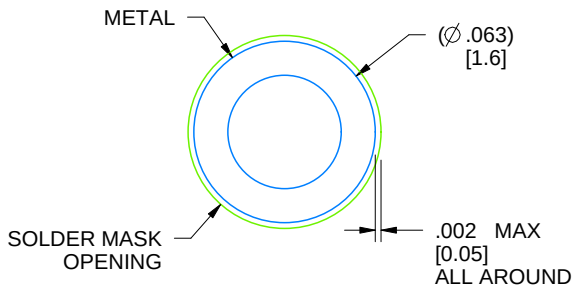
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



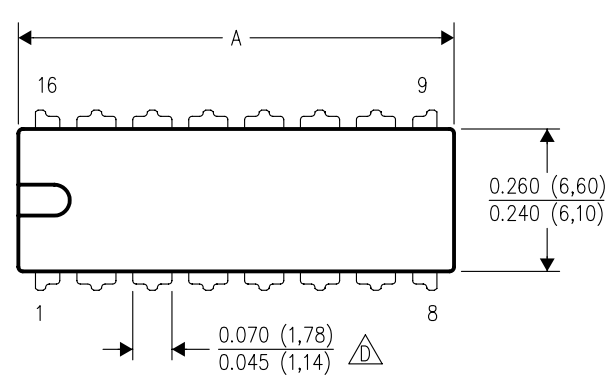
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

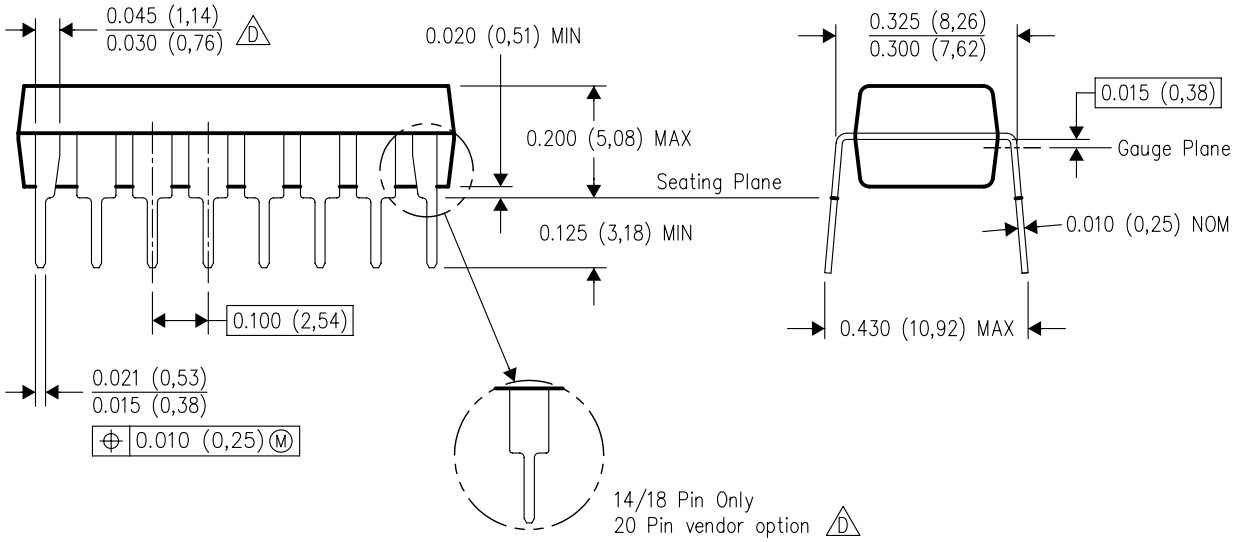
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

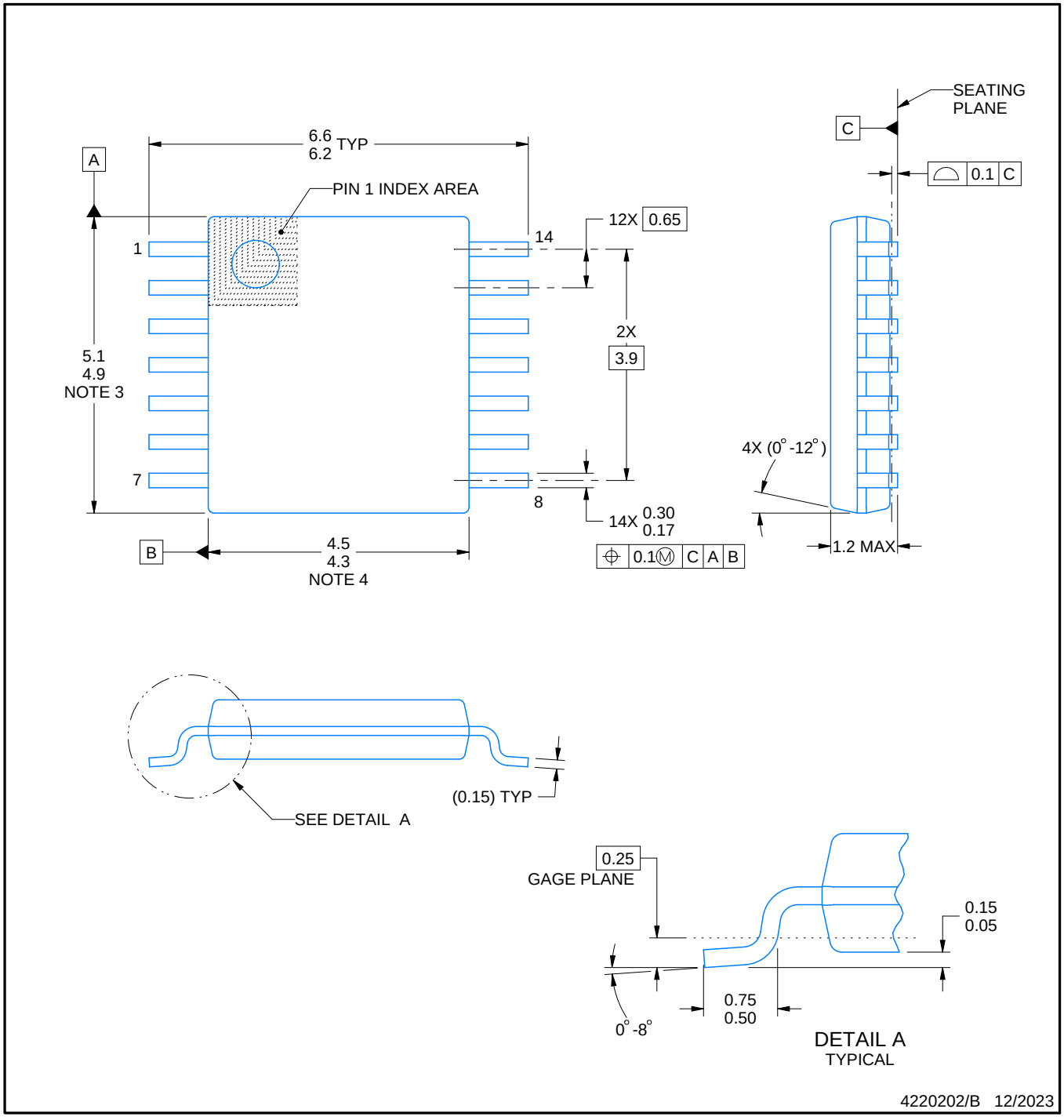
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

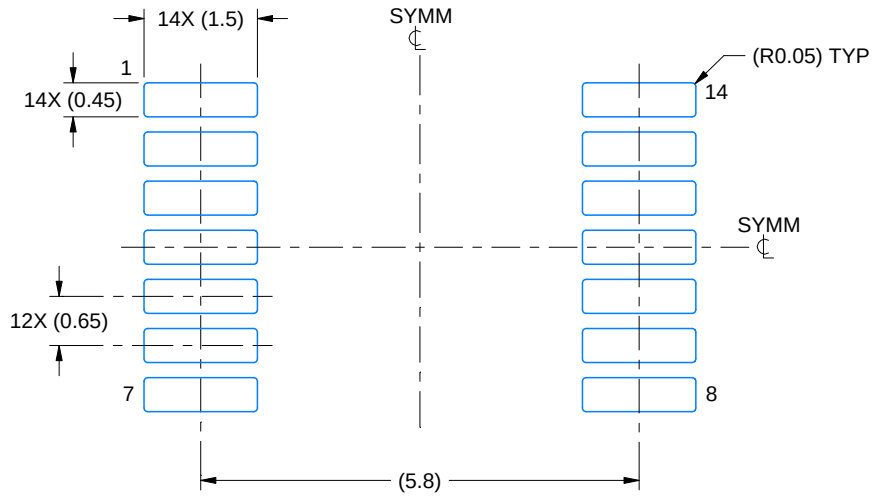
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

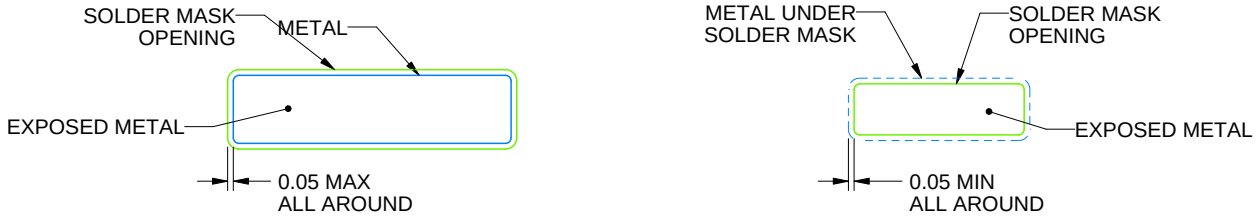


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

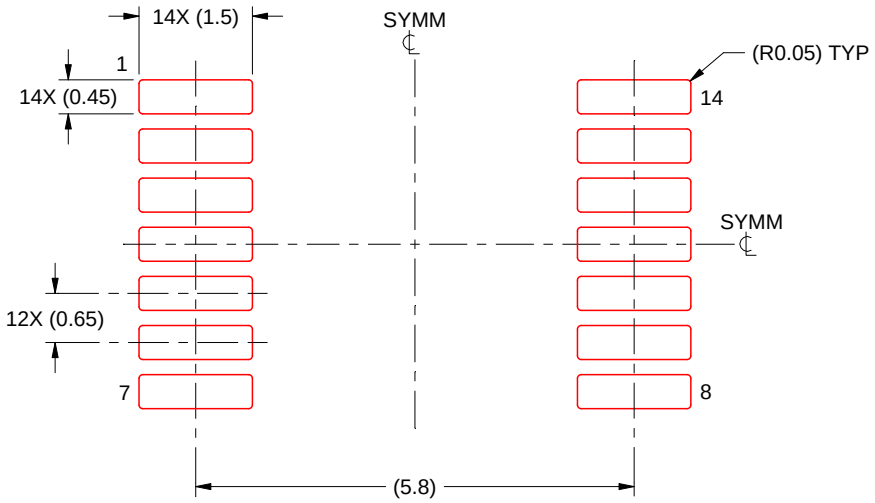


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

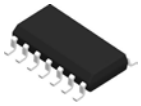


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

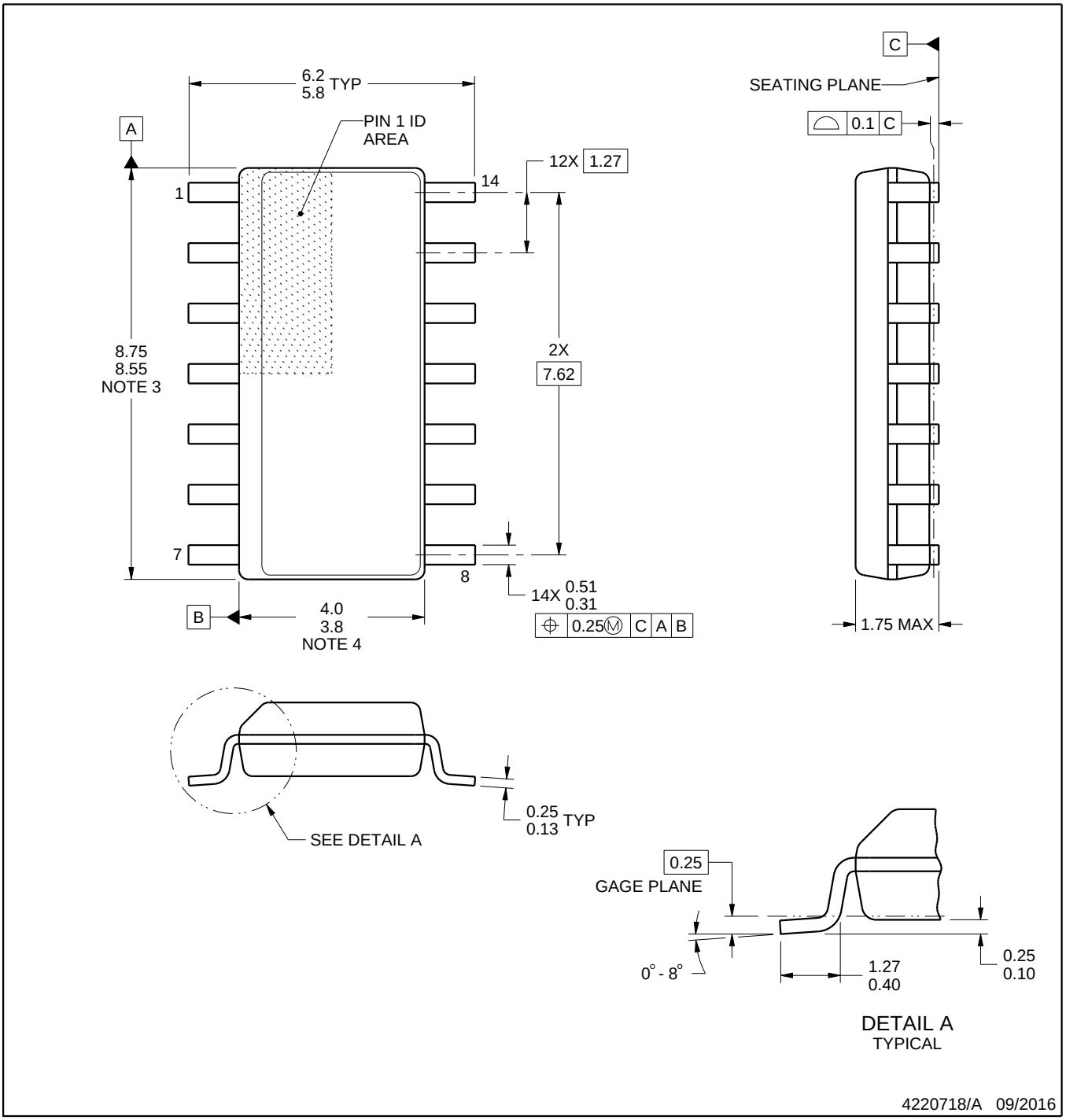


PACKAGE OUTLINE

D0014A

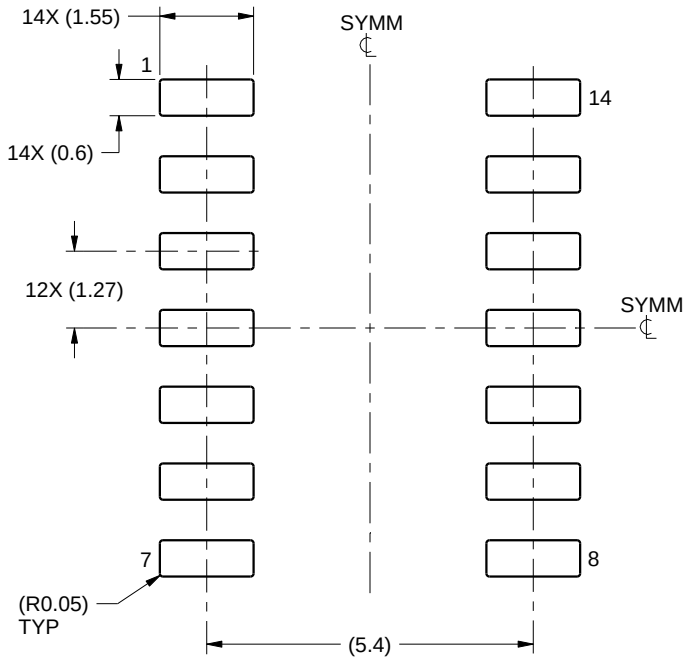
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

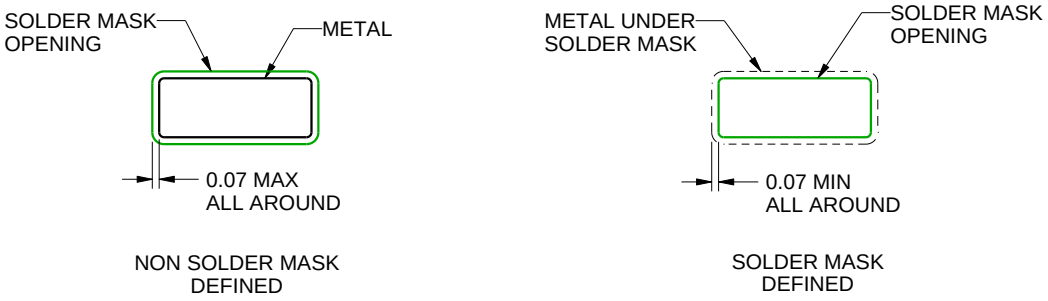


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

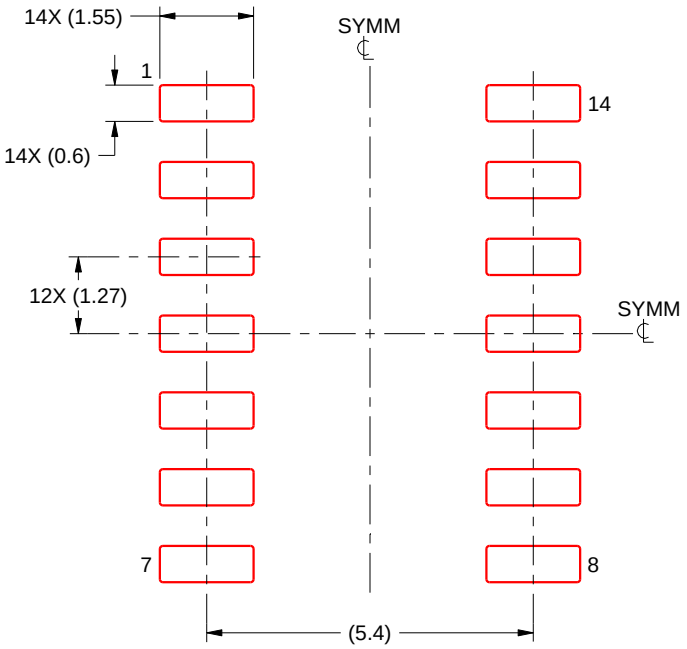
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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