

CDx4HC138、CDx4HCT138、CDx4HC238、CDx4HCT238 ハイスピード CMOS ロジック 3~8 ライン・デコーダ/デマルチプレクサ (反転および非反転)

1 特長

- 8 つのデータ出力のいずれかを選択:
 - '138 はアクティブ LOW
 - '238 はアクティブ HIGH
- I/O ポートまたはメモリ・セレクト
- カスケード接続を簡単にするための 3 つのイネーブル入力
- 13ns の伝搬遅延 (標準値、 $V_{CC} = 5V$ 、 $C_L = 15pF$ 、 $T_A = 25^\circ C$)
- ファンアウト (全温度範囲にわたって)
 - バス・ドライバ出力: 15 の LSTTL 負荷
 - 標準出力: 10 の LSTTL 負荷
- 広い動作温度範囲: $-55^\circ C \sim 125^\circ C$
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V~6V で動作
 - 優れたノイズ耐性: $N_{IL} = V_{CC}$ の 30%、 $N_{IH} = V_{CC}$ の 30% ($V_{CC} = 5V$ の場合)
- HCT タイプ
 - 4.5V~5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{IL} = 0.8V$ (最大値)、 $V_{IH} = 2V$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_L \leq 1\mu A$

2 概要

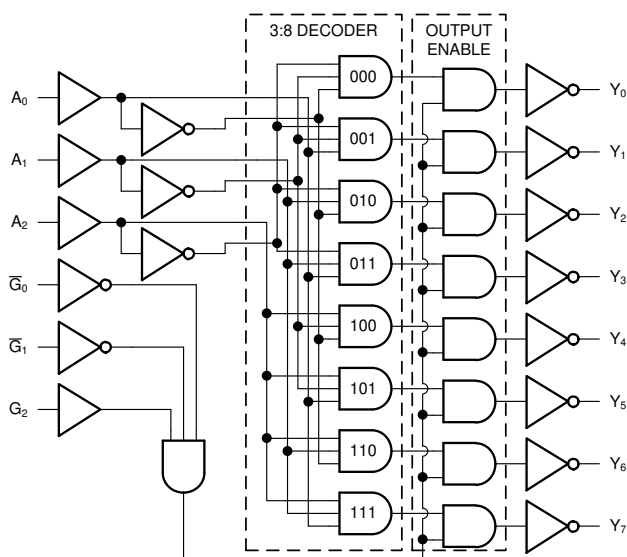
CDx4HC(T)138 および '238 は、1 つの通常の (アクティブ HIGH) 出力ストロブ (G_2) と 2 つのアクティブ LOW 出力ストロブ ($\overline{G}_1$ 、 $\overline{G}_0$) を備えた 3~8 デコーダです。いずれかのストロブ入力により出力が無効化されると、すべての出力は HIGH 状態に強制されます。ストロブ入力により出力が無効化されている場合以外は、選択された出力のみが LOW であり、その他のすべての出力は HIGH です。

CDx4HC(T)238 は、1 つの通常の (アクティブ HIGH) 出力ストロブ (G_2) と 2 つのアクティブ LOW 出力ストロブ ($\overline{G}_1$ 、 $\overline{G}_0$) を備えた 3~8 デコーダです。いずれかのストロブ入力により出力が無効化されると、すべての出力は LOW 状態に強制されます。ストロブ入力により出力が無効化されている場合以外は、選択された出力のみが HIGH であり、その他のすべての出力は LOW です。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD74HC138E	PDIP (16)	25.40mm × 6.35mm
CD74HCT138E	PDIP (16)	25.40mm × 6.35mm
CD74HCT238E	PDIP (16)	25.40mm × 6.35mm
CD74HC138M	SOIC (16)	9.90mm × 3.90mm
CD74HCT238M	SOIC (16)	9.90mm × 3.90mm
CD74HC238NS	SO (16)	10.20mm × 5.30mm
CD74HC238PW	TSSOP (16)	5.00mm × 4.40mm
CD74HCT238PW	TSSOP (16)	5.00mm × 4.40mm
CD54HC138F	CDIP (16)	21.34mm × 6.92mm
CD54HCT138F	CDIP (16)	21.34mm × 6.92mm
CD54HCT238F	CDIP (16)	21.34mm × 6.92mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図 '138



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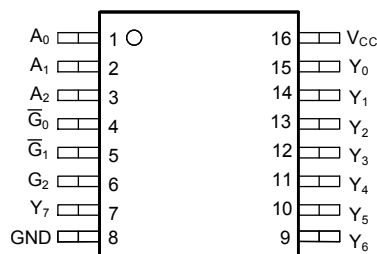
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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision I (August 2004) to Revision J (November 2021)	Page
• 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新.....	1
• 現行の TI の命名規則に合わせてピン名を以下のように更新。E ₃ を G ₂ 、E ₂ を G ₁ 、E ₁ を G ₀	1

4 Pin Configuration and Functions



**J, N, D, NS, or PW package
16-Pin CDIP, PDIP, SOIC, SO, or TSSOP
Top View**

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	A ₀	I	Address select 0
2	A ₁	I	Address select 1
3	A ₂	I	Address select 2
4	$\overline{G}_0$	I	Output strobe 0, active low
5	$\overline{G}_1$	I	Output strobe 1, active low
6	G ₂	I	Output strobe 2
7	Y ₇	O	Output 7
8	GND	—	Ground
9	Y ₆	O	Output 6
10	Y ₅	O	Output 5
11	Y ₄	O	Output 4
12	Y ₃	O	Output 3
13	Y ₂	O	Output 2
14	Y ₁	O	Output 1
15	Y ₀	O	Output 0
16	V _{CC}	—	Positive supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
I_{IK}	Input clamp diode current	For $V_I < 0.5V$ or $V_I > V_{CC} + 0.5V$		± 20 mA
I_{OK}	Output clamp diode current	For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		± 20 mA
I_O	Output source or sink current per output pin	For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		± 25 mA
	Continuous current through V_{CC} or GND			± 50 mA
T_J	Junction temperature			150 °C
T_{stg}	Storage temperature range			-65 150 °C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)			300 °C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	$V_{CC} = 2V$		1000	ns
		$V_{CC} = 4.5V$		500	
		$V_{CC} = 6V$		400	
T_A	Temperature range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		CD74HC(T)138, CD74HC(T)238				UNIT
		N (PDIP)	D (SOIC)	NS (SOP)	PW (TSSOP)	
		16 Pins	16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	67	73	64	108	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	
HC TYPES										
V _{IH}	High-level input voltage		2	1.5		1.5		1.5		V
			4.5	3.15		3.15		3.15		V
			6	4.2		4.2		4.2		V
V _{IL}	Low-level input voltage		2	0.5		0.5		0.5		V
			4.5	1.35		1.35		1.35		V
			6	1.8		1.8		1.8		V
V _{OH}	High-level output voltage	I _{OH} = − 20 μA	2	1.9		1.9		1.9		V
		I _{OH} = − 20 μA	4.5	4.4		4.4		4.4		V
		I _{OH} = − 20 μA	6	5.9		5.9		5.9		V
	High-level output voltage	I _{OH} = − 4 mA	4.5	3.98		3.84		3.7		V
		I _{OH} = − 5.2 mA	6	5.48		5.34		5.2		V
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	2	0.1		0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1		0.1		0.1		V
		I _{OL} = 20 μA	6	0.1		0.1		0.1		V
	Low-level output voltage	I _{OL} = 4 mA	4.5	0.26		0.33		0.4		V
		I _{OL} = 5.2 mA	6	0.26		0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	6	±0.1		±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} or GND	6	8		80		160		μA
HCT TYPES										
V _{IH}	High-level input voltage		4.5 to 5.5	2		2		2		V
V _{IL}	Low-level input voltage		4.5 to 5.5	0.8		0.8		0.8		V
V _{OH}	High-level output voltage	I _{OH} = − 20 μA	4.5	4.4		4.4		4.4		V
	High-level output voltage	I _{OH} = − 4 mA	4.5	3.98		3.84		3.7		V
V _{OL}	Low-level output voltage	I _{OL} = 20 μA	4.5	0.1		0.1		0.1		V
	Low-level output voltage	I _{OH} = 4 mA	4.5	0.26		0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} and GND	5.5	±0.1		±1		±1		μA
I _{CC}	Supply current	V _I = V _{CC} and GND	5.5	8		80		160		μA
ΔI _{CC}	Additional supply current per input pin	A ₀ - A ₂ inputs held at V _{CC} − 2.1 V	4.5 to 5.5	100	540	675		735		μA
		G ₀ and G ₁ inputs held at V _{CC} − 2.1 V	4.5 to 5.5	100	450	562.5		612.5		μA
		G ₂ input held at V _{CC} − 2.1 V	4.5 to 5.5	100	360	450		490		μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics⁽²⁾

Input $t_i = 6\text{ns}$. (See [Parameter Measurement Information](#))

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES												
t _{pd}	Address to output	C _L = 50pF	2	150			190		225		ns	
			4.5	13 ⁽³⁾			30		38			45
		C _L = 50pF	6	26			33		38			
	Strobe $\overline{G}_0$, $\overline{G}_1$, G ₂ to output HC/HCT 138	C _L = 50pF	2	150			190		265		ns	
			4.5	30			38		53			
			6	26			33		45			
t _t	Output transition time	C _L = 50pF	2	75			95		110		MHz	
			4.5	15			19		22			
			6	13			16		19			
C _{pd}	Power dissipation capacitance ⁽¹⁾	C _L = 15pF	5	67							pF	
C _i	Input capacitance			10			10		10		pF	
HCT TYPES												
t _{pd}	Address to output	C _L = 50pF	4.5	14 ⁽³⁾			35		44		53	ns
	Strobe G ₂ to output HC/HCT138	C _L = 50pF	4.5				35		44		53	ns
	Strobe $\overline{G}_0$, $\overline{G}_1$ to output HC/HCT238	C _L = 15pF	4.5				40		50		60	ns
t _t	Output transition time	C _L = 15pF	4.5				15		19		22	
C _{pd}	Power dissipation capacitance ⁽¹⁾	C _L = 15pF	5	67								pF
C _i	Input capacitance			10			10		10			pF

(1) C_{PD} is used to determine the dynamic power consumption, per gate.

(2) For details on power calculation, see [SCAA035B](#)

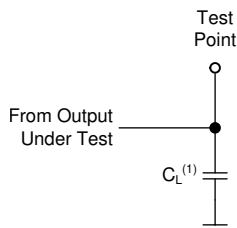
(3) $C_L = 15\text{pF}$ and $V_{CC} = 5$

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

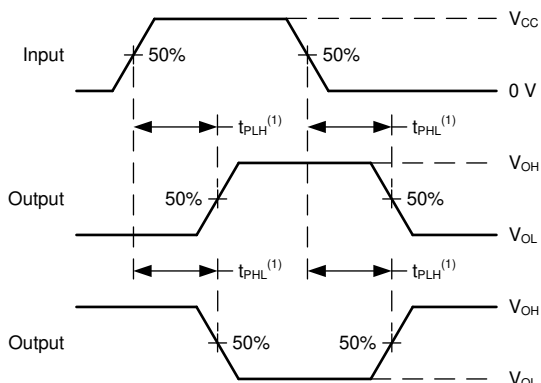
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



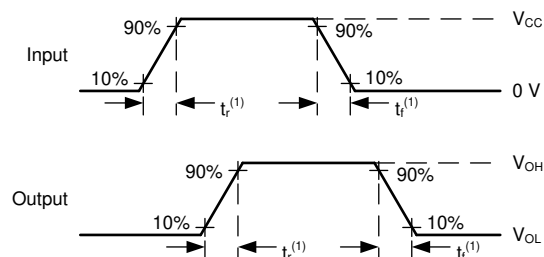
(1) C_L includes probe and test-fixture capacitance.

FIG 6-1. Load Circuit for Push-Pull Outputs



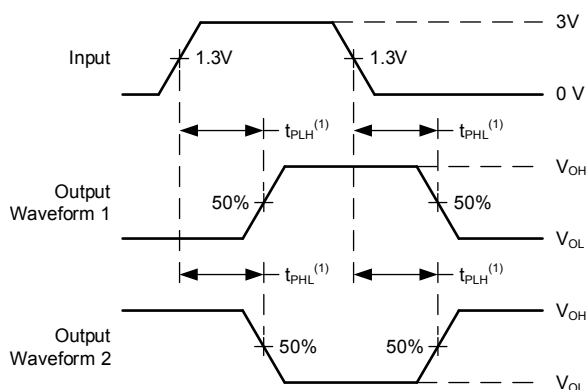
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

FIG 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

FIG 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

FIG 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

7 Detailed Description

7.1 Overview

The CDx4HC(T)138 and '238 are high speed silicon gate CMOS decoders well suited to memory address decoding or data routing applications. They contain a single 3:8 decoder.

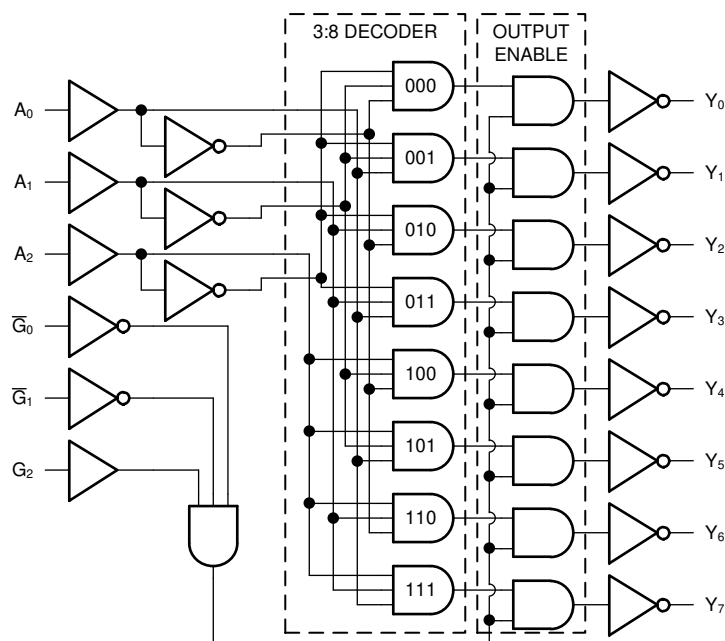
The CDx4HC(T)138 and '238 have three address select inputs (A_2 , A_1 , and A_0). The circuit functions as a normal one-of-eight decoder.

Three strobe inputs (G_2 , $\overline{G}_1$ and $\overline{G}_0$) are provided to simplify cascading and to facilitate demultiplexing. When any input strobe is active, all outputs are forced into the high state for the '138 function. When any input strobe is active, all outputs are forced into the low state for the '238 function.

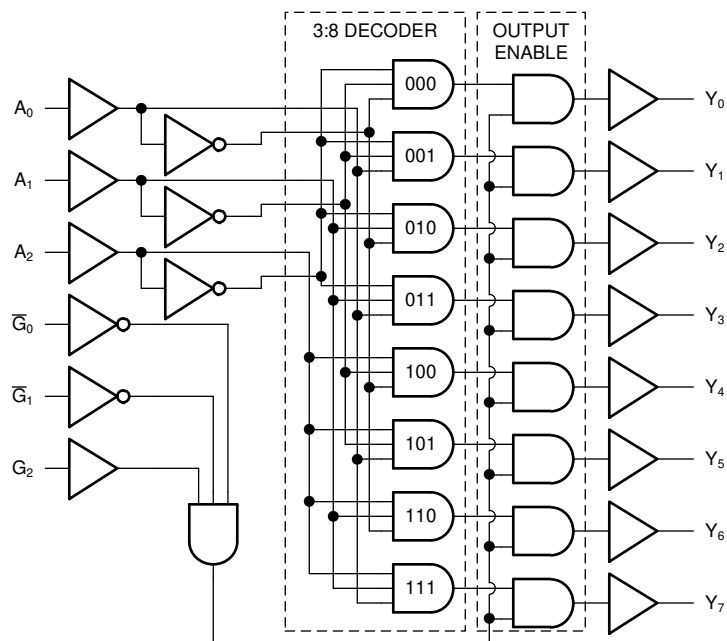
The demultiplexing function is accomplished by first using the select inputs to choose the desired output, and then using one of the strobe inputs as the data input.

The outputs for the CDx4HC(T)138 are normally low when selected. The outputs for the CDxHC(T)238 are normally high when selected.

7.2 Functional Block Diagram



7-1. Functional Block Diagram '138



7-2. Functional Block Diagram '238

7.3 Device Functional Modes

表 7-1. Function Table 'HC138, 'HCT138

INPUTS						OUTPUTS							
STROBE			ADDRESS										
G2	G1	G0	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

表 7-2. Function Table 'HC238, 'HCT238

INPUTS						OUTPUTS							
STROBE			ADDRESS										
G2	G1	G0	A ₂	A ₁	A ₀	Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8688401EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688401EA CD54HC238F3A
CD54HC138F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC138F
CD54HC138F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC138F
CD54HC138F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8406201EA CD54HC138F3A
CD54HC138F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8406201EA CD54HC138F3A
CD54HC238F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688401EA CD54HC238F3A
CD54HC238F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8688401EA CD54HC238F3A
CD54HCT138F	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT138F
CD54HCT138F.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT138F
CD54HCT138F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550401EA CD54HCT138F3A
CD54HCT138F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550401EA CD54HCT138F3A
CD54HCT238F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974501EA CD54HCT238F3A
CD54HCT238F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974501EA CD54HCT238F3A
CD74HC138E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC138E
CD74HC138E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC138E
CD74HC138M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC138M
CD74HC138M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC138M
CD74HC138M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M
CD74HC138M96E4	Active	Production	null (null)	2500 LARGE T&R	-	Call TI	Call TI	-55 to 125	
CD74HC138M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M
CD74HC138M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC138M
CD74HC138MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC138M

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD74HC238E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC238E
CD74HC238E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC238E
CD74HC238EE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC238E
CD74HC238M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC238M
CD74HC238M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238M961G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238M961G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HC238M
CD74HC238NSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238NSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC238M
CD74HC238PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ238
CD74HC238PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HJ238
CD74HC238PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ238
CD74HC238PWR1G4	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ238
CD74HC238PWT	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HJ238
CD74HCT138E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT138E
CD74HCT138E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT138E
CD74HCT138M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT138M
CD74HCT138M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT138M
CD74HCT138M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT138M
CD74HCT238E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT238E
CD74HCT238E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT238E
CD74HCT238M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT238M
CD74HCT238M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT238M
CD74HCT238M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT238M
CD74HCT238PW	Obsolete	Production	TSSOP (PW) 16	-	-	Call TI	Call TI	-55 to 125	HK238
CD74HCT238PWR	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HK238
CD74HCT238PWR.A	Active	Production	TSSOP (PW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK238

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC138, CD54HC238, CD54HCT138, CD54HCT238, CD74HC138, CD74HC238, CD74HCT138, CD74HCT238 :

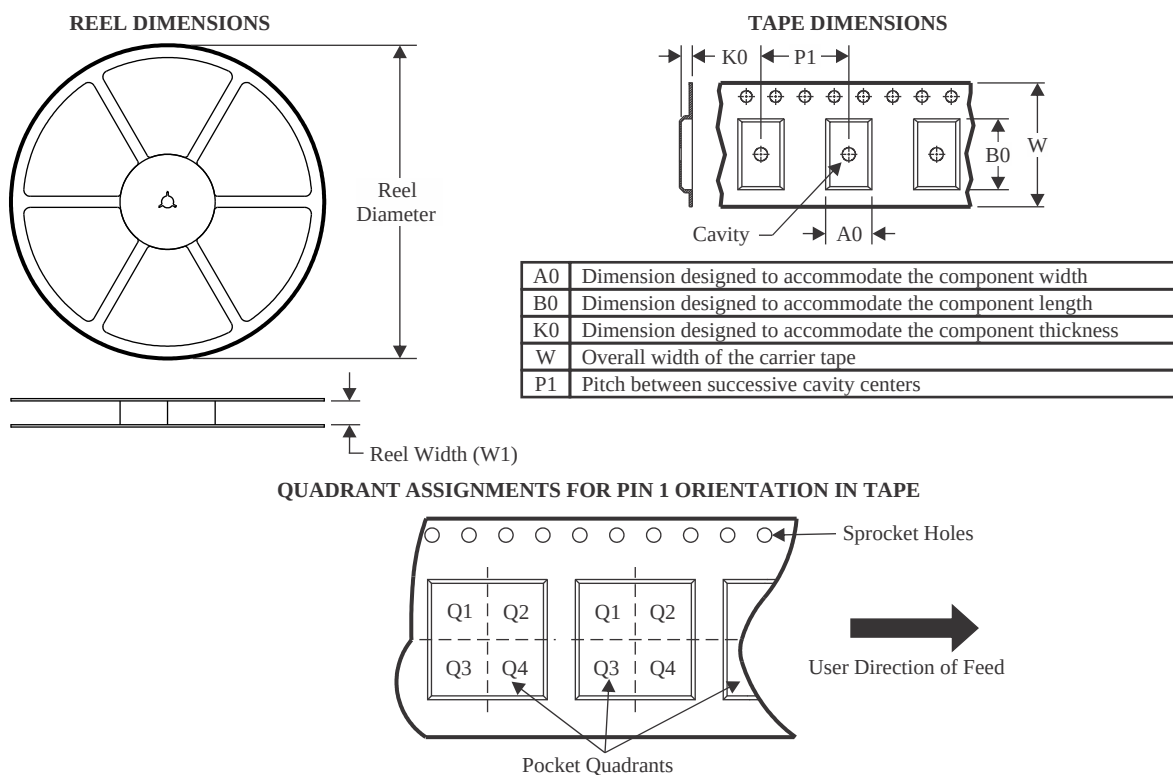
- Catalog : [CD74HC138](#), [CD74HC238](#), [CD74HCT138](#), [CD74HCT238](#)
- Automotive : [CD74HC138-Q1](#), [CD74HC138-Q1](#)
- Military : [CD54HC138](#), [CD54HC238](#), [CD54HCT138](#), [CD54HCT238](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

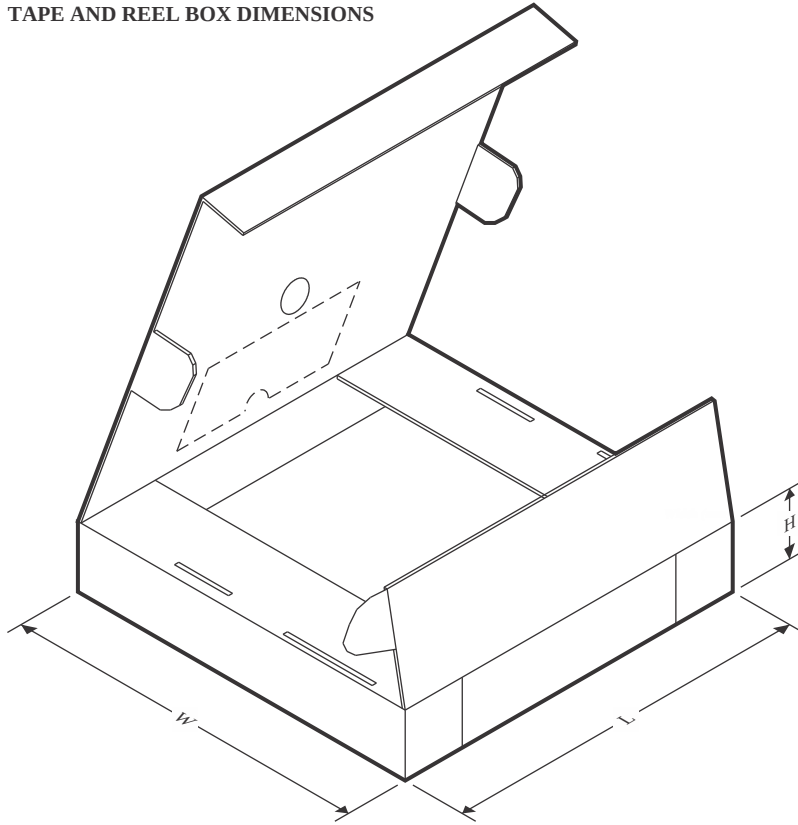
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC138M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238M961G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC238NSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.3	1.6	8.0	12.0	Q1
CD74HC238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC238PWR1G4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HCT138M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT238PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

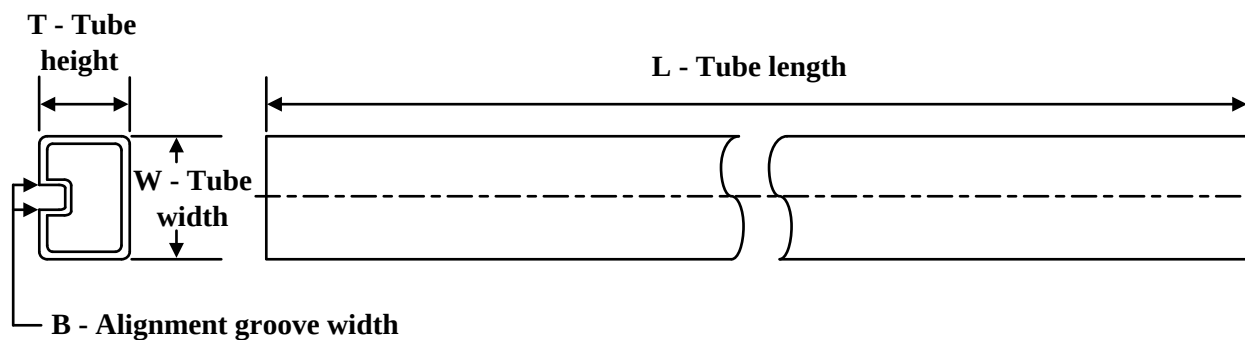
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC138M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC138M96G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC238M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC238M96	SOIC	D	16	2500	340.5	336.1	32.0
CD74HC238M961G4	SOIC	D	16	2500	353.0	353.0	32.0
CD74HC238NSR	SOP	NS	16	2000	353.0	353.0	32.0
CD74HC238PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HC238PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC238PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
CD74HC238PWR1G4	TSSOP	PW	16	2000	356.0	356.0	35.0
CD74HCT138M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT238M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT238PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC238EE4	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT138E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT238E.A	N	PDIP	16	25	506	13.97	11230	4.32



SOP - 2.00 mm max height

SOP

NS0016A



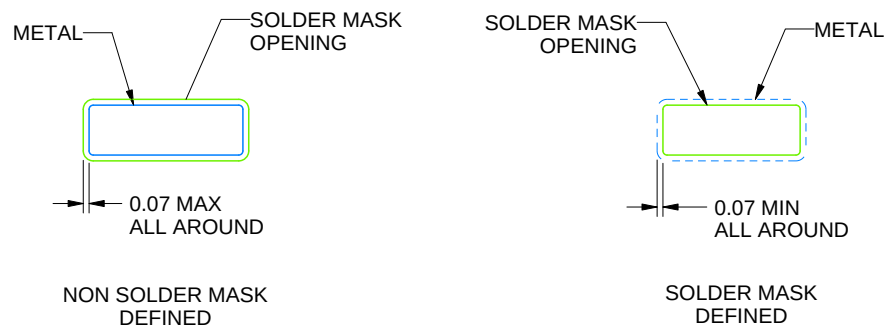
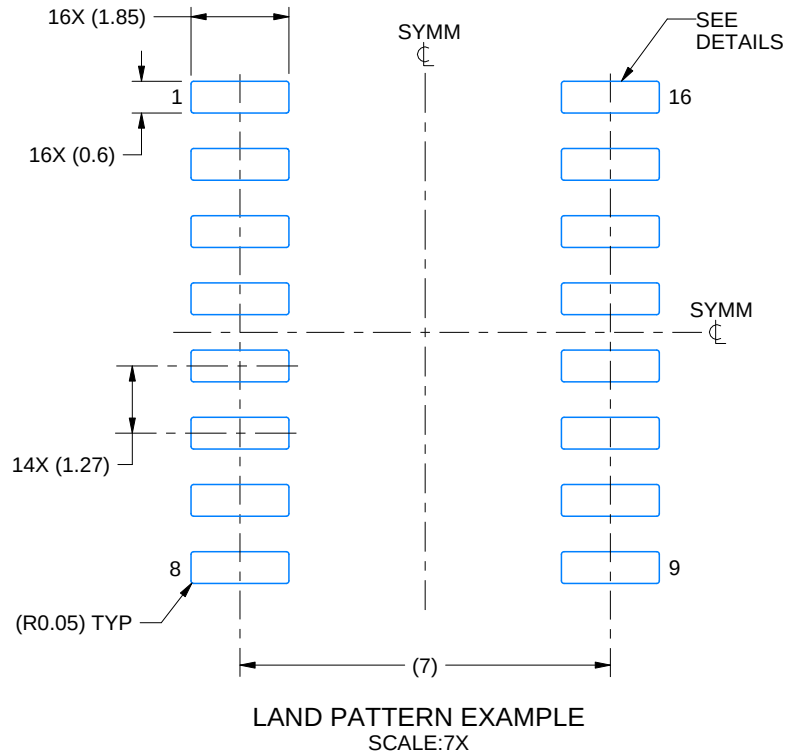
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



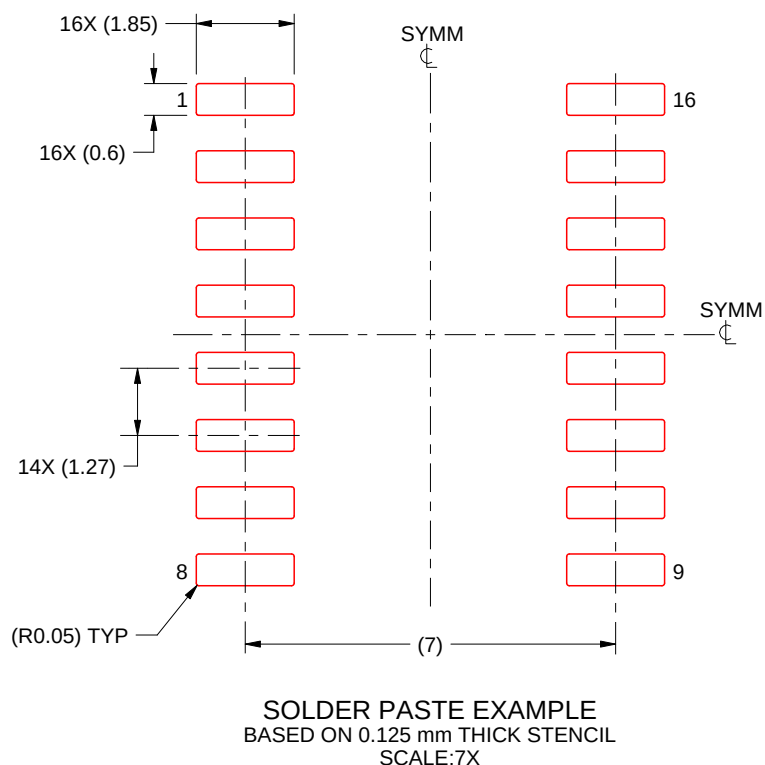
SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



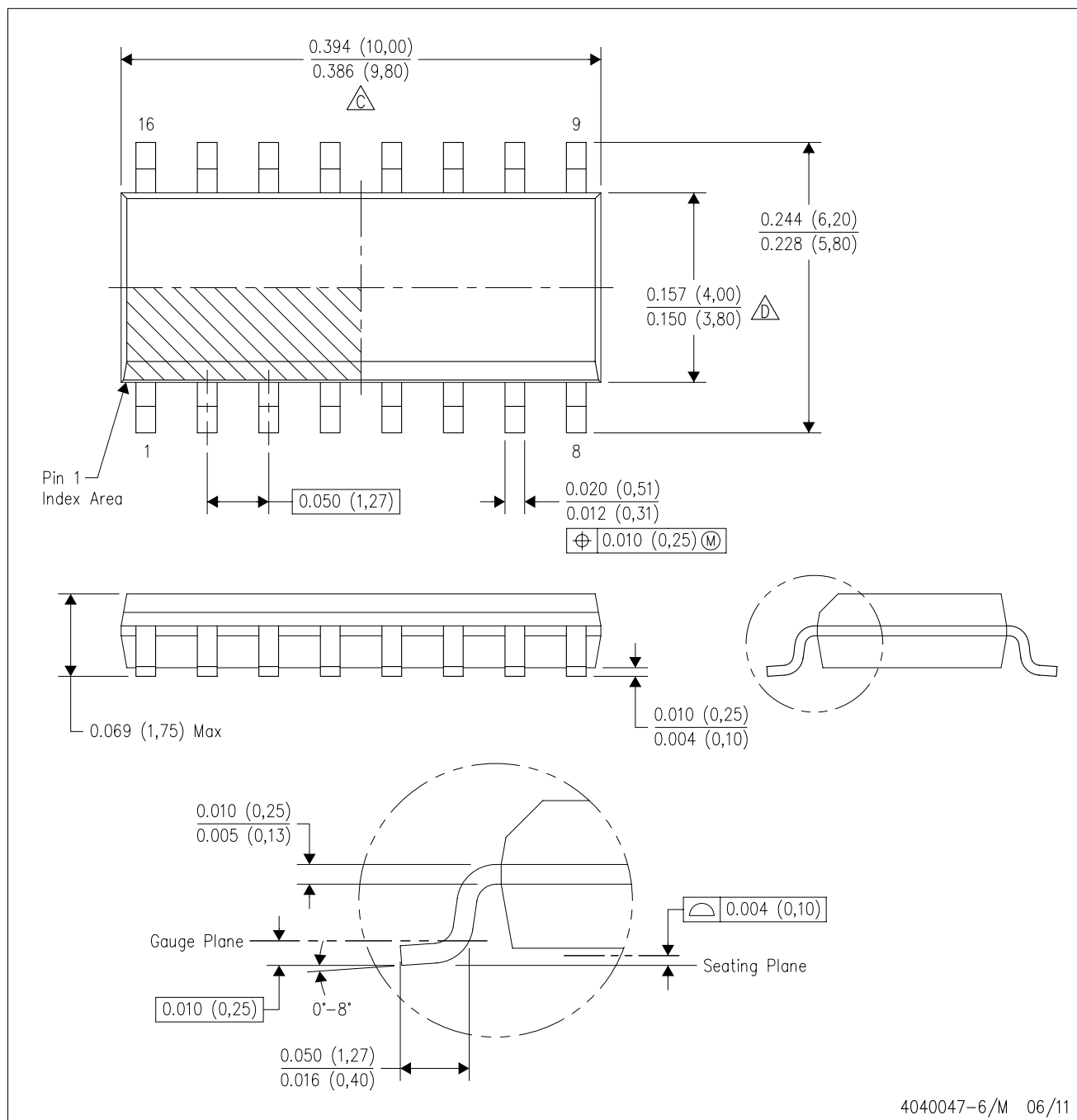
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

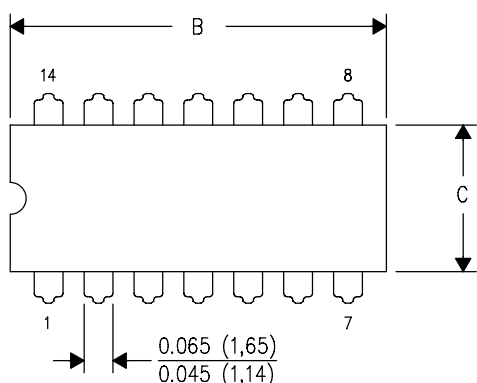


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

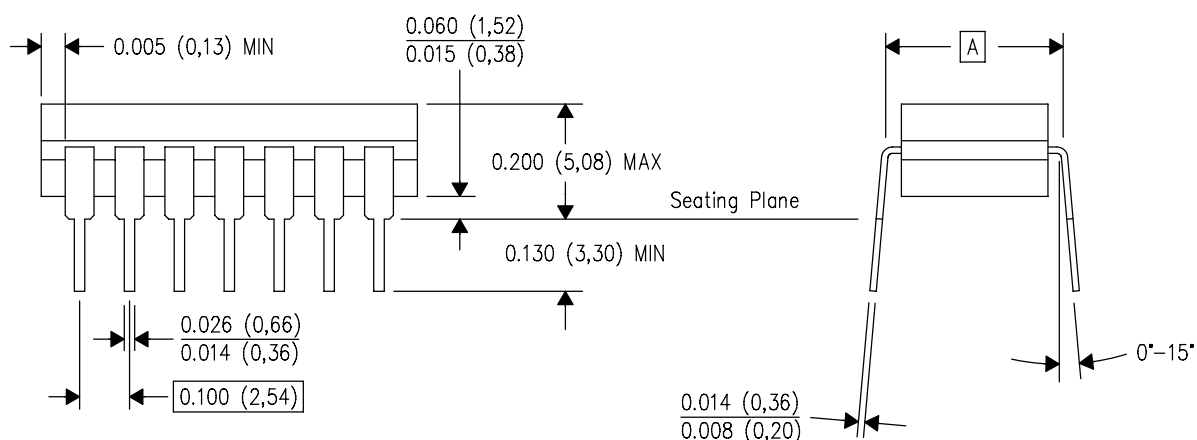
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE

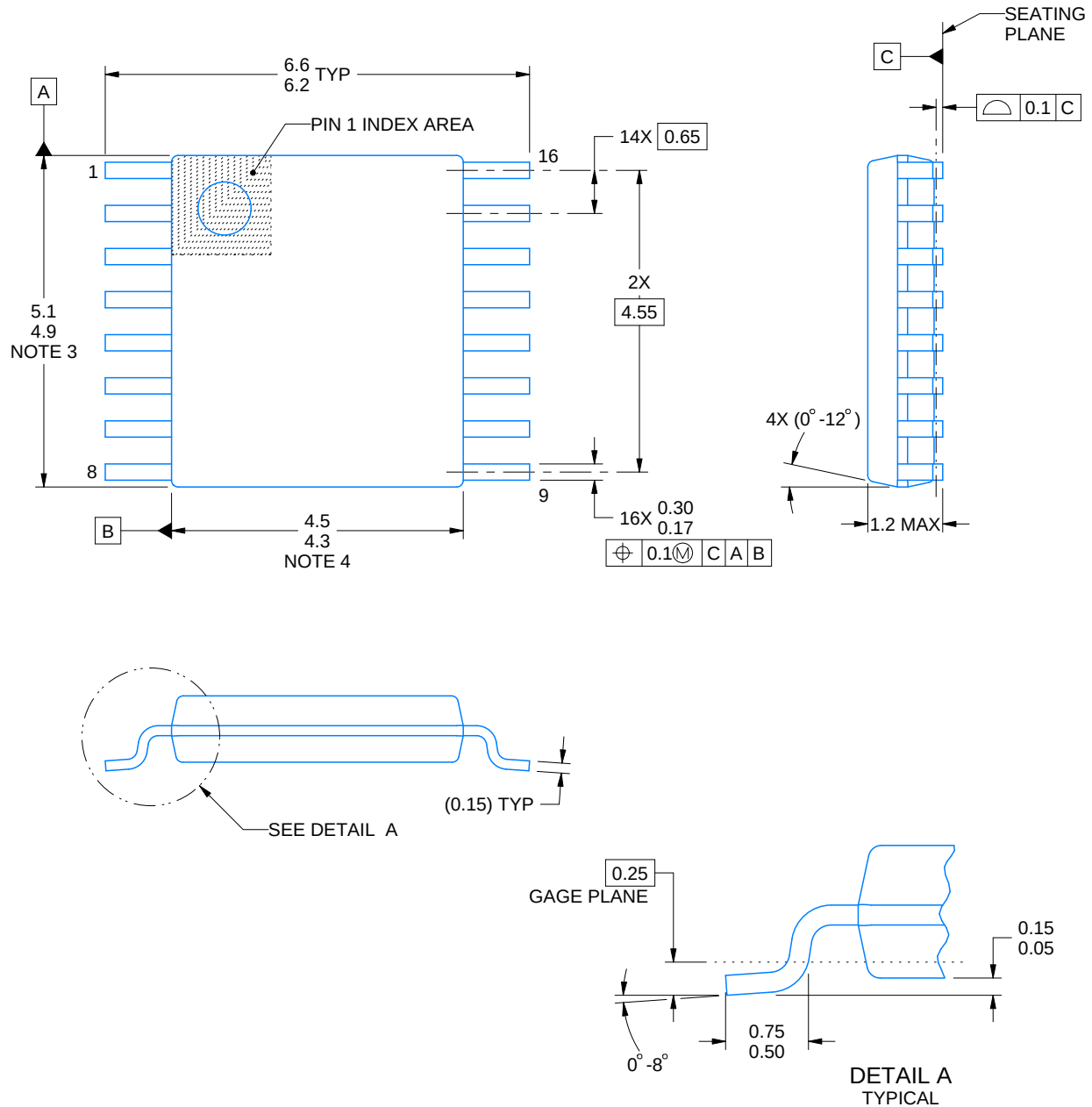
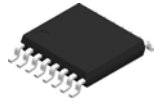


PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



4220204/B 12/2023

NOTES:

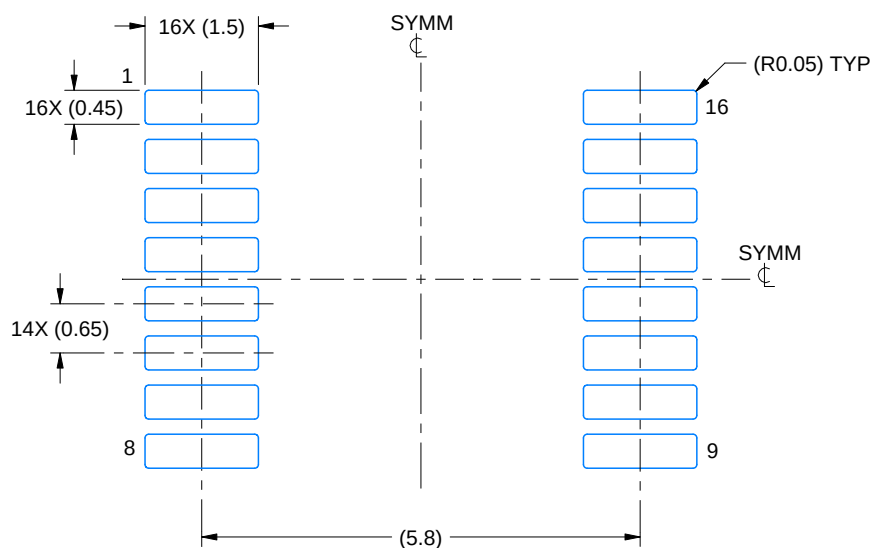
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

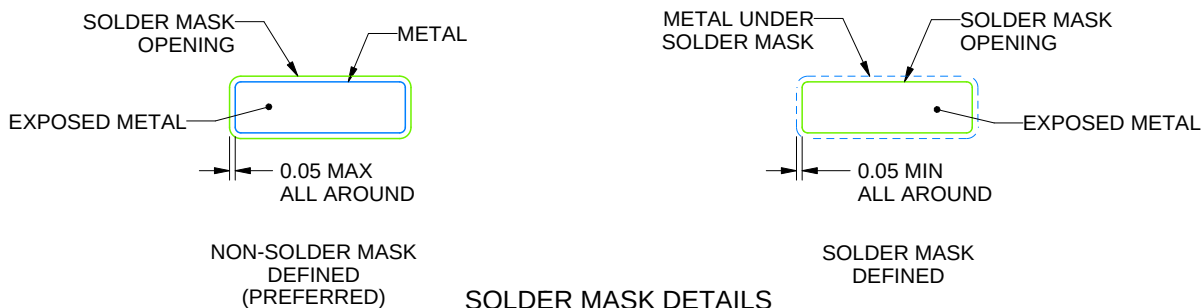
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

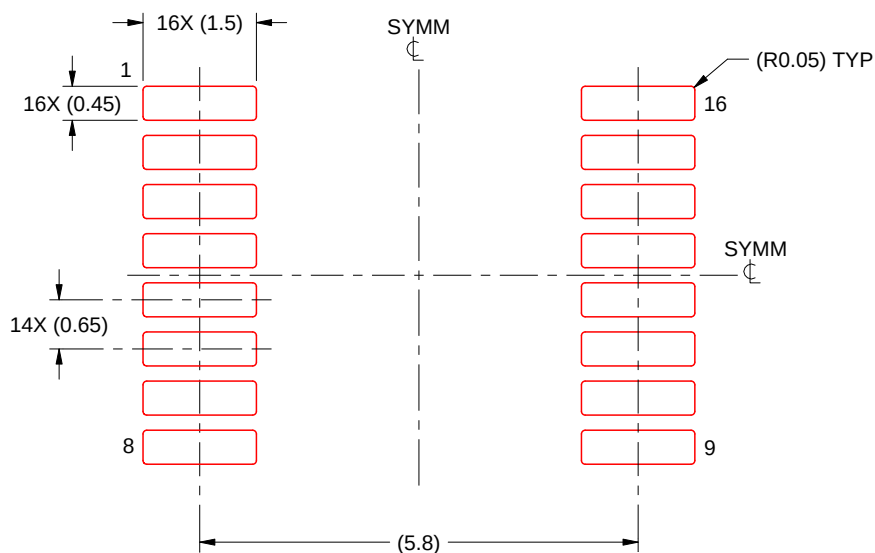
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

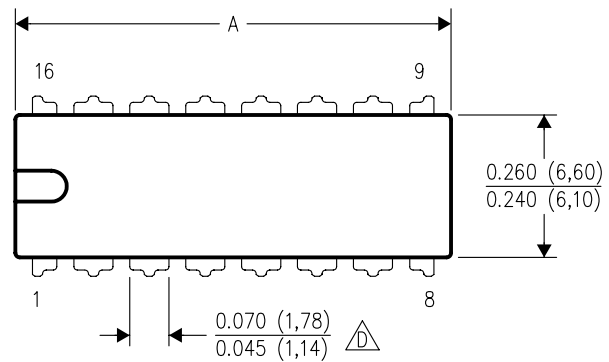
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

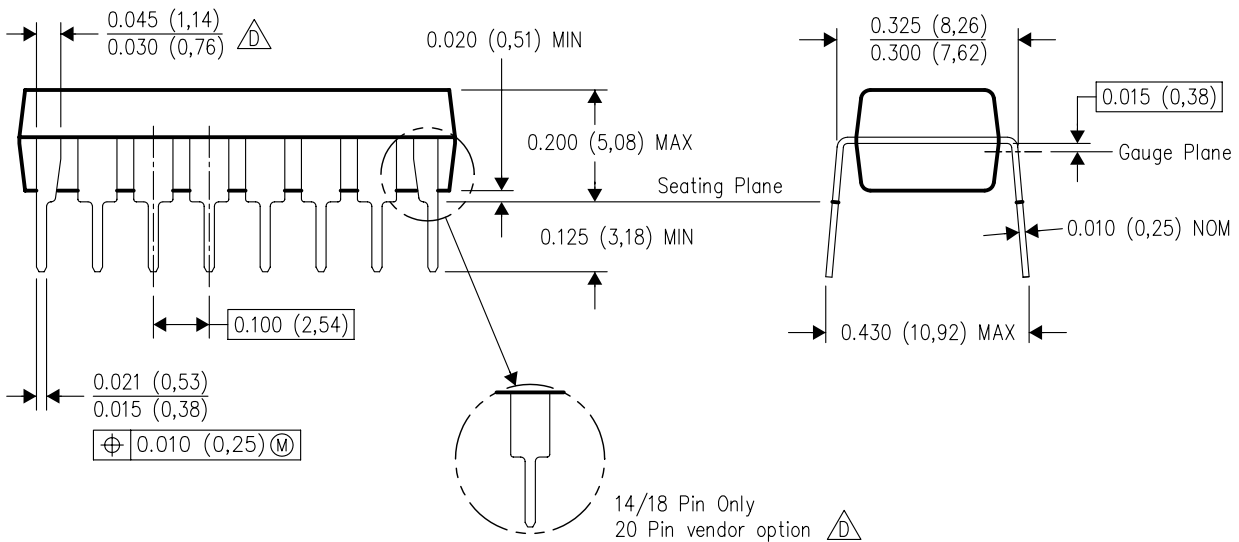
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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