



CD54HC283, CD74HC283, CD54HCT283, CD74HCT283

JAJSOX9E – NOVEMBER 1997 – REVISED JULY 2022

ハイスピード CMOS ロジック、高速桁上がり機能搭載、4 ビット、2 進全加算器

1 特長

- 2 つの 2 進数を加算
- 完全内部ルックアヘッド
- 高速リップル・キャリーによる経済的な拡張
- 正ロジックと負ロジックの両方で動作
- ファンアウト (全温度範囲にわたって)
 - 標準出力は 10 個の LSTTL 負荷を駆動可能
 - バス・ドライバ出力は 15 個の LSTTL 負荷を駆動可能
- 広い動作温度範囲: -55°C ~ 125°C
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V ~ 6V で動作
 - 優れたノイズ耐性: V_{CC} に対して $N_{\text{IL}} = 30\%$ 、 $N_{\text{IH}} = 30\%$ ($V_{\text{CC}} = 5\text{V}$ 時)
- HCT タイプ
 - 4.5V ~ 5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{\text{IL}} = 0.8\text{V}$ (最大値)、 $V_{\text{IH}} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_{\text{I}} \leq 1\mu\text{A}$

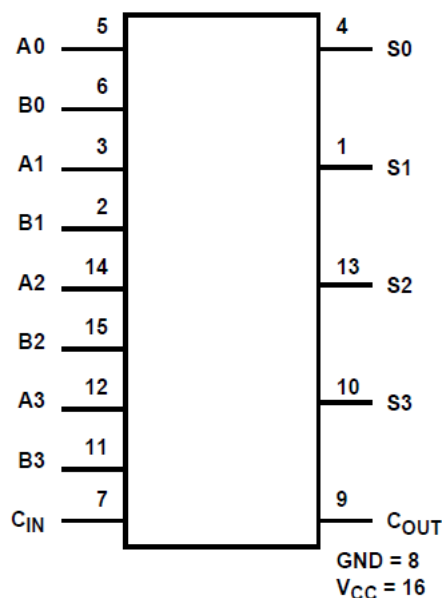
2 概要

CDx4HC283 および CDx4HCT283 は、4 ビットのバイナリ加算器を内蔵しています。CDx4HCT283 は TTL 電圧互換入力を備えています。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC283	J (CDIP) (16)	24.38mm × 6.92mm
CD74HC283CD74HC283	D (SOIC) (16)	9.90mm × 3.90mm
	N (PDIP) (16)	19.31mm × 6.35mm
CD74HCT283CD74HCT283	D (SOIC) (16)	9.90mm × 3.90mm
	N (PDIP) (16)	19.31mm × 6.35mm

(1) すべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム



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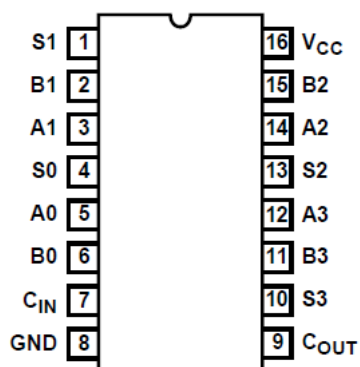
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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2003) to Revision E (July 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....	1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		– 0.5	7	V
I _{IK}	Input diode current	For V _I < –0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output diode current	For V _O < –0.5 V or V _O > V _{CC} + 0.5 V		±20	mA
I _O	Drain current, per output	For –0.5 V < V _O < V _{CC} + 0.5 V		±25	mA
I _O	Output source or sink current per output pin	For V _O > –0.5 V or V _O < V _{CC} + 0.5 V		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (Soldering 10s)(SOIC - lead tips only)			300	°C

- (1) Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	HC types	2	6	V
V _I , V _O	DC input or output voltage		0	V _{CC}	V
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Temperature range		–55	125	V

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	UNIT
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	73	67	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V _{OH}	High level output voltage	I _{OH} = –20 µA	2	1.9			1.9		1.9		V
		I _{OH} = –20 µA	4.5	4.4			4.4		4.4		
		I _{OH} = –20 µA	6	5.9			5.9		5.9		
		I _{OH} = –4 mA	4.5	3.98			3.84		3.7		V
		I _{OH} = –5.2 mA	6	6			5.34		5.2		
V _{OL}	Low level output voltage	I _{OL} = 20 µA	2	0.1			0.1		0.1		V
		I _{OL} = 20 µA	4.5	0.1			0.1		0.1		
		I _{OL} = 20 µA	6	0.1			0.1		0.1		
		I _{OL} = 4 mA	4.5	0.26			0.33		0.4		V
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		
I _I	Input leakage current	V _{CC} or GND	6	±0.1			±1		±1		µA
I _{CC}	Supply current	V _{CC} or GND	6	8			80		160		µA
HCT Types											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level output voltage	I _{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
V _{OH}		I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V _{OL}	Low level output voltage	I _{OL} = 20 µA	4.5	0.1			0.1		0.1		V
V _{OL}		I _{OL} = 4 mA	4.5	0.26			0.33		0.4		V
I _I	Input leakage current	V _{CC} to GND	5.5	±0.1			±1		±1		µA
I _{CC}	Supply current	V _{CC} or GND	5.5	8			80		160		µA
ΔI _{CC} ⁽¹⁾	Additional supply current per input pin	C _{IN} input held at V _{CC} – 2.1	4.5 to 5.5	100 540			675		735		µA
		B1, A1, A0 inputs held at V _{CC} – 2.1	4.5 to 5.5	100 360			450		490		µA
		B0 input held at V _{CC} – 2.1	4.5 to 5.5	100 144			180		196		µA
		B3, A3, A2, B2 inputs held at V _{CC} – 2.1	4.5 to 5.5	100 180			225		245		µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Switching Characteristics

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			–40 to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t _{PLH} , t _{PHL}	Propagation delay C _{IN} to S0	C _L = 50 pF	2	160			200		240		ns
			4.5	32			40		45		
		C _L = 15 pF	5	13							
		C _L = 50 pF	6	27			34		41		
t _{PLH} , t _{PHL}	C _{IN} to S1	C _L = 50 pF	2	180			225		270		ns
			4.5	36			45		54		
		C _L = 15 pF	5	15							
		C _L = 50 pF	6	31			38		46		
t _{PLH} , t _{PHL}	C _{IN} to S2, C _{IN} to C _{OUT}	C _L = 50 pF	2	195			245		295		ns
			4.5	39			49		59		
		C _L = 15 pF	5	16							
		C _L = 50 pF	6	33			42		50		
t _{PLH} , t _{PHL}	C _{IN} to S3	C _L = 50 pF	2	230			290		345		ns
			4.5	46			58		69		
		C _L = 15 pF	5	19							
		C _L = 50 pF	6	39			49		59		
t _{PLH} , t _{PHL}	An, Bn to C _{OUT}	C _L = 50 pF	2	195			245		295		ns
			4.5	39			49		59		
		C _L = 15 pF	5	16							
		C _L = 50 pF	6	33			42		50		
t _{PLH} , t _{PHL}	An, Bn to Sn	C _L = 50 pF	2	210			265		315		ns
			4.5	42			53		63		
		C _L = 15 pF	5	18							
		C _L = 50 pF	6	36			45		54		
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		
			6	13			16		19		
C _{IN}	Input capacitance	C _L = 50 pF	-	10			10		10		pF
C _{PD}	Power dissipation capacitance ^{(1) (2)}		5	70							pF
HCT TYPES											
t _{PLH} , t _{PHL}	Propagation delay C _{IN} to S0	C _L = 15 pF	5	13							ns
		C _L = 50 pF	4.5	31			39		47		
t _{PLH} , t _{PHL}	C _{IN} to S1	C _L = 15 pF	5	18							ns
		C _L = 50 pF	4.5	43			54		65		
t _{PLH} , t _{PHL}	C _{IN} to S2, C _{IN} to C _{OUT}	C _L = 15 pF	5	19							ns
		C _L = 50 pF	4.5	46			58		69		
t _{PLH} , t _{PHL}	C _{IN} to S3	C _L = 15 pF	5	22							ns
		C _L = 50 pF	4.5	53			66		80		
t _{PLH} , t _{PHL}	An, Bn to C _{OUT}	C _L = 15 pF	5	20							ns
		C _L = 50 pF	4.5	48			60		72		
t _{PLH} , t _{PHL}	An, Bn to Sn	C _L = 15 pF	5	21							ns
		C _L = 50 pF	4.5	49			61		74		

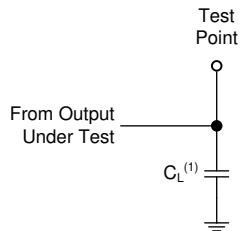
5.5 Switching Characteristics (continued)

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			–40 to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	4.5			15		19		22	ns
C _{IN}	Input capacitance					10		10		10	pF
C _{PD}	Power dissipation capacitance ^{(1) (2)}		5		82						pF

(1) C_{PD} is used to determine the dynamic power consumption, per package.

(2) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information



1. Includes probe and test-fixture capacitance.

FIG 6-1. Load Circuit for Push-Pull Output

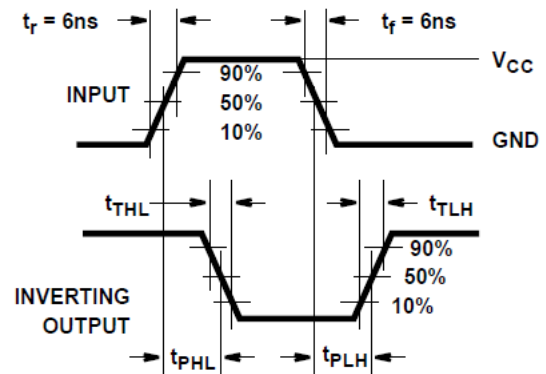


FIG 6-2. HC and HCT Transition Times and Propagation Delay Times, Combination Logic

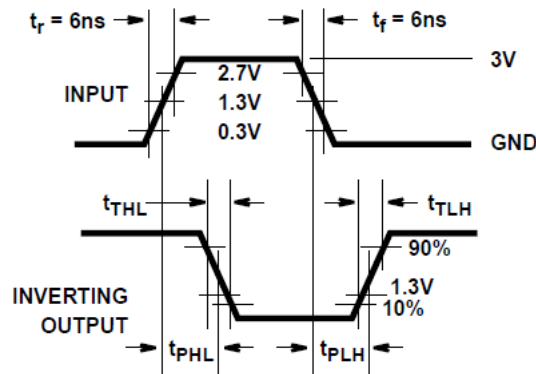


FIG 6-3. HCT Transition Times and Propagation Delay Times, Combination Logic

1. The greater between t_{r_i} and t_{f_i} is the same as t_{r_i} .
2. The greater between $t_{p_{lh}}$ and $t_{p_{hl}}$ is the same as $t_{p_{d_i}}$.

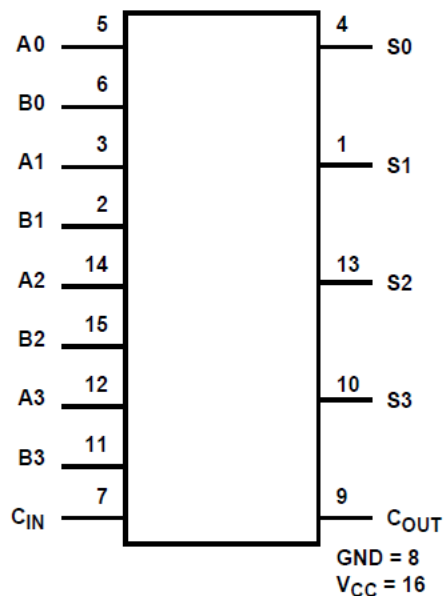
7 Detailed Description

7.1 Overview

The 'HC283 and 'HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

7.2 Functional Block Diagram



7.3 Feature Description

- Balanced CMOS Push-Pull Outputs
- Clamp Diode Structure

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8976501EA	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A
CD54HC283F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A
CD54HC283F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A
CD54HCT283F3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT283F3A
CD54HCT283F3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT283F3A
CD74HC283E	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC283E
CD74HC283E.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC283E
CD74HC283M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC283M
CD74HC283M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M
CD74HC283M96G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M
CD74HC283M96G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M
CD74HCT283E	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT283E
CD74HCT283E.A	NRND	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT283E
CD74HCT283M	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT283M
CD74HCT283M96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HCT283M
CD74HCT283M96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M
CD74HCT283M961G4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M
CD74HCT283M961G4.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M
CD74HCT283MT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	HCT283M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

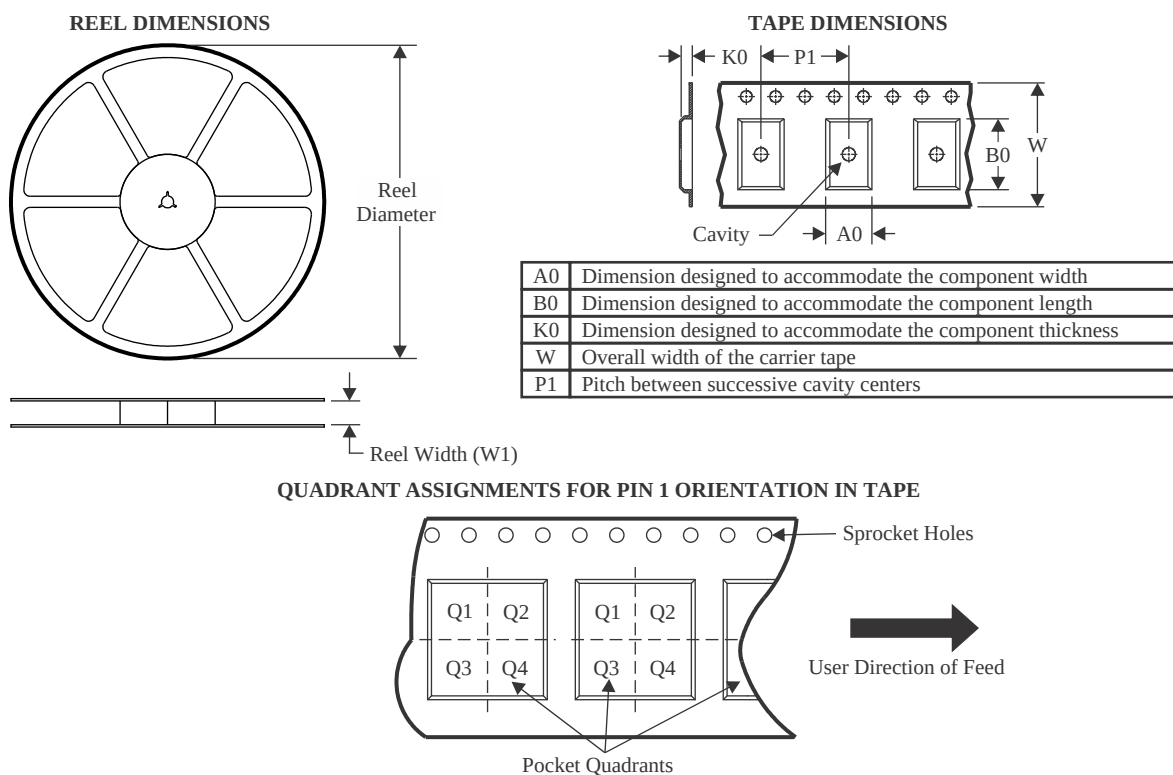
OTHER QUALIFIED VERSIONS OF CD54HC283, CD54HCT283, CD74HC283, CD74HCT283 :

- Catalog : [CD74HC283](#), [CD74HCT283](#)
- Military : [CD54HC283](#), [CD54HCT283](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

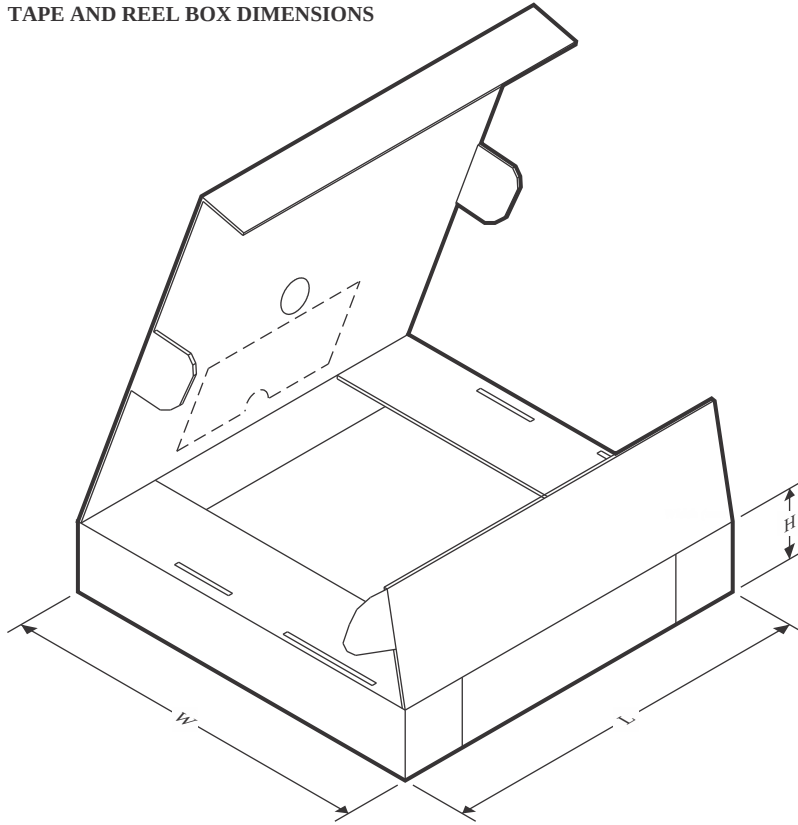
TAPE AND REEL INFORMATION



*All dimensions are nominal

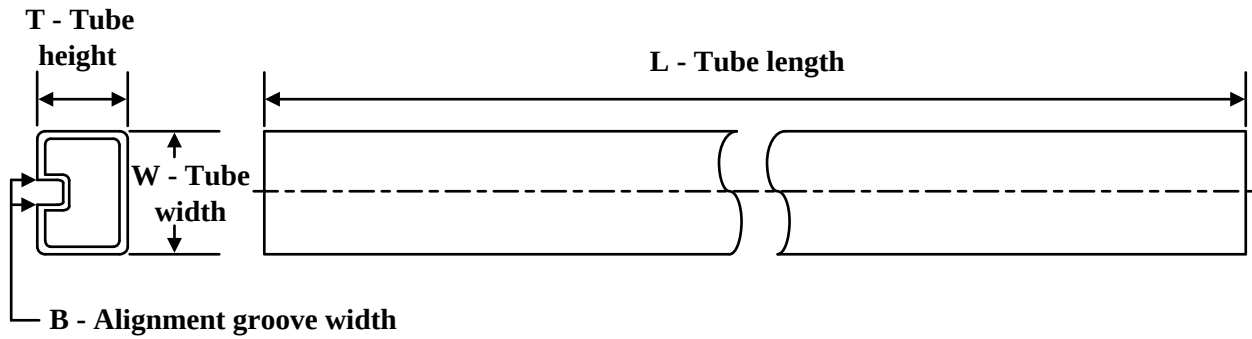
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT283M961G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT283M96	SOIC	D	16	2500	366.0	364.0	50.0
CD74HCT283M96	SOIC	D	16	2500	353.0	353.0	32.0
CD74HCT283M961G4	SOIC	D	16	2500	353.0	353.0	32.0

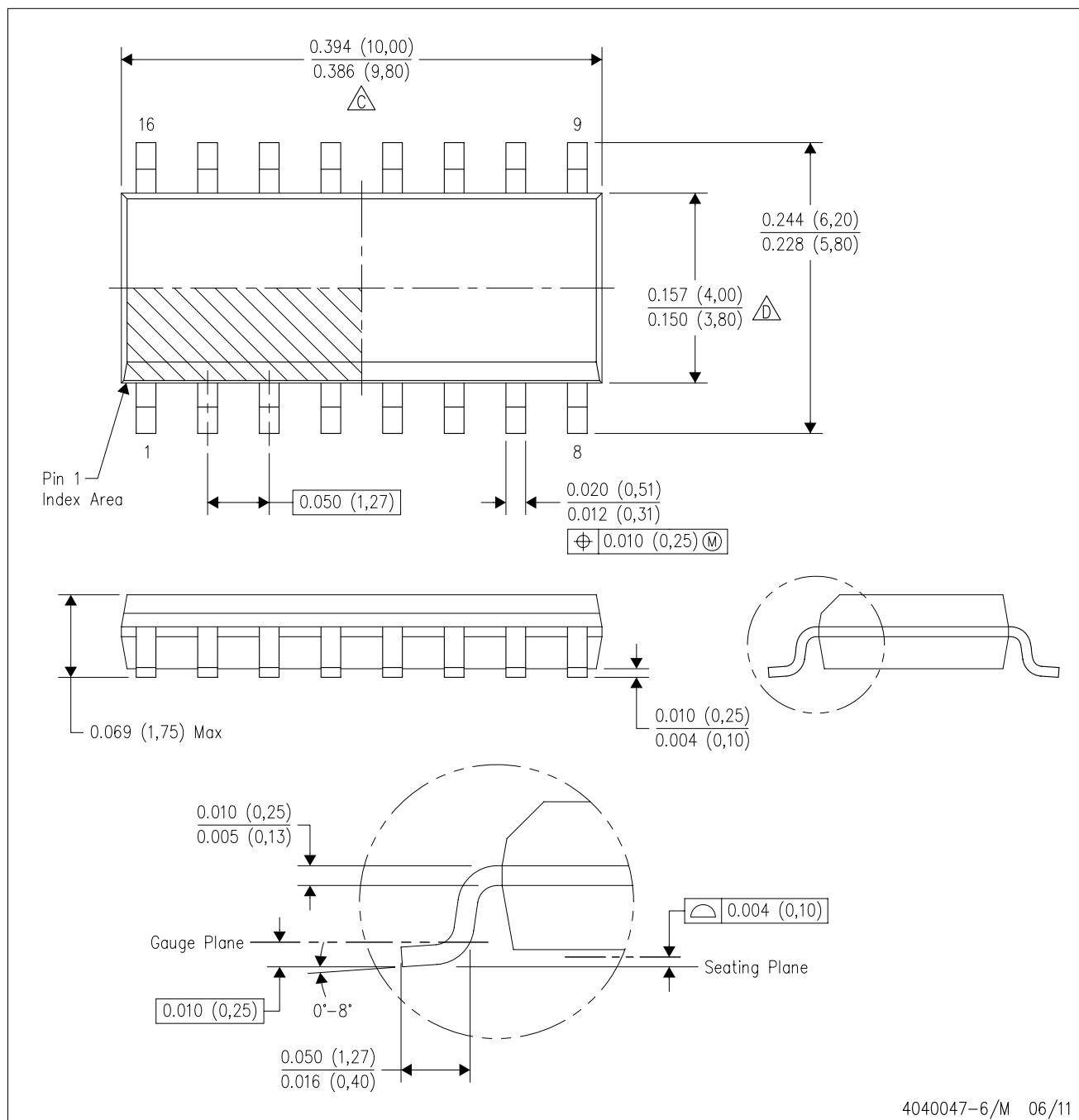
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E.A	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT283E.A	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



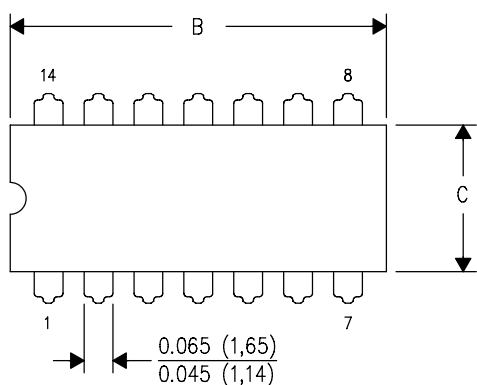
4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

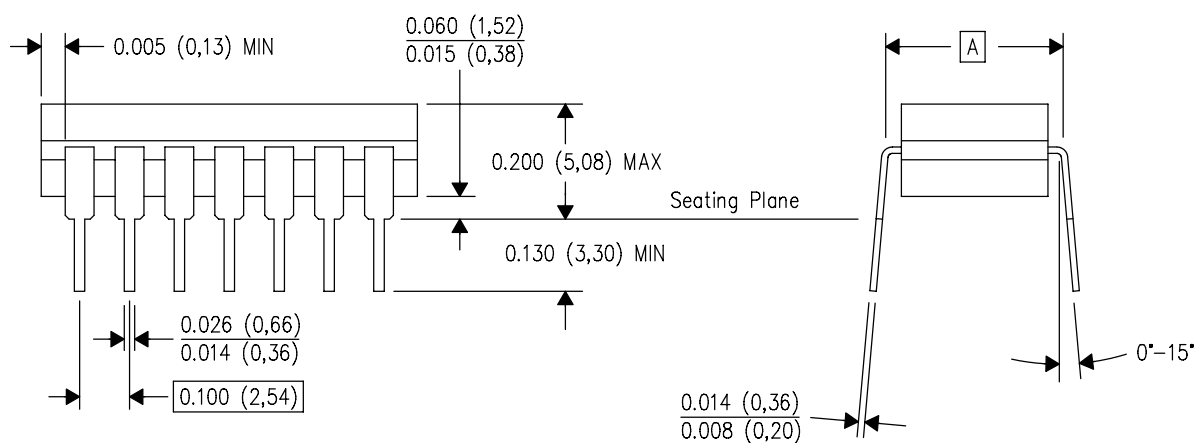
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



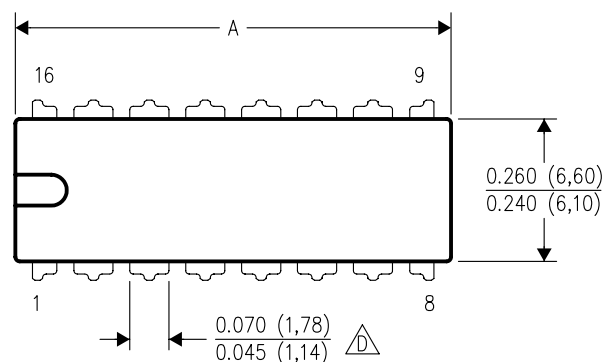
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

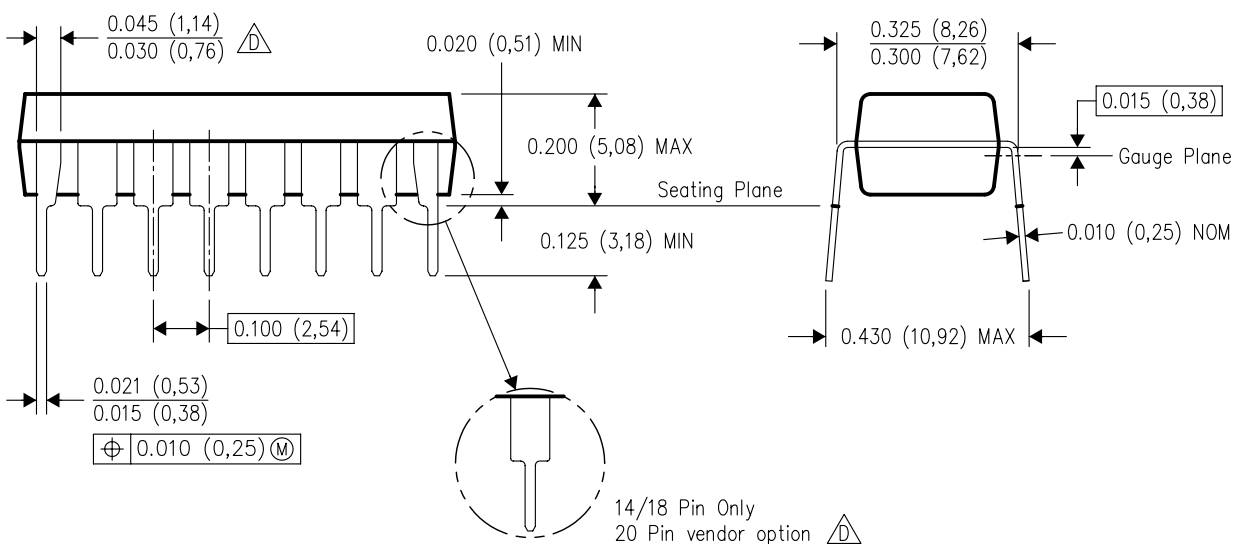
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

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