TEXAS INSTRUMENTS
CD54HC373, CD74HC373
JAJSNS9C – FEBRUARY 2001 – REVISED MAY 2022

CDx4HC373 3 ステート出力、オクタル・トランスペアレント D タイプ・ラッチ

1 特長

- 2V～6V の V_{CC} で動作
- 広い動作温度範囲:-55℃～125℃
- 平衡な伝搬遅延と遷移時間
- 標準出力は最大 15 の LS-TTL 負荷を駆動
- LS-TTL ロジック IC に比べて消費電力を大幅削減

2 概要

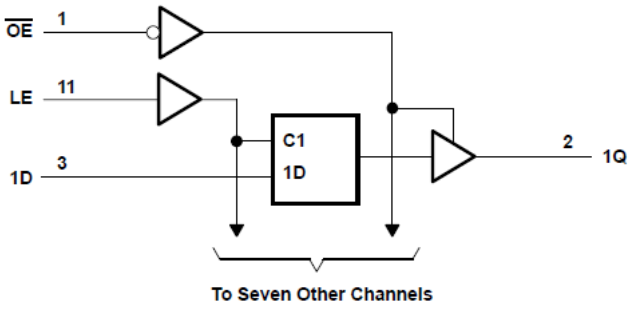
HC373 デバイスは、2V～6V の V_{CC} で動作するように設計されたオクタル・トランスペアレント D タイプ・ラッチです。

ラッチ・イネーブル (LE) 入力が HIGH の場合、Q 出力はデータ (D) 入力に従います。LE を LOW にすると、D 入力のロジック・レベルで Q 出力がラッチされます。

製品情報

部品番号	パッケージ[1]	本体サイズ (公称)
CD74HC373M	SOIC (20)	12.80mm × 7.50mm
CD74HC373E	PDIP (20)	25.40mm × 6.35mm
CD54HC373F	CDIP (20)	26.92mm × 6.92mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 概要 ... 1
3 Revision History ... 2
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 Recommended Operating Conditions(1) ... 4
5.3 Thermal Information ... 4
5.4 Electrical Characteristics ... 5
5.5 Timing Requirements ... 5
5.6 Switching Characteristics ... 6
5.7 Operating Characteristics ... 6
6 Parameter Measurement Information ... 7
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Device Functional Modes ... 8
8 Power Supply Recommendations ... 9
9 Layout ... 9
9.1 Layout Guidelines ... 9
10 Device and Documentation Support ... 10
10.1 Receiving Notification of Documentation Updates ... 10
10.2 サポート・リソース ... 10
10.3 Trademarks ... 10
10.4 Electrostatic Discharge Caution ... 10
10.5 Glossary ... 10
11 Mechanical, Packaging, and Orderable Information ... 10

3 Revision History

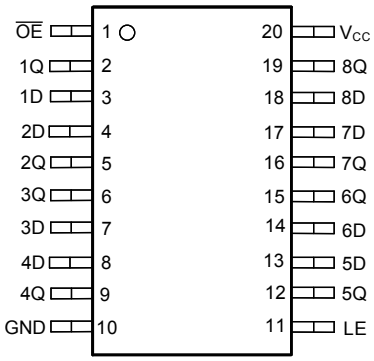
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (January 2022) to Revision C (May 2022)	Page
• Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6	4

Changes from Revision A (April 2003) to Revision B (January 2022)	Page
• 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新	1

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4 Pin Configuration and Functions



J, N, or DW package
20-Pin CDIP, PDIP, or SOIC
Top View

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC}$		± 20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$		± 20	mA
I_O	Continuous output drain current per output	$V_O = 0$ to V_{CC}		± 35	mA
I_O	Continuous output source or sink current per output	$V_O = 0$ to V_{CC}		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V		1000	ns
		V_{CC} = 4.5 V		500	
		V_{CC} = 6 V		400	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.3 Thermal Information

THERMAL METRIC		DW (SOIC) 20 PINS	N (PDIP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	109.1	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	77.6	65.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.5	55.3	°C/W
ψ_{JB}	Junction-to-top characterization parameter	77.1	65.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

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5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C		T_A = –55°C to 125°C		T_A = –40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9		1.9		1.9		V
			4.5 V	4.4		4.4		4.4		
			6 V	5.9		5.9		5.9		
		I_{OH} = –6 mA	4.5 V	3.98		3.7		3.84		
		I_{OH} = –7.8 mA	6 V	5.48		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V		0.1		0.1		0.1	V
			4.5 V		0.1		0.1		0.1	
			6 V		0.1		0.1		0.1	
		I_{OL} = 6 mA	4.5 V		0.26		0.4		0.33	
		I_{OL} = 7.8 mA	6 V		0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1		±1		±1	µA
I_{OZ}	V_O = V_{CC} or 0		6 V		±0.5		±10		±5	µA
I_{CC}	V_I = V_{CC} or 0	I_O = 0	6 V		8		160		80	µA
C_i					10		10		10	pF
C_o					20		20		20	pF

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

		V_{CC}	T_A = 25°C		T_A = –55°C to 125°C		T_A= –40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before LE ↓	2 V	50		75		65		ns
		4.5 V	10		15		13		
		6 V	9		13		11		
t_h	Hold time, data after LE ↓	2 V	5		5		5		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

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5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C		T_A = –55°C to 125°C		T_A = –40°C to 85°C		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 50 pF	2 V		150		225		190	ns
				4.5 V		30		45		38	
				6 V		26		38		33	
	LE	Q	C_L = 50 pF	2 V		175		265		220	
				4.5 V		35		53		44	
				6 V		30		45		37	
t_{en}	$\overline{OE}$	Q	C_L = 50 pF	2 V		150		225		190	ns
				4.5 V		30		45		38	
				6 V		26		38		33	
t_{dis}	$\overline{OE}$	Q	C_L = 50 pF	2 V		150		225		190	ns
				4.5 V		30		45		38	
				6 V		26		38		33	
t_t		Q	C_L = 50 pF	2 V		60		90		75	ns
				4.5 V		12		18		15	
				6 V		10		15		13	

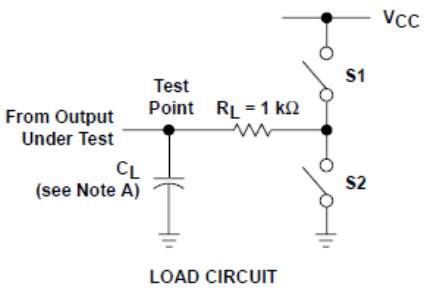
5.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	51	pF

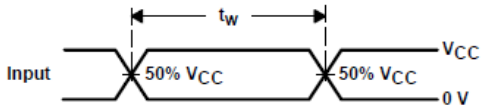
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6 Parameter Measurement Information

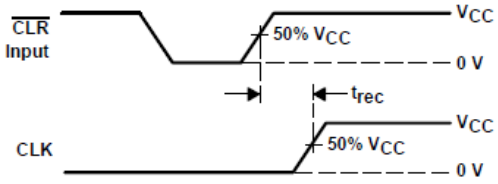


LOAD CIRCUIT

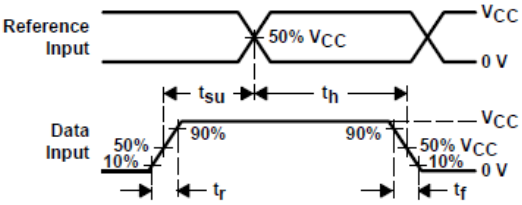
PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd} or t_t		Open	Open



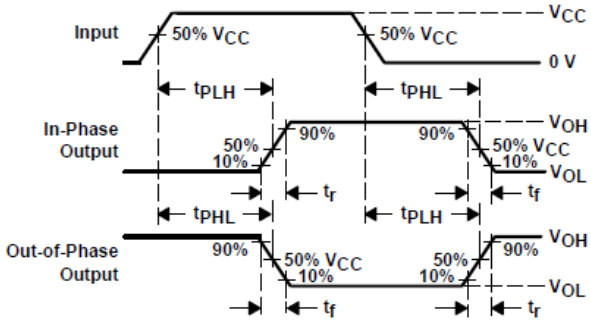
VOLTAGE WAVEFORMS
PULSE DURATION



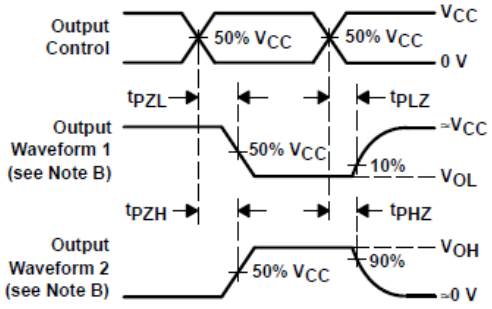
VOLTAGE WAVEFORMS
RECOVERY TIME



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, fmaxis measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.
I. All parameters and waveforms are not applicable to all devices.

図 6-1. Load Circuit and Voltage Waveforms

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7 Detailed Description

7.1 Overview

The ’HC373 devices are octal transparent D-type latches designed for 2-V to 6-V V_{CC} operation.

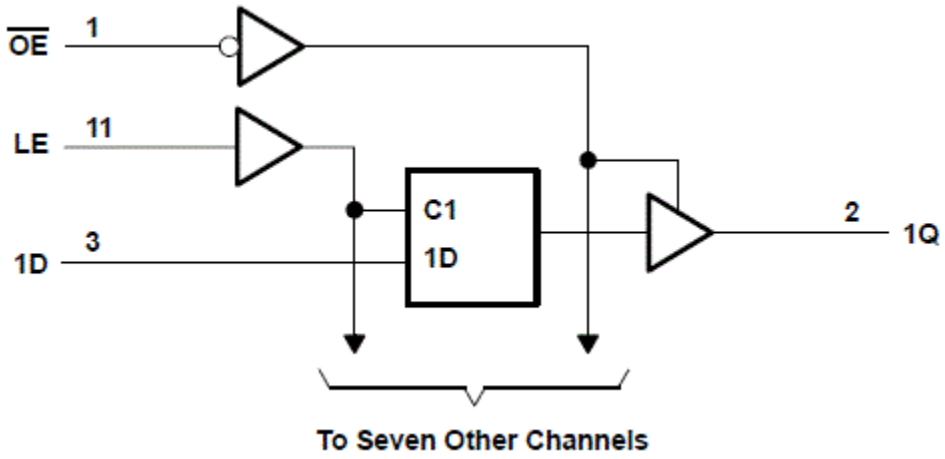
When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table(each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

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10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.3 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC373F	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC373F
CD54HC373F.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC373F
CD54HC373F3A	NRND	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201RA CD54HC373F3A
CD54HC373F3A.A	NRND	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407201RA CD54HC373F3A
CD74HC373E	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC373E
CD74HC373E.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC373E
CD74HC373EE4	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC373E
CD74HC373M	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-55 to 125	HC373M
CD74HC373M96	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC373M
CD74HC373M96.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC373M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC373, CD74HC373 :

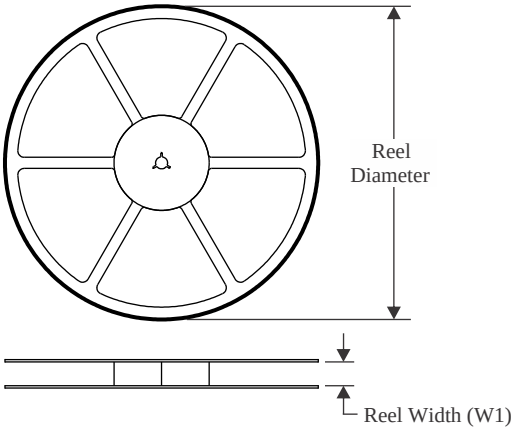
- Catalog : CD74HC373
- Military : CD54HC373

NOTE: Qualified Version Definitions:

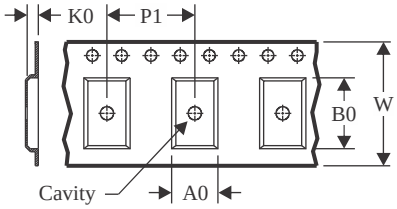
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

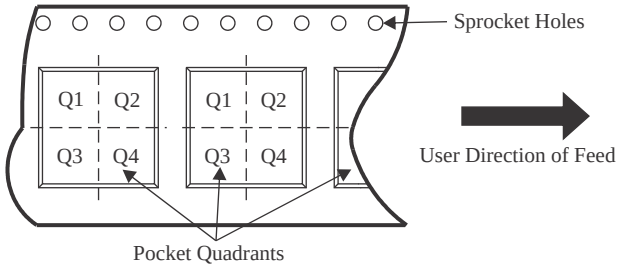


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

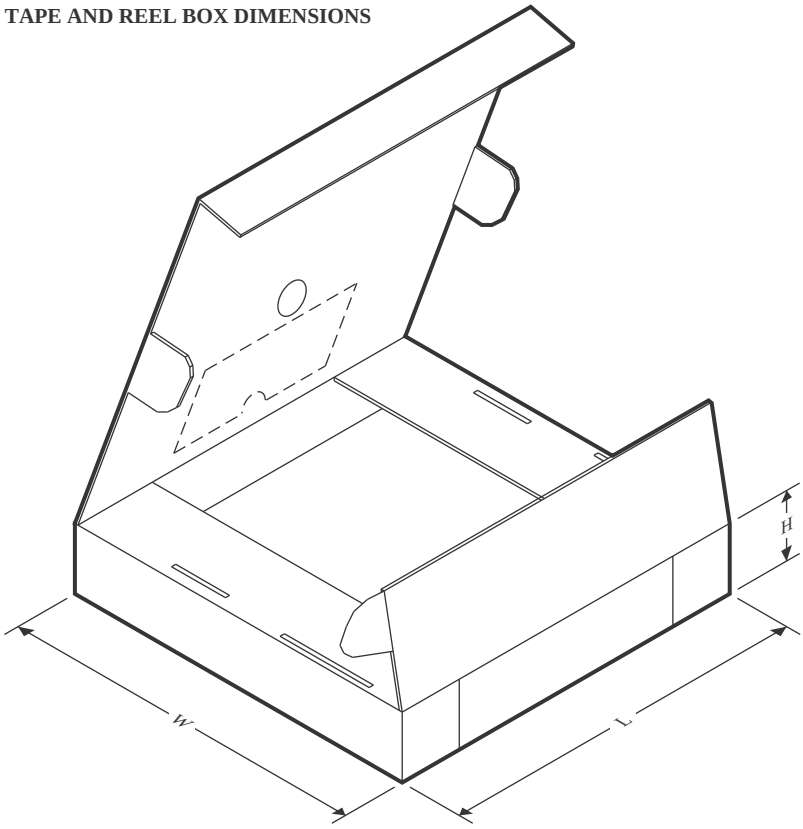
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC373M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HC373M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

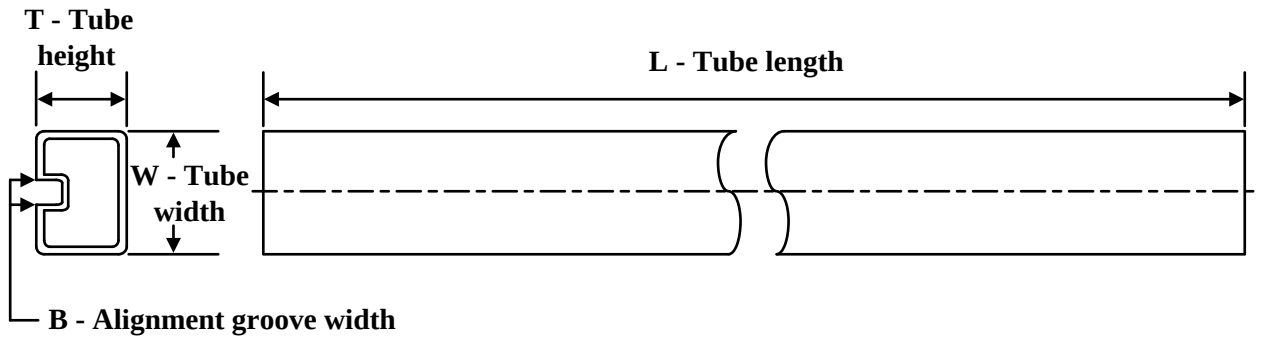
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC373M96	SOIC	DW	20	2000	356.0	356.0	45.0
CD74HC373M96	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE



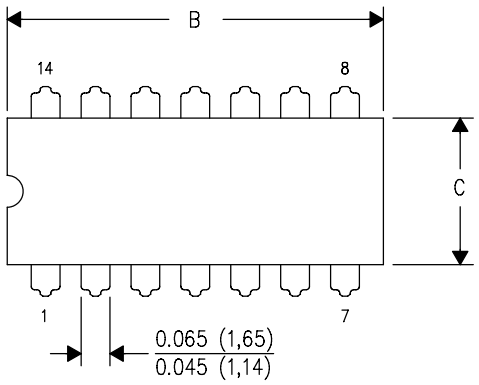
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC373E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC373E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC373EE4	N	PDIP	20	20	506	13.97	11230	4.32

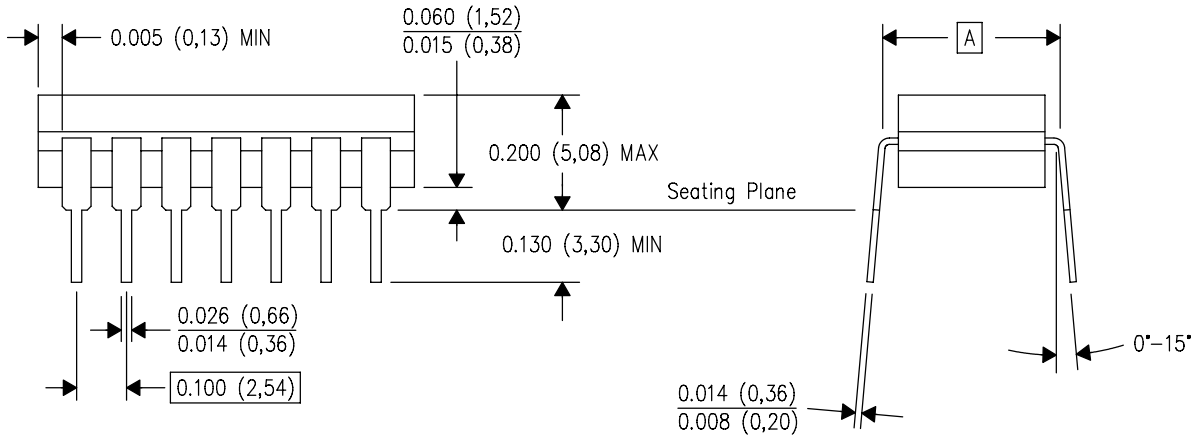
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



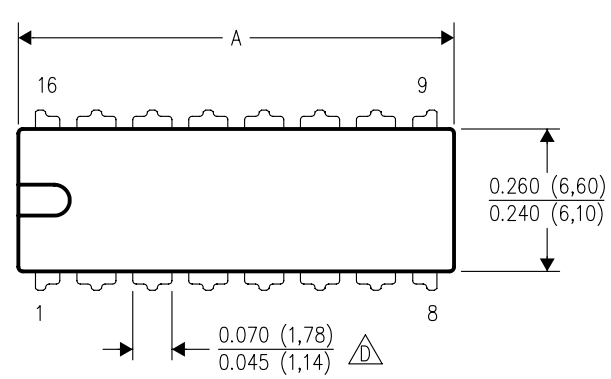
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

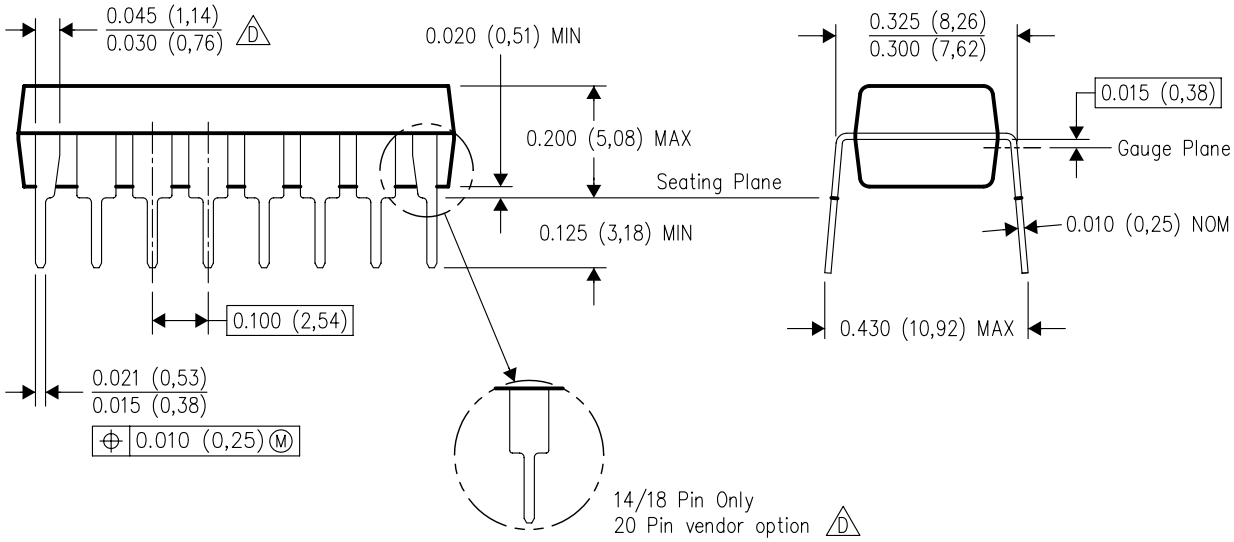
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

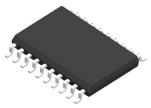


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

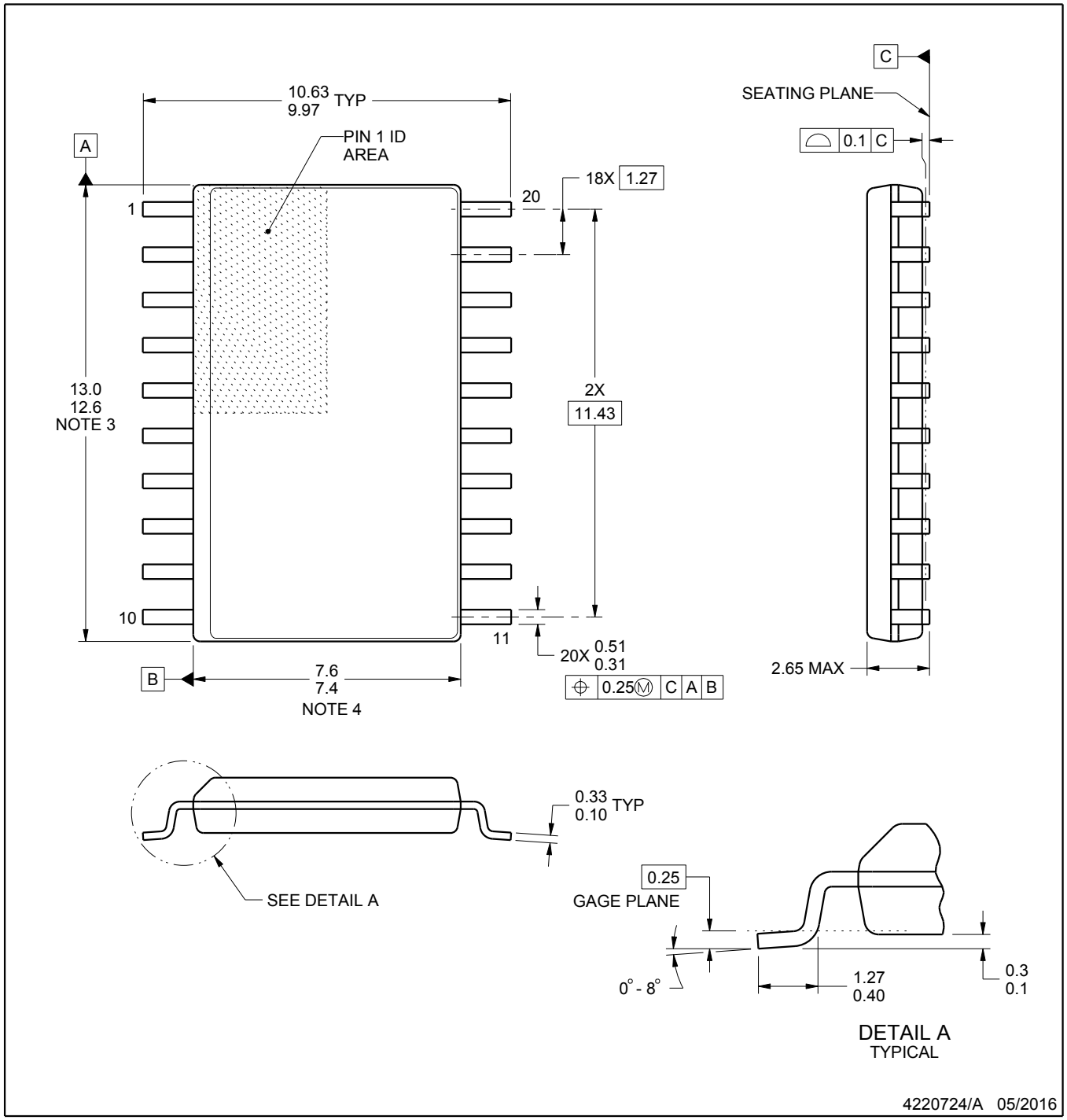


PACKAGE OUTLINE

DW0020A

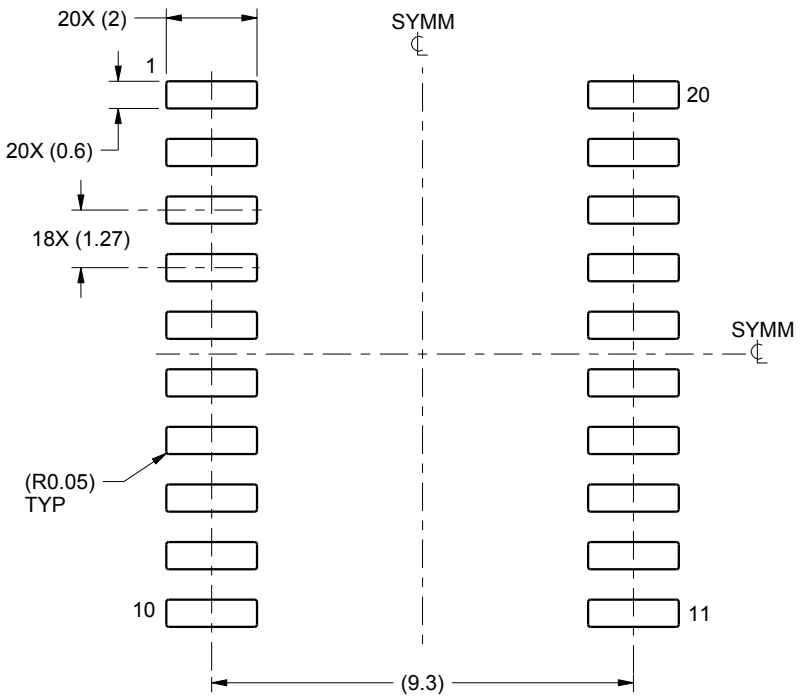
SOIC - 2.65 mm max height

SOIC

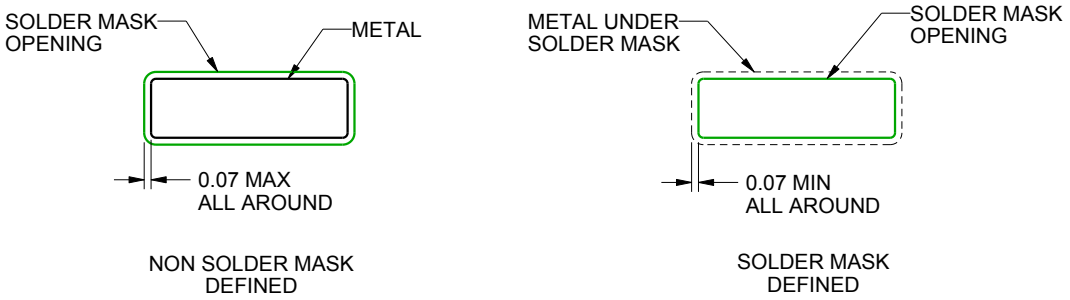


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

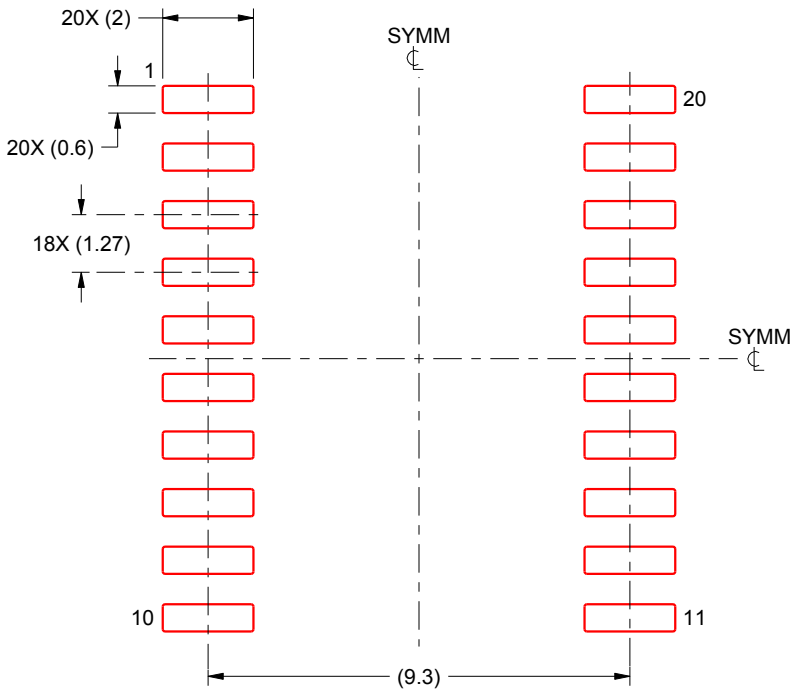


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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