TEXAS INSTRUMENTS
CD74HC74, CD54HC74
E – JANUARY 1998 – REVISED MAY 2021

CDx4HC74 デュアル D タイプ ポジティブ・エッジ・トリガ・フリップ・フロップ、クリアおよびプリセット付

1 特長

- バッファ付き入力
- 広い動作電圧範囲：2V～6V
- 広い動作温度範囲：-55℃～+125℃
- 最大 10 個の LSTTL 負荷ファンアウトに対応
- LSTTL ロジック IC に比べて消費電力を大幅削減

2 アプリケーション

- モメンタリ・スイッチからトグル・スイッチへの変換
- クロック信号の 2 分割または 4 分割

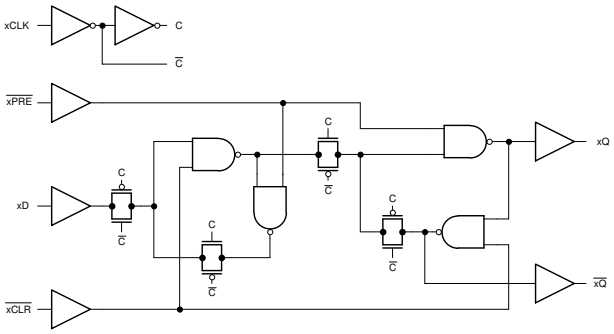
3 概要

CDx4HC74 デバイスには、2 つの独立した D タイプ正エッジ・トリガ型フリップ・フロップが内蔵されており、それぞれに非同期のプリセット・ピンとクリア・ピンが備わっています。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
CD74HC74M	SOIC (14)	8.70mm × 3.90mm
CD74HC74E	PDIP (14)	19.30mm × 6.40mm
CD54HC74F	CDIP (14)	21.30mm × 7.60mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図

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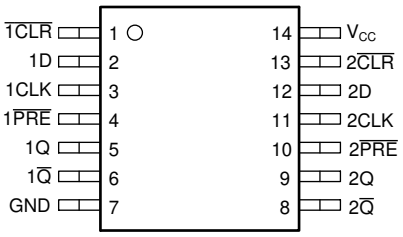
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (September 2003) to Revision E (June 2020)	Page
• 新しいデータシート標準に更新	1
• HCT デバイスをスタンドアロンのデータシート (SCHS409) へ移動	1
• $R_{\theta JA}$ increased for the D package from 86 to 133.6 °C/W and decreased for the N package from 80 to 62.2 °C/W	4

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5 Pin Configuration and Functions



D, N, or J Package
14-Pin SOIC, PDIP, or CDIP
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1 $\overline{CLR}$	1	Input	Channel 1, Clear Input, Active Low
1D	2	Input	Channel 1, Data Input
1CLK	3	Input	Channel 1, Positive edge triggered clock input
1 $\overline{PRE}$	4	Input	Channel 1, Preset Input, Active Low
1Q	5	Output	Channel 1, Output
1 $\overline{Q}$	6	Output	Channel 1, Inverted Output
GND	7	—	Ground
2 $\overline{Q}$	8	Output	Channel 2, Inverted Output
2Q	9	Output	Channel 2, Output
2 $\overline{PRE}$	10	Input	Channel 2, Preset Input, Active Low
2CLK	11	Input	Channel 2, Positive edge triggered clock input
2D	12	Input	Channel 2, Data Input
2 $\overline{CLR}$	13	Input	Channel 2, Clear Input, Active Low
V_{CC}	14	—	Positive Supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V		±20	mA
I_{OK}	Output clamp current(2)	$V_O < –0.5$ V or $V_O > V_{CC} + 0.5$ V		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature(3)	Plastic package		150	°C
		Hermetic package or die		175	
	Lead temperature (soldering 10s)	SOIC - lead tips only		300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) Guaranteed by design.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V			0.5	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 6 V			1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition time	V_{CC} = 2 V			1000	ns
		V_{CC} = 4.5 V			500	
		V_{CC} = 6 V			400	
T_A	Operating free-air temperature		–55		125	°C

6.3 Thermal Information

THERMAL METRIC(1)		CD74HC74		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.2	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.9	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.9	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	29.5	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.7	89.1	°C/W

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THERMAL METRIC[1]		CD74HC74		UNIT
		N (PDIP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	Operating free-air temperature (T_A)									UNIT
					25°C			–40°C to 85°C			–55°C to 125°C			
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = –20 µA	2 V	1.9			1.9			1.9			V
				4.5 V	4.4			4.4			4.4			
				6 V	5.9			5.9			5.9			
			I_{OH} = –4 mA	4.5 V	3.98			3.84			3.7			
			I_{OH} = –5.2 mA	6 V	5.48			5.34			5.2			
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V			0.1			0.1			0.1	V
				4.5 V			0.1			0.1			0.1	
				6 V			0.1			0.1			0.1	
			I_{OL} = 4 mA	4.5 V			0.26			0.33			0.4	
			I_{OL} = 5.2 mA	6 V			0.26			0.33			0.4	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V			±0.1			±1			±1	µA
I_{CC}	Supply current	V_I = V_{CC} or 0	I_O = 0	6 V			4			40			80	µA
C_i	Input capacitance			5 V			10			10			10	pF

6.5 Timing Requirements

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

			V_{CC}	Operating free-air temperature (T_A)									UNIT
				25°C			–40°C to 85°C			–55°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{su}	Setup time	Data to CP	2 V	60			75			90			ns
			4.5 V	12			15			18			
			6 V	10			13			15			
t_h	Hold time		2 V	3			3			3			ns
			4.5 V	3			3			3			
			6 V	3			3			3			
t_{rem}	Removal time	$\overline{R}$, $\overline{S}$, to CP	2 V	30			40			45			ns
			4.5 V	6			8			9			
			6 V	5			7			8			

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over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

			V_{CC}	Operating free-air temperature (T_A)									UNIT
				25°C			–40°C to 85°C			–55°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_w	Pulse width	$\overline{R}$, $\overline{S}$	2 V	80			100			120			ns
			4.5 V	16			20			24			
			6 V	14			17			20			
		CP	2 V	80			100			120			
			4.5 V	16			20			24			
			6 V	14			17			20			
f_{max}	CP frequency		2 V	6			5			4			MHz
			4.5 V	30			25			20			
			6 V	35			29			23			

6.6 Switching Characteristics

over operating free-air temperature range; typical values measured at TA = 25°C (unless otherwise noted).

PARAMETER		FROM	TO	TEST CONDITIONS	V_{CC}	Operating free-air temperature (T_A)									UNIT
						25°C			–40°C to 85°C			–55°C to 125°C			
						MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	Propagation delay	CP	Q, $\overline{Q}$	C_L = 50 pF	2 V			175			220			265	ns
					4.5 V			35			44			53	
					6 V			30			37			45	
				C_L = 15 pF	5 V		14								
		$\overline{R}$, $\overline{S}$	Q, $\overline{Q}$	C_L = 50 pF	2 V			200			250			300	
					4.5 V			40			50			60	
					6 V			34			43			51	
				C_L = 15 pF	5 V		17								
t_t	Transition-time		Y	C_L = 50 pF	2 V			75			95			110	ns
					4.5 V			15			19			22	
					6 V			13			16			19	

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		25		pF

6.8 Typical Characteristics

T_A = 25°C

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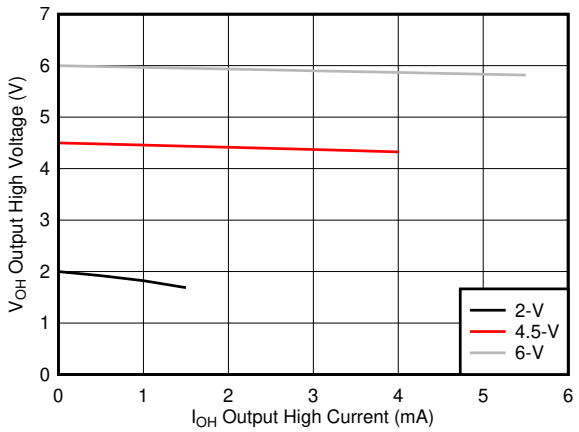


図 6-1. Typical output voltage in the high state (V_{OH})

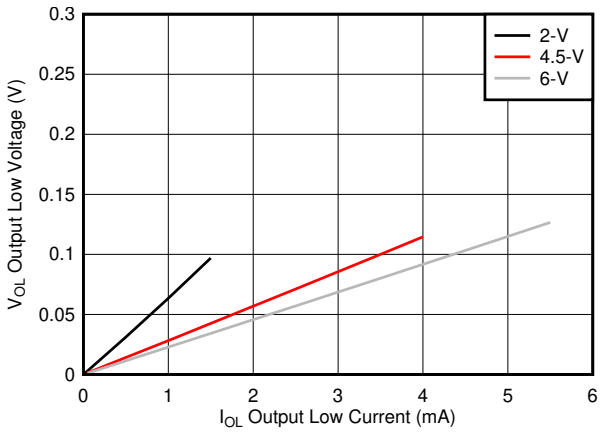
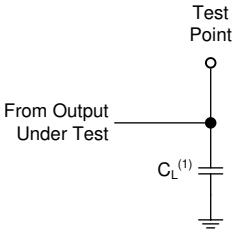


図 6-2. Typical output voltage in the high state (V_{OL})

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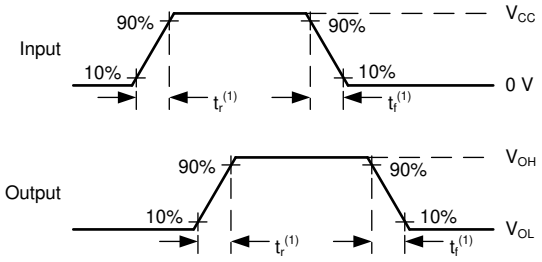
7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.
- The outputs are measured one at a time, with one input transition per measurement.



A. C_L= 50 pF and includes probe and jig capacitance.

図 7-1. Load Circuit



A. t_t is the greater of t_r and t_f.

図 7-2. Voltage Waveforms Transition Times

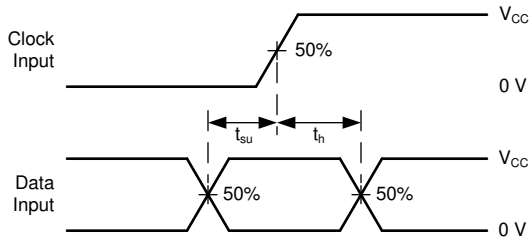


図 7-3. Voltage Waveforms Setup and Hold Times

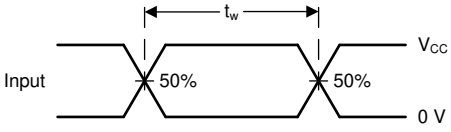
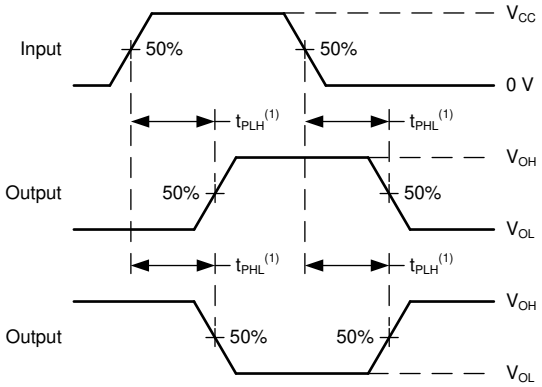


図 7-4. Voltage Waveforms Pulse Width



A. The maximum between t_{PLH} and t_{PHL} is used for t_{pd}.

図 7-5. Voltage Waveforms Propagation Delays

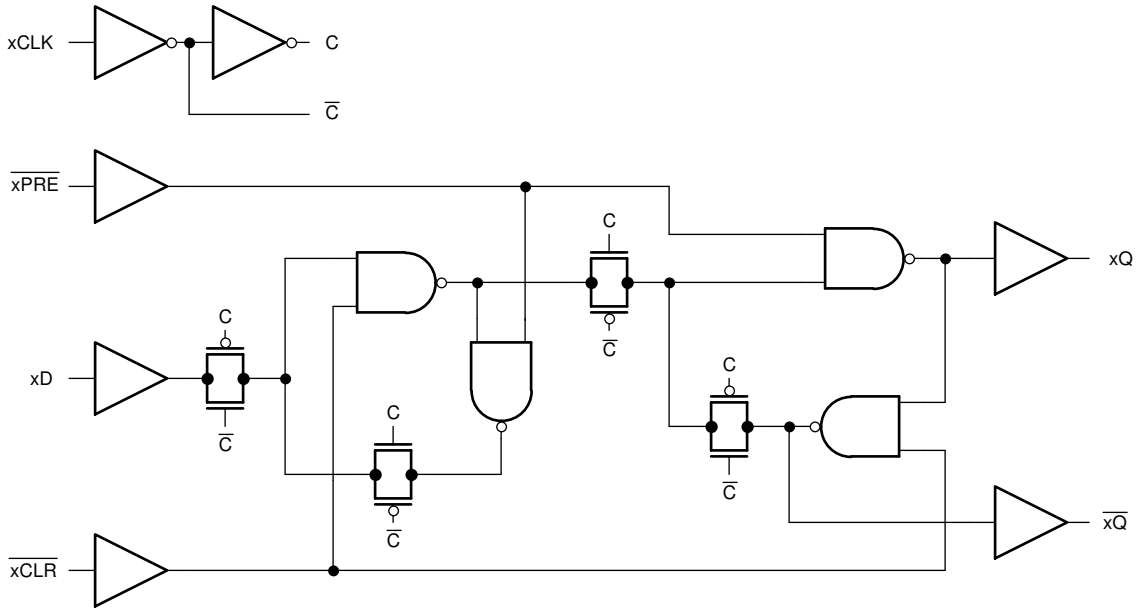
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8 Detailed Description

8.1 Overview

The CDx4HC74 devices contain two independent D-type positive-edge-triggered flip-flops with asynchronous preset and clear pins for each.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *セクション 6.1* must be followed at all times.

The CD74HC74 can drive a load with a total capacitance less than or equal to the maximum load listed in the *セクション 6.6* connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *セクション 6.1*.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *セクション 6.4*. The worst case resistance is calculated with the maximum input voltage, given in the *セクション 6.1*, and the maximum input leakage current, given in the *セクション 6.4*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *セクション 6.2* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

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8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in 図 8-1.

> **注意**
>
> Voltages beyond the values specified in the セクション 6.1 table can cause damage to the device. The recommended input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

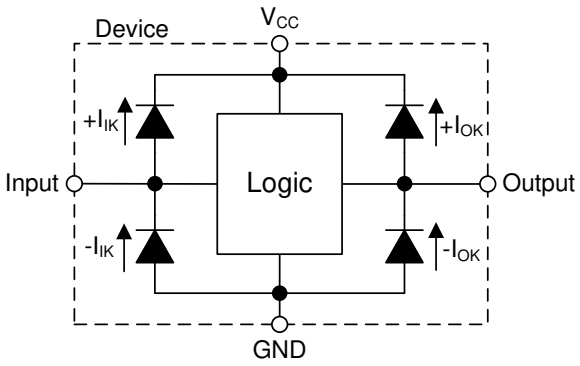


図 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H(1)	H(1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

(1) This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

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9 Application and Implementation

注

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9.1 Application Information

Toggle switches are typically large, mechanically complex and relatively expensive. It is desirable to use a momentary switch instead because they are small, mechanically simple and low cost. Some systems require a toggle switch's functionality but are space or cost constrained and must use a momentary switch instead.

If the data input (D) of the D-type flip-flop is tied to the inverted output ($\overline{Q}$), then each clock pulse will cause the value at the output (Q) to toggle. The momentary switch can be debounced and connected through a Schmitt-trigger buffer to the clock input (CLK) to toggle the output.

This application also utilizes a power-on reset circuit to ensure that the output always starts in the LOW state when power is applied.

9.2 Typical Application

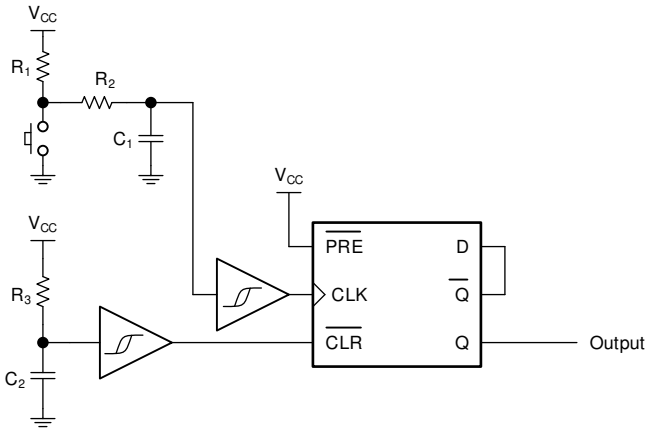


図 9-1. Typical application schematic

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *セクション 6.2*. The supply voltage sets the device's electrical characteristics as described in the *セクション 6.4*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the CD74HC74 plus the maximum supply current, I_{CC}, listed in the *セクション 6.4*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the *セクション 6.1*.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

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> **注意**
>
> The maximum junction temperature, T_J(max) listed in the *セクション 6.1*, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the *セクション 6.1*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the CD74HC74, as specified in the *セクション 6.4*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The CD74HC74 has standard CMOS inputs, so input signal edge rates cannot be slow. Slow input edge rates can cause oscillations and damaging shoot-through current. The recommended rates are defined in the *セクション 6.2*.

Refer to the *セクション 8.3* for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *セクション 6.4*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *セクション 6.4*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *セクション 8.3* for additional information regarding the outputs for this device.

9.2.1.4 Timing Considerations

The CD74HC74 is a clocked device. As such, it requires special timing considerations to ensure normal operation.

Primary timing factors to consider:

- Maximum clock frequency: the maximum operating clock frequency defined in *セクション 6.5* is the maximum frequency at which the device is guaranteed to function. This value refers specifically to the triggering waveform, measuring from one trigger level to the next.
- Pulse duration: ensure that the triggering event duration is larger than the minimum pulse duration, as defined in the *セクション 6.5*.
- Setup time: ensure that the data has changed at least one setup time prior to the triggering event, as defined in the *セクション 6.5*.
- Hold time: ensure that the data remains in the desired state at least one hold time after the triggering event, as defined in the *セクション 6.5*.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *セクション 11*.
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the CD74HC74 to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω. This will ensure that the maximum output current from the *セクション 6.1* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

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4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation

9.2.3 Application Curves

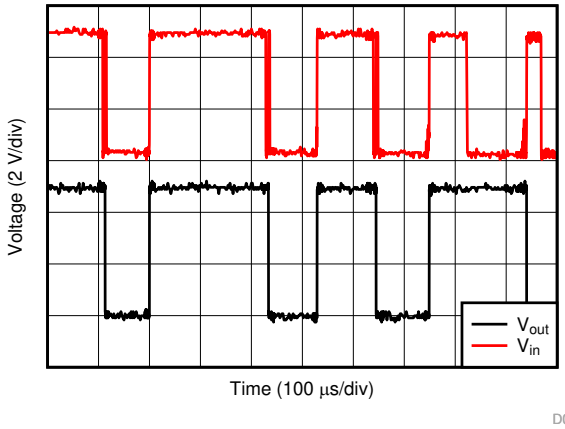


図 9-2. Waveform for non-debounced switch.

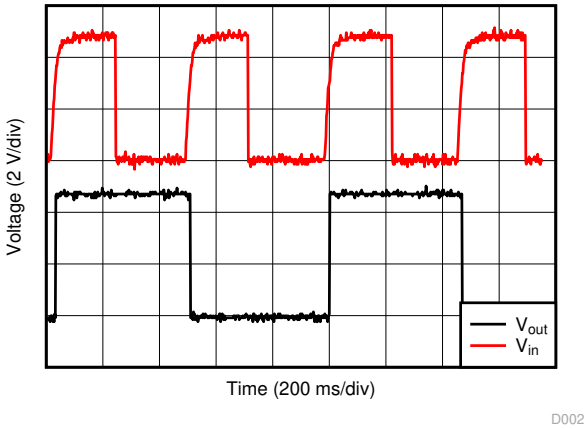


図 9-3. Waveform for debounced switch.

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *セクション 6.2*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *図 11-1*.

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11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

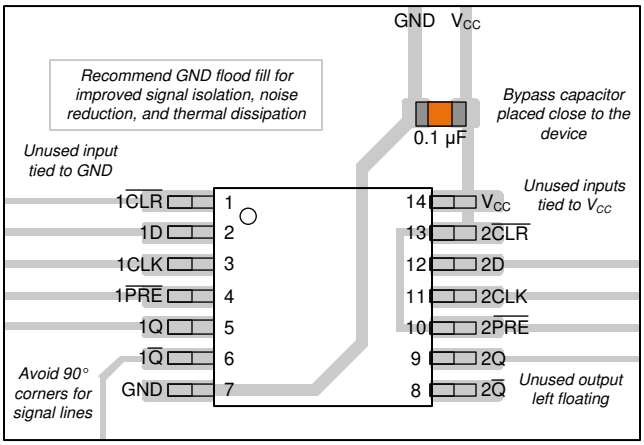


図 11-1. Example layout for the CD74HC74

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing with Logic

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 サポート・リソース

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12.5 静電気放電に関する注意事項



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12.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC74F	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC74F
CD54HC74F.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC74F
CD54HC74F3A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8405601CA CD54HC74F3A
CD54HC74F3A.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8405601CA CD54HC74F3A
CD74HC74E	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC74E
CD74HC74E.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC74E
CD74HC74EE4	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC74E
CD74HC74M	Obsolete	Production	SOIC (D) | 14	-	-	Call TI	Call TI	-55 to 125	HC74M
CD74HC74M96	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HC74M
CD74HC74M96.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M
CD74HC74M96G4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M
CD74HC74M96G4.A	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M
CD74HC74MT	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M
CD74HC74MT.A	Active	Production	SOIC (D) | 14	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC74M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC74, CD74HC74 :

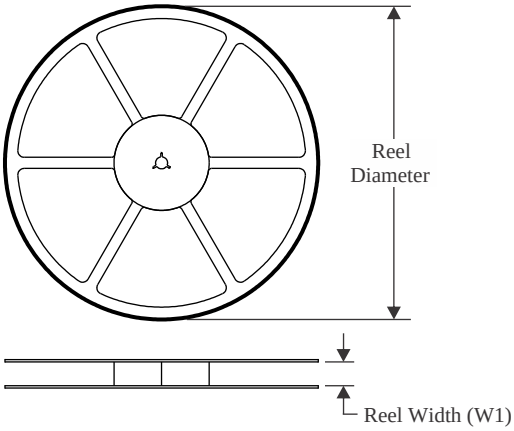
- Catalog : CD74HC74
- Military : CD54HC74

NOTE: Qualified Version Definitions:

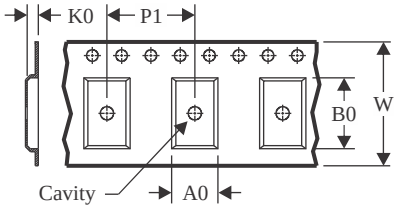
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

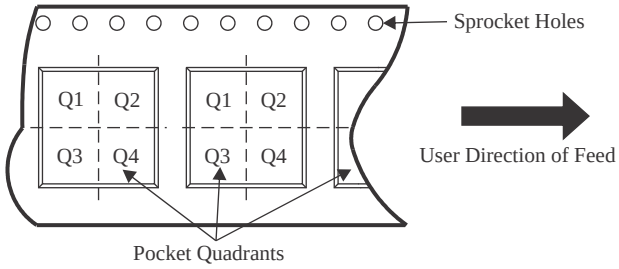


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

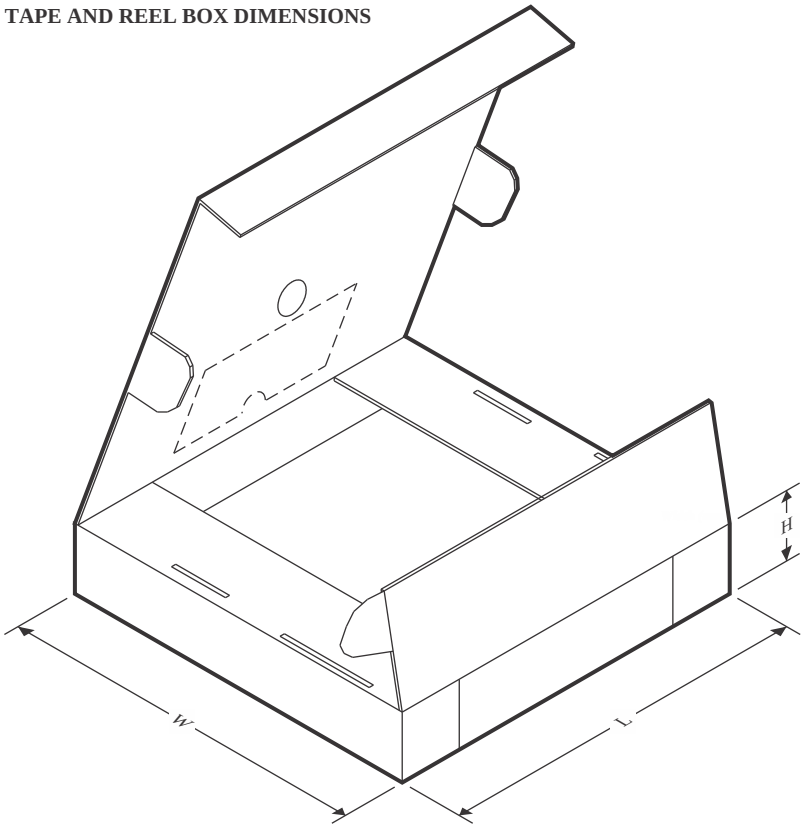
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC74M96G4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC74MT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

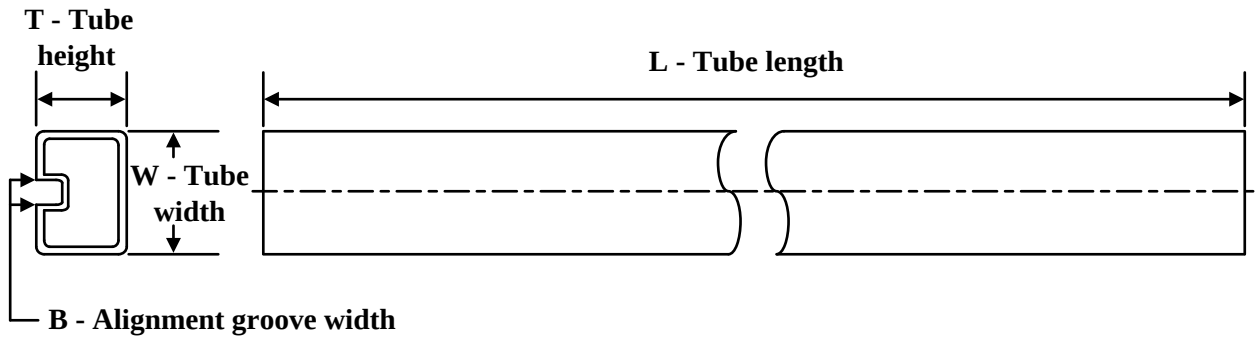
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

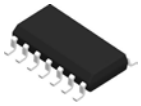
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC74M96G4	SOIC	D	14	2500	353.0	353.0	32.0
CD74HC74MT	SOIC	D	14	250	213.0	191.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC74E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC74E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC74E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC74E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC74EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC74EE4	N	PDIP	14	25	506	13.97	11230	4.32

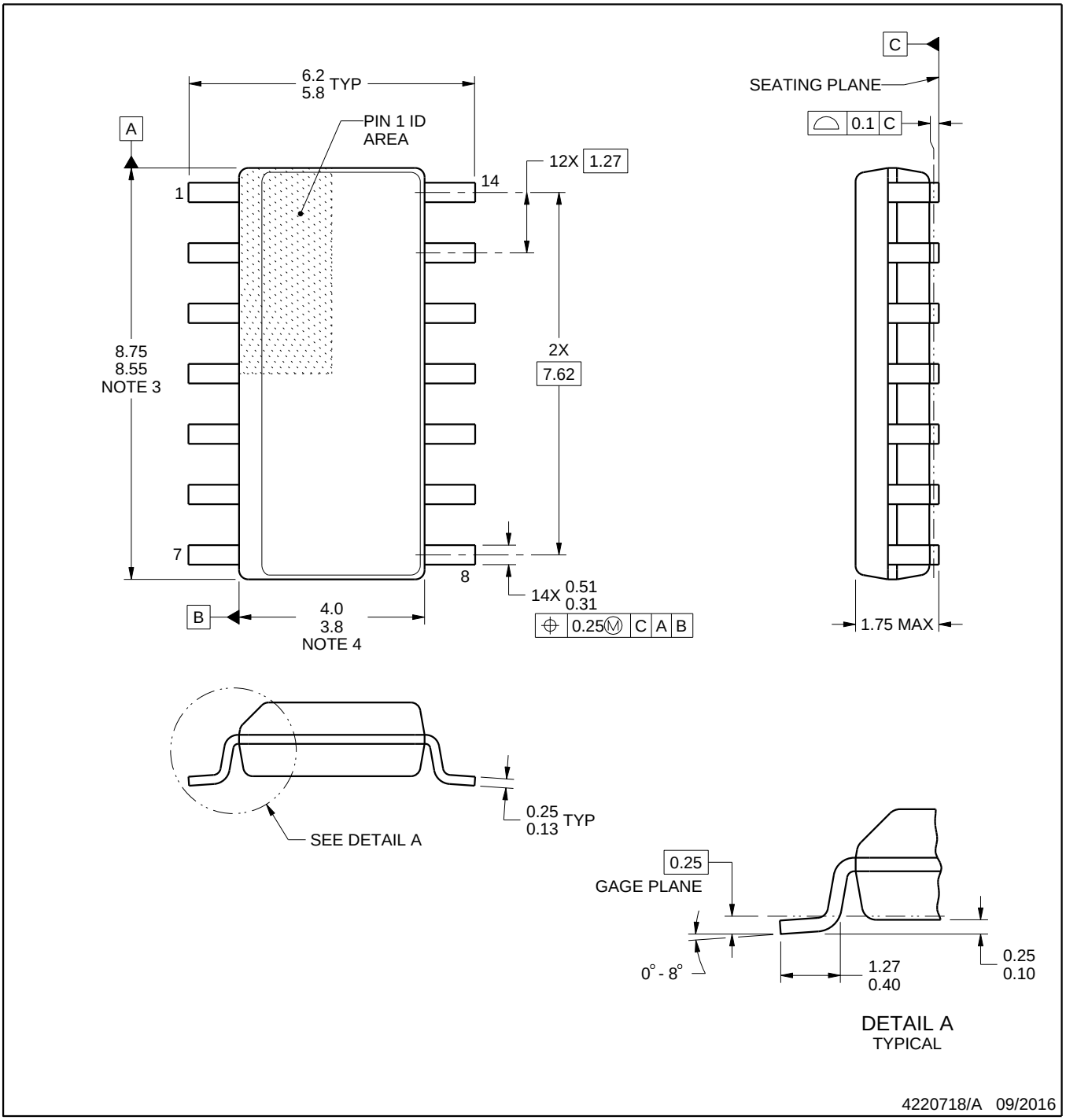


PACKAGE OUTLINE

D0014A

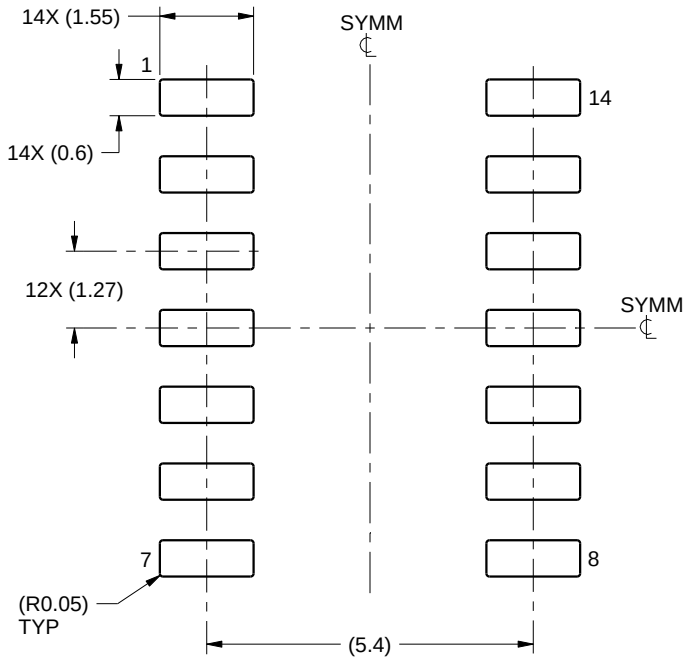
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

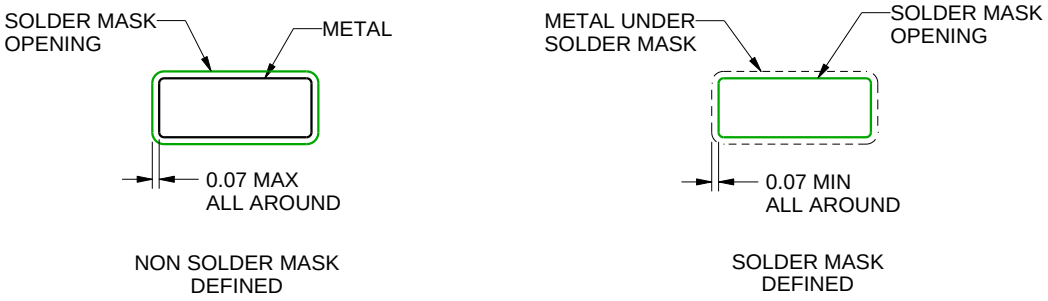


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

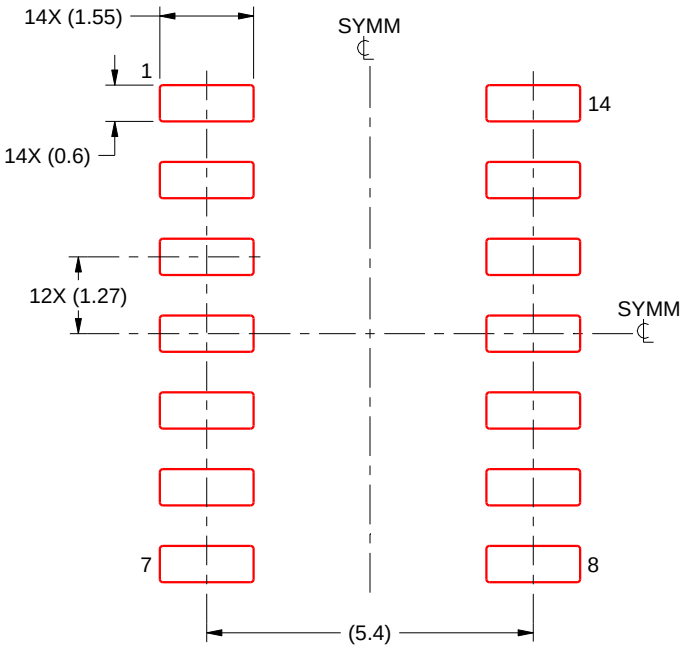
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

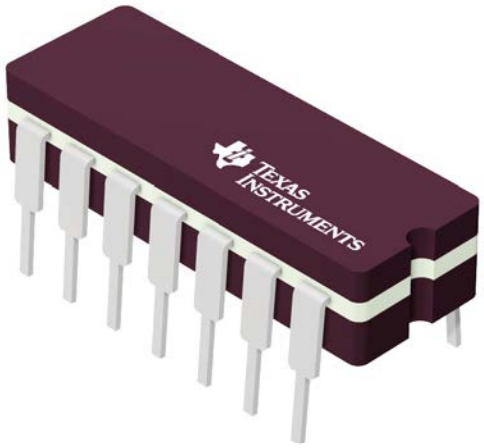
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

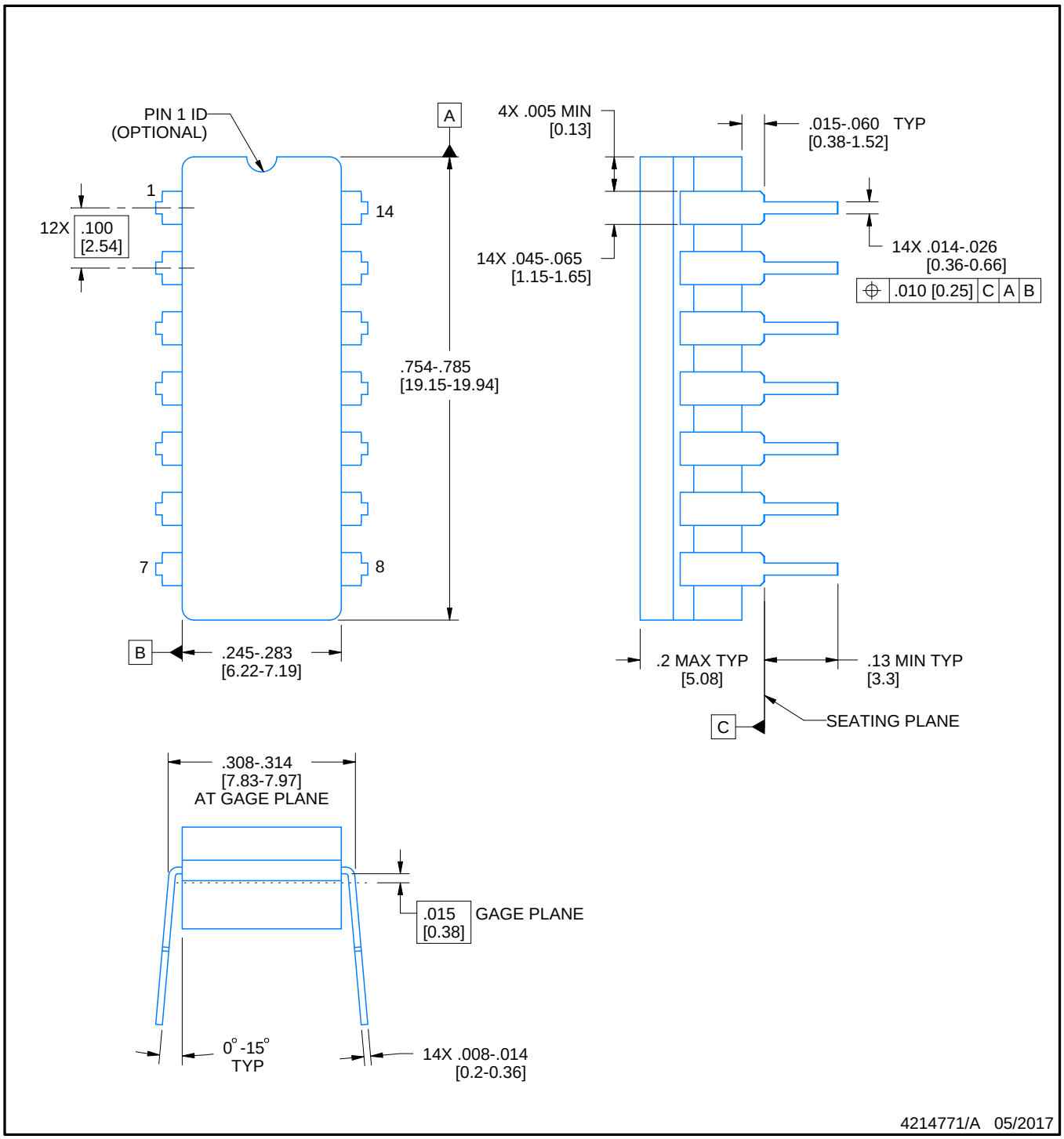


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

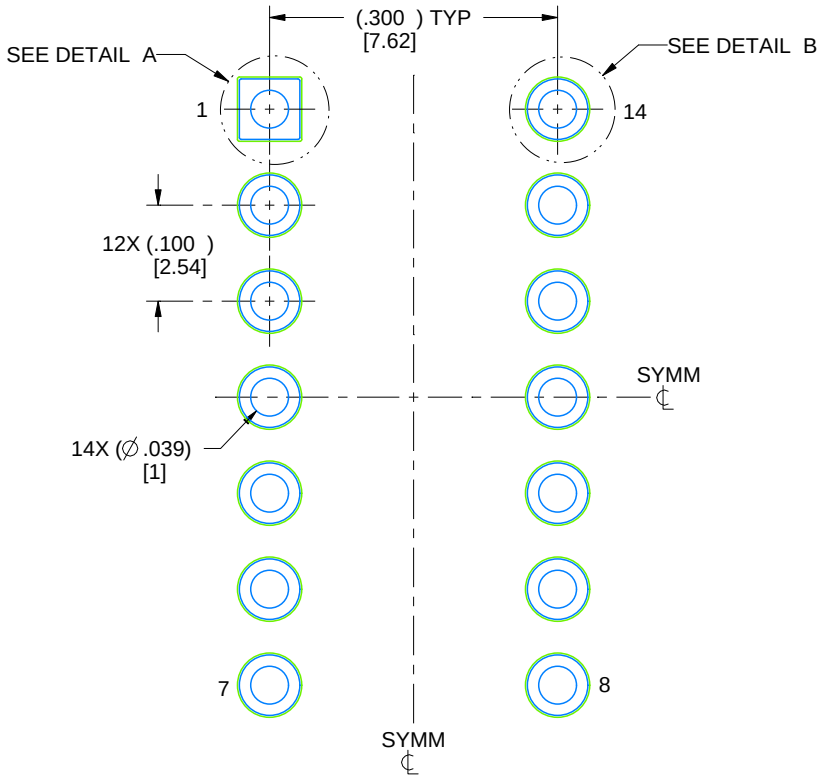
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

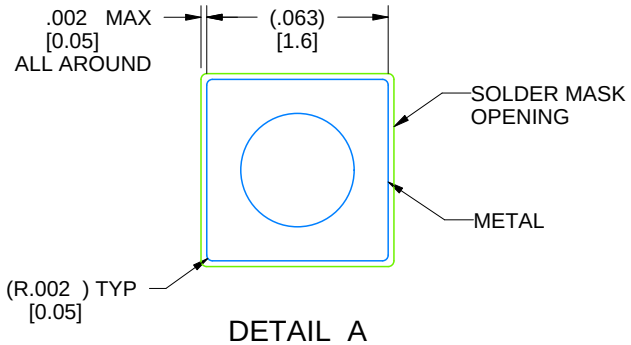
J0014A

CDIP - 5.08 mm max height

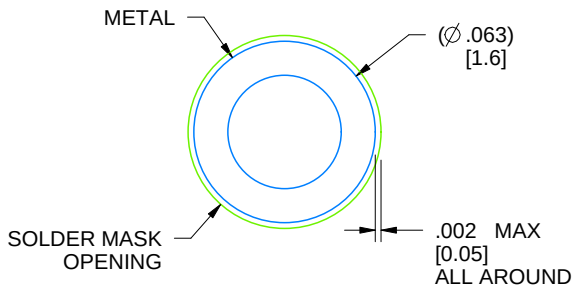
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



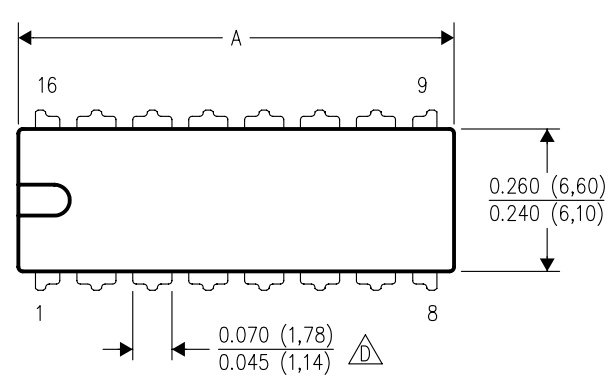
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

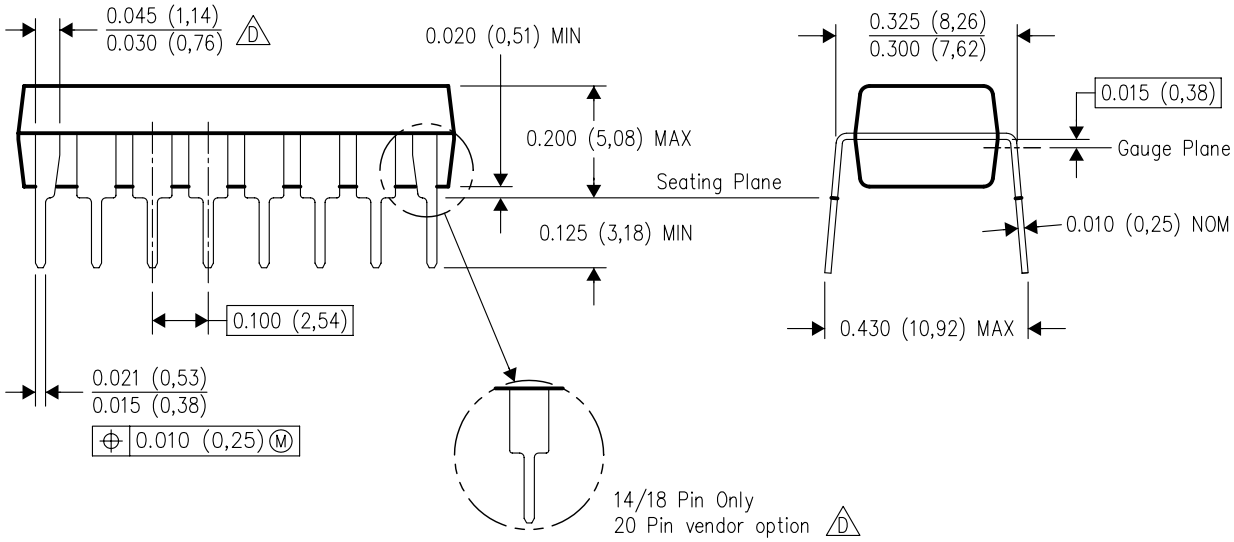
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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最終更新日：2025 年 10 月