

CDx4HC640、CDx4HCT640 高速 CMOS ロジック、オクタール、スリー・ステート・バス・トランシーバ、反転型

1 特長

- バッファ付き入力
- スリー・ステート出力
- 複数のデータ・バス・アーキテクチャを採用したアプリケーション
- ファンアウト (全温度範囲にわたって)
 - 標準出力: 10 個の LSTTL 負荷
 - バス・ドライバ出力: 15 の LSTTL 負荷
- 広い動作温度範囲: $-55^{\circ}\text{C} \sim 125^{\circ}\text{C}$
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
 - 2V~6V で動作
 - 優れたノイズ耐性: V_{CC} に対して $N_{\text{IL}} = 30\%$ 、 $N_{\text{IH}} = 30\%$ ($V_{\text{CC}} = 5\text{V}$ 時)
- HCT タイプ
 - 4.5V~5.5V で動作
 - LSTTL 入力ロジックと直接互換、 $V_{\text{IL}} = 0.8\text{V}$ (最大値)、 $V_{\text{IH}} = 2\text{V}$ (最小値)
 - CMOS 入力互換、 V_{OL} 、 V_{OH} で $I_{\text{I}} \leq 1\mu\text{A}$

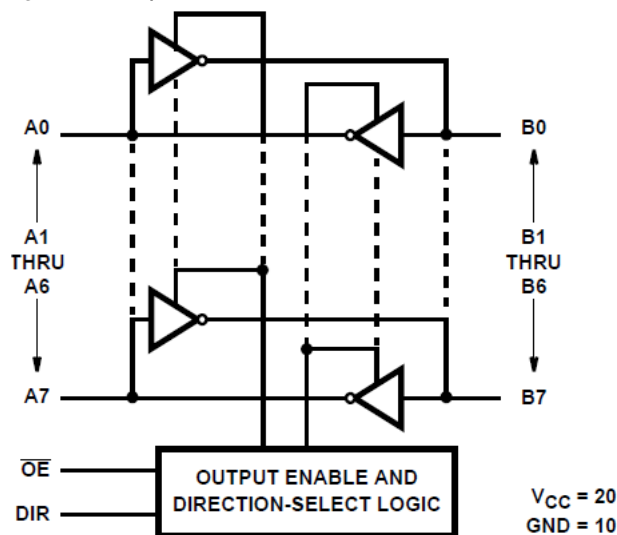
2 概要

CDx4HC640 および CDx4HCT640 は、スリー・ステート出力の反転オクタール・バス・トランシーバです。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
CD54HC640	J (CDIP, 20)	26.92mm × 6.92mm
CD74HC640	N (PDIP, 20)	25.4mm × 6.35mm
	DW (SOIC, 20)	12.80mm × 7.50mm
CD54HCT640	J (CDIP, 20)	26.92mm × 6.92mm
CD74HCT640	N (PDIP, 20)	25.40mm × 6.35mm
	DW (SOIC, 20)	12.80mm × 7.50mm

- (1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ブロック図



Table of Contents

1 特長	1	7.3 Device Functional Modes.....	8
2 概要	1	8 Power Supply Recommendations	9
3 Revision History	2	9 Layout	9
4 Pin Configuration and Functions	3	9.1 Layout Guidelines.....	9
5 Specifications	4	10 Device and Documentation Support	10
5.1 Absolute Maximum Ratings.....	4	10.1 Documentation Support.....	10
5.2 Recommended Operating Conditions.....	4	10.2 Receiving Notification of Documentation Updates..	10
5.3 Thermal Information.....	4	10.3 サポート・リソース.....	10
5.4 Electrical Characteristics.....	5	10.4 Trademarks.....	10
5.5 Switching Characteristics ⁽²⁾	6	10.5 Electrostatic Discharge Caution.....	10
6 Parameter Measurement Information	7	10.6 Glossary.....	10
7 Detailed Description	8	11 Mechanical, Packaging, and Orderable Information	10
7.1 Overview.....	8		
7.2 Functional Block Diagram.....	8		

3 Revision History

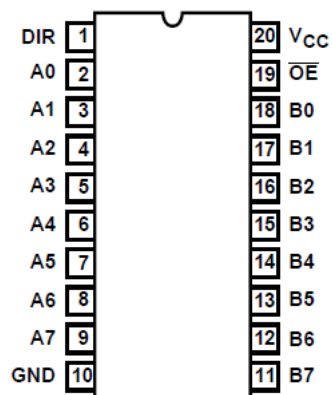
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2003) to Revision C (July 2022)

Page

- 最新のデータシート規格を反映するように、文書全体にわたって表、図、相互参照の採番方法を更新..... **1**

4 Pin Configuration and Functions



J, N and DW Package
20-Pin CDIP, PDIP or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$		± 20	mA
I_{OK}	Output diode current	For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$		± 20	mA
I_O	Drain current, per output	For $-0.5V < V_O < V_{CC} + 0.5V$		± 35	mA
I_O	Output source or sink current per output pin	For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$		± 25	mA
	Continuous current through V_{CC} or GND			± 50	mA
T_J	Junction Temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s)(SOIC - lead tips only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage	HC types	2	6	V
		HCT types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	$V_{CC} = 2V$		1000	ns
		$V_{CC} = 4.5V$		500	
		$V_{CC} = 6V$		400	
T_A	Temperature range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP)	DW (SOIC)	UNIT
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾	69	58	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽¹⁾	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V _{IL}	Low-level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		V
			6	1.8			1.8		1.8		V
V _{OH}	High-level output voltage CMOS loads	I _{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I _{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
		I _{OH} = – 20 μA	6	5.9			5.9		5.9		V
	High-level output voltage TTL loads	I _{OH} = – 6 mA	4.5	3.98			3.84		3.7		V
		I _{OH} = – 7.8 mA	6	5.48			5.34		5.2		V
V _{OL}	Low-level output voltage CMOS loads	I _{OL} = 20 μA	2	0.1			0.1		0.1		V
		I _{OL} = 20 μA	4.5	0.1			0.1		0.1		V
		I _{OL} = 20 μA	6	0.1			0.1		0.1		V
	Low-level output voltage TTL loads	I _{OL} = 6 mA	4.5	0.26			0.33		0.4		V
		I _{OL} = 7.8 mA	6	0.26			0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	6	±0.1			±1		±1		μA
I _{CC}	Quiescent device current	V _I = V _{CC} or GND	6	8			80		160		μA
I _{OZ}	Three-state leakage current	V _O = V _{CC} or GND	6	±0.5			±5		±10		μA
HCT TYPES											
V _{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low-level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High-level output voltage CMOS loads	V _{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	V _{OH} = – 6 mA	4.5	3.98			3.84		3.7		V
V _{OL}	Low-level output voltage CMOS loads	V _{OL} = 20 μA	4.5	0.1			0.1		0.1		V
	Low-level output voltage TTL	V _{OL} = 6 mA	4.5	0.26			0.33		0.4		V
I _I	Input leakage current	V _I = V _{CC} or GND	5.5	±0.1			±1		±1		μA
I _{CC}	Quiescent device current	V _I = V _{CC} or GND	5.5	8			80		160		μA
I _{OZ}	Three-state leakage current	V _O = V _{CC} or GND	5.5	±0.5			±5		±10		
ΔI _{CC} ⁽¹⁾	Additional quiescent device current per input pin	DIR input held at V _{CC} – 2.1	4.5 to 5.5	100 324			405		441		μA
		OE and A inputs held at v _{CC} – 2.1	4.5 to 5.5	100 540			675		735		
		B input held at V _{CC} – 2.1	4.5 to 5.5	100 540			675		735		

(1) For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA

5.5 Switching Characteristics⁽²⁾

Input $t_i = 6\text{ns}$. Unless otherwise specified, $C_L = 50\text{pF}$

PARAMETER		V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES										
t _{pd}	Propagation delay A to B B to $\bar{A}$	2			90		115		135	ns
		4.5		7 ⁽¹⁾	18		23		27	
		6			15		20		23	
t _{pd}	Propagation delay Output High-Z To high level, low level	2			150		190		225	ns
		4.5		12 ⁽¹⁾	30		38		45	
		6			26		33		38	
t _{pd}	Propagation delay Output high level Output low level to high Z	2			150		190		225	ns
		4.5		12 ⁽¹⁾	30		38		45	
		6			26		33		38	
t _t	Output transition time	2			60		75		90	ns
		4.5			12		15		18	
		6			10		13		15	
C _i	Input Capacitance		10		10		10		10	pF
C _O	Three-state output capacitance				20		20		20	pF
C _{pd}	Power dissipation capacitance (3) (4)	5		38						pF
HCT TYPES										
t _{pd}	Propagation delay A to B B to $\bar{A}$	4.5		9 ⁽¹⁾	22		28		33	ns
t _{pd}	Propagation delay Output High-Z To high level, low level	4.5		12 ⁽¹⁾	30		38			ns
t _{pd}	Propagation delay Output high level Output low level to high Z	4.5		12 ⁽¹⁾	30		38			ns
t _t	Transition times	4.5			12		15			ns
C _i	Input capacitance		10		10		10			pF
C _O	Three-state output capacitance				20		20			pF
C _{pd}	Power dissipation capacitance (3) (4)	5		41						pF

(1) Typical value tested at 5V, $C_L = 15\text{pF}$.

(2) For details on CMOS power calculation see, [SCAA053B](#)

(3) CPD is used to determine the dynamic power consumption, per channel

(4) $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

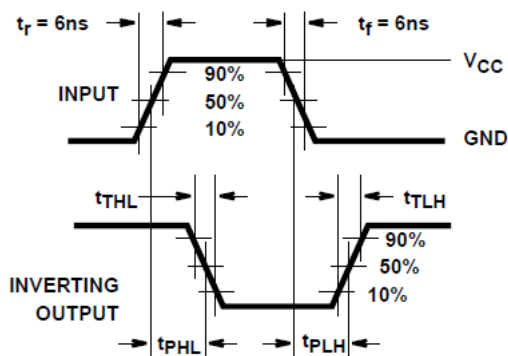


FIG 6-1. HC transition times and propagation delay times, combination logic

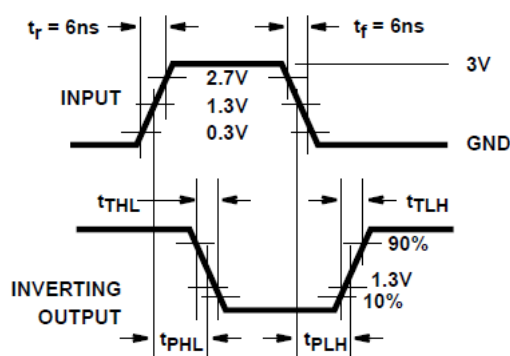


FIG 6-2. HCT transition times and propagation delay times, combination logic

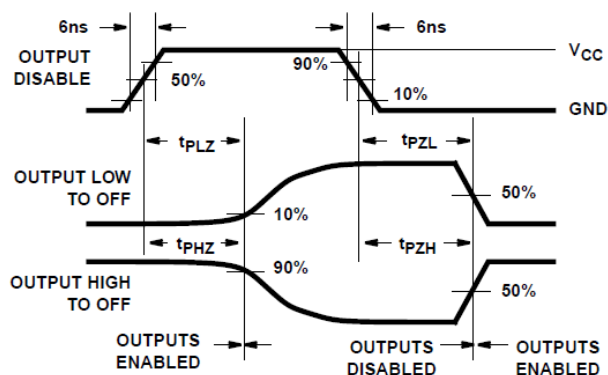


FIG 6-3. HC three-state propagation delay waveform

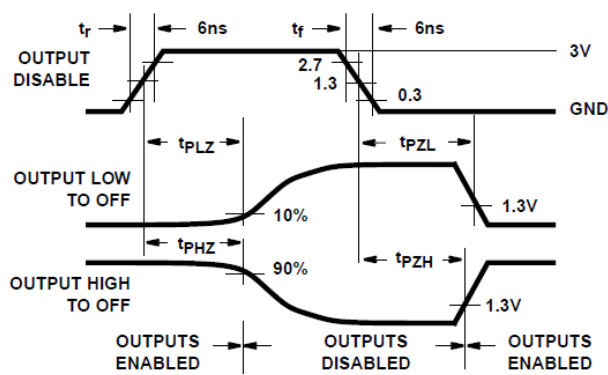
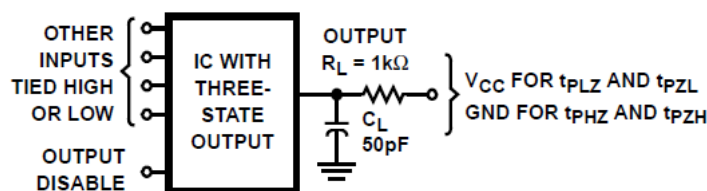


FIG 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is output $R_L = 1k\Omega$ to V_{CC} , $C_L = 50pF$.

FIG 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

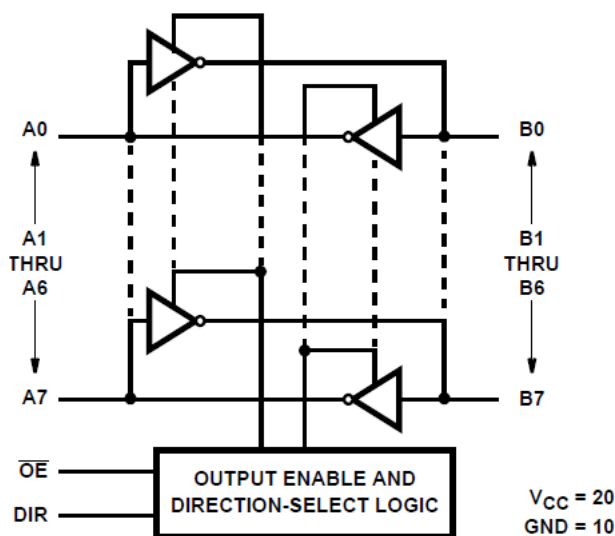
7.1 Overview

The CDx4HC640 and CDx4HCT640 silicon-gate CMOS three-state bidirectional inverting and non-inverting buffers are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits, and have speeds comparable to low power Schottky TTL circuits. They can drive 15 LSTTL loads. The CDx4HC640 and CDx4HCT640 devices have inverting buffers.

The direction of data flow (A to B, B to A) is controlled by the DIR input.

Outputs are enabled by a low on the Output Enable input ($\overline{OE}$); a high $\overline{OE}$ puts these devices in the high impedance mode.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Function Table⁽²⁾

Control Inputs ⁽¹⁾		Data Port Status	
$\overline{OE}$	DIR	A_n	B_n
L	L	$\overline{O}$	I
H	H	Z	Z
H	L	Z	Z
L	H	I	$\overline{O}$

- (1) H = High level. L = Low level. I = Input. $\overline{O}$ = Output (inversion of input level). Z = High impedance.
- (2) To prevent excess currents in the High-Z modes all I/O terminals should be terminated with 1k Ω to 1M Ω resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8974001RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD54HC640F3A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780901RA CD54HC640F3A
CD54HC640F3A.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8780901RA CD54HC640F3A
CD54HCT640F3A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD54HCT640F3A.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974001RA CD54HCT640F3A
CD74HC640E	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC640E
CD74HC640E.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC640E
CD74HC640M	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC640M
CD74HC640M.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC640M
CD74HCT640E	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT640E
CD74HCT640E.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT640E
CD74HCT640M	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT640M
CD74HCT640M.A	Active	Production	SOIC (DW) 20	25 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT640M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

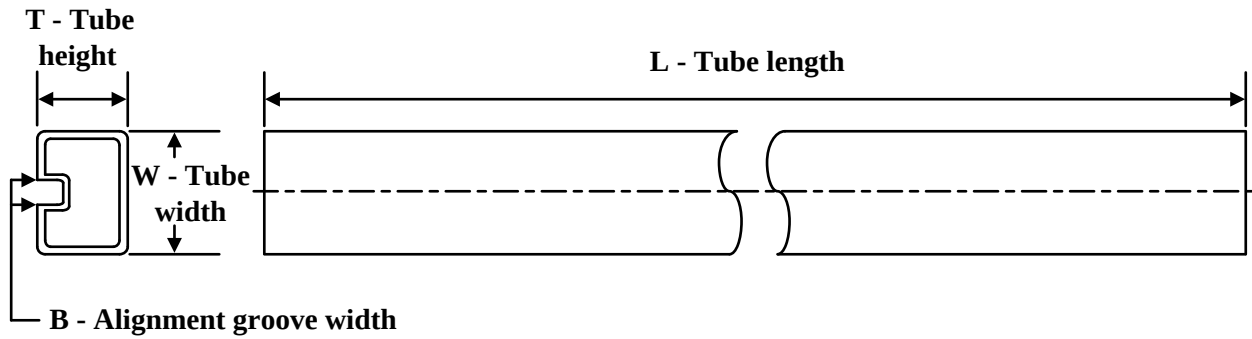
OTHER QUALIFIED VERSIONS OF CD54HC640, CD54HCT640, CD74HC640, CD74HCT640 :

- Catalog : [CD74HC640](#), [CD74HCT640](#)
- Military : [CD54HC640](#), [CD54HCT640](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE



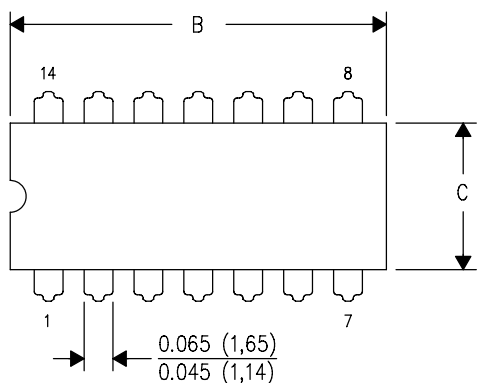
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC640E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC640E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC640M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HC640M.A	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT640E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT640E.A	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT640M	DW	SOIC	20	25	507	12.83	5080	6.6
CD74HCT640M.A	DW	SOIC	20	25	507	12.83	5080	6.6

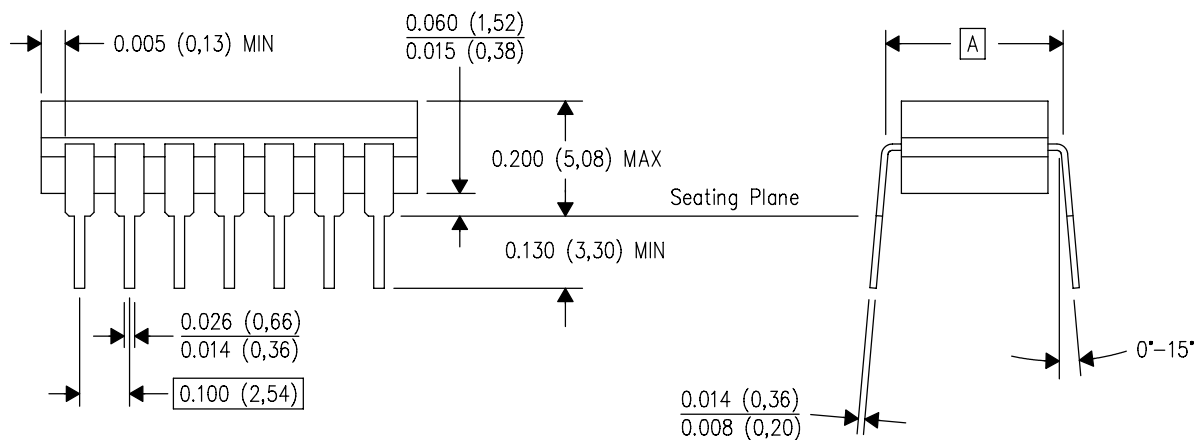
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



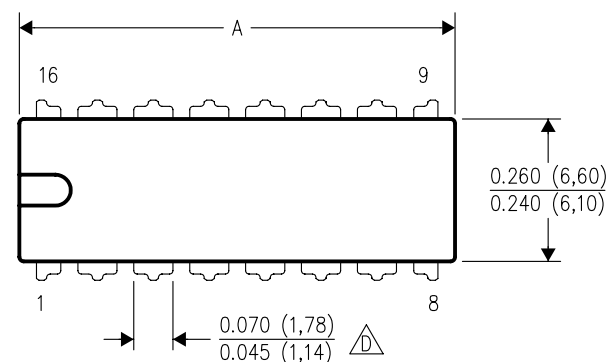
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

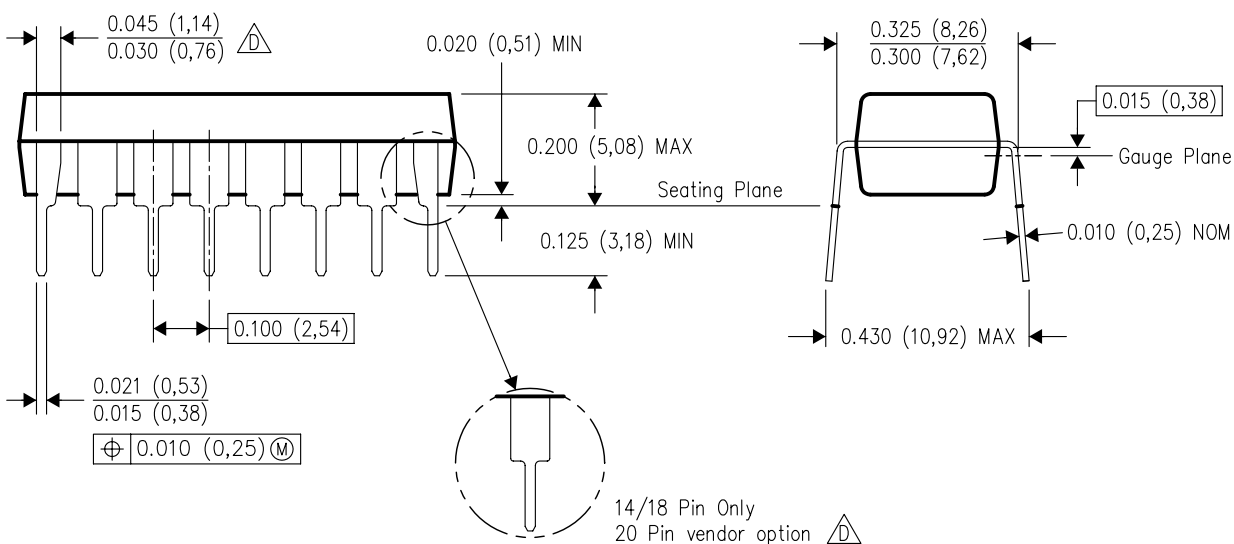
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

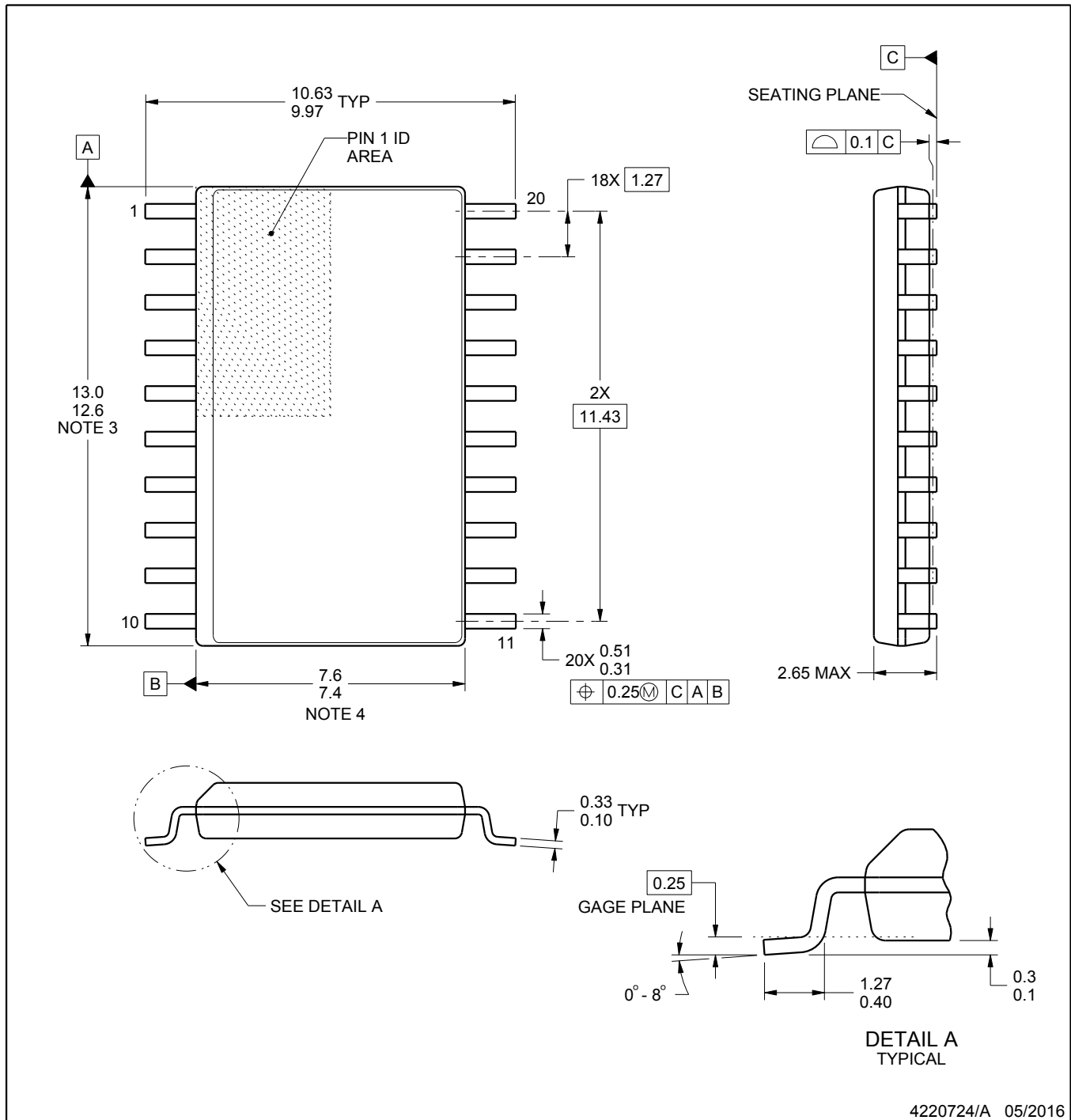
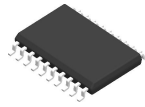


PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.



NOTES:

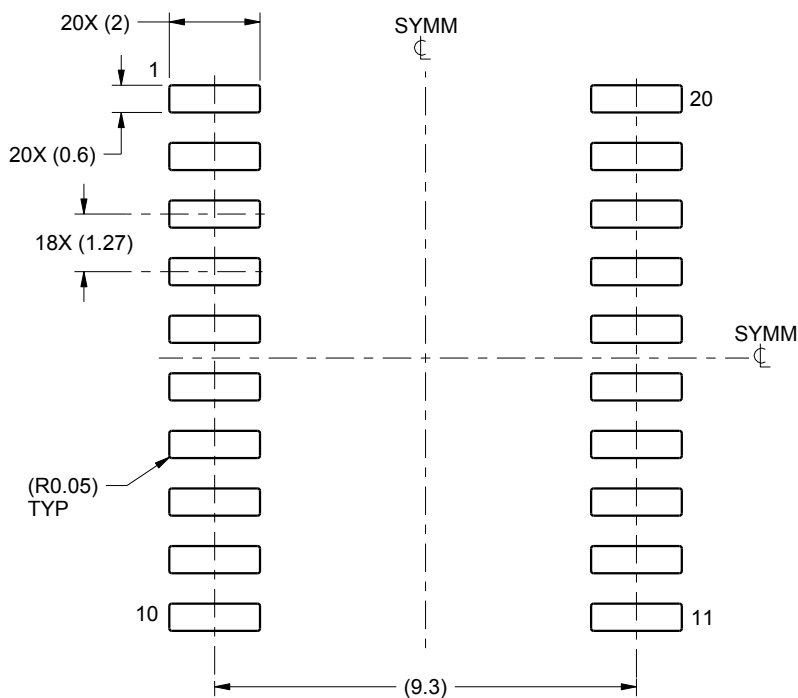
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

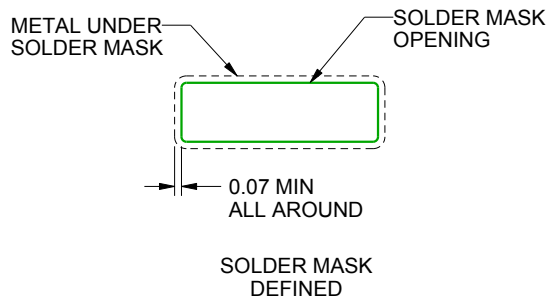
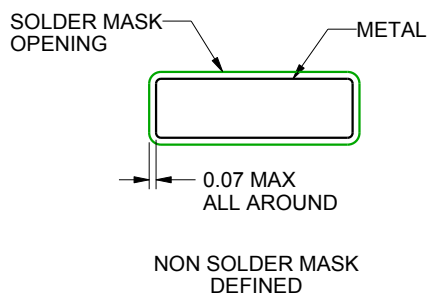
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

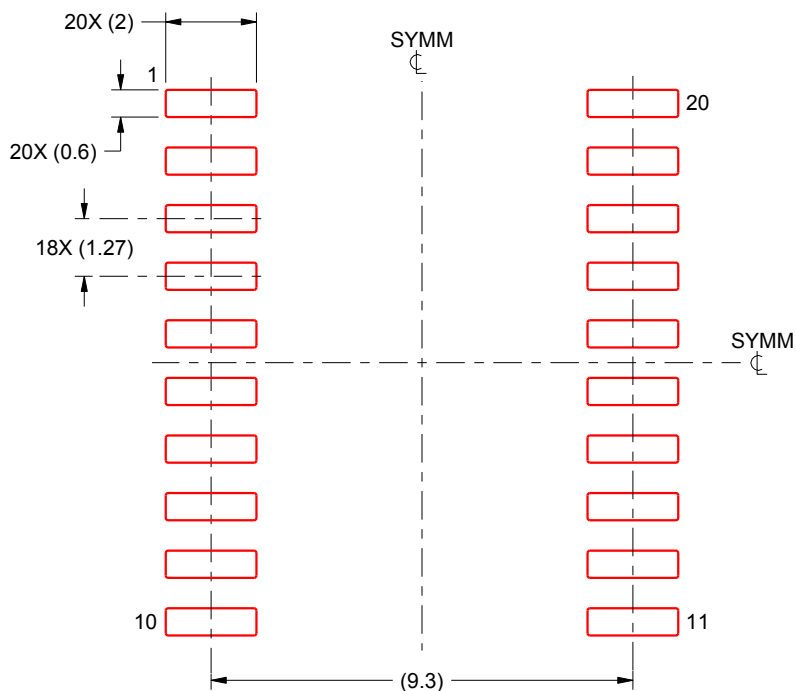
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含みいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、TI は一切の責任を拒否します。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、[TI の総合的な品質ガイドライン](#)、[ti.com](https://www.ti.com) または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月