TEXAS INSTRUMENTS
CDCDB803
JAJSKP6A – AUGUST 2021 – REVISED MAY 2022

CDCDB803 PCIe Gen 1～Gen 6 向け DB800ZL 準拠 8 出力クロック・バッファ

1 特長

- 8 つの LP-HCSL 出力、プログラム可能な内蔵 85Ω (デフォルト) または 100Ω 差動出力終端付き
- 8 つのハードウェア出力イネーブル (OE#) 制御
- PCIe Gen 6 フィルタ後の付加位相ジッタ：20fs RMS (最大値)
- PCIe Gen 5 フィルタ後の付加位相ジッタ：25fs RMS (最大値)
- DB2000Q フィルタ後の付加位相ジッタ：38fs RMS (最大値)
- 共通クロック (CC) アーキテクチャと個別リファレンス (IR) アーキテクチャをサポート
  - スペクトラム拡散対応
- 出力間スキュー：<50ps
- 入出力間遅延：<3ns
- フェイルセーフ入力
- プログラム可能な出力スルーレート制御
- 9 つの選択可能な SMBus アドレス
- コアおよび入出力電源電圧：3.3V
- ハードウェア制御による低消費電力モード (PD#)
- 消費電流：72mA (最大値)
- 6mm × 6mm、48 ピン VQFN パッケージ

2 アプリケーション

- マイクロサーバー / タワー・サーバー
- ストレージ・エリア・ネットワーク (SAN) およびホスト・バス・アダプタ (HBA) カード
- ネットワーク接続ストレージ (NAS)
- ハードウェア・アクセラレータ
- ラック・サーバー

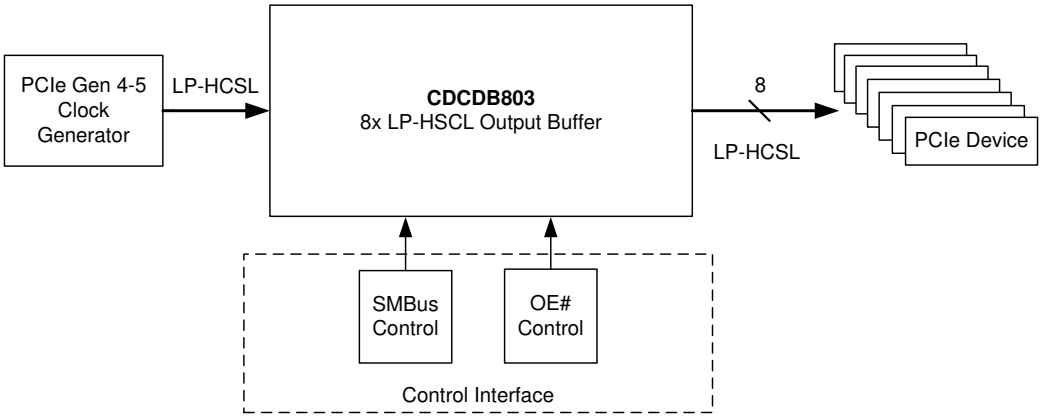
3 説明

CDCDB803 は、PCIe Gen 1 ~ 6、QuickPath Interconnect (QPI)、UPI、SAS、SATA インターフェイス用のリファレンス・クロックを分配できる 8 出力 LP-HCSL、DB800ZL 準拠クロック・バッファです。SMBus インターフェイスおよび 8 本の出力イネーブル・ピンにより、8 個の出力すべてを個別に設定および制御できます。CDCDB803 は DB800ZL から派生したバッファであり、DB800ZL 仕様のシステム・パラメータと同等またはそれを上回る性能を備えています。また、DB2000Q 仕様のパラメータと同等またはそれを上回る性能も備えています。CDCDB803 は、6mm × 6mm の 48 ピン VQFN パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
CDCDB803	VQFN (48)	6.00mm × 6.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



CDCDB803 システム図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 説明 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 6
6.1 Absolute Maximum Ratings ... 6
6.2 ESD Ratings ... 6
6.3 Recommended Operating Conditions ... 6
6.4 Thermal Information ... 6
6.5 Electrical Characteristics ... 7
6.6 Timing Requirements ... 9
6.7 Typical Characteristics ... 10
7 Parameter Measurement Information ... 11
8 Detailed Description ... 12
8.1 Overview ... 12
8.2 Functional Block Diagram ... 12
8.3 Feature Description ... 12
8.4 Device Functional Modes ... 13
8.5 Programming ... 14
8.6 Register Maps ... 16
9 Application and Implementation ... 20
9.1 Application Information ... 20
9.2 Typical Application ... 20
10 Power Supply Recommendations ... 22
11 Layout ... 23
11.1 Layout Guidelines ... 23
11.2 Layout Examples ... 23
12 Device and Documentation Support ... 25
12.1 Device Support ... 25
12.2 Receiving Notification of Documentation Updates ... 25
12.3 サポート・リソース ... 25
12.4 Trademarks ... 25
12.5 Electrostatic Discharge Caution ... 25
12.6 Glossary ... 25
13 Mechanical, Packaging, and Orderable Information ... 25

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (August 2021) to Revision A (May 2022)	Page
• データシートのタイトルを更新	1
• データシートに PCIe Gen 6 を追加	1
• Changed the pin descriptions for pins 5, 8 and 46	3

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5 Pin Configuration and Functions

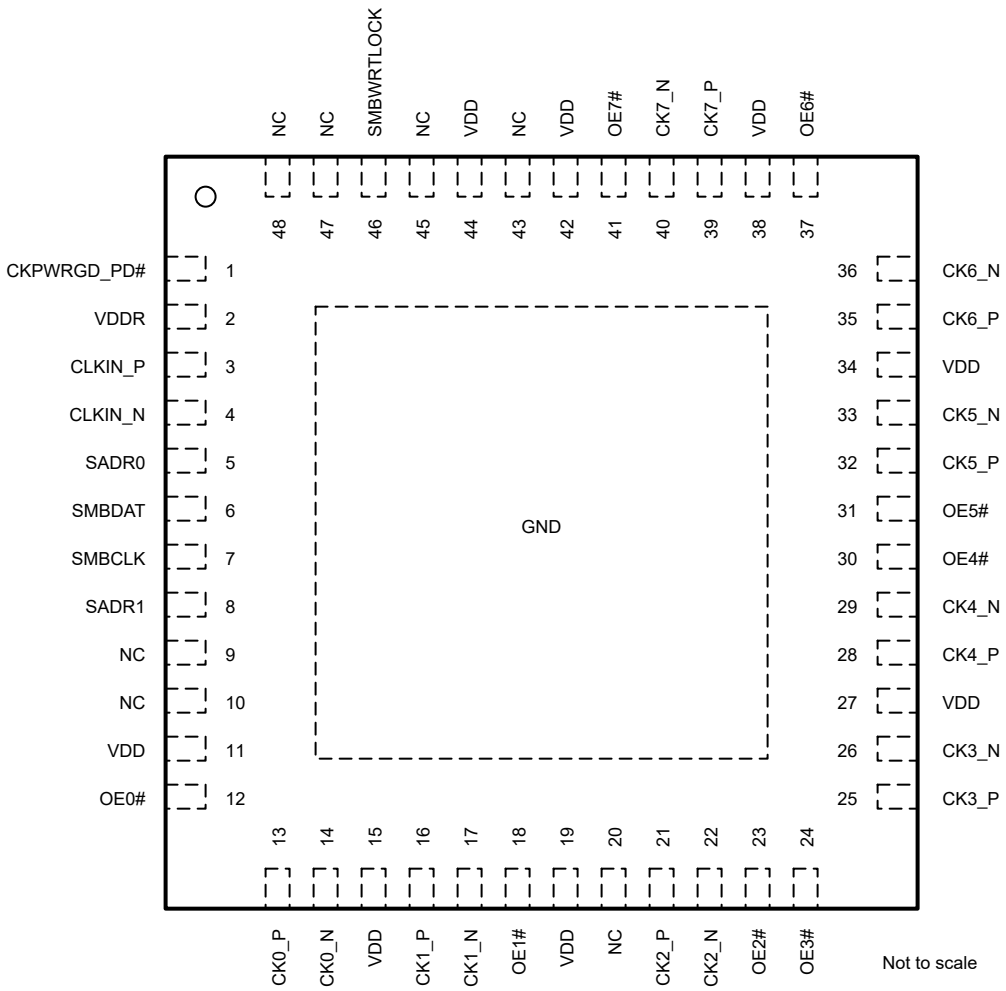


図 5-1. CDCDB803 RSL Package 48-Pin VQFN Top View

表 5-1. Pin Functions

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
INPUT CLOCK			
CLKIN_P	3	I	LP-HCSL differential clock input. Typically connected directly to the differential output of clock source.
CLKIN_N	4	I	
OUTPUT CLOCKS			
CK0_P	13	O	LP-HCSL differential clock output of channel 0. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK0_N	14	O	
CK1_P	16	O	LP-HCSL differential clock output of channel 1. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK1_N	17	O	

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表 5-1. Pin Functions (continued)

PIN		TYPE[2]	DESCRIPTION
NAME	NO.		
CK2_P	21	O	LP-HCSL differential clock output of channel 2. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK2_N	22	O	
CK3_P	25	O	LP-HCSL differential clock output of channel 3. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK3_N	26	O	
CK4_P	28	O	LP-HCSL differential clock output of channel 4. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK4_N	29	O	
CK5_P	32	O	LP-HCSL differential clock output of channel 5. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK5_N	33	O	
CK6_P	35	O	LP-HCSL differential clock output of channel 6. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK6_N	36	O	
CK7_P	39	O	LP-HCSL differential clock output of channel 7. Typically connected directly to PCIe differential clock input. If unused, the pins can be left no connect.
CK7_N	40	O	
MANAGEMENT AND CONTROL [1]			
CKPWRGD_PD#	1	I, S, PD	Clock Power Good and Power Down multi-function input pin with internal 180-kΩ pulldown. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. After PWRGD has been asserted high for the first time, the pin becomes a PD# pin and it controls power-down mode: LOW: Power-down mode, all output channels tri-stated. HIGH: Normal operation mode.
OE0#	12	I, S, PD	Output Enable for channel 0 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 0. HIGH: disable output channel 0.
OE1#	18	I, S, PD	Output Enable for channel 1 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 1. HIGH: disable output channel 1.
OE2#	23	I, S, PD	Output Enable for channel 2 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 2. HIGH: disable output channel 2.
OE3#	24	I, S, PD	Output Enable for channel 3, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 3. HIGH: disable output channel 3.
OE4#	30	I, S, PD	Output Enable for channel 4, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 4. HIGH: disable output channel 4.
OE5#	31	I, S, PD	Output Enable for channel 5, with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 5. HIGH: disable output channel 5.
OE6#	37	I, S, PD	Output Enable for channel 6 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 6. HIGH: disable output channel 6.
OE7#	41	I, S, PD	Output Enable for channel 7 with internal 180-kΩ pulldown, active low. Typically connected to GPIO of microcontroller. If unused, the pin can be left no connect. LOW: enable output channel 7. HIGH: disable output channel 7.
SMBUS AND SMBUS ADDRESS			

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表 5-1. Pin Functions (continued)

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
SADR0	5	I, S, PU / PD	SMBus address strap bit[0]. This is a 3-level input that is decoded in conjunction with pin 8 to set SMBus address. It has internal 180-kΩ pullup / pulldown network biasing to GND when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration input, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground.
SMBDAT	6	I / O	Data pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k.
SMBCLK	7	I	Clock pin of SMBus interface. Typically pulled up to 3.3-V VDD using external pullup resistor. The recommended pullup resistor value is > 8.5k.
SADR1	8	I, S, PU / PD	SMBus address strap bit[1]. This is a 3-level input that is decoded in conjunction with pin B4 to set SMBus address. It has internal 180-kΩ pullup / pulldown network biasing to GND when no connect. For a high-level input configuration, the pin should be pulled up to 3.3-V VDD through an external pullup resistor from 1k to 5k with 5% tolerance. For a low-level input configuration, the pin should be pulled down to ground through an external pulldown resistor from 1k to 5k with 5% tolerance. For a mid-level input configuration, the pin should be left floating and not connected to VDD or ground.
SMBWRTLOCK	46	I, PD	SMBWRTLOCK: Disables write commands on SMBus. All writes will be ignored when SMBWRTLOCK is asserted (reads are not affected). Internal 180-kΩ pulldown, active high. 0 = SMBus write enabled. 1 = SMBus write disabled.
SUPPLY VOLTAGE AND GROUND			
VDDR	2	P	Power supply input for input clock receiver. Connect to 3.3-V power supply rail with decoupling capacitor to GND. Place a 0.1-µF capacitor close to each supply pin between power supply and ground.
VDD	11, 15, 19, 27, 34, 38, 42, 44	P	3.3-V power supply for output channels and core voltage.
GND	DAP	G	Ground. Connect ground pad to system ground.
NO CONNECT			
NC	9, 10, 20, 43, 45	—	Do not connect to GND or VDD.
NC	47, 48	—	No connect. Pins may be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the Absolute Maximum Ratings.

(1) The “#” symbol at the end of a pin name indicates that the active state occurs when the signal is at a low voltage level. When “#” is not present, the signal is active high.

(2) The definitions below define the I/O type for each pin.

- I = Input
- O = Output
- I / O = Input / Output
- PU / PD = Internal 180-kΩ Pullup / Pulldown network biasing to VDD/2
- PD = Internal 180-kΩ Pulldown
- S = Hardware Configuration Pin
- P = Power Supply
- G = Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}, V_{DD_R}	Power supply voltage	−0.3	3.6	V
V_{IN}	IO input voltage	−0.3	3.6	V
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature	−65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±3500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	IO, Core supply voltage	3	3.3	3.6	V
V_{DD_R}	Input supply voltage	3	3.3	3.6	V
T_A	Ambient temperature	−40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		Device Package RSL (QFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

VDD, VDD_R = 3.3 V ± 5 %, −40°C ≤ T_A ≤ 105°C. Typical values are at VDD = VDD_R = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CONSUMPTION						
I_{DD_R}	Core supply current	Active mode. CKPWRGD_PD# = 1			9	mA
		Power-down mode. CKPWRGD_PD# = 0			2.2	
I_{DD}	IO supply current	All outputs disabled			18	mA
		All outputs active, 100MHz (Per output)			7.8	
		Power-down mode. CKPWRGD_PD# = 0			1.5	
CLOCK INPUT						
f_{IN}	Input frequency		50	100	250	MHz
V_{IN}	Input voltage swing	Differential voltage between CLKIN_P and CLKIN_N(1)	200		2300	$mV_{Diff-peak}$
dV/dt	Input voltage edge rate	20% - 80% of input swing	0.7			V/ns
DV_{CROSS}	Total variation of V_{CROSS}	Total variation across V_{CROSS}		140		mV
DC_{IN}	Input duty cycle		40		60	%
C_{IN}	Input capacitance(2)	Differential capacitance between CLKIN_P and CLKIN_N pins		2.2		pF
CLOCK OUTPUT						
f_{OUT}	Output frequency		50	100	250	MHz
C_{OUT}	Output capacitance(1)	Differential capacitance between CKx_P and CKx_N pins		4		pF
V_{OH}	Output high voltage	Single-ended(2) (3)	225		270	mV
V_{OL}	Output low voltage		10		150	
V_{HIGH}	Output high voltage	Measured into an AC load as defined in DB800ZL	660		850	
V_{LOW}	Output low voltage	Measured into an AC load as defined in DB800ZL	–150		150	
V_{MAX}	Output Max voltage	Measured into an AC load as defined in DB800ZL			1150	
V_{CROSS}	Crossing point voltage	(3) (4)	130		200	
$V_{CROSSAC}$	Crossing point voltage (AC load)	Measured into an AC load as defined in DB800ZL	250		550	
DV_{CROSS}	Total variation of V_{CROSS}	Variation of V_{CROSS} (3) (4)		35	140	
V_{ovs}	Overshoot voltage	(3)			V_{OH}+75	
$V_{ovs(AC)}$	Overshoot voltage (AC load)	Measured into an AC load as defined in DB800ZL			V_{HIGH}+300	
V_{uds}	Undershoot voltage	(3)			V_{OL}–75	
$V_{uds(AC)}$	Undershoot voltage	Measured into an AC load as defined in DB800ZL			V_{LOW}–300	mV
V_{rb}	Ringback Voltage	Measured into an AC load as defined in DB800ZL and taken from Single Ended waveform (relative to V_{HIGH} and V_{LOW})	-0.2		0.2	V
Z_{DIFF}	Differential impedance (Default setting, 85 Ω)	Measured at V_{OL}/V_{OH}	81	85	89	Ω
	Differential impedance (Output impedance selection bit =1, 100 Ω)	Measured at V_{OL}/V_{OH}	95	100	105	
Z_{DIFF_CROSS}	Differential impedance (Default setting, 85 Ω)	Measured at V_{CROSS}	68	85	102	
	Differential impedance (Output impedance selection bit = 1, 100 Ω)	Measured at V_{CROSS}	80	100	120	

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VDD, VDD_R = 3.3 V ± 5 %, −40°C ≤ T_A ≤ 105°C. Typical values are at VDD = VDD_R = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{EDGE}	Differential edge rate	Measured (+-150 mV) around V_{CROSS} (7)		2		4	V/ns
Dt_{EDGE}	Edge rate matching	Measured (+-75 mV) V_{CROSS} (7)				20	%
t_{STABLE}	Power good assertion to stable clock output	CKPWRGD_PD# pin transitions from 0 to 1, f_{IN} = 100 MHz	Measured when positive output reaches 0.2V			1.8	ms
$t_{DRIVE_PD\#}$	Power good assertion to outputs driven high	CKPWRGD_PD# pin transitions from 0 to 1, f_{IN} = 100 MHz	Measured when positive output reaches 0.2V			300	µs
t_{OE}	Output enable assertion to stable clock output	OEx# pin transitions from 1 to 0				10	CLKIN Periods
t_{OD}	Output enable de-assertion to no clock output	OEx# pin transitions from 0 to 1				10	
t_{PD}	Power-down assertion to no clock output	CKPWRGD_PD# pin transitions from 1 to 0				3	
t_{DCD}	Duty cycle distortion	Differential; f_{IN} = 100MHz, f_{IN_DC} = 50%		–1		1	%
t_{DLY}	Propagation delay	(5)		0.5		3	ns
t_{SKEW}	Skew between outputs	(6)				50	ps
$t_{DELAY(IN-OUT)}$	Input to output delay variation	Input-to-output delay variation at 100 MHz across voltage and temperature		–250		250	ps
$J_{CKx_DB2000Q}$ (7)	Additive jitter for DB2000Q	DB2000Q filter, for input of 200 mV differential swing @ 1.5 V/ns				0.038	ps, RMS
J_{CKx_PCIE} (7)	Additive jitter for PCIe6.0	PLL BW: 0.5 - 1 MHz; CDR = 10 MHz	Input clock slew rate = 2 V/ns			0.02	ps, RMS
	Additive jitter for PCIe5.0	PCIe5.0 filter				0.025	
	Additive jitter for PCIe4.0	PLL BW = 2 - 5 MHz; CDR = 10 MHz	Input clock slew rate ≥ 1.8 V/ns			0.06	
	Additive jitter for PCIe3.0		Input clock slew rate ≥ 0.6 V/ns			0.1	
J_{CKx}	Additive jitter	f_{IN} = 100 MHz; slew rate ≥ 3 V/ns; 12 kHz to 20 MHz integration bandwidth.			100	160	fs, RMS
NF	Noise floor	f_{IN} = 100 MHz; f_{Offset} ≥ 10 MHz	Input clock slew rate ≥ 3 V/ns		–160	-155	dBc/Hz
SMBUS INTERFACE, OEx#, CKPWRGD_PD#							
V_{IH}	High level input voltage			2.0			V
V_{IL}	Low level input voltage					0.8	
I_{IH}	Input leakage current	With internal pull-up/pull-down	GND ≤ V_{IN} ≤ V_{DD}	–30		30	µA
I_{IL}	Input leakage current	With internal pull-up/pull-down	GND ≤ V_{IN} ≤ V_{DD}	–30		30	µA
I_{IH}	Input leakage current	Without internal pull-up/pull-down	GND ≤ V_{IN} ≤ V_{DD}	−5		5	µA
I_{IL}	Input leakage current	Without internal pull-up/pull-down	GND ≤ V_{IN} ≤ V_{DD}	−5		5	µA

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VDD, VDD_R = 3.3 V ± 5 %, −40°C ≤ T_A ≤ 105°C. Typical values are at VDD = VDD_R = 3.3 V, 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance				4.5		pF
C_{OUT}	Output capacitance				4.5		pF
3-LEVEL DIGITAL INTERFACE (SADR0, SADR1)							
V_{IH}	High level input voltage			2.3			V
V_{IM}	Mid level input voltage			1.25	V_{DD}/2	1.725	
V_{IL}	Low level input voltage					0.85	
I_{IH}	Input leakage current	With internal pull-up/pull-down	V_{IN} = V_{DD}	–30		30	µA
I_{IL}	Input leakage current	With internal pull-up/pull-down	V_{IN} = GND	–30		30	µA
C_{IN}	Input capacitance(1)				4.5		pF

(1) Voltage swing includes overshoot.
(2) Not tested in production. Ensured by design and characterization.
(3) Measured into DC test load.
(4) V_{CROSS} is single-ended voltage when CKx_P = CKx_N with respect to system ground. Only valid on rising edge of CKx, when CKx_P is rising.
(5) Measured from rising edge of CLK_IN to any CKx output.
(6) Measured from rising edge of any CKx output to any other CKx output.
(7) Measured into AC test load.

6.6 Timing Requirements

VDD, VDD_R = 3.3 V ± 5 %, −40°C ≤ T_A ≤ 105°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
SMBUS-COMPATIBLE INTERFACE TIMING						
f_{SMB}	SMBus operating frequency		10		400	kHz
t_{BUF}	Bus free time between STOP and START		4.7			µs
t_{HD_STA}	START condition hold time	SMBCLK low after SMBDAT low	4			
t_{SU_STA}	START condition setup time	SMBCLK high before SMBDAT low	4.7			
t_{SU_STO}	STOP condition setup time		4			
t_{HD_DAT}	SMBDAT hold time		300			ns
t_{SU_DAT}	SMBDAT setup time		250			
$t_{TIMEOUT}$	Detect SMBCLK low timeout	In terms of device input clock frequency	1e6			cycles
t_{LOW}	SMBCLK low period		4.7			µs
t_{HIGH}	SMBCLK high period		4		50	
t_F	SMBCLK/SMBDAT fall time(1)				300	ns
t_R	SMBCLK/SMBDAT rise time(2)				1000	

(1) TF = (VIHMIN + 0.15) to (VILMAX - 0.15)
(2) TR = (VILMAX - 0.15) to (VIHMIN + 0.15)

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6.7 Typical Characteristics

図 6-1 shows both the phase noise of the source as well as the output of the DUT (CDCDB803). It can be seen from the phase noise plot that the DUT has a very low phase noise profile with total jitter of 71 fs, rms. If we rms subtract the clock reference noise, the additive jitter of CDCDB803 under typical conditions would be lower than 71 fs, rms.

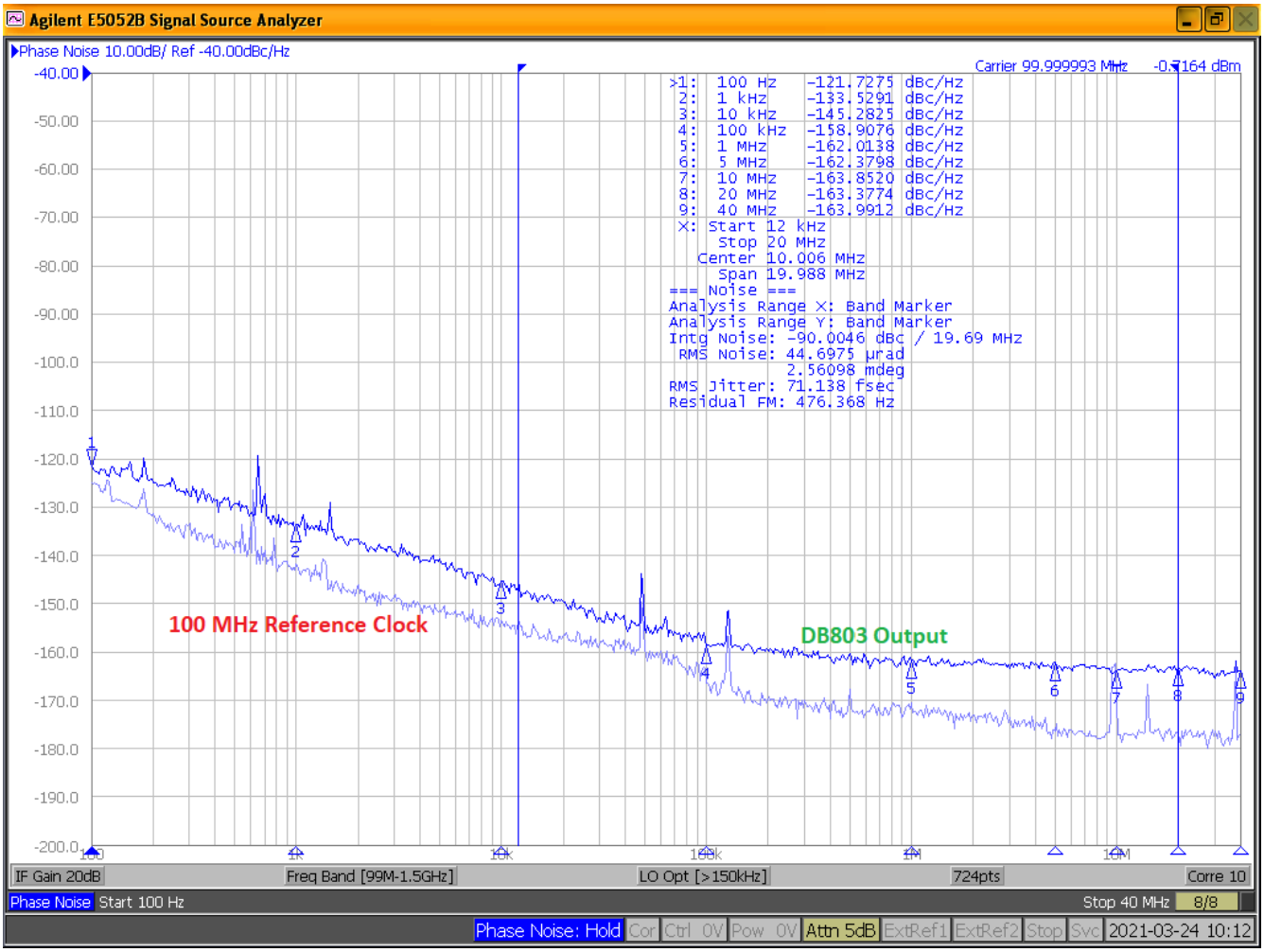


図 6-1. CDCDB803 Clock Out (CK0:8) Phase Noise

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7 Parameter Measurement Information

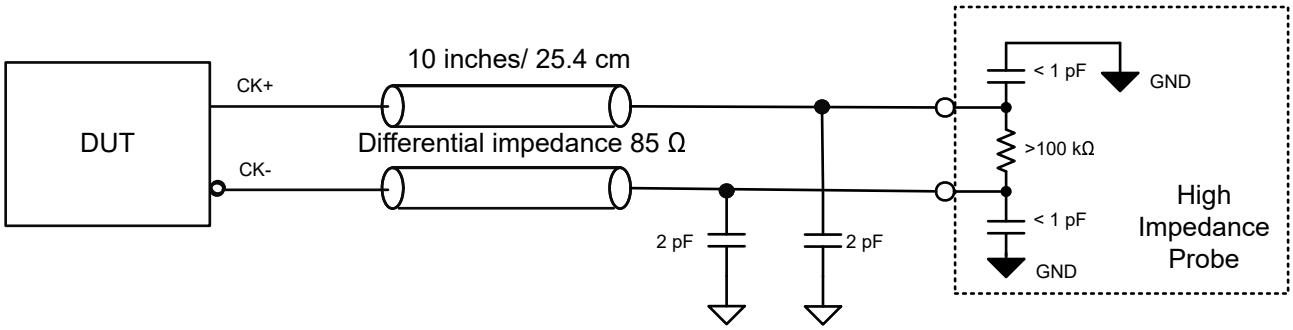
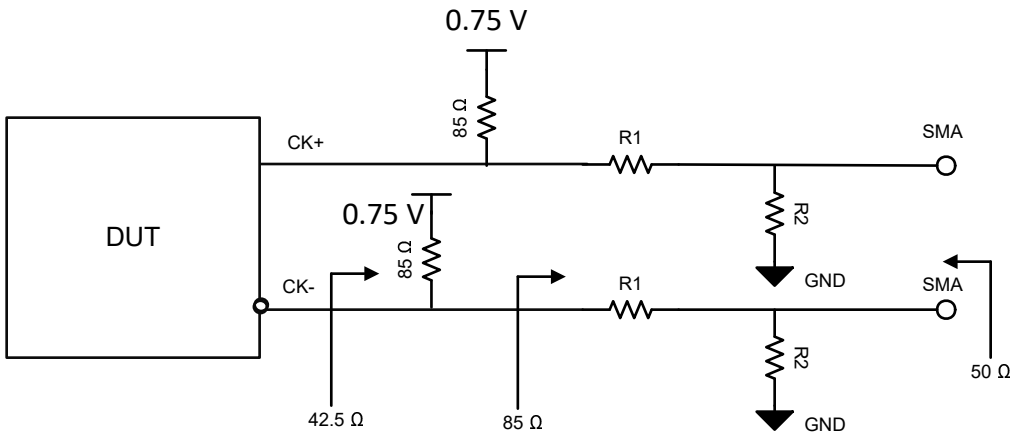


図 7-1. AC Test Load (Referencing Intel DB2000QL Document)



R1 = 47 Ω and R2 = 147 Ω.

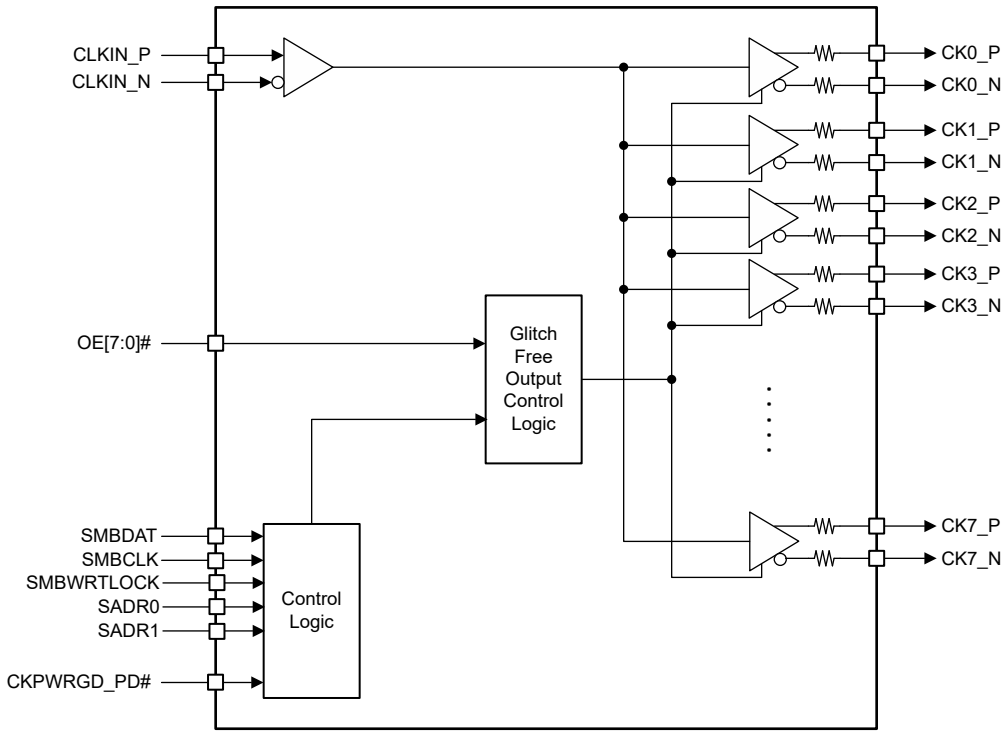
図 7-2. DC Simulation Load (Referencing Intel DB2000QL Document)

8 Detailed Description

8.1 Overview

The CDCDB803 is a low additive-jitter, low propagation delay clock buffer designed to meet the strict performance requirements for PCIe Gen 1-6, QPI, UPI, SAS, and SATA reference clocks. The CDCDB803 allows buffering and replication of a single clock source to up to eight individual outputs in the LP-HCSL format. The CDCDB803 also includes status and control registers accessible by an SMBus version 2.0 compliant interface. The device integrates a large amount of external passive components to reduce overall system cost.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fail-Safe Input

The CDCDB803 is designed to support fail-safe input operation feature. This feature allows the user to drive the device inputs before V_{DD} is applied without damaging the device. Refer to the *Absolute Maximum Ratings* table for more information on the maximum input supported by the device.

8.3.2 Output Enable Control

The CDCDB803 uses SMBus and OE# to control the state of the output channels. The OE# pins control the state of the output with the same number. For example, the OE5# pin controls the state of the CK5 output driver. The SMBus registers may enable or disable the output when the corresponding OE# pin is held low.

8.3.3 SMBus

The CDCDB803 has an SMBus interface that is active only when CKPWRGD_PD# = 1. The SMBus allows individual enable/disable of each output.

When CKPWRGD_PD# = 0, the SMBus pins are placed in a Hi-Z state, but all register settings are retained. The SMBus register values are only retained while V_{DD} remains inside of the recommended operating voltage.

8.3.3.1 SMBus Address Assignment

The SMBus address is assigned by configuration of two pins (SADR1 and SADR0) that each support three levels. This configuration allows the CDCDB803 to assume nine different SMBus addresses.

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The SMBus address pins are sampled when PWRGD is set to 1. See 表 8-1 for address pin configuration. The address can only be changed by power cycling the device.

表 8-1. SMBus Address Assignment

SADR1	SADR0	SMBus ADDRESS : WRITE OPERATION (READ/WRITE=0)	SMBus ADDRESS : READ OPERATION (READ/WRITE=1)
L	L	0xD8	0xD9
L	M	0xDA	0xDB
L	H	0xDE	0xDF
M	L	0xC2	0xC3
M	M	0xC4	0xC5
M	H	0xC6	0xC7
H	L	0xCA	0xCB
H	M	0xCC	0xCD
H	H	0xCE	0xCF

8.4 Device Functional Modes

8.4.1 CKPWRGD_PD# Function

The CKPWRGD_PD# pin is used to set two state variables inside of the device: PWRGD and PD#. The PWRGD and PD# variables control which functions of the device are active at any time, as well as the state of the input and output pins.

The PWRGD and PD# states are multiplexed on the CKPWRGD_PD# pin. CKPWRGD_PD# must remain below V_{OL} and not exceed V_{DDR} + 0.3 V until V_{DD} and V_{DDR} are present and within the recommended operating conditions. After CKPWRGD_PD# is set high, a valid CLKIN must be present to use PD#.

The first rising edge of the CKPWRGD_PD# pin sets PWRGD = 1. After PWRGD is set to 1, the CKPWRGD_PD# pin is used to assert PD# mode only. PWRGD variable will only be cleared to 0 with the removal of V_{DD} and V_{DDR}.

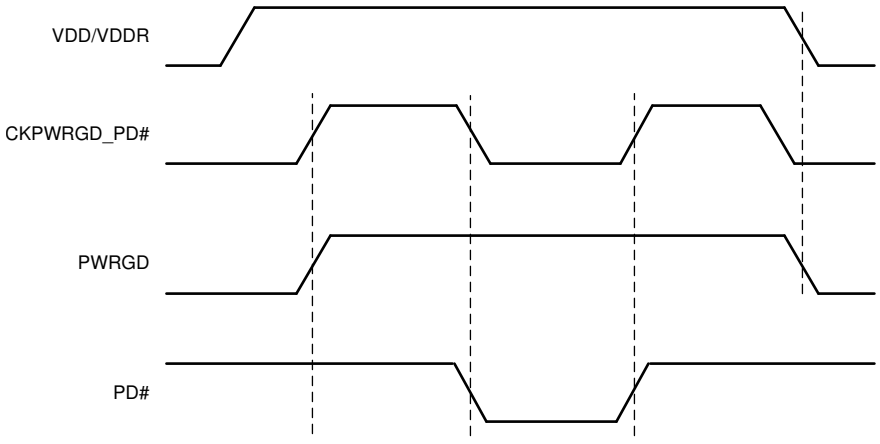


図 8-1. PWRGD and PD# State Changes

8.4.2 OE[7:0]# and SMBus Output Enables

Each output channel, 0 to 7, can be individually enabled or disabled by a SMBus control register bit, called SMB enable bits. Additionally, each output channel has a dedicated, corresponding, OE[7:0]# hardware pin. The OE[7:0]# pins are asynchronously asserted-low signals that may enable or disable the output.

Refer to 表 8-2 for enabling and disabling outputs through the hardware and software. Note that both the SMB enable bit must be a 1 and the OEx# pin must be an input low voltage 0 for the output channel to be active.

表 8-2. OE[7:0]# Functionality

Control Inputs	Power State Variables (Internal)		CLKIN	OE[7:0]# HARDWARE PINS AND SMBus CONTROL REGISTER BITS			CK[7:0]_P/ CK[7:0]_N
CKPWRGD_PD#	PWRGD	PD#		OE[7:0]#	OUT_EN_CLK[7:0]	DRIVE_OP_STATE_CTRL	
0	0	0	X	X	X	X	LOW/LOW
1	1	1	X(1)	X	0	0	LOW/LOW
						1	TRI-STATE
				1	X	0	LOW/LOW
						1	TRI-STATE
			Running(1)	0	1	X	Running
0		0	X(2)	X	X	0	LOW/LOW
						1	TRI-STATE

(1) To enter the power-down state, CLKIN must remain active for at least 3 clock cycles after CKPWRGD_PD# transitions from 1 to 0.
(2) To enter the powered-up state with active clock outputs, CLKIN must be active before CKPWRGD_PD# transitions from 0 to 1.

8.4.3 Output Slew Rate Control

The CDCDB803 provides output slew rate control feature which customer can use to compensate for increased output trace length based on their board design. The slew rate of a bank of 4 outputs 0 to 3 and 4 to 7, can be changed within a given range by a SMBus control register called CAPTRIM. Refer to 表 8-16 for more information.

8.4.4 Output Impedance Control

The integrated termination on the CDCDB803 can be programmed either for 85 Ω or 100 Ω. This flexibility ensures that the customer can use the same device across various applications irrespective of the characteristic board impedance which is typically either 85 Ω or 100 Ω. This termination resistor can be changed for all the outputs as whole using bit 5 of a register called OUTSET. Refer to 表 8-14 for more information.

8.5 Programming

The CDCDB803 uses SMBus to program the states of its eight output drivers. See *SMBus* for more information on the SMBus programming, and *Register Maps* for information on the registers.

表 8-3. Command Code Definition

BIT	DESCRIPTION
7	0 = *Block Read* or *Block Write* operation 1 = *Byte Read* or *Byte Write* operation
(6:0)	Register address for *Byte* operations, or starting register address for *Block*, operations

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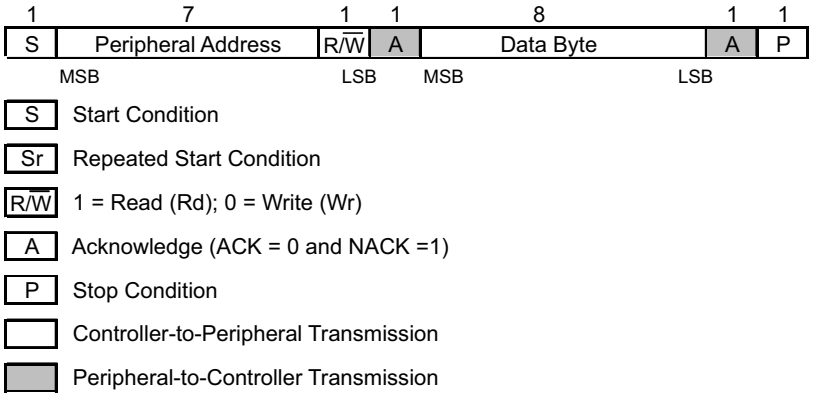


図 8-2. Generic Programming Sequence

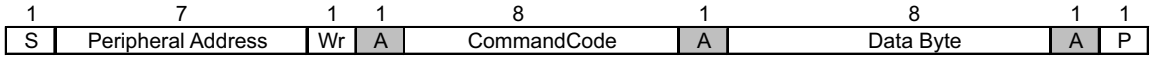


図 8-3. Byte Write Protocol

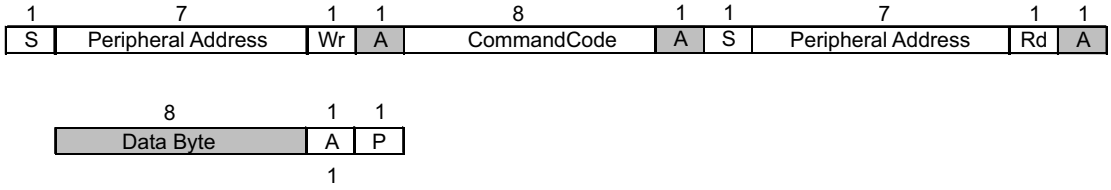


図 8-4. Byte Read Protocol

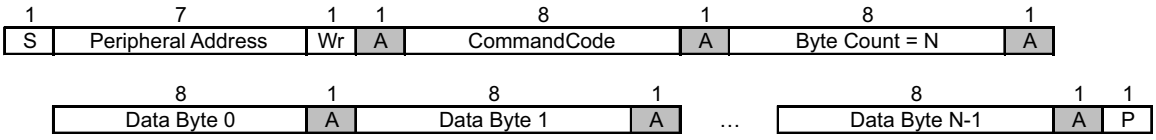


図 8-5. Block Write Protocol

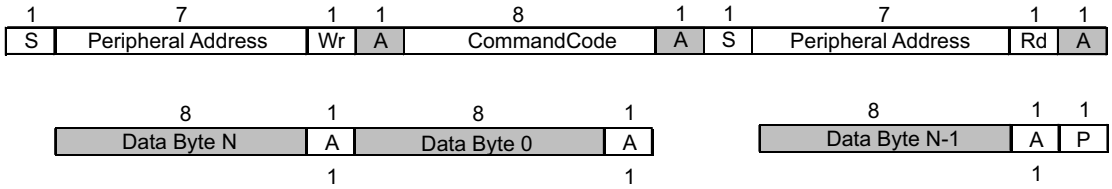


図 8-6. Block Read Protocol

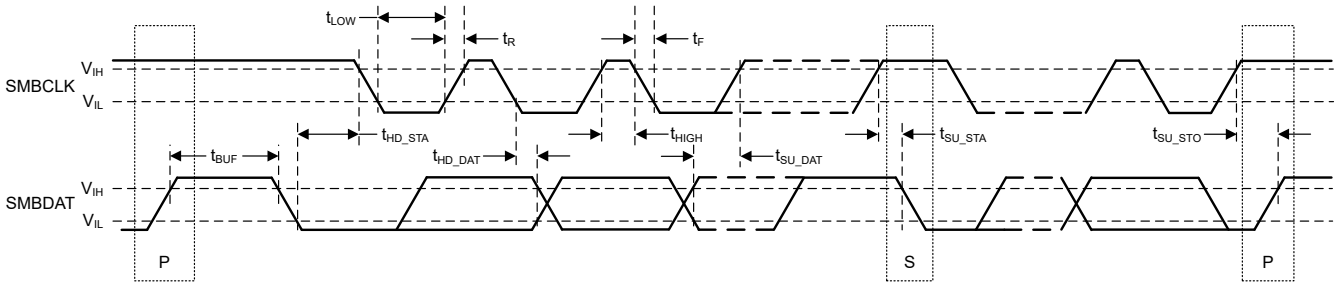


図 8-7. SMBus Timing Diagram

8.6 Register Maps

8.6.1 CDCDB803 Registers

表 8-4 lists the CDCDB803 registers. All register locations not listed in 表 8-4 should be considered as reserved locations and the register contents should not be modified.

表 8-4. CDCDB803 Registers

Address	Acronym	Register Name	Section
0h	RCR1	Reserved Control Register 1	Go
1h	OECR1	Output Enable Control 1	Go
2h	OECR2	Output Enable Control 2	Go
3h	OERDBK	Output Enable# Pin Read Back	Go
4h	RCR2	Reserved Control Register 2	Go
5h	VDRREVID	Vendor/Revision Identification	Go
6h	DEVID	Device Identification	Go
7h	BTRDCNT	Byte Read Count Control	Go
8h	OUTSET	Output Setting Control	Go
4Ch	CAPTRIM	Slew Rate Capacitor Cluster 1 & 2	Go

Complex bit access types are encoded to fit into small table cells. 表 8-5 shows the codes that are used for access types in this section.

表 8-5. CDCDB803 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 RCR1 Register (Address = 0h) [reset = 47h]

RCR1 is shown in 表 8-6.

Return to the Summary Table.

The RCR1 register contains reserved bits.

表 8-6. RCR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Reserved	R	4h	Reserved.
3-0	Reserved	R/W	7h	Writing to these bits will not affect the functionality of the device.

8.6.1.2 OECR1 Register (Address = 1h) [reset = FFh]

OECR1 is shown in OECR1 Register Field Descriptions.

Return to the Summary Table.

The OECR1 register contains bits that enable or disable individual output clock channels [5:0].

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表 8-7. OECR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_EN_CLK5	R/W	1h	This bit controls the output enable signal for output channel CK5_P/CK5_N. 0h = Output Disabled 1h = Output Enabled
6	OUT_EN_CLK4	R/W	1h	This bit controls the output enable signal for output channel CK4_P/CK4_N. 0h = Output Disabled 1h = Output Enabled
5	OUT_EN_CLK3	R/W	1h	This bit controls the output enable signal for output channel CK3_P/CK3_N. 0h = Output Disabled 1h = Output Enabled
4	OUT_EN_CLK2	R/W	1h	This bit controls the output enable signal for output channel CK2_P/CK2_N. 0h = Output Disabled 1h = Output Enabled
3	Reserved	R/W	1h	Writing to this bit will not affect the functionality of the device.
2	OUT_EN_CLK1	R/W	1h	This bit controls the output enable signal for output channel CK1_P/CK1_N. 0h = Output Disabled 1h = Output Enabled
1	OUT_EN_CLK0	R/W	1h	This bit controls the output enable signal for output channel CK0_P/CK0_N. 0h = Output Disabled 1h = Output Enabled
0	Reserved	R/W	1h	Writing to this bit will not affect the functionality of the device.

8.6.1.3 OECR2 Register (Address = 2h) [reset = 0Fh]

OECR2 is shown in OECR2 Register Field Descriptions.

Return to the Summary Table.

The OECR2 register contains bits that enable or disable individual output clock channels [7:6].

表 8-8. OECR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	Reserved	R/W	1h	Writing to these bits will not affect the functionality of the device.
2	OUT_EN_CLK7	R/W	1h	This bit controls the output enable signal for output channel CK7_P/CK7_N. 0h = Output Disabled 1h = Output Enabled
1	Reserved	R/W	1h	Writing to this bit will not affect the functionality of the device.
0	OUT_EN_CLK6	R/W	1h	This bit controls the output enable signal for output channel CK6_P/CK6_N. 0h = Output Disabled 1h = Output Enabled

8.6.1.4 OERDBK Register (Address = 3h) [reset = 0h]

OERDBK is shown in 表 8-9.

Return to the Summary Table.

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The OERDBK register contains bits that report the current state of the OE[7:0]# input pins.

表 8-9. OERDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RB_OE7	R	0h	This bit reports the logic level present on the OE7# pin.
6	RB_OE6	R	0h	This bit reports the logic level present on the OE6# pin.
5	RB_OE5	R	0h	This bit reports the logic level present on the OE5# pin.
4	RB_OE4	R	0h	This bit reports the logic level present on the OE4# pin.
3	RB_OE3	R	0h	This bit reports the logic level present on the OE3# pin.
2	RB_OE2	R	0h	This bit reports the logic level present on the OE2# pin.
1	RB_OE1	R	0h	This bit reports the logic level present on the OE1# pin.
0	RB_OE0	R	0h	This bit reports the logic level present on the OE0# pin.

8.6.1.5 RCR2 Register (Address = 4h) [reset = 0h]

RCR2 is shown in RCR2 Register Field Descriptions.

Return to the Summary Table.

The RCR2 register contains reserved bits.

表 8-10. RCR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Reserved	R	0h	Reserved.

8.6.1.6 VDRREVID Register (Address = 5h) [reset = 0Ah]

VDRREVID is shown in 表 8-11.

Return to the Summary Table.

The VDRREVID register contains a vendor identification code and silicon revision code.

表 8-11. VDRREVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	REV_ID	R	0h	Silicon revision code. Silicon revision code bits [3:0] map to register bits [7:4] directly.
3-0	VENDOR_ID	R	Ah	Vendor identification code. Vendor ID bits [3:0] map to register bits [3:0] directly.

8.6.1.7 DEVID Register (Address = 6h) [reset = E7h]

DEVID is shown in 表 8-12.

Return to the Summary Table.

The DEVID register contains a device identification code.

表 8-12. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DEV_ID	R	E7h	Device ID code. Device ID bits[7:0] map to register bits[7:0] directly.

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8.6.1.8 BTRDCNT Register (Address = 7h) [reset = 8h]

BTRDCNT is shown in 表 8-13.

Return to the Summary Table.

The BTRDCNT register contains bits [4:0] which configure the number of bytes which will be read back.

表 8-13. BTRDCNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	Reserved	R/W	0h	Writing to these bits will not affect the functionality of the device.
4	BYTE_COUNTER	R/W	0h	Writing to this register configures how many bytes will be read back.
3-0	BYTE_COUNTER	R/W	8h	

8.6.1.9 OUTSET Register (Address = 8h) [reset = 0h]

OUTSET is shown in 表 8-14.

Return to the Summary Table.

Bit5 of the OUTSET register sets the termination for all the outputs while bit4 can be used to set the power-down state for all outputs. The remaining bits for this register are reserved.

表 8-14. OUTSET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved.
5	CH_ZOUT_SEL	R/W	0h	Select between 85 Ω (0) and 100 Ω (1) Output impedance
4	d_DRIVE_OP_STATE_CTRL	R/W	0h	Power-down state of all output clocks. 0: LOW/LOW 1: TRI_STATE
3-0	Reserved	R/W	0h	Register bits can be written to 0. Writing a different value than 0 will affect device functionality.

8.6.1.10 CAPTRIM Register (Address = 4Ch) [reset = 66h]

CAPTRIM is shown in 表 8-16.

Return to the Summary Table.

Bits [7:4] of the CAPTRIM register is used to control the slew rate for output channel cluster 2. Bits [3:0] control the slew rate for output channel cluster 1. Refer below for cluster identification.

表 8-15. Cluster Identification

Cluster	Outputs
1	CK3, CK2, CK1, CK0
2	CK7, CK6, CK5, CK4

表 8-16. CAPTRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CLUSTER2_CAP_TRIM	R/W	6h	Slew Rate Reduction Cap Trim for Cluster 2. Default value of 6h. 0: minimum F: maximum
3-0	CLUSTER1_CAP_TRIM	R/W	6h	Slew Rate Reduction Cap Trim for Cluster 1. Default value of 6h. 0: minimum F: maximum

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9 Application and Implementation

Note

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9.1 Application Information

The CDCDB803 is a fanout buffer that supports PCIe generation 4 and PCIe generation 5 REFCLK distribution. The device is used to distribute up to eight copies of a typically 100-MHz clock.

9.2 Typical Application

図 9-1 shows a CDCDB803 typical application. In this application, a clock generator provides a 100-MHz reference to the CDCDB803 which then distributes that clock to PCIe endpoints. The clock generator may be a discrete clock generator like the CDCI6214 or it may be integrated in a larger component such as a Platform Controller Hub (PCH) or application processor.

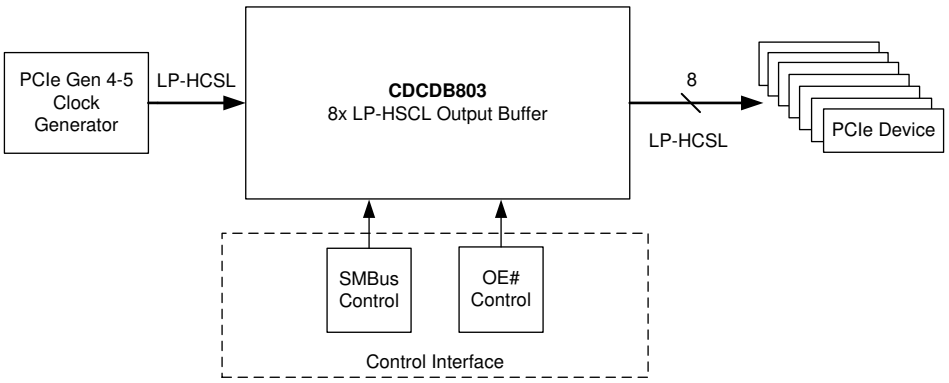


図 9-1. Typical Application

9.2.1 Design Requirements

Consider a typical server motherboard application which must distribute a 100-MHz PCIe reference clock from the PCH of a processor chipset to multiple endpoints. An example of clock input and output requirements is:

- Clock Input:
  - 100-MHz LP-HCSL
- Clock Output:
  - 2x 100-MHz to processors, LP-HCSL
  - 3x 100-MHz to riser/retimer, LP-HCSL
  - 3x 100-MHz to DDR memory controller, LP-HCSL

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9.2.2 Detailed Design Procedure

The following items must be determined before starting design of a CDCDB803 socket:

- Output Enable Control Method
- SMBus address

9.2.2.1 Output Enable Control Method

The device provides an option to either use SMBus programmed registers (software) to control the outputs or by using the hardware OE# pins. In case of using software to control the outputs, the hardware OE# pins can be left floating as each of these pins have a pulldown to ground. Refer to 表 8-2 and the *Register Maps* section for more information on programming the register.

When the user wants to control the outputs with the hardware OE# pins, they can do so for example by connecting these pins to a GPIO controller and follow the *Pin Configuration and Functions* section to set the outputs to HIGH/LOW. The bits OUT_EN_CLK7 to OUT_EN_CLK0 used to control the outputs are shown in registers OECR1 (表 8-7) and OECR2 (表 8-8). These register bits are set to 1 by default to ensure that the outputs are "software enabled" and their state is therefore set by hardware OE# pins.

9.2.2.2 SMBus Address

An SMBus address should be selected from the listed potential addresses in 表 8-1. The appropriate pullup or pulldown resistor should be placed on the SADRx pins as indicated in the table. Ensure the SMBus address is not already in use to avoid conflict.

9.2.3 Application Curves

図 6-1 in the *Typical Characteristics* section can be used as both an application curve and a typical characteristics plot in this example.

The 図 9-2 and 図 9-3 show characterization data for the Output slew rate for various CAPTRIM codes and across temperature. Customers can use these plots as reference for choosing the appropriate output slew rate based on their system requirement.

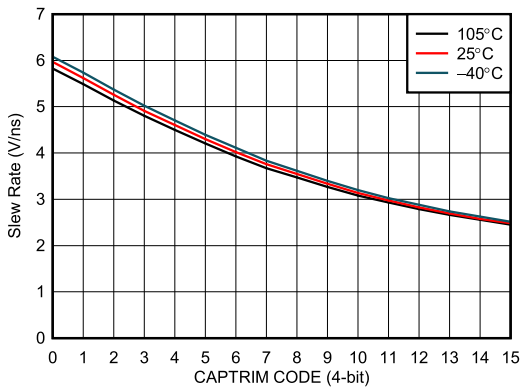


図 9-2. Output Slew Rate vs. CAPTRIM Code

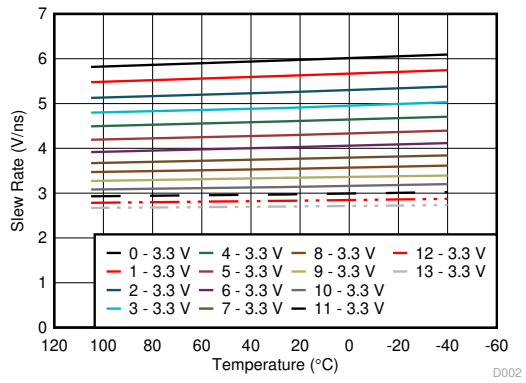


図 9-3. Slew Rate Variation Across Temperature for Different CAPTRIM Code

10 Power Supply Recommendations

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when the jitter and phase noise is critical to applications.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guards the power-supply system against induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, place the capacitors very close to the power-supply terminals and lay out with short loops to minimize inductance. TI recommends to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock buffer. These beads prevent the switching noise from leaking into the board supply. It is imperative to choose an appropriate ferrite bead with very low DC resistance to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply terminals that is greater than the minimum voltage required for proper operation.

図 10-1 shows the recommended power supply filtering and decoupling method.

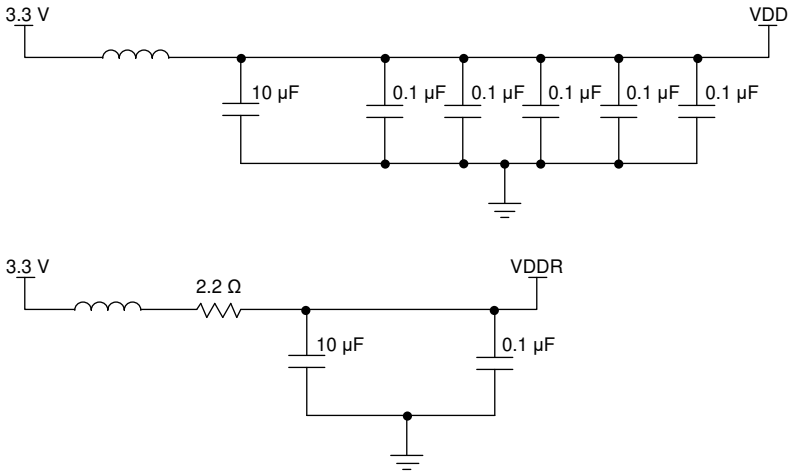


図 10-1. Power Supply Decoupling

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11 Layout

11.1 Layout Guidelines

The following section provides the layout guidelines to ensure good thermal performance and power supply connections for the CDCDB803.

In *Layout Examples*, the CDCDB803 has 85-Ω differential output impedance LP-HCSL format drivers as per register default settings. All transmission lines connected to CKx pins should be 85-Ω differential impedance, 42.5-Ω single-ended impedance to avoid reflections and increased radiated emissions. If 100-Ω output impedance is enabled, the transmission lines connected to CKx pins should be 100-Ω differential impedance, 50-Ω single-ended impedance. Take care to eliminate or reduce stubs on the transmission lines.

11.2 Layout Examples

図 11-1 through 図 11-3 are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

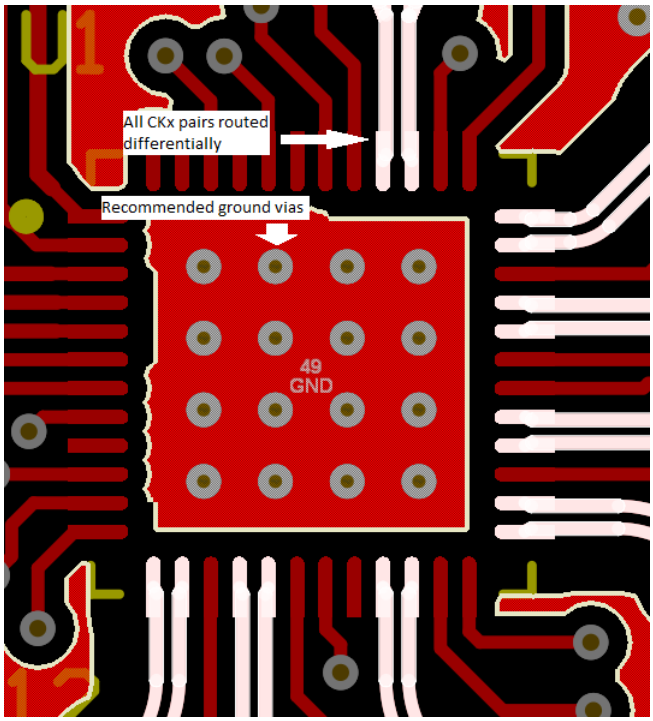


図 11-1. PCB Layout Example for CDCDB803, Top layer

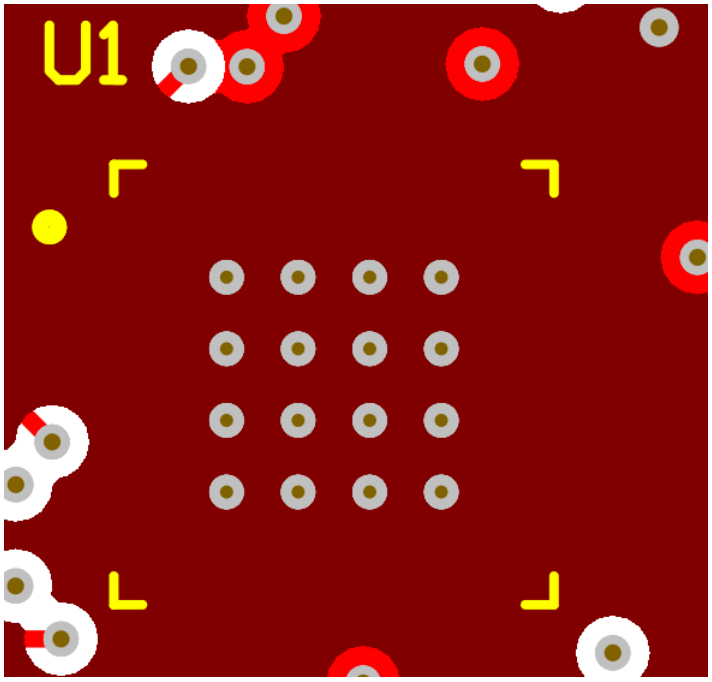


図 11-2. PCB Layout Example for CDCDB803, GND Layer

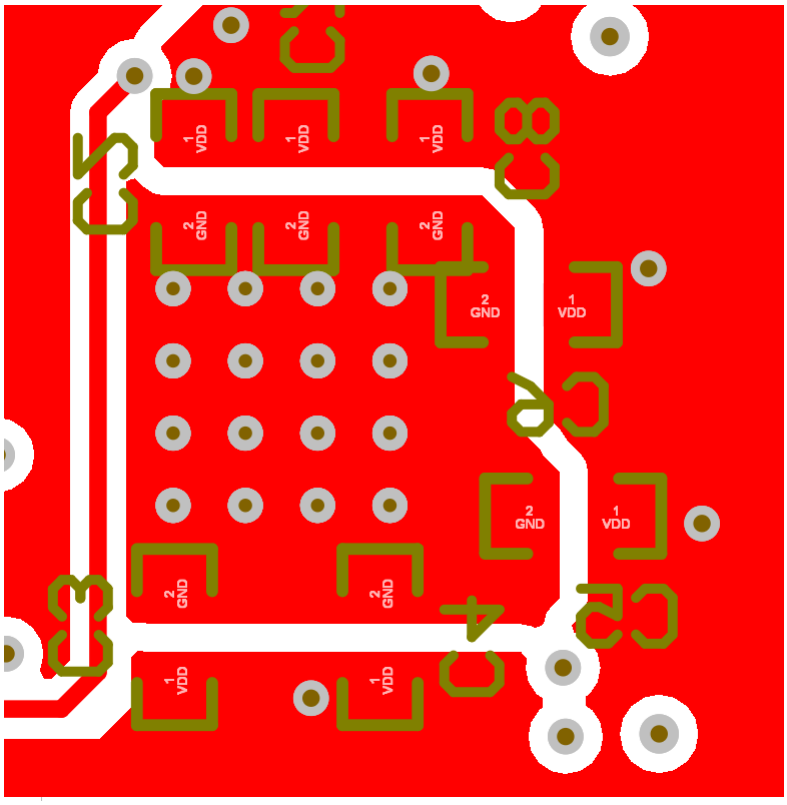


図 11-3. PCB Layout Example for CDCDB803, Bottom Layer

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12 Device and Documentation Support

12.1 Device Support

12.1.1 TICS Pro

TICS Pro is an offline software tool for EVM programming and also for register map generation to program a device configuration for a specific application. For TICS Pro, go to https://www.ti.com/tool/TICSPRO-SW.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCDB803ERSLR	Active	Production	VQFN (RSL) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803ERSLR.A	Active	Production	VQFN (RSL) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803ERSLT	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803ERSLT.A	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803RSLR	Active	Production	VQFN (RSL) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803RSLR.A	Active	Production	VQFN (RSL) | 48	4000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803RSLT	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803
CDCDB803RSLT.A	Active	Production	VQFN (RSL) | 48	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	CDCB803

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

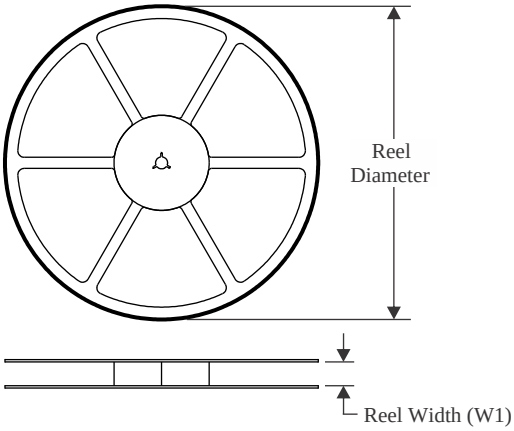
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

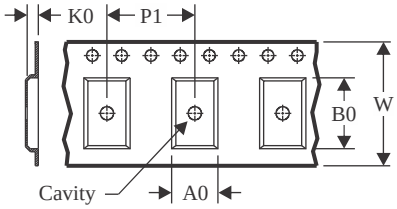
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

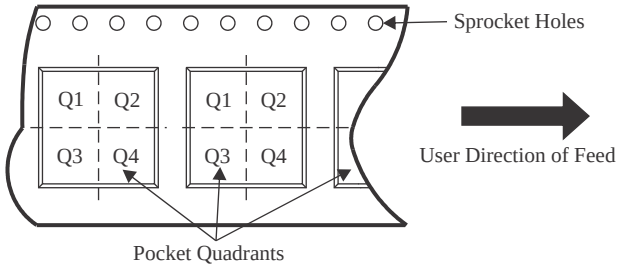


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

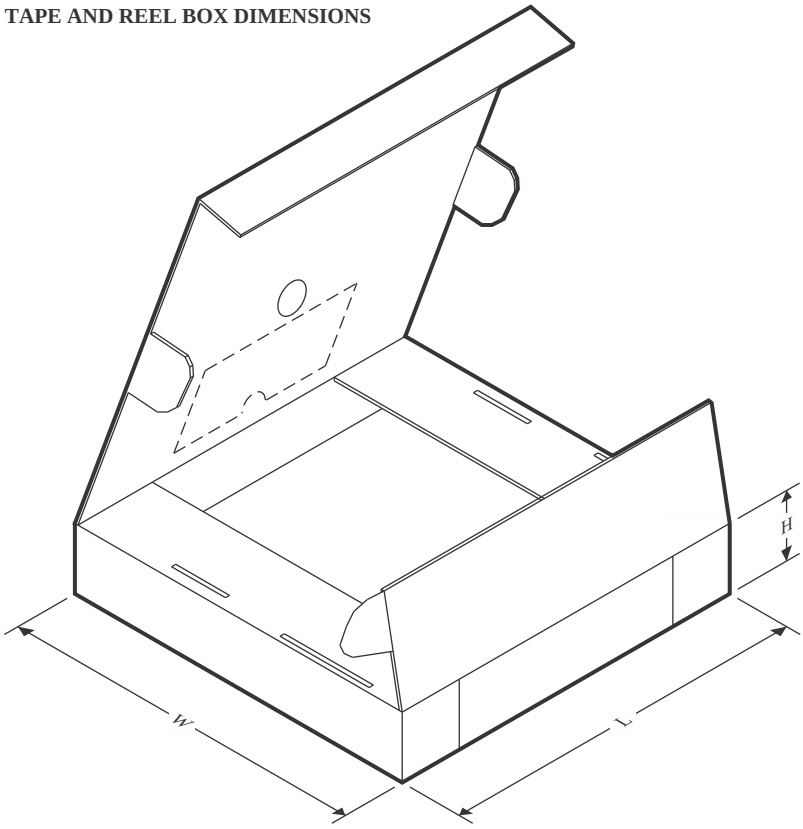
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCDB803ERSLR	VQFN	RSL	48	4000	330.0	16.4	6.3	6.3	1.3	8.0	16.0	Q1
CDCDB803ERSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.3	8.0	16.0	Q1
CDCDB803RSLR	VQFN	RSL	48	4000	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
CDCDB803RSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCDB803ERSLR	VQFN	RSL	48	4000	360.0	360.0	36.0
CDCDB803ERSLT	VQFN	RSL	48	250	210.0	185.0	35.0
CDCDB803RSLR	VQFN	RSL	48	4000	353.0	353.0	32.0
CDCDB803RSLT	VQFN	RSL	48	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

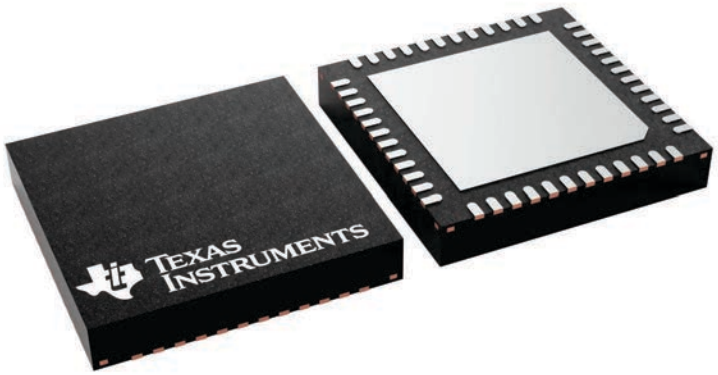
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



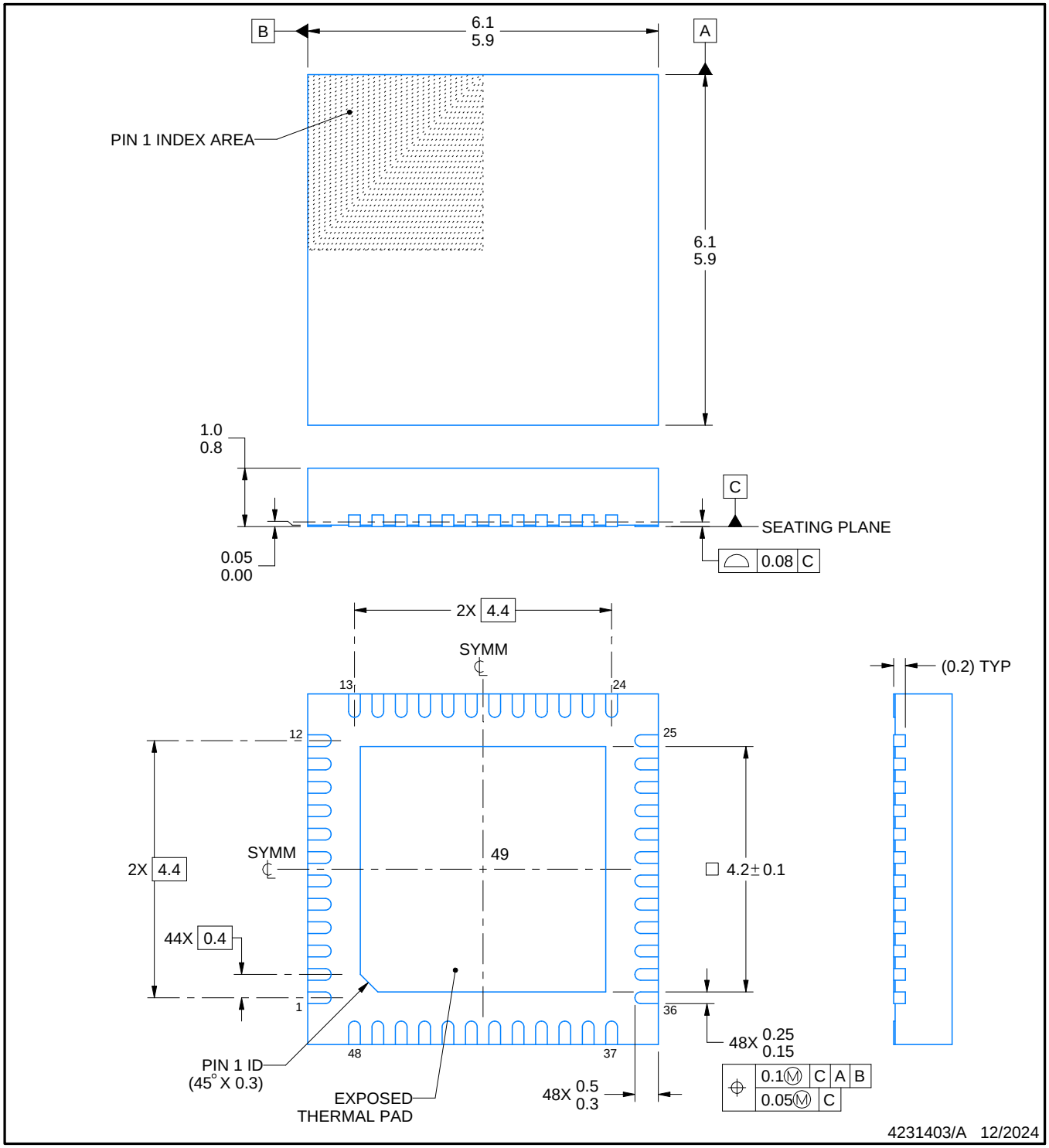
4225749/A

RSL0048G

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

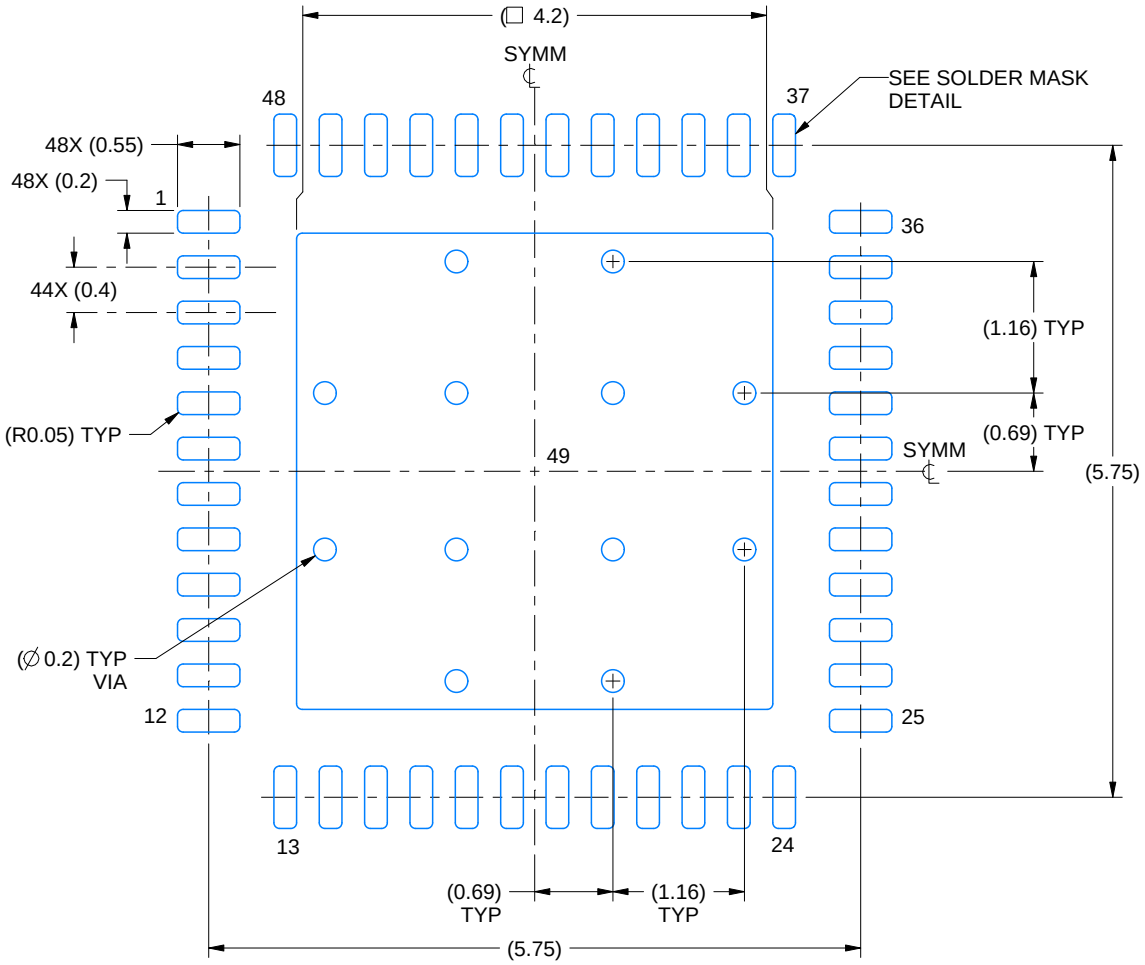
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

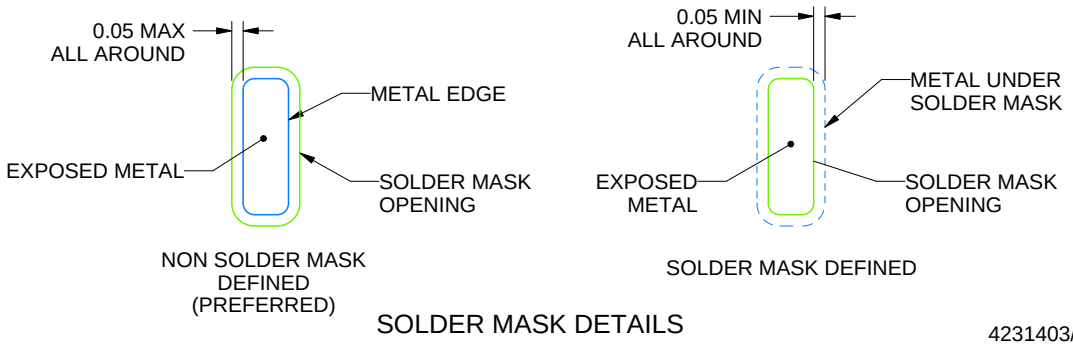
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

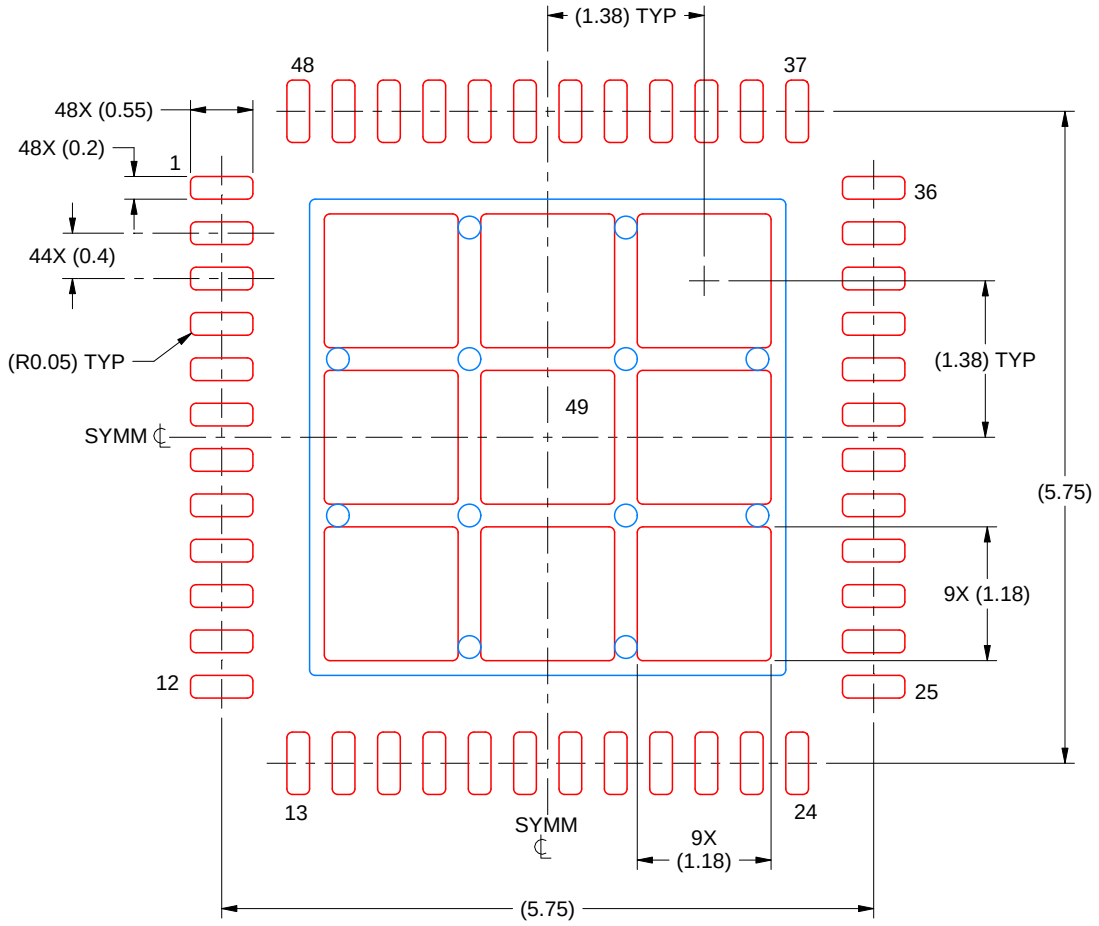


SOLDER MASK DETAILS

4231403/A 12/2024

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月