

SSC Clock Generator/Buffer

FEATURES

- Part of a Family of Easy to use Clock Generator Devices With Optional SSC
- SSC Capable Clock Generator / Buffer
- SSC Controllable via 3 External Pins
 - $\pm 0\%$ to $\pm 1.5\%$ Center Spread
- 1 External Control Pin for SSC ON / OFF Selection
- 40 MHz to 108 MHz Single-Ended LVCMOS Input
- Single 3.3V Device Power Supply
- Wide Temperature Range – 40°C to 85°C
- Low Space Consumption by 8 Pin TSSOP Package

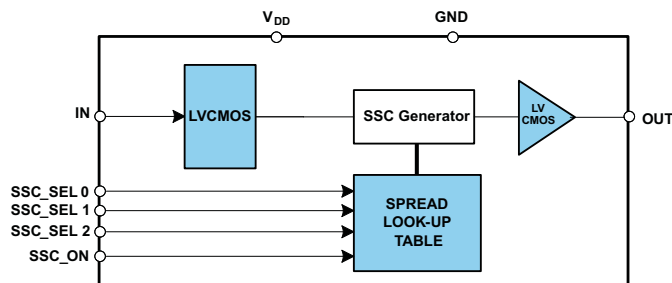
APPLICATIONS

- Consumer and Industrial Applications Requiring EMI Reduction through Spread Spectrum Clocking

PACKAGE

IN	1	8	VDD
SSC_SEL 0	2	7	SSC_SEL 2
SSC_SEL 1	3	6	OUT
GND	4	5	SSC_ON

BLOCK DIAGRAM



DESCRIPTION

The CDCS501 is a spread spectrum capable, LVCMOS Input Clock Buffer for EMI reduction.

The device is designed to counter common EMI problems in modern electronic designs.

It accepts a 3.3V LVCMOS signal at the input and spread this signal by a small amount, centered around the input frequency. The amount of spread can be selected via 3 control pins. The Functional Table contains detailed information on the amount of spread. A 4th control pin can be used to activate or deactivate the Spread Spectrum Clock Generator.

Selecting SSC_ON = off will turn the Spread Spectrum Clock Generator off only. The device will still pass the LVCMOS signal that's presented at its input through to its output. This pin is low active.

The wide operating frequency range covers most commonly used midrange Audio and Video frequencies. The CDCS501 operates in 3.3V environment.

It is characterized for operation from –40°C to 85°C, and available in an 8-pin TSSOP package.



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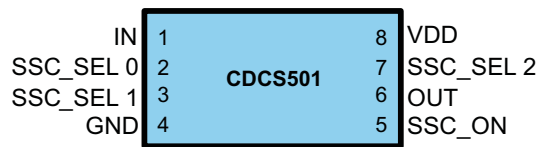
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTION TABLE

SSC_ON	SSC_SEL 0	SSC_SEL 1	SSC_SEL 2	SPREAD AMOUNT
1	x	x	X	0.00%
0	0	0	0	1.00%
0	0	0	1	1.50%
0	0	1	0	1.00%
0	0	1	1	1.50%
0	1	0	0	0.50%
0	1	0	1	0.75%
0	1	1	0	0.00%
0	1	1	1	0.50%

DEVICE INFORMATION

PACKAGE



PIN FUNCTIONS

PIN			
NAME	NO.	Type	Description
IN	1	I	LVC MOS Clock Input
OUT	6	O	LVC MOS Clock Output
SSC_SEL 0, 1, 2	2, 3, 7	I	Spread Selection Pins, internal Pull-up
SSC_ON	5	I	SSC on/off Pin, active low; internal Pull-down
VDD	8	Power	3.3V Power Supply
GND	4	Ground	Ground

PACKAGE THERMAL RESISTANCE FOR TSSOP (PW) PACKAGE⁽¹⁾

CDCS501PW 8-PIN TSSOP			THERMAL AIRFLOW (CFM)				UNIT
			0	150	250	500	
R _{θJA}	High K		149	142	138	132	°C / W
	Low K		230	185	170	150	
R _{θJc}	High K	65					°C / W
	Low K	69					

(1) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V _{DD}	Supply voltage range	–0.5 to 4.6	V
V _{IN}	Input voltage range	–0.5 to 4.6	V
V _{out}	Output voltage range	–0.5 to 4.6	V
I _{IN}	Input current (V _I < 0, V _I > V _{DD})	20	mA
I _{out}	Continuous output current	50	mA
T _{ST}	Storage temperature range	–65 to 150	°C
T _J	Maximum junction temperature	125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V _{DD}	Supply voltage	3.0		3.6	V
f _{IN}	Input Frequency	40		108	MHz
V _{IL}	Low level input voltage LVCMOS			0.3 V _{DD}	V
V _{IH}	High level input voltage LVCMOS	0.7 V _{DD}			V
V _I	Input Voltage threshold LVCMOS		0.5 V _{DD}		V
C _L	Output Load Test LVCMOS			15	pF
I _{OH} /I _{OL}	Output Current			12	mA
T _A	Operating free-air temperature	–40		85	°C

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Device supply current	$f_{IN} = 80 \text{ MHz}$		26		mA
f_{OUT}	Output frequency		40		108	MHz
I_{IH}	LVC MOS input current	$V_I = V_{DD}; V_{DD} = 3.6V$			10	μA
I_{IL}	LVC MOS input current	$V_I = 0 \text{ V}; V_{DD} = 3.6V$			-10	μA
V_{OH}	LVC MOS high-level output voltage	$I_{OH} = -0.1mA$	2.9			V
		$I_{OH} = -8mA$	2.4			
		$I_{OH} = -12mA$	2.2			
V_{OL}	LVC MOS low-level output voltage	$I_{OL} = 0.1mA$			0.1	V
		$I_{OL} = 8mA$			0.5	
		$I_{OL} = 12mA$			0.8	
$t_{JIT(C-C)}$	Cycle to cycle jitter cycles	$f_{out} = 80 \text{ MHz}; SSC = 1\%, 10000 \text{ cycles}$		110		ps
t_r/t_f	Rise and fall time	20%–80%		0.75		ns
O_{dc}	Output duty cycle		45%		55%	
f_{MOD}	Modulation frequency			30		kHz

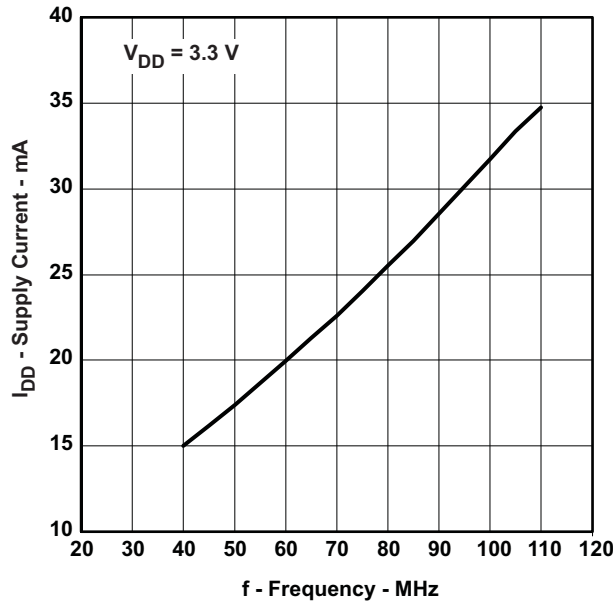


Figure 1. I_{DD} vs. Input Frequency, $V_{DD} = 3.3V$

APPLICATION INFORMATION

SSC MODULATION

The exact implementation of the SSC modulation plays a vital role for the EMI reduction. The CDCS501 uses a triangular modulation scheme implemented in a way that the modulation frequency depends on the VCO frequency of the internal PLL and the spread amount is independent from the VCO frequency.

The modulation frequency can be calculated by using the below formula.

$$f_{\text{mod}} = f_{\text{IN}} / 2480$$

PARAMETER MEASUREMENT INFORMATION

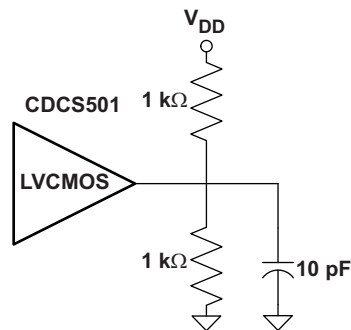


Figure 2. Test Load

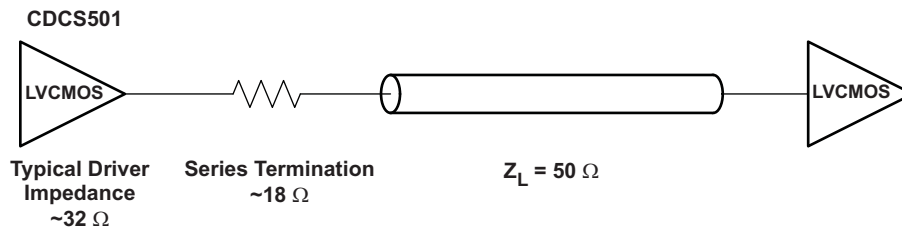


Figure 3. Test Load for 50-Ω Board Environment

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CDCS501PW	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS501
CDCS501PW.B	Active	Production	TSSOP (PW) 8	150 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS501
CDCS501PWR	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS501
CDCS501PWR.B	Active	Production	TSSOP (PW) 8	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CS501

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCS501PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCS501PWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDCS501PW	PW	TSSOP	8	150	530	10.2	3600	3.5
CDCS501PW.B	PW	TSSOP	8	150	530	10.2	3600	3.5

PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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