TEXAS INSTRUMENTS
CSD87355Q5D
JAJSDT1A – MARCH 2016 – REVISED SEPTEMBER 2017

CSD87355Q5D 同期整流降圧 NexFET™パワー・ブロック

1 特長

- ハーフ・ブリッジ・パワー・ブロック
- 25A時に92.5%のシステム効率
- 最大45Aで動作
- 高周波数での動作(最高1.5MHz)
- 高密度SON、占有面積5mm×6mm
- 5Vゲートの駆動に最適化
- 低いスイッチング損失
- インダクタンスが非常に低いパッケージ
- RoHS準拠
- ハロゲン不使用
- 鉛不使用の端子メッキ処理

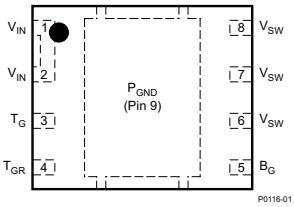
2 アプリケーション

- 同期降圧コンバータ
  - 高周波数のアプリケーション
  - 大電流、低デューティ・サイクルのアプリケーション
- マルチフェーズの同期整流降圧コンバータ
- POL DC/DCコンバータ
- IMVP、VRM、VRDアプリケーション

3 概要

CSD87355Q5D NexFET™パワー・ブロックは、同期整流降圧アプリケーションに最適化された設計で、大電流、高効率、高周波数の能力を小さな5mm×6mmの外形に収めています。この製品は5Vのゲート駆動アプリケーション用に最適化されており、外部のコントローラ/ドライバからの任意の5Vゲート・ドライブと組み合わせて、高密度の電源を実現できます。

上面図

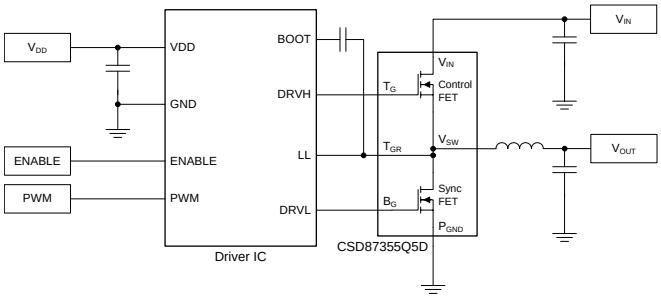


注文情報(1)

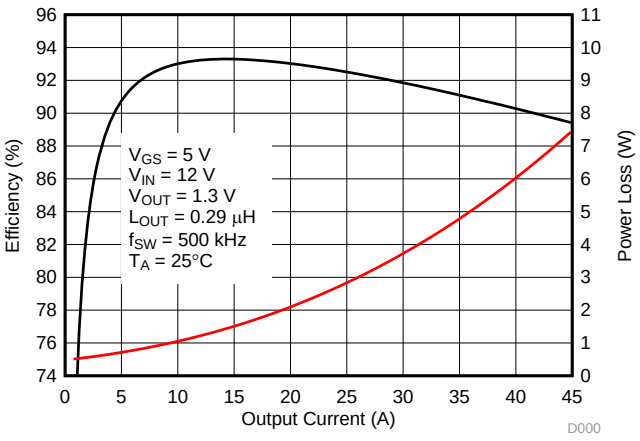
デバイス	メディア	数量	パッケージ	配送
CSD87355Q5D	13インチ・リール	2500	SON 5mm×6mm プラスチック・パッケージ	テープ・アンド・リール
CSD87355Q5DT	7インチ・リール	250		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

回路例



標準的な電力ブロックの効率と電力損失との関係



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

2016年3月発行のものから更新 **Page**

- Added footnote for $Z_{DS(ON)}$ in the *Electrical Characteristics* table. ... 4
- 削除「*Q5Dのテープ・アンド・リール情報*」セクション ... 19

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5 Specifications

5.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}	–0.8	30	V
	T_G to T_{GR}	–8	10	V
	B_G to P_{GND}	–8	10	V
Pulsed current rating, I_{DM}(2)			120	A
Power dissipation, P_D			12	W
Avalanche energy E_{AS}	Sync FET, I_D = 89 A, L = 0.1 mH		396	mJ
	Control FET, I_D = 50 A, L = 0.1 mH		125	mJ
Operating junction temperature, T_J		–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Pulse duration ≤ 50 µS. Duty cycle ≤ 0.01.

5.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–55	150	°C

5.3 Recommended Operating Conditions

T_A = 25° (unless otherwise noted)

		MIN	MAX	UNIT
V_{GS}	Gate drive voltage	4.5	10	V
V_{IN}	Input supply voltage		27	V
f_{SW}	Switching frequency C_{BST} = 0.1 µF (min)	200	1500	kHz
	Operating current		45	A
T_J	Operating temperature		125	°C

5.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu)(1)(2)			102	°C/W
	Junction-to-ambient thermal resistance (max Cu)(1)(2)			50	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package)(2)			20	°C/W
	Junction-to-case thermal resistance (P_{GND} pin)(2)			2	°C/W

(1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.
(2) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.5 Power Block Performance

T_A = 25° (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power loss, P_{LOSS}(1)	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH, T_J = 25ºC		2.8		W
V_{IN} quiescent current, I_{QVIN}	T_G to T_{GR} = 0 V ,B_G to P_{GND} = 0 V		10		µA

(1) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

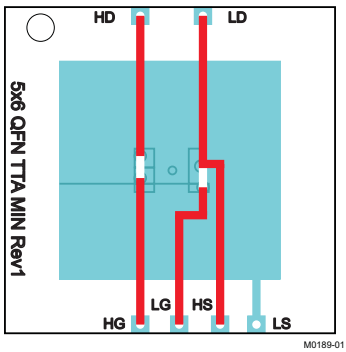
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5.6 Electrical Characteristics

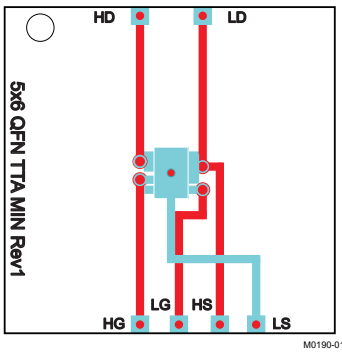
T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = 250 µA	30			30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	1.00		1.90	0.75		1.20	V
$Z_{DS(ON)}$ (1)	Drain-to-source ON impedance	V_{IN} = 12 V, V_{GS} = 5 V, V_{OUT} = 1.3 V, I_{OUT} = 25 A, f_{SW} = 500 kHz, L_{OUT} = 0.29 µH		3.9			0.9		mΩ
g_{fs}	Transconductance	V_{DS} = 3 V, I_{DS} = 20 A		90			151		S
DYNAMIC CHARACTERISTICS									
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1430	1860		3570	4640	pF
C_{OSS}	Output capacitance			716	930		1730	2240	pF
C_{RSS}	Reverse transfer capacitance			25	32		52	67	pF
R_G	Series gate resistance			0.6	1.2		0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_{DS} = 20 A		10.5	13.7		24.3	31.5	nC
Q_{gd}	Gate charge – gate-to-drain			2.3			4.1		nC
Q_{gs}	Gate charge – gate-to-source			3.2			5.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.7			2.8		nC
Q_{OSS}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		18			40		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 20 A, R_G = 2 Ω		8			10		ns
t_r	Rise time			18			14		ns
$t_{d(off)}$	Turn off delay time			13			27		ns
t_f	Fall time			3			6		ns
DIODE CHARACTERISTICS									
V_{SD}	Diode forward voltage	I_{DS} = 20 A, V_{GS} = 0 V		0.8	1.0		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{dd} = 17 V, I_F = 20 A, di/dt = 300 A/µs		43			82		nC
t_{rr}	Reverse recovery time			23.8			32.3		ns

(1) Equivalent based on application testing. See *Application and Implementation* section for details.



Max $R_{\theta JA}$ = 50°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071-mm thick) Cu.

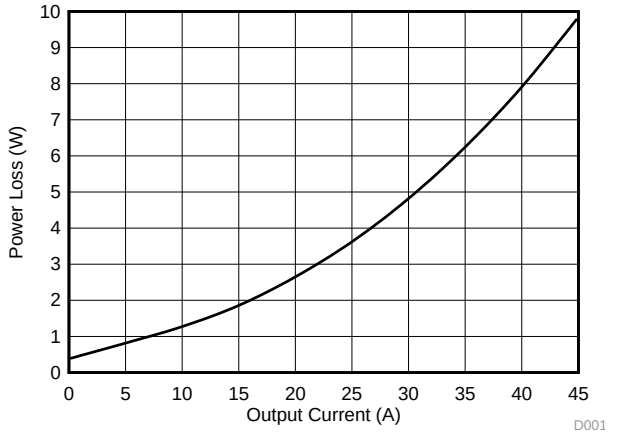


Max $R_{\theta JA}$ = 102°C/W when mounted on minimum pad area of 2 oz. (0.071-mm thick) Cu.

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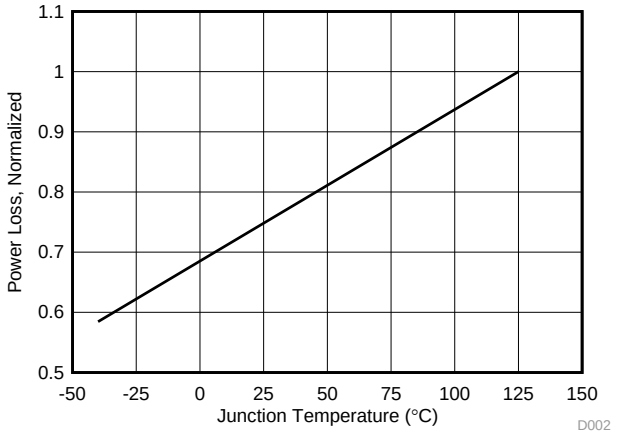
5.7 Typical Power Block Device Characteristics

T_J = 125°C, unless stated otherwise. The Typical Power Block System Characteristic curves 図 3, , and 図 4 are based on measurements made on a PCB design with dimensions of 4” (W) × 3.5” (L) × 0.062” (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation.



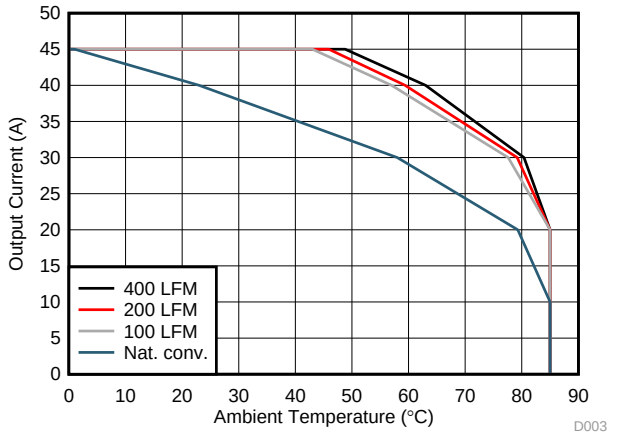
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

図 1. Power Loss vs Output Current



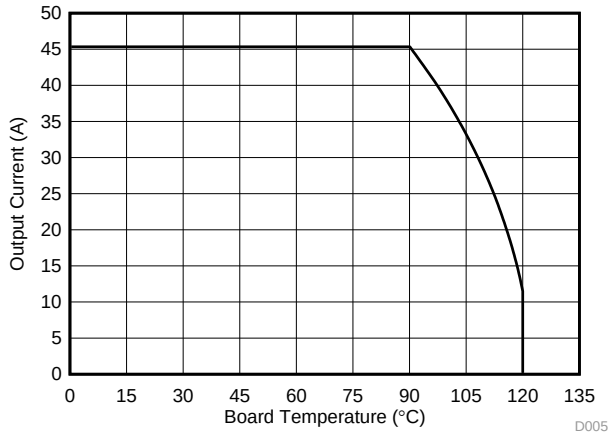
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

図 2. Normalized Power Loss vs Temperature



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

図 3. Safe Operating Area (SOA) – Thermal Airflow Measurement PCB Vertical Mount



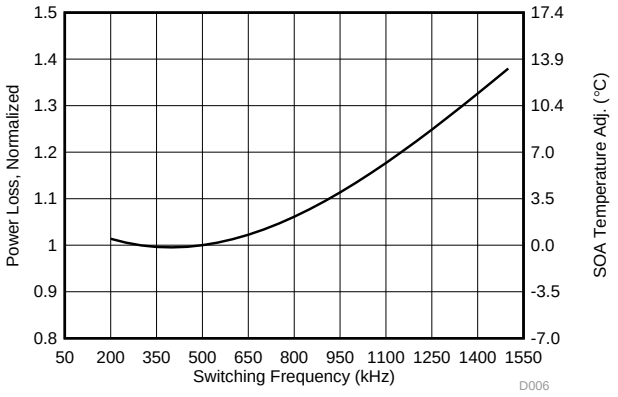
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz L_{OUT} = 0.29 µH

図 4. Typical Safe Operating Area (SOA)

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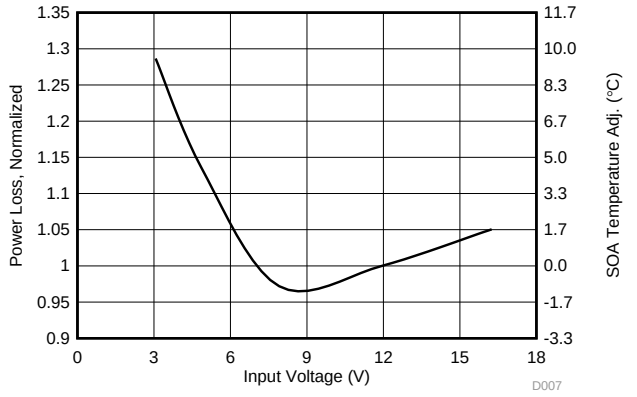
Typical Power Block Device Characteristics (continued)

T_J = 125°C, unless stated otherwise. The Typical Power Block System Characteristic curves 図 3, , and 図 4 are based on measurements made on a PCB design with dimensions of 4” (W) × 3.5” (L) × 0.062” (H) and 6 copper layers of 1-oz. copper thickness. See *Application and Implementation* for detailed explanation.



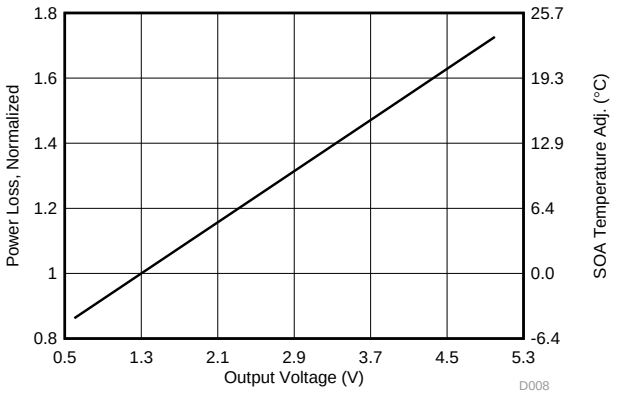
V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
L_{OUT} = 0.29 µH I_{OUT} = 45 A

図 5. Normalized Power Loss vs Switching Frequency



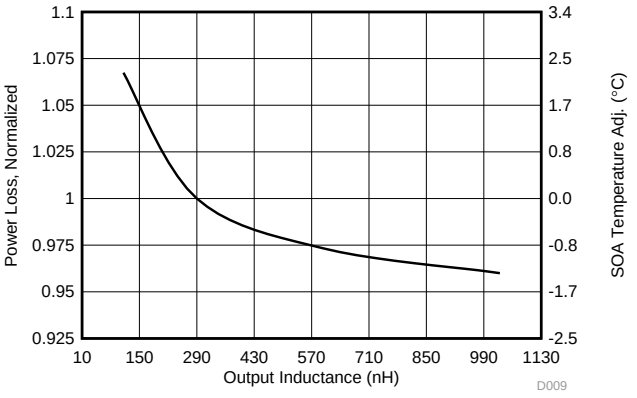
V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.29 µH
f_{SW} = 500 kHz I_{OUT} = 45 A

図 6. Normalized Power Loss vs Input Voltage



V_{IN} = 12 V V_{GS} = 5 V f_{SW} = 500 kHz
L_{OUT} = 0.29 µH I_{OUT} = 45 A

図 7. Normalized Power Loss vs. Output Voltage



V_{IN} = 12 V V_{GS} = 5 V V_{OUT} = 1.3 V
f_{SW} = 500 kHz I_{OUT} = 45 A

図 8. Normalized Power Loss vs Output Inductance

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5.8 Typical Power Block MOSFET Characteristics

T_A = 25°C, unless stated otherwise.

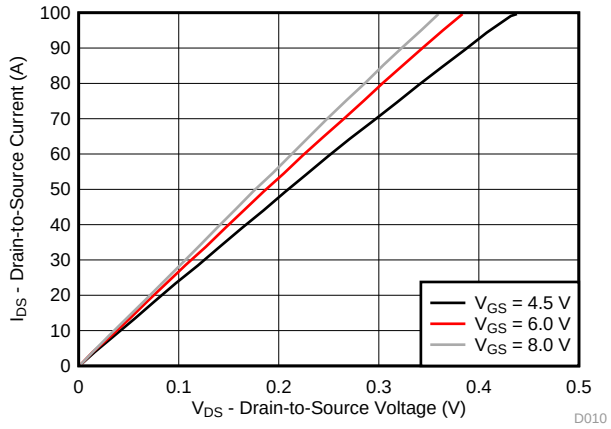


図 9. Control MOSFET Saturation

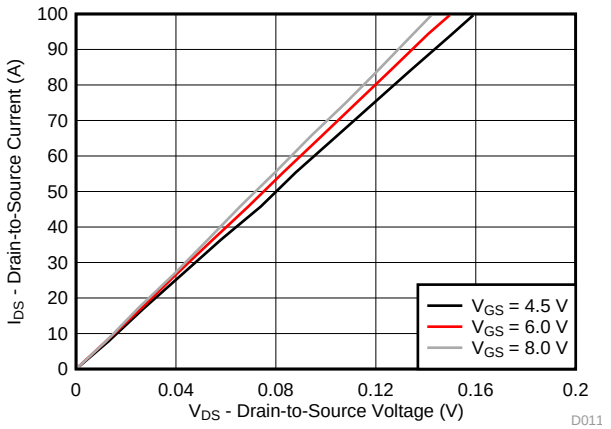


図 10. Sync MOSFET Saturation

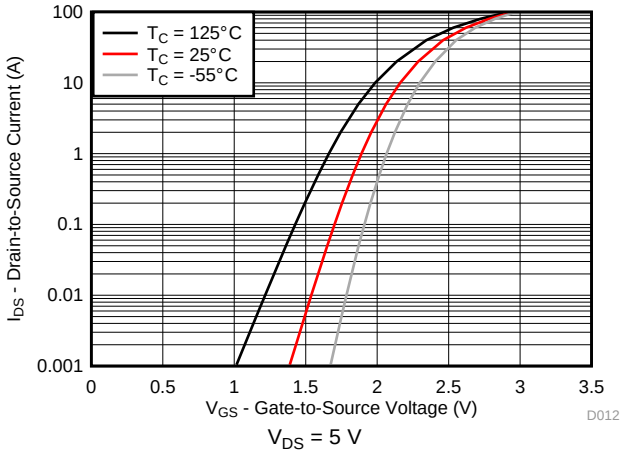


図 11. Control MOSFET Transfer

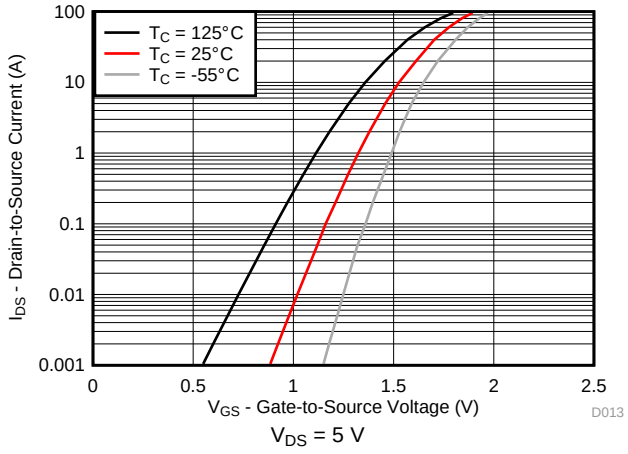


図 12. Sync MOSFET Transfer

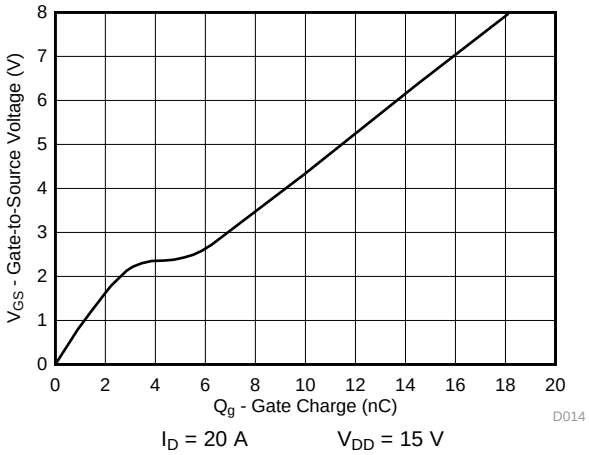


図 13. Control MOSFET Gate Charge

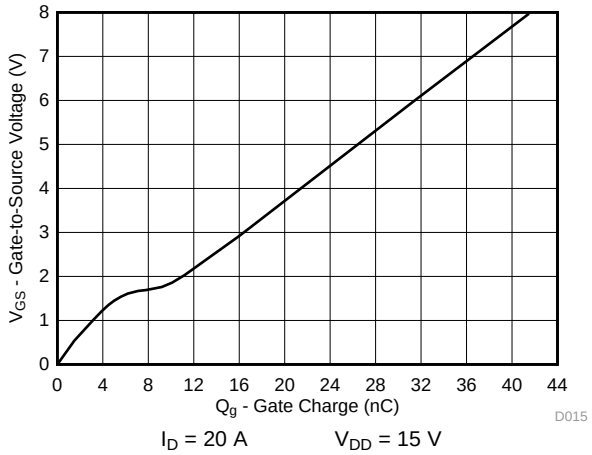


図 14. Sync MOSFET Gate Charge

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Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

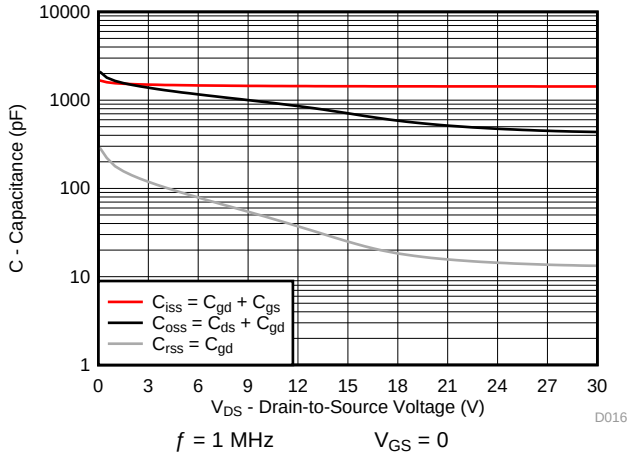


図 15. Control MOSFET Capacitance

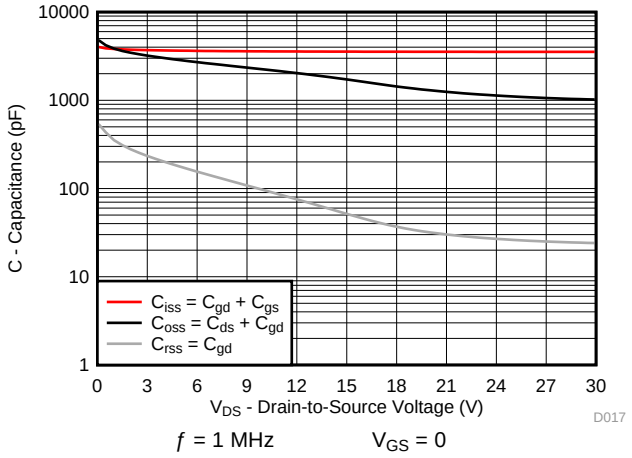


図 16. Sync MOSFET Capacitance

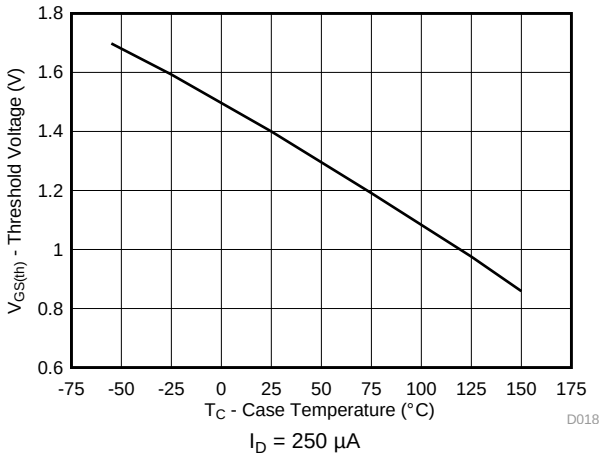


図 17. Control MOSFET $V_{GS(th)}$

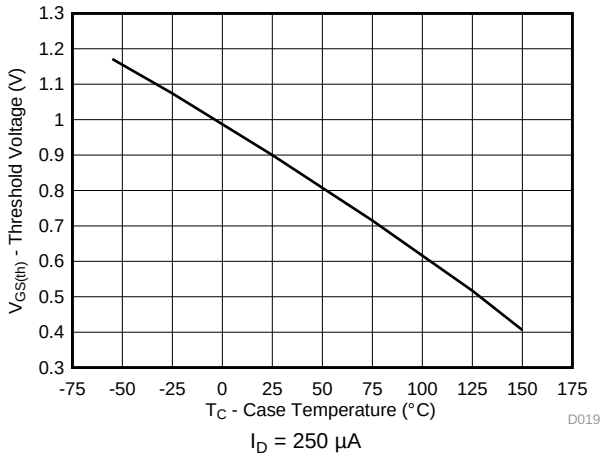


図 18. Sync MOSFET $V_{GS(th)}$

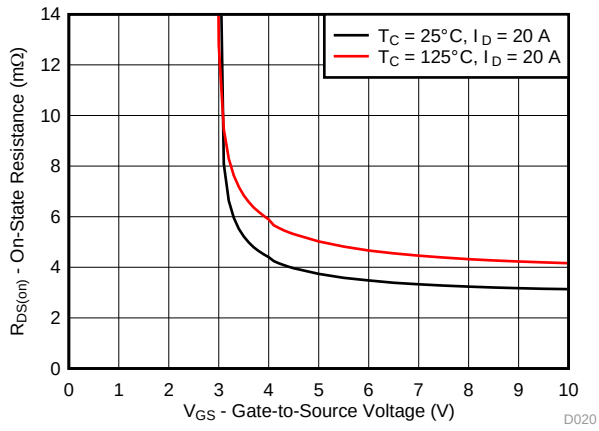


図 19. Control MOSFET $R_{DS(ON)}$ vs V_{GS}

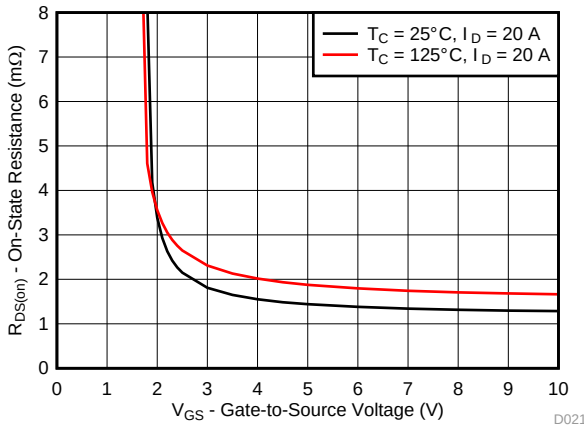


図 20. Sync MOSFET $R_{DS(ON)}$ vs V_{GS}

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Typical Power Block MOSFET Characteristics (continued)

T_A = 25°C, unless stated otherwise.

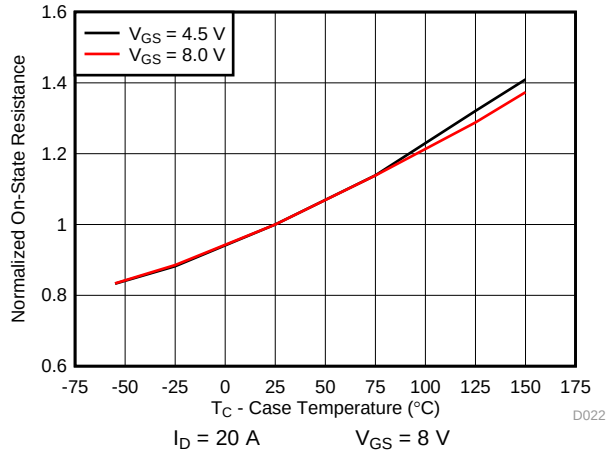


図 21. Control MOSFET Normalized $R_{DS(ON)}$

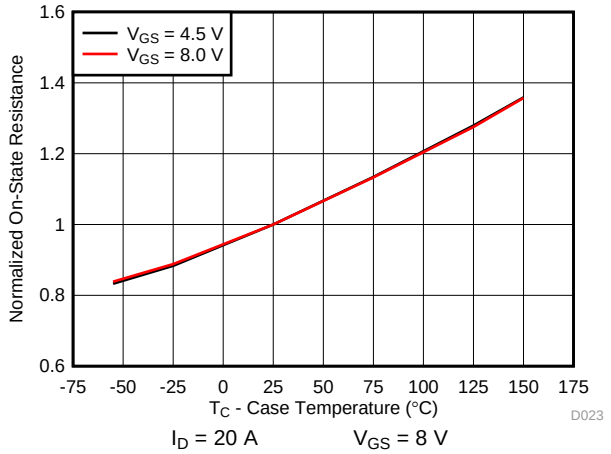


図 22. Sync MOSFET Normalized $R_{DS(ON)}$

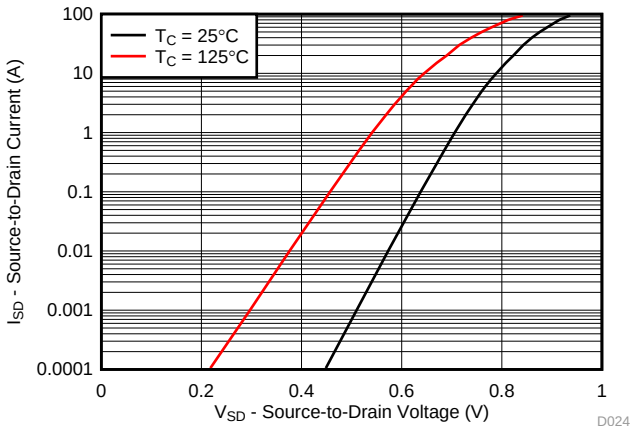


図 23. Control MOSFET Body Diode

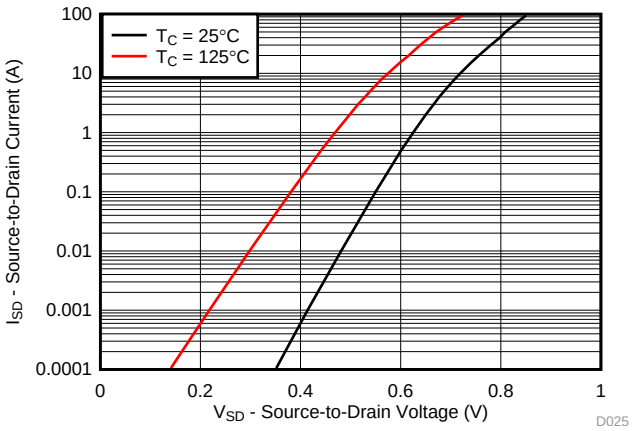


図 24. Sync MOSFET Body Diode

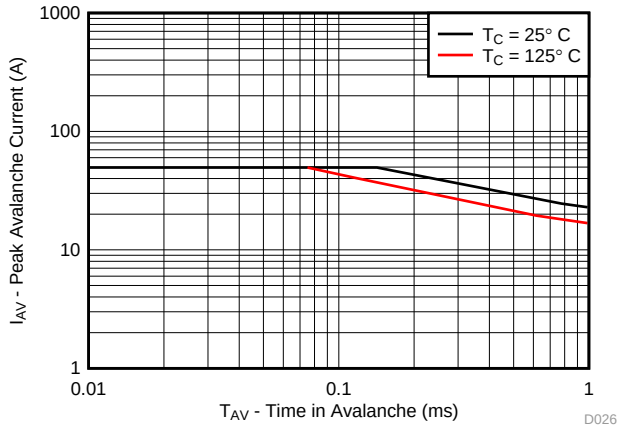


図 25. Control MOSFET Unclamped Inductive Switching

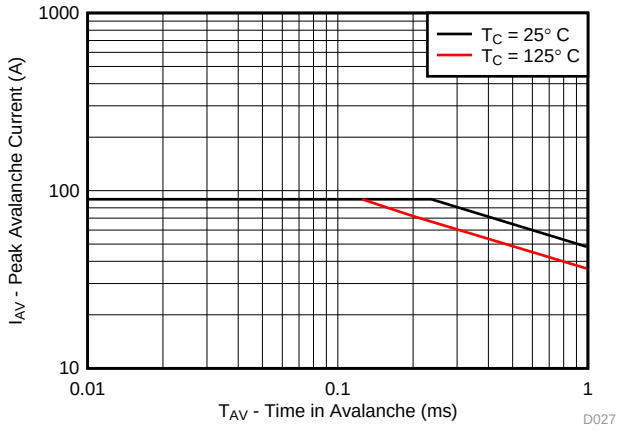


図 26. Sync MOSFET Unclamped Inductive Switching

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6 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87355Q5D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Equivalent System Performance

Many of today's high performance computing systems require low power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's Synchronous Buck Topology. In particular, there has been an emphasis in improving the performance of the critical Power Semiconductor in the Power Stage of this application (see 図 27). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

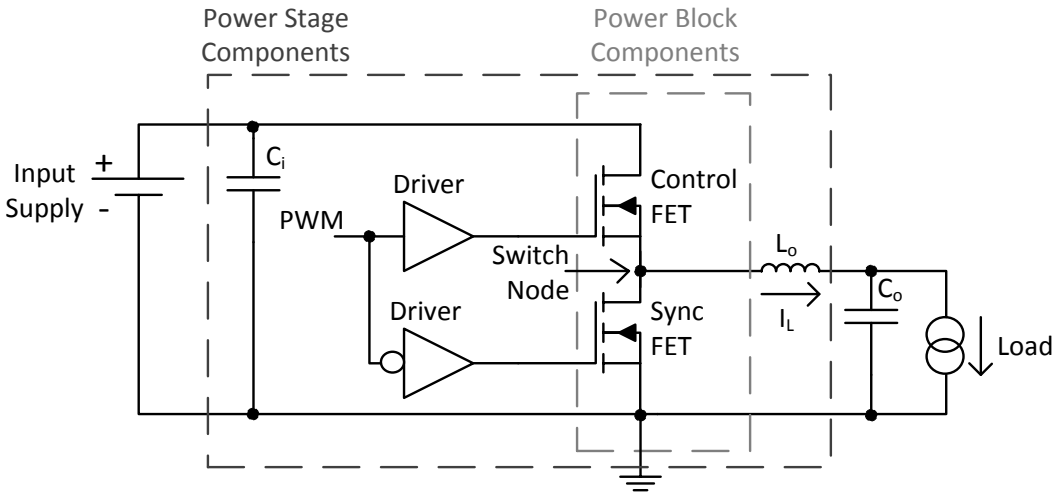


図 27.

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Application Information (continued)

The CSD87355Q5D is part of TI's Power Block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD}, Q_{GS}, and Q_{RR}. Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the Control FET and Sync FET connections (see 図 28). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in TI's Application Note SLPA009.

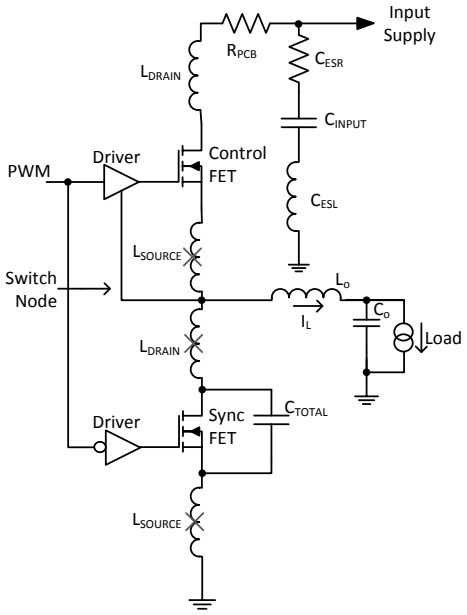
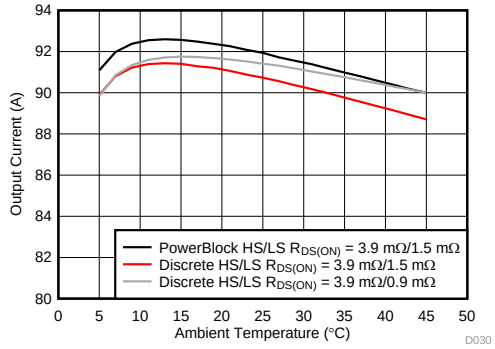


図 28.

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. 図 29 and 図 30 compare the efficiency and power loss performance of the CSD87355Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87355Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's Power Block technology.

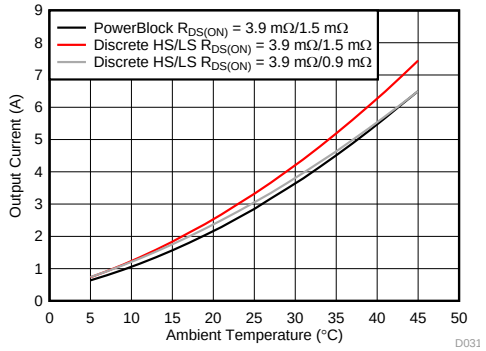
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Application Information (continued)



V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.3 µH
f_{SW} = 500 kHz V_{DD}= 5 V T_A = 25°C

図 29. Efficiency



V_{IN} = 12 V V_{OUT} = 1.3 V L_{OUT} = 0.3 µH
f_{SW} = 500 kHz V_{DD} = 5 V T_A = 25°C

図 30. Power Loss

表 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87355Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's Power Block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87355Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

表 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS		UNIT
	TYP	MAX	TYP	MAX	
Effective AC On-Impedance $Z_{DS(ON)}$ (V_{GS} = 5 V)	3.9	-	0.9	-	mΩ
DC Measured $R_{DS(ON)}$ (V_{GS} = 4.5 V)	3.9	4.7	1.5	1.8	mΩ

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. 図 1 plots the power loss of the CSD87355Q5D as a function of load current. This curve is measured by configuring and running the CSD87355Q5D as it would be in the final application (see 図 31).The measured power loss is the CSD87355Q5D loss and consists of both input conversion loss and gate drive loss. 式 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in 図 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87355Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. 図 3 to 図 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4" (W) × 3.5" (L) × 0.062" (T) and 6 copper layers of 1-oz. copper thickness.

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6.1.4 Normalized Curves

The normalized curves in the CSD87355Q5D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

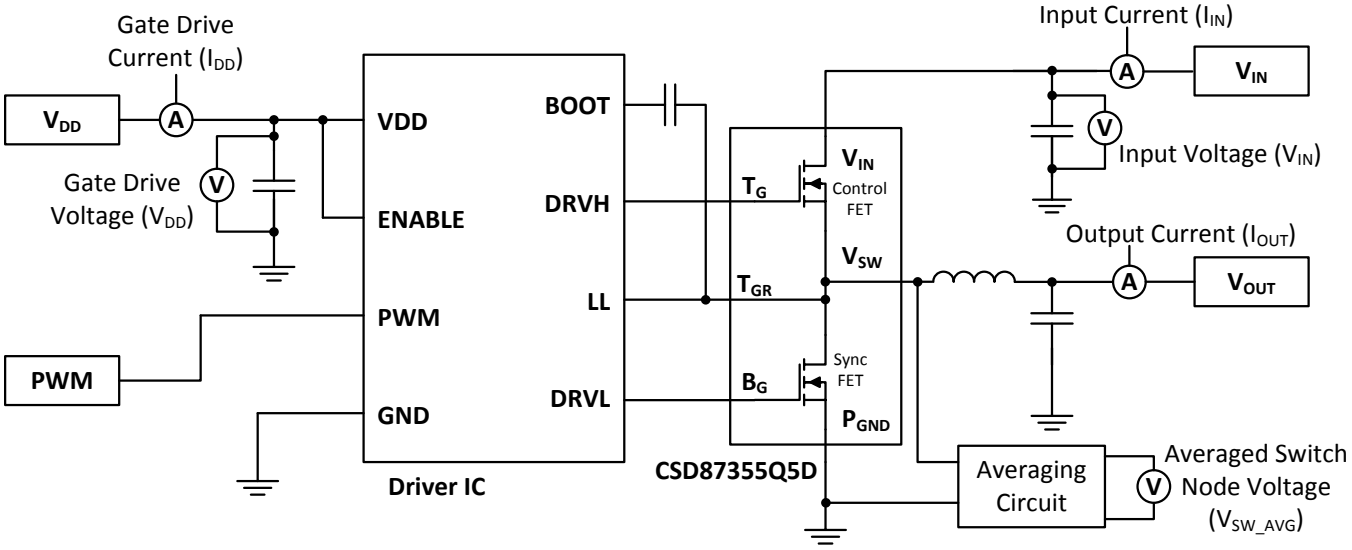


図 31.

Typical Application (continued)

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see *Operating Conditions*). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.2 Operating Conditions

- Output Current = 25 A
- Input Voltage = 7 V
- Output Voltage = 1.4 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 µH

6.2.2.1 Calculating Power Loss

- Power Loss at 25 A = 3.62 W (図 1)
- Normalized Power Loss for input voltage ≈ 0.99 (図 6)
- Normalized Power Loss for output voltage ≈ 1.02 (図 7)
- Normalized Power Loss for switching frequency ≈ 1.06 (図 5)
- Normalized Power Loss for output inductor ≈ 1.03 (図 8)
- **Final calculated Power Loss = 3.62 W × 0.99 × 1.02 × 1.06 × 1.03 ≈ 3.99 W**

6.2.2.2 Calculating SOA Adjustments

- SOA adjustment for input voltage ≈ –0.24ºC (図 6)
- SOA adjustment for output voltage ≈ 0.63ºC (図 7)
- SOA adjustment for switching frequency ≈ 2.12ºC (図 5)
- SOA adjustment for output inductor ≈ 0.91ºC (図 8)
- **Final calculated SOA adjustment = –0.24 + 0.63 + 2.12 + 0.91 ≈ 3.42C**

In the previous design example, the estimated power loss of the CSD87355Q5D would increase to 4 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.4ºC. 図 32 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.4ºC. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

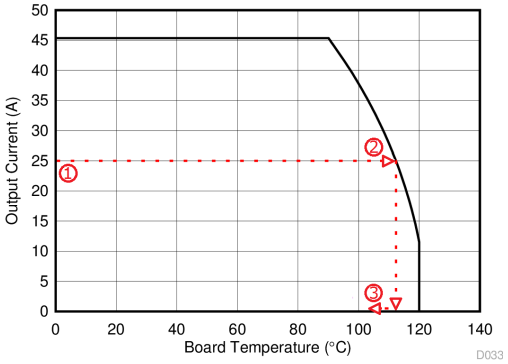


図 32. Power Block SOA

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7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10 kV/µs. Take special care with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see 図 33). The example in 図 33 uses 6 × 10-µF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a Boost Resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended Boost Resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of Driver IC used in conjunction with the Power Block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to TI App Note SLUP100 for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see 図 33. (1)

7.1.2 Thermal Considerations

The Power Block has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in 図 33 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

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7.2 Layout Example

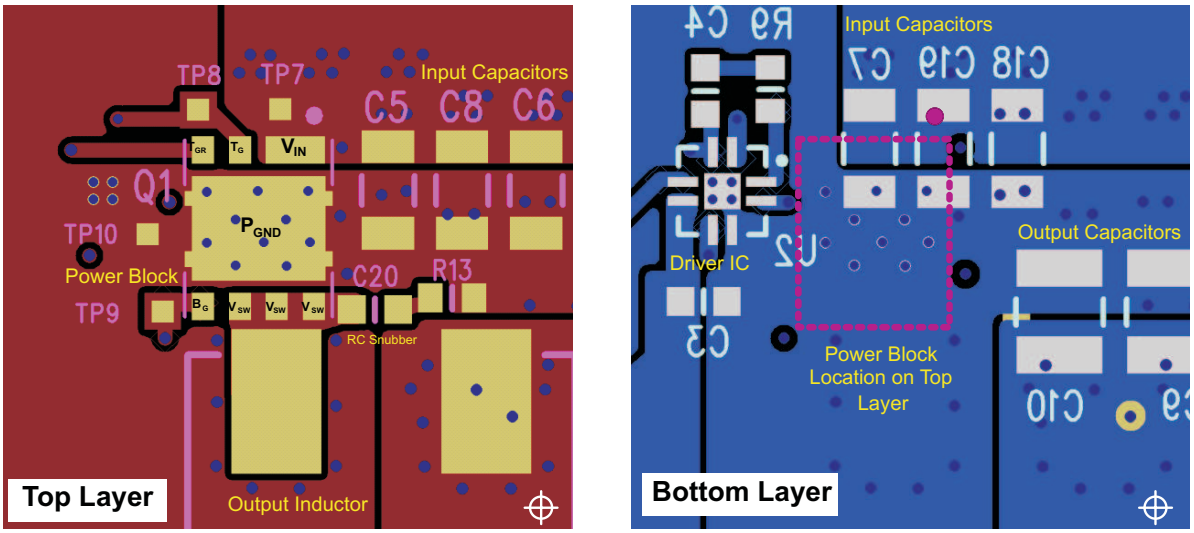


図 33. Recommended PCB Layout (Top View)

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8 デバイスおよびドキュメントのサポート

8.1 コミュニティ・リソース

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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8.4 Glossary

SLYZ022 — *TI Glossary*.

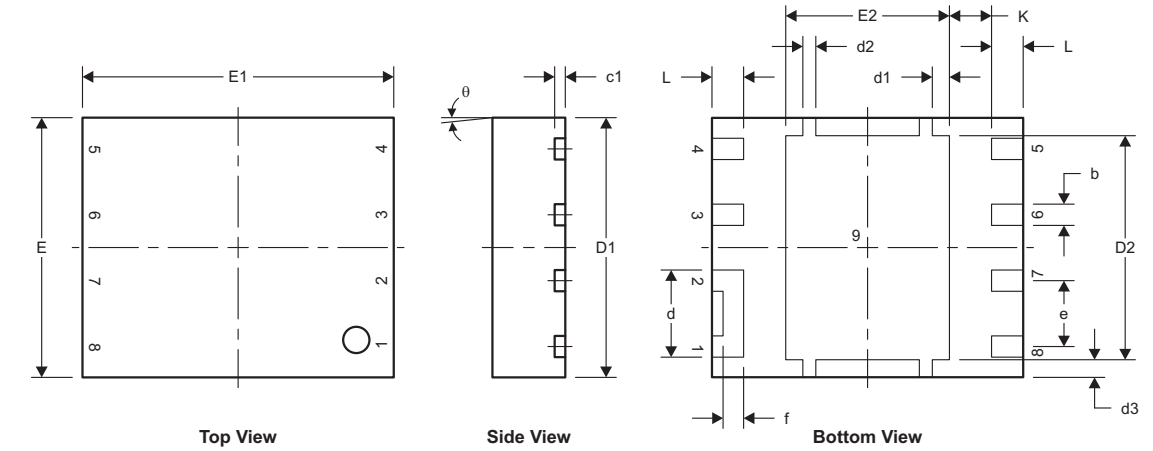
This glossary lists and explains terms, acronyms, and definitions.

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9 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

9.1 Q5Dパッケージの寸法



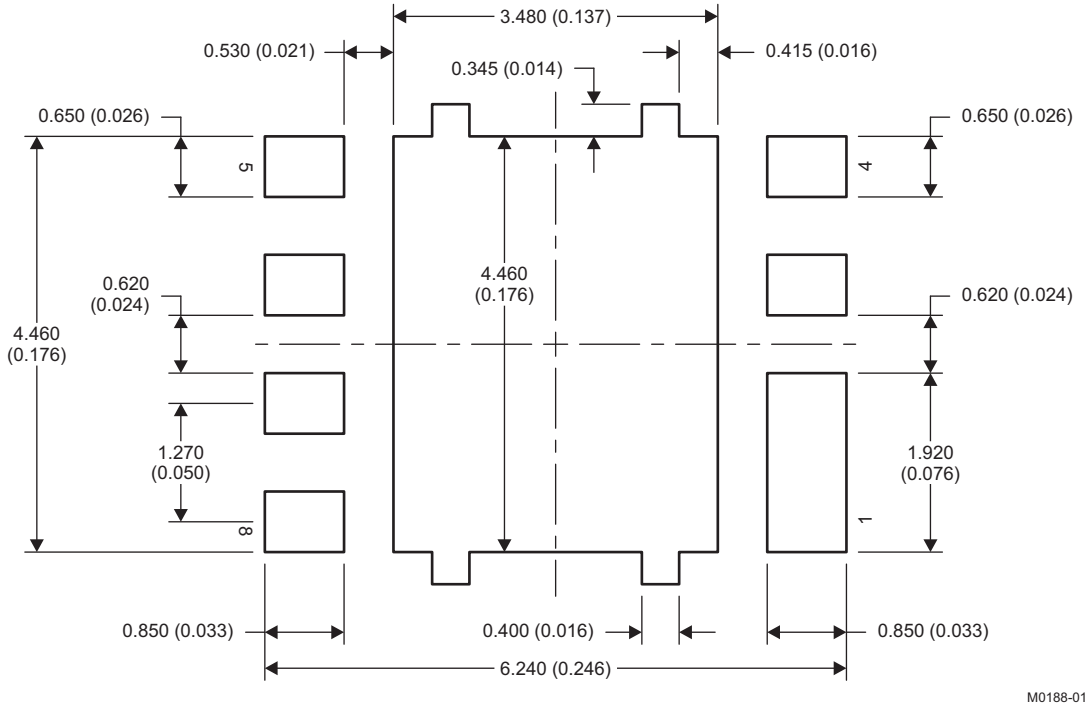
Pinout	
Position	Designation
Pin 1	V_{IN}
Pin 2	V_{IN}
Pin 3	T_G
Pin 4	T_{GR}
Pin 5	B_G
Pin 6	V_{SW}
Pin 7	V_{SW}
Pin 8	V_{SW}
Pin 9	P_{GND}

M0187-01

寸法	ミリメートル		インチ	
	最小	最大	最小	最大
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 (標準値)		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

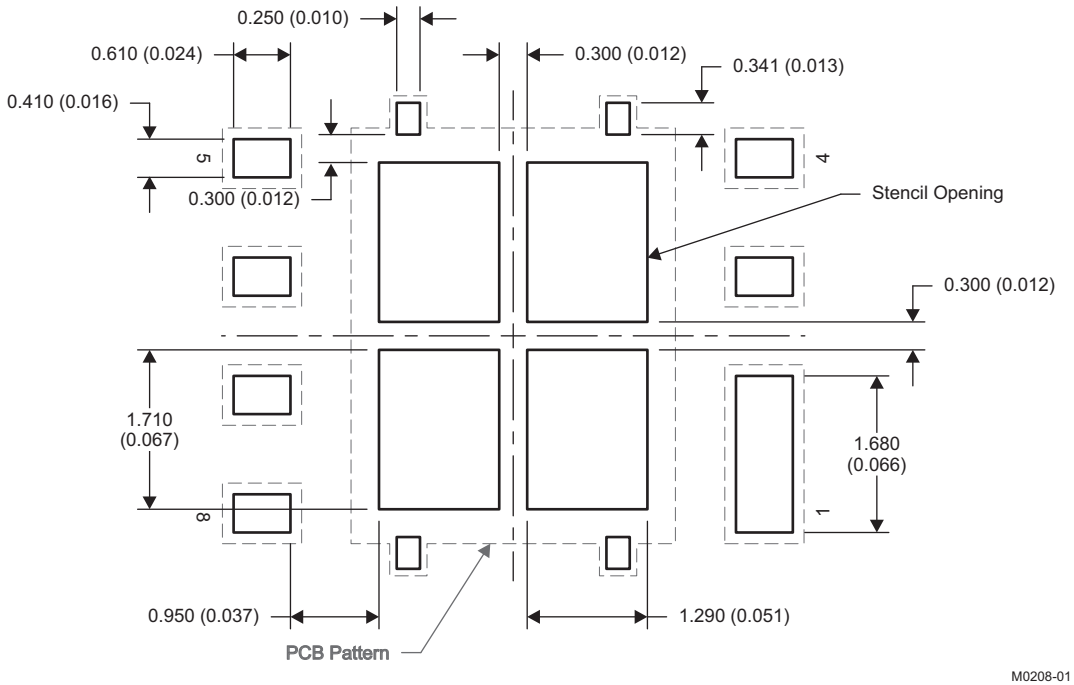
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9.2 推奨ランド・パターン



NOTE: 寸法はmm (インチ)単位です。

9.3 推奨ステンシル



NOTE: 寸法はmm (インチ)単位です。

PCBデザインの推奨回路レイアウトについては、アプリケーション・ノートSLPA005『*PCBレイアウト技法によるリンギングの低減*』を参照してください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD87355Q5D	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D
CSD87355Q5D.B	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D
CSD87355Q5DG4	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D
CSD87355Q5DG4.B	Active	Production	LSON-CLIP (DQY) | 8	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D
CSD87355Q5DT	Active	Production	LSON-CLIP (DQY) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D
CSD87355Q5DT.B	Active	Production	LSON-CLIP (DQY) | 8	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

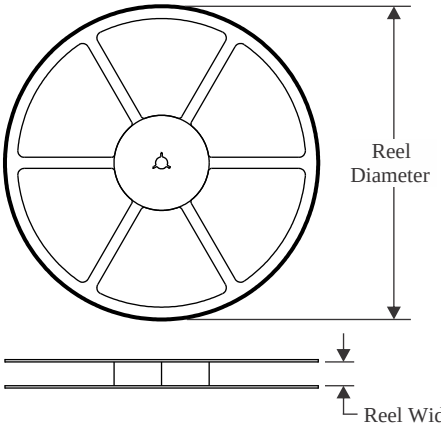
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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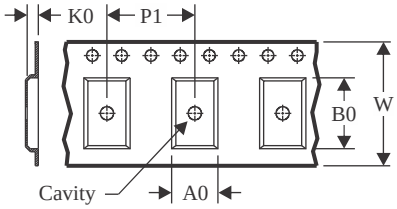
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

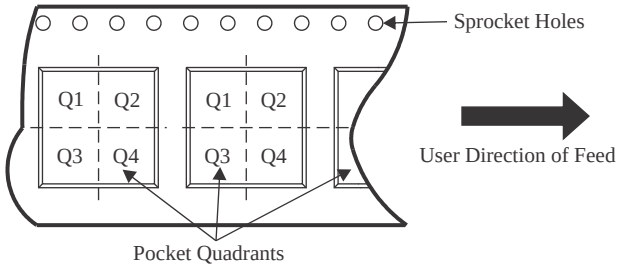


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

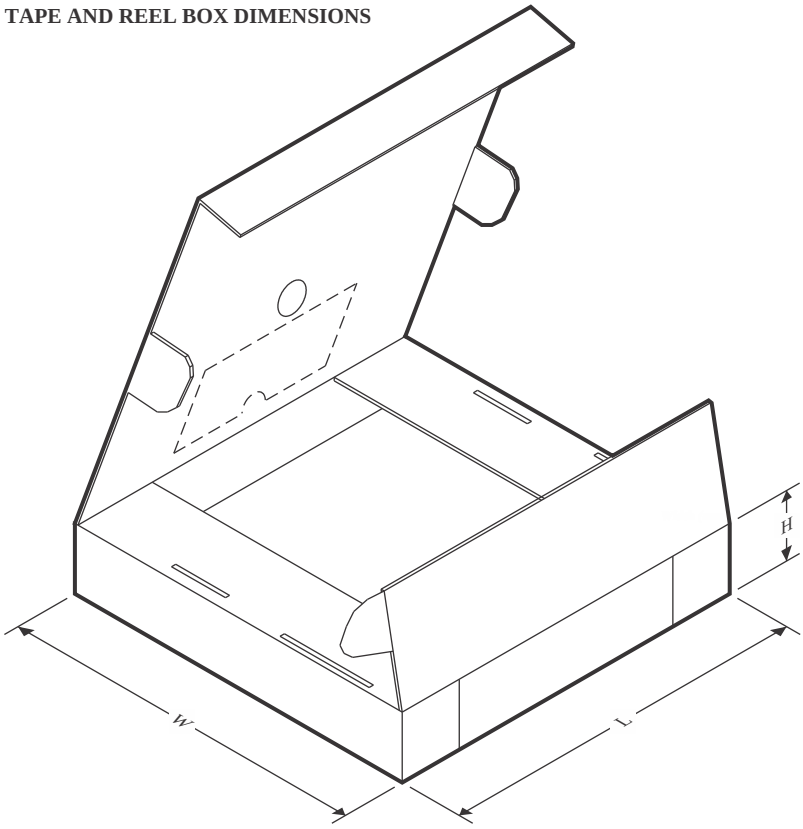
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87355Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD87355Q5DG4	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD87355Q5DT	LSON-CLIP	DQY	8	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87355Q5D	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0
CSD87355Q5DG4	LSON-CLIP	DQY	8	2500	346.0	346.0	33.0
CSD87355Q5DT	LSON-CLIP	DQY	8	250	182.0	182.0	20.0

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