TEXAS INSTRUMENTS
DAC81408, DAC71408, DAC61408
JAJSFQ0A – JULY 2018 – REVISED NOVEMBER 2018

# DACx1408 8チャネル、16/14/12ビット、内部基準電圧付き、高電圧出力DAC

## 1 特長

- **性能**
  - 16ビット分解能で単調性を規定
  - INL：16ビット分解能で最大値±1LSB
  - TUE：FSR最大値の±0.1%
- **2.5Vの高精度内部基準電圧を搭載**
  - 初期精度: ±2.5mV (最大値)
  - 低ドリフト: 5ppm/℃ (標準値)
- **柔軟な出力構成**
  - 出力範囲: ±2.5V、±5V、±10V、±20V
    0～5V、0～10V、0～20V、0～40V
  - 差動出力モード
- **高い駆動能力：電源レールから1.5Vで±25mA**
- **3つの専用A-Bトグル・ピンによるディザリング信号生成**
- **アナログ温度出力**
  - センサ・ゲイン: -4mV/°C
- **50MHz SPI互換のシリアル・インターフェイス**
  - 4線式モード、1.7V～5.5Vでの動作
  - デイジー・チェーン動作
  - CRCエラー・チェック
- **温度範囲**: -40℃～+125℃
- **小型パッケージ**
  - 6mm×6mm、40ピンのVQFN

## 2 アプリケーション

- **光ネットワーク**: マッハツェンダー変調器のバイアス制御
- **産業用オートメーション**
- **試験/測定機器**

## 3 概要

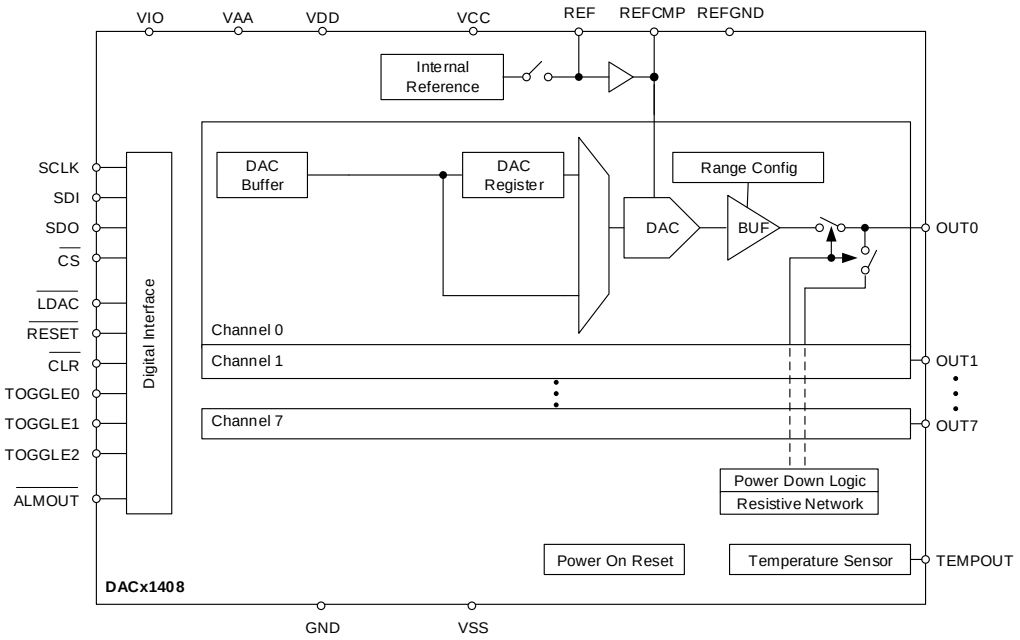
DAC81408、DAC71408、DAC61408 (DACx1408)は、16、14、12ビット分解能の8チャネル、バッファ付き、高電圧出力のデジタル/アナログ・コンバータ(DAC)のピン互換ファミリです。DACx1408には、低ドリフト、2.5Vの内部基準電圧が搭載されており、ほとんどのアプリケーションでは外付けの高精度基準電圧が不要になります。これらのデバイスは単調性が規定されており、±1LSB INLの高い線形性を達成しています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ(公称) |
|---|---|---|
| DAC81408<br>DAC71408<br>DAC61408 | VQFN(40) | 6.00mm×6.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

**機能ブロック図**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。
English Data Sheet: SLASER3

# 目次

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 改訂履歴 ... 2
5 概要（続き） ... 3
6 **Device Comparison Table** ... 4
7 **Pin Configuration and Functions** ... 4
8 **Specifications** ... 6
8.1 Absolute Maximum Ratings ... 6
8.2 ESD Ratings ... 6
8.3 Recommended Operating Conditions ... 6
8.4 Thermal Information ... 7
8.5 Electrical Characteristics ... 8
8.6 Timing Requirements ... 12
8.7 Typical Characteristics ... 14
9 **Parameter Measurement Information** ... 22
10 **Detailed Description** ... 23
10.1 Overview ... 23
10.2 Functional Block Diagram ... 23
10.3 Feature Description ... 24
10.4 Device Functional Modes ... 27
10.5 Programming ... 29
10.6 Register Maps ... 32
11 **Application and Implementation** ... 47
11.1 Application Information ... 47
11.2 Typical Application ... 47
12 **Power Supply Recommendations** ... 50
13 **Layout** ... 51
13.1 Layout Guidelines ... 51
13.2 Layout Example ... 51
14 デバイスおよびドキュメントのサポート ... 52
14.1 ドキュメントのサポート ... 52
14.2 関連リンク ... 52
14.3 ドキュメントの更新通知を受け取る方法 ... 52
14.4 コミュニティ・リソース ... 52
14.5 商標 ... 52
14.6 静電気放電に関する注意事項 ... 52
14.7 Glossary ... 52
15 メカニカル、パッケージ、および注文情報 ... 52

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**2018年7月発行のものから更新** **Page**

- DAC81408を「事前情報」から「量産データ」に 変更 ... 1
- DAC71408およびDAC61408を「製品プレビュー」から「量産データ」に 変更 ... 1


Copyright © 2018, Texas Instruments Incorporated

## 5 概要（続き）

出力構成をユーザーが選択可能で、フルスケールの双極性出力電圧の±20V、±10V、±5V、±2.5V、およびフルスケール単極性出力電圧の40V、20V、10V、5Vを使用できます。各DACチャネルのフルスケール出力範囲は別々にプログラム可能です。統合されたDAC出力バッファは最大25mAをシンクまたはソースできるため、追加のオペアンプの必要性が低下します。チャネルの各ペアは、オフセット較正付きの差動出力を提供するよう構成可能です。3つの専用A-Bトグル・ピンにより、最大3つの周波数についてディザリング信号を生成できます。

DACx1408にはパワー・オン・リセット回路が組み込まれており、電源オン時にDAC出力をグランドに接続します。デバイスのレジスタが動作用に正しく構成されるまで、出力がこの状態に維持されます。

DACx1408との通信は、1.7V～5.5Vでの動作をサポートする4線式のシリアル・インターフェイスにより行われます。

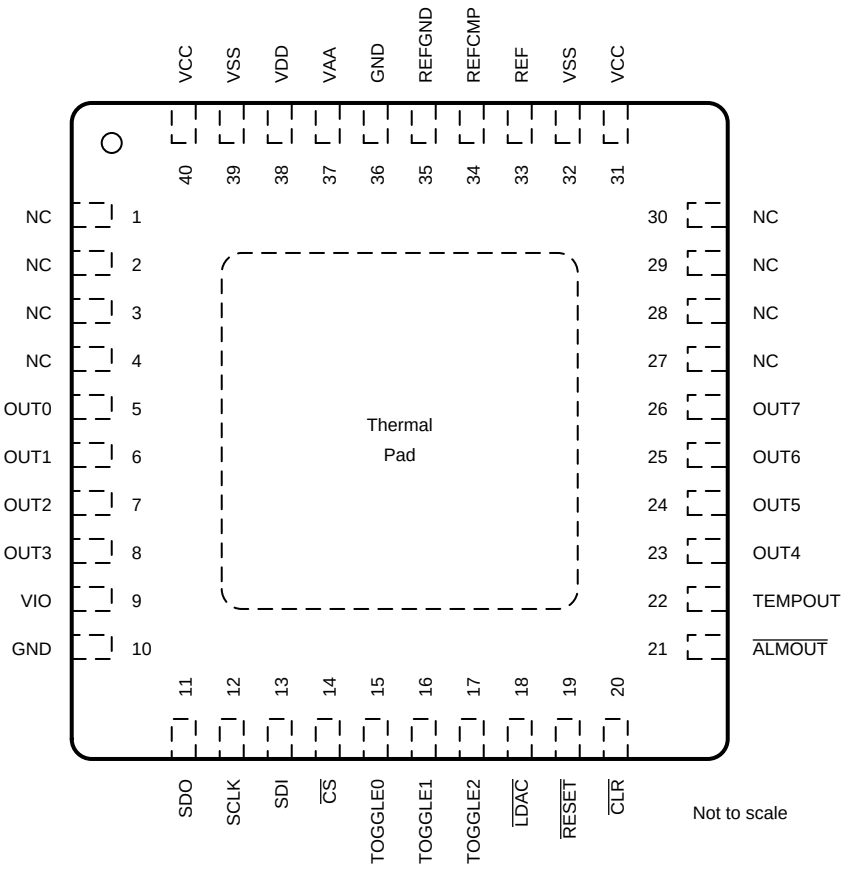
Copyright © 2018, Texas Instruments Incorporated

# 6 Device Comparison Table

| DEVICE | RESOLUTION |
|---|---|
| DAC81408 | 16-Bit |
| DAC71408 | 14-Bit |
| DAC61408 | 12-Bit |

# 7 Pin Configuration and Functions

**RHA Package**
**40-Pin VQFN**
**Top View**





Copyright © 2018, Texas Instruments Incorporated

## Pin Functions

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| OUT[0:7] | 5 - 8, 23 - 26 | O | Analog DAC output voltages. |
| NC | 1, 2, 3, 4, 27, 28, 29, 30 | O | No connection. |
| VIO | 9 | PWR | IO supply voltage. (1.7 V to 5.5 V). This pin sets the I/O operating voltage for the device. |
| GND | 10, 36 | GND | Ground reference point for all circuitry on the device. |
| SDO | 11 | O | Serial interface data output. The SDO pin must be enabled before operation by setting the SDO-EN bit. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit (rising edge by default). |
| SCLK | 12 | I | Serial interface clock. |
| SDI | 13 | I | Serial interface data input. Data are clocked into the input shift register on each falling edge of the SCLK pin. |
| $\overline{CS}$ | 14 | I | Active low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, it enables the serial interface input shift register. |
| TOGGLE0 | 15 | I | Toggle pins. Control signals for those DAC outputs configured for toggle operation to switch between the two DAC data registers associated with each DAC. A logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. Connect the TOGGLE pins to ground if not using the toggle operation. |
| TOGGLE1 | 16 | I | |
| TOGGLE2 | 17 | I | |
| $\overline{LDAC}$ | 18 | I | Active low synchronization signal. When the $\overline{LDAC}$ pin is low, the DAC outputs of those channels configured in synchronous mode are updated simultaneously. Connect to VIO if unused. |
| $\overline{RESET}$ | 19 | I | Active low reset input. Logic low on this pin causes the device to issue a power-on-reset event. |
| $\overline{CLR}$ | 20 | I | Active low clear input. Logic low on this pin clears all DAC outputs to their clear code. Connect to VIO if unused. |
| $\overline{ALMOUT}$ | 21 | O | $\overline{ALMOUT}$ is an open drain alarm output. An external 10-kΩ pull-up resistor to a voltage no higher than $V_{IO}$ is required. |
| TEMPOUT | 22 | O | Analog temperature monitor output. |
| VCC | 31, 40 | PWR | Output positive analog power supply (9 V to 41.5 V). |
| VSS | 32, 39 | PWR | Output negative analog power supply (-21.5 V to 0 V). |
| REF | 33 | I/O | Reference input to the device when operating with external reference. When using internal reference, this is the reference output voltage pin. Connect a 150-nF capacitor to ground. |
| REFCMP | 34 | I/O | Reference compensation capacitor connection. Connect a 330-pF capacitor between REFCMP and REFGND. |
| REFGND | 35 | GND | Ground reference point for the internal reference. |
| VAA | 37 | PWR | Analog supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VDD pin. |
| VDD | 38 | PWR | Digital supply voltage (4.5 V to 5.5 V). This pin must be at the same potential as the VAA pin. |
| THERMAL PAD | – | – | The thermal pad is located on the package underside. The thermal pad should be connected to any internal PCB ground plane through multiple vias for good thermal performance. |

Copyright © 2018, Texas Instruments Incorporated

# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ to GND | -0.3 | 6 | V |
| | $V_{IO}$ to GND | -0.3 | 6 | V |
| | $V_{CC}$ to GND | -0.3 | 44 | V |
| | $V_{SS}$ to GND | -22 | 0.3 | V |
| | REFGND to GND | -0.3 | 0.9 | V |
| | $V_{DD}$ to $V_{AA}$ | -0.3 | 0.3 | V |
| | $V_{CC}$ to $V_{SS}$ | -0.3 | 44 | V |
| Pin voltage | DAC outputs to GND | $V_{SS}$ - 0.3 | $V_{CC}$ + 0.3 | V |
| | TEMPOUT to GND | -0.3 | $V_{DD}$ + 0.3 | V |
| | REF and REFCMP to GND | -0.3 | $V_{DD}$ + 0.3 | V |
| | Digital inputs to GND | -0.3 | $V_{IO}$ + 0.3 | V |
| | SDO to GND | -0.3 | $V_{IO}$ + 0.3 | V |
| | $\overline{\text{ALARMOUT}}$ to GND | -0.3 | 6 | V |
| Operating junction temperature, $T_J$ | | -40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | -60 | 150 | °C |

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{AA}$ (1) | | 4.5 | | 5.5 | V |
| $V_{DD}$ (1) | | 4.5 | | 5.5 | V |
| $V_{IO}$ | | 1.7 | | 5.5 | V |
| $V_{CC}$ | | 9 | | 41.5 | V |
| $V_{SS}$ (2) | | -21.5 | | 0 | V |
| $V_{CC} – V_{SS}$ | | 9 | | 43 | V |
| Digital input voltage | | 0 | | $V_{IO}$ | V |
| $V_{REFIN}$ | Reference input voltage to $V_{REFGND}$ | 2.49 | 2.5 | 2.51 | V |
| $V_{REFGND}$ (3) | REFGND pin voltage | 0 | 0 | 0.6 | V |
| $T_A$ | Operating ambient temperature | -40 | | 125 | °C |

(1) $V_{AA}$ and $V_{DD}$ must be at the same potential.
(2) $V_{SS}$ is only connected to GND when all DAC outputs are unipolar.
(3) If $V_{REFGND}$ is not connected to GND, a buffered source must be used to drive it.


Copyright © 2018, Texas Instruments Incorporated

## 8.4 Thermal Information

| THERMAL METRIC(1) | | DACx1408 |
|---|---|---|
| | | RHA (VQFN) |
| | | 40 PINS |
| $R_{\Theta JA}$ | Junction-to-ambient thermal resistance | 26.8 |
| $R_{\Theta JC(top)}$ | Junction-to-case (top) thermal resistance | 14.1 |
| $R_{\Theta JB}$ | Junction-to-board thermal resistance | 3.4 |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.2 |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 3.4 |
| $R_{\Theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.7 |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

Copyright © 2018, Texas Instruments Incorporated

## 8.5 Electrical Characteristics

all minimum/maximum specifications at $T_A$ = -40℃ to +125℃ and all typical specifications at $T_A$ = 25℃, $V_{CC}$ = 9 V to 41.5 V, $V_{SS}$ = -21.5 V to 0 V, $V_{DD}$ = $V_{AA}$ = 4.5 V to 5.5 V, $V_{REFIN}$ = 2.5 V, $V_{IO}$ = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at $V_{IO}$ or GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE (1)** | | | | | | |
| DAC81408 | Resolution | | 16 | | | Bits |
| | Integral nonlinearity (INL) | All ranges, except 0 to 40 V and ±2.5 V | -1 | ±0.5 | 1 | LSB |
| | | 0 to 40 V and ±2.5 V range | -2 | ±1 | 2 | LSB |
| | Differential nonlinearity (DNL) | Specified 16-bit monotonic | -1 | ±0.5 | 1 | LSB |
| DAC71408 | Resolution | | 14 | | | Bits |
| | Integral nonlinearity (INL) | All ranges | -1 | ±0.5 | 1 | LSB |
| | Differential nonlinearity (DNL) | Specified 14-bit monotonic | -1 | ±0.5 | 1 | LSB |
| DAC61408 | Resolution | | 12 | | | Bits |
| | Integral nonlinearity (INL) | All ranges | -1 | ±0.5 | 1 | LSB |
| | Differential nonlinearity (DNL) | Specified 12-bit monotonic | -1 | ±0.5 | 1 | LSB |
| TUE | Total unadjusted error | All ranges, except ±2.5 V | -0.1 | ±0.01 | 0.1 | %FSR |
| | | ±2.5 V range | -0.2 | ±0.02 | 0.2 | |
| | Unipolar offset error | All unipolar ranges | -0.03 | ±0.015 | 0.03 | %FSR |
| | Unipolar zero-code error | All unipolar ranges | 0 | 0.04 | 0.1 | %FSR |
| | Bipolar zero error | All bipolar ranges | -0.2 | ±0.02 | 0.2 | %FSR |
| | Full-scale error | All ranges | -0.2 | ±0.075 | 0.2 | %FSR |
| | Gain error | All ranges, except ±2.5 V | -0.1 | ±0.02 | 0.1 | %FSR |
| | | ±2.5 V range | -0.2 | ±0.02 | 0.2 | |
| | Unipolar offset error drift | All unipolar ranges | | ±2 | | ppm of FSR/°C |
| | Bipolar zero error drift | All bipolar ranges | | ±2 | | ppm of FSR/°C |
| | Gain error drift | All ranges | | ±2 | | ppm of FSR/°C |
| | Output voltage drift over time | $T_A$ = 40°C, Full-scale code, 1900 hours | | 5 | | ppm of FSR |
| **DIFFERENTIAL MODE PERFORMANCE (1)** | | | | | | |
| TUE | Total unadjusted error | All ranges | -0.1 | ±0.01 | 0.1 | %FSR |
| | | ±2.5 V range | -0.2 | ±0.02 | 0.2 | |
| | Common mode error | All bipolar ranges. Midscale code | -0.1 | ±0.01 | 0.1 | %FSR |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| | Output voltage headroom | to $V_{SS}$ and $V_{CC}$ (-10 mA ≤ $I_{OUT}$ ≤ 10 mA) | 1 | | | V |
| | | to $V_{SS}$ and $V_{CC}$ (-15 mA ≤ $I_{OUT}$ ≤ 15 mA) | 1.5 | | | |
| | Short circuit current (2) | Full-scale output shorted to $V_{SS}$ | | 40 | | mA |
| | | Zero-scale output shorted to $V_{CC}$ | | 40 | | |
| | Load regulation | Midscale code, -15 mA ≤ $I_{OUT}$ ≤ 15 mA | | 70 | | µV/mA |
| | Maximum capacitive load (3) | $R_{LOAD}$ = open | 0 | | 1 | nF |
| | DC output impedance | Midscale code | | 0.05 | | Ω |
| | | Full-scale code | | 40 | | |

(1) End point fit between codes. 16-bit: Code 256 to 65280, 14-bit: Code 128 to 16256, 12-bit: Code 32 to 4064.
(2) Temporary overload condition protection. Junction temperature can be exceeded during current limit. Operation above the specified maximum junction temperature may impair device reliability.
(3) Specified by design and characterization, not production tested.


Copyright © 2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

all minimum/maximum specifications at $T_A$ = -40℃ to +125℃ and all typical specifications at $T_A$ = 25℃, $V_{CC}$ = 9 V to 41.5 V, $V_{SS}$ = -21.5 V to 0 V, $V_{DD}$ = $V_{AA}$ = 4.5 V to 5.5 V, $V_{REFIN}$ = 2.5 V, $V_{IO}$ = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at $V_{IO}$ or GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | |
| | Output voltage settling time | ¼ to ¾ scale and ¾ to ¼ scale settling time to ±1 LSB, ±10 V range, $R_L$ = 5 kΩ, $C_L$ = 200 pF | | 12 | | µs |
| | Slew rate | 0 to 5 V range | | 1 | | V/µs |
| | | All other output ranges | | 4 | | |
| | Power-on glitch magnitude | Power-down to active DAC output. ±20 V range, midscale code, $R_L$ = 5 kΩ, $C_L$ = 200 pF | | 0.3 | | V |
| | Output noise | 0.1 Hz to 10 Hz, midscale code, 0 to 5 V range | | 15 | | µVpp |
| | Output noise density | 1 kHz, midscale code, 0 to 5 V range | | 78 | | nV/Hz |
| | AC PSRR | Midscale code, frequency = 60 Hz, amplitude 200 mVpp superimposed on $V_{DD}$, $V_{CC}$ or $V_{SS}$ | | 1 | | LSB/V |
| | DC PSRR | Midscale code, $V_{DD}$ = 5 V ± 5%, $V_{CC}$ = 20 V, $V_{SS}$ = -20 V | | 1 | | LSB/V |
| | | Midscale code, $V_{DD}$ = 5 V, $V_{CC}$ = 20 V ± 5%, $V_{SS}$ = -20 V | | 1 | | |
| | | Midscale code, $V_{DD}$ = 5 V, $V_{CC}$ = 20 V, $V_{SS}$ = -20 V ± 5% | | 1 | | |
| | Code change glitch impulse | 1 LSB change around major carrier, 0 to 5 V range | | 4 | | nV-s |
| | Channel to Channel AC crosstalk | 0 to 5 V range. Measured channel at midscale. Full-scale swing on all other channels | | 4 | | nV-s |
| | Channel to Channel DC crosstalk | 0 to 5 V range. Measured channel at midscale. All other channels at full-scale | | 0.25 | | LSB |
| | Digital feedthrough | 0 to 5 V range. Midscale code, $f_{SCLK}$ = 1 MHz | | 1 | | nV-s |

Copyright © 2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

all minimum/maximum specifications at $T_A$ = -40℃ to +125℃ and all typical specifications at $T_A$ = 25℃, $V_{CC}$ = 9 V to 41.5 V, $V_{SS}$ = -21.5 V to 0 V, $V_{DD}$ = $V_{AA}$ = 4.5 V to 5.5 V, $V_{REFIN}$ = 2.5 V, $V_{IO}$ = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at $V_{IO}$ or GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **EXTERNAL REFERENCE INPUT** | | | | | | |
| $V_{REFIN}$ | Reference input voltage range | to $V_{REFGND}$ | 2.49 | 2.5 | 2.51 | V |
| | Reference input current | | | 50 | | µA |
| | Reference input impedance | | | 50 | | kΩ |
| | Reference input capacitance | | | 20 | | pF |
| **INTERNAL REFERENCE** | | | | | | |
| $V_{REFOUT}$ | Reference output voltage range | $T_A$ = 25°C | 2.4975 | | 2.5025 | V |
| | Reference output drift | | | 5 | 15 | ppm/°C |
| | Reference output impedance | | | 0.1 | | Ω |
| | Reference output noise | 0.1 Hz to 10 Hz | | 12 | | µVpp |
| | Reference output noise density | 10 kHz, $REF_{LOAD}$ = 10 nF | | 150 | | nV/Hz |
| | Reference load current | | | 5 | | mA |
| | Reference load regulation | Source | | 80 | | µV/mA |
| | Reference line regulation | | | 20 | | µV/V |
| | Reference output drift over time | $T_A$ = 25°C, 1900 hours | | 250 | | µV |
| | Reference thermal hysteresis | First cycle | | ±700 | | µV |
| | | Additional cycle | | ±50 | | |
| **DIGITAL INPUTS AND OUTPUTS** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 × $V_{IO}$ | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 × $V_{IO}$ | V |
| | Input current | | | ±2 | | µA |
| | Input pin capacitance | | | 2 | | pF |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 0.2 mA | $V_{IO}$ - 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 0.2 mA | | | 0.4 | V |
| | Output pin capacitance | | | 5 | | pF |
| **ALARM OUTPUT** | | | | | | |
| | Output pin capacitance | | | 5 | | pF |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = -0.2 mA | | | 0.4 | V |
| **TEMPERATURE OUTPUT** | | | | | | |
| $V_{TEMPOUT,0C}$ | Output voltage offset at 0℃ | | | 1.34 | | V |
| | Sensor gain | | | -4 | | mV/°C |


Copyright © 2018, Texas Instruments Incorporated

## Electrical Characteristics (continued)

all minimum/maximum specifications at $T_A$ = -40℃ to +125℃ and all typical specifications at $T_A$ = 25℃, $V_{CC}$ = 9 V to 41.5 V, $V_{SS}$ = -21.5 V to 0 V, $V_{DD}$ = $V_{AA}$ = 4.5 V to 5.5 V, $V_{REFIN}$ = 2.5 V, $V_{IO}$ = 1.7 V to 5.5 V, DAC outputs unloaded, Digital inputs at $V_{IO}$ or GND (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER REQUIREMENTS** | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static. | | 0.05 | 0.5 | mA |
| | | Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static. | | 0.05 | 0.5 | mA |
| | | Power-down mode | | 0.05 | 0.5 | mA |
| $I_{AA}$ | $V_{AA}$ supply current | Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static. | | 20 | 30 | mA |
| | | Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static. | | 18 | 28 | mA |
| | | Power-down mode | | 2 | 85 | µA |
| $I_{CC}$ | $V_{CC}$ supply current | Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static. | | 5 | 10 | mA |
| | | Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static. | | 5 | 10 | mA |
| | | Power-down mode | | 10 | 30 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | Active mode. Internal reference enabled. Full-scale code. ±20 V output range. SPI static. | -10 | -5 | | mA |
| | | Active mode. Internal reference disabled. Full-scale code. ±20 V output range. SPI static. | -10 | -5 | | mA |
| | | Power-down mode | -30 | -10 | | µA |
| $I_{IO}$ | $V_{IO}$ supply current | SCLK and SDI toggling at 50 MHz | | 350 | 500 | µA |

Copyright © 2018, Texas Instruments Incorporated

## 8.6 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SERIAL INTERFACE - WRITE OPERATION** | | | | | | |
| $f_{(SCLK)}$ | Serial clock frequency | $V_{IO}$ = 1.7 V to 2.7 V | | | 25 | MHz |
| | | $V_{IO}$ = 2.7 V to 5.5 V | | | 50 | |
| $t_{SCLKHIGH}$ | SCLK high time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 10 | | | |
| $t_{SCLKLOW}$ | SCLK low time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 10 | | | |
| $t_{SDIS}$ | SDI setup time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{SDIH}$ | SDI hold time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSS}$ | $\overline{CS}$ to SCLK falling edge setup time | $V_{IO}$ = 1.7 V to 2.7 V | 30 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 15 | | | |
| $t_{CSH}$ | SCLK falling edge to $\overline{CS}$ rising edge | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSHIGH}$ | $\overline{CS}$ hight time | $V_{IO}$ = 1.7 V to 2.7 V | 50 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 25 | | | |
| $t_{DACWAIT}$ | Sequential DAC update wait time | $V_{IO}$ = 1.7 V to 2.7 V | 2.4 | | | µs |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 2.4 | | | |
| $t_{BCASTWAIT}$ | Broadcast DAC update wait time | $V_{IO}$ = 1.7 V to 2.7 V | 4 | | | µs |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 4 | | | |
| **SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 0** | | | | | | |
| $f_{(SCLK)}$ | Serial clock frequency | $V_{IO}$ = 1.7 V to 2.7 V | | | 15 | MHz |
| | | $V_{IO}$ = 2.7 V to 5.5 V | | | 20 | |
| $t_{SCLKHIGH}$ | SCLK high time | $V_{IO}$ = 1.7 V to 2.7 V | 33 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 25 | | | |
| $t_{SCLKLOW}$ | SCLK low time | $V_{IO}$ = 1.7 V to 2.7 V | 33 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 25 | | | |
| $t_{SDIS}$ | SDI setup time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{SDIH}$ | SDI hold time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSS}$ | $\overline{CS}$ to SCLK falling edge setup time | $V_{IO}$ = 1.7 V to 2.7 V | 30 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 20 | | | |
| $t_{CSH}$ | SCLK falling edge to $\overline{CS}$ rising edge | $V_{IO}$ = 1.7 V to 2.7 V | 8 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSHIGH}$ | $\overline{CS}$ high time | $V_{IO}$ = 1.7 V to 2.7 V | 50 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 25 | | | |
| $t_{SDOZD}$ | SDO tri-state to driven | $V_{IO}$ = 1.7 V to 2.7 V | 0 | | 20 | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 0 | | 20 | |
| $t_{SDODLY}$ | SDO output delay | $V_{IO}$ = 1.7 V to 2.7 V | 0 | | 35 | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 0 | | 20 | |


Copyright © 2018, Texas Instruments Incorporated

## Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SERIAL INTERFACE - READ AND DAISY CHAIN OPERATION, FSDO = 1** | | | | | | |
| $f_{(SCLK)}$ | Serial clock frequency | $V_{IO}$ = 1.7 V to 2.7 V | | | 25 | MHz |
| | | $V_{IO}$ = 2.7 V to 5.5 V | | | 35 | |
| $t_{SCLKHIGH}$ | SCLK high time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 14 | | | |
| $t_{SCLKLOW}$ | SCLK low time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 14 | | | |
| $t_{SDIS}$ | SDI setup time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{SDIH}$ | SDI hold time | $V_{IO}$ = 1.7 V to 2.7 V | 10 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSS}$ | $\overline{CS}$ to SCLK falling edge setup time | $V_{IO}$ = 1.7 V to 2.7 V | 30 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 20 | | | |
| $t_{CSH}$ | SCLK falling edge to $\overline{CS}$ rising edge | $V_{IO}$ = 1.7 V to 2.7 V | 8 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 5 | | | |
| $t_{CSHIGH}$ | $\overline{CS}$ high time | $V_{IO}$ = 1.7 V to 2.7 V | 50 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 25 | | | |
| $t_{SDOZD}$ | SDO tri-state to driven | $V_{IO}$ = 1.7 V to 2.7 V | 0 | | 20 | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 0 | | 20 | |
| $t_{SDODLY}$ | SDO output delay | $V_{IO}$ = 1.7 V to 2.7 V | 0 | | 35 | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 0 | | 20 | |
| **DIGITAL LOGIC** | | | | | | |
| $t_{LOGDLY}$ | $\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time | $V_{IO}$ = 1.7 V to 2.7 V | 40 | | | ns |
| $t_{LOGDLY}$ | $\overline{CS}$ rising edge to $\overline{LDAC}$ or $\overline{CLR}$ falling edge delay time | $V_{IO}$ = 2.7 V to 5.5 V | 20 | | | |
| $t_{LDAC}$ | $\overline{LDAC}$ low time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 10 | | | |
| $t_{CLR}$ | $\overline{CLR}$ low time | $V_{IO}$ = 1.7 V to 2.7 V | 20 | | | ns |
| | | $V_{IO}$ = 2.7 V to 5.5 V | 10 | | | |
| $t_{RESET}$ | POR reset delay | $V_{IO}$ = 1.7 V to 2.7 V | | | 1 | ms |
| | | $V_{IO}$ = 2.7 V to 5.5 V | | | 1 | |
| $f_{TOGGLE}$ | TOGGLE frequency | $V_{IO}$ = 1.7 V to 2.7 V | | | 100 | kHz |
| | | $V_{IO}$ = 2.7 V to 5.5 V | | | 100 | |

Copyright © 2018, Texas Instruments Incorporated

## 8.7 Typical Characteristics

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

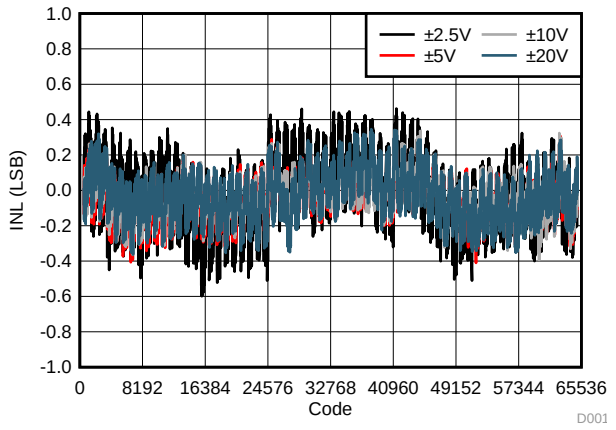



**図 1. Integral Linearity Error vs Digital Input Code (Bipolar Outputs)**

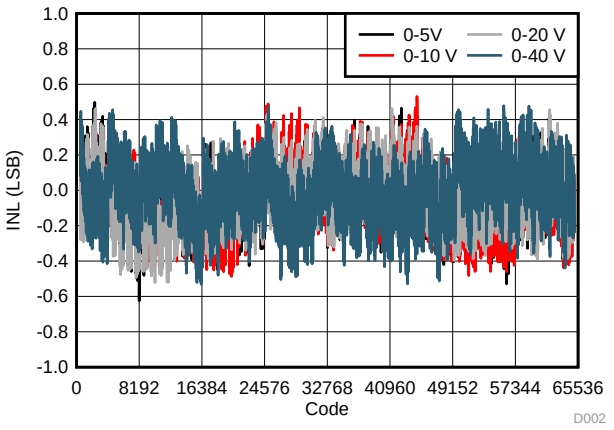



**図 2. Integral Linearity Error vs Digital Input Code (Unipolar Outputs)**

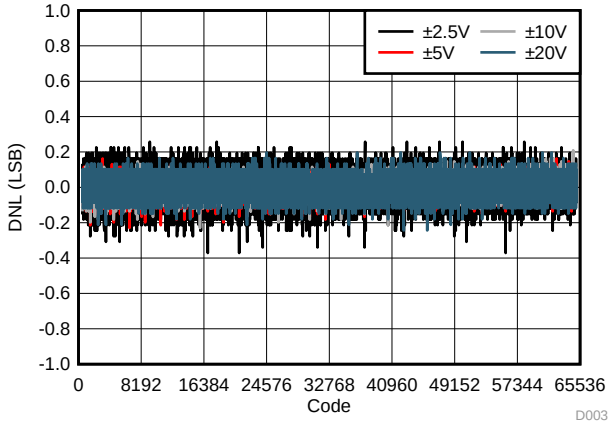



**図 3. Differential Linearity Error vs Digital Input Code (Bipolar Outputs)**

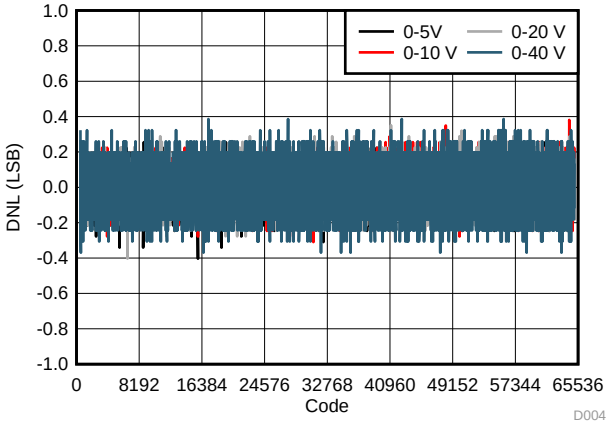



**図 4. Differential Linearity Error vs Digital Input Code (Unipolar Outputs)**

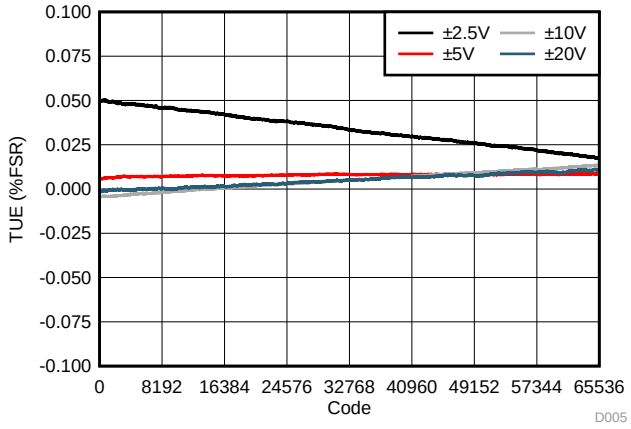



**図 5. Total Unadjusted Error vs Digital Input Code (Bipolar Outputs)**

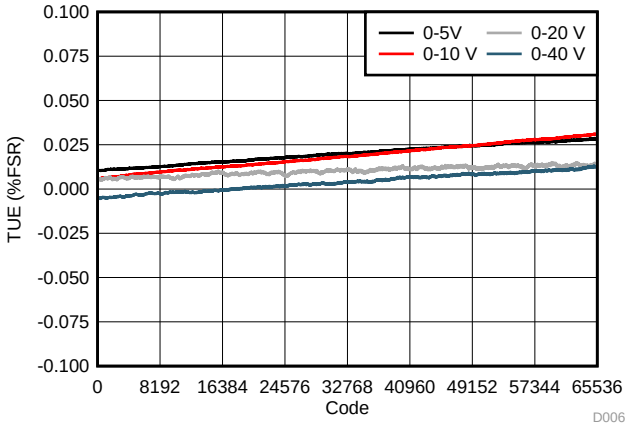



**図 6. Total Unadjusted Error vs Digital Input Code (Unipolar Outputs)**


Copyright © 2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

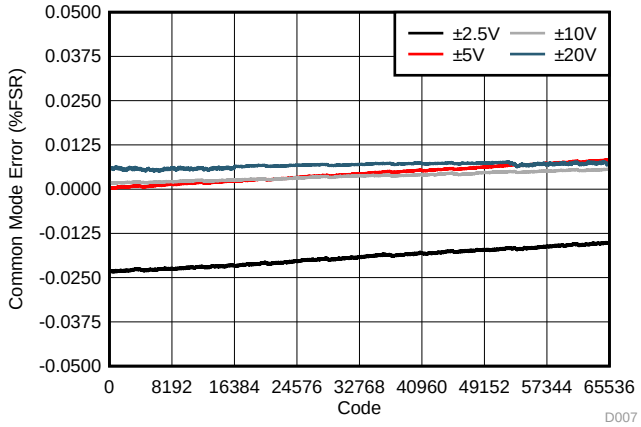



図 7. Common Mode Error vs Digital Input Code (Differential Bipolar Outputs)

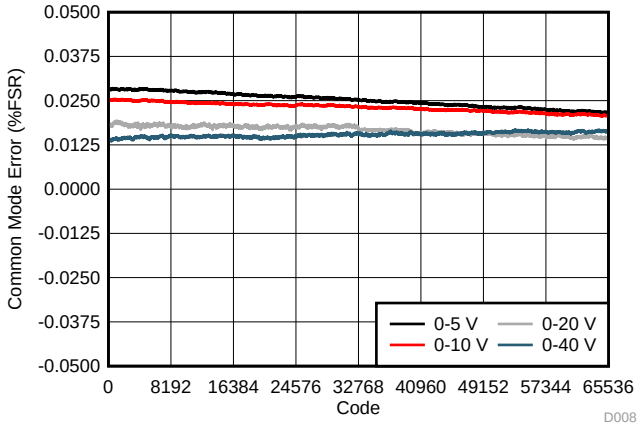
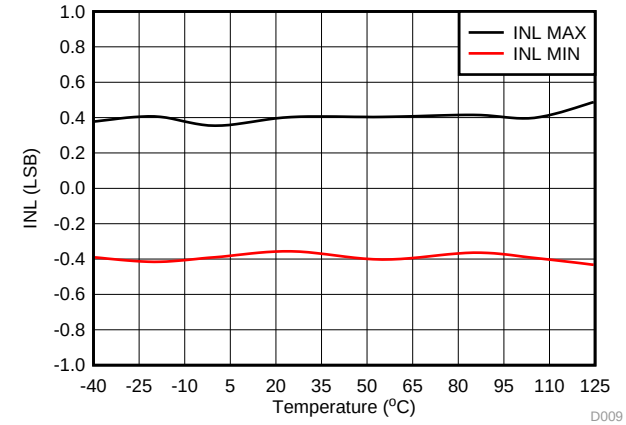
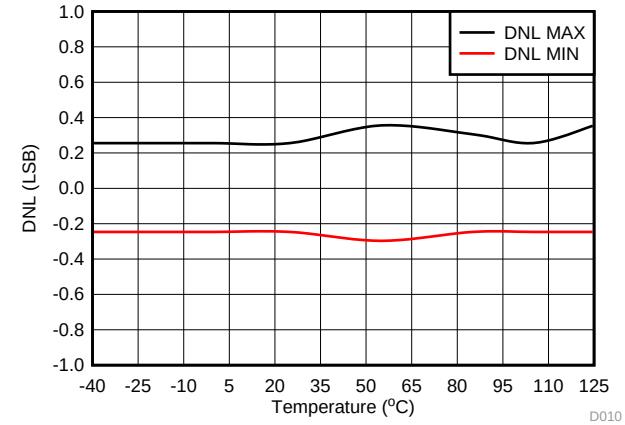



図 8. Common Mode Error vs Digital Input Code (Differential Unipolar Outputs)




±20-V Output Range

図 9. Integral Linearity Error vs Temperature




±20-V Output Range

図 10. Differential Linearity Error vs Temperature

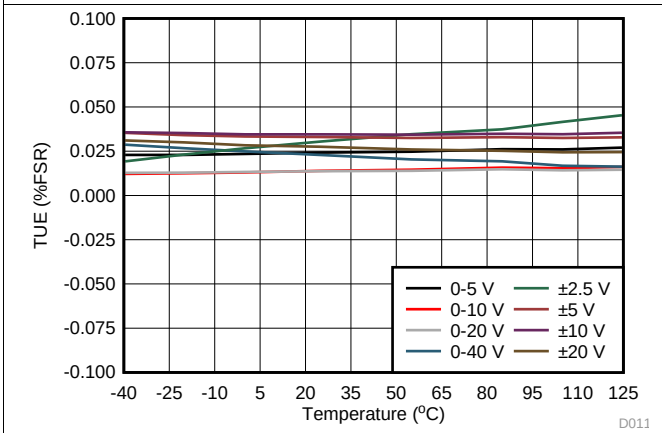



図 11. Total Unadjusted Error vs Temperature

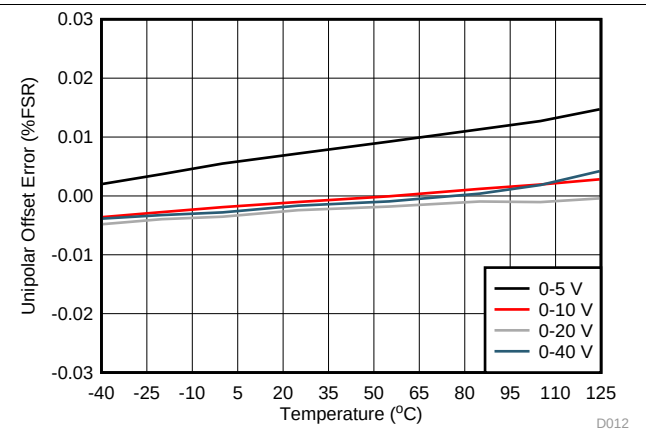



図 12. Unipolar Offset Error vs Temperature

Copyright © 2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

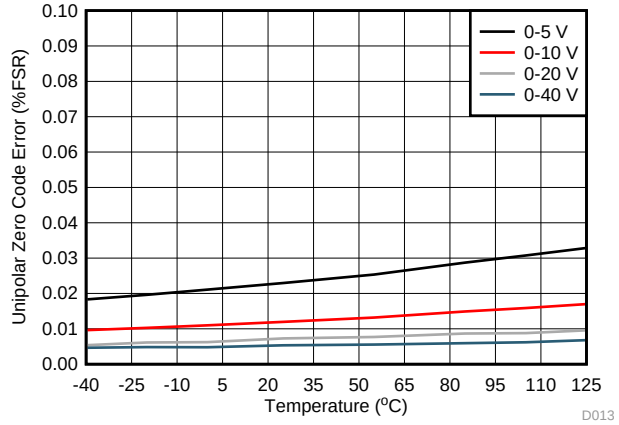



図 13. Unipolar Zero Code Error vs Temperature

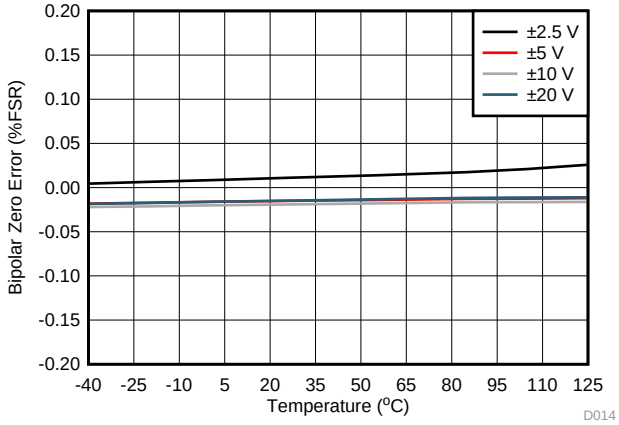



図 14. Bipolar Zero Error vs Temperature

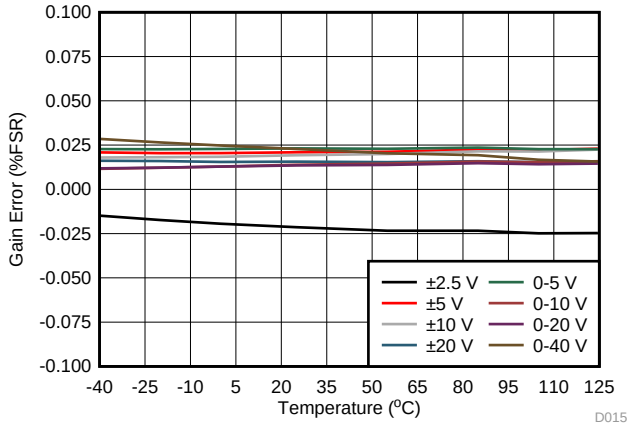



図 15. Gain Error vs Temperature

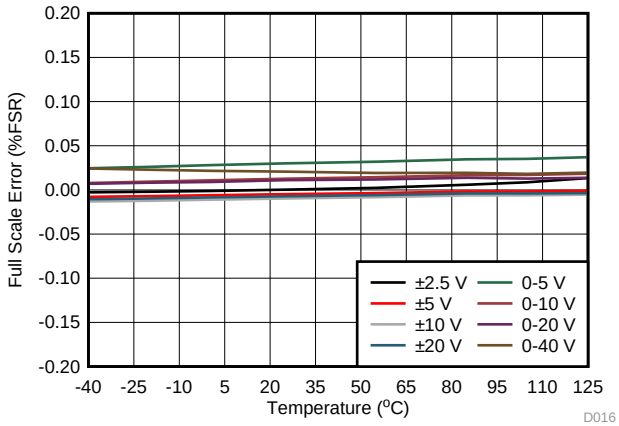



図 16. Full-Scale Error vs Temperature

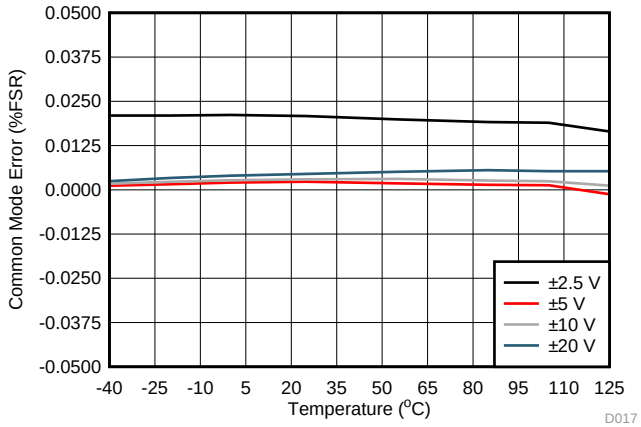



図 17. Common Mode Error vs Temperature (Differential Bipolar Outputs)

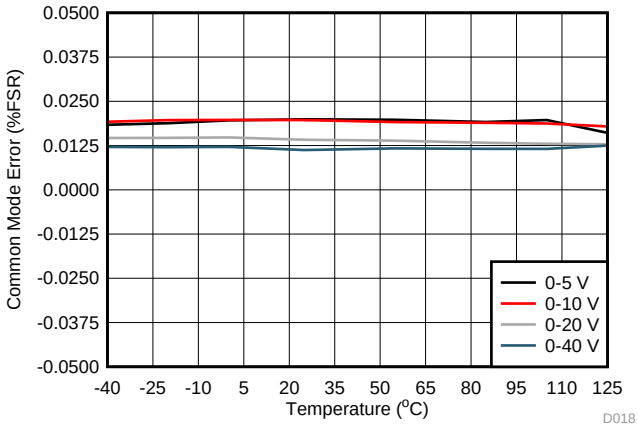
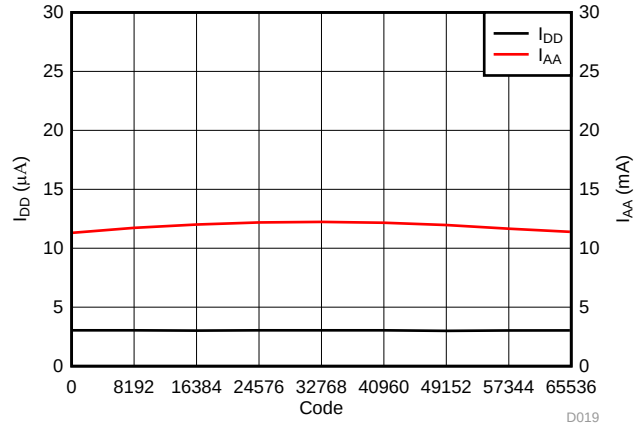



図 18. Common Mode Error vs Temperature (Differential Unipolar Outputs)


Copyright © 2018, Texas Instruments Incorporated

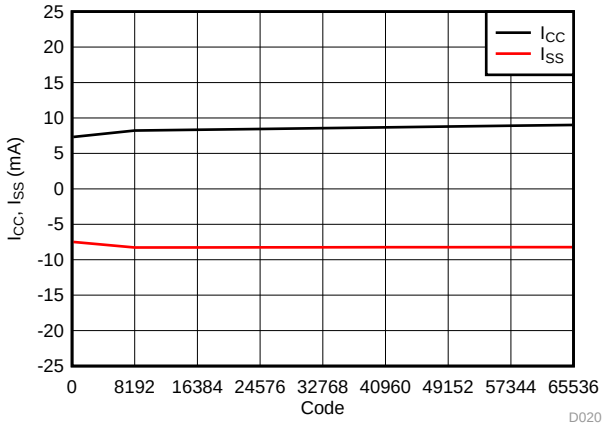
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



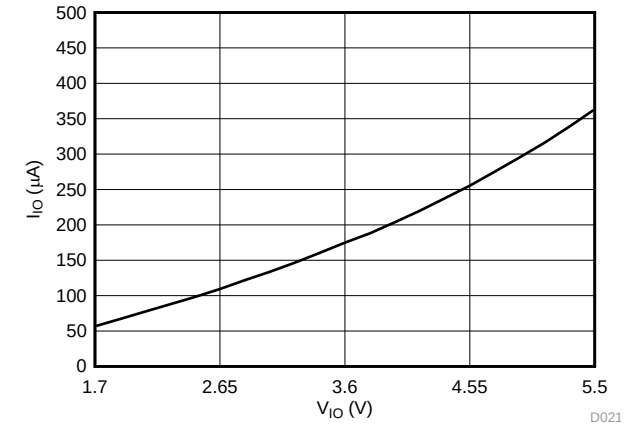

±20-V Output Range

**図 19. Supply Current ($I_{DD}$, $I_{AA}$) vs Digital Input Code**



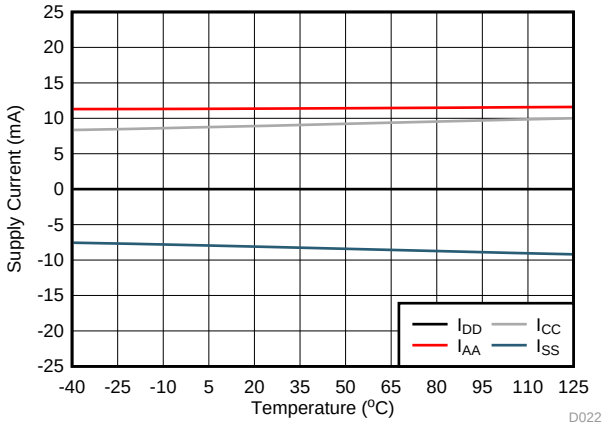

±20-V Output Range

**図 20. Supply Current ($I_{CC}$, $I_{SS}$) vs Digital Input Code**



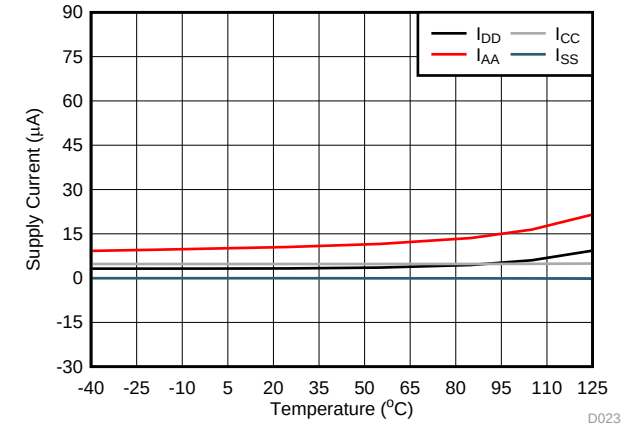

±20-V Output Range

**図 21. Supply Current ($I_{IO}$) vs Supply Voltage**



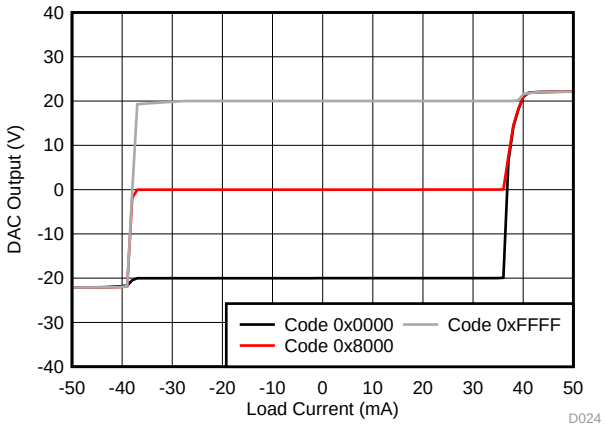

±20-V Output Range

**図 22. Supply Current vs Temperature**




±20-V Output Range

**図 23. Power-Down Current vs Temperature**



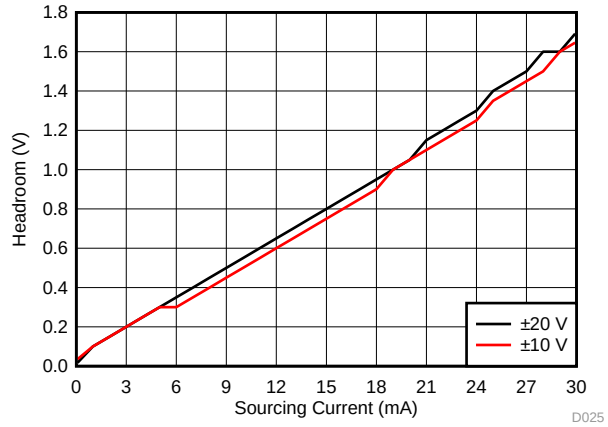

±20-V Output Range

**図 24. Source and Sink Capability**

Copyright © 2018, Texas Instruments Incorporated

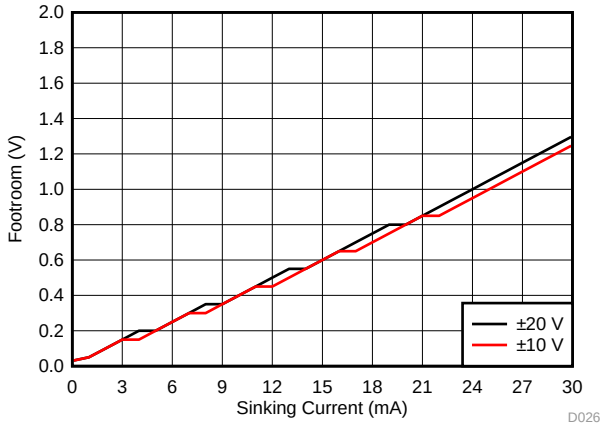
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.



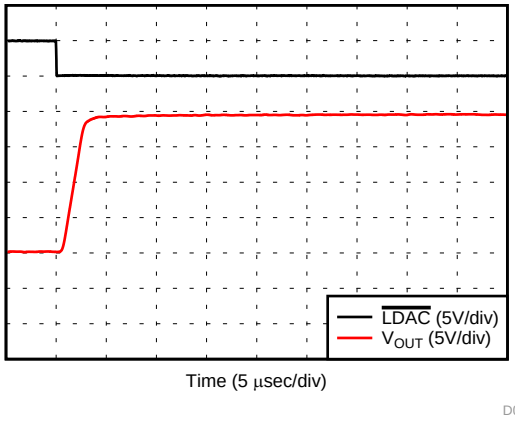

Full-scale Code

**図 25. $V_{CC}$ Headroom vs Sourcing Current**



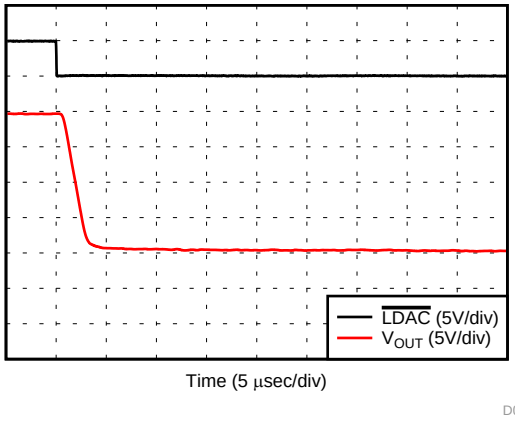

Zero Code

**図 26. $V_{SS}$ Footroom vs Sinking Current**



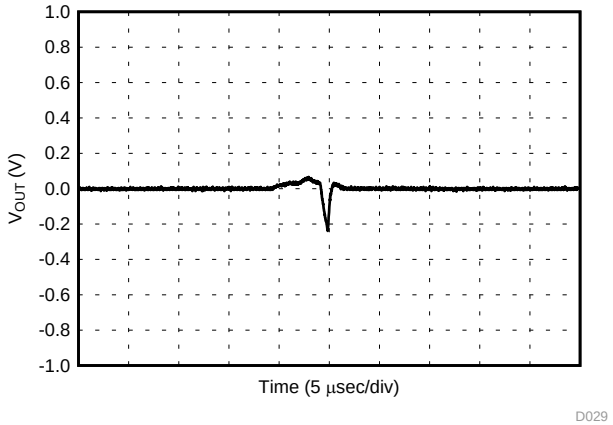

±20-V Output Range

**図 27. Full-Scale Settling Time, Rising Edge**



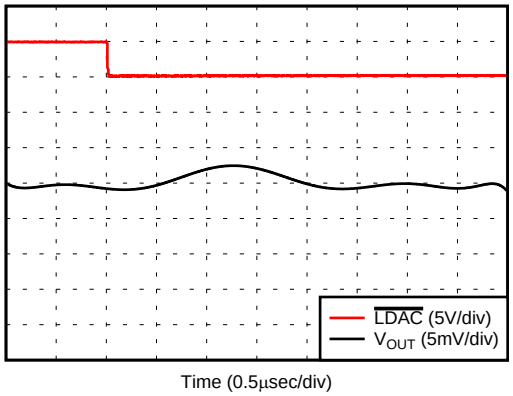

±20-V Output Range

**図 28. Full-Scale Settling Time, Falling Edge**




Power-down to Active DAC Mode
±20-V Output Range

**図 29. DAC Output Enable Glitch**



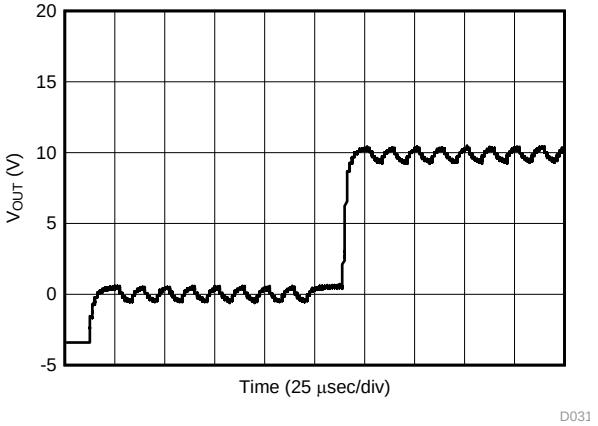

0 to 5-V Output Range

**図 30. Glitch Impulse, 1 LSB Step**


Copyright © 2018, Texas Instruments Incorporated

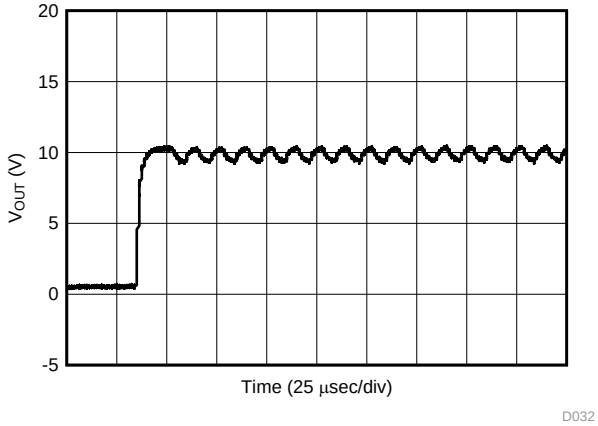
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.




±20-V Output Range
Toggle signal: 1 $V_{PP}$
DC Change: Midscale to 3/4 Full-scale

**図 31. Toggle Output Change Response**




±20-V Output Range
Toggle signal: 1 $V_{PP}$
DC value: 3/4 Full-scale

**図 32. Toggle Enable Response**

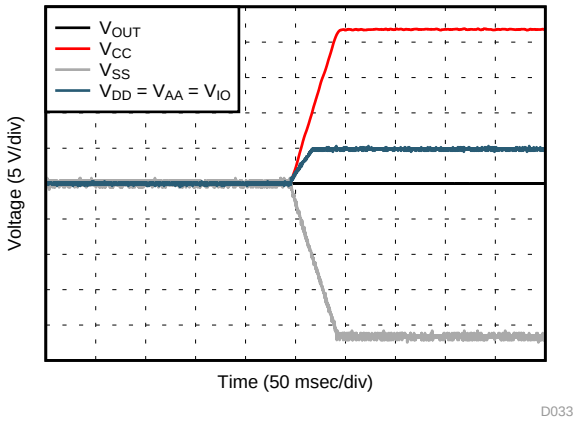



**図 33. Power-Up Response**

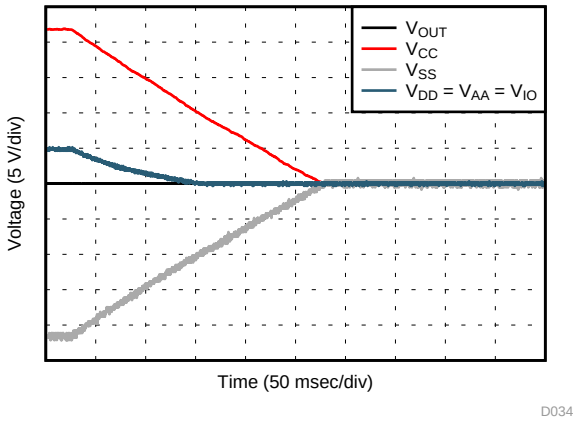
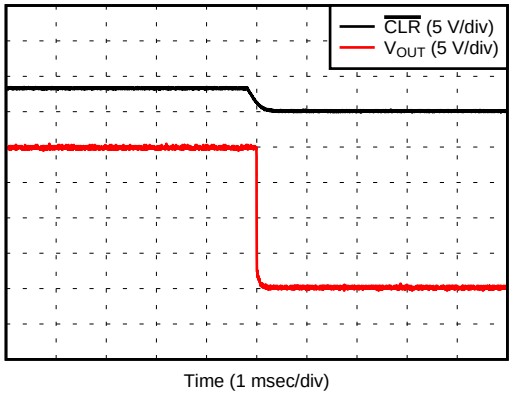
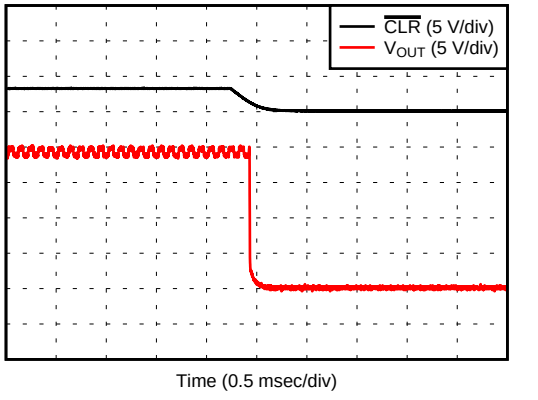



**図 34. Power-Down Response**




±20-V Output Range
Full-scale Code to 0 V

**図 35. Clear Command Response**



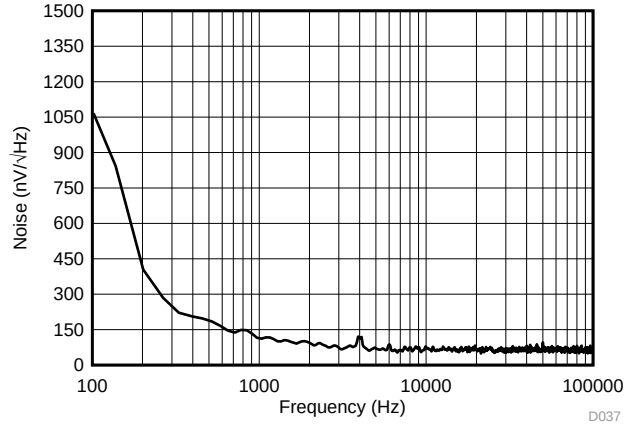

±20-V Output Range
Toggle signal: 1 $V_{PP}$
DC value at 20 V

**図 36. Clear Command Response in Toggle Mode**

Copyright © 2018, Texas Instruments Incorporated

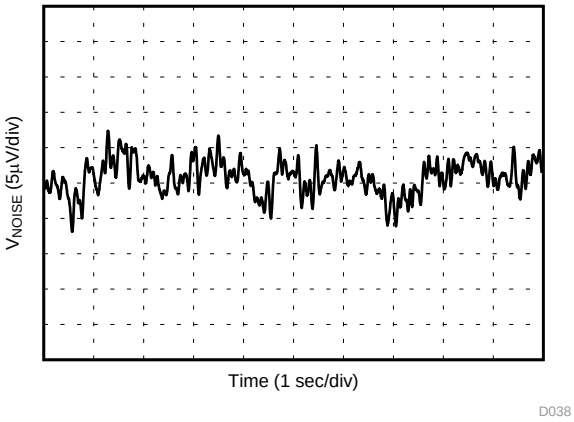
## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.




0 to 5-V Output Range
Midscale Code

**図 37. DAC Output Noise Density vs Frequency**




0 to 5-V Output Range
Midscale Code

**図 38. DAC Output Noise**

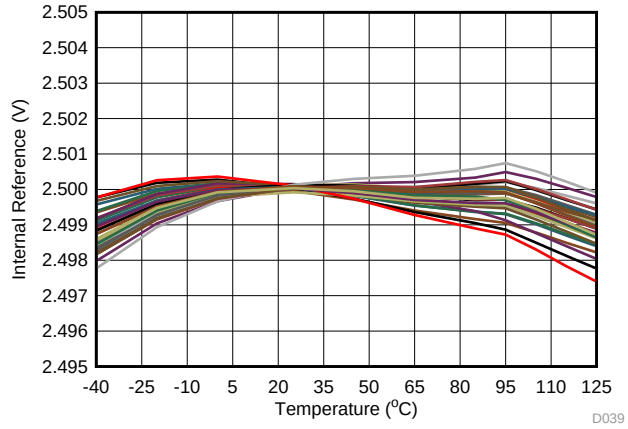



**図 39. Internal Reference Voltage vs Temperature**

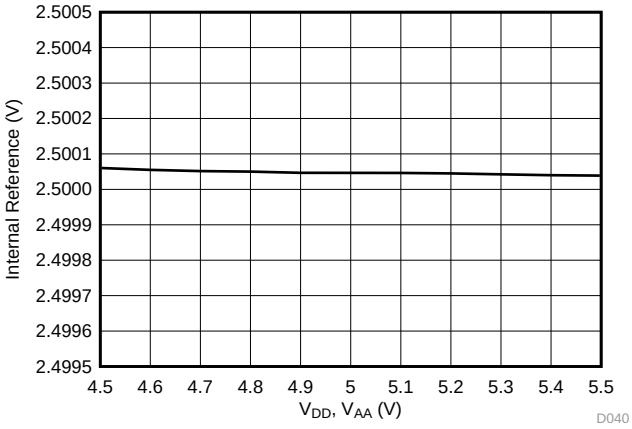



**図 40. Internal Reference Voltage vs Supply Voltage**

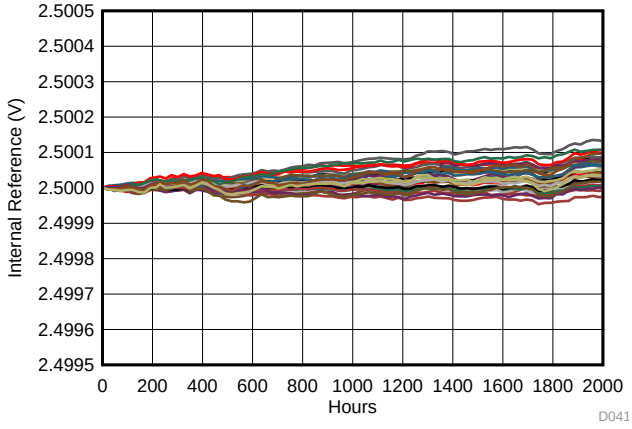



**図 41. Internal Reference Voltage vs Time**

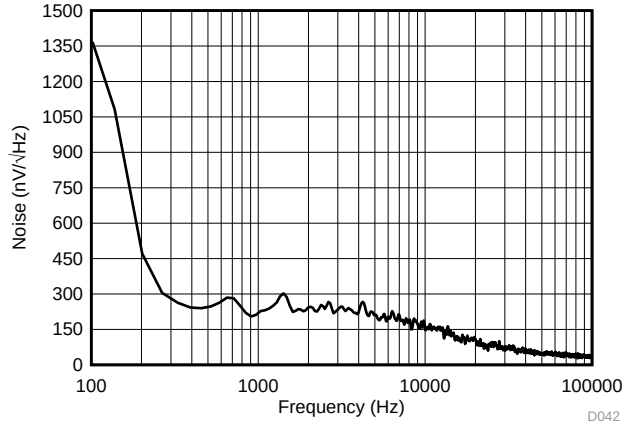



**図 42. Internal Reference Noise Density vs Frequency**


Copyright © 2018, Texas Instruments Incorporated

## Typical Characteristics (continued)

at $T_A$ = 25°C, $V_{DD}$ = $V_{AA}$ = 5 V, $V_{REFIN}$ = 2.5 V. Unipolar ranges: $V_{SS}$ = 0 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. Bipolar ranges: $V_{SS}$ ≤ $V_{MIN}$ – 1.5 V and $V_{CC}$ ≥ $V_{MAX}$ + 1.5 V for the DAC range. DAC outputs unloaded, unless otherwise noted.

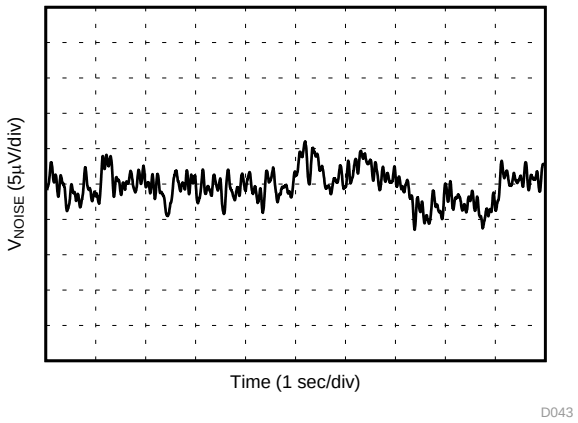



**図 43. Internal Reference Noise**

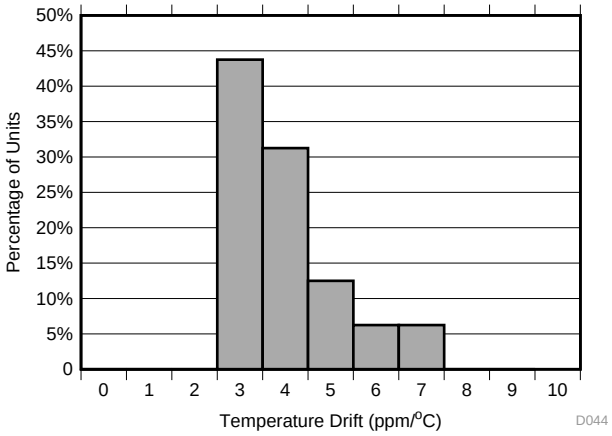



**図 44. Internal Reference Temperature Drift Histogram**

# 9 Parameter Measurement Information

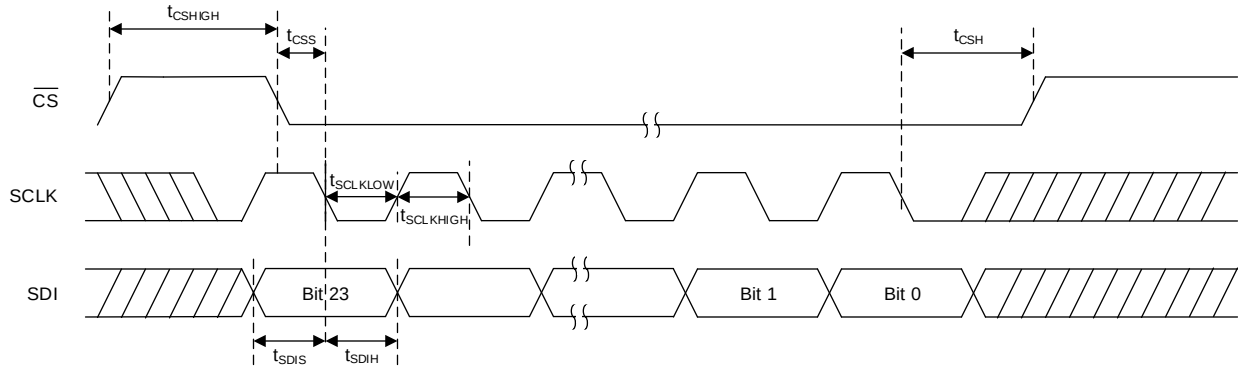



**図 45. Serial Interface Write Timing Diagram**

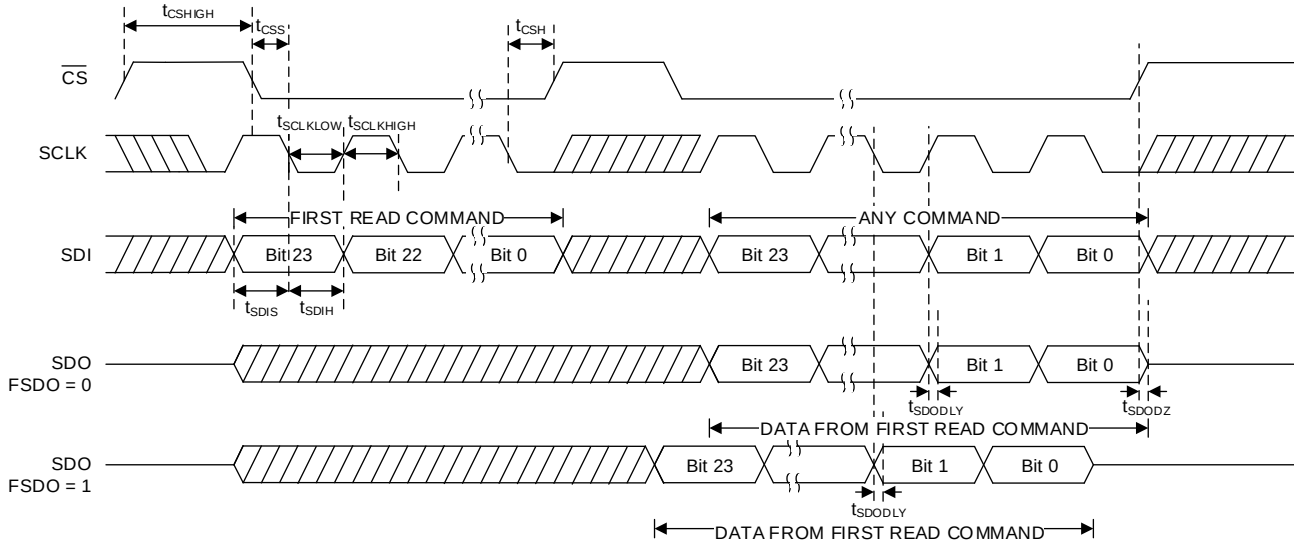



**図 46. Serial Interface Read Timing Diagram**


Copyright © 2018, Texas Instruments Incorporated

# 10 Detailed Description

## 10.1 Overview

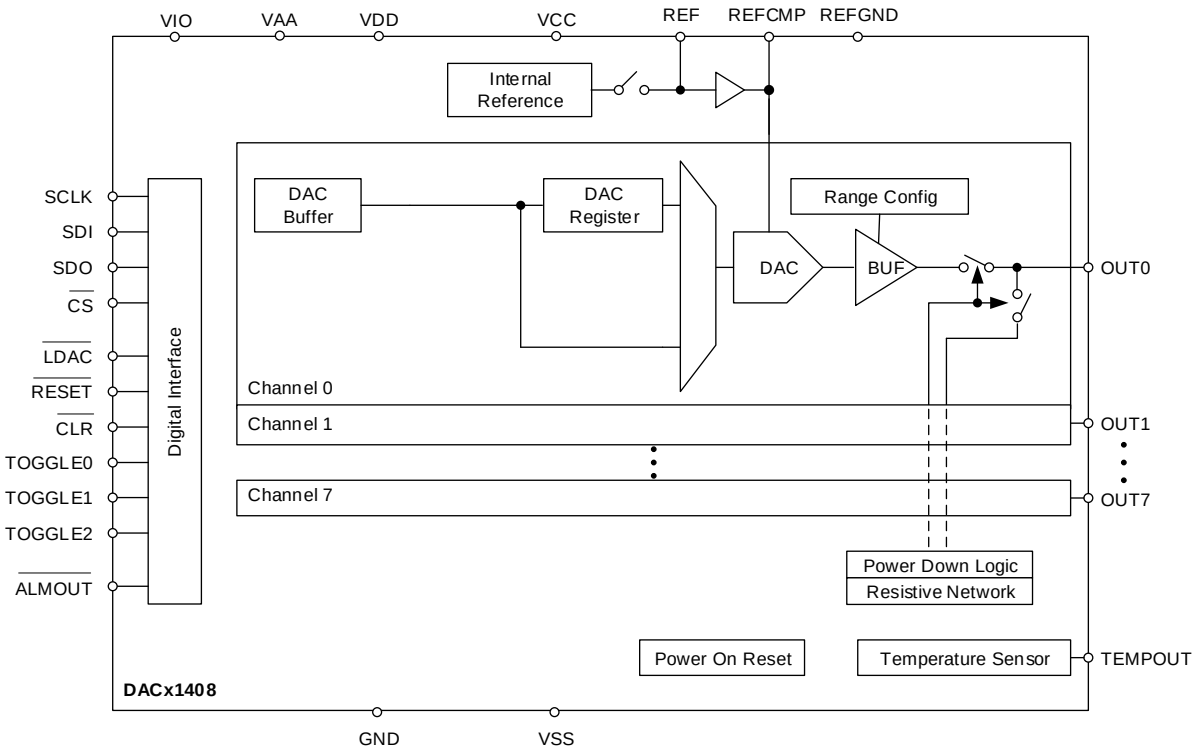
The DACx1408 is a pin-compatible family of 8-channel, buffered, high-voltage output digital-to-analog converters (DACs) with 16-, 14- and 12-bit resolution. The DACx1408 includes a 2.5-V internal reference. A user selectable output configuration enables full-scale bipolar output voltages: ±20 V, ±10 V, ±5 V or ±2.5 V and full-scale unipolar output voltages: 40 V, 20 V, 10 V or 5 V. The full-scale output range for each DAC channel is independently programmable. In addition, each pair of DAC channels can be configured to provide a differential output. Three dedicated A-B toggle pins enable dither signal generation with up to three possible frequencies.

The DACx1408 operates from five supply voltages: $V_{DD}$, $V_{AA}$, $V_{CC}$, $V_{SS}$ and $V_{IO}$. $V_{DD}$ and $V_{AA}$ are the digital and analog supplies for the DACs, internal reference and other low voltage components and must be set at the same potential. $V_{CC}$ and $V_{SS}$ are the positive and analog supplies for the DAC output amplifiers. $V_{IO}$ sets the logic levels for the digital inputs and outputs.

Communication to the DACx1408 is performed through a 4-wire serial interface that supports stand-alone and daisy-chain operation. The optional frame-error checking provides added robustness to the DACx1408 serial interface.

The DACx1408 incorporates a power-on-reset circuit that connects the DAC outputs to ground at power-up. The outputs remain at this state until the device registers are properly configured for operation.

## 10.2 Functional Block Diagram



## 10.3 Feature Description

### 10.3.1 Digital-to-Analog Converters (DACs) Architecture

Each output channel in the DACx1408 consists of an R-2R ladder architecture followed by an output buffer amplifier capable of rail-to-rail operation. The output amplifiers can drive 25 mA with 1.5-V headroom from either $V_{CC}$ or $V_{SS}$ while maintaining the specified TUE specification for the device. The full-scale output voltage for each channel can be individually configured to the following ranges:

- -20 V to +20 V
- -10 V to +10 V
- -5 V to +5 V
- -2.5 V to +2.5 V
- 0 V to +40V
- 0 V to +20 V
- 0 V to +10 V
- 0 V to +5 V

図 47 shows a block diagram of the DAC architecture.

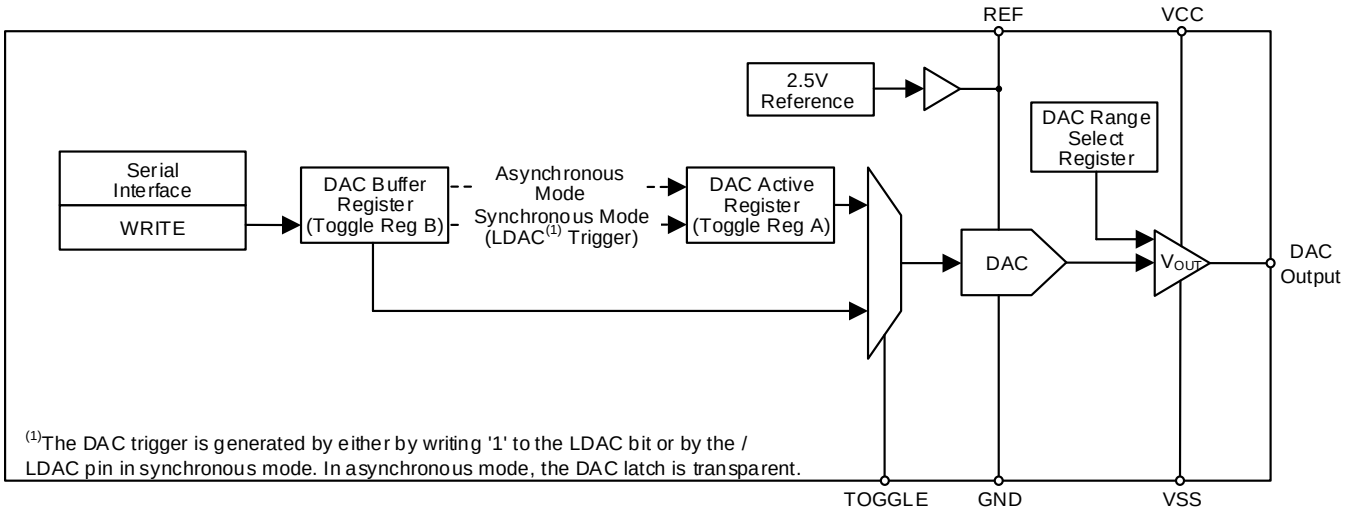



**図 47. DACx1408 DAC Block Diagram**

#### *10.3.1.1 DAC Transfer Function*

The input data are written to the individual DAC Data registers in straight binary format for all output ranges. The DAC transfer function is given by 式 1.

$$V_{OUT} = \left( \frac{CODE}{2^n} \times FSR \right) + V_{MIN} \quad (1)$$

where

- CODE is the decimal equivalent of the binary code that is loaded to the DAC register. CODE range is from 0 to $2^n - 1$.
- n is the DAC resolution in bits. Either 12 (DAC61408), 14 (DAC71408) or 16 (DAC81408).
- FSR is the DAC full-scale range. Equal to $V_{MAX} - V_{MIN}$ for the selected DAC output range.
- $V_{MIN}$ is the lowest voltage for the selected DAC output range.


Copyright © 2018, Texas Instruments Incorporated

## Feature Description (continued)

### *10.3.1.2 DAC Register Structure*

Data written to the DAC data registers is initially stored in the DAC buffer registers. Transfer of data from the DAC buffer registers to the active DAC registers can be configured to happen immediately (asynchronous mode) or initiated by a DAC trigger signal (synchronous mode). Once the DAC active registers are updated, the DAC outputs change to the new values.

After a power-on or reset event, all DAC registers are set to zero code, the DAC output amplifiers are powered down, and the DAC outputs are clamped to ground.

#### 10.3.1.2.1 DAC Register Synchronous and Asynchronous Updates

The update mode for each DAC channel is determined by the status of its corresponding SYNC-EN bit. In asynchronous mode, a write to the DAC data register results in an immediate update of the DAC active register and DAC output on a $\overline{CS}$ rising edge. In synchronous mode, writing to the DAC data register doe not automatically update the DAC output. Instead the update occurs only after a trigger event. A DAC trigger signal is generated either through the LDAC bit or by the $\overline{LDAC}$ pin. The synchronous update mode enables simultaneous update of multiple DAC outputs. In both update modes a minimum wait time of 1 µs is required between DAC output updates.

#### 10.3.1.2.2 Broadcast DAC Register

The DAC broadcast register enables a simultaneous update of multiple DAC outputs with the same value with a single register write. Broadcast operation is only possible when all DAC channels are in single-ended mode operation. If one or more outputs are configured in differential mode the broadcast command is ignored.

Each DAC channel can be configured to update or remain unaffected by a broadcast command by setting the corresponding DAC-BRDCAST-EN bit. A register write to the BRDCAST-DATA register forces those DAC channels that have been configured for broadcast operation to update their DAC buffer registers to this value. The DAC outputs update to the broadcast value according to their synchronous mode configuration.

#### 10.3.1.2.3 Clear DAC Operation

The DAC outputs are set in clear mode through the $\overline{CLEAR}$ pin. In clear mode each DAC data channel is set to the clear code associated with its configuration as shown in . A $\overline{CLR}$ pin logic low forces all DAC channels to clear the contents of their buffer and active registers to the clear code, and sets the analog outputs accordingly regardless of their synchronization setting.

**表 1. Clear DAC Value**

| UNIPOLAR / BIPOLAR RANGE | DIFFERENTIAL MODE | CLEAR CODE |
|---|---|---|
| Unipolar | No | Zero code |
| Unipolar | Yes | Midscale code |
| Bipolar | No | Midscale code |
| Bipolar | Yes | Midscale code |

When a DAC is operating in toggle mode, a clear command sets both toggle registers to the clear value.

### 10.3.2 Internal Reference

The DAx1408 include a 2.5-V bandgap reference with a typical temperature drift of 5 ppm/ºC. The internal reference is externally available at the REF pin. An external buffer amplifier with a high impedance input is required to drive any external load.

A minimum 150-nF capacitor is recommended between the reference output and GND for noise filtering. A compensation capacitor (330 pF, typical) should be connected between the REFCMP pin and REFGND.

Operation from an external reference is also supported by powering down the internal reference. The external reference is applied to the REF pin.

Copyright © 2018, Texas Instruments Incorporated

### 10.3.3 Device Reset Options

#### *10.3.3.1 Power-on-Reset (POR)*

The DACx1408 includes a power-on reset function. After the supplies have been established, a POR event is issued. The POR causes all registers to initialize to their default values and communication with the device is valid only after a 1 ms power-on-reset delay. After a POR event, the device is set in power-down mode where all DAC channels and internal reference are powered down and the DAC output pins are connected to ground through a 10-kΩ internal resistor.

#### *10.3.3.2 Hardware Reset*

A device hardware reset event is initiated by a minimum 500 ns logic low on the $\overline{\text{RESET}}$ pin. A hardware reset initiates a POR event.

#### *10.3.3.3 Software Reset*

A device software reset event is initiated by writing the reserved code 0x1010 to SOFT-RESET in the TRIGGER register. The software reset command is triggered on the $\overline{\text{CS}}$ rising edge of the instruction. A software reset initiates a POR event.

### 10.3.4 Thermal Protection

Due to the DACx1408 DAC channel density and high drive capability it is important to understand the effects of power dissipation on the temperature of the device and ensure it does not exceed the maximum junction temperature.

#### *10.3.4.1 Analog Temperature Sensor: TEMPOUT Pin*

The DACx1408 includes an analog temperature monitor with an unbuffered output voltage that is inversely proportional to the device junction temperature. The TEMPOUT pin output voltage has a temperature slope of -4 mV/°C and a 1.34-V offset as described by 式 2.

$$V_{TEMPOUT} = \left( \frac{-4\ mV}{°C} \times T \right) + 1.34\ V \tag{2}$$

where:

- T is the device junction temperature in °C.
- $V_{TEMPOUT}$ is the temperature monitor output voltage.

#### *10.3.4.2 Thermal Shutdown*

The DACx1408 incorporates a thermal shutdown that is triggered when the die temperature exceeds 140ºC. A thermal shutdown sets the TEMP-ALM bit and causes all DAC outputs to power-down, however the internal reference remains powered on. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a thermal shutdown condition by setting the TEMPALM-EN bit. Once a thermal shutdown is triggered, the device stays in shutdown even after the device temperature lowers.

The die temperature must fall below 140ºC before the device can be returned to normal operation. To resume normal operation, the thermal alarm must be cleared through the ALM-RESET bit while the DAC channels are in power-down mode.


Copyright © 2018, Texas Instruments Incorporated

## 10.4 Device Functional Modes

### 10.4.1 Toggle Mode

Each DAC in the device can be independently configured to operate in toggle mode. A DAC channel in toggle mode incorporates two DAC registers (Register A and Register B) and can be set to switch repetitively between these two values. The DACx1408 toggle mode operation can be configured to introduce a dither signal to the DAC output, to generate a periodic signal or to implement ON/OFF signaling, among some examples.

To update the toggle registers the following sequence should be followed:

1. Set DAC channel in synchronous mode and disable toggle mode for that channel
2. Write the desired Register A value to the DAC data register
3. Issue a DAC trigger signal to load Register A
4. Write the desired Register B value to the DAC data register
5. Enable toggle mode to load Register B

Once both registers are loaded with data, any of the three TOGGLE[2:0] pins can be used to switch those DACs configured for toggle operation back and forth between the contents of their two DAC specific registers by using an external clock or logic signal. A TOGGLE pin logic low updates the DAC output to the value set by Register A. A logic high updates the DAC output to the value set by Register B. The three TOGGLE[2:0] pins give the DACx1408 the option to operate with up to three toggle rates.

Additionally, the device can be configured for software controlled toggle operation by setting the SOFTTOGGLE-EN bit. In this mode, any of the three AB-TOG[2:0] bits can be used as a toggle control signal. Setting the ABTOG bit to 1 enables Register B and clearing it to 0 enables Register A.

### 10.4.2 Differential Mode

Each pair of DAC channels in the device can be independently configured to operate as a differential output pair. The differential output of a *DACx-y* pair is updated by writing to the *DACx* channel. For proper operation, the two DAC pairs must be configured to the same output range prior to enabling differential mode. 図 48 and 図 49 show the ideal differential output voltages ($V_{DIFF}$) and common mode voltages ($V_{CM}$) for a DAC differential pair configured for ±20-V and 0 to 40-V operation, respectively.

Once configured as a differential output, the *DACx-y* pair can be set for toggle operation by updating the *DACx* toggle registers as described in Toggle Mode.

Imbalances between the two differential signals result in common-mode and amplitude errors. The device incorporates an offset register that enables the user to introduce a voltage offset to the *DACy* channel of the *DACx-y* differential pair to compensate for a DC offset error between the two channels. The offset compensation gives a ±0.2%FSR adjustment window. The differential DAC data register must be rewritten after an update to the offset register.

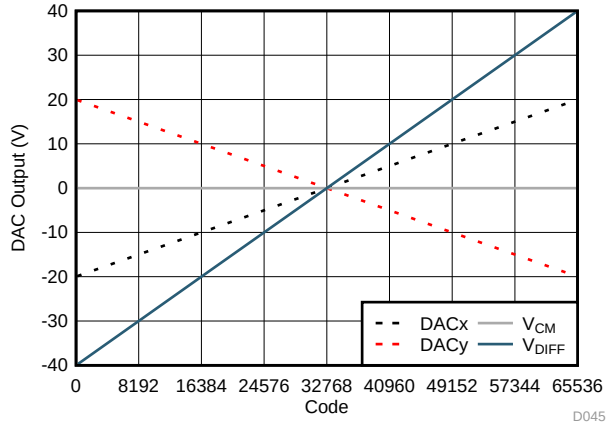



**図 48. Differential Bipolar Output (16-Bit): ±20-V Output Range**

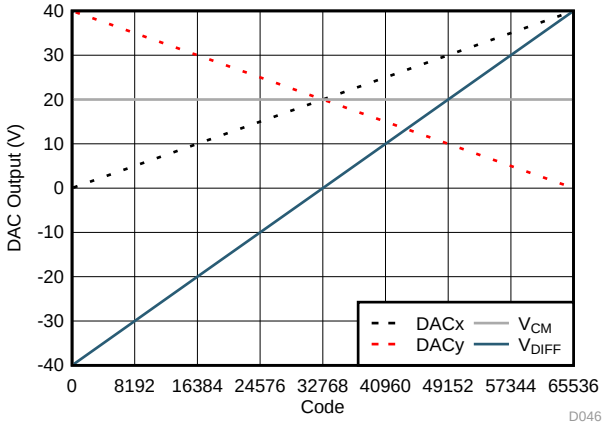



**図 49. Differential Unipolar Output (16-Bit): 0 to 40-V Output Range**

Copyright © 2018, Texas Instruments Incorporated

## Device Functional Modes (continued)

### 10.4.3 Power-Down Mode

The DACx1408 DAC output amplifiers and internal reference power-down status can be individually configured and monitored though the PWDWN registers. Setting a DAC channel in power-down mode disables the output amplifier and clamps the output pin to ground through an internal 10-kΩ resistor.

The DAC data registers are not cleared when the DAC goes into power-down which makes it possible to have the same output voltage upon return to normal operation. The DAC data registers can also be updated while in power-down mode.

After a power-on or reset event all the DAC channels and the internal reference are in power-down mode. The entire device can be configured into power-down or active modes through the DEV-PWDWN bit.


Copyright © 2018, Texas Instruments Incorporated

## 10.5 Programming

The DACx1408 is controlled through a flexible four-wire serial interface that is compatible with SPI type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the DACx1408 registers and can be configured to daisy-chain multiple devices for write operations. The DACx1408 incorporates an optional error checking mode to validate SPI data communication integrity in noisy environments.

### 10.5.1 Stand-Alone Operation

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long with error checking disabled and 32 bits long with error checking enabled, thus the $\overline{CS}$ pin must stay low for at least 24 or 32 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is de-asserted high. If the access cycle contains less than then minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the first 24 or 32 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO is in a Hi-Z state.

In an error checking disabled access cycle (24 bits long) the first byte input to SDI is the instruction cycle which identifies the request as a read or write command and the 6-bit address to be accessed. The last 16 bits in the cycle form the data cycle.

**表 2. Serial Interface Access Cycle**

| BIT | FIELD | DESCRIPTION |
|---|---|---|
| 23 | RW | Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation. |
| 22 | x | Don't care bit. |
| 21-16 | A[5:0] | Register address. Specifies the register to be accessed during the read or write operation. |
| 15-0 | DI[15:0] | Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values. |

Read operations require that the SDO pin is first enabled by setting the SDO-EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data. Data are clocked out on SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit.

**表 3. SDO Output Access Cycle**

| BIT | FIELD | DESCRIPTION |
|---|---|---|
| 23 | RW | Echo RW from previous access cycle. |
| 22 | x | Echo bit 22 from previous access cycle. |
| 21-16 | A[5:0] | Echo address from previous access cycle. |
| 15-0 | DO[15:0] | Readback data requested on previous access cycle. |

Copyright © 2018, Texas Instruments Incorporated

#### 10.5.1.1 Streaming Mode Operation

Since updating the eight channels data registers requires a large amount of data to be passed to the device, the device supports streaming mode. In streaming mode the DAC data registers can be written to the device without providing an instruction command for each data register. Streaming mode is enabled by setting the STREN bit. Once enabled the streaming operation is implemented by holding the $\overline{CS}$ active and continuing to shift new data into the device.

The instruction cycle includes the starting address. The device starts writing to this address and automatically increments the address as long as $\overline{CS}$ is asserted. If the last DAC data register address has been reached and $\overline{CS}$ is still asserted, the additional data is ignored by the device.

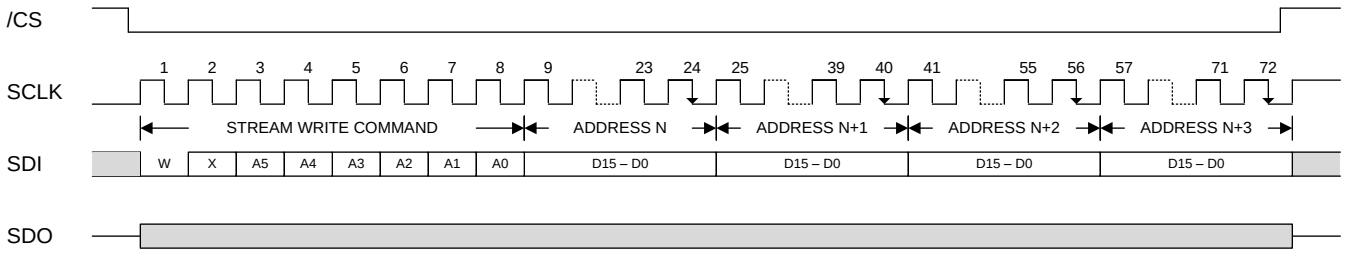



**図 50. Serial Interface Streaming Write Cycle**

### 10.5.2 Daisy-Chain Operation

For systems that contain more than one DACx1408 devices, the SDO pin can be used to daisy-chain them together. The SDO pin must be enabled by setting the SDO-EN bit before initiating the daisy-chain operation. Daisy-chain operation is useful in reducing the number of serial interface lines.

The first falling edge on the $\overline{CS}$ pin starts the operation cycle. If more than 24 SCLK pulses are applied while the $\overline{CS}$ pin is kept low, the data ripples out of the shift register and is clocked out on the SDO pin either on the falling edge or rising edge of SCLK according to the FSDO bit. By connecting the SDO output of the first device to the SDI input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. As a result the total number of clock cycles must be equal to 24 × N, where N is the total number of DACx1408 devices in the daisy chain. When the serial transfer to all devices is complete the $\overline{CS}$ signal is taken high. This action transfers the data from the SPI shift registers to the internal registers of each device in the daisy chain and prevents any further data from being clocked into the input shift register. Daisy-chain operation is not supported while in streaming mode.

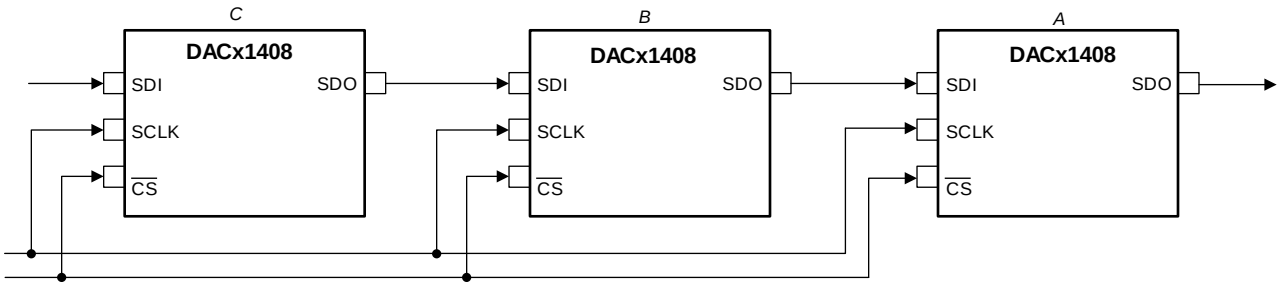



**図 51. Daisy-Chain Layout**


Copyright © 2018, Texas Instruments Incorporated

### 10.5.3 Frame Error Checking

If the DACx1408 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature is enabled by setting the CRC-EN bit.

The error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, 100000111). When error checking is enabled, the serial interface access cycle width is 32 bits. The normal 24-bit SPI data is appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. In all serial interface readback operations the CRC polynomial is output on the SDO pin as part of the 32-bit cycle.

**表 4. Error Checking Serial Interface Access Cycle**

| BIT | FIELD | DESCRIPTION |
|---|---|---|
| 31 | RW | Identifies the communication as a read or write command to the address register. R/W = 0 sets a write operation. R/W = 1 sets a read operation. |
| 30 | CRC-ERROR | Reserved bit. Set to zero. |
| 29-24 | A[5:0] | Register address. Specifies the register to be accessed during the read or write operation. |
| 23-8 | DI[15:0] | Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[5:0]. If a read command, the data cycle bits are don't care values. |
| 7-0 | CRC | 8-bit CRC polynomial. |

The DACx1408 decodes the 32-bit access cycle to compute the CRC remainder on CS rising edges. If no error exists, the CRC remainder is zero and data are accepted by the device.

A write operation failing the CRC check causes the data to be ignored by the device. After the write command, a second access cycle can be issued to determine the error checking results (CRC-ERROR bit) on the SDO pin.

If there is a CRC error, the CRC-ALM bit of the status register is set to 1. The $\overline{\text{ALMOUT}}$ pin can be configured to monitor a CRC error by setting the CRCALM-EN bit.

**表 5. Write Operation Error Checking Cycle**

| BIT | FIELD | DESCRIPTION |
|---|---|---|
| 31 | RW | Echo RW from previous access cycle (RW = 0). |
| 30 | CRC-ERROR | Returns a 1 when a CRC error is detected, 0 otherwise. |
| 29-24 | A[5:0] | Echo address from previous access cycle. |
| 23-8 | DO[15:0] | Echo data from previous access cycle. |
| 7-0 | CRC | Calculated CRC value of bits 31:8. |

A read operation must be followed by a second access cycle to get the requested data on the SDO pin. The error check result (CRC-ERROR bit) from the read command is output on the SDO pin.

As in the case of a write operation failing the CRC check, the CRC-ALM bit of the status register is set to 1 and the $\overline{\text{ALMOUT}}$ pin, if configured for CRC alerts, is set low.

**表 6. Read Operation Error Checking Cycle**

| BIT | FIELD | DESCRIPTION |
|---|---|---|
| 31 | RW | Echo RW from previous access cycle (RW = 1). |
| 30 | CRC-ERROR | Returns a 1 when a CRC error is detected, 0 otherwise. |
| 29-24 | A[5:0] | Echo address from previous access cycle. |
| 23-8 | DO[15:0] | Echo data from previous access cycle. |
| 7-0 | CRC | Calculated CRC value of bits 31:8. |

Copyright © 2018, Texas Instruments Incorporated

## 10.6 Register Maps

表 7 lists the memory-mapped registers for the device. All register offset addresses not listed in 表 7 should be considered as reserved locations and the register contents should not be modified.

**表 7. DACx1408 Registers**

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| 00h | NOP | NOP Register | Go |
| 01h | DEVICEID | Device ID Register | Go |
| 02h | STATUS | Status Register | Go |
| 03h | SPICONFIG | SPI Configuration Register | Go |
| 04h | GENCONFIG | General Configuration Register | Go |
| 05h | BRDCONFIG | Broadcast Configuration Register | Go |
| 06h | SYNCCONFIG | Sync Configuration Register | Go |
| 07h | TOGGCONFIG0 | DAC[7:4] Toggle Configuration Register | Go |
| 08h | TOGGCONFIG1 | DAC[3:0] Toggle Configuration Register | Go |
| 09h | DACPWDWN | DAC Power-Down Register | Go |
| 0Bh | DACRANGE0 | DAC[7:4] Range Register | Go |
| 0Ch | DACRANGE1 | DAC[3:0] Range Register | Go |
| 0Eh | TRIGGER | Trigger Register | Go |
| 0Fh | BRDCAST | Broadcast Data Register | Go |
| 14h | DAC0 | DAC0 Data Register | Go |
| 15h | DAC1 | DAC1 Data Register | Go |
| 16h | DAC2 | DAC2 Data Register | Go |
| 17h | DAC3 | DAC3 Data Register | Go |
| 18h | DAC4 | DAC4 Data Register | Go |
| 19h | DAC5 | DAC5 Data Register | Go |
| 1Ah | DAC6 | DAC6 Data Register | Go |
| 1Bh | DAC7 | DAC7 Data Register | Go |
| 21h | OFFSET0 | DAC[6-7;4-5] Differential Offset Register | Go |
| 22h | OFFSET1 | DAC[2-3;0-1] Differential Offset Register | Go |


Copyright © 2018, Texas Instruments Incorporated

Complex bit access types are encoded to fit into small table cells. 表 8 shows the codes that are used for access types in this section.

**表 8. Access Type Codes**

| Access Type | Code | Description |
|---|---|---|
| **Read Type** | | |
| R | R | Read |
| **Write Type** | | |
| W | W | Write |
| **Reset or Default Value** | | |
| *-n* | | Value after reset or the default value |
| **Register Array Variables** | | |
| i,j,k,l,m,n | | When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula. |
| y | | When this variable is used in a register name, an offset, or an address it refers to the value of a register array. |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.1 NOP Register (Offset = 00h) [reset = 0000h]

NOP is shown in 図 52 and described in 表 9.

Return to Summary Table.

**図 52. NOP Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NOP | | | | | | | | | | | | | | | |
| W-0h | | | | | | | | | | | | | | | |

**表 9. NOP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | NOP | W | 0h | No operation. Write 0000h for proper no-operation command. |

### 10.6.2 DEVICEID Register (Offset = 01h) [reset = ----h]

DEVICEID is shown in 図 53 and described in 表 10.

Return to Summary Table.

**図 53. DEVICEID Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DEVICEID | | | | | | | |
| R----h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DEVICEID | | | | | | VERSIONID | |
| R----h | | | | | | R-0h | |

**表 10. DEVICEID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-2 | DEVICEID | R | ---h | Device ID<br>DAC81408: 298h<br>DAC71408: 288h<br>DAC61408: 248h |
| 1-0 | VERSIONID | R | 0h | Version ID. Subject to change. |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.3 STATUS Register (Offset = 02h) [reset = 0000h]

STATUS is shown in 図 54 and described in 表 11.

Return to Summary Table.

**図 54. STATUS Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CRC-ALM | DAC-BUSY | TEMP-ALM |
| R-0h | | | | | R-0h | R-0h | R-0h |

**表 11. STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-3 | RESERVED | R | 0h | This bit is reserved. |
| 2 | CRC-ALM | R | 0h | CRC-ALM = 1 indicates a CRC error. |
| 1 | DAC-BUSY | R | 0h | DAC-BUSY = 1 indicates DAC registers are not ready for updates. |
| 0 | TEMP-ALM | R | 0h | TEMP-ALM = 1 indicates die temperature is over +140°C. A thermal alarm event forces the DAC outputs to go into power-down mode. |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.4 SPICONFIG Register (Offset = 03h) [reset = 0A24h]

SPICONFIG is shown in 図 55 and described in 表 12.

Return to Summary Table.

**図 55. SPICONFIG Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | TEMPALM-EN | DACBUSY-EN | CRCALM-EN | RESERVED |
| R-0h | | | | R/W-1h | R/W-0h | R/W-1h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | SOFTTOGGLE-EN | DEV-PWDWN | CRC-EN | STR-EN | SDO-EN | FSDO | RESERVED |
| R-1h | R/W-0h | R/W-1h | R/W-0h | R/W-0h | R/W-1h | R/W-0h | R-0h |

**表 12. SPICONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-12 | RESERVED | R | 0h | This bit is reserved. |
| 11 | TEMPALM-EN | R/W | 1h | When set to 1 a thermal alarm triggers the $\overline{\text{ALMOUT}}$ pin. |
| 10 | DACBUSY-EN | R/W | 0h | When set to 1 the $\overline{\text{ALMOUT}}$ pin is set between DAC output updates. Contrary to other alarm events, this alarm resets automatically. |
| 9 | CRCALM-EN | R/W | 1h | When set to 1 a CRC error triggers the $\overline{\text{ALMOUT}}$ pin. |
| 8 | RESERVED | R | 0h | This bit is reserved. |
| 7 | RESERVED | R | 1h | This bit is reserved. |
| 6 | SOFTTOGGLE-EN | R/W | 0h | When set to 1 enables soft toggle operation. |
| 5 | DEV-PWDWN | R/W | 1h | DEV-PWDWN = 1 sets the device in power-down mode<br>DEV-PWDWN = 0 sets the device in active mode |
| 4 | CRC-EN | R/W | 0h | When set to 1 frame error checking is enabled. |
| 3 | STR-EN | R/W | 0h | When set to 1 streaming mode operation is enabled. |
| 2 | SDO-EN | R/W | 1h | When set to 1 the SDO pin is operational. |
| 1 | FSDO | R/W | 0h | Fast SDO bit (half-cycle speedup). When 0, SDO updates during SCLK rising edges. When 1, SDO updates during SCLK falling edges. |
| 0 | RESERVED | R | 0h | This bit is reserved. |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.5 GENCONFIG Register (Offset = 04h) [reset = 7F00h]

GENCONFIG is shown in 図 56 and described in 表 13.

Return to Summary Table.

**図 56. GENCONFIG Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | REF-PWDWN | RESERVED | | | | | |
| R-0h | R/W-1h | R-1h | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | RESERVED | DAC-6-7-DIFF-EN | DAC-4-5-DIFF-EN | DAC-2-3-DIFF-EN | DAC-0-1-DIFF-EN | RESERVED | RESERVED |
| R-0h | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h |

**表 13. GENCONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESERVED | R | 0h | This bit is reserved. |
| 14 | REF-PWDWN | R/W | 1h | REF-PWDWN = 1 powers down the internal reference<br>REF-PWDWN = 0 activates the internal reference |
| 13-8 | RESERVED | R | 1h | This bit is reserved. |
| 7 | RESERVED | R | 0h | This bit is reserved. |
| 6 | RESERVED | R | 0h | This bit is reserved. |
| 5 | DAC-6-7-DIFF-EN | R/W | 0h | When set to 1 the corresponding DAC pair is set to operate in differential mode. The DAC data registers must be rewritten after enabling or disabling differential operation. |
| 4 | DAC-4-5-DIFF-EN | R/W | 0h | |
| 3 | DAC-2-3-DIFF-EN | R/W | 0h | |
| 2 | DAC-0-1-DIFF-EN | R/W | 0h | |
| 1 | RESERVED | R | 0h | This bit is reserved. |
| 0 | RESERVED | R | 0h | This bit is reserved. |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.6 BRDCONFIG Register (Offset = 05h) [reset = FFFFh]

BRDCONFIG is shown in 図 57 and described in 表 14.

Return to Summary Table.

**図 57. BRDCONFIG Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | RESERVED | RESERVED | RESERVED | DAC7-BRDCAST-EN | DAC6-BRDCAST-EN | DAC5-BRDCAST-EN | DAC4-BRDCAST-EN |
| R-1h | R-1h | R-1h | R-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAC3-BRDCAST-EN | DAC2-BRDCAST-EN | DAC1-BRDCAST-EN | DAC0-BRDCAST-EN | RESERVED | RESERVED | RESERVED | RESERVED |
| R/W-1h | R/W-0h | R/W-0h | R/W-0h | R-1h | R-1h | R-1h | R-1h |

**表 14. BRDCONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESERVED | R | 1h | This bit is reserved. |
| 14 | RESERVED | R | 1h | This bit is reserved. |
| 13 | RESERVED | R | 1h | This bit is reserved. |
| 12 | RESERVED | R | 1h | This bit is reserved. |
| 11 | DAC7-BRDCAST-EN | R/W | 1h | When set to 1 the corresponding DAC is set to update its output to the value set in the BRDCAST register. All DAC channels must be configured in single-ended mode for broadcast operation. If one or more outputs are configured in differential mode the broadcast mode is ignored.<br>When cleared to 0 the corresponding DAC output remains unaffected by a BRDCAST command. |
| 10 | DAC6-BRDCAST-EN | R/W | 1h | |
| 9 | DAC5-BRDCAST-EN | R/W | 1h | |
| 8 | DAC4-BRDCAST-EN | R/W | 1h | |
| 7 | DAC3-BRDCAST-EN | R/W | 1h | |
| 6 | DAC2-BRDCAST-EN | R/W | 1h | |
| 5 | DAC1-BRDCAST-EN | R/W | 1h | |
| 4 | DAC0-BRDCAST-EN | R/W | 1h | |
| 3 | RESERVED | R | 1h | This bit is reserved. |
| 2 | RESERVED | R | 1h | This bit is reserved. |
| 1 | RESERVED | R | 1h | This bit is reserved. |
| 0 | RESERVED | R | 1h | This bit is reserved. |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.7 SYNCCONFIG Register (Offset = 06h) [reset = 0000h]

SYNCCONFIG is shown in 図 58 and described in 表 15.

Return to Summary Table.

**図 58. SYNCCONFIG Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | RESERVED | RESERVED | RESERVED | DAC7-SYNC-EN | DAC6-SYNC-EN | DAC5-SYNC-EN | DAC4-SYNC-EN |
| R-0h | R-0h | R-0h | R-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAC3-SYNC-EN | DAC2-SYNC-EN | DAC1-SYNC-EN | DAC0-SYNC-EN | RESERVED | RESERVED | RESERVED | RESERVED |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R-0h | R-0h | R-0h | R-0h |

**表 15. SYNCCONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESERVED | R | 0h | This bit is reserved. |
| 14 | RESERVED | R | 0h | This bit is reserved. |
| 13 | RESERVED | R | 0h | This bit is reserved. |
| 12 | RESERVED | R | 0h | This bit is reserved. |
| 11 | DAC7-SYNC-EN | R/W | 0h | When set to 1 the corresponding DAC output is set to update in response to an LDAC trigger (synchronous mode).<br>When cleared to 0 the corresponding DAC output is set to update immediately (asynchronous mode). |
| 10 | DAC6-SYNC-EN | R/W | 0h | |
| 9 | DAC5-SYNC-EN | R/W | 0h | |
| 8 | DAC4-SYNC-EN | R/W | 0h | |
| 7 | DAC3-SYNC-EN | R/W | 0h | |
| 6 | DAC2-SYNC-EN | R/W | 0h | |
| 5 | DAC1-SYNC-EN | R/W | 0h | |
| 4 | DAC0-SYNC-EN | R/W | 0h | |
| 3 | RESERVED | R | 0h | This bit is reserved. |
| 2 | RESERVED | R | 0h | This bit is reserved. |
| 1 | RESERVED | R | 0h | This bit is reserved. |
| 0 | RESERVED | R | 0h | This bit is reserved. |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.8 TOGGCONFIG0 Register (Offset = 07h) [reset = 0000h]

TOGGCONFIG0 is shown in 図 59 and described in 表 16.

Return to Summary Table.

**図 59. TOGGCONFIG0 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | RESERVED | | RESERVED | | RESERVED | |
| R-0h | | R-0h | | R-0h | | R-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAC7-AB-TOGG-EN | | DAC6-AB-TOGG-EN | | DAC5-AB-TOGG-EN | | DAC4-AB-TOGG-EN | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

**表 16. TOGGCONFIG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | RESERVED | R | 0h | This bit is reserved. |
| 13-12 | RESERVED | R | 0h | This bit is reserved. |
| 11-10 | RESERVED | R | 0h | This bit is reserved. |
| 9-8 | RESERVED | R | 0h | This bit is reserved. |
| 7-6 | DAC7-AB-TOGG-EN | R/W | 0h | Enables toggle mode operation and configures the toggle pin or soft toggle bit:<br>0h = Toggle mode disabled<br>1h = Toggle mode enabled: TOGGLE0<br>2h = Toggle mode enabled: TOGGLE1<br>3h = Toggle mode enabled: TOGGLE2 |
| 5-4 | DAC6-AB-TOGG-EN | R/W | 0h | |
| 3-2 | DAC5-AB-TOGG-EN | R/W | 0h | |
| 1-0 | DAC4-AB-TOGG-EN | R/W | 0h | |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.9 TOGGCONFIG1 Register (Offset = 08h) [reset = 0000h]

TOGGCONFIG1 is shown in 図 60 and described in 表 17.

Return to Summary Table.

**図 60. TOGGCONFIG1 Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DAC3-AB-TOGG-EN | | DAC2-AB-TOGG-EN | | DAC1-AB-TOGG-EN | | DAC0-AB-TOGG-EN | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | RESERVED | | RESERVED | | RESERVED | |
| R-0h | | R-0h | | R-0h | | R-0h | |

**表 17. TOGGCONFIG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-14 | DAC3-AB-TOGG-EN | R/W | 0h | Enables toggle mode operation and configures the toggle pin or soft toggle bit:<br>0h = Toggle mode disabled<br>1h = Toggle mode enabled: TOGGLE0<br>2h = Toggle mode enabled: TOGGLE1<br>3h = Toggle mode enabled: TOGGLE2 |
| 13-12 | DAC2-AB-TOGG-EN | R/W | 0h | |
| 11-10 | DAC1-AB-TOGG-EN | R/W | 0h | |
| 9-8 | DAC0-AB-TOGG-EN | R/W | 0h | |
| 7-6 | RESERVED | R | 0h | This bit is reserved. |
| 5-4 | RESERVED | R | 0h | This bit is reserved. |
| 3-2 | RESERVED | R | 0h | This bit is reserved. |
| 1-0 | RESERVED | R | 0h | This bit is reserved. |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.10 DACPWDWN Register (Offset = 09h) [reset = FFFFh]

DACPWDWN is shown in 図 61 and described in 表 18.

Return to Summary Table.

**図 61. DACPWDWN Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | RESERVED | RESERVED | RESERVED | DAC7-PWDWN | DAC6-PWDWN | DAC5-PWDWN | DAC4-PWDWN |
| R-1h | R-1h | R-1h | R-1h | R/W-1h | R/W-1h | R/W-1h | R/W-1h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DAC3-PWDWN | DAC2-PWDWN | DAC1-PWDWN | DAC0-PWDWN | RESERVED | RESERVED | RESERVED | RESERVED |
| R/W-1h | R/W-1h | R/W-1h | R/W-1h | R-1h | R-1h | R-1h | R-1h |

**表 18. DACPWDWN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15 | RESERVED | R | 1h | This bit is reserved. |
| 14 | RESERVED | R | 1h | This bit is reserved. |
| 13 | RESERVED | R | 1h | This bit is reserved. |
| 12 | RESERVED | R | 1h | This bit is reserved. |
| 11 | DAC7-PWDWN | R/W | 1h | When set to 1 the corresponding DAC is in power-down mode and its output is connected to GND through a 10-kΩ internal resistor. |
| 10 | DAC6-PWDWN | R/W | 1h | |
| 9 | DAC5-PWDWN | R/W | 1h | |
| 8 | DAC4-PWDWN | R/W | 1h | |
| 7 | DAC3-PWDWN | R/W | 1h | |
| 6 | DAC2-PWDWN | R/W | 1h | |
| 5 | DAC1-PWDWN | R/W | 1h | |
| 4 | DAC0-PWDWN | R/W | 1h | |
| 3 | RESERVED | R | 1h | This bit is reserved. |
| 2 | RESERVED | R | 1h | This bit is reserved. |
| 1 | RESERVED | R | 1h | This bit is reserved. |
| 0 | RESERVED | R | 1h | This bit is reserved. |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.11 DACRANGEn Register (Offset = 0Bh - 0Ch) [reset = 0000h]

DACRANGEn is shown in 図 62 and described in 表 19.

Return to Summary Table.

**図 62. DACRANGEn Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| DACa-RANGE[3:0] | | | | DACb-RANGE[3:0] | | | |
| W-0h | | | | W-0h | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DACc-RANGE[3:0] | | | | DACd-RANGE[3:0] | | | |
| W-0h | | | | W-0h | | | |

**表 19. DACRANGEn Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-12 | DACa-RANGE[3:0] | W | 0h | Sets the output range for the corresponding DAC.<br>0000 = 0 to 5 V<br>0001 = 0 to 10 V<br>0010 = 0 to 20 V<br>0100 = 0 to 40 V<br>1001 = -5 V to +5 V<br>1010 = -10 V to +10 V<br>1100 = -20 V to +20 V<br>1110 = -2.5 V to +2.5 V<br>All others: invalid<br>The two outputs of a differential DAC pair must be configured to the same output range prior to setting them up as a differential pair.<br>a: 7 or 3; b: 6 or 2; c: 5 or 1; d: 4 or 0 |
| 11-8 | DACb-RANGE[3:0] | W | 0h | |
| 7-4 | DACc-RANGE[3:0] | W | 0h | |
| 3-0 | DACd-RANGE[3:0] | W | 0h | |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.12 TRIGGER Register (Offset = 0Eh) [reset = 0000h]

TRIGGER is shown in 図 63 and described in 表 20.

Return to Summary Table.

**図 63. TRIGGER Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | ALM-RESET |
| W-0h | | | | | | | W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AB-TOG2 | AB-TOG1 | AB-TOG0 | LDAC | SOFT-RESET[3:0] | | | |
| W-0h | W-0h | W-0h | W-0h | W-0h | | | |

**表 20. TRIGGER Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-9 | RESERVED | W | 0h | This bit is reserved |
| 8 | ALM-RESET | W | 0h | Set this bit to 1 to clear an alarm event. Not applicable for a DAC-BUSY alarm event. |
| 7 | AB-TOG2 | W | 0h | If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 2 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A. |
| 6 | AB-TOG1 | W | 0h | If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 1 in the TOGGCONFIG register. Set to 1 to updated to Register B and clear to 0 for Register A. |
| 5 | AB-TOG0 | W | 0h | If soft toggle is enabled set, this bit controls the toggle between values for those DACs that have been set in toggle mode 0 in the TOGGCONFIG register. Set to 1 to update to Register B and clear to 0 for Register A. |
| 4 | LDAC | W | 0h | Set this bit to 1 to synchronously load those DACs who have been set in synchronous mode in the SYNCCONFIG register. |
| 3-0 | SOFT-RESET[3:0] | W | 0h | When set to the reserved code 1010 resets the device to its default state. |


Copyright © 2018, Texas Instruments Incorporated

### 10.6.13 BRDCAST Register (Offset = 0Fh) [reset = 0000h]

BRDCAST is shown in 図 64 and described in 表 21.

Return to Summary Table.

**図 64. BRDCAST Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BRDCAST-DATA[15:0] | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

**表 21. BRDCAST Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | BRDCAST-DATA[15:0] | R/W | 0h | Writing to the BRDCAST register forces those DAC channels that have been set to broadcast in the BRDCONFIG register to update its active register data to the BRDCAST-DATA one.<br>Data is MSB aligned in straight binary format and follows the format below:<br>DAC81408: { DATA[15:0] }<br>DAC71408: { DATA[13:0], x, x }<br>DAC61408: { DATA[11:0], x, x, x, x}<br>x – Don 't care bits |

### 10.6.14 DACn Register (Offset = 14h - 1Bh) [reset = 0000h]

DACn is shown in 図 65 and described in 表 22.

Return to Summary Table.

**図 65. DACn Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DACn-DATA[15:0] | | | | | | | | | | | | | | | |
| R/W-0h | | | | | | | | | | | | | | | |

**表 22. DACn Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-0 | DACn-DATA[15:0] | R/W | 0h | Stores the 16-, 14- or 12-bit data to be loaded to DACn in MSB aligned straight binary format. In differential DAC mode data is loaded into the lowest-valued DAC in the DAC pair (in pair DAC 01, data is loaded into DAC0 and writes to DAC1 are ignored).<br>Data follows the format below:<br>DAC81408: { DATA[15:0] }<br>DAC71408: { DATA[13:0], x, x }<br>DAC61408: { DATA[11:0], x, x, x, x}<br>x – Don 't care bits |

Copyright © 2018, Texas Instruments Incorporated

### 10.6.15 OFFSETn Register (Offset = 21h - 22h) [reset = 0000h]

OFFSETn is shown in 図 66 and described in 表 23.

Return to Summary Table.

**図 66. OFFSETn Register**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| OFFSETab[7:0] | | | | | | | |
| R/W-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| OFFSETcd[7:0] | | | | | | | |
| R/W-0h | | | | | | | |

**表 23. OFFSETn Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 15-8 | OFFSETab[7:0] | R/W | 0h | Provides offset adjustment to DACy in the differential DACx-y pair in two 's complement format.<br>Data follows the format below:<br>• DAC81408:<br>– Format: { OFFSET[7:0] }<br>– Range: -128 LSB to +127 LSB<br>• DAC71408:<br>– Format: { OFFSET[5:0], x, x }<br>– Range: -32 LSB to +31 LSB<br>• DAC61408:<br>– Format: { OFFSET[3:0], x, x, x, x}<br>– Range: -8 LSB to +7 LSB<br>x – Don 't care bits<br>The differential DAC data register must be rewritten after updating the offset register.<br>ab: 6-7 or 2-3; cd: 4-5 or 0-1 |
| 7-0 | OFFSETcd[7:0] | R/W | 0h | |


Copyright © 2018, Texas Instruments Incorporated

# 11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 11.1 Application Information

The DACx1408 family provides 8-channel high-voltage and high-current output in both single-ended and differential configurations. The outputs can be configured to multiple ranges and square waves can be generated using the toggle modes. This makes the DAC family suitable for Automatic Test Equipment (ATE) and servo control applications. In addition to these features, the low power-on glitch of this DAC makes it suitable for Motor Control applications like CNC machines as well.

## 11.2 Typical Application

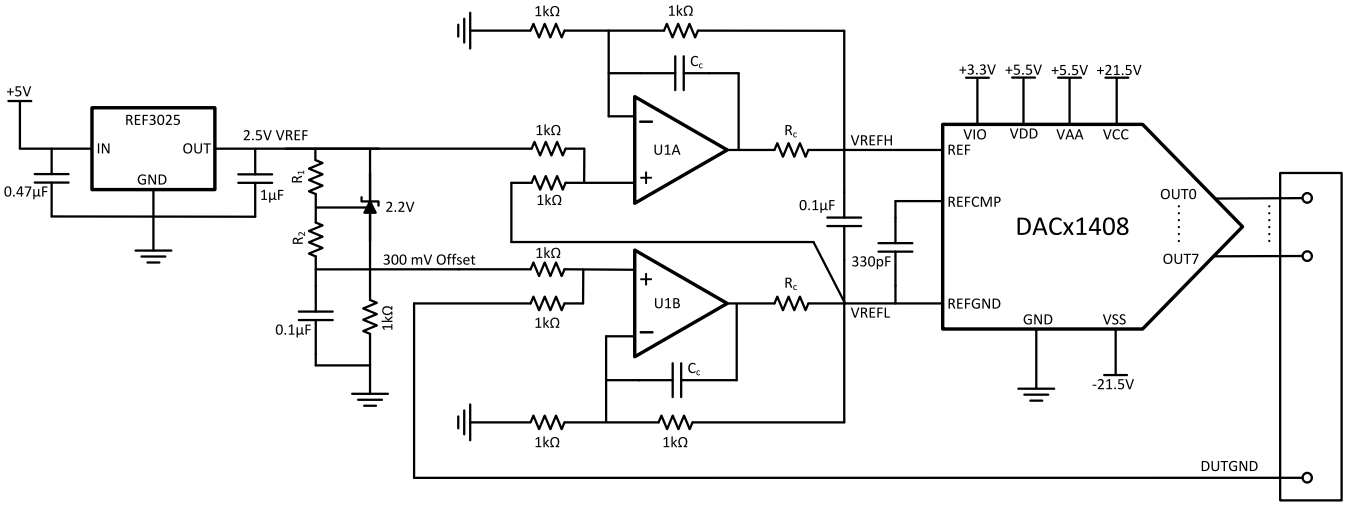



**図 67. Schematic for Remote Ground Tracking**

### 11.2.1 Design Requirements

In ATE and Motor Control applications, typically the systems are designed modular wherein the control module is located spatially away from the Device Under Test (DUT) module. Such a scheme allows ground potentials across modules to vary due to the impedance of the interconnects. This ground potential variation, in turn introduces inaccuracies to the DAC output when measured with respect to the remote or DUT ground. 図 67 provides a method to compensate the variations in the remote ground. The ground variation in such applications is typically within ±300 mV that includes DC and 50 Hz/60 Hz mains frequency components. While the best way to handle this variation is to put opamps in level shifter configuration at each output, a low cost and low footprint solution is always preferable. The following sections focus on the latter approach.

Copyright © 2018, Texas Instruments Incorporated

## Typical Application (continued)

### 11.2.2 Detailed Design Procedure for Remote Ground Tracking

In order to make the DAC outputs follow the remote ground, the best approach is to level shift the reference input. 図 67 depicts a method wherein both the REF and REFGND inputs are level shifted with respect to DUTGND. However, as the DAC doesn't allow the REFGND to become negative compared to GND, an offset voltage of 300mV needs to be applied as shown. This method requires an external 2.5V reference and a way to generate a stable 300-mV reference. A dual opamp U1 is used to shift both REFGND and REF by (DUTGND + 300-mV offset). 表 24 provides the nodal analysis of the circuit. As evident, the DAC outputs track the DUTGND with an offset of 300mV. This offset can be easily compensated in software. Note that the absolute max values between REFGND and GND must be respected. When the absolute max values are reached, they should only be for a transient period and not for sustained amount of time.

**表 24. Nodal Analysis of the Circuit**

| DUTGND (GND±0.3V) | REFGND PIN | REF PIN | VOUT-GND AT 0V CODE | VOUT-GND AT 5V CODE | VOUT-DUTGND AT 0V CODE | VOUT-DUTGND AT 5V CODE |
|---|---|---|---|---|---|---|
| 0V | 0.3V | 2.8V | 0.3V | 5.3V | 0.3V | 5.3V |
| 0.3V | 0.6V | 3.1V | 0.6V | 5.6V | 0.3V | 5.3V |
| -0.3V | 0V | 2.5V | 0V | 5V | 0.3V | 5.3V |

#### *11.2.2.1 Generating 300mV Offset*

There is no off-the-shelf solution for generating a 300-mV offset, unfortunately. 図 67 depicts a method to generate it using discrete components. It uses LM4041 adjustable shunt regulator on high-side from the 2.5-V reference. It has a reference input pin that sets the voltage across this device. Given that $V_{Ref}$ is 1.233 V, choosing R1 = 16 kΩ and R2 = 12 kΩ the voltage $V_o$ can be calculated by superposition as 2.16 V. This will provide an offset of (2.5 V – 2.16 V) = 340 mV that will provide a safe margin from DAC ground.

#### *11.2.2.2 Amplifier Selection*

The amplifier needs to be bipolar in order to operate linearly near ground. A dual package is preferable for optimizing area. Considering these factors, TLV2442A seems to be the best option from cost and accuracy points of view. Other parts like OPA2277 can be used when higher accuracy is required.

#### *11.2.2.3 Passive Component Selection*

In order to minimize additional offset and gain error the gain resistors around the opamps need to be matched. An 8-channel resistor network can be used for better matching. $R_c$ and $C_c$ values can be chosen as 22 Ω and 1000 pF, respectively in order to compensate the pole caused by the large bypass capacitor at the opamp outputs.


Copyright © 2018, Texas Instruments Incorporated

### 11.2.3 Application Curves

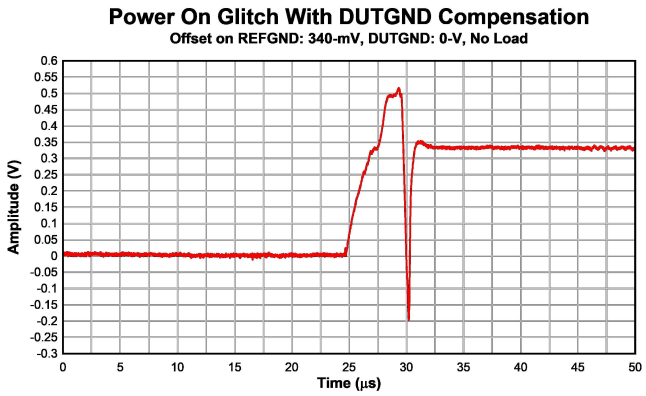



図 68. Power-On Glitch With DUTGND Compensation

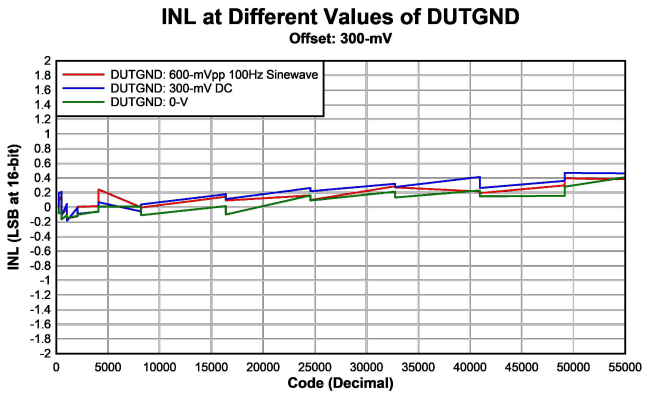



図 69. INL (Major Code) at Different Values of DUTGND

Copyright © 2018, Texas Instruments Incorporated

## 12 Power Supply Recommendations

The DACx1408 requires 5 power supply inputs: VIO, VDD, VAA, VCC and VSS. VDD and VAA should be at same level. Assuming VIO and VDD/VAA to be different, there are 4 separate power supply sources required. It is recommended to provide a 0.1-µF ceramic capacitor close to each power supply pin. Please note that VCC and VSS have 2 pins each. In addition, a 4.7-µF or 10-µF bulk capacitor is recommended for each power supply. Tantalum or aluminum types can be chosen for the bulk capacitors. There is no sequencing requirement for the power supplies. As the DAC output range is configurable, the power supply headroom should be taken care of for achieving linearity at codes close to power supply rails. When sourcing or sinking current from or to the DAC output, the heat dissipation needs to be considered. For example, a typical application of MZM bias with 25-mA load current from or to 12 channels with 2.5-V power supply headroom can create a power dissipation across the DAC of (12*2.5*25 mA) = 0.75 W. The thermal design to dissipate this much of power may involve inclusion of heat sinks in order to avoid thermal shutdown of the device.


Copyright © 2018, Texas Instruments Incorporated

# 13 Layout

## 13.1 Layout Guidelines

The pin out of DACx1408 has been designed in such a way that the analog, digital and power pins are spatially separated from each other, which makes the PCB layout simple. An example layout is shown in 図 70. As evident, every power supply pin has a 0.1-µF capacitor close to it. The layout of the analog and digital signals should be laid out away from each other or on different PCB layers. It is recommended to provide an unbroken reference plane (either ground or VIO) for the digital signals. The higher frequency signals such as SCLK and SDI should have appropriate impedance termination in order to address signal integrity.

## 13.2 Layout Example

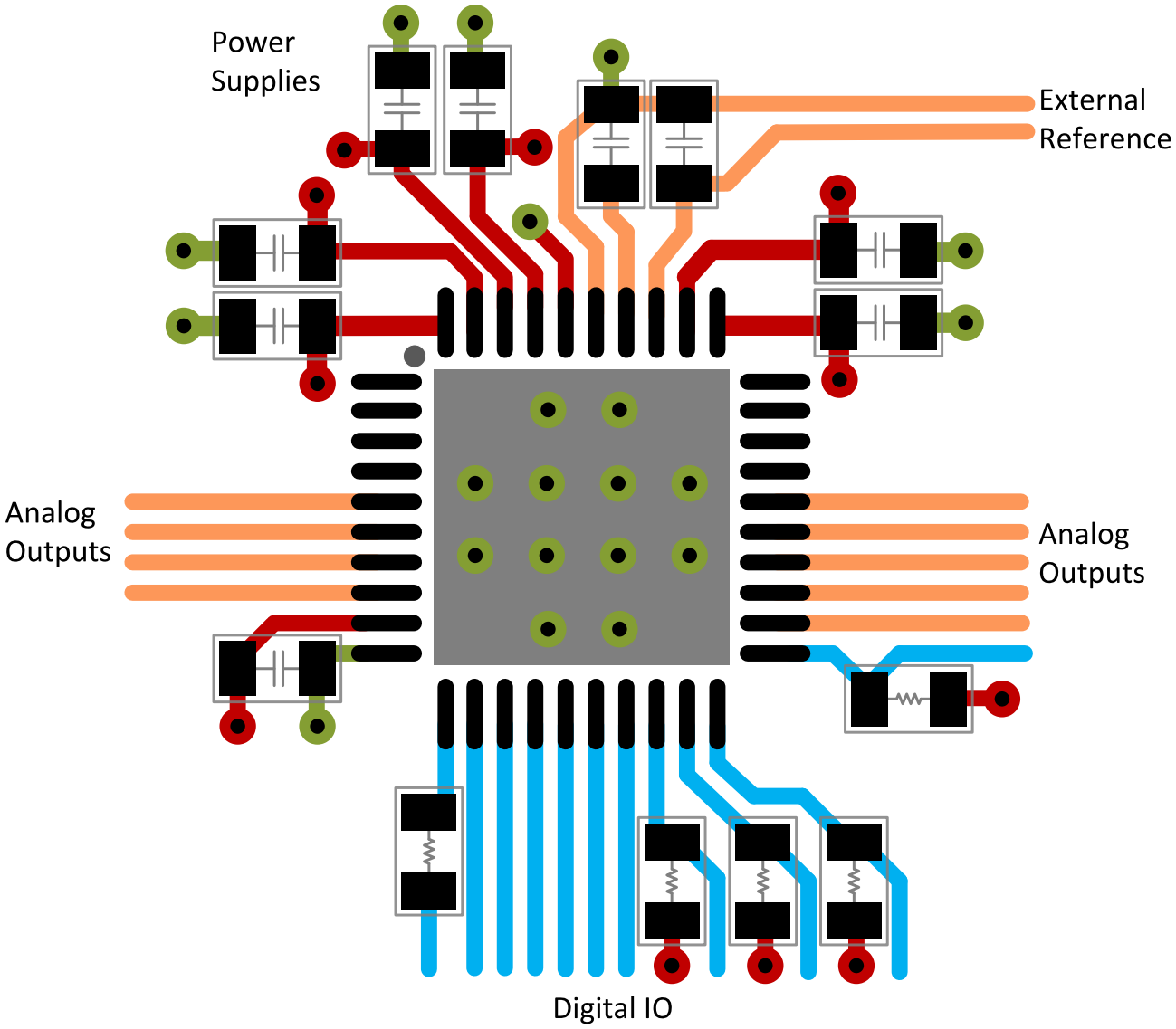



**図 70. Example Layout**

Copyright © 2018, Texas Instruments Incorporated

# 14 デバイスおよびドキュメントのサポート

## 14.1 ドキュメントのサポート

## 14.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

**表 25. 関連リンク**

| 製品 | プロダクト・フォルダ | ご注文はこちら | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|---|---|---|---|---|---|
| DAC81408 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| DAC71408 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| DAC61408 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

## 14.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 14.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™オンライン・コミュニティ** ***TIのE2E ( Engineer-to-Engineer ) コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

**設計サポート** ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

## 14.5 商標

E2E is a trademark of Texas Instruments.

## 14.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。


Copyright © 2018, Texas Instruments Incorporated

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| DAC61408RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC61408 |
| DAC61408RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC61408 |
| DAC61408RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC61408 |
| DAC61408RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC61408 |
| DAC71408RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC71408 |
| DAC71408RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC71408 |
| DAC71408RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC71408 |
| DAC71408RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC71408 |
| DAC81408RHAR | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC81408 |
| DAC81408RHAR.A | Active | Production | VQFN (RHA) \| 40 | 2500 \| LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC81408 |
| DAC81408RHAT | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC81408 |
| DAC81408RHAT.A | Active | Production | VQFN (RHA) \| 40 | 250 \| SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | DAC81408 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# GENERIC PACKAGE VIEW

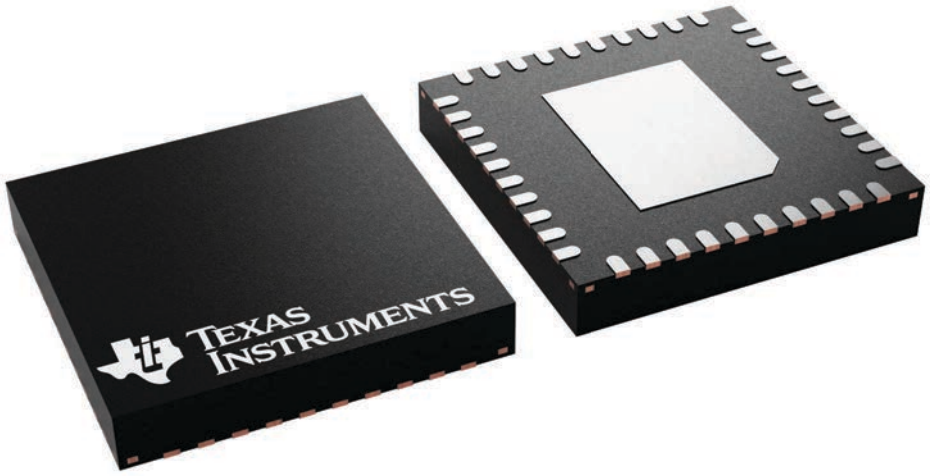
## RHA 40

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



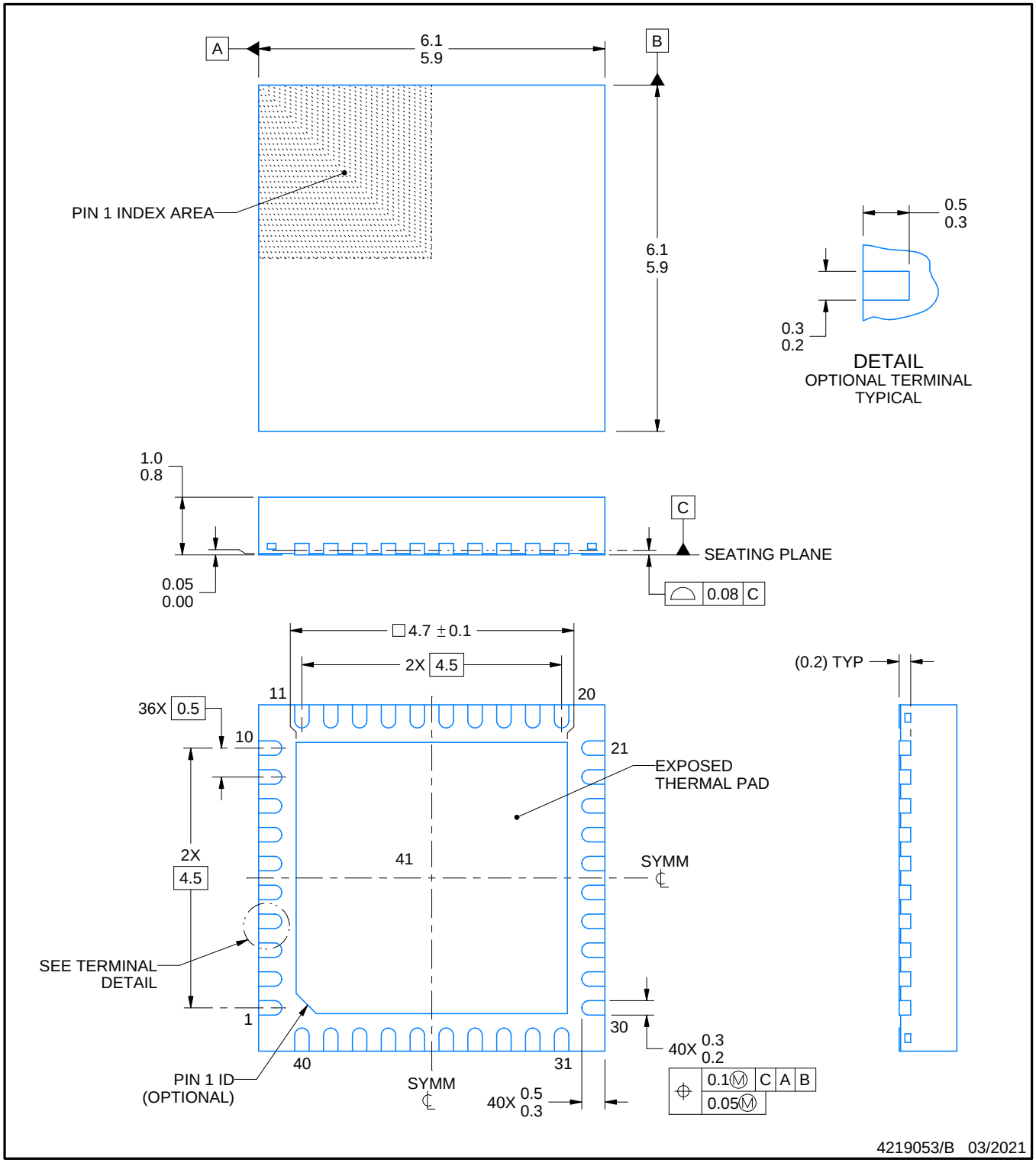

4225870/A

# RHA0040C

# PACKAGE OUTLINE

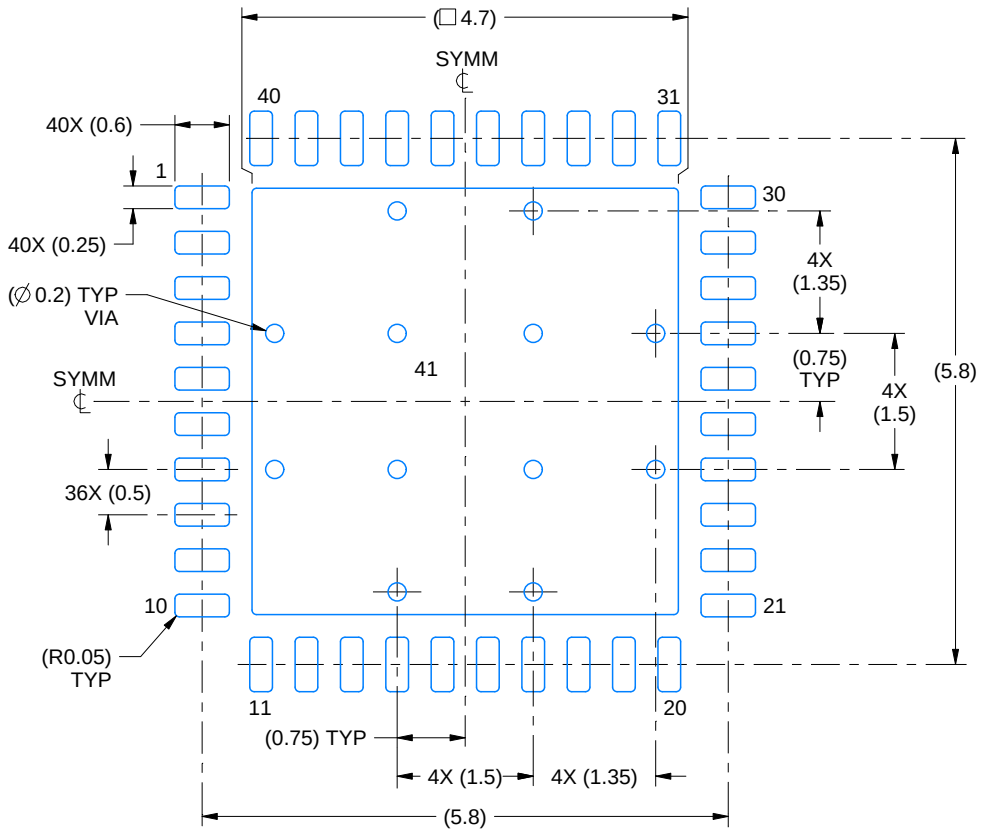
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

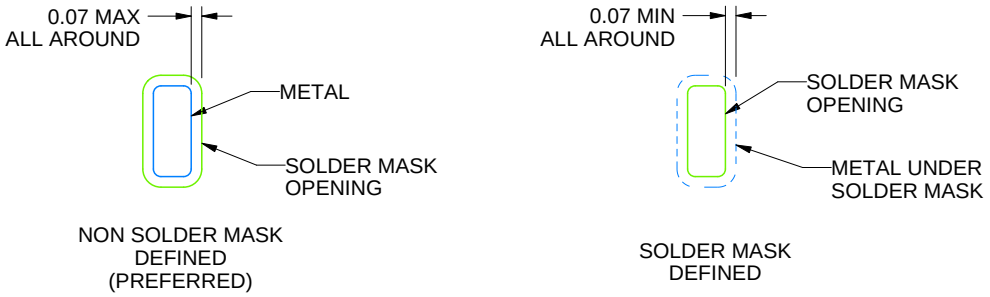



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
SCALE:12X

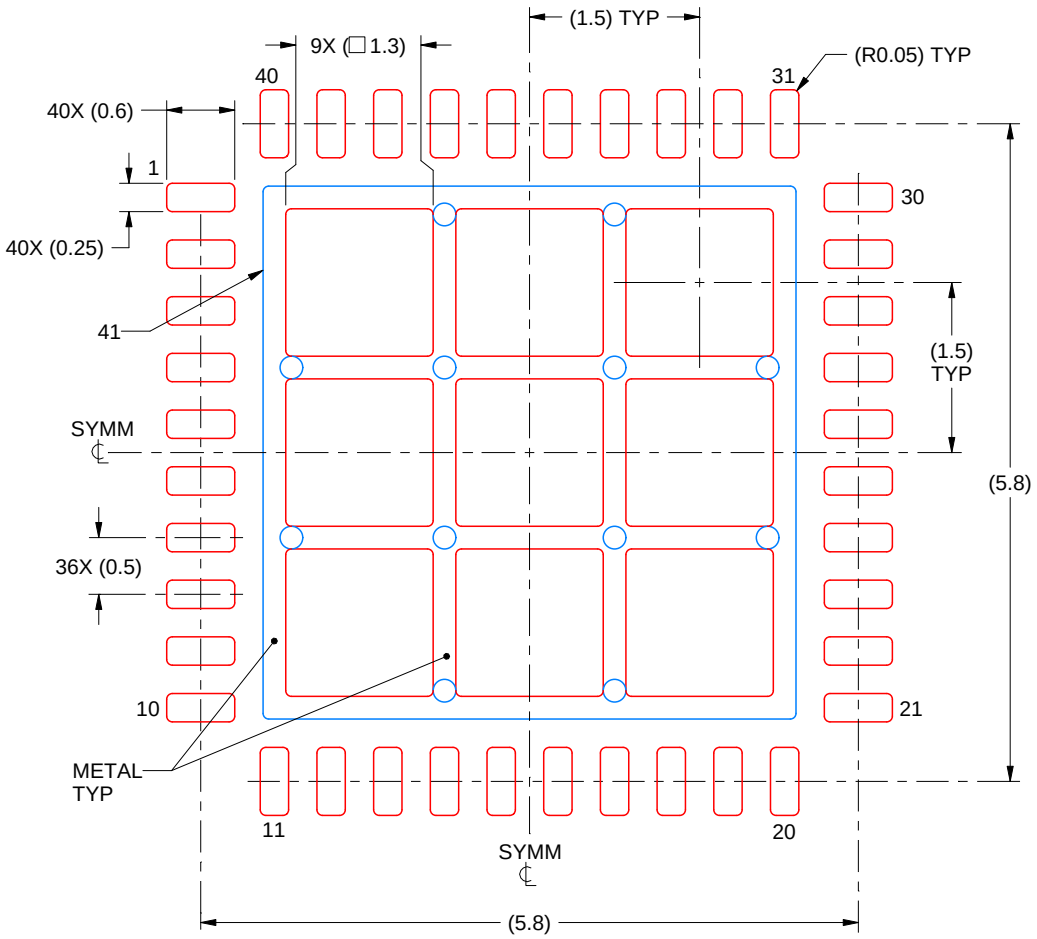



SOLDER MASK DETAILS

4219053/B 03/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 41:
69% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

4219053/B 03/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月