TEXAS INSTRUMENTS
DAC7760, DAC8760
JAJSEF2D – JUNE 2013 – REVISED DECEMBER 2021

DACx760 シングル・チャネル、12 および 16 ビット、プログラム可能な電流および電圧出力、4mA～20mA 電流ループ・アプリケーション向け D/A コンバータ

1 特長

- 電流出力:4mA～20mA、0mA～20mA、0mA～24mA
- 電圧出力:
  - 0V～5V、0V～10V、±5V、±10V
  - 0V～5.5V、0V～11V、±5.5V、±11V (10%のオーバーレンジ)
- 総合未調整誤差 (TUE):±0.1% FSR (最大値)
- DNL:±1 LSB (最大値)
- 電圧と電流を同時に出力
- 5V 基準電圧 (10ppm/℃、最大値) を内蔵
- 4.6V 電源出力を内蔵
- 高信頼性機能:
  - CRC チェックとウォッチドッグ・タイマ
  - サーマル・アラーム
  - オープン・アラーム、短絡電流制限
- 広い温度範囲:–40℃～125℃
- パッケージ:6mm × 6mm 40 ピン VQFN および 24 ピン HTSSOP

2 アプリケーション

- アナログ出力モジュール
- CPU (PLC コントローラ)
- HVAC (空調) バルブおよびアクチュエータの制御
- 流量トランスミッタ
- その他のセンサ・トランスミッタ
- アクチュエータ

3 概要

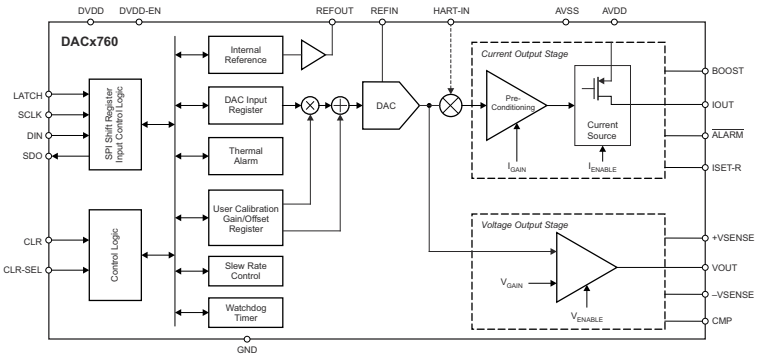
DACx760 は、高精度の完全統合型 12 ビット および 16 ビットの D/A コンバータ (DAC) で、産業用プロセス制御アプリケーションの要件を満たすよう設計されています。これらのデバイスは、4 mA～20mA、0mA～20mA、0mA～24 mA の電流出力、または、0V～5V、0V～10V、±5V、±10V、もしくは 10% のオーバーレンジ (0V～5.5V、0V～11V、±5.5V、±11V) の電圧出力にプログラムできます。電流と電圧の出力はどちらも同時に有効にでき、単一のデータ・レジスタで制御されます。

これらのデバイスは、パワーオン・リセット機能を備えており、電源オン時には既知の状態 (IOUT と VOUT はどちらもディセーブルで Hi-Z 状態) になります。CLR および CLR-SEL ピンは、電圧出力をゼロスケールまたは中間スケールに設定し、電流出力が有効な場合は範囲の下限に設定します。ゼロ・レジスタおよびゲイン・レジスタをプログラムして、最終システムの中でデバイスをデジタル的に較正できます。出力のスルー・レートも、レジスタによりプログラム可能です。電流出力に外部の HART® 信号を重ね合わせることができます。これらのデバイスは、単一の 10V~36V 電源または最大 ±18V のデュアル電源で動作します。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
DACx760	HTSSOP (24)	7.80mm × 4.40mm
	VQFN (40)	6.00mm × 6.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (January 2018) to Revision D (December 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• Changed CMP pin description in *Pin Functions* table to include 100-pF capacitance to ground	3
• Deleted *Timing Requirements: Daisy-Chain Mode* section and *Daisy-Chain Mode Timing* figure	14
• Added 100-pF capacitance to ground for larger external compensation capacitors in *Voltage Output Stage* section	29
• Deleted *Power-Supply Sequence* section	32
• Deleted daisy-chain operation content from *Watchdog Timer* section	34
• Deleted *The DACx760 Shares the SPI Bus With Other Devices* subsection from *Watchdog Timer* section	34
• Deleted daisy-chain operation content from *Frame Error Checking* section	34
• Added CRC fault software reset command of 0x96 to *Frame Error Checking* section	34
• Deleted *The DACx760 Shares the SPI Bus With Other Devices* subsection from *Frame Error Checking* section	34
• Changed duplicated 010 step-size from 0.125 to 0.25 in Table 8-3, *Slew Rate Step-Size Options*	36
• Added CRC fault reset command to Table 8-8, *Write Address Functions*	41
• Deleted *Daisy-Chain Operation* section	42
• Added *Multiple Devices on the Bus* section	42
• Changed *Command and Register Map* table to delete daisy-chain operation content and add CRC fault reset content	43
• Changed DCEN to Reserved for DB3 in Table 8-17, *Control Register*	44
• Added series resistance for supply and 100-pF capacitance from CMP to GND for Figure 9-3	50
• Added text on fast supply ramp, series resistance for power supply, and content from deleted *Power-Supply Sequence* to the *Power Supply Recommendations* section	53
• Added power supply series resistance and CMP capacitor to GND to Figure 11-1, *Layout Example*	55

Changes from Revision B (June 2016) to Revision C (January 2018)	Page
• Added first sentence to second paragraph and added last paragraph to *Frame Error Checking* section	34
• Added last paragraph to *User Calibration* section	35

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5 Device Comparison Table

RESOLUTION (Bits)	CURRENT AND VOLTAGE OUTPUT	CURRENT OUTPUT
12	DAC7760	DAC7750
16	DAC8760	DAC8750

6 Pin Configuration and Functions

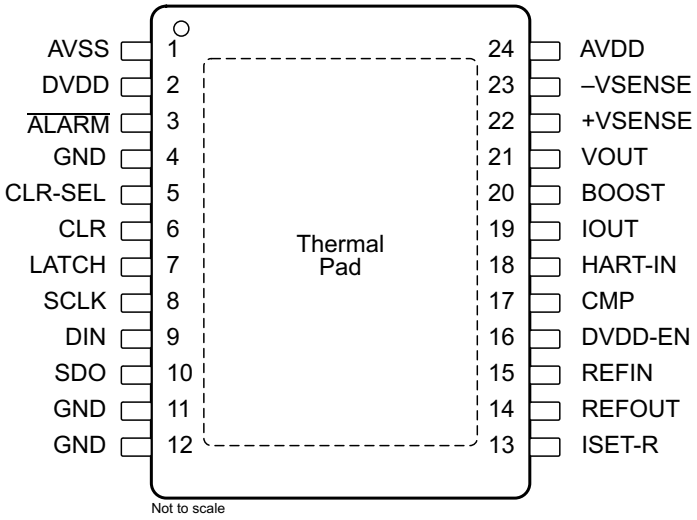


図 6-1. PWP (24-Pin HTSSOP) Package, Top View

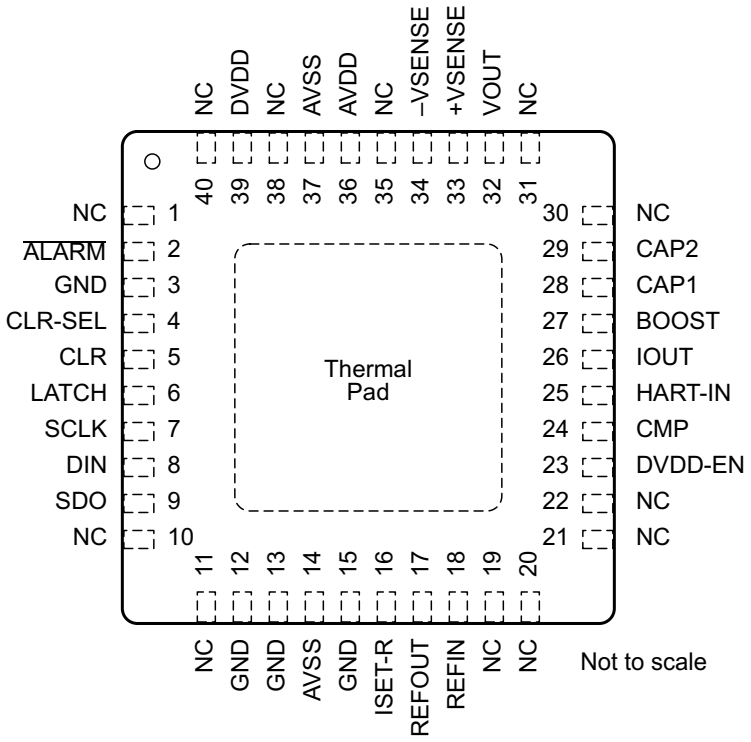


図 6-2. RHA (40-Pin VQFN) Package, Top View

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表 6-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	PWP (HTSSOP)	RHA (VQFN)		
$\overline{\text{ALARM}}$	3	2	Digital output	Alarm pin. Open drain output. External pullup resistor required (10 kΩ). The pin goes low (active) when the $\overline{\text{ALARM}}$ condition is detected (open circuit, over temperature, timeout and so forth).
AVDD	24	36	Supply input	Positive analog power supply.
AVSS	1	14, 37	Supply input	Negative analog power supply in dual power-supply operation. Connects to GND in single power-supply operation.
BOOST	20	27	Analog output	Boost pin. External transistor connection (optional).
CAP1	—	28	Analog input	Connection for current output filtering capacitor (optional).
CAP2	—	29	Analog input	Connection for current output filtering capacitor (optional).
CLR	6	5	Digital input	Clear input. Logic high on this pin causes the part to enter CLEAR state. Active high.
CLR-SEL	5	4	Digital input	Selects the VOUT value in CLEAR state, after power-on and reset.
CMP	17	24	Analog output	External compensation capacitor connection pin (optional). Addition of the external capacitor (connected between VOUT and this pin) improves the stability with high capacitive loads at the VOUT pin by reducing the bandwidth of the output amplifier, thus increasing the settling time. If an external compensation capacitor greater than 470 pF is used, connect an additional 100-pF capacitor from CMP to GND.
DIN	9	8	Digital input	Serial data input. Data are clocked into the 24-bit input shift register on the rising edge of the serial clock input. Schmitt-Trigger logic input.
DVDD	2	39	Supply input or output	Digital power supply. Can be input or output, depending on DVDD-EN pin.
DVDD-EN	16	23	Digital input	Internal power-supply enable pin. Connect this pin to GND to disable the internal supply, or leave this pin unconnected to enable the internal supply. When this pin is connected to GND, an external supply must be connected to the DVDD pin.
GND	4	3,	Supply input	Ground reference point for all digital circuitry of the device. Connect to 0 V.
GND	11, 12	12, 13, 15	Supply input	Ground reference point for all analog circuitry of the device. Connect to 0 V.
HART-IN	18	25	Analog input	Input pin for HART modulation.
IOUT	19	26	Analog output	Current output pin
ISET-R	13	16	Analog input	Connection pin for external precision resistor (15 kΩ); see *セクション 8*.
LATCH	7	6	Digital input	Load DAC registers input. A rising edge on this pin loads the input shift register data into the DAC data and control registers and updates the DAC outputs.
NC	—	1, 10, 11, 19, 20, 21, 22, 30, 31, 35, 38, 40	—	No connection.
REFOUT	14	17	Analog output	Internal reference output. Connect to REFIN when using internal reference.
REFIN	15	18	Analog input	Reference input
SCLK	8	7	Digital input	Serial clock input of serial peripheral interface (SPI). Data can be transferred at rates up to 30 MHz. Schmitt-Trigger logic input.
SDO	10	9	Digital output	Serial data output. Data are valid on the rising edge of SCLK.
Thermal Pad	—	—	Supply input	The thermal pad is internally connected to the AVSS supply. For enhanced thermal performance, thermally connect the pad to a copper plane. The pad can be electrically connected to the same potential as the AVSS pin (either negative supply voltage or GND) or left electrically unconnected provided a supply connection is made at the AVSS pin. The AVSS pin must always be connected to either the negative supply voltage or GND, independent of the thermal pad connection.
VOUT	21	32	Analog output	Voltage output pin. This is a buffered analog voltage output.
+VSENSE	22	33	Analog input	Sense pin for the positive voltage output load connection.

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表 6-1. Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	PWP (HTSSOP)	RHA (VQFN)		
–VSENSE	23	34	Analog input	Sense pin for the negative voltage output load connection.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	40	V
AVDD to GND	–0.3	40	V
AVSS to GND	–20	0.3	V
DVDD to GND	–0.3	6	V
VOUT to AVSS	AVSS	AVDD	V
VOUT to GND(2)	AVSS	AVDD	V
IOUT to AVSS	AVSS	AVDD	V
IOUT to GND(2)	AVSS	AVDD	V
CMP to AVSS	–0.3	6	V
REFIN to GND	–0.3	6	V
REFOUT to GND	–0.3	6	V
Current into REFOUT		10	mA
Digital input voltage to GND	–0.3	DVDD + 0.3	V
SDO to GND	–0.3	DVDD + 0.3	V
$\overline{ALARM}$ to GND	–0.3	6	V
Power dissipation	$(T_{Jmax} – T_A)/R_{\theta JA}$		W
Junction temperature, T_{Jmax}		150	°C
Operating temperature	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AVSS tied to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD (AVDD + |AVSS| ≤ 36 V)		10		36	V
AVSS (AVDD + |AVSS| ≤ 36 V)		–18		0	V
DVDD, Internal regulator disabled		2.7		5.5	V
Reference input voltage		4.95		5.05	V
External reference current (REFIN = 5 V, outputs off or IOUT enabled)			30		µA
Loop compliance voltage (output = 24 mA)(1)				AVDD – 2	V
V_{IH}, Digital input high voltage		2			V
V_{IL}, Digital input low voltage	3.6 V < AVDD < 5.5 V			0.8	V
	2.7 V < AVDD < 3.6 V			0.6	
Specified performance temperature		–40		125	°C

(1) Loop compliance voltage is defined as the voltage at the IOUT pin

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7.4 Thermal Information

THERMAL METRIC[1]		DACx760		UNIT
		RHA (VQFN)	PWP (HTSSOP)	
		40 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.9	32.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	14.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	12.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	12	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	0.63	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external, and DVDD = 2.7 V to 5.5 V; for VOUT: R_L = 1 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω; all specifications are from T_A = –40°C to +125°C (unless otherwise noted); typical specifications are at 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
VOLTAGE OUTPUT						
Voltage output ranges (normal mode)	AVDD ≥ 10 V		0		5	V
	AVDD ≥ 10.5 V		0		10	
	AVSS ≤ –5.5 V, AVDD ≥ 10 V		–5		5	
	AVSS ≤ –10.5 V, AVDD ≥ 10.5 V		–10		10	
Voltage output range (overrange mode)	AVDD ≥ 10 V		0		5.5	V
	AVDD ≥ 11.5 V		0		11	
	AVSS ≤ –6 V, AVDD ≥ 10 V		–5.5		5.5	
	AVSS ≤ –11.5 V, AVDD ≥ 11.5 V		–11		11	
Resolution	DAC8760		16			Bits
	DAC7760		12			
ACCURACY[2]						
Total unadjusted error, TUE	T_A = –40°C to 125°C		–0.07%		0.07%	FSR
	T_A = –40°C to +85°C		–0.06%		0.06%	
	T_A = 25°C		–0.04%	±0.015%	0.04%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL	T_A = –40°C to 125°C				±0.04%	FSR
	T_A = –40°C to +85°C				±0.022%	
Bipolar zero error	T_A = –40°C to 125°C		–7		7	mV
	T_A = –40°C to +85°C		–6		6	
	T_A = 25°C, ±5 V and ±5.5 V		–1.5	±0.5	1.5	
	T_A = 25°C, ±10 V and ±11 V		–3	±1	3	
Bipolar zero error temperature coefficient				±1		ppm FSR/°C
Zero-scale error[3]	Unipolar range (0 V to 5 V, 0 V to 5.5 V, 0 V to 10 V, 0 V to 11 V)	T_A = –40°C to 125°C	–4		4	mV
		T_A = –40°C to +85°C	–2		2	
		T_A = 25°C	–0.6	±0.1	0.6	
	Bipolar range (±5 V, ±5.5 V, ±10 V, ±11 V)	T_A = –40°C to 125°C	–10		10	mV
		T_A = 25°C	–3.5	±1	3.5	
Zero-scale error temperature coefficient				±2		ppm FSR/°C
Offset error	T_A = –40°C to 125°C, unipolar range		–4		4	mV
	T_A = –40°C to +85°C, unipolar range		–2		2	
	T_A = 25°C, unipolar range		–0.6	±0.1	0.6	

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7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external, and DVDD = 2.7 V to 5.5 V; for VOUT: R_L = 1 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω; all specifications are from T_A = –40°C to +125°C (unless otherwise noted); typical specifications are at 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACCURACY (continued)					
Offset error temperature coefficient			±1		ppm FSR/°C
Gain error	T_A = –40°C to 125°C	–0.07%		0.07%	FSR
	T_A = –40°C to +85°C	–0.06%		0.06%	
	T_A = 25°C	–0.04%	±0.01%	0.04%	
Gain error temperature coefficient			±3		ppm FSR/°C
Full-scale error	T_A = –40°C to 125°C	–0.07%		0.07%	FSR
	T_A = –40°C to +85°C	–0.06%		0.06%	
	T_A = 25°C	–0.04%	±0.01%	0.04%	
Full-scale error temperature coefficient			±1		ppm FSR/°C
VOLTAGE OUTPUT (UNIPOLAR AND BIPOLAR MODES)					
Headroom	AVDD with respect to VOUT full scale	0.5			V
Footroom	AVSS with respect to VOUT zero scale	–0.5			V
Output voltage drift vs time	T_A = 125°C, 1000 hrs		±15		ppm FSR
Short-circuit current			30		mA
Load	For specified performance	1			kΩ
Capacitive load stability[4]	R_L = ∞			20	nF
	R_L = 1 kΩ			5	nF
	R_L = 1 kΩ, external compensation capacitor (4 nF) connected			1	µF
DC output impedance	Code = 0x8000		0.3		Ω
DC PSRR[4]	No output load		3	10	µV/V
CURRENT OUTPUT					
Output current ranges	RANGE bits = 111	0		24	mA
	RANGE bits = 110	0		20	
	RANGE bits = 101	4		20	
Resolution	DAC8760	16			Bits
	DAC7760	12			
ACCURACY (0-mA to 20-mA and 0-mA to 24-mA Range)[1]					
Total unadjusted error, TUE	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
	T_A = –40°C to +85°C	–0.16%		0.16%	
	T_A = 25°C	–0.08%	±0.02%	0.08%	
Differential nonlinearity, DNL	Monotonic			±1	LSB
Relative accuracy, INL[5]	T_A = –40°C to +125°C			±0.08%	FSR
	T_A = –40°C to +85°C			±0.024%	
Offset error	T_A = –40°C to +125°C	–0.17%		0.17%	FSR
	T_A = –40°C to +85°C	–0.1%		0.1%	
	T_A = 25°C	–0.07%	±0.01%	0.07%	
Offset error temperature coefficient			±5		ppm FSR/°C
Full-scale error	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
	T_A = –40°C to +85°C	–0.16%		0.16%	
	T_A = 25°C	–0.08%	±0.015%	0.08%	
Full-scale error temperature coefficient	Internal R_{SET}		±5		ppm FSR/°C
	External R_{SET}		±10		

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7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external, and DVDD = 2.7 V to 5.5 V; for VOUT: R_L = 1 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω; all specifications are from T_A = –40°C to +125°C (unless otherwise noted); typical specifications are at 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY (0-mA to 20-mA and 0-mA to 24-mA Range) (continued)						
Gain error	Internal R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
		T_A = –40°C to +85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.17%		0.17%	
		T_A = –40°C to +85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.05%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = +125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±25		
ACCURACY (4-mA TO 20-mA RANGE)[1]						
Total unadjusted error, TUE	Internal R_{SET}	T_A = –40°C to +125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0.08%	±0.02%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.29%		0.29%	
		T_A = –40°C to +85°C	–0.25%		0.25%	
		T_A = 25°C	–0.1%	±0.02%	0.1%	
Differential nonlinearity, DNL	Monotonic				±1	LSB
Relative accuracy, INL[5]	T_A = –40°C to +125°C				±0.08%	FSR
	T_A = –40°C to +85°C				±0.024%	
Offset error	Internal R_{SET}	T_A = –40°C to +125°C	–0.22%		0.22%	FSR
		T_A = –40°C to +85°C	–0.2%		0.2%	
	External R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	
		T_A = –40°C to +85°C	–0.18%		0.18%	
	Internal and External R_{SET}, T_A = 25°C		–0.07%	±0.01%	0.07%	
Offset error temperature coefficient				±3		ppm FSR/°C
Full-scale error	Internal R_{SET}	T_A = –40°C to +125°C	–0.25%		0.25%	FSR
		T_A = 25°C	–0.08%	±0.015%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.29%		0.29%	
		T_A = –40°C to +85°C	–0.25%		0.25%	
		T_A = 25°C	–0.1%	±0.015%	0.1%	
Full-scale error temperature coefficient	Internal R_{SET}			±5		ppm FSR/°C
	External R_{SET}			±10		
Gain error	Internal R_{SET}	T_A = –40°C to +125°C	–0.2%		0.2%	FSR
		T_A = –40°C to +85°C	–0.15%		0.15%	
		T_A = 25°C	–0.08%	±0.01%	0.08%	
	External R_{SET}	T_A = –40°C to +125°C	–0.16%		0.16%	
		T_A = –40°C to +85°C	–0.12%		0.12%	
		T_A = 25°C	–0.05%	±0.01%	0.055%	
Gain error temperature coefficient	Internal R_{SET}			±3		ppm FSR/°C
	External R_{SET}			±8		
Output current drift vs time	T_A = 125°C, 1000 hrs	Internal R_{SET}		±50		ppm FSR
		External R_{SET}		±75		
CURRENT OUTPUT[4]						
Inductive load				50		mH
DC PSRR					1	µA/V
Output impedance	Code = 0x8000			50		MΩ

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7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external, and DVDD = 2.7 V to 5.5 V; for VOUT: R_L = 1 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω; all specifications are from T_A = –40°C to +125°C (unless otherwise noted); typical specifications are at 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL REFERENCE INPUT					
Reference input capacitance			10		pF
INTERNAL REFERENCE OUTPUT					
Reference output	T_A = 25°C	4.995		5.005	V
Reference temperature coefficient(4)	T_A = –40°C to +85°C			±10	ppm/°C
Output noise (0.1 Hz to 10 Hz)	T_A = 25°C		14		μV_{PP}
Noise spectral density	T_A = 25°C, 10 kHz		185		nV/√Hz
Capacitive load			600		nF
Load current			±5		mA
Short-circuit current (REFOUT shorted to GND)			25		mA
Load regulation	AVDD = 24 V, AVSS = 0 V, T_A = 25°C, sourcing		55		µV/mA
	AVDD = 24 V, AVSS = 0 V, T_A = 25°C, sinking		120		
Line regulation			±1.2		µV/V
DVDD INTERNAL REGULATOR					
Output voltage	AVDD = 24 V		4.6		V
Output load current(4)				10	mA
Load regulation			3.5		mV/mA
Line regulation			1		mV/V
Short-circuit current	AVDD = 24 V, to GND		35		mA
Capacitive load stability(4)				2.5	µF
DIGITAL INPUTS					
Hysteresis voltage			0.4		V
Input current	DVDD-EN, V_{IN} ≤ 5 V	–2.7			µA
	All pins other than DVDD-EN			±1	µA
Pin capacitance	Per pin		10		pF
DIGITAL OUTPUTS					
SDO	V_{OL}, output low voltage, sinking 200 µA			0.4	V
	V_{OH}, output high voltage, sourcing 200 µA	DVDD – 0.5			V
	High-impedance leakage			±1	µA
$\overline{ALARM}$	V_{OL}, output low voltage, 10-kΩ pullup resistor to DVDD			0.4	V
	V_{OL}, output low voltage, 2.5 mA			0.6	V
	High-impedance leakage			±1	µA
High-impedance output capacitance			10		pF

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7.5 Electrical Characteristics (continued)

at AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external, and DVDD = 2.7 V to 5.5 V; for VOUT: R_L = 1 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω; all specifications are from T_A = –40°C to +125°C (unless otherwise noted); typical specifications are at 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS					
AIDD	Outputs disabled, external DVDD			3	mA
	Outputs disabled, internal DVDD			4	
	Code = 0x8000, VOUT enabled, unloaded			4.6	
	Code = 0x0000, IOUT enabled			3	
	Code = 0x0000, both outputs enabled, VOUT unloaded			4.6	
AISS	Outputs disabled			0.6	mA
	Outputs disabled, Internal DVDD			0.6	
	Code = 0x8000, VOUT enabled, unloaded			2.6	
	Code = 0x0000, IOUT enabled			0.6	
	Code = 0x0000, both outputs enabled, VOUT unloaded			2.6	
DIDD	V_{IH} = DVDD, V_{IL} = GND, interface idle			1	mA
Power dissipation	AVDD = 36 V, AVSS = GND, VOUT enabled, unloaded, DVDD = 5 V		140	170	mW
	AVDD = 18 V, AVSS = –18 V, VOUT enabled, unloaded, DVDD = 5 V			135	
TEMPERATURE					
Thermal alarm			142		°C
Thermal alarm hysteresis			18		°C

(1) DAC8760 and DAC7760 current output range is set by writing to RANGE bits in control register at address 0x55.
(2) When powered with AVSS = 0 V, INL and offset error for the 0-V to 5-V and 0-V to 10-V ranges are calculated beginning from code 0x0100 for DAC8760 and from code 0x0010 for DAC7760.
(3) Assumes a footroom of 0.5 V.
(4) Specified by design and characterization; not production tested.
(5) For 0-mA to 20-mA and 0-mA to 24-mA ranges, INL is calculated beginning from code 0x0100 for DAC8760 and from code 0x0010 for DAC7760.

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7.6 Electrical Characteristics: AC

At AVDD = 10 V to 36 V, AVSS = –18 V to 0 V, AVDD + |AVSS| ≤ 36 V, GND = 0 V, REFIN = 5-V external; and DVDD = 4.5 V to 5.5 V. For VOUT: R_L = 2 kΩ, C_L = 200 pF; for IOUT: R_L = 300 Ω. All specifications –40°C to 125°C, unless otherwise noted. Typical specifications are at 25°C.

PARAMETER(1)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE					
CURRENT OUTPUT					
Output current settling time	16-mA step, to 0.1% FSR, no L (inductance)		10		µs
	16-mA step, to 0.1% FSR, L < 1 mH		25		
AC PSRR	200-mV, 50-Hz or 60-Hz sine wave superimposed on power-supply voltage		–75		dB
VOLTAGE OUTPUT					
Output voltage settling time	0 V to 10 V, to ±0.03% FSR		22		µs
	0 V to 5 V, to ±0.03% FSR		13		
Slew rate			0.5		V/µs
Power-on glitch energy			2.5		µV-s
Digital-to-analog glitch energy			0.4		µV-s
Glitch impulse peak amplitude			200		mV
Digital feedthrough			2		nV-s
Output noise (0.1-Hz to 10-Hz bandwidth)			0.1		LSB_{PP}
1 / f corner frequency			100		Hz
Output noise spectral density	Measured at 10 kHz		180		nV/√Hz
AC PSRR	200-mV, 50-Hz, or 60-Hz sine wave superimposed on power-supply voltage		–75		dB

(1) Specified by characterization, not production tested.

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7.7 Timing Requirements: Write Mode

At T_A = –40°C to +125°C and DV_{DD} = 2.7 V to 5.5 V, unless otherwise noted. See 図 7-1 for timing diagram.

PARAMETER(1)		MIN	MAX	UNIT
t_1	SCLK cycle time	33		ns
t_2	SCLK low time	13		ns
t_3	SCLK high time	13		ns
t_4	LATCH delay time	13		ns
t_5	LATCH high time(2)	40		ns
t_6	Data setup time	5		ns
t_7	Data hold time	7		ns
t_8	LATCH low time	40		ns
t_9	CLR pulse width	20		ns
t_{10}	CLR activation time		5	µs

(1) Specified by design, not production tested.
(2) Based on digital interface circuitry only.
When writing to DAC control and config registers, consider the analog output specifications in *セクション 7.6*.

7.8 Timing Requirements: Readback Mode

At T_A = –40°C to +125°C and DV_{DD} = 2.7 V to 5.5 V, unless otherwise noted. See 図 7-2 for timing diagram.

PARAMETER(1)		MIN	MAX	UNIT
t_{11}	SCLK cycle time	60		ns
t_{12}	SCLK low time	25		ns
t_{13}	SCLK high time	25		ns
t_{14}	LATCH delay time	13		ns
t_{15}	LATCH high time	40		ns
t_{16}	Data setup time	5		ns
t_{17}	Data hold time	7		ns
t_{18}	LATCH low time	40		ns
t_{19}	Serial output delay time ($C_{L,\ SDO}$ = 15 pF)		35	ns
t_{20}	LATCH rising edge to SDO 3-state ($C_{L,\ SDO}$ = 15 pF)		35	ns

(1) Specified by design, not production tested.

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7.9 Timing Diagrams

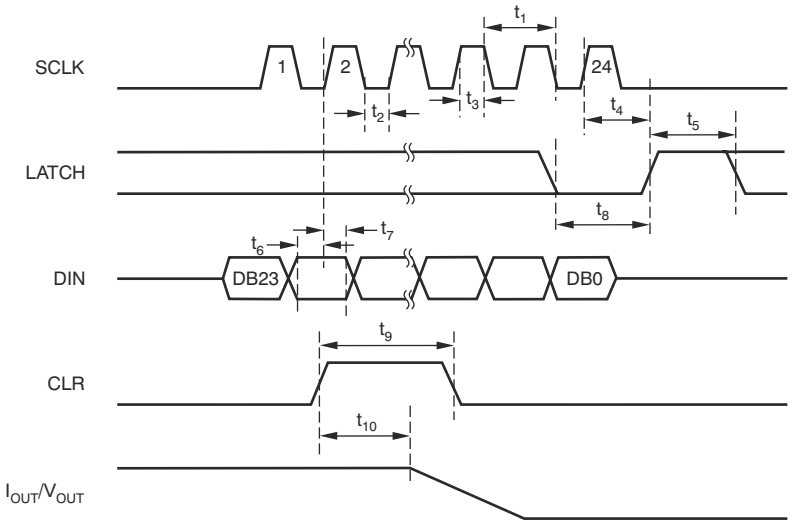


図 7-1. Write Mode Timing

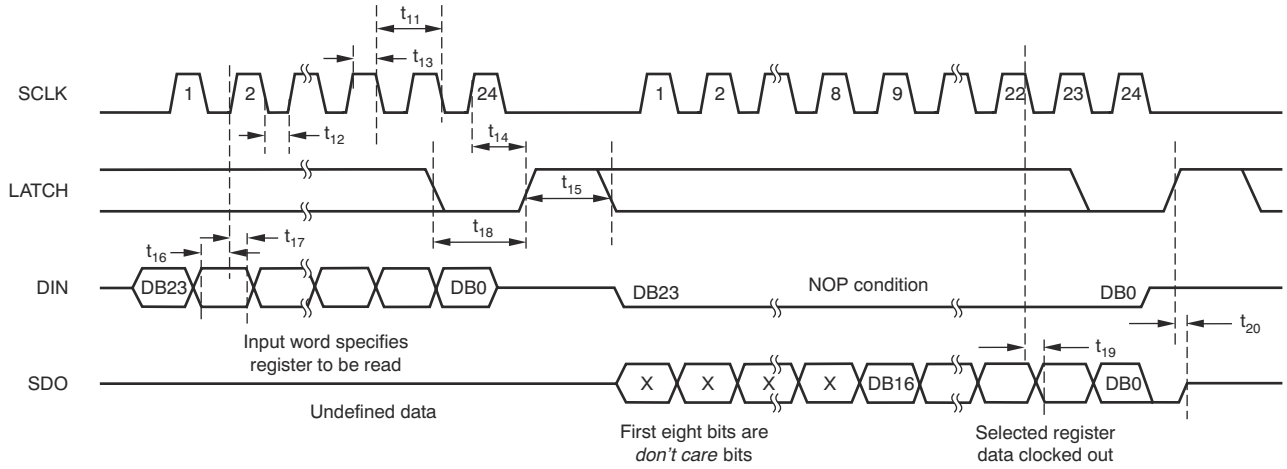


図 7-2. Readback Mode Timing

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7.10 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

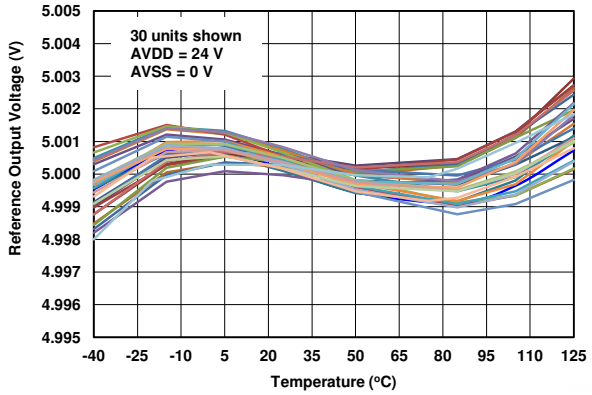


図 7-3. REFOUT vs Temperature

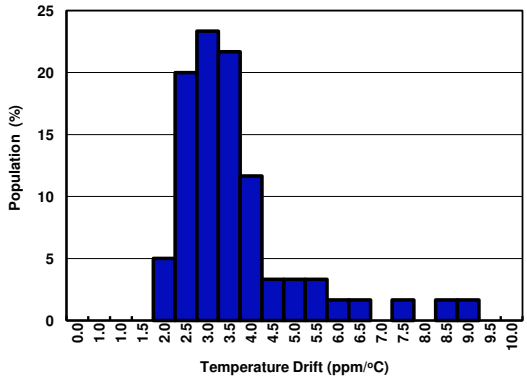


図 7-4. Internal Reference Temperature Drift Histogram

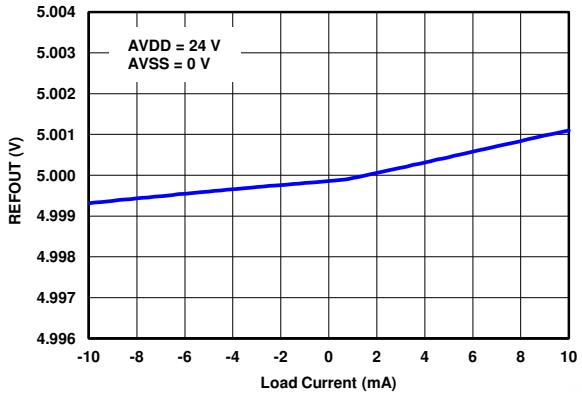


図 7-5. REFOUT vs Load Current

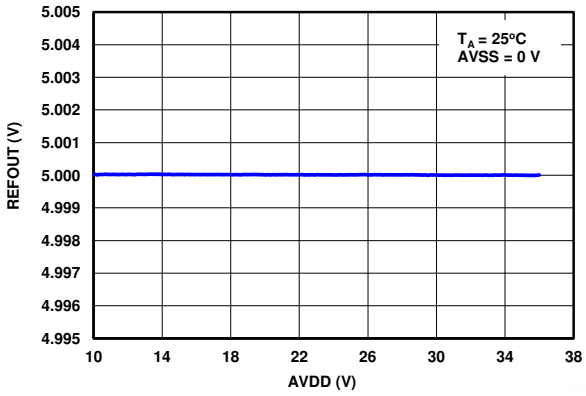


図 7-6. REFOUT vs AVDD

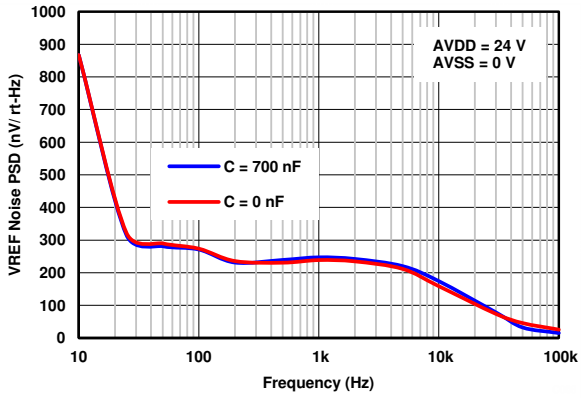


図 7-7. REFOUT Noise PSD vs Frequency

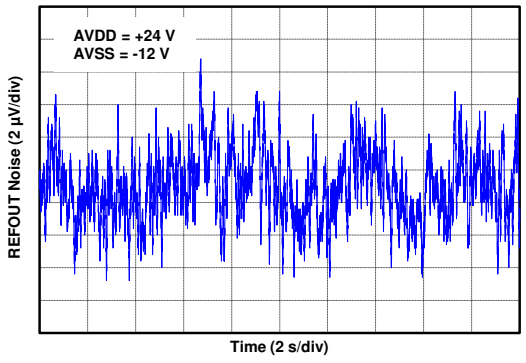


図 7-8. Internal Reference, Peak-to-Peak Noise (0.1 Hz to 10 Hz)

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

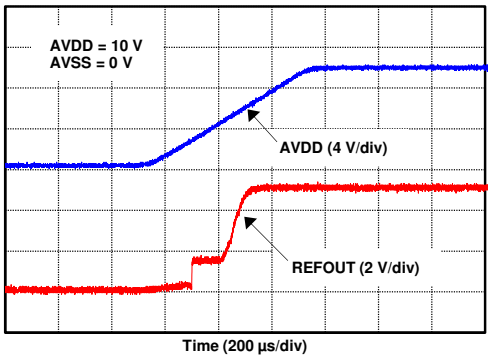


図 7-9. REFOUT Transient vs Time

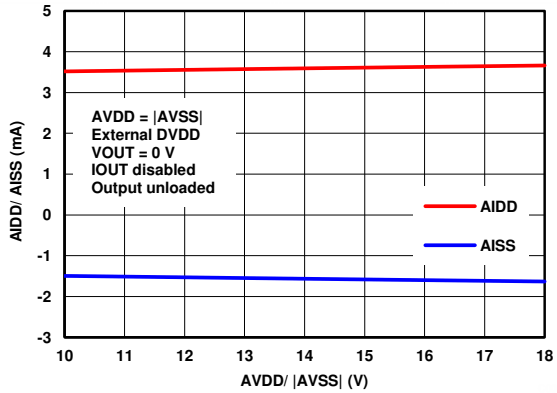


図 7-10. AIDD or AISS vs AVDD or AVSS

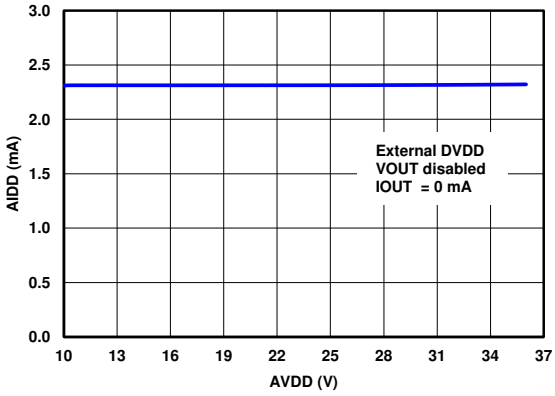


図 7-11. AIDD vs AVDD

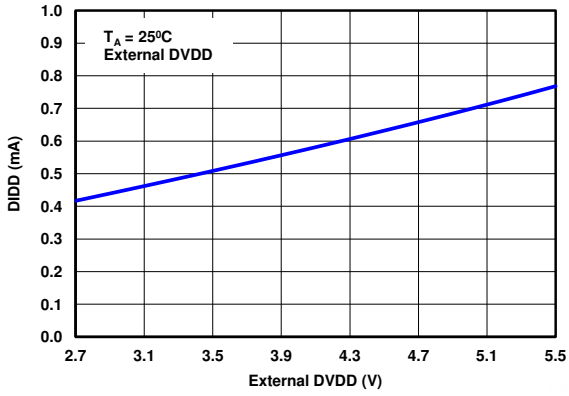


図 7-12. DIDD vs External DVDD

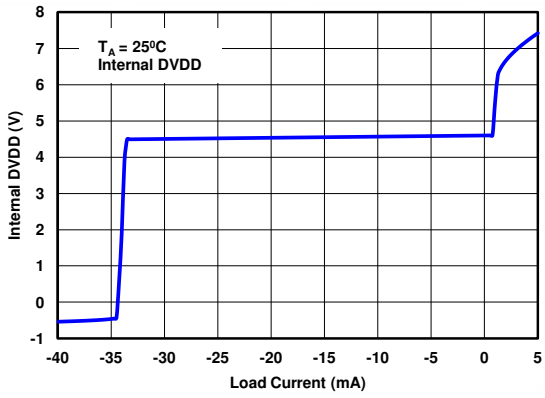


図 7-13. Internal DVDD vs Load Current

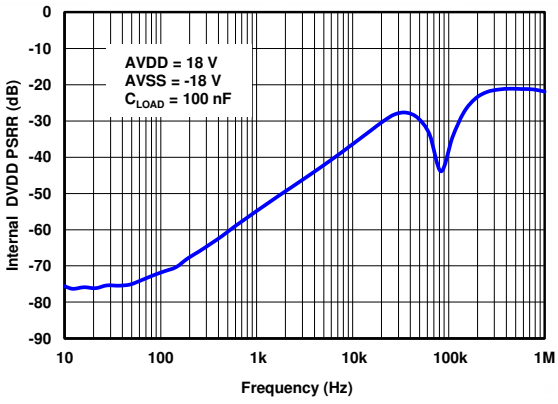


図 7-14. Internal DVDD PSRR vs Frequency

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

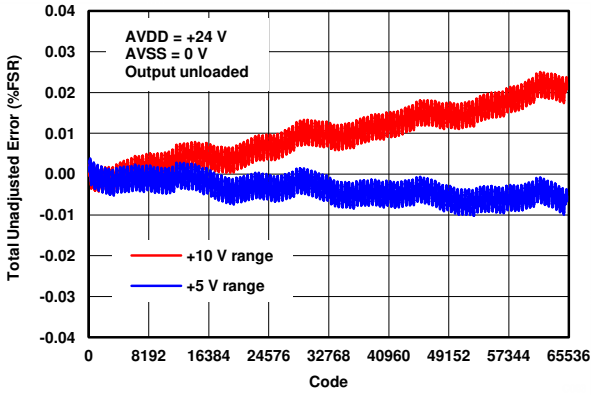


図 7-15. VOUT TUE vs Code (Unipolar Outputs)

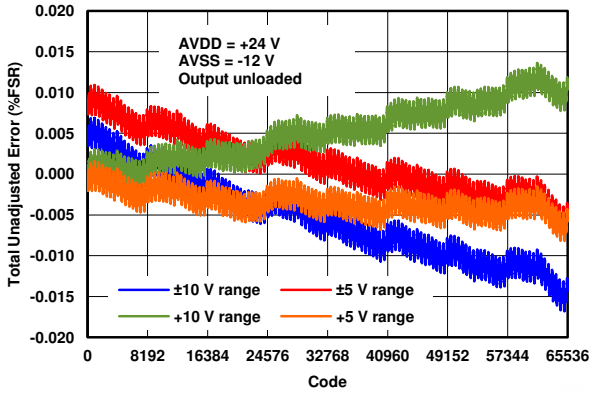


図 7-16. VOUT TUE vs Code

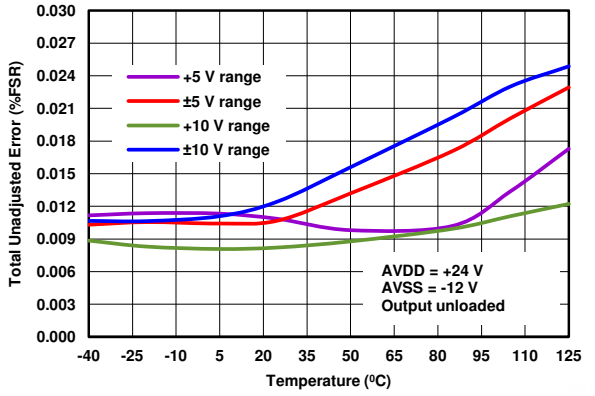


図 7-17. VOUT TUE vs Temperature

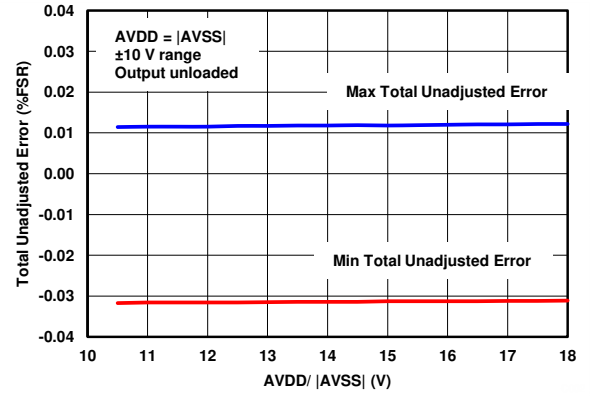


図 7-18. VOUT TUE vs Supply

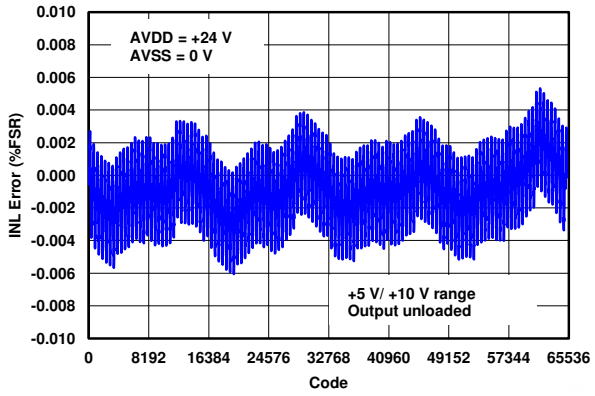


図 7-19. VOUT INL vs Code (Unipolar Outputs)

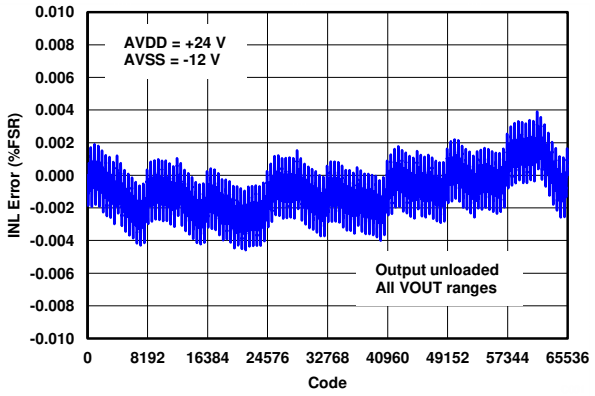


図 7-20. VOUT INL vs Code

7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

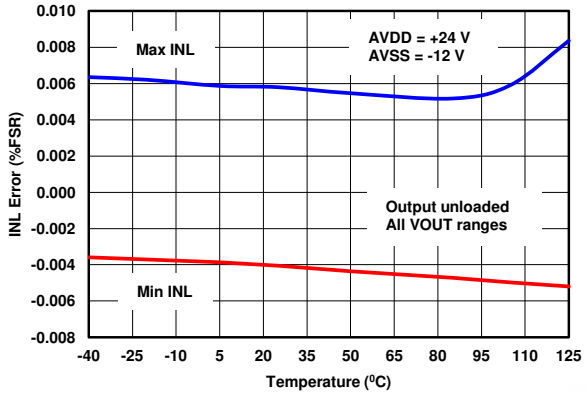


図 7-21. VOUT INL vs Temperature

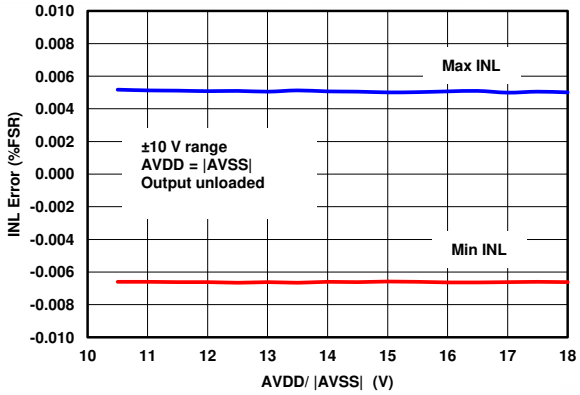


図 7-22. VOUT INL vs Supply

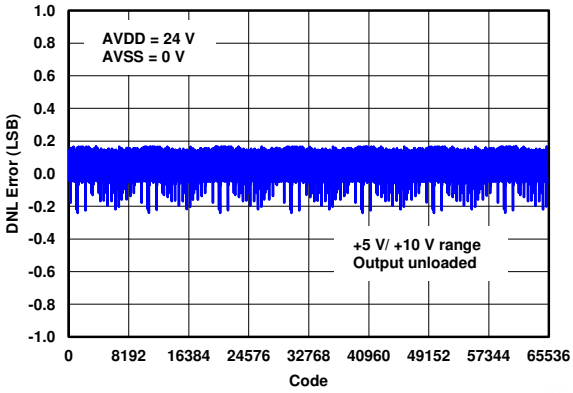


図 7-23. VOUT DNL vs Code (Unipolar Outputs)

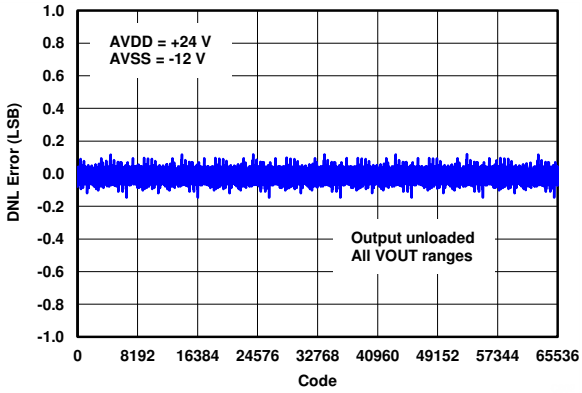


図 7-24. VOUT DNL vs Code

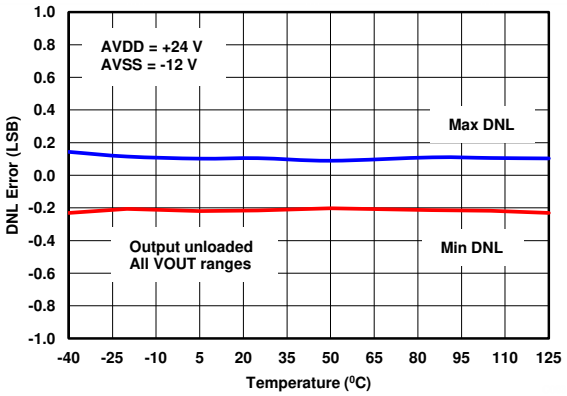


図 7-25. VOUT DNL vs Temperature

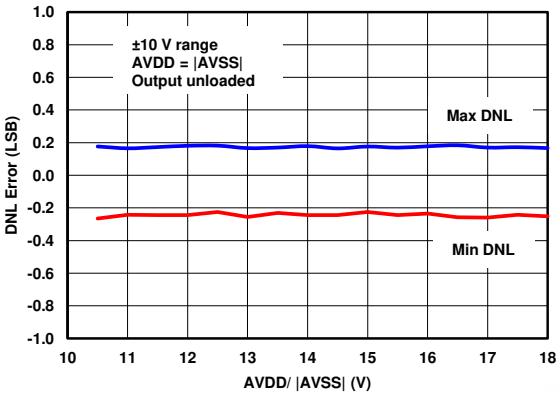


図 7-26. VOUT DNL vs Supply

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

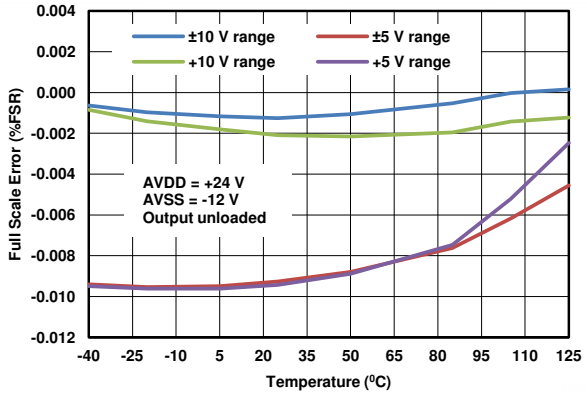


図 7-27. VOUT Full-Scale Error vs Temperature

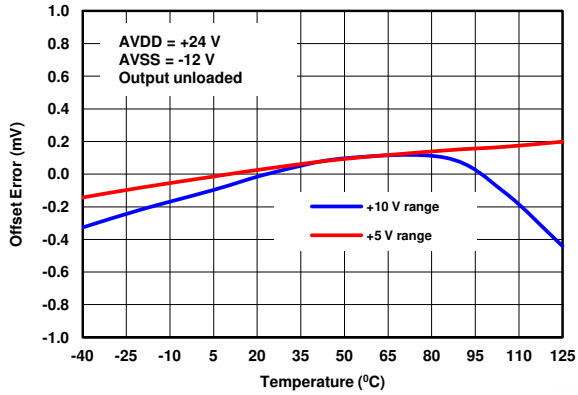


図 7-28. Offset Error vs Temperature

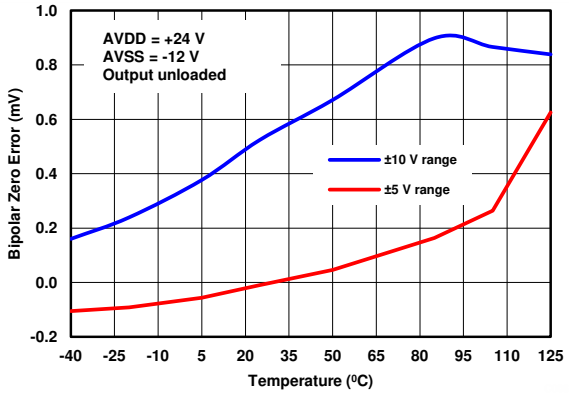


図 7-29. Bipolar Zero Error vs Temperature

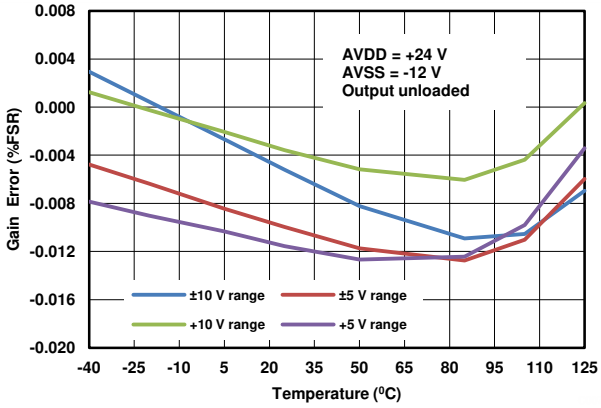


図 7-30. Gain Error vs Temperature

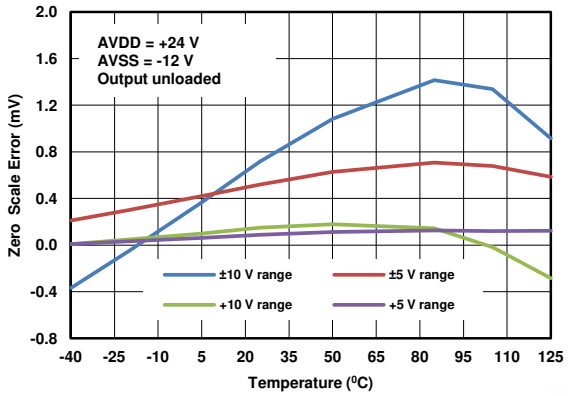


図 7-31. Zero-Scale Error vs Temperature

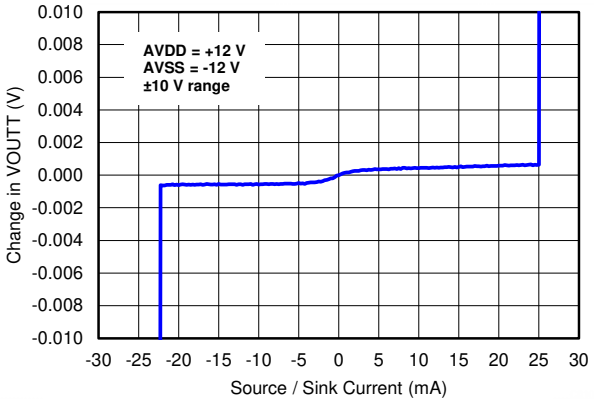


図 7-32. VOUT (Full-Scale) vs Load Current (Source or Sink)

7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

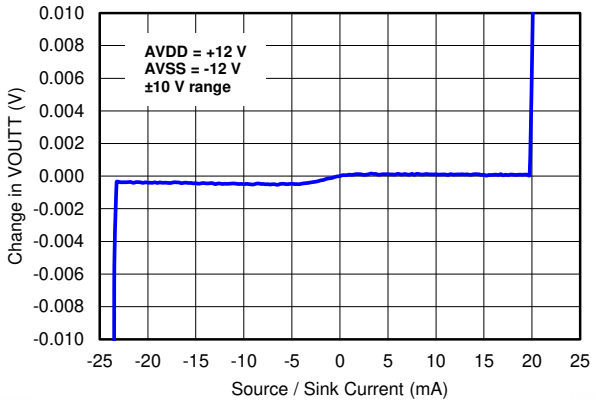


図 7-33. VOUT (Zero-Scale) vs Load Current (Source or Sink)

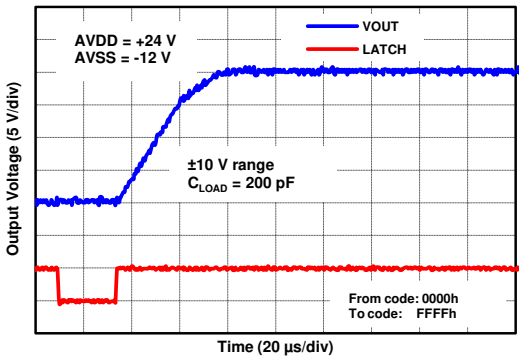


図 7-34. BP10V Rising

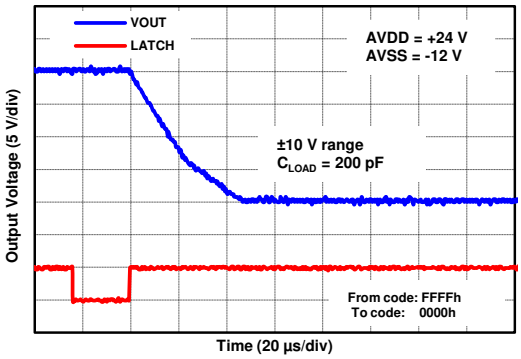


図 7-35. BP10V Falling

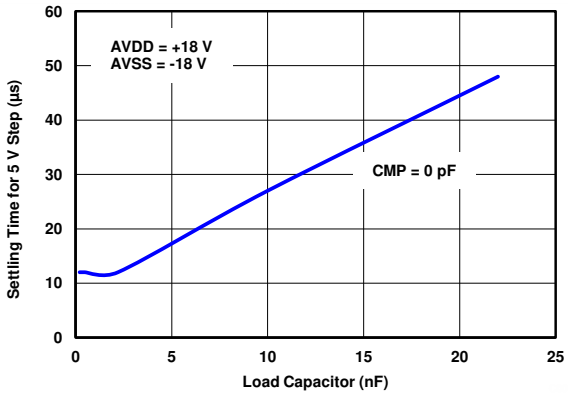


図 7-36. VOUT Settling Time vs Load (No Compensation Capacitor)

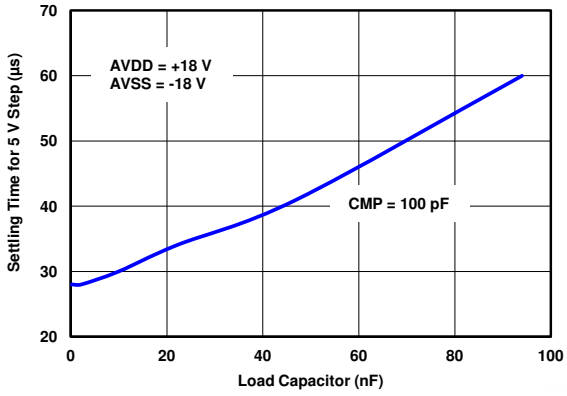


図 7-37. VOUT Settling Time vs LOAD (100 pF Between VOUT and CMP Pins)

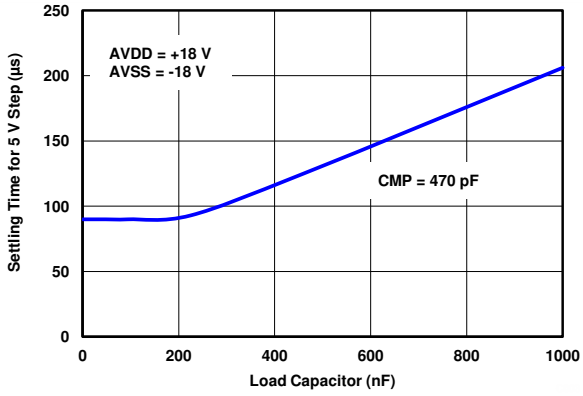


図 7-38. VOUT Settling Time vs LOAD (470 pF Between VOUT and CMP Pins)

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

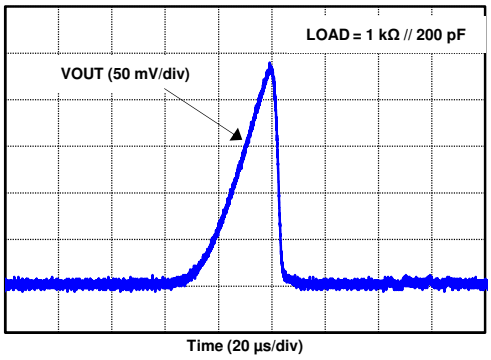


図 7-39. VOUT Power-On Glitch

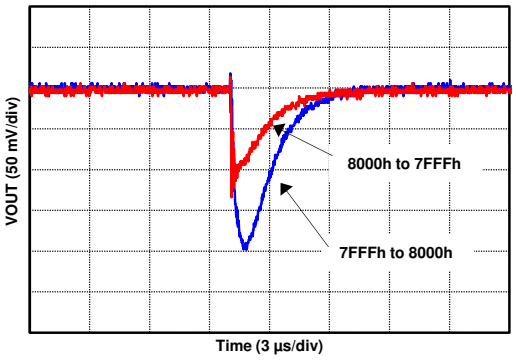


図 7-40. VOUT Digital-to-Analog Glitch

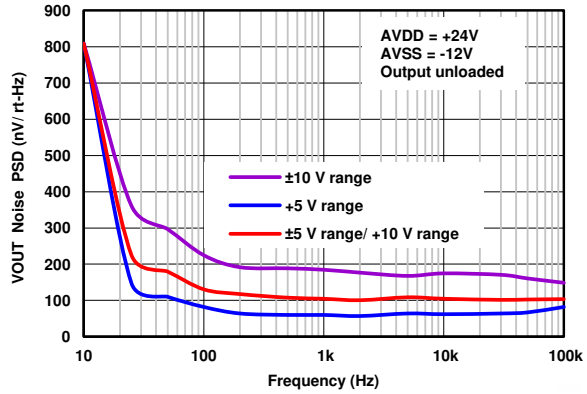


図 7-41. VOUT Noise PSD vs Frequency

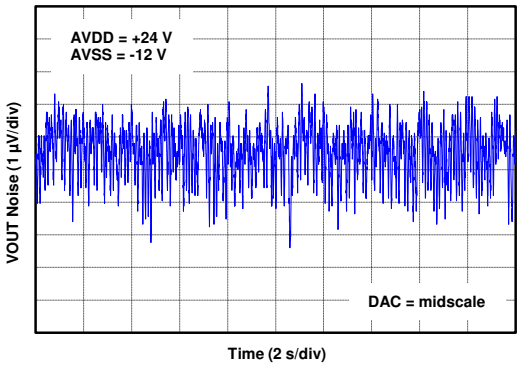


図 7-42. VOUT, Peak-to-Peak Noise (0.1 Hz to 10 Hz)

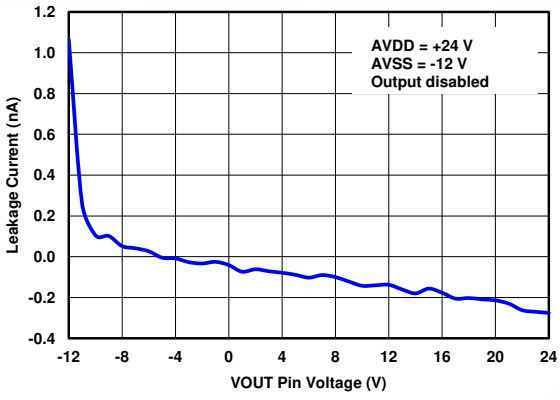


図 7-43. VOUT Hi-Z Leakage Current vs Voltage

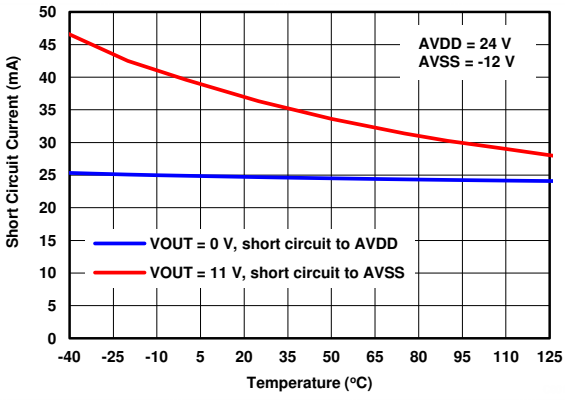


図 7-44. VOUT Short-Circuit Current vs Temperature

7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

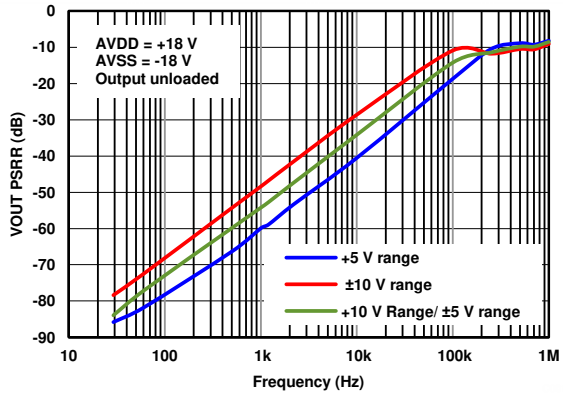


図 7-45. AVDD PSRR for VOUT

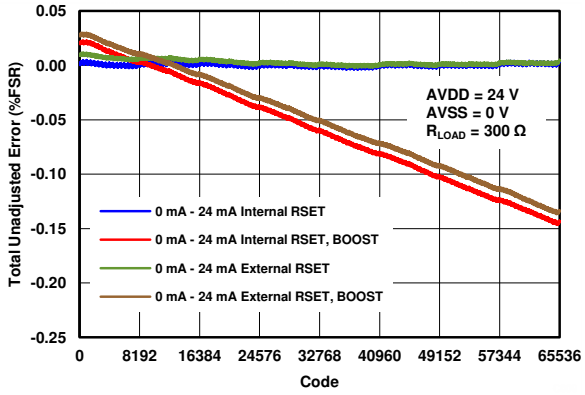


図 7-46. IOUT TUE vs Code (0 mA to 24 mA)

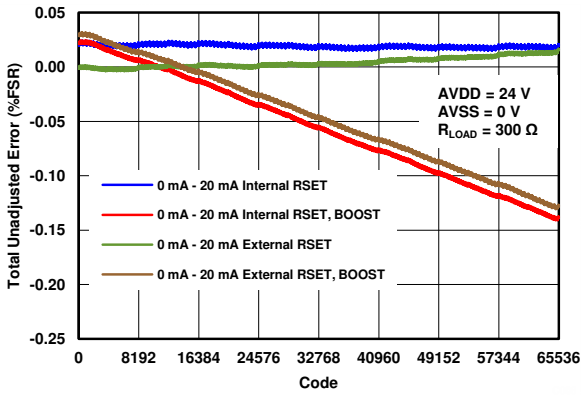


図 7-47. IOUT TUE vs Code (0 mA to 20 mA)

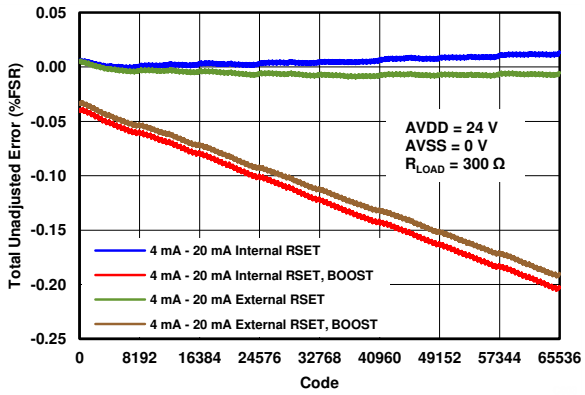


図 7-48. IOUT TUE vs Code (4 mA to 20 mA)

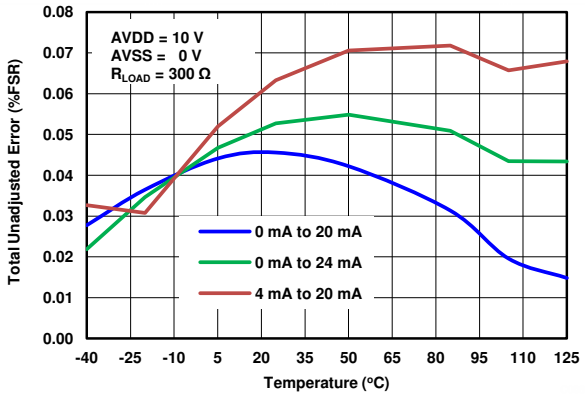


図 7-49. IOUT TUE vs Temperature (Internal R_{SET})

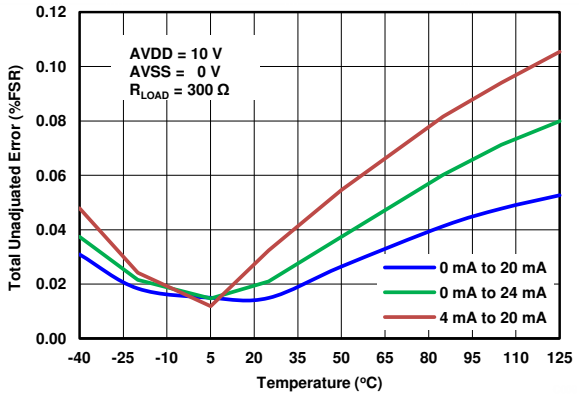


図 7-50. IOUT TUE vs Temperature (External R_{SET})

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

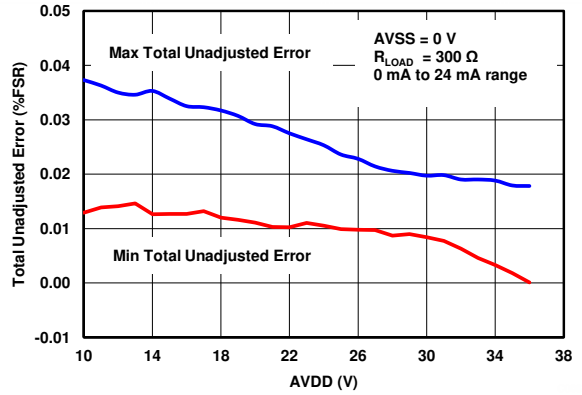


図 7-51. IOUT TUE vs Supply (Internal R_{SET})

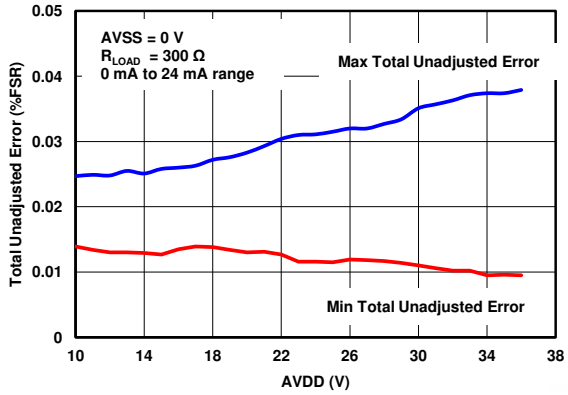


図 7-52. IOUT TUE vs Supply (External R_{SET})

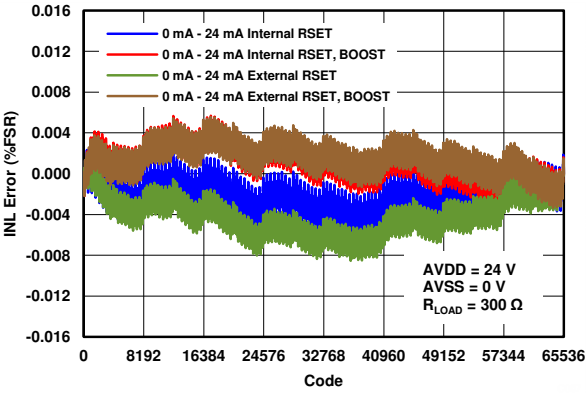


図 7-53. IOUT INL vs Code (0 mA to 24 mA)

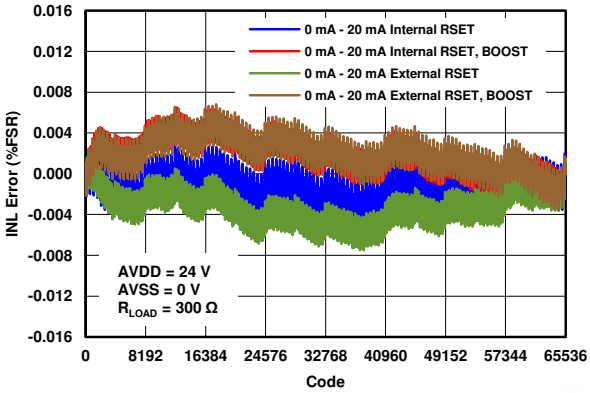


図 7-54. IOUT INL vs Code (0 mA to 20 mA)

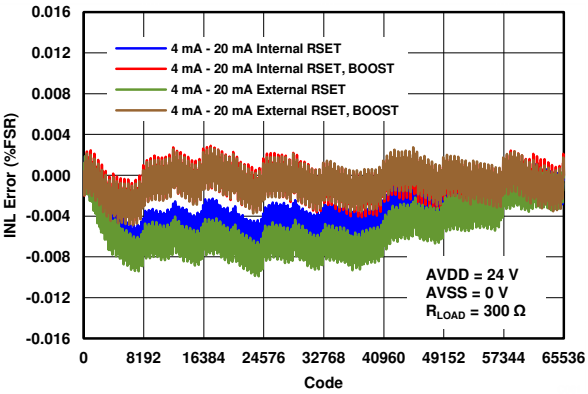


図 7-55. IOUT INL vs Code (4 mA to 20 mA)

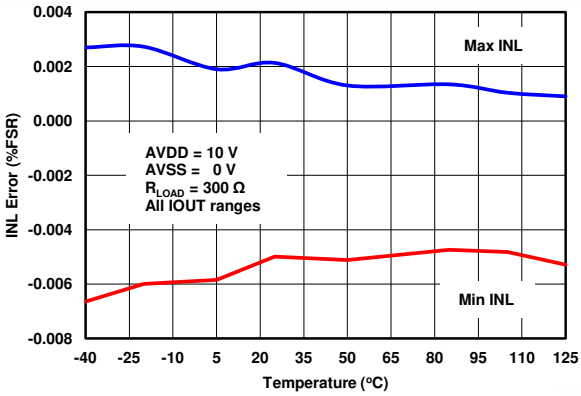


図 7-56. IOUT INL vs Temperature (Internal R_{SET})

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

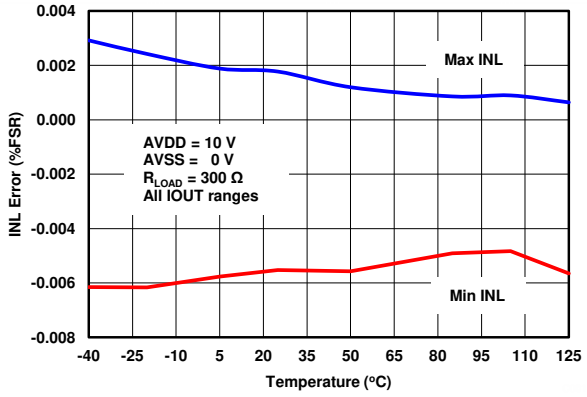


図 7-57. IOUT INL vs Temperature (External R_{SET})

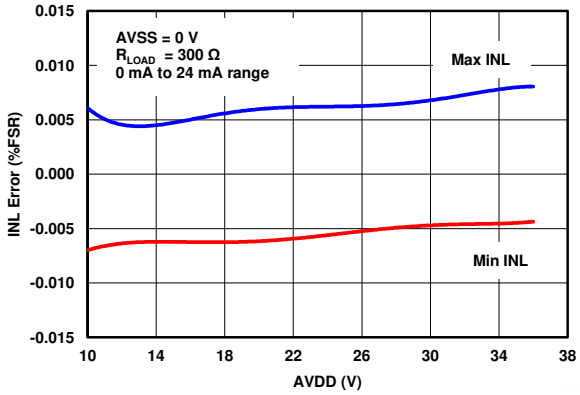


図 7-58. IOUT INL vs Supply (Internal R_{SET})

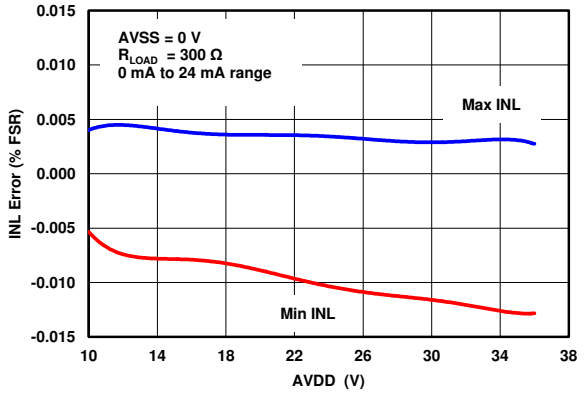


図 7-59. IOUT INL vs Supply (External R_{SET})

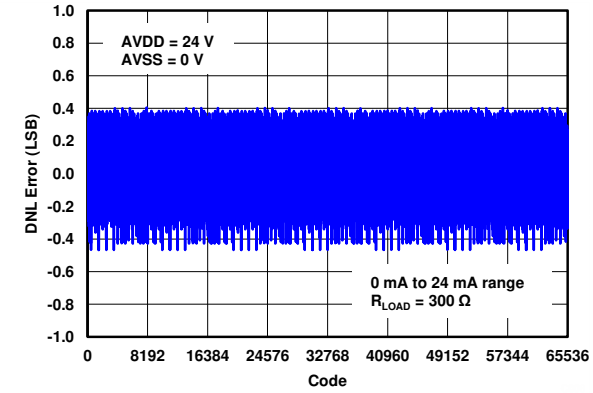


図 7-60. IOUT DNL vs CODE (0 mA to 24 mA)

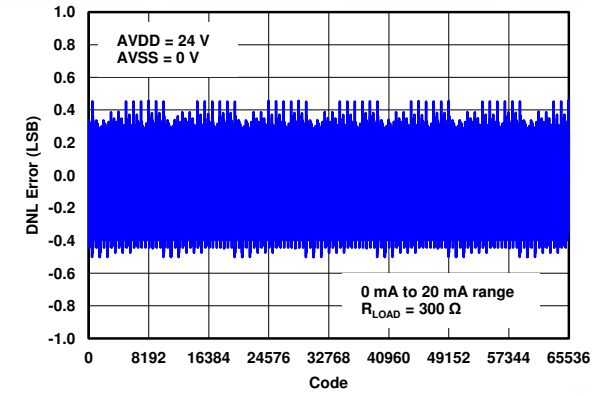


図 7-61. IOUT DNL vs Code (0 mA to 20 mA)

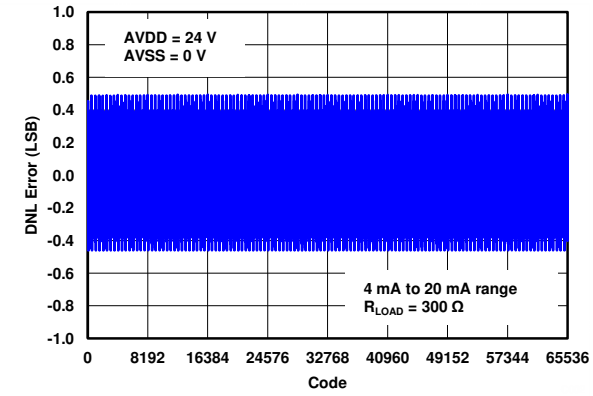


図 7-62. IOUT DNL vs Code (4 mA to 20 mA)

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

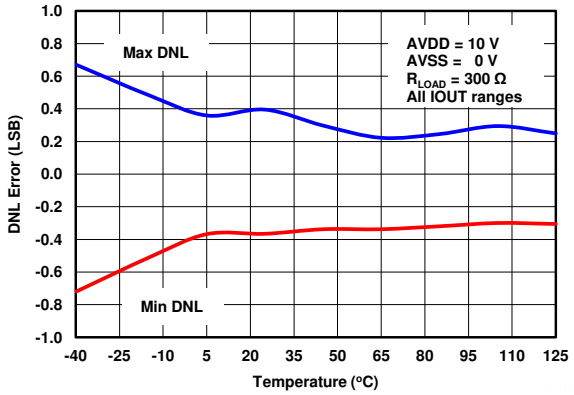


図 7-63. IOUT DNL vs Temperature (Internal R_{SET})

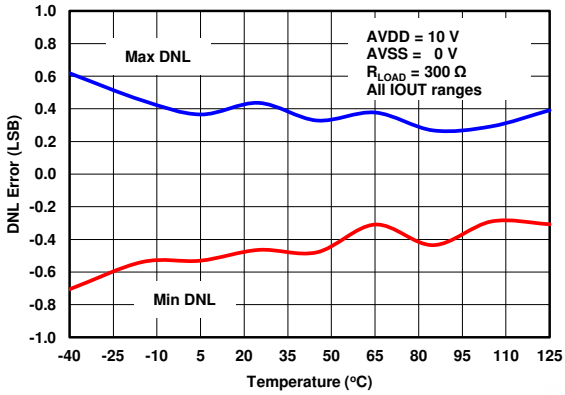


図 7-64. IOUT DNL vs Temperature (External R_{SET})

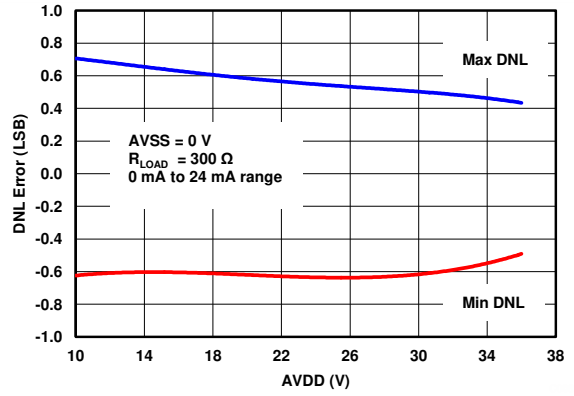


図 7-65. IOUT DNL vs Supply (Internal R_{SET})

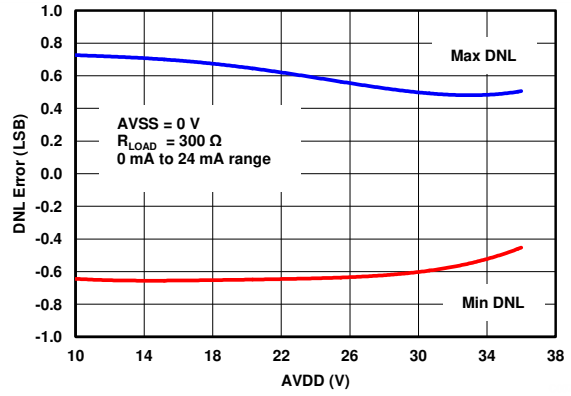


図 7-66. IOUT DNL vs Supply (External R_{SET})

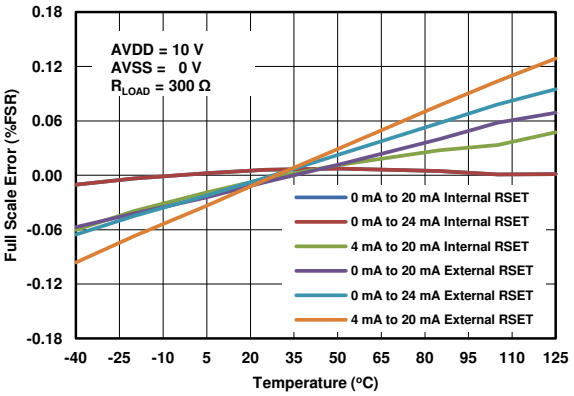


図 7-67. IOUT Full-Scale Error vs Temperature

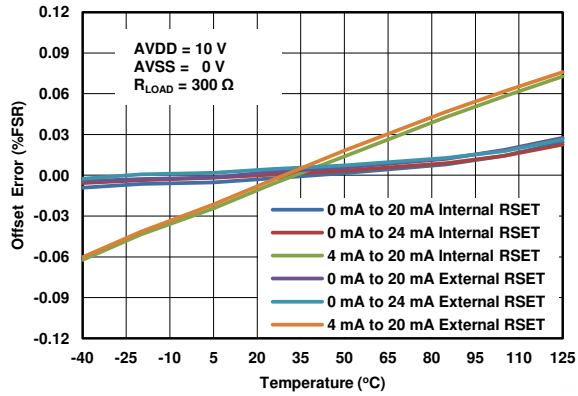


図 7-68. IOUT Offset Error vs Temperature

7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

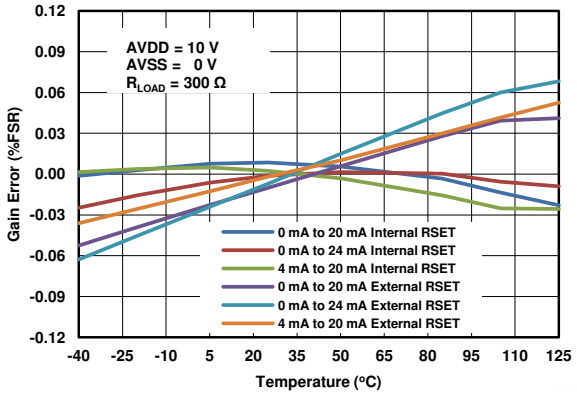
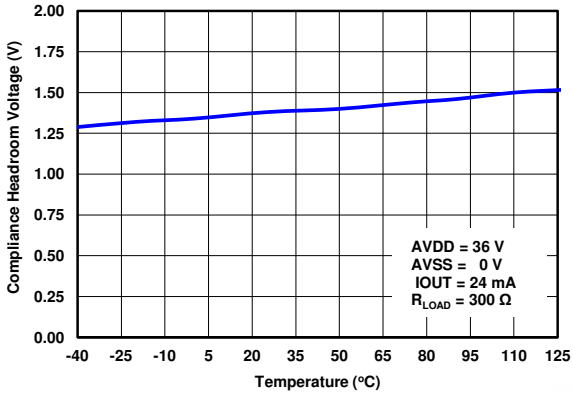
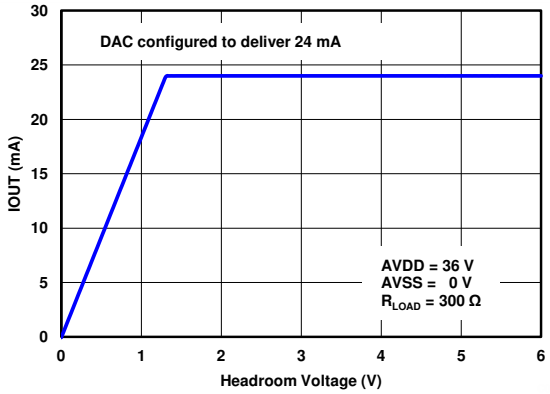


図 7-69. IOUT Gain Error vs Temperature



Compliance voltage headroom is defined as the drop from AVDD pin to the IOUT pin.

図 7-70. Compliance Headroom Voltage(1) vs Temperature



Compliance voltage headroom is defined as the drop from AVDD pin to the IOUT pin.

図 7-71. IOUT vs Compliance Headroom Voltage

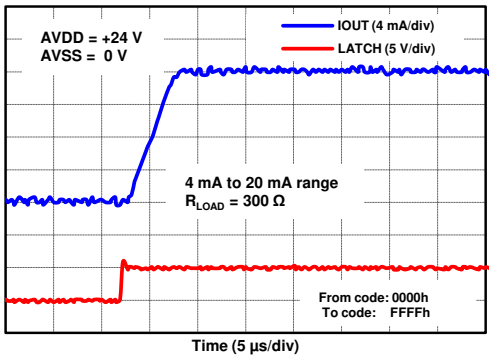


図 7-72. 4-mA to 20-mA Rising

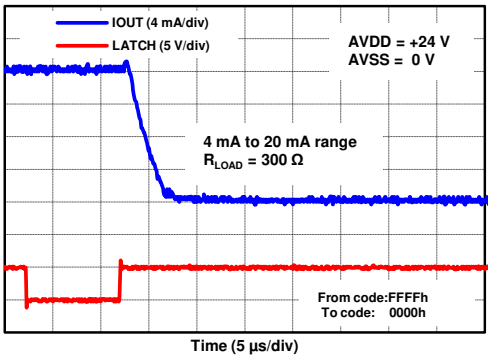


図 7-73. 4-mA to 20-mA Falling

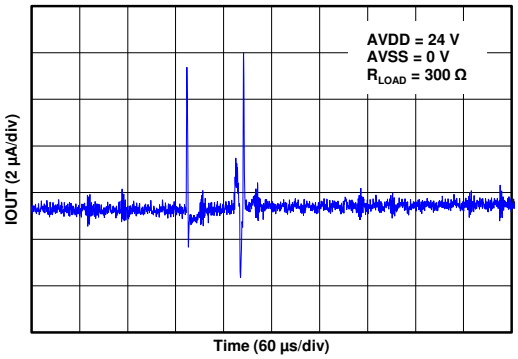


図 7-74. IOUT Power-On Glitch

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7.10 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

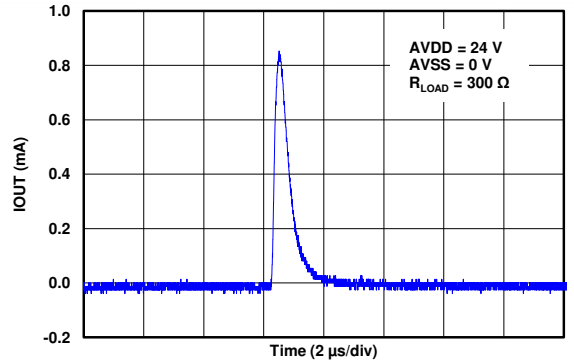


図 7-75. IOUT Output Enable Glitch

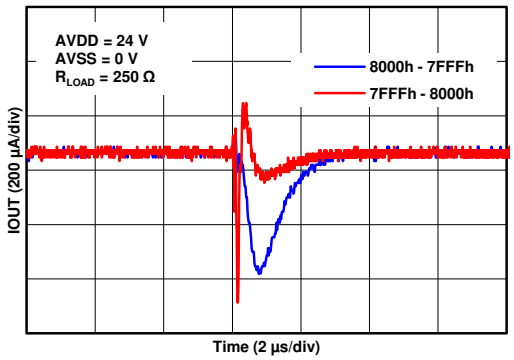


図 7-76. IOUT Digital-to-Analog Glitch

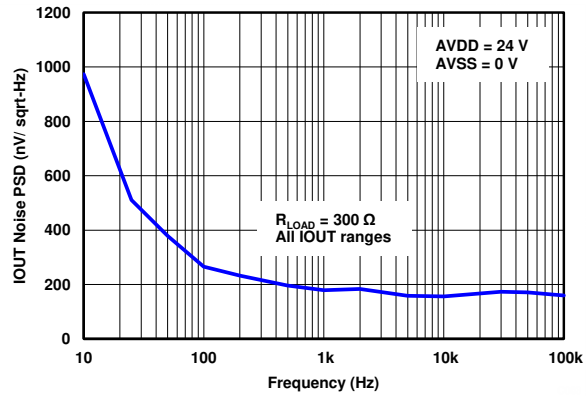


図 7-77. IOUT Noise PSD vs Frequency

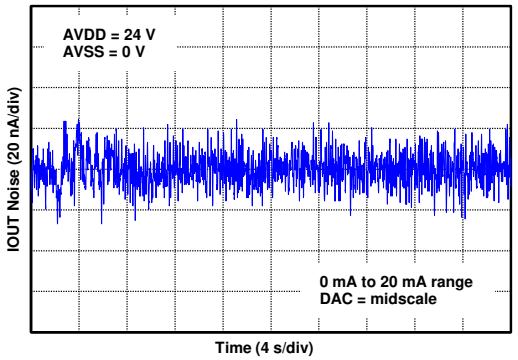


図 7-78. IOUT Peak-to-Peak Noise vs Time (0.1 Hz to 10 Hz)

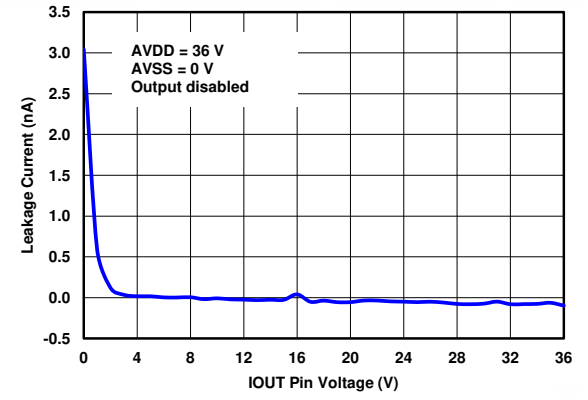


図 7-79. IOUT Hi-Z Leakage Current vs Voltage

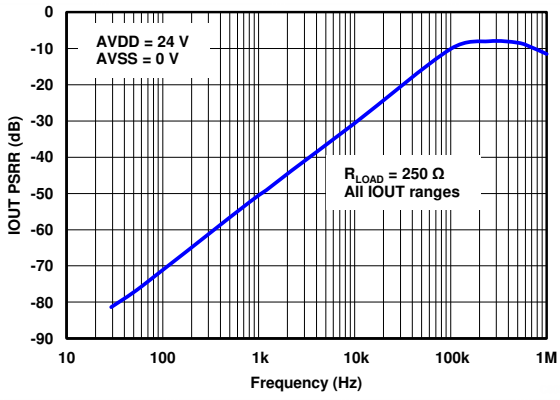


図 7-80. IOUT PSRR vs Frequency

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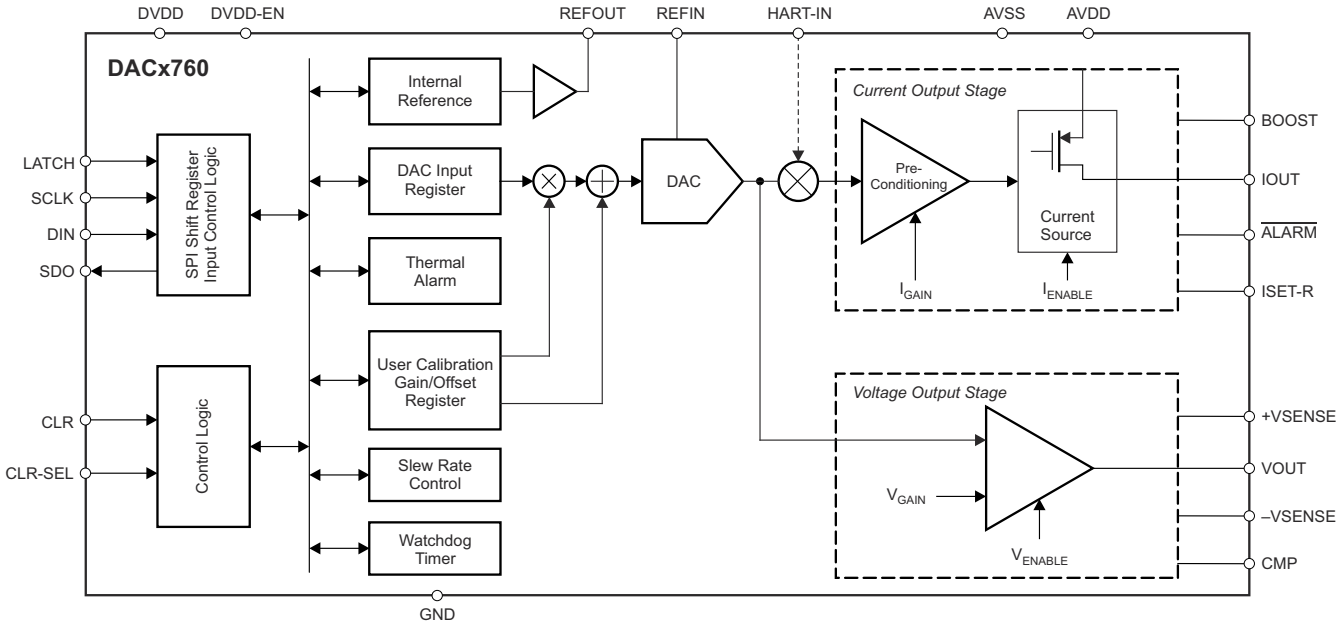
8 Detailed Description

8.1 Overview

The DAC8760 and DAC7760 are low-cost, precision, fully-integrated, 16-bit an 12-bit digital-to-analog converters (DACs) designed to meet the requirements of industrial process control applications. These devices can be programmed as a current output with a range of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA; or as a voltage output with a range of 0 V to 5 V, 0 V to 10 V, ±5 V, or ±10 V, with a 10% overrange (0 V to 5.5 V, 0 V to 11 V, ±5.5 V, or ±11 V). Both current and voltage outputs can be simultaneously enabled while being controlled by a single data register.

These devices include a power-on-reset function to ensure powering up in a known state (both IOUT and VOUT are disabled and in a high-impedance state). The CLR and CLR-SEL pins set the voltage outputs to zero-scale or mid-scale, and the current output to the low-end of the range, if the output is enabled. Zero code error and gain error calibration registers can be programmed to digitally calibrate the device in the end system. The output slew rate is also programmable. These devices can AC couple an external HART signal on the current output and can operate with either a single 10-V to 36-V supply, or dual supplies up to ±18 V.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 DAC Architecture

The DAC8760 and DAC7760 (DACx760) consist of a resistor-string digital-to-analog converter (DAC) followed by a buffer amplifier. The output of the buffer drives the current output and the voltage output. The resistor-string section is simply a string of resistors, each of value *R*, from REF to GND, as 図 8-1 illustrates. This type of architecture makes sure the DAC is monotonic. The 16-bit binary digital code (DAC8760) loaded to the DAC register determines at which node on the string the voltage is tapped off before it is fed into the output amplifier.

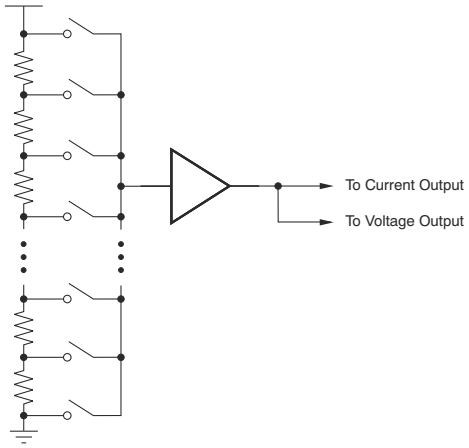


図 8-1. DAC Structure: Resistor String

The current-output stage converts the voltage output from the string to current. The voltage output provides a buffered output of the programmed range to the external load. When the current output or the voltage output is disabled, it is in a high impedance (Hi-Z) state. After power-on, both output stages are disabled. See *セクション 9.1.1* for different options to configure the current and voltage output pins.

8.3.2 Voltage Output Stage

The voltage output stage as conceptualized in 図 8-2 provides the voltage output according to the DAC code and the output range setting. The output range can be programmed as 0 V to 5 V or 0 V to 10 V for unipolar output mode, and ±5 V or ±10 V for bipolar output mode. In addition, an option is available to increase the output voltage range by 10%. The output current drive can be up to 10 mA. The output stage has short-circuit current protection that limits the output current to 30 mA. To maintain proper performance, a minimum 0.5-V power-supply headroom is required. The voltage output is able to drive a capacitive load up to 1 µF. For loads greater than 20 nF, to keep the output voltage stable at the expense of reduced bandwidth and increased settling time, connect an external compensation capacitor between CMP and VOUT. If an external compensation capacitor greater than 470 pF is used, connect an additional 100-pF capacitor from CMP to GND.

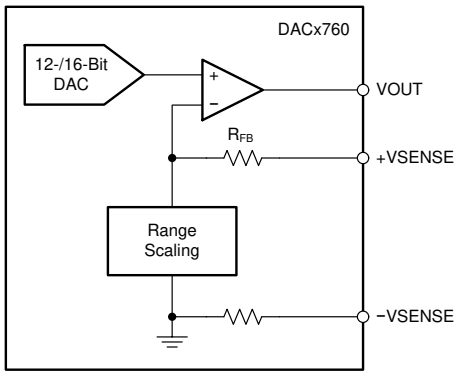


図 8-2. Voltage Output

The +VSENSE pin is provided to enable sensing of the load by connecting to points electrically closer to the load. This configuration allows the internal output amplifier to make sure that the correct voltage is applied across the load, as long as headroom is available on the power supply. Ideally, this pin is used to correct for resistive drops on the system board and is connected to VOUT at the pins. In some cases, both VOUT and +VSENSE are brought out as pins and, through separate lines, connected remotely together at the load. In case the +VSENSE line is cut, use an optional 5-kΩ resistor between VOUT and +VSENSE to prevent the amplifier loop from breaking. The –VSENSE pin, on the other hand, is provided as a GND sense reference output from the internal VOUT amplifier. The output swing of the VOUT amplifier is relative to the voltage seen at this pin. The actual voltage difference between the –VSENSE pin and the device GND pins is not expected to be more than a few 100 µV. The internal resistor in 図 8-2 between the device internal GND and the –VSENSE pin is typically 2 kΩ.

After power on, the power-on-reset circuit makes sure that all registers are at their default values. Therefore, the voltage output buffer is in a Hi-Z state; however, the +VSENSE pin connects to the amplifier inputs through an internal 60-kΩ feedback resistor (R_{FB} in 図 8-2). If the VOUT and +VSENSE pins are connected together, the VOUT pin is also connected to the same node through the feedback resistor. This node is protected by internal circuitry and settles to a value between GND and the reference input.

The output voltage (VOUT) can be expressed as 式 1 and 式 2.

For unipolar output mode:

$$VOUT = VREF \bullet GAIN \bullet \frac{CODE}{2^N} \quad (1)$$

For bipolar output mode:

$$VOUT = VREF \bullet GAIN \bullet \frac{CODE}{2^N} - GAIN \bullet \frac{VREF}{2} \quad (2)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760
- VREF is the reference voltage; for internal reference, VREF = 5 V
- *GAIN* is automatically selected for a desired voltage output range as shown in 表 8-1

表 8-1. Voltage Output Range vs Gain Setting(1)

VOLTAGE OUTPUT	GAIN
0 V to 5 V	1
0 V to 10 V	2
±5 V	2
±10 V	4

(1) VREF = 5 V

The voltage range is set according to the value of the RANGE bits and the OVR bit in the *Control Register*. The OVR bit makes the gain value in 表 8-1 increase by 10%, thereby increasing the voltage output range, as shown in 表 8-8 (see *セクション 8.4.1* for more details).

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8.3.3 Current Output Stage

The current output stage consists of a preconditioner and a current source as conceptualized in 図 8-3. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA to 20 mA, 0 mA to 24 mA, or 4 mA to 20 mA. An external boost transistor can be used to reduce the power dissipation of the device. The maximum compliance voltage on pin IOUT equals (AVDD – 2 V). In single power-supply mode, the maximum AVDD is 36 V, and the maximum compliance voltage is 34 V. After power on, the IOUT pin is in a Hi-Z state.

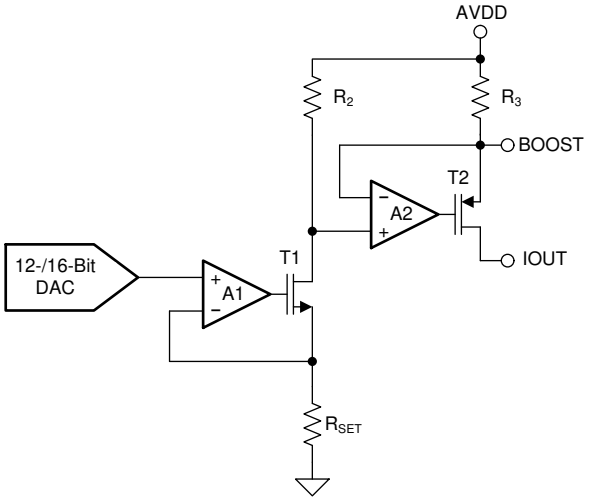


図 8-3. Current Output

Resistor R_{SET} (used to convert the DAC voltage to current) determines the stability of the output current over temperature. If desired, an external, low-drift, precision 15-kΩ resistor can be connected to the ISET-R pin and used instead of the internal R_{SET} resistor.

For a 5-V reference, the output can be expressed as shown in 式 3 through 式 5.

For a 0-mA to 20-mA output range:

$$IOUT = 20mA \bullet \frac{CODE}{2^N} \quad (3)$$

For a 0-mA to 24-mA output range:

$$IOUT = 24mA \bullet \frac{CODE}{2^N} \quad (4)$$

For a 4-mA to 20-mA output range:

$$IOUT = 16mA \bullet \frac{CODE}{2^N} + 4mA \quad (5)$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.

The current-output range is normally set according to the value of the RANGE bits in the *Control Register*. When both the voltage and current outputs are enabled in dual-output mode, the range is set by the IOUT RANGE bits in the *Configuration Register*. See *セクション 8.4.1* for more details. For more details on controlling the current output when both the VOUT and IOUT pins are simultaneously enabled, see *セクション 9.1.1*.

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8.3.4 Internal Reference

The DACx760 includes an integrated 5-V reference with a buffered output (REFOUT) capable of driving up to 5 mA (source or sink) with an initial accuracy of ±5 mV (maximum) and a temperature drift coefficient of 10 ppm/°C (maximum).

8.3.5 Digital Power Supply

An internally generated 4.6-V supply capable of driving up to 10 mA can be output on DVDD by leaving the DVD-EN pin unconnected. This configuration simplifies the system power-supply design especially when an isolation barrier is required to cross and generate the digital supply. The internally generated supply can be used to drive isolation components used for the digital data lines and other miscellaneous components like references and temp sensors. See 図 9-6 for an example application. If an external supply is preferred, the DVDD pin (which can be driven up to 5.5 V in this case) can be made into an input by tying DVDD-EN to GND (see *セクション 7.5* for detailed specifications).

8.3.6 DAC Clear

The DAC has an asynchronous clear function through the CLR pin, which is active-high and allows the voltage output to be cleared to either zero-scale code or midscale code. This action is user-selectable through the CLR-SEL pin or the CLRSEL bit of 表 8-17, as 表 8-2 describes. The CLR-SEL pin and CLRSEL register are ORed together. The current output clears to the bottom of its preprogrammed range. When the CLR signal returns to low, the output remains at the cleared value. The pre-clear value can be restored by pulsing the LATCH signal without clocking any data. A new value cannot be programmed until the CLR pin returns to low. Note that in dual-output mode, the value that the DAC data register is cleared to follows the settings for the voltage output mode.

表 8-2. CLR-SEL Options

CLR-SEL	OUTPUT VALUE	
	UNIPOLAR OUTPUT RANGE	BIPOLAR OUTPUT RANGE
0	0 V	0 V
1	Midscale	Negative full-scale

In addition to defining the output value for a clear operation, the CLRSEL bit and the CLR-SEL pin also define the default output value. During the selection of a new voltage range, the output value corresponds to the definitions given in 表 8-7. To avoid glitches on the output, disable the output by writing a *0* to the OUTEN bit of 表 8-17 before changing the voltage range. When the OUTEN bit is set to *1*, the output goes to the default value as defined by the CLRSEL bit and the CLR-SEL pin.

8.3.7 Power-On Reset

The DACx760 incorporates two internal POR circuits for the DVDD and AVDD supplies. The DVDD and AVDD POR signals are ANDed together so that both supplies must be at their minimal specified values for the device to *not* be in a reset condition. These POR circuits initialize internal logic and registers as well as set the analog outputs to a known state while the device supplies are ramping. All registers are reset to their default values with the default value of the data register being determined by the CLR-SEL pin. The behavior of IOUT and VOUT is described in their respective sections. Typically the POR function can be ignored as long as the device supplies power up and maintain the specified minimum voltage levels. However, in the case of supply drop or brownout, the DACx760 can have an internal POR reset event or lose digital memory integrity. 図 8-4 represents the threshold levels for the internal POR for both the DVDD and AVDD supplies.

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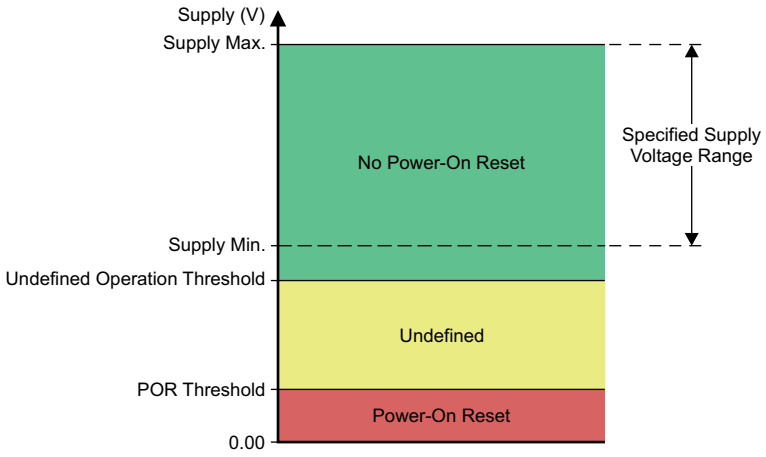


図 8-4. Relevant Voltage Levels for POR Circuit

For the DVDD supply, no internal POR occurs for nominal supply operation from 2.7 V (supply minimum) to 5.5 V (supply maximum). For the DVDD supply region between 2.4 V (undefined operation threshold) and 0.8 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the DVDD supply below 0.8 V (POR threshold), the internal POR resets as long as the supply voltage is below 0.8 V for approximately 1 ms.

For the AVDD supply, no internal POR occurs for nominal supply operation from 10 V (supply minimum) to 36 V (supply maximum). For AVDD supply voltages between 8 V (undefined operation threshold) to 1 V (POR threshold), the internal POR circuit may or may not provide a reset over all temperature conditions. For the AVDD supply below 1 V (POR threshold), the internal POR resets as long as the supply voltage is below 1 V for approximately 1 ms. In case the DVDD or AVDD supply drops to a level where the internal POR signal is indeterminate, either power cycle the device or toggle the LATCH pin followed by a software reset. Both options initialize the internal circuitry to a known state and provide proper operation.

8.3.8 Alarm Detection

The device also provides an alarm detection feature. When one or more of following events occur, the $\overline{\text{ALARM}}$ pin goes low:

- The current output load is in open circuit; or
- The voltage at IOUT reaches a level where the accuracy of the output current is compromised. This condition is detected by monitoring internal voltage levels of the IOUT circuitry and is typically below the specified compliance voltage headroom (defined as the voltage drop between the AVDD and IOUT pins) minimum of 2 V; or
- The die temperature has exceeded 142°C; or
- The SPI watchdog timer exceeded the timeout period (if enabled); or
- The SPI frame error CRC check encountered an error (if enabled).

When the $\overline{\text{ALARM}}$ pins of multiple DACx760 devices are connected together to form a wired-AND function, the host processor must read the status register of each device to know all the fault conditions that are present. Note that the thermal alarm has hysteresis of about 18°C. After being set, the alarm only resets when the die temperature drops below 124°C.

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8.3.9 Watchdog Timer

This feature is useful to make sure that communication between the host processor and the DACx760 has not been lost. Enable the watchdog timer by setting the WDEN bit of the *Configuration Register* to *1*. The watchdog timeout period can be set using the WDPD bits of the configuration register; see 表 8-3. The timer period is based off an internal oscillator with a typical value of 8 MHz.

表 8-3. Watchdog Timeout Period

WDPD BITS	WATCHDOG TIMEOUT PERIOD (Typical, ms)
00	10 ms
01	51 ms
10	102 ms
11	204 ms

If enabled, the chip must have an SPI frame with 0x95 as the write address byte written to the device within the programmed timeout period. Otherwise, the $\overline{\text{ALARM}}$ pin asserts low and the WD-FLT bit of the status register is set to *1*. The $\overline{\text{ALARM}}$ pin can be asserted low for any of the different conditions, as explained in *セクション 8.3.8*. To reset the WD-FLT bit to *0*, use a software reset, disable the watchdog timer, or power down the device.

8.3.10 Frame Error Checking

If the DACx760 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CRCEN bit of the *Configuration Register* to *1*. The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in 表 8-4. Start with the default 24-bit frame and enable frame error checking through the CRCEN bit and switch to the 32-bit frame. The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32-bit frame.

表 8-4. SPI Frame With Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

When in CRC mode, the DACx760 calculates CRC words every 32-clocks, unconditional of when the LATCH pin toggles. The DACx760 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the $\overline{\text{ALARM}}$ pin asserts low and the CRC-FLT bit of the status register is also set to 1. The $\overline{\text{ALARM}}$ pin can be asserted low for any of the different conditions, as explained in *セクション 8.3.8*. To reset the CRC-FLT bit to 0, use a software reset command of 0x96, disable the frame error checking, or power down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

If CRC mode is enabled on the first frame issued to the device after power up, issue a no operation (NOOP) command to the device to reset the SPI clock and SPI frame alignment in the event that any transients on the SCLK line are interpreted as SCLK periods. To issue a NOOP command to the device, simply toggle the LATCH pin without any SCLK periods.

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8.3.11 User Calibration

The device implements a user-calibration function to allow for trimming the system gain and zero errors. There is a gain calibration register and a zero calibration register; the DAC output is calibrated according to the value of these registers. The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The gain register must be programmed to a value of 0x8000 to achieve the default gain of 1 because the power-on value of the register is 0x0000, which is equivalent to a gain of 0.5. The zero code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the zero register is twos complement. The gain and offset calibration is described by 式 6.

$$CODE_OUT = CODE \bullet \frac{User_GAIN + 2^{15}}{2^{16}} + User_ZERO \tag{6}$$

where

- *CODE* is the decimal equivalent of the code loaded to the DAC data register at address 0x01.
- *N* is the bits of resolution; 16 for DAC8760 and 12 for DAC7760.
- *User_ZERO* is the signed 16-bit code in the zero register.
- *User_GAIN* is the unsigned 16-bit code in the gain register.
- *CODE_OUT* is the decimal equivalent of the code loaded to the DAC (limited between 0x0000 to 0xFFFF for DAC8760 and 0x000 to 0xFFF for DAC7760).

This implementation is purely digital and the output is still limited by the programmed value at both ends of the voltage or current output range. In addition, remember that the correction only makes sense for endpoints inside of the true device end points. To correct more than just the actual device error (for example, a system offset), the valid range for the adjustment changes accordingly and must be taken into account. This range is set by the RANGE, OVR, DUAL OUTEN, and IOUT RANGE bits, as described in *セクション 8.4.1*.

New calibration codes are only applied to subsequent writes of the DAC data register. Updating the calibration codes does not automatically update the DAC output. Additionally, before applying new DAC data, configure the calibration codes along with the slew rate control.

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8.3.12 Programmable Slew Rate

The slew rate control feature controls the rate at which the output voltage or current changes. With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

To reduce the slew rate, enable the slew rate control feature through bit 4 of 表 8-17. With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [7:5] (SRSTEP) and bits [11:8] (SRCLK) of the control register. SRCLK defines the rate at which the digital slew updates; SRSTEP defines the amount by which the output value changes at each update. If the DAC data register is read while the DAC output is still changing, the instantaneous value is read. 表 8-5 lists the slew rate step-size options. 表 8-6 summarizes the slew rate update clock options.

表 8-5. Slew Rate Step-Size (SRSTEP) Options

SRSTEP	STEP SIZE (LSB)	
	DAC7760	DAC8760
000	0.0625	1
001	0.125	2
010	0.25	4
011	0.5	8
100	1	16
101	2	32
110	4	64
111	8	128

表 8-6. Slew Rate Update Clock (SRCLK) Options

SRCLK	DAC UPDATE FREQUENCY (Hz)
0000	258,065
0001	200,000
0010	153,845
0011	131,145
0100	115,940
0101	69,565
0110	37,560
0111	25,805
1000	20,150
1001	16,030
1010	10,295
1011	8,280
1100	6,900
1101	5,530
1110	4,240
1111	3,300

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The time required for the output to slew over a given range can be expressed as 式 7:

$$\text{Slew Time} = \frac{\text{Output Change}}{\text{Step Size} \cdot \text{Update Clock Frequency} \cdot \text{LSB Size}} \quad (7)$$

where

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for IOUT or volts (V) for VOUT

When the slew rate control feature is enabled, all output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. To verify that the slew operation has completed, read Bit 1 (SR-ON) of the *Status Register*. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range. 図 8-5 illustrates an example of IOUT slewing at a rate set by the previously described parameters. In this example for the DAC8760 (LSB size of 305 nA for the 0-mA to 20-mA range), the settings correspond to an update clock frequency of 6.9 kHz and a step size of 128 LSB. As shown for the case with no capacitors on CAP1 or CAP2, the steps occur at the update clock frequency (6.9 kHz corresponds to a period close to 150 µs) and the size of each step is about 38 µA (128 × 305 nA). The slew time for a specific code change can be calculated using 式 7.

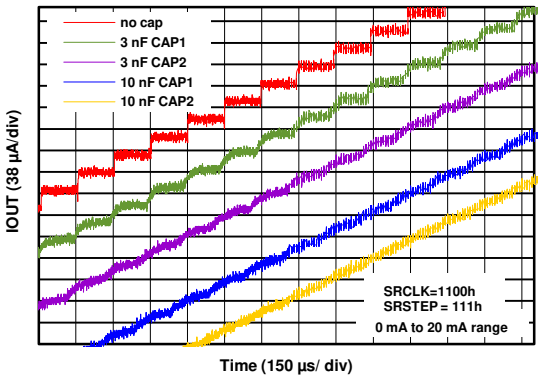


図 8-5. IOUT vs Time With Digital Slew Rate Control

Apply the desired programmable slew rate control setting prior to updating the DAC data register because updates to the DAC data register in tandem with updates to the slew rate control registers can create race conditions that may result in unexpected DAC data.

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8.4 Device Functional Modes

8.4.1 Setting Voltage and Current Output Ranges

For voltage and current outputs in normal mode (VOUT and IOUT are not simultaneously enabled), the output range is set according to 表 8-7.

表 8-7. RANGE Bits vs Output Range

RANGE	OUTPUT RANGE
000	0 V to +5 V
001	0 V to +10 V
010	±5 V
011	±10 V
100	Not allowed(1)
101	4 mA to 20 mA
110	0 mA to 20 mA
111	0 mA to 24 mA

(1) RANGE bits cannot be programmed to 0x100. Previous value is held when this command is written.

Note that changing the RANGE bits at any time causes the DAC data register to be cleared based on the value of CLR-SEL (pin or register bit) and the new value of the RANGE bits.

In addition to the RANGE bits, the OVR bit extends the voltage output range by 10%. if the OVR bit is set, the voltage output range follows 表 8-8, as long as there is headroom with the supply.

表 8-8. Voltage Output Overrange

VOLTAGE OUTPUT RANGE	VOLTAGE OUTPUT OVERRANGE
0 V to 5 V	0 V to 5.5 V
0 V to 10 V	0 V to +11 V
±5 V	±5.5 V
±10 V	±11 V

When VOUT and IOUT are simultaneously enabled (dual-output mode) by setting DUAL OUTEN in the *Configuration Register*, the voltage output is controlled by RANGE in the *Control Register* (see 表 8-9), and the current output is controlled by IOUT RANGE in the *Configuration Register* (see 表 8-10).

表 8-9. RANGE Bits vs Voltage Output Range in Dual-Output Mode

RANGE	OUTPUT RANGE
000	0 V to +5 V
001	0 V to +10 V
010	±5 V
011	±10 V
100	Not allowed(1)
1xx	Disabled

(1) RANGE bits cannot be programmed to 0x100. Previous value is held when this command is written.

表 8-10. IOUT RANGE Bits vs Current Output Range in Dual-Output Mode

RANGE	OUTPUT RANGE
00	Disabled
01	4 mA to 20 mA
10	0 mA to 20 mA
11	0 mA to 24 mA

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8.4.2 Boost Configuration for IOUT

An external NPN transistor can be used as shown in 図 8-6 to reduce power dissipation on the die. Most of the load current flows through the NPN transistor with a small amount flowing through the on-chip PMOS transistor based on the gain of the NPN transistor. This reduces the temperature induced drift on the die and internal reference and is an option for use cases at the extreme end of the supply, load current, and ambient temperature ranges. Resistor R_2 stabilizes this circuit for cases where the R_{LOAD} is a short or a very small load like a multimeter. Recommended values for R_1, R_2 and C_1 in this circuit are 1 kΩ, 20 Ω and 0.22 µF. An equivalent solution is to place R_2 (with a recommended value of 2 kΩ instead of the 20 Ω) in series with the base of the transistor instead of the configuration shown in 図 8-6. Note that there is some gain error introduced by this configuration as seen in 図 7-46 for the 0-mA to 24-mA range. TI recommends using the internal transistor in most cases as the values in セクション 7.5 are based on the configuration with the internal on-chip PMOS transitor.

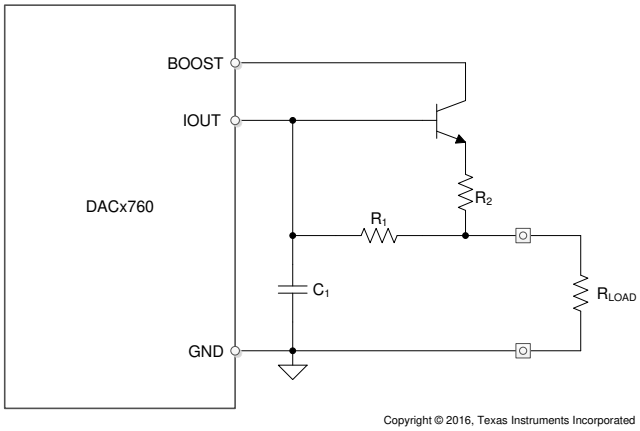


図 8-6. Boost Mode Configuration

8.4.3 Filtering the Current Output (only on the VQFN package)

The VQFN package provides access to internal nodes of the circuit as shown in 図 9-3. Capacitors can be placed on these pins and AVDD to form a filter on the output current, reducing bandwidth and the slew rate of the output. However, to achieve large reductions in slew rate, the programmable slew rate can be used to avoid having to use large capacitors. Even in that case, the capacitors on CAP1 and CAP2 can be used to smooth out the stairsteps caused by the digital code changes as shown in 図 8-7. However, note that power supply ripple also couples into the part through these capacitors.

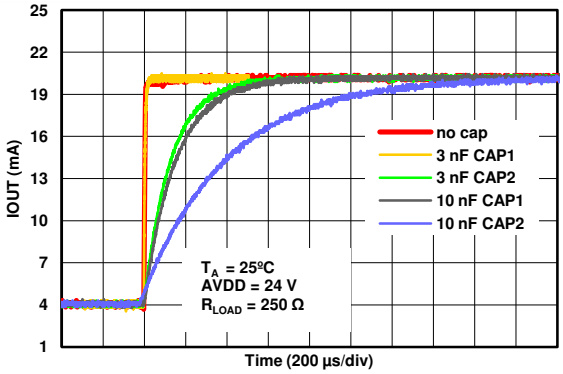


図 8-7. IOUT vs Time for Different Capacitor Values on CAP1 and CAP2

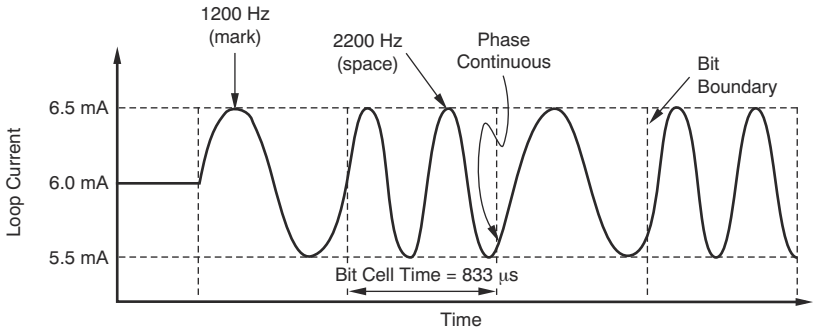
8.4.4 HART Interface

On the DACx760, HART digital communication can be modulated onto the input signal by two methods:

8.4.4.1 For 4-mA to 20-mA Mode

This method is limited to the case where the RANGE bits of 表 8-17 are programmed to the 4-mA to 20-mA range. Some applications require going beyond the 4-mA to 20-mA range. In those cases, see second method described in this section.

The external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz and 2200 Hz) can be capacitively coupled in through the HART-IN pin and transferred to a current that is superimposed on the 4-mA to 20-mA current output. The HART-IN pin has a typical input impedance of 35 kΩ that together with the input capacitor used to couple the external HART signal forms a filter to attenuate frequencies beyond the HART band-pass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. 図 8-8 illustrates the output current versus time operation for a typical HART signal.



NOTE: DC current = 6 mA.

図 8-8. Output Current vs Time

表 8-11 specifies the performance of the HART-IN pin.

表 8-11. HART-IN Pin Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input impedance	HART signal ac-coupled into pin		35		kΩ
Output current (peak-to-peak)	Input signal of 500 mV (peak-to-peak)	0.9	1	1.1	mA

8.4.4.2 For All Current Output Modes

The use of the HART-IN pin to implement HART modulation is limited to the case where the RANGE bits of 表 8-17 are set to the 4-mA to 20-mA range. To implement HART in all current-output modes, see *セクション 9.1.2*.

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8.5 Programming

8.5.1 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDI, SDO, SCLK, and LATCH) that operates at clock rates of up to 30 MHz and is compatible with SPI, QSPI, Microwire, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits. The timing for the digital interface is shown in 図 7-1 and 図 7-2.

8.5.1.1 SPI Shift Register

The default frame is 24 bits wide (see *セクション 8.3.10* for 32-bit frame mode) and begins with the rising edge of SCLK that clocks in the MSB. The subsequent bits are latched on successive rising edges of SCLK. The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in 表 8-12.

表 8-12. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

The host processor must issue 24 bits before it issues a rising edge on the LATCH pin. Input data bits are clocked in regardless of the LATCH pin and are unconditionally latched on the rising edge of LATCH. By default, the SPI shift register resets to 000000h at power on or after a reset.

8.5.1.2 Write Operation

A write operation is accomplished when the address byte is set according to 表 8-13. For more information on the DACx760 registers, see *セクション 8.6.1*.

表 8-13. Write Address Functions

ADDRESS BYTE	FUNCTION
0x00	No operation (NOP)
0x01	Write DAC Data register
0x02	Register read
0x55	Write control register
0x56	Write reset register
0x57	Write configuration register
0x58	Write DAC gain calibration register
0x59	Write DAC zero calibration register
0x95	Watchdog timer reset
0x96	CRC error reset

8.5.1.3 Read Operation

A read operation is accomplished when the address byte is 0x02. Follow the read operation with a no-operation (NOP) command to clock out an addressed register, as shown in 図 7-2. To read from a register, the address byte and data word is as shown in 表 8-14. The read register value is output MSB first on SDO on successive falling edges of SCLK.

表 8-14. Default SPI Frame for Register Read

ADDRESS BYTE	DATA WORD	
	BIT 15:BIT 6	BIT 5:BIT 0
0x02	X (*don't care*)	Register read address (see 表 8-15)

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表 8-15 shows the register read addresses available on the DACx760 devices.

表 8-15. Register Read Address Functions

READ ADDRESS(1)	FUNCTION
XX XX00	Read status register
XX XX01	Read DAC data register
XX XX10	Read control register
00 1011	Read configuration register
01 0011	Read DAC gain calibration register
01 0111	Read DAC zero calibration register

(1) X denotes *don't care* bits.

8.5.1.4 Stand-Alone Operation

SCLK can operate in either continuous or burst mode as long as the LATCH rising edge occurs after the appropriate number of SCLK cycles. Providing more than or less than 24 SCLK cycles before the rising edge of LATCH results in incorrect data being programmed into the device registers and incorrect data sent out on SDO. The rising edge of SCLK that clocks in the MSB of the 24-bit input frame marks the beginning of the write cycle, and data are written to the addressed registers on the rising edge of LATCH.

8.5.1.5 Multiple Devices on the Bus

Communication with the device is not directly gated by LATCH; therefore, do not connect multiple devices in parallel without gating SCLK. 図 8-9 shows two devices with SCLK gated for each device.

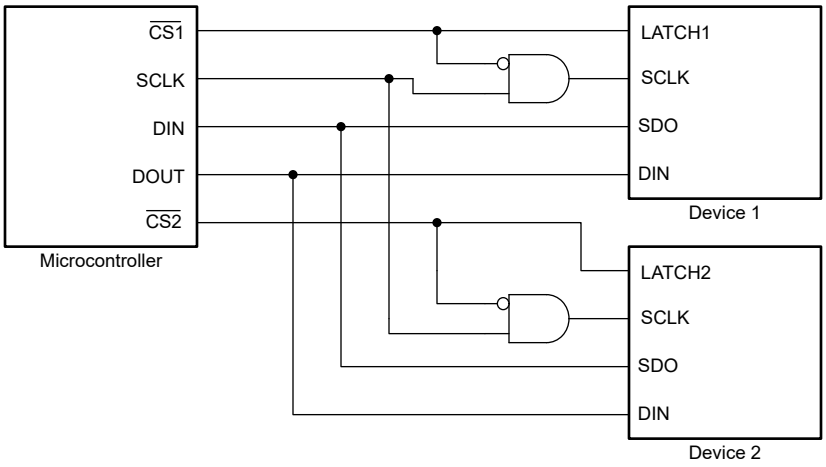


図 8-9. Multiple Devices on the Bus Using Gated SCLK

The microcontroller uses two chip select lines, one for each LATCH pin. Each line is used to gate the SCLK for communication for each device.

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8.6 Register Maps

8.6.1 DACx760 Command and Register Map

表 8-16 shows the available commands and registers on the DACx760 devices. *No operation*, *read operation*, *watchdog timer reset* and *CRC fault reset* refer to commands and are not explicit registers. For more information on these commands, see セクション 8.5.1.3, セクション 8.3.9, and セクション 8.3.10. See セクション 8.6.1.1 for descriptions of all DACx760 registers.

表 8-16. Command and Register Map

REGISTER COMMAND	READ/ WRITE ACCESS	DATA BITS (DB15:DB0)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control	R/W	CLRSEL	OVR	REXT	OUTEN	SRCLK				SRSTEP			SREN	Reserved	RANGE		
Configuration	R/W	X(1)					IOUT RANGE		DUAL OUTEN	APD	Reserved	CALEN	HARTEN	CRCEN	WDEN	WDPD	
DAC Data (2)	R/W	D15:D0															
No operation(3)	—	X															
Read Operation (3)	—	X										READ ADDRESS					
Reset	W	Reserved															RESET
Status	R	Reserved											CRC-FLT	WD-FLT	I-FLT	SR-ON	T-FLT
DAC Gain Calibration (2)	R/W	G15:G0, unsigned															
DAC Zero Calibration (2)	R/W	Z15:Z0, signed															
Watchdog Timer Reset (3)	—	X															
CRC Fault Reset (3)	—	X															

(1) X denotes *don't care* bits.
(2) DAC8760 (16-bit version) shown. DAC7760 (12-bit version) contents are located in DB15:DB4.
For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.
(3) *No operation*, *read operation*, *watchdog timer reset*, and *CRC fault reset* are commands and not registers.

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8.6.1.1 DACx760 Register Descriptions

8.6.1.1.1 Control Register

The DACx760 control register is written to at address 0x55. 表 8-17 shows the description for the control register bits.

表 8-17. Control Register 0x55

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15	CLRSEL	0	VOUT clear value select bit. When bit = *0*, VOUT is 0 V in セクション 8.3.6 mode or after reset. When bit = *1*, VOUT is midscale in unipolar output and negative-full-scale in bipolar output in セクション 8.3.6 mode or after reset.
DB14	OVR	0	Setting the bit increases the voltage output range by 10%.
DB13	REXT	0	External current setting resistor enable.
DB12	OUTEN	0	Output enable. Bit = *1*: Output is determined by RANGE bits. Bit = *0*: Output is disabled. IOUT and VOUT are *Hi-Z*.
DB11:DB8	SRCLK[3:0]	0000	Slew rate clock control. Ignored when bit SREN = *0*
DB7:DB5	SRSTEP[2:0]	000	Slew rate step size control. Ignored when bit SREN = *0*
DB4	SREN	0	Slew Rate Enable. Bit = *1*: Slew rate control is enabled, and the ramp speed of the output change is determined by SRCLK and SRSTEP. Bit = *0*: Slew rate control is disabled. Bits SRCLK and SRSTEP are ignored. The output changes to the new level immediately.
DB3	Reserved	0	Reserved. Must be set to 0.
DB2:DB0	RANGE[2:0]	000	Output range bits.

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8.6.1.1.2 Configuration Register

The DACx760 configuration register is written to at address 0x57. 表 8-18 summarizes the description for the configuration register bits.

表 8-18. Configuration Register 0x57

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB11		0h	Reserved. User must not write any value other than zero to these bits.
DB10:DB9	IOUT RANGE	00	IOUT range. These bits are only used if both voltage and current outputs are simultaneously enabled through bit 8 (DUAL OUTEN). The voltage output range is still controlled by bits 2:0 of the *Control Register* (RANGE bits). The current range is controlled by these bits and has similar behavior to RANGE[1:0] when RANGE[2] = *1*. However, unlike the RANGE bits, a change to this field does not make the DAC data register go to its default value.
DB8	DUAL OUTEN	0	DAC dual output enable. This bit controls if the voltage and current outputs are enabled simultaneously. Both are enabled when this bit is high. However, both outputs are controlled by the same DAC data register.
DB7	APD	0	Alternate power down. On power-up, +VSENSE is connected to the internal VOUT amplifier inverting pin. Diodes exist at this node to REFIN and GND. Setting this bit connects this node to ground through a resistor. When set, the equivalent resistance seen from +VSENSE to GND is 70 kΩ. This is useful in applications where the VOUT and IOUT pins are tied together.
DB6		0	Reserved. Do not write any value other than zero to these bits.
DB5	CALEN	0	User calibration enable. When user calibration is enabled, the DAC data are adjusted according to the contents of the gain and zero calibration registers. See *セクション 8.3.11*.
DB4	HARTEN	0	Enable interface through HART-IN pin (only valid for IOUT set to 4-mA to 20-mA range through RANGE bits). Bit = *1*: HART signal is connected through internal resistor and modulates output current. Bit = *0*: HART interface is disabled.
DB3	CRCEN	0	Enable frame error checking.
DB2	WDEN	0	Watchdog timer enable.
DB1:DB0	WDPD[1:0]	00	Watchdog timeout period.

8.6.1.1.3 DAC Registers

The DAC registers consist of a DAC data register (表 8-19), a DAC gain calibration register (表 8-20), and a DAC zero calibration register (表 8-21). User calibration as described in *セクション 8.3.11* is a feature that allows for trimming the system gain and zero errors. 表 8-19 through 表 8-21 show the DAC8760, 16-bit version of these registers. The DAC7760 (12-bit version) register contents are located in DB15:DB4. For DAC7760, DB3:DB0 are *don't care* bits when writing and zeros when reading.

表 8-19. DAC Data Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	D15:D0	0000h	DAC data register. Format is unsigned straight binary.

表 8-20. DAC Gain Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	G15:G0	0000h	Voltage and current gain calibration register for user calibration. Format is unsigned straight binary.

表 8-21. DAC Zero Calibration Register

DATA BITS	NAME	DEFAULT	DESCRIPTION
DB15:DB0	Z15:Z0	0000h	Voltage and current zero calibration register for user calibration. Format is twos complement.

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8.6.1.1.4 Reset Register

The DACx760 reset register is written to at address 0x56. 表 8-22 provides the description.

表 8-22. Reset Register 0x56

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB1		0000h	Reserved. Writing to these bits does not cause any change.
DB0	RESET	0	Software reset bit. Writing 1 to the bit performs a software reset to reset all registers and the $\overline{\text{ALARM}}$ status to the respective power-on reset default value. After reset completes the RESET bit clears itself.

8.6.1.1.5 Status Register

This read-only register consists of four $\overline{\text{ALARM}}$ status bits (CRC-FLT, WD-FLT, I-FLT, and T-FLT) and bit SR-ON that shows the slew rate status.

The device continuously monitors the output and die temperature. When an alarm occurs, the corresponding $\overline{\text{ALARM}}$ status bit is set (*1*). Whenever an $\overline{\text{ALARM}}$ status bit is set, it remains set until the event that caused it is resolved. The $\overline{\text{ALARM}}$ bit can only be cleared by performing a software reset, or a power-on reset (by cycling power), or having the error condition resolved. These bits are reasserted if the ALARM condition continues to exist in the next monitoring cycle.

The $\overline{\text{ALARM}}$ bit goes to *0* when the error condition is resolved.

表 8-23. Status Register

DATA BIT(S)	NAME	DEFAULT	DESCRIPTION
DB15:DB5		000h	Reserved. Reading these bits returns 0.
DB4	CRC-FLT	0	Bit = *1* indicates CRC error on SPI frame. Bit = *0* indicates normal operation.
DB3	WD-FLT	0	Bit = *1* indicates watchdog timer timeout. Bit = *0* indicates normal operation.
DB2	I-FLT	0	Bit = *1* indicates *Open Circuit* or *Compliance Voltage Violation* in IOUT loading. Bit = *0* indicates IOUT load is at normal condition.
DB1	SR-ON	0	Bit = *1* when DAC code is slewing as determined by SRCLK and SRSTEP. Bit = *0* when DAC code is not slewing.
DB0	T-FLT	0	Bit = *1* indicates die temperature is over 142°C. Bit = *0* indicates die temperature is not over 142°C.

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9 Application and Implementation

Note

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9.1 Application Information

9.1.1 Controlling the VOUT and IOUT Pins

This section describes how to control the VOUT and IOUT pins for three use cases:

9.1.1.1 VOUT and IOUT Pins are Independent Outputs, Never Simultaneously Enabled

In most applications, VOUT and IOUT are not connected together. In addition, only one is enabled at a time or they are both powered down. In this configuration, bits 10 down to 7 of the *Configuration Register* must be set to 0000 (default value). Bits 2 down to 0 of the *Control Register* (RANGE bits) control VOUT and IOUT.

9.1.1.2 VOUT and IOUT Pins are Independent Outputs, Simultaneously Enabled

When VOUT and IOUT are independent outputs and simultaneously enabled, bit 8 of the *Configuration Register* (DUAL OUTEN) must be set to 1. Bits 2 down to 0 of the *Control Register* (RANGE bits) control VOUT and bits 10 down to 9 of the *Configuration Register* (IOUT RANGE) control IOUT. Note that only one DAC code register exists and therefore the voltage and current outputs are controlled by the same code. Note that changing the RANGE bits at any time causes the DAC data register to be cleared based on the value of the CLR-SEL pin or CLRSEL register bit and the new value of the RANGE bits.

9.1.1.3 VOUT and IOUT Pins are Tied Together, Never Simultaneously Enabled

When the VOUT and IOUT pins are tied together, bit 8 of the *Configuration Register* (DUAL OUTEN) must be set to 0. Bits 2 down to 0 of the *Control Register* (RANGE) control VOUT and IOUT. Special consideration must be paid to the +VSENSE pin in this case. When VOUT is disabled, the +VSENSE pin is connected to the internal amplifier input through an internal 60-kΩ resistor as shown in 図 8-2. This internal node has diode clamps to REFIN and GND. Setting bit 6 of the *Configuration Register* (APD) forces this internal node to be tied to GND through a 10-kΩ resistor, in effect, the +VSENSE pin is tied to GND through a 70-kΩ power-down resistor. 図 9-1 shows the leakage current into the +VSENSE pin for both settings of the APD bit.

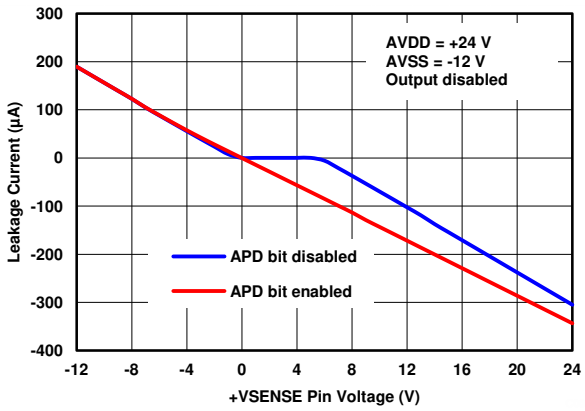


図 9-1. +VSENSE Leakage Current vs Pin Voltage

Whether the APD bit is set or not set, the current output in this case incurs a gain error because the internal resistor acts as a parallel load in addition to the external load. If this gain error is undesirable, it can be corrected through the gain calibration register shown in 表 8-20. Another option is to use the application circuit in 図 9-2.

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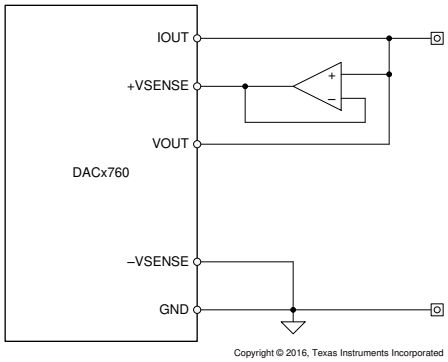


図 9-2. VOUT and IOUT Tied Together to One Pin

The buffer amplifier prevents leakage through the internal 60-kΩ resistor in current output mode and does not allow it to be seen as a parallel load. The VOUT pin is in high impedance mode in this case and allows minimal leakage current. Note that the offset of the external amplifier adds to the overall VOUT offset error and any potential phase shift from the external amplifier can cause VOUT stability issues.

9.1.2 Implementing HART in All Current Output Modes

If it is desirable to implement HART irrespective of the RANGE bit settings, there are two ways to do this.

9.1.2.1 Using CAP2 Pin on VQFN Package

The first method of implementing HART is to couple the signal through the CAP2 pin, as conceptualized in 図 9-3. Note that this pin is only available in the 40-pin VQFN package.

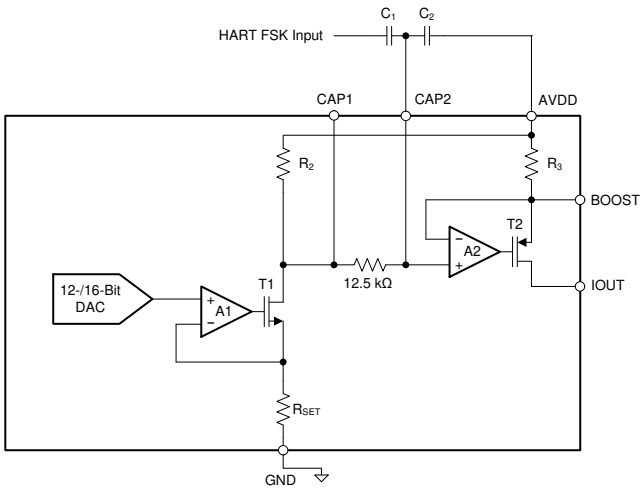


図 9-3. Implementing HART on IOUT Using the CAP2 Pin

In 図 9-3, R_3 is nominally 40 Ω, and R_2 is dependent on the current output range (set by the RANGE bits) as described below:

- 4-mA to 20-mA range: R_2 = 2.4 kΩ typical
- 0-mA to 20-mA range: R_2 = 3 kΩ typical
- 0-mA to 24-mA range: R_2 = 3.6 kΩ typical

The purpose of the 12.5-kΩ resistor is to create a filter when CAP1 and CAP2 are used.

To insert the external HART signal on the CAP2 pin, an external ac-coupling capacitor is typically connected to CAP2. The high-pass filter 3-dB frequency would be determined by the resistive impedance looking into CAP2 (R_2 + 12.5 kΩ) and the coupling capacitor value. The 3-dB frequency would be 1 /(2 × π × [R_2 + 12.5 kΩ] × [Coupling Cap Value]).

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After the input HART frequency is greater than the 3-dB frequency, the ac signal is seen at the plus input of amplifier A2 and would therefore be seen across the 40-Ω resistor. To generate a 1-mA signal on the output would therefore require a 40-mV peak-to-peak signal on CAP2. Because most HART modems do not output a 40-mV signal, a capacitive divider is used in the above circuit to attenuate the FSK signal from the modem. In the above circuit, the high-pass cutoff frequency would be 1 / (2 × π × [R_2+12.5 kΩ] × [C_1 + C_2]). There is one disadvantage of this approach: if the AVDD supply was not clean, any ripple on it could couple into the part.

9.1.2.2 Using the ISET-R Pin

The second method to implement HART is to couple the HART signal through the ISET-R pin when IOUT is operated using an external R_{SET} resistor. The FSK signal from the modem is ac coupled into the pin through a series combination of Rin and Cin as shown in 図 9-4.

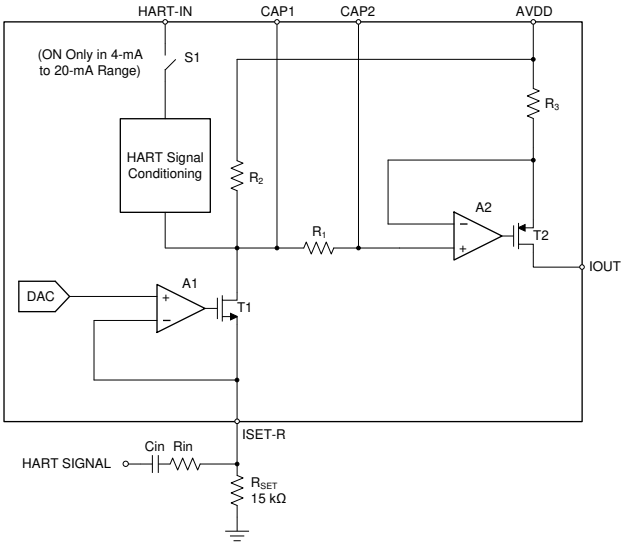


図 9-4. Implementing HART With the ISET-R pin

The magnitude of the ac current output is calculated as (V_{HART} × k) / Rin, where k is a constant that represents the gain transfer function from the ISET-R pin to the IOUT pin and depends on the selected current output range as follows: k = 60 for the 4-mA to 20-mA range, 75 for the 0-mA to 20-mA range, and 90 for the 0-mA to 24-mA range. The series input resistor and capacitor form a high-pass filter at the ISET-R pin and Cin must be selected to make sure that all signals in the HART extended-frequency band pass through unattenuated.

9.1.3 Short-Circuit Current Limiting

The DACx760 voltage output includes an internal circuit to typically regulate the load current to about 30 mA. However, this parameter is not production tested or trimmed. Optionally, use an external current limiting circuit on VOUT. However, if the VOUT, IOUT and +VSENSE pins are tied together, this circuit must be placed in the VOUT path before the circuit is tied together to the other pins at the common pin. The nature of the current-limiting circuit depends on the application and load. An example of a unidirectional current limiter is shown in 図 9-5.

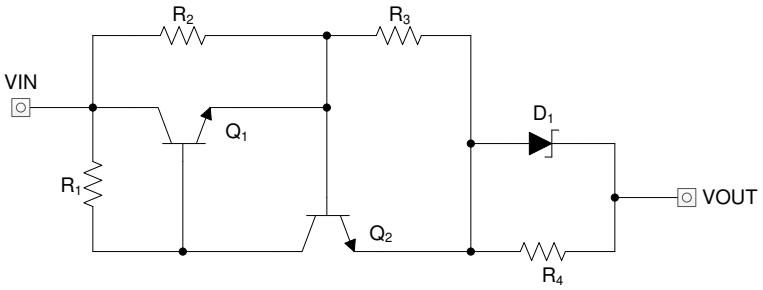


図 9-5. Unidirectional Current Limiter Circuit

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Under normal operation, most current in this circuit flows through Q1 and into R_3. As current increases through R_3, so does the voltage drop across R_3, which increases the base-emitter voltage of Q_2. Eventually the base-emitter voltage of Q_2 becomes high enough to turn on Q_2, which turns off Q_1 and reduce the current that can pass from VIN to VOUT. The value of R_3 sets the current limit. Be aware that this example is very simple and only applies for sourcing current into a resistive load. For cases involving both sourcing and sinking current as well as nonresistive loads, more complex circuits are required to achieve bidirectional current limiting.

9.2 Typical Application

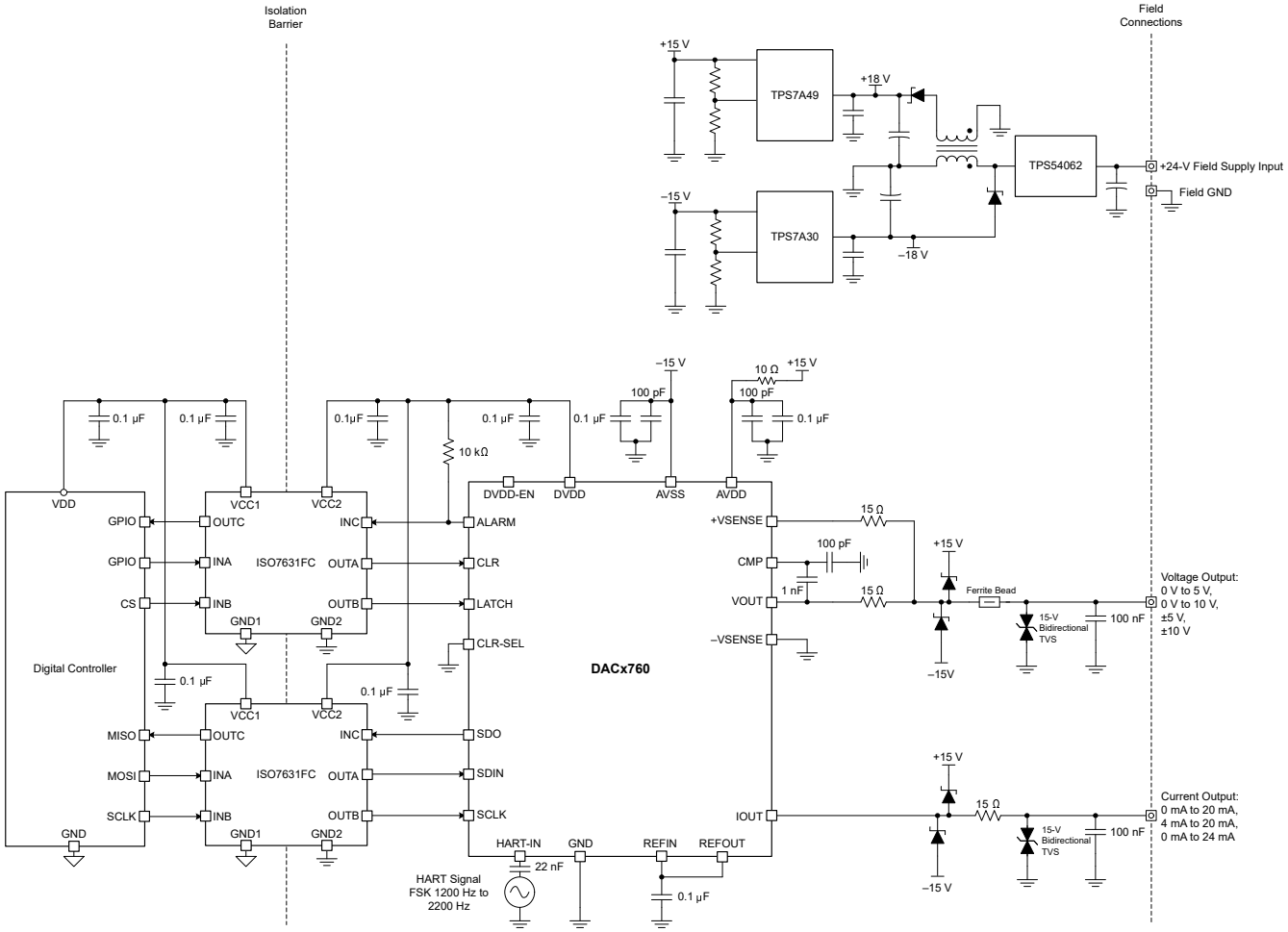


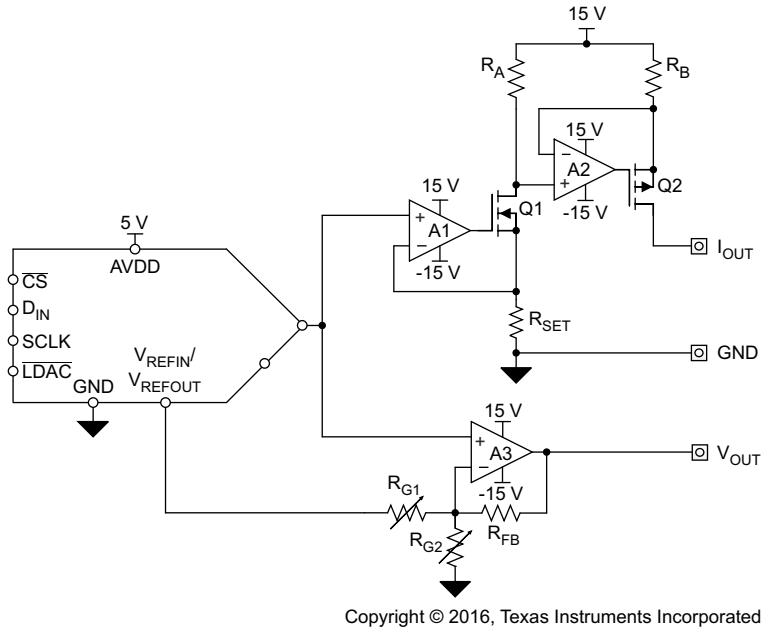
図 9-6. Voltage and Current Output Driver for Factory Automation and Control, EMC and EMI Protected - DACx760 in an Analog Output (AO) Module

9.2.1 Design Requirements

Analog I/O modules are used by programmable logic controllers (PLCs) and distributed control systems (DCSs) to interface to sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications for both performance as well as protection. These outputs are typically current loops based on the 4-mA to 20-mA range and derivatives or voltage outputs ranging from 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. Common error budgets accommodate 0.1% full-scale range total unadjusted error (% FSR TUE) at room temperature. Designs that desire stronger accuracy over temperature frequently implement calibration. Often times the PLC back-plane provides access to a 12-V to 36-V analog supply from which a majority of supply voltages are derived.

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9.2.2 Detailed Design Procedure



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図 9-7. Generic Design for Typical PLC Current and Voltage Outputs

図 9-7 illustrates a common generic solution for realizing these desired voltage and current output spans.

The current output circuit is comprised of amplifiers A1 and A2, MOSFETs Q1 and Q1, and the three resistors R_{SET}, R_A, and R_B. This two-stage current source enables the ground-referenced DAC output voltage to drive the high-side amplifier required for the current-source.

The voltage output circuit is composed of amplifier A3 and the resistor network consisting of R_{FB}, R_{G1}, and R_{G2}. A3 operates as a modified summing amplifier, where the DAC controls the noninverting input and the inverting input has one path to GND and a second to V_{REF}. This configuration allows the single-ended DAC to create both the unipolar 0-V to 5-V and 0-V to 10-V outputs and the bipolar ±5-V and ±10-V outputs by modifying the values of R_{G1} and R_{G2}.

図 9-6 generates clean ±15-V supplies using a synchronous step-down regulator (TPS54062) and two high-voltage, ultra-low noise, linear regulators (TPS7A49 and TPS7A30). A field supply terminal is shown instead of the more common use case of a back-plane supply. The design uses two triple channel isolators (ISO7631FC) to provide galvanic isolation for the digital lines to communicate to the main controller. Note that these isolators can be driven by the internally-generated supply (DVDD) from the DACx760 to save components and cost. The DACx760 supplies up to 10 mA that meets the supply requirements of the two isolators running at up to 10 Mbps. Note that additional cost savings are possible if noncritical digital signals such as CLR and ALARM are tied to GND or left unconnected. Finally, a protection scheme with transient voltage suppressors and other components is placed on all pins which connect to the field.

The protection circuitry is designed to provide immunity to the IEC61000-4 test suite which includes system-level industrial transient tests. The protection circuit includes transient voltage suppressor (TVS) diodes, clamp-to-rail steering diodes, and pass elements in the form of resistors and ferrite beads. For more detail about selecting these components, see TIPD153.

9.2.3 Application Curves

The current output circuit was measured in 0-mA to 24-mA mode using an 8.5 digit digital multi-meter to measure the output while driving a 300-Ω load at 25°C. The measured results are shown in 図 9-8. The voltage output circuit was measured in ±10-V mode using an 8.5 digit digital multi-meter to measure the output while driving a
1-kΩ load at 25°C. The measured results are shown in 図 9-9. In both cases, the voltage and current outputs remain within the specified performance of the data sheet.

The design was also exposed to IEC61000-4 electrostatic discharge, electrically fast transient, conducted immunity, and radiated immunity tests on both the current and voltage outputs. During each of these tests a 6.5 digit digital multi-meter, set in fast 5.5 digit acquisition mode, was used to monitor the outputs. Complete data sets for the voltage and current outputs during these tests are available in TIPD153.

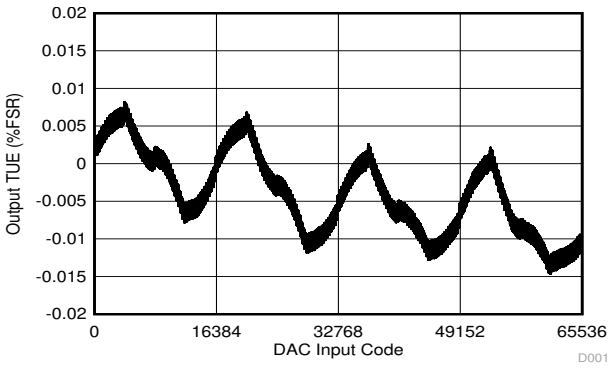


図 9-8. Voltage Output TUE Versus Code

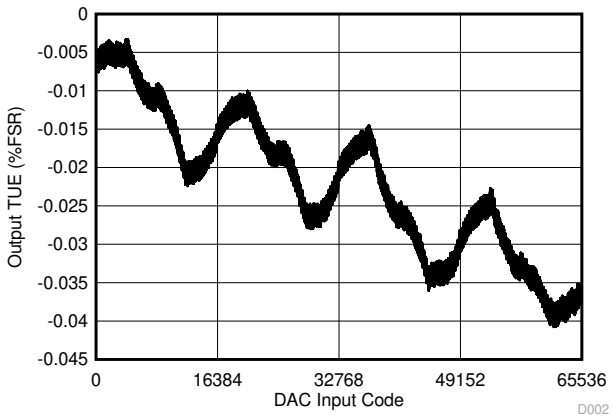


図 9-9. Current Output TUE Versus Code

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10 Power Supply Recommendations

The DACx760 family operates within the specified single-supply range of 10 V to 36 V applied to the AVDD pin. The device also operates with the specified dual-supply range of 10 V to 18 V applied to AVDD, and 0 V to –18 V on AVSS, or any subsequent combination that does not exceed the maximum difference of 36 V between AVDD and AVSS. The digital supply, DVDD, operates within the specified supply range of 2.7 V to 5.5 V or is powered by the internal 4.6-V LDO.

Switching power supplies and DC/DC converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high frequency spikes. This noise can be easily coupled into the DAC output voltage or current through various paths between the power connections and analog output. To further reduce noise, include bulk and local decoupling capacitors.

CAUTION

Do not ramp the supplies for the DACx760 faster than 1 V/ns or damage may result to the device. To help reduce the supply ramp, use a 10-Ω series resistor from the analog supply to the device AVDD connection.

The DACx760 has internal power-on reset (POR) circuitry for both the digital DVDD and analog AVDD supplies. This circuitry makes sure that the internal logic and power-on state of the DAC power up to the proper state independent of the supply sequence. The recommended power-supply sequence is to first have the analog AVDD supply come up, followed by the digital DVDD supply. DVDD can come up first as long as AVDD ramps to at least 5 V within 50 µs. If neither condition can be satisfied, issue a software reset command using the SPI bus after both AVDD and DVDD are stable.

The current consumption on the AVDD and AVSS pins, the short-circuit current limit for the voltage output, and current ranges for the current output are listed in *セクション 7.5*. The power supply must meet the requirements listed in *セクション 7.5*.

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11 Layout

11.1 Layout Guidelines

To maximize the performance of the DACx760 in any application, good layout practices and proper circuit design must be followed. A few recommendations specific to the DACx760 are:

1. As is seen in 図 9-3, CAP2 is directly connected to the input of the final IOUT amplifier. Any noise or unwanted ac signal routed near the CAP1 and/or CAP2 pins could capacitively couple onto internal nodes and affect IOUT. Therefore, with the QFN package, it is important to avoid routing any digital or HART signal trace over the CAP1 and CAP2 traces.
2. The thermal PAD must be connected to the lowest potential in the system.
3. The +VSENSE connection must be a low-impedance trace connected close to the point of load.
4. AVDD and AVSS must have decoupling capacitors local to the respective pins.
5. The reference capacitor must be placed close to the reference input pin.
6. Avoid routing switching signals near the reference input.
7. For designs that include protection circuits:
   a. Place diversion elements, such as TVS diodes or capacitors, close to off-board connectors to make sure that return current from high-energy transients does not cause damage to sensitive devices.
   b. Use large, wide traces to provide a low-impedance path to divert high-energy transients away from I/O terminals.

11.1.1 Thermal Considerations

The DACx760 is designed for a maximum junction temperature of +150°C. In cases where the maximum AVDD is driving maximum current into ground, this could be exceeded. Use the following equation, from *セクション 7.1*, to determine the maximum junction temperature that can be reached:

$$\text{Power Dissipation} = (T_{Jmax} - T_A)/\theta_{JA} \quad (8)$$

where

- T_{Jmax} = 150°C
- T_A is the ambient temperature
- θ_{JA} is the package dependent junction-to-ambient thermal resistance, which is found in *セクション 7.4*

The power dissipation can be calculated by multiplying all the supply voltages with the currents supplied, which is found in the *Power Requirements* subsection of *セクション 7.5*.

Consider an example: IOUT is enabled, supplying 24 mA into GND with a 25°C ambient temperature, AVDD of 24 V, AVSS is tied to GND and DVDD is generated internally. From the specifications table, the maximum value of AIDD = 3 mA when IOUT is enabled and DAC code = 0x0000. Also, the maximum value of DIDD = 1 mA. Accordingly, the worst case power dissipation is 24 V × (24 mA + 3 mA + 1 mA) = 672 mW. Using the $R_{\theta JA}$ value for the TSSOP package, we get T_{Jmax} = 25°C + (32.3 × 0.672)°C = 46.7°C. At 85°C ambient temperature, the corresponding value of T_{Jmax} is 106.7°C. Using this type of analysis, the system designer can both specify and design for the equipment operating conditions. Note that the thermal pad in both packages is recommended to be connected to a copper plane for enhanced thermal performance.

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11.2 Layout Example

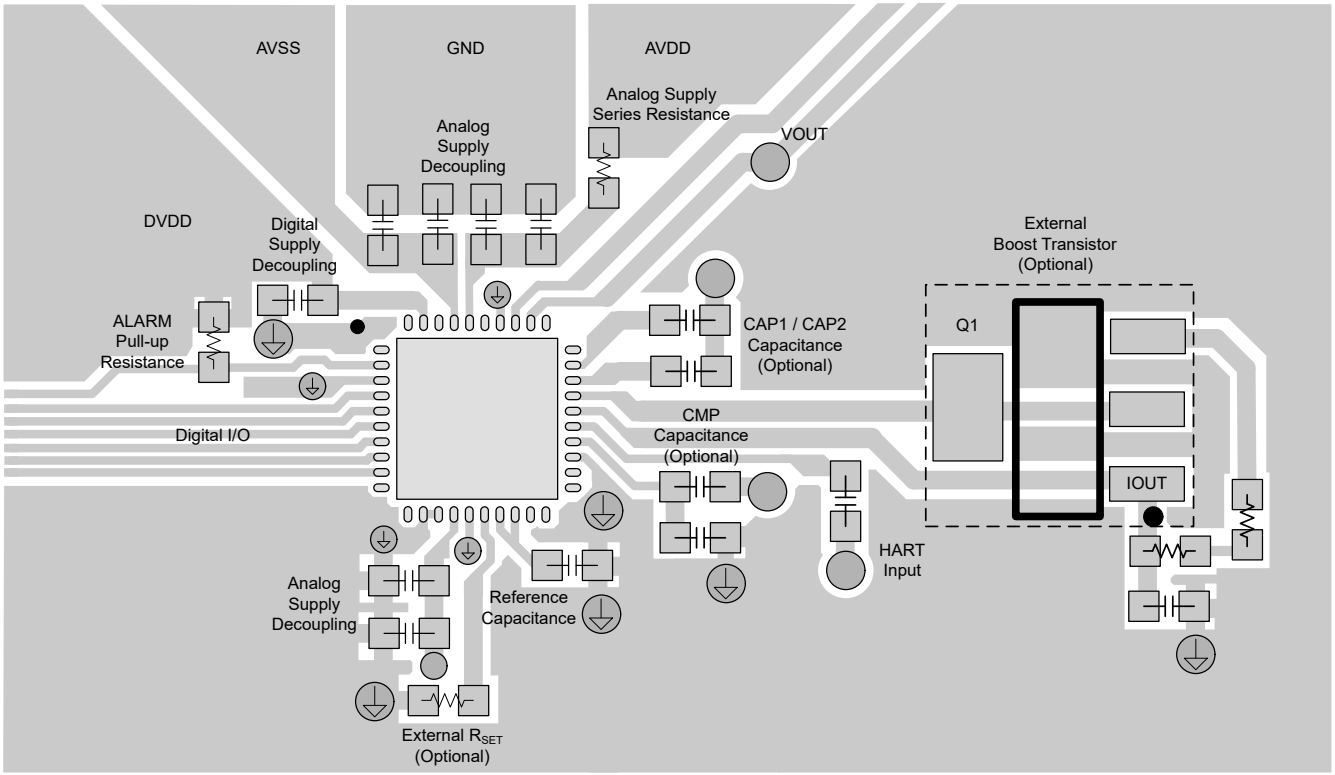


図 11-1. DACx760 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Single-Channel Industrial Voltage & Current Output Driver, Isolated, EMC/EMI Tested Reference Design*
- Texas Instruments, *Implementing HART™ Communication with the DAC8760 Family*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.4 Trademarks

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HART® is a registered trademark of HART Communication Foundation.
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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC7760IPWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWP.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPR.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPRG4	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPRG4.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IPWPRG4.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC7760IRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC7760
DAC8760IPWP	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWP.A	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWP.B	Active	Production	HTSSOP (PWP) | 24	60 | TUBE	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPR	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPR.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPR.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPRG4	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPRG4.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IPWPRG4.B	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAR	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAR.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAR.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHARG4	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHARG4.A	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8760IRHARG4.B	Active	Production	VQFN (RHA) | 40	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAT	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAT.A	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760
DAC8760IRHAT.B	Active	Production	VQFN (RHA) | 40	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	DAC8760

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

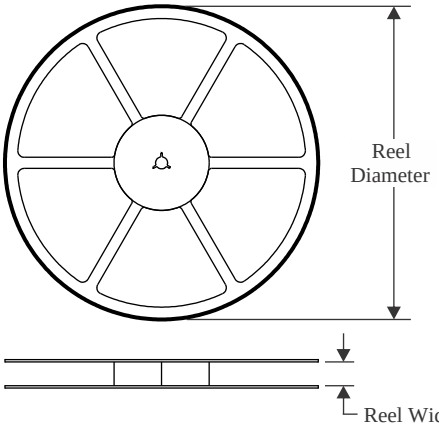
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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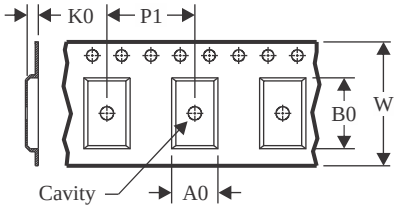
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

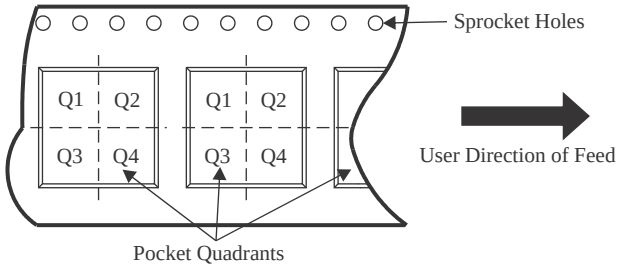


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

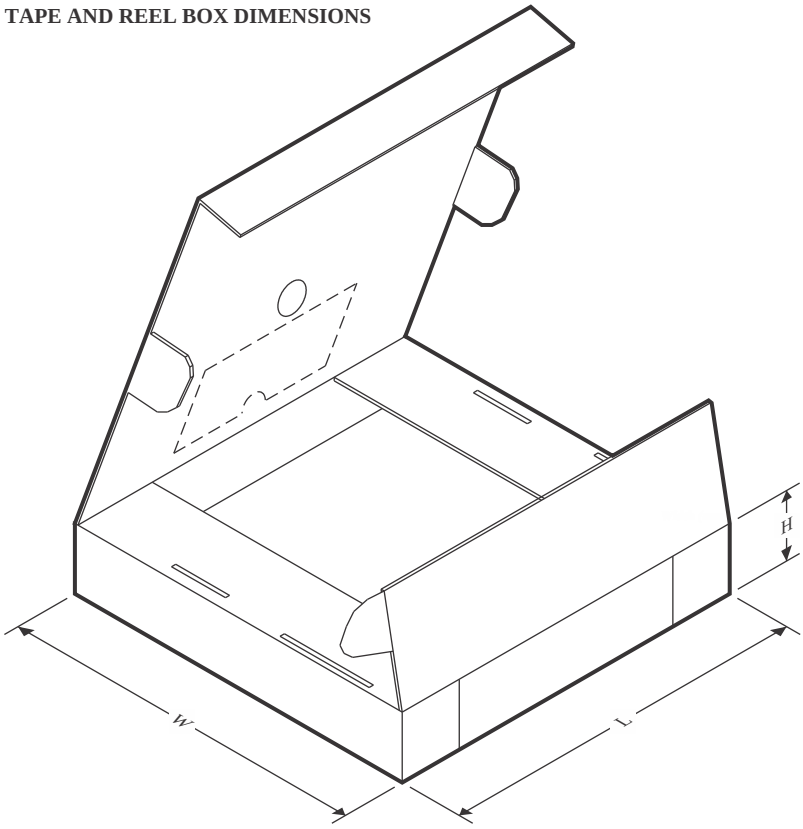
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7760IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC7760IPWPRG4	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC7760IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC7760IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8760IPWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8760IPWPRG4	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DAC8760IRHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8760IRHARG4	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DAC8760IRHAT	VQFN	RHA	40	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

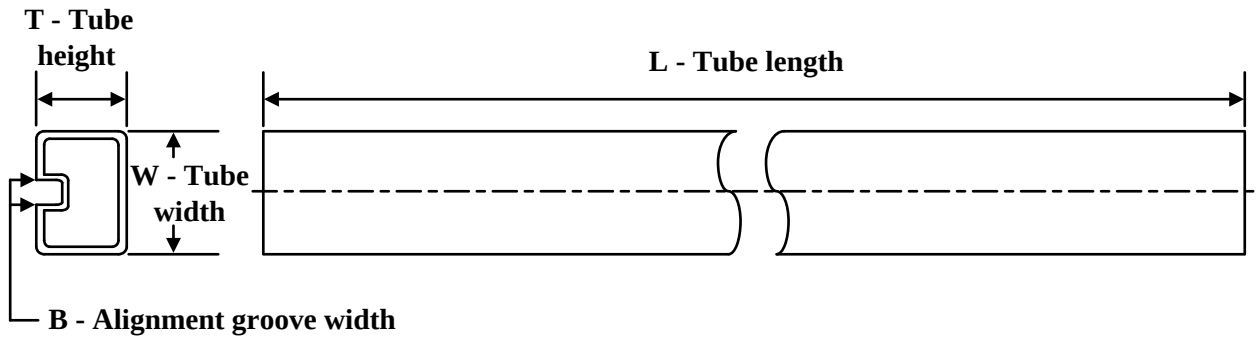
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7760IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC7760IPWPRG4	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC7760IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC7760IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0
DAC8760IPWPR	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC8760IPWPRG4	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DAC8760IRHAR	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8760IRHARG4	VQFN	RHA	40	2500	367.0	367.0	38.0
DAC8760IRHAT	VQFN	RHA	40	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7760IPWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC7760IPWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC7760IPWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8760IPWP	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8760IPWP.A	PWP	HTSSOP	24	60	530	10.2	3600	3.5
DAC8760IPWP.B	PWP	HTSSOP	24	60	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

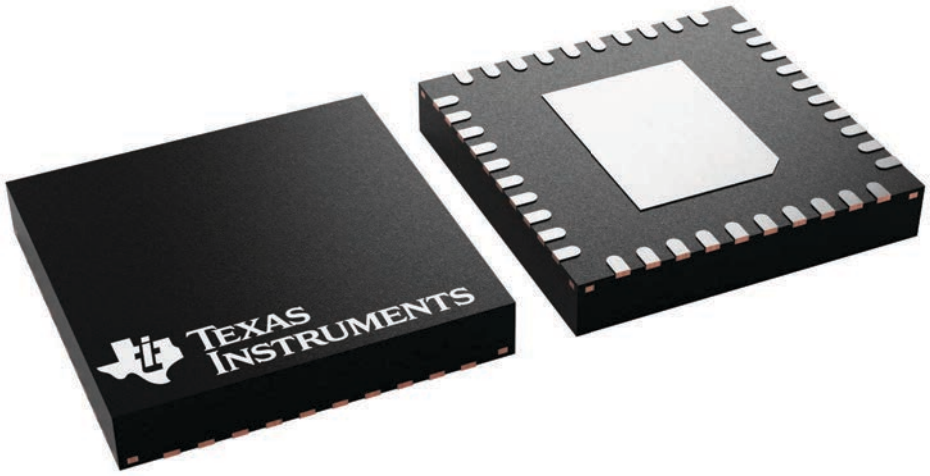
RHA 40

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225870/A

GENERIC PACKAGE VIEW

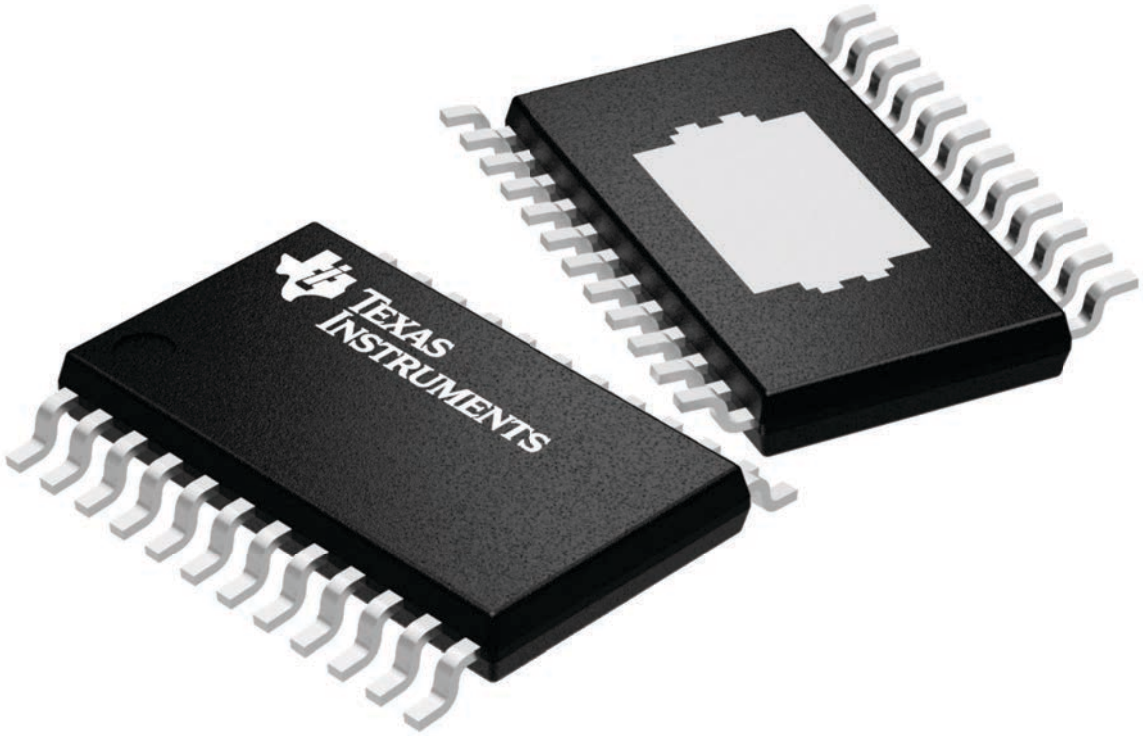
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

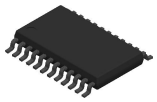
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

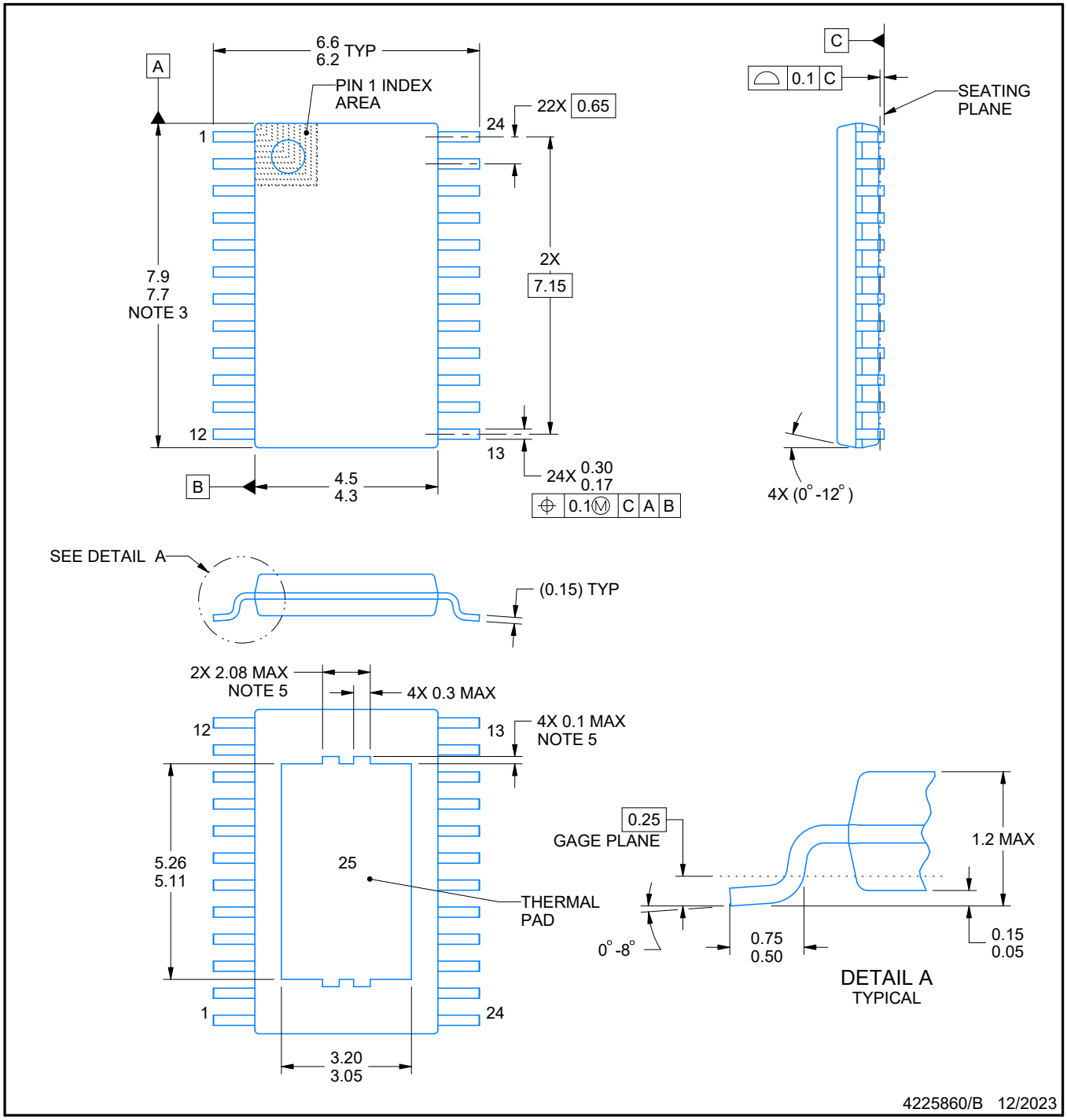
PACKAGE OUTLINE

PWP0024J



PowerPAD™ TSSOP - 1.2 mm max height

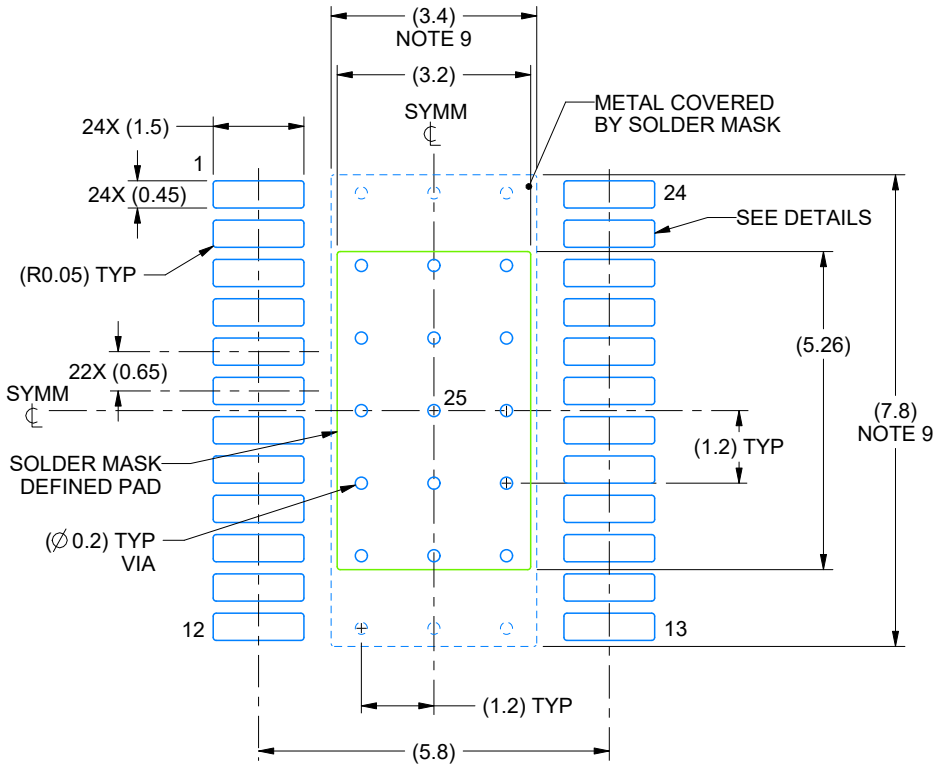
SMALL OUTLINE PACKAGE



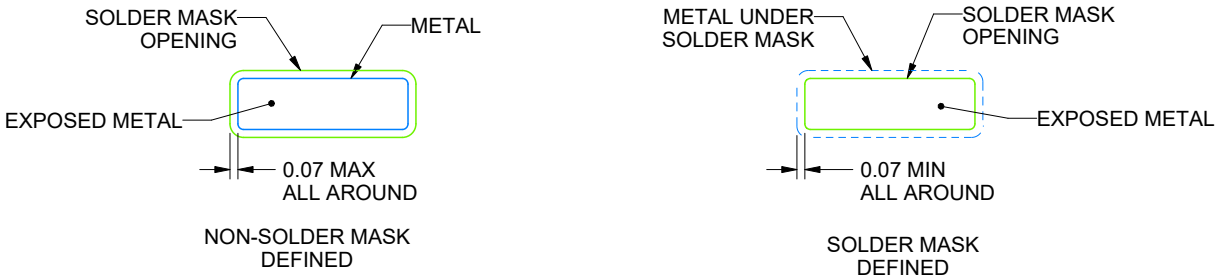
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

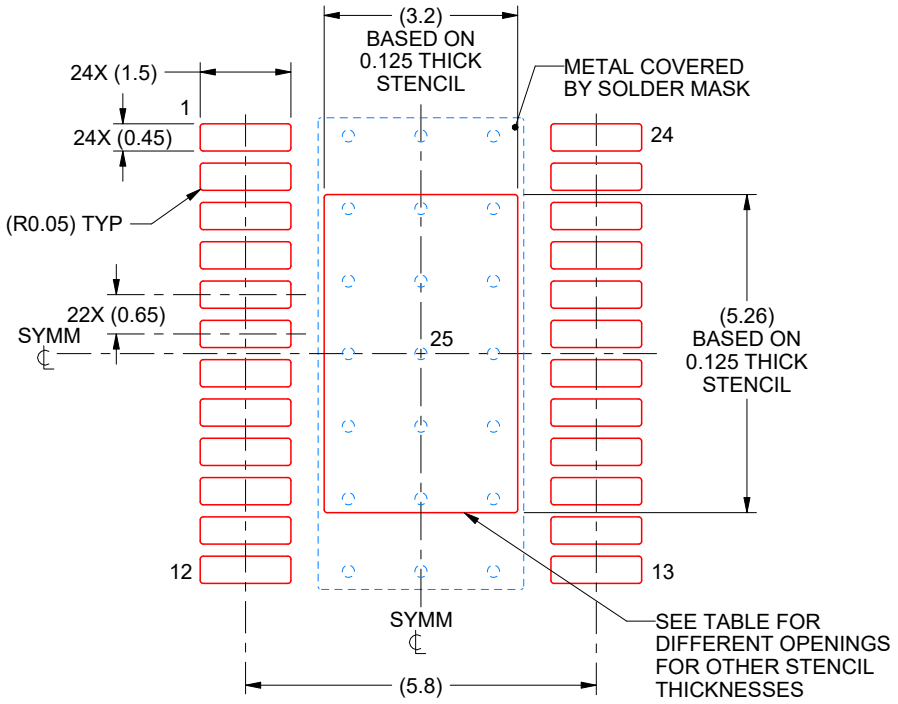


SOLDER MASK DETAILS

4225860/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

4225860/B 12/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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