# DLP230KP .23 HD デジタル・マイクロミラー・デバイス

## 1 特長

- 超小型 0.23 インチ (5.95mm) 対角マイクロミラー・アレイ
  - 画面に 1280 × 720 ピクセルを表示
  - マイクロミラー・ピッチ：5.4µm
  - マイクロミラー傾斜角：17° (水平面に対して)
  - 側面照明による最適な効率と光学エンジン・サイズ
  - 偏波無依存のアルミニウム製マイクロミラー表面
- 8 ビットの SubLVDS 入力データ・バス
- ディスプレイ・アプリケーション専用 DLPC3434 コントローラ
- 専用の DLPA2000、DLPA2005 または DLPA3000 PMIC/LED ドライバによる信頼性の高い動作

## 2 ディスプレイ・アプリケーション

- 超低消費電力、ウルトラモバイル・ピコ・プロジェクタ
- スマートフォン、タブレット、ノート PC
- スマート・スピーカ
- スマート・ホーム

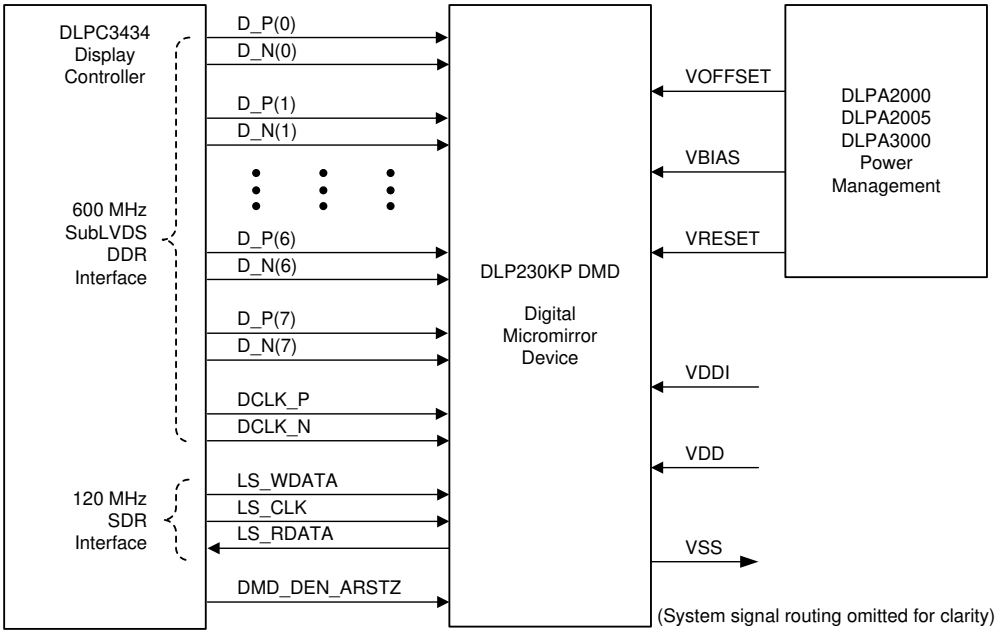
## 3 概要

DLP230KP デジタル・マイクロミラー・デバイス (DMD) は、デジタル制御の MOEMS (micro-opto-electromechanical system) 空間光変調器 (SLM) です。適切な光学システムと組み合わせることで、デバイス DMD は鮮明で高品質の HD 画像または映像を表示できます。このチップセットは、この DMD と DLPC3434 コントローラで構成されています。DLPA2000、DLPA2005、DLPA3000 PMIC/LED ドライバも、このチップセットをサポートします。このデバイスは物理的なサイズが小さいため、高画質、小さな外形、低消費電力が重要な携帯機器に使用できます。

**製品情報**

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|---|---|---|
| DLP230KP | FQP (54) | 16.8mm × 5.92mm × 3.58mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**アプリケーション概略図**

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

# Table of Contents

**1 特長** ... 1
**2 ディスプレイ・アプリケーション** ... 1
**3 概要** ... 1
**4 Revision History** ... 2
**5 Pin Configuration and Functions** ... 3
**6 Specifications** ... 6
6.1 Absolute Maximum Ratings ... 6
6.2 Storage Conditions ... 7
6.3 ESD Ratings ... 7
6.4 Recommended Operating Conditions ... 7
6.5 Thermal Information ... 9
6.6 Electrical Characteristics ... 9
6.7 Timing Requirements ... 10
6.8 Switching Characteristics ... 15
6.9 System Mounting Interface Loads ... 16
6.10 Micromirror Array Physical Characteristics ... 17
6.11 Micromirror Array Optical Characteristics ... 18
6.12 Window Characteristics ... 19
6.13 Chipset Component Usage Specification ... 19
**7 Detailed Description** ... 20
7.1 Overview ... 20
7.2 Functional Block Diagram ... 20
7.3 Feature Description ... 21
7.4 Device Functional Modes ... 21
7.5 Optical Interface and System Image Quality Considerations ... 21
7.6 Micromirror Array Temperature Calculation ... 22
7.7 Micromirror Power Density Calculation ... 23
7.8 Micromirror Landed-On/Landed-Off Duty Cycle ... 25
**8 Application and Implementation** ... 29
8.1 Application Information ... 29
8.2 Typical Application ... 30
**9 Power Supply Recommendations** ... 32
9.1 Power Supply Power-Up Procedure ... 32
9.2 Power Supply Power-Down Procedure ... 32
9.3 Power Supply Sequencing Requirements ... 33
**10 Layout** ... 35
10.1 Layout Guidelines ... 35
10.2 Layout Example ... 35
**11 Device and Documentation Support** ... 36
11.1 Device Support ... 36
11.2 Chipset Resources ... 36
11.3 ドキュメントの更新通知を受け取る方法 ... 36
11.4 サポート・リソース ... 37
11.5 Trademarks ... 37
11.6 静電気放電に関する注意事項 ... 37
11.7 用語集 ... 37
**12 Mechanical, Packaging, and Orderable Information** ... 38
12.1 Package Option Addendum ... 39

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision C (May 2022) to Revision D (July 2023) | Page |
|---|---|
| • Added "ILLUMINATION" to the *Recommended Operating Conditions* | 7 |
| • Updated *Micromirror Array Temperature Calculation* | 22 |
| • Added *Micromirror Power Density Calculation* | 23 |

| Changes from Revision B (April 2022) to Revision C (May 2022) | Page |
|---|---|
| • Updated Absolute Maximum Ratings disclosure to the latest TI standard | 6 |
| • Updated *Micromirror Array Optical Characteristics* | 18 |
| • Added *Third-Party Products Disclaimer* | 36 |


Copyright © 2023 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

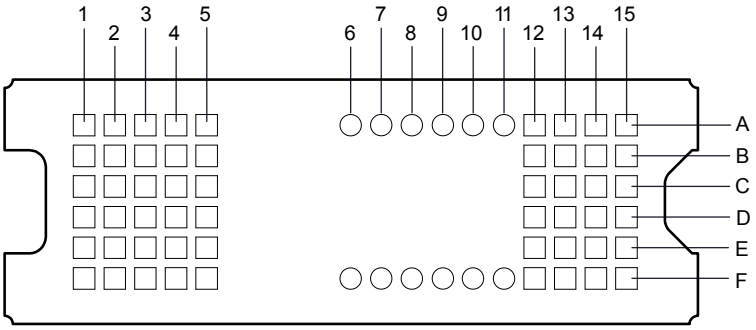



**図 5-1. FQP Package, 54-Pin CLGA (Bottom View)**

**表 5-1. Pin Functions – Connector Pins**

| PIN[1] | | TYPE | SIGNAL | DATA RATE | DESCRIPTION | PACKAGE NET LENGTH[2] (mm) |
|---|---|---|---|---|---|---|
| NAME | NO. | | | | | |
| **DATA INPUTS** | | | | | | |
| D_N(0) | A2 | I | SubLVDS | Double | Data, negative | 1.96 |
| D_N(1) | A1 | I | SubLVDS | Double | Data, negative | 1.42 |
| D_N(2) | C1 | I | SubLVDS | Double | Data, negative | 1.35 |
| D_N(3) | B4 | I | SubLVDS | Double | Data, negative | 3.36 |
| D_N(4) | F5 | I | SubLVDS | Double | Data, negative | 4.29 |
| D_N(5) | D4 | I | SubLVDS | Double | Data, negative | 3.20 |
| D_N(6) | E1 | I | SubLVDS | Double | Data, negative | 1.76 |
| D_N(7) | F3 | I | SubLVDS | Double | Data, negative | 2.66 |
| D_P(0) | A3 | I | SubLVDS | Double | Data, positive | 1.97 |
| D_P(1) | B1 | I | SubLVDS | Double | Data, positive | 1.49 |
| D_P(2) | C2 | I | SubLVDS | Double | Data, positive | 1.44 |
| D_P(3) | A4 | I | SubLVDS | Double | Data, positive | 3.45 |
| D_P(4) | E5 | I | SubLVDS | Double | Data, positive | 4.32 |
| D_P(5) | D5 | I | SubLVDS | Double | Data, positive | 3.27 |
| D_P(6) | E2 | I | SubLVDS | Double | Data, positive | 1.85 |
| D_P(7) | F2 | I | SubLVDS | Double | Data, positive | 2.75 |
| DCLK_N | C3 | I | SubLVDS | Double | Clock, negative | 1.94 |
| DCLK_P | D3 | I | SubLVDS | Double | Clock, positive | 2.02 |
| **CONTROL INPUTS** | | | | | | |
| LS_WDATA | A12 | I | LPSDR[1] | Single | Write data for low speed interface | 2.16 |
| LS_CLK | B12 | I | LPSDR | Single | Clock for low-speed interface | 3.38 |
| DMD_DEN_ARSTZ | B14 | I | LPSDR | Single | Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode. | 0.67 |
| DMD_DEN_ARSTZ | F1 | I | LPSDR | Single | | 14.90 |
| LS_RDATA | C13 | O | LPSDR | Single | Read data for low-speed interface | 2.44 |
| **POWER** | | | | | | |
| $V_{BIAS}$ [3] | A15 | Power | | | Supply voltage for positive bias level at micromirrors | |
| $V_{BIAS}$ [3] | A5 | Power | | | | |

Copyright © 2023 Texas Instruments Incorporated

**表 5-1. Pin Functions – Connector Pins (continued)**

| PIN[1] | | TYPE | SIGNAL | DATA RATE | DESCRIPTION | PACKAGE NET LENGTH[2] (mm) |
|---|---|---|---|---|---|---|
| NAME | NO. | | | | | |
| $V_{OFFSET}$ [3] | F13 | Power | | | Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes.<br>Supply voltage for offset level at micromirrors | |
| $V_{OFFSET}$ [3] | F4 | Power | | | | |
| $V_{RESET}$ | B15 | Power | | | Supply voltage for negative reset level at micromirrors | |
| $V_{RESET}$ | B5 | Power | | | | |
| $V_{DD}$ [3] | C15 | Power | | | Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes | |
| $V_{DD}$ | C5 | Power | | | | |
| $V_{DD}$ | D14 | Power | | | | |
| $V_{DD}$ | D15 | Power | | | | |
| $V_{DD}$ | E14 | Power | | | | |
| $V_{DD}$ | E15 | Power | | | | |
| $V_{DD}$ | F14 | Power | | | | |
| $V_{DD}$ | F15 | Power | | | | |
| $V_{DDI}$ | C14 | Power | | | Supply voltage for SubLVDS receivers | |
| $V_{DDI}$ | C4 | Power | | | | |
| $V_{DDI}$ | D13 | Power | | | | |
| $V_{DDI}$ | E13 | Power | | | | |
| $V_{SS}$ | A13 | Ground | | | Common return. Ground for all power | |
| $V_{SS}$ | A14 | Ground | | | | |
| $V_{SS}$ | B13 | Ground | | | | |
| $V_{SS}$ | B2 | Ground | | | | |
| $V_{SS}$ | B3 | Ground | | | | |
| $V_{SS}$ | C12 | Ground | | | | |
| $V_{SS}$ | D1 | Ground | | | | |
| $V_{SS}$ | D12 | Ground | | | | |
| $V_{SS}$ | D2 | Ground | | | | |
| $V_{SS}$ | E12 | Ground | | | | |
| $V_{SS}$ | E3 | Ground | | | | |
| $V_{SS}$ | E4 | Ground | | | | |
| $V_{SS}$ | F12 | Ground | | | | |

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)*. See JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQP ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 in/ns.
Propagation delay = 0.265 ns/inch = 265 ps/in = 10.43 ps/mm
(3) The following power supplies are all required to operate the DMD: $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, $V_{RESET}$. All $V_{SS}$ connections are also required.


Copyright © 2023 Texas Instruments Incorporated

**表 5-2. Pin Functions – Test Pads**

| NUMBER | SYSTEM BOARD |
|---|---|
| A6 | Do not connect. |
| A7 | Do not connect. |
| A8 | Do not connect. |
| A9 | Do not connect. |
| A10 | Do not connect. |
| A11 | Do not connect. |
| F6 | Do not connect. |
| F7 | Do not connect. |
| F8 | Do not connect. |
| F9 | Do not connect. |
| F10 | Do not connect. |
| F11 | Do not connect. |

Copyright © 2023 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted[1])

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | Supply voltage for LVCMOS core logic[2]<br>Supply voltage for LPSDR low speed interface | –0.5 | 2.3 | V |
| | $V_{DDI}$ | Supply voltage for SubLVDS receivers[2] | –0.5 | 2.3 | V |
| | $V_{OFFSET}$ | Supply voltage for HVCMOS and micromirror electrode[2] [3] | –0.5 | 11 | V |
| | $V_{BIAS}$ | Supply voltage for micromirror electrode[2] | –0.5 | 19 | V |
| | $V_{RESET}$ | Supply voltage for micromirror electrode[2] | –15 | 0.5 | V |
| | $\lvert V_{DDI}–V_{DD}\rvert$ | Supply voltage delta (absolute value)[4] | | 0.3 | V |
| | $\lvert V_{BIAS}–V_{OFFSET}\rvert$ | Supply voltage delta (absolute value)[5] | | 11 | V |
| | $\lvert V_{BIAS}–V_{RESET}\rvert$ | Supply voltage delta (absolute value)[6] | | 34 | V |
| Input voltage | Input voltage for other inputs LPSDR[2] | | –0.5 | $V_{DD}$ + 0.5 | V |
| | Input voltage for other inputs SubLVDS[2] [7] | | –0.5 | $V_{DDI}$ + 0.5 | V |
| Input pins | $\lvert V_{ID}\rvert$ | SubLVDS input differential voltage (absolute value)[7] | | 810 | mV |
| | $I_{ID}$ | SubLVDS input differential current | | 10 | mA |
| Clock frequency | $f_{clock}$ | Clock frequency for low speed interface LS_CLK | | 130 | MHz |
| | $f_{clock}$ | Clock frequency for high speed interface DCLK | | 620 | MHz |
| Environmental | $T_{ARRAY}$ and $T_{WINDOW}$ | Temperature – operational [8] | –20 | 90 | °C |
| | | Temperature – non-operational[8] | –40 | 90 | °C |
| | $\lvert T_{DELTA}\rvert$ | Absolute temperature delta between any point on the window edge and the ceramic test point TP1[9] | | 30 | °C |
| | $T_{DP}$ | Dew Point - operating and non-operating | | 81 | °C |

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminals ($V_{SS}$). The following power supplies are all required to operate the DMD: $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, and $V_{RESET}$. All $V_{SS}$ connections are also required.
(3) $V_{OFFSET}$ supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between $V_{DDI}$ and $V_{DD}$ may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between $V_{BIAS}$ and $V_{OFFSET}$ may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between $V_{BIAS}$ and $V_{RESET}$ may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated in セクション 7.6) or of any point along the window edge is defined in 図 7-1. The location of thermal test point TP2 in 図 7-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 図 7-1. The window test point TP2 shown in 図 7-1 is intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.


Copyright © 2023 Texas Instruments Incorporated

## 6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{DMD}$ | DMD storage temperature | –40 | 85 | °C |
| $T_{DP}$ | Average dew point temperature (non-condensing) (1) | | 24 | °C |
| $T_{DP-ELR}$ | Elevated dew point temperature range (non-condensing) (2) | 28 | 36 | °C |
| $CT_{ELR}$ | Cumulative time in elevated dew point temperature range | | 6 | months |

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of $CT_{ELR}$.

## 6.3 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **SUPPLY VOLTAGE RANGE**(3) | | | | | |
| $V_{DD}$ | Supply voltage for LVCMOS core logic<br>Supply voltage for LPSDR low-speed interface | 1.65 | 1.8 | 1.95 | V |
| $V_{DDI}$ | Supply voltage for SubLVDS receivers | 1.65 | 1.8 | 1.95 | V |
| $V_{OFFSET}$ | Supply voltage for HVCMOS and micromirror electrode(4) | 9.5 | 10 | 10.5 | V |
| $V_{BIAS}$ | Supply voltage for mirror electrode | 17.5 | 18 | 18.5 | V |
| $V_{RESET}$ | Supply voltage for micromirror electrode | –14.5 | –14 | –13.5 | V |
| $\lvert V_{DDI}–V_{DD}\rvert$ | Supply voltage delta (absolute value)(5) | | | 0.3 | V |
| $\lvert V_{BIAS}–V_{OFFSET}\rvert$ | Supply voltage delta (absolute value)(6) | | | 10.5 | V |
| $\lvert V_{BIAS}–V_{RESET}\rvert$ | Supply voltage delta (absolute value)(7) | | | 33 | V |
| **CLOCK FREQUENCY** | | | | | |
| $f_{clock}$ | Clock frequency for low speed interface LS_CLK(8) | 108 | | 120 | MHz |
| $f_{clock}$ | Clock frequency for high speed interface DCLK(9) | 300 | | 540 | MHz |
| | Duty cycle distortion DCLK | 44% | | 56% | |
| **SUBLVDS INTERFACE**(9) | | | | | |
| $\lvert V_{ID}\rvert$ | SubLVDS input differential voltage (absolute value). See 図 6-8, 図 6-9. | 150 | 250 | 350 | mV |
| $V_{CM}$ | Common mode voltage. See 図 6-8, 図 6-9. | 700 | 900 | 1100 | mV |
| $V_{SUBLVDS}$ | SubLVDS voltage. See 図 6-8, 図 6-9. | 575 | | 1225 | mV |
| $Z_{LINE}$ | Line differential impedance (PWB/trace) | 90 | 100 | 110 | Ω |
| $Z_{IN}$ | Internal differential termination resistance. See 図 6-10. | 80 | 100 | 120 | Ω |
| | 100-Ω differential PCB trace | 6.35 | | 152.4 | mm |

Copyright © 2023 Texas Instruments Incorporated

## 6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **ENVIRONMENTAL** | | | | | |
| $T_{ARRAY}$ | Array temperature – long-term operational(10) (11) (12) (13) | 0 | | 40 to 70(12) | °C |
| | Array temperature – short-term operational, 25 hr max(11) (14) | –20 | | –10 | °C |
| | Array temperature – short-term operational, 500 hr max(11) (14) | –10 | | 0 | °C |
| | Array temperature – short-term operational, 500 hr max(11) (14) | 70 | | 75 | °C |
| $T_{WINDOW}$ | Window temperature – operational(15) (16) | | | 90 | °C |
| $\lvert T_{DELTA} \rvert$ | Absolute temperature difference between any point on the window edge and the ceramic test point TP1(17) | | | 15 | °C |
| $T_{DP-AVG}$ | Average dew point temperature (non-condensing) (18) | | | 24 | °C |
| $T_{DP-ELR}$ | Elevated dew point temperature range (non-condensing) (19) | 28 | | 36 | °C |
| $CT_{ELR}$ | Cumulative time in elevated dew point temperature range | | | 6 | months |
| **ILLUMINATION** | | | | | |
| $ILL_{UV}$ | Illumination power at wavelengths < 410 nm(10) | | | 10 | mW/cm$^2$ |
| $ILL_{VIS}$ | Illumination power at wavelengths ≥ 410 nm and ≤ 800 nm(20) | | | 26.1 | W/cm$^2$ |
| $ILL_{IR}$ | Illumination power at wavelengths > 800 nm | | | 10 | mW/cm$^2$ |
| $ILL_{BLU}$ | Illumination power at wavelengths ≥ 410 nm and ≤ 475 nm(20) | | | 8.3 | W/cm$^2$ |
| $ILL_{BLU1}$ | Illumination power at wavelengths ≥ 410 nm and ≤ 445 nm(20) | | | 1.5 | W/cm$^2$ |
| $ILL_{\theta}$ | Illumination marginal ray angle(15) | | | 55 | deg |

(1) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(2) The following power supplies are all required to operate the DMD: $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, and $V_{RESET}$. All $V_{SS}$ connections are also required.
(3) All voltage values are with respect to the ground pins ($V_{SS}$).
(4) $V_{OFFSET}$ supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(7) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(8) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(9) Refer to the SubLVDS timing requirements in セクション 6.7.
(10) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 図 7-1 and the package thermal resistance using the calculation in セクション 7.6.
(12) Per 図 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to セクション 7.8 for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the usable life of the device.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including at the pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document and may negatively affect lifetime.
(16) Window temperature is the highest temperature on the window edge shown in 図 7-1. The location of thermal test point TP2 in 図 7-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 図 7-1. The window test point TP2 shown in 図 7-1 is intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of $CT_{ELR}$.
(20) The maximum allowable optical power incident on the DMD is limited by the maximum optical power density for each wavelength range specified and the micromirror array temperature ($T_{ARRAY}$).


Copyright © 2023 Texas Instruments Incorporated

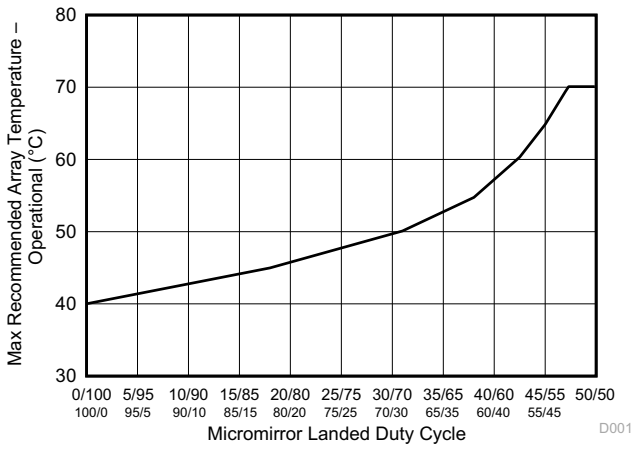



**図 6-1. Maximum Recommended Array Temperature – Derating Curve**

## 6.5 Thermal Information

| THERMAL METRIC(1) | | DLP230KP FQP (CLGA) 54 PINS | UNIT |
|---|---|---|---|
| Thermal resistance | Active area to test point 1 (TP1) (1) | 9.0 | °C/W |

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in セクション 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipated by the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

## 6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS(2) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT** | | | | | | |
| $I_{DD}$ | Supply current: $V_{DD}$ (3) (4) | $V_{DD}$ = 1.95 V | | | 65 | mA |
| | | $V_{DD}$ = 1.8 V | | 53 | | |
| $I_{DDI}$ | Supply current: $V_{DDI}$ (3) (4) | $V_{DDI}$ = 1.95 V | | | 12 | mA |
| | | $V_{DD}$ = 1.8 V | | 11 | | |
| $I_{OFFSET}$ | Supply current: $V_{OFFSET}$ (5) (6) | $V_{OFFSET}$ = 10.5 V | | | 1.5 | mA |
| | | $V_{OFFSET}$ = 10 V | | 1.4 | | |
| $I_{BIAS}$ | Supply current: $V_{BIAS}$ (5) (6) | $V_{BIAS}$ = 18.5 V | | | 0.3 | mA |
| | | $V_{BIAS}$ = 18 V | | 0.29 | | |
| $I_{RESET}$ | Supply current: $V_{RESET}$ (6) | $V_{RESET}$ = –14.5 V | | | –1.3 | mA |
| | | $V_{RESET}$ = –14 V | | –1.2 | | |
| **POWER**(7) | | | | | | |
| $P_{DD}$ | Supply power dissipation: $V_{DD}$ (3) (4) | $V_{DD}$ = 1.95 V | | | 126.75 | mW |
| | | $V_{DD}$ = 1.8 V | | 95.4 | | |
| $P_{DDI}$ | Supply power dissipation: $V_{DDI}$ (3) (4) | $V_{DDI}$ = 1.95 V | | | 23.4 | mW |
| | | $V_{DD}$ = 1.8 V | | 19.8 | | |
| $P_{OFFSET}$ | Supply power dissipation: $V_{OFFSET}$ (5) (6) | $V_{OFFSET}$ = 10.5 V | | | 15.75 | mW |
| | | $V_{OFFSET}$ = 10 V | | 14 | | |

Copyright © 2023 Texas Instruments Incorporated

## 6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | TEST CONDITIONS(2) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_{BIAS}$ | Supply power dissipation: $V_{BIAS}$ (5) (6) | $V_{BIAS}$ = 18.5 V | | | 5.55 | mW |
| | | $V_{BIAS}$ = 18 V | | 5.22 | | |
| $P_{RESET}$ | Supply power dissipation: $V_{RESET}$ (6) | $V_{RESET}$ = –14.5 V | | | 18.85 | mW |
| | | $V_{RESET}$ = –14 V | | 16.80 | | |
| $P_{TOTAL}$ | Supply power dissipation: Total | | | 151.22 | 190.3 | mW |
| **LPSDR INPUT**(8) | | | | | | |
| $V_{IH(DC)}$ | DC input high voltage(9) | | 0.7 × $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| $V_{IL(DC)}$ | DC input low voltage(9) | | –0.3 | | 0.3 × $V_{DD}$ | V |
| $V_{IH(AC)}$ | AC input high voltage(9) | | 0.8 × $V_{DD}$ | | $V_{DD}$ + 0.3 | V |
| $V_{IL(AC)}$ | AC input low voltage(9) | | –0.3 | | 0.2 × $V_{DD}$ | V |
| $\Delta V_T$ | Hysteresis ( $V_{T+} – V_{T–}$ ) | 図 6-10 | 0.1 × $V_{DD}$ | | 0.4 × $V_{DD}$ | V |
| $I_{IL}$ | Low–level input current | $V_{DD}$ = 1.95 V; $V_I$ = 0 V | –100 | | | nA |
| $I_{IH}$ | High–level input current | $V_{DD}$ = 1.95 V; $V_I$ = 1.95 V | | | 100 | nA |
| **LPSDR OUTPUT**(10) | | | | | | |
| $V_{OH}$ | DC output high voltage | $I_{OH}$ = –2 mA | 0.8 × $V_{DD}$ | | | V |
| $V_{OL}$ | DC output low voltage | $I_{OL}$ = 2 mA | | | 0.2 × $V_{DD}$ | V |
| **CAPACITANCE** | | | | | | |
| $C_{IN}$ | Input capacitance LPSDR | $f$ = 1 MHz | | | 10 | pF |
| | Input capacitance SubLVDS | $f$ = 1 MHz | | | 20 | pF |
| $C_{OUT}$ | Output capacitance | $f$ = 1 MHz | | | 10 | pF |
| $C_{RESET}$ | Reset group capacitance | $f$ = 1 MHz; (540 × 120) micromirrors | 90 | | 150 | pF |

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins ($V_{SS}$).
(3) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, $V_{RESET}$. All $V_{SS}$ connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) LPSDR specification is for pin LS_RDATA.

## 6.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LPSDR** | | | | | | |
| $t_r$ | Rise slew rate(1) | (30% to 80%) × $V_{DD}$, 図 6-3 | 1 | | 3 | V/ns |
| $t_f$ | Fall slew rate(1) | (70% to 20%) × $V_{DD}$, 図 6-3 | 1 | | 3 | V/ns |
| $t_r$ | Rise slew rate(2) | (20% to 80%) × $V_{DD}$, 図 6-3 | 0.25 | | | V/ns |
| $t_f$ | Fall slew rate(2) | (80% to 20%) × $V_{DD}$, 図 6-3 | 0.25 | | | V/ns |
| $t_c$ | Cycle time LS_CLK | 図 6-2 | 7.7 | 8.3 | | ns |
| $t_{W(H)}$ | Pulse duration LS_CLK high | 50% to 50% reference points, 図 6-2 | 3.1 | | | ns |
| $t_{W(L)}$ | Pulse duration LS_CLK low | 50% to 50% reference points, 図 6-2 | 3.1 | | | ns |

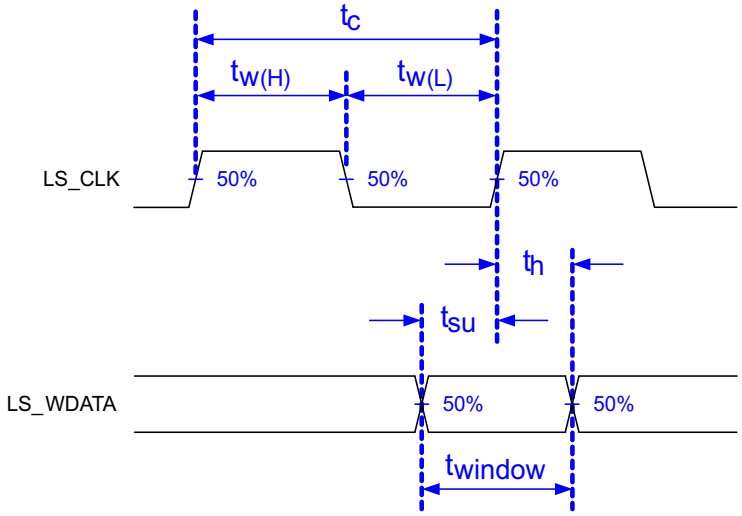

Copyright © 2023 Texas Instruments Incorporated

## 6.7 Timing Requirements (continued)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{su}$ | Setup time | LS_WDATA valid before LS_CLK ↑, 図 6-2 | 1.5 | | | ns |
| $t_h$ | Hold time | LS_WDATA valid after LS_CLK ↑, 図 6-2 | 1.5 | | | ns |
| $t_{WINDOW}$ | Window time(1) (3) | Setup time + hold time, 図 6-2 | 3 | | | ns |
| $t_{DERATING}$ | Window time derating(1) (3) | For each 0.25 V/ns reduction in slew rate below 1 V/ns, 図 6-5 | | 0.35 | | ns |
| **SubLVDS** | | | | | | |
| $t_r$ | Rise slew rate | 20% to 80% reference points, 図 6-4 | 0.7 | 1 | | V/ns |
| $t_f$ | Fall slew rate | 80% to 20% reference points, 図 6-4 | 0.7 | 1 | | V/ns |
| $t_c$ | Cycle time DCLK | 図 6-6 | 1.79 | 1.85 | | ns |
| $t_{W(H)}$ | Pulse duration DCLK high | 50% to 50% reference points, 図 6-6 | 0.79 | | | ns |
| $t_{W(L)}$ | Pulse duration DCLK low | 50% to 50% reference points, 図 6-6 | 0.79 | | | ns |
| $t_{su}$ | Setup time | D(0:7) valid before DCLK ↑ or DCLK ↓, 図 6-6 | | | | |
| $t_h$ | Hold time | D(0:7) valid after DCLK ↑ or DCLK ↓, 図 6-6 | | | | |
| $t_{WINDOW}$ | Window time | Setup time + hold time, 図 6-6, 図 6-7 | | | 0.3 | ns |
| $t_{LVDS-ENABLE+REFGEN}$ | Power-up receiver(4) | | | | 2000 | ns |

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in 図 6-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 図 6-3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.




Low-speed interface is LPSDR and adheres to *セクション 6.6* and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

**図 6-2. LPSDR Switching Parameters**

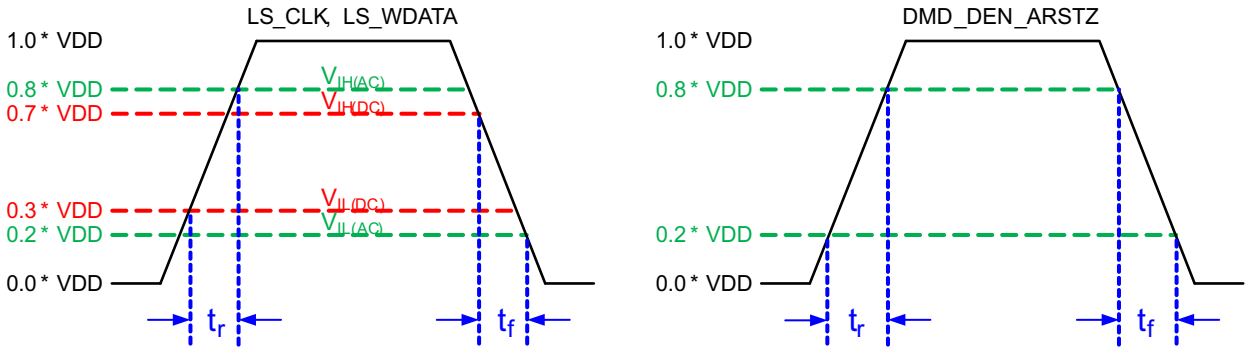



**図 6-3. LPSDR Input Rise and Fall Slew Rate**

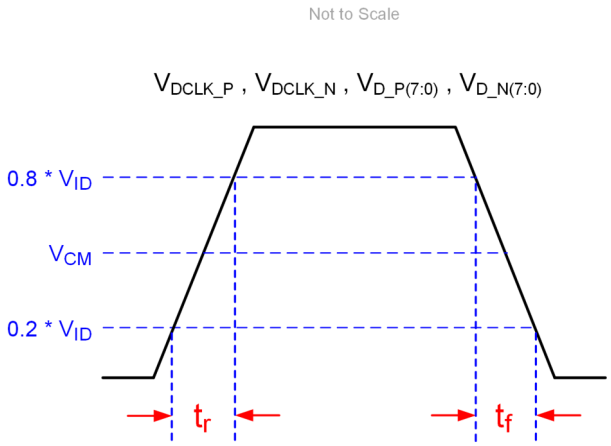



**図 6-4. SubLVDS Input Rise and Fall Slew Rate**


Copyright © 2023 Texas Instruments Incorporated

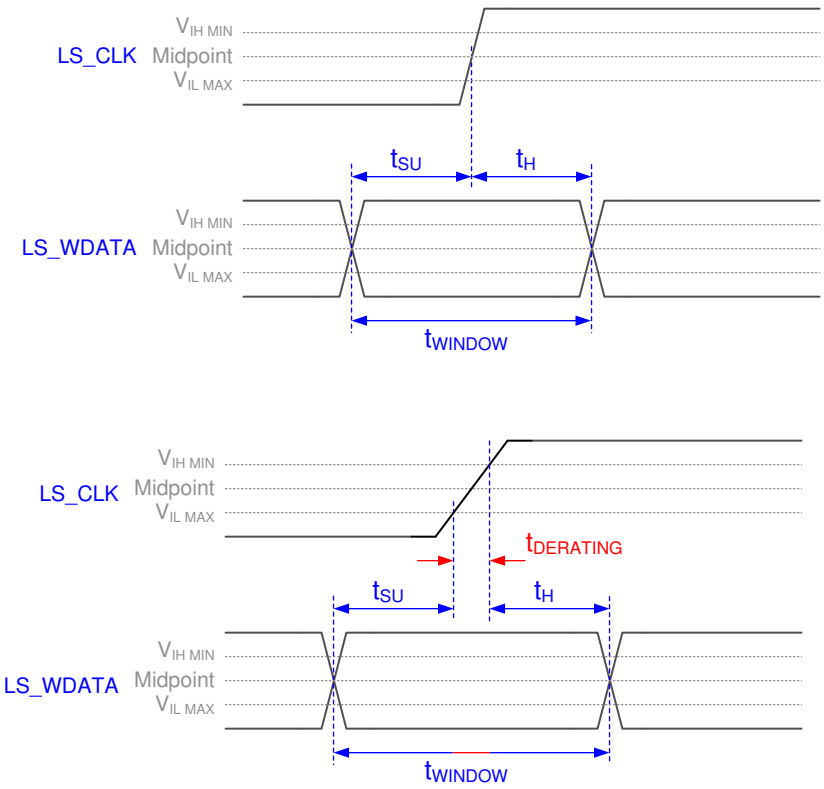



**図 6-5. Window Time Derating Concept**

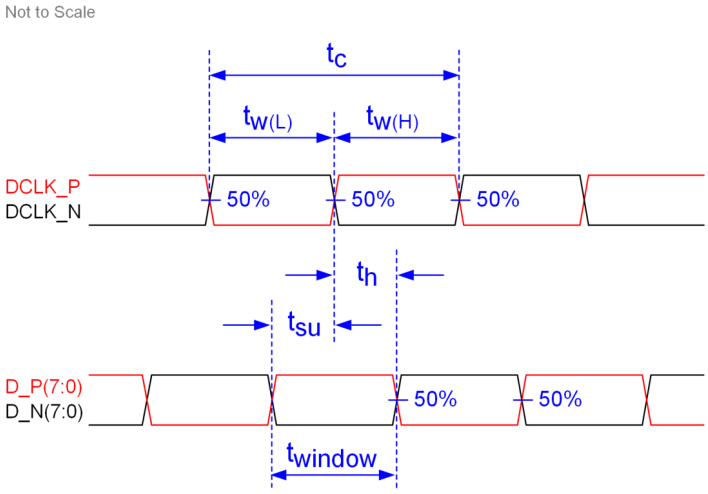
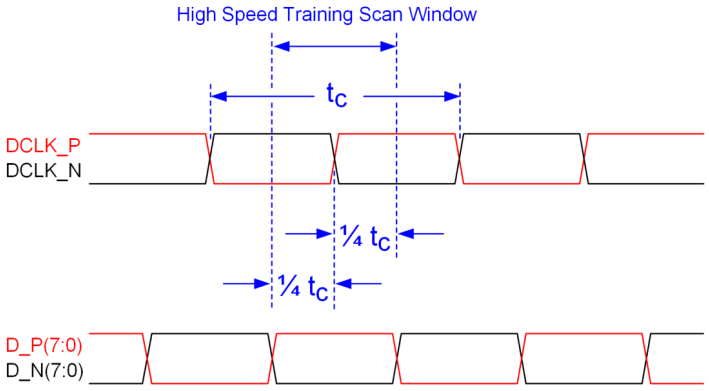



**図 6-6. SubLVDS Switching Parameters**




Note: Refer to セクション 7.3.3 for details.

**図 6-7. High-Speed Training Scan Window**

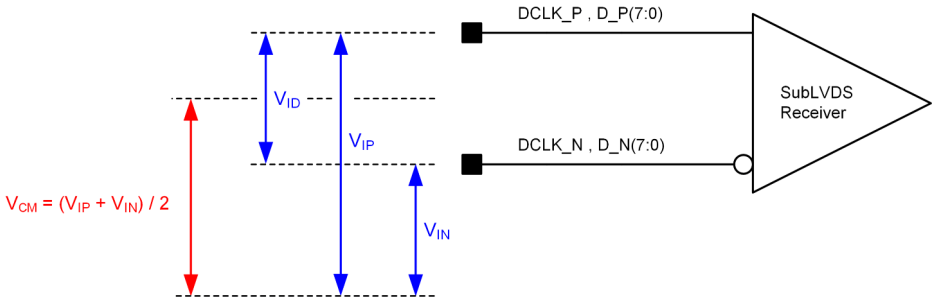



**図 6-8. SubLVDS Voltage Parameters**

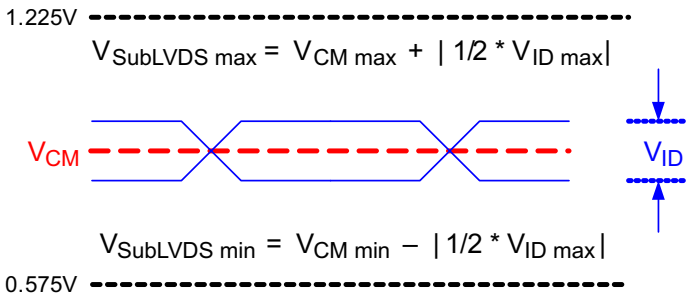



**図 6-9. SubLVDS Waveform Parameters**

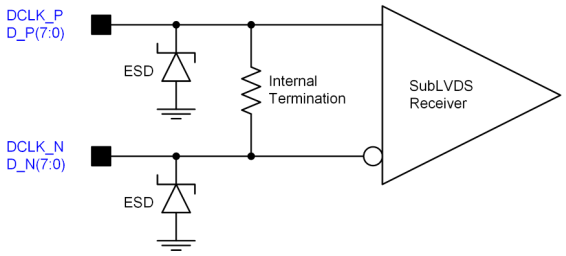



**図 6-10. SubLVDS Equivalent Input Circuit**


Copyright © 2023 Texas Instruments Incorporated

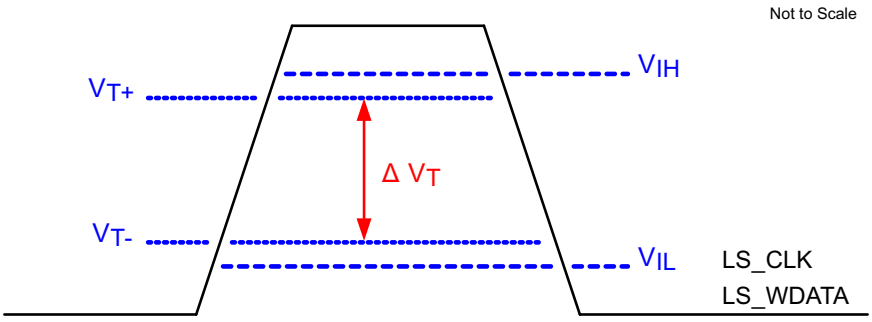



**図 6-11. LPSDR Input Hysteresis**

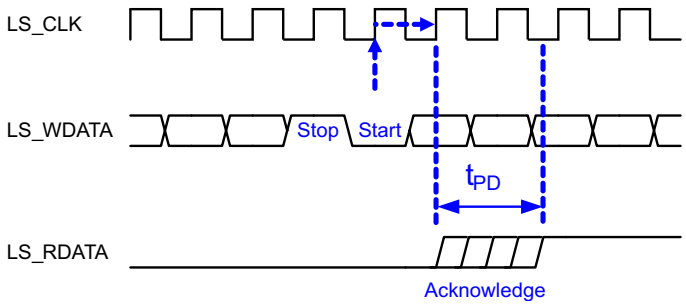
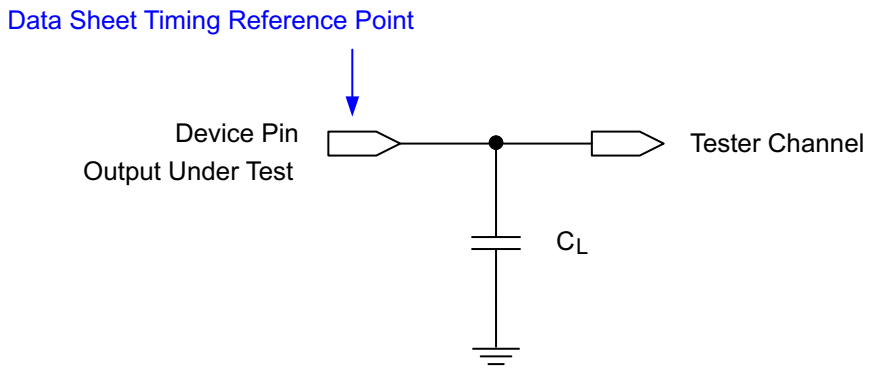



**図 6-12. LPSDR Read Out**




See セクション 7.3.4 for more information.

**図 6-13. Test Load Circuit for Output Propagation Measurement**

## 6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). (1)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output. See 図 6-12. | $C_L$ = 5 pF | | | 11.1 | ns |
| | | $C_L$ = 10 pF | | | 11.3 | ns |
| | | $C_L$ = 85 pF | | | 15 | ns |
| | Slew rate, LS_RDATA | | 0.5 | | | V/ns |
| | Output duty cycle distortion, LS_RDATA | | 40% | | 60% | |

(1) Device electrical characteristics comply with the values in セクション 6.4 unless otherwise noted.

Copyright © 2023 Texas Instruments Incorporated

## 6.9 System Mounting Interface Loads

| PARAMETER | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Maximum system mounting interface load to be applied to the: | | | | |
| • Thermal interface area (1) | | | 45 | N |
| • Clamping and electrical interface area (1) | | | 100 | N |

(1) Uniformly distributed within area shown in 図 6-14.

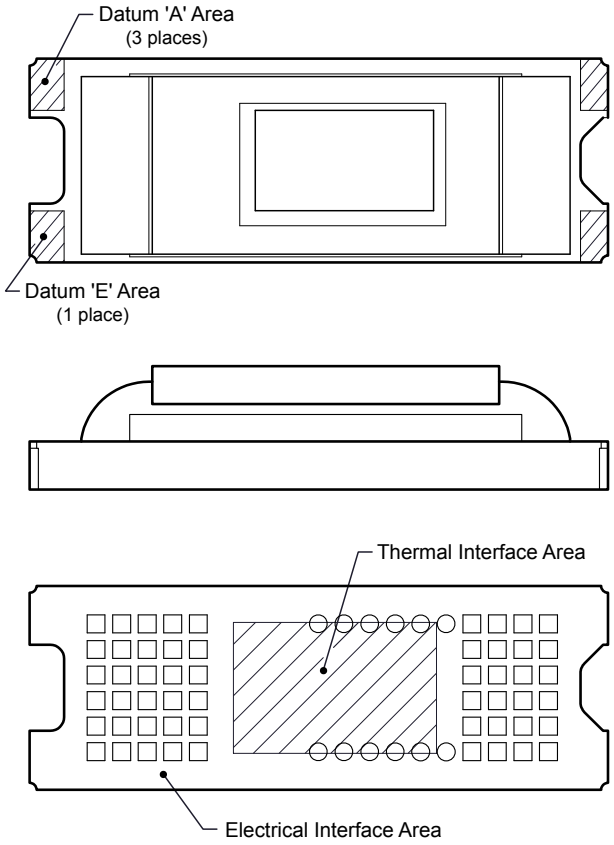



**図 6-14. System Interface Loads**


Copyright © 2023 Texas Instruments Incorporated

## 6.10 Micromirror Array Physical Characteristics

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Number of active columns(1) | See 図 6-15. | 960 | micromirrors |
| Number of active rows(1) | See 図 6-15. | 540 | micromirrors |
| Micromirror (pixel) pitch | See 図 6-16. | 5.4 | µm |
| Micromirror active array width | Micromirror pitch × number of active columns; see 図 6-15 | 5.184 | mm |
| Micromirror active array height | Micromirror pitch × number of active rows; see 図 6-15. | 2.916 | mm |
| Micromirror active border | Pond of micromirror (POM)(2) | 20 | micromirrors/side |

(1) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display two distinct pixels on the screen during every frame, resulting in a full 1280 × 720 pixel image being displayed.
(2) The structure and qualities of the border around the active array include a band of partially functional micromirrors called the POM. These micromirrors are structurally or electrically prevented from tilting toward the bright or ON state, but require an electrical bias to tilt toward OFF.

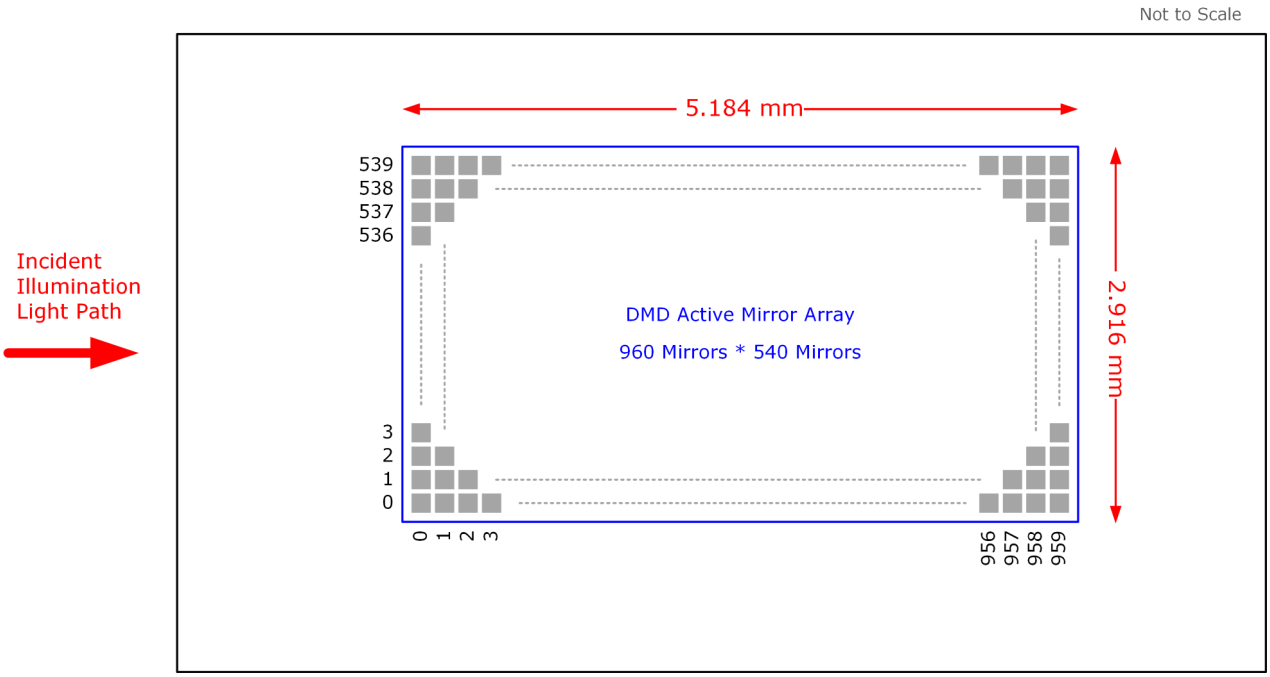



**図 6-15. Micromirror Array Physical Characteristics**

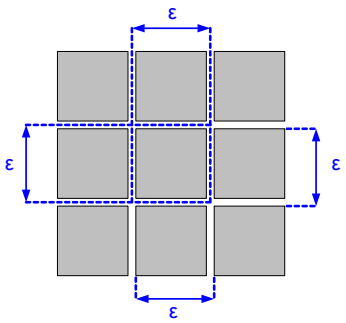



**図 6-16. Mirror (Pixel) Pitch**

## 6.11 Micromirror Array Optical Characteristics

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Micromirror tilt angle | | DMD landed state(1) | | 17 | | ° |
| Micromirror tilt angle tolerance(2) (3) (4) (5) | | | –1.4 | | 1.4 | ° |
| Micromirror tilt direction(6) (7) | | Landed ON state | | 180 | | ° |
| | | Landed OFF state | | 270 | | |
| Micromirror crossover time(8) | | Typical performance | | 1 | 3 | µs |
| Micromirror switching time(9) | | Typical performance | 10 | | | |
| Image performance(10) | Bright pixel(s) in active area (11) | Gray 10 screen (12) | | | 0 | micromirrors |
| | Bright pixel(s) in the POM (13) | Gray 10 screen (12) | | | 1 | |
| | Dark pixel(s) in the active area (14) | White screen | | | 4 | |
| | Adjacent pixel(s) (15) | Any screen | | | 0 | |
| | Unstable pixel(s) in active area (16) | Any screen | | | 0 | |

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See 図 6-17.
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
Test set degamma shall be linear
Test set brightness and contrast shall be set to nominal
The diagonal size of the projected image shall be a minimum of 20 inches
The projections screen shall be 1X gain
The projected image shall be inspected from a 38-inch minimum viewing distance
The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
Red = 10/255
Green = 10/255
Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.


Copyright © 2023 Texas Instruments Incorporated

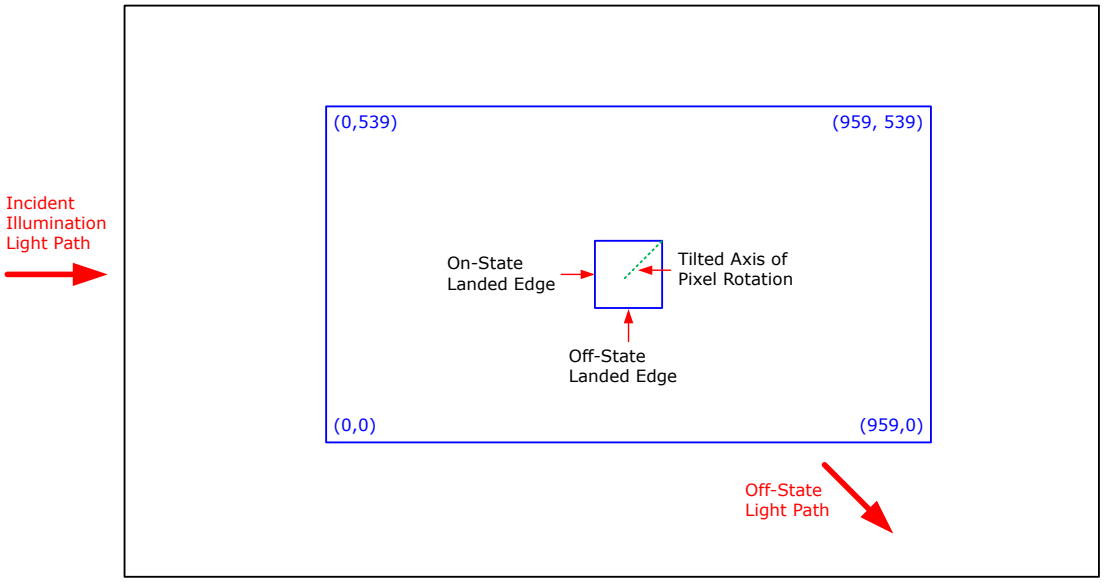



**図 6-17. Landed Pixel Orientation and Tilt**

## 6.12 Window Characteristics

| PARAMETER(1) | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Window material designation | | | Corning Eagle XG | | |
| Window refractive index | At wavelength 546.1 nm | | 1.5119 | | |
| Window aperture(2) | | | | See (2) | |
| Illumination overfill(3) | | | | See (3) | |
| Window transmittance, single-pass through both surfaces and glass | Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI | 97% | | | |
| | Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI | 97% | | | |

(1) See セクション 7.5 for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the DLP230KP device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

## 6.13 Chipset Component Usage Specification

注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP230KP is a component of one or more DLP® chipsets. Reliable function and operation of the DLP230KP requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

Copyright © 2023 Texas Instruments Incorporated

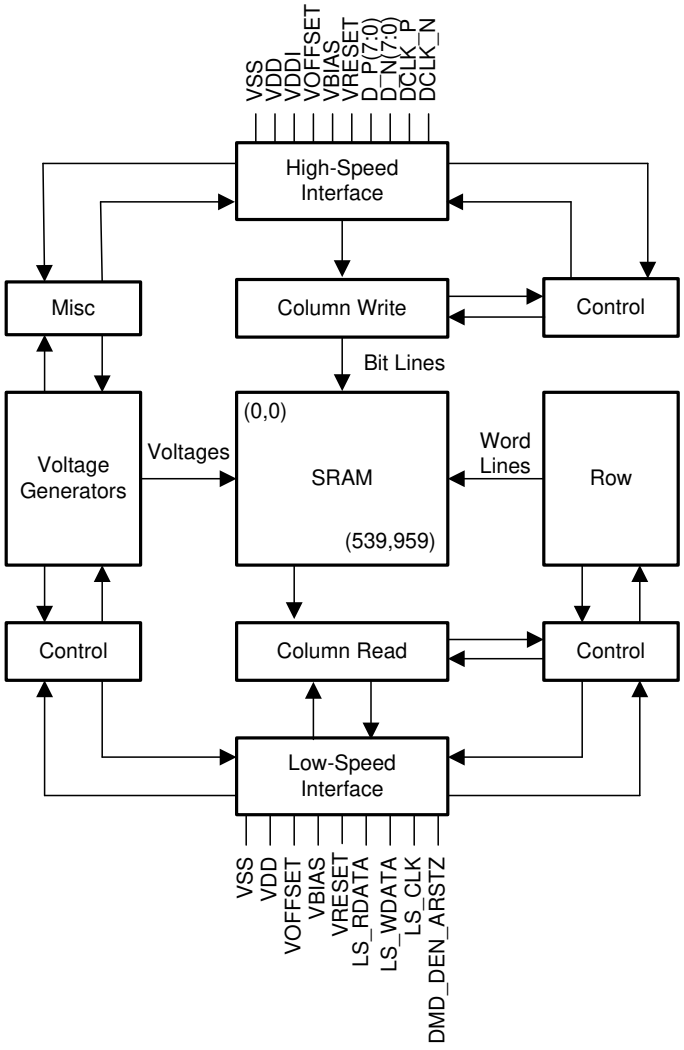
# 7 Detailed Description

## 7.1 Overview

The DLP230KP is a 0.23-inch diagonal spatial light modulator of aluminum micromirrors. Micromirror array size is 960 columns by 540 rows in a square micromirror arrangement. The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display two distinct pixels on the screen during every frame, resulting in a full 1280 × 720 pixel image being displayed. The electrical interface is sub low voltage differential signaling (SubLVDS) data.

This chipset comprises this DMS and the DLPC3434 controller. The DLPA2000, DLP2005, and DLP3000 PMIC/LED drivers also support this chipset. To ensure reliable operation, the DLP230KP DMD must always be used with the DLPC3434 ZVB display controller and the DLPA2000, DLP2005, or DLP3000 PMIC/LED driver.

## 7.2 Functional Block Diagram




A. Details omitted for clarity.


Copyright © 2023 Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 Power Interface

The power management IC DLPA2000, DLPA2005, and DLPA3000 contain three regulated DC supplies for the DMD reset circuitry: $V_{BIAS}$, $V_{RESET}$ and $V_{OFFSET}$, as well as the two regulated DC supplies for the DLPC3434ZVB controller.

### 7.3.2 Low-Speed Interface

The low speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low–speed clock, and LS_WDATA is the low speed data input.

### 7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs with a dedicated clock.

### 7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 図 6-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 7.4 Device Functional Modes

The DLPC3434 controller manages the functional modes of the DMD. For more information, download the controller data sheet or contact a TI applications engineer.

## 7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

### 7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat–state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

### 7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

Copyright © 2023 Texas Instruments Incorporated

### 7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

## 7.6 Micromirror Array Temperature Calculation

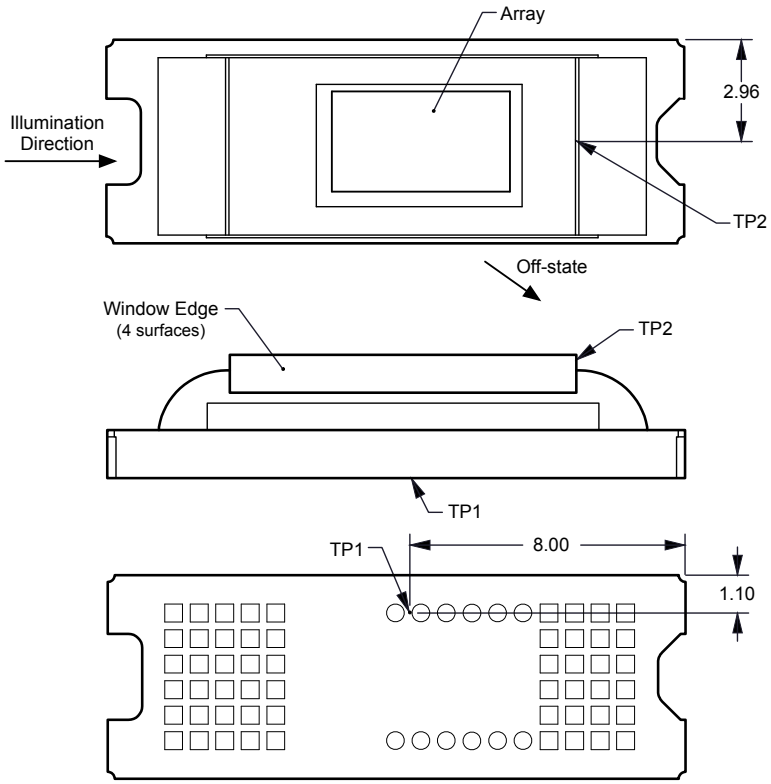



**図 7-1. DMD Thermal Test Points**


Copyright © 2023 Texas Instruments Incorporated

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in 図 7-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- $T_{ARRAY}$ = Computed array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = Thermal resistance of package specified in セクション 6.5 from array to ceramic TP1 (°C/Watt)
- $Q_{ARRAY}$ = Total DMD power on the array (W) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = Nominal electrical power (W)
- $Q_{INCIDENT}$ = Incident illumination optical power (W)
- $Q_{ILLUMINATION}$ = (DMD average thermal absorptivity × $Q_{INCIDENT}$) (W)
- DMD average thermal absorptivity = 0.4

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.17 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a single chip or multichip DMD system. It assumes an illumination distribution of 83.7% on the active array, and 16.3% on the array border.

The sample calculation for a typical projection application is as follows:

$Q_{INCIDENT}$ = 2.9 W (measured)

$T_{CERAMIC}$ = 55.0°C (measured)

$Q_{ELECTRICAL}$ = 0.17 W

$Q_{ARRAY}$ = 0.17 W + (0.40 × 2.9 W) = 1.33 W

$T_{ARRAY}$ = 55.0°C + (1.33 W × 9.0°C/W) = 67.0°C

## 7.7 Micromirror Power Density Calculation

The calculation of the optical power density of the illumination on the DMD in the different wavelength bands uses the total measured optical power on the DMD, percent illumination overfill, area of the active array, and ratio of the spectrum in the wavelength band of interest to the total spectral optical power.

- $ILL_{UV} = [OP_{UV\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm$^2$)
- $ILL_{VIS} = [OP_{VIS\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm$^2$)
- $ILL_{IR} = [OP_{IR\text{-}RATIO} \times Q_{INCIDENT}] \times 1000 \div A_{ILL}$ (mW/cm$^2$)
- $ILL_{BLU} = [OP_{BLU\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm$^2$)
- $ILL_{BLU1} = [OP_{BLU1\text{-}RATIO} \times Q_{INCIDENT}] \div A_{ILL}$ (W/cm$^2$)

Copyright © 2023 Texas Instruments Incorporated

- $A_{ILL} = A_{ARRAY} \div (1 - OV_{ILL})$ ($cm^2$)

where:

- $ILL_{UV}$ = UV illumination power density on the DMD ($mW/cm^2$)
- $ILL_{VIS}$ = VIS illumination power density on the DMD ($W/cm^2$)
- $ILL_{IR}$ = IR illumination power density on the DMD ($mW/cm^2$)
- $ILL_{BLU}$ = BLU illumination power density on the DMD ($W/cm^2$)
- $ILL_{BLU1}$ = BLU1 illumination power density on the DMD ($W/cm^2$)
- $A_{ILL}$ = illumination area on the DMD ($cm^2$)
- $Q_{INCIDENT}$ = total incident optical power on DMD (W) (measured)
- $A_{ARRAY}$ = area of the array ($cm^2$) (data sheet)
- $OV_{ILL}$ = percent of total illumination on the DMD outside the array (%) (optical model)
- $OP_{UV\text{-}RATIO}$ = ratio of the optical power for wavelengths <410 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{VIS\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{IR\text{-}RATIO}$ = ratio of the optical power for wavelengths >800 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤475 nm to the total optical power in the illumination spectrum (spectral measurement)
- $OP_{BLU1\text{-}RATIO}$ = ratio of the optical power for wavelengths ≥410 and ≤445 nm to the total optical power in the illumination spectrum (spectral measurement)

The illumination area varies and depends on the illumination overfill. The total illumination area on the DMD is the array area and overfill area around the array. The optical model is used to determine the percent of the total illumination on the DMD that is outside the array ($OV_{ILL}$) and the percent of the total illumination that is on the active array. From these values the illumination area ($A_{ILL}$) is calculated. The illumination is assumed to be uniform across the entire array.

From the measured illumination spectrum, the ratio of the optical power in the wavelength bands of interest to the total optical power is calculated.

Sample calculation:

$Q_{INCIDENT}$ = 2.90 W (measured)

$A_{ARRAY}$ = (0.5184 × 0.2916) = 0.1512 $cm^2$ (data sheet)

$OV_{ILL}$ = 16.3% (optical model)

$OP_{UV\text{-}RATIO}$ = 0.00021 (spectral measurement)

$OP_{VIS\text{-}RATIO}$ = 0.99977 (spectral measurement)

$OP_{IR\text{-}RATIO}$ = 0.00002 (spectral measurement)

$OP_{BLU\text{-}RATIO}$ = 0.28100 (spectral measurement)

$OP_{BLU1\text{-}RATIO}$ = 0.03200 (spectral measurement)


Copyright © 2023 Texas Instruments Incorporated

$A_{ILL}$ = 0.1512 ÷ (1 - 0.163) = 0.1806 $cm^2$

$ILL_{UV}$ = [0.00021 × 2.90W] × 1000 ÷ 0.1806 $cm^2$ = 3.372 $mW/cm^2$

$ILL_{VIS}$ = [0.99977 × 2.90W] ÷ 0.1806 $cm^2$ = 16.05 $W/cm^2$

$ILL_{IR}$ = [0.00002 × 2.90W] × 1000 ÷ 0.1806 $cm^2$ = 0.321 $mW/cm^2$

$ILL_{BLU}$ = [0.28100 × 2.90W] ÷ 0.1806 $cm^2$ = 4.51 $W/cm^2$

$ILL_{BLU1}$ = [0.03200 × 2.90W] ÷ 0.1806 $cm^2$ = 0.51 $W/cm^2$

## 7.8 Micromirror Landed-On/Landed-Off Duty Cycle

### 7.8.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time and in the OFF state 25% of the time, whereas 25/75 would indicate that the pixel is in the ON state 25% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.

### 7.8.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Copyright © 2023 Texas Instruments Incorporated

### 7.8.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the DMD's usable life. This is quantified in the de-rating curve shown in 図 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

### 7.8.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the nominal landed duty cycle of a given pixel is determined by the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience very close to a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

**表 7-1. Grayscale Value and Landed Duty Cycle**

| Grayscale Value | Nominal Landed Duty Cycle |
|---|---|
| 0% | 0/100 |
| 10% | 10/90 |
| 20% | 20/80 |
| 30% | 30/70 |
| 40% | 40/60 |
| 50% | 50/50 |
| 60% | 60/40 |
| 70% | 70/30 |
| 80% | 80/20 |
| 90% | 90/10 |
| 100% | 100/0 |

Accounting for color rendition (but still ignoring image processing) requires knowing both the color scale value (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where "color cycle time" is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the nominal landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_\%} \times \text{Red_Scale_Value}) + (\text{Green_Cycle_\%} \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_\%} \times \text{Blue_Scale_Value}) \quad (1)$$

where

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that red, green, and blue are displayed (respectively) to achieve the desired white point.


Copyright © 2023 Texas Instruments Incorporated

For example, assuming that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the nominal landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 7-2.

**表 7-2. Example Landed Duty Cycle for Full-Color Pixels**

| Red Cycle Percentage | Green Cycle Percentage | Blue Cycle Percentage |
|---|---|---|
| 50% | 20% | 30% |

| Red Scale Value | Green Scale Value | Blue Scale Value | Nominal Landed Duty Cycle |
|---|---|---|---|
| 0% | 0% | 0% | 0/100 |
| 100% | 0% | 0% | 50/50 |
| 0% | 100% | 0% | 20/80 |
| 0% | 0% | 100% | 30/70 |
| 12% | 0% | 0% | 6/94 |
| 0% | 35% | 0% | 7/93 |
| 0% | 0% | 60% | 18/82 |
| 100% | 100% | 0% | 70/30 |
| 0% | 100% | 100% | 50/50 |
| 100% | 0% | 100% | 80/20 |
| 12% | 35% | 0% | 13/87 |
| 0% | 35% | 60% | 25/75 |
| 12% | 0% | 60% | 24/76 |
| 100% | 100% | 100% | 100/0 |

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLP controller DLPC3434ZVB, the three functions which influence the actual landed duty cycle are gamma, IntelliBright™, and bitplane sequencing rules.

Gamma is a power function of the form Output_Level = A × Input_Level$^{Gamma}$, where A is a scaling factor that is typically set to 1.

In the DLPC3434ZVB controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 図 7-2.

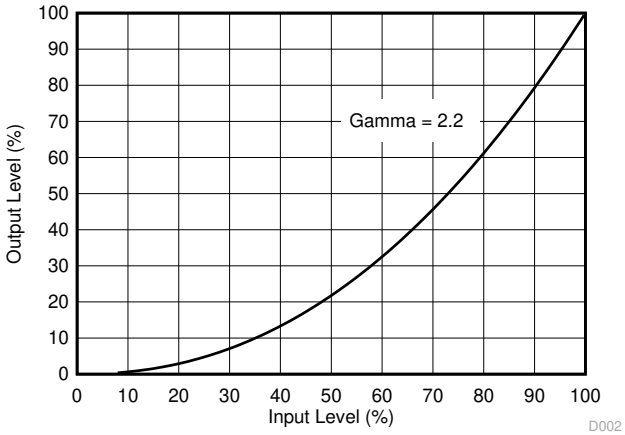



**図 7-2. Example of Gamma = 2.2**

For example, from 図 7-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then the gray scale value is 13% after gamma is applied. This reduction indicates that gamma has a direct impact on the displayed gray scale level of a pixel, and it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithm for content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma applied to every pixel of every frame is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply different amounts of either boost or compression to every pixel of every frame.

Give consideration to any image processing which occurs before the DLPC3434 controller.


Copyright © 2023 Texas Instruments Incorporated

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3434 controller. The new high tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Applications of interest include projection technology embedded in display devices such as ultra low-power battery operated mobile accessory projectors, phones, tablets, ultra mobile low end smart TVs, and virtual assistants.

The PMIC/LED driver strictly controls the DMD power-up and power-down sequencing. Refer to セクション 9 for power-up and power-down specifications. To ensure reliable operation, the DMD must always be used with the DLPC3434 display controller and either the DLPA2000, DLPA2005, and DLPA3000 PMIC/LED driver.

Copyright © 2023 Texas Instruments Incorporated

## 8.2 Typical Application

A common application when using a DLP230KP DMD and a DLPC3434 is for creating a Pico projector that can be used as an accessory to a smartphone, tablet, or a laptop. The DLPC3434 controller in the Pico projector receives images from a multimedia front end within the product as shown in 図 8-1 .

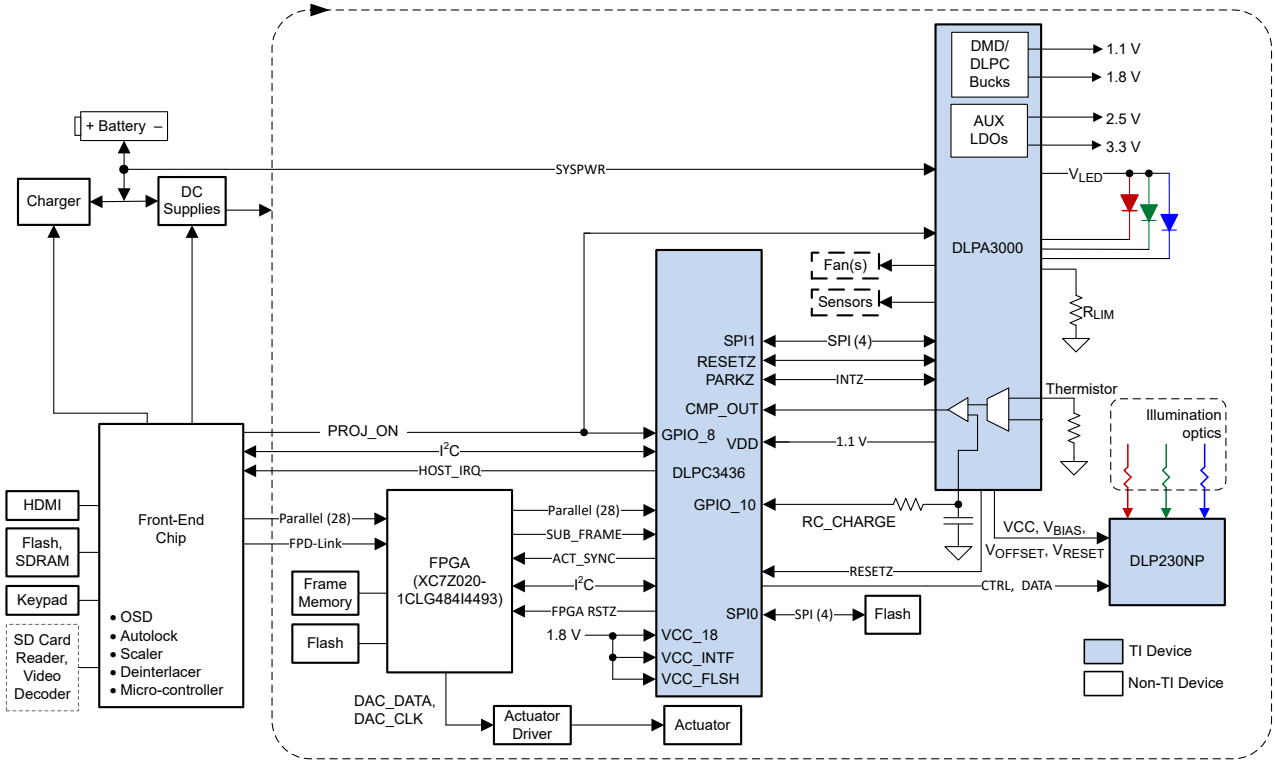



**図 8-1. Typical Application Diagram**

### 8.2.1 Design Requirements

A pico projector is created by using a DLP chipset comprised of a DLP230KP DMD, a DLPC3434 controller, and a DLPA2000/2005/3000 PMIC/LED driver. The DLPC3434 controller performs the digital image processing, the DLPA2000/2005/3000 provides the needed analog functions for the projector, and the DLP230KP DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips are needed. At a minimum a flash part is needed to store the DLPC3434 controller software.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico projector.

The DLPC3434 controller receives image data from the multimedia front end over a 24-bit parallel interface. An $I^2C$ interface should be connected from the multimedia front end for sending commands to the DLPC3434 controller for configuring the chipset for different features.

### 8.2.2 Detailed Design Procedure

For connecting together the DLPC3434 controller, the DLPA2000/2005/3000, and the DLP230KP DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.


Copyright © 2023 Texas Instruments Incorporated

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

### 8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in 図 8-2. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

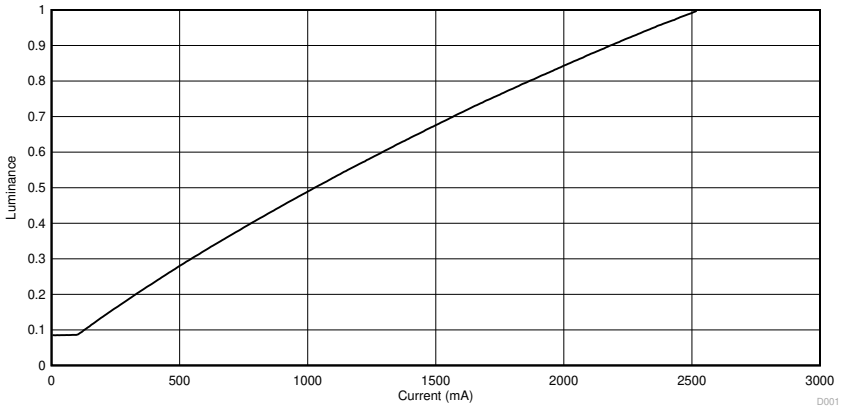



**図 8-2. Luminance vs LED Current**

Copyright © 2023 Texas Instruments Incorporated

# 9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, and $V_{RESET}$. All $V_{SS}$ connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA2000/2005/3000 devices.

> **注意**
>
> For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.
>
> $V_{DD}$, $V_{DDI}$, $V_{OFFSET}$, $V_{BIAS}$, and $V_{RESET}$ power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the specified requirements results in a significant reduction in the DMD reliability and lifetime. Refer to 図 9-2. $V_{SS}$ must also be connected.

## 9.1 Power Supply Power-Up Procedure

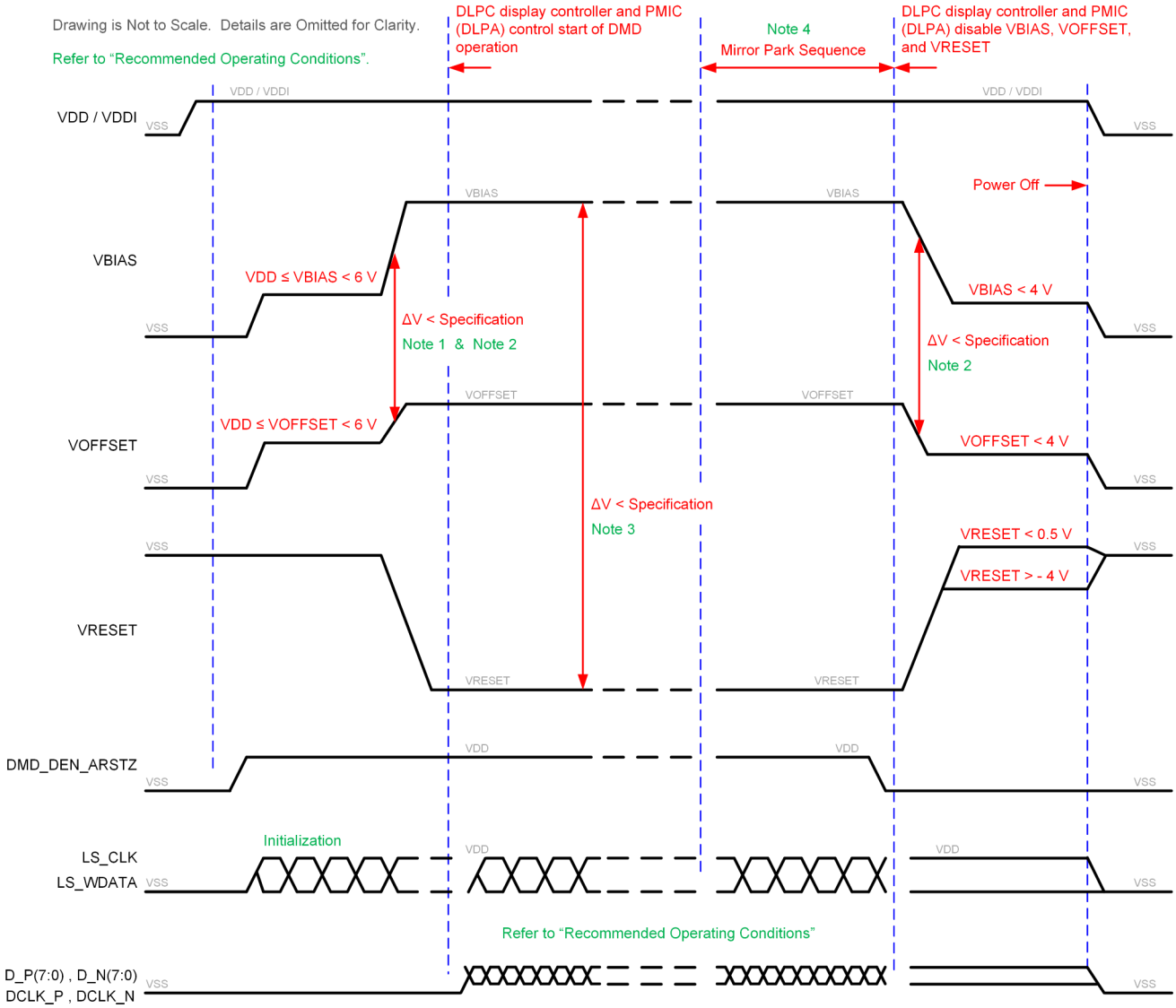
- During power-up, $V_{DD}$ and $V_{DDI}$ must always start and settle before $V_{OFFSET}$, $V_{BIAS}$, and $V_{RESET}$ voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between $V_{BIAS}$ and $V_{OFFSET}$ must be within the specified limit shown in セクション 6.4. Refer to 図 9-2 for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after $V_{DD}$ and $V_{DDI}$ have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of $V_{RESET}$ with respect to $V_{OFFSET}$ and $V_{BIAS}$. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in 図 9-1.

## 9.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. $V_{DD}$ and $V_{DDI}$ must be supplied until after $V_{BIAS}$, $V_{RESET}$, and $V_{OFFSET}$ are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving $V_{BIAS}$ prior to $V_{OFFSET}$, but it is a strict requirement that the delta between $V_{BIAS}$ and $V_{OFFSET}$ must be within the specified limit shown in セクション 6.4 (Refer to Note 2 for 図 9-1).
- During power-down, the DMD's LPSDR input pins must be less than $V_{DDI}$, the specified limit shown in セクション 6.4.
- During power-down, there is no requirement for the relative timing of $V_{RESET}$ with respect to $V_{OFFSET}$ and $V_{BIAS}$.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in 図 9-1.


Copyright © 2023 Texas Instruments Incorporated

## 9.3 Power Supply Sequencing Requirements




A. Refer to 表 9-1 and 図 9-2 for critical power-up sequence delay requirements.

B. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in セクション 6.4. OEMs may find that the most reliable way to ensure this is to power $V_{OFFSET}$ prior to $V_{BIAS}$ during power-up and to remove $V_{BIAS}$ prior to $V_{OFFSET}$ during power-down. Refer to 表 9-1 and 図 9-2 for power-up delay requirements.

C. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit shown in セクション 6.4.

D. When system power is interrupted, the DLPA2000/2005/3000 initiates hardware power-down that disables $V_{BIAS}$, $V_{RESET}$ and $V_{OFFSET}$ after the micromirror park sequence.

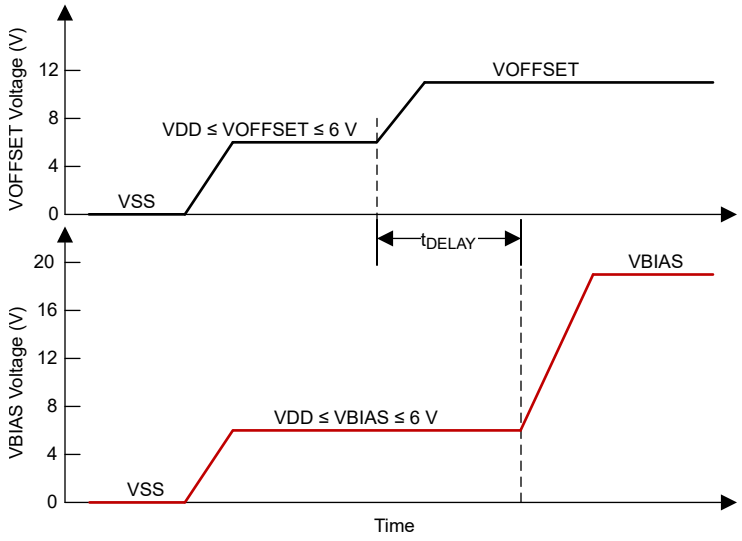
E. Drawing is not to scale and details are omitted for clarity.

**図 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)**

Copyright © 2023 Texas Instruments Incorporated

**表 9-1. Power-Up Sequence Delay Requirement**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{DELAY}$ | Delay requirement from $V_{OFFSET}$ power up to $V_{BIAS}$ power up | 2 | | ms |
| $V_{OFFSET}$ | Supply voltage level at beginning of power–up sequence delay (see 図 9-2) | | 6 | V |
| $V_{BIAS}$ | Supply voltage level at end of power–up sequence delay (see 図 9-2) | | 6 | V |




Refer to 表 9-1 for $V_{OFFSET}$ and $V_{BIAS}$ supply voltage levels during power-up sequence delay.

**図 9-2. Power-Up Sequence Delay Requirement**


Copyright © 2023 Texas Instruments Incorporated

# 10 Layout

## 10.1 Layout Guidelines

The DMD connects to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, and impedance, see the DLPC3434 controller data sheet. For a detailed layout example refer to the layout design files. Some layout guidelines for routing to the DMD are:

- Match lengths for the LS_WDATA nd LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 図 10-1.
- Minimum of two 100-nF (25 V) capacitors - one close to $V_{BIAS}$ pin. Capacitors C4 and C8 in 図 10-1.
- Minimum of two 100-nF (25 V) capacitors - one close to each $V_{RST}$ pin. Capacitors C3 and C7 in 図 10-1.
- Minimum of two 220-nF (25 V) capacitors - one close to each $V_{OFS}$ pin. Capacitors C5 and C6 in 図 10-1.
- Minimum of four 100-nF (6.3 V) capacitors - two close to each side of the DMD. Capacitors C1, C2, C9 and C10 in 図 10-1.

## 10.2 Layout Example

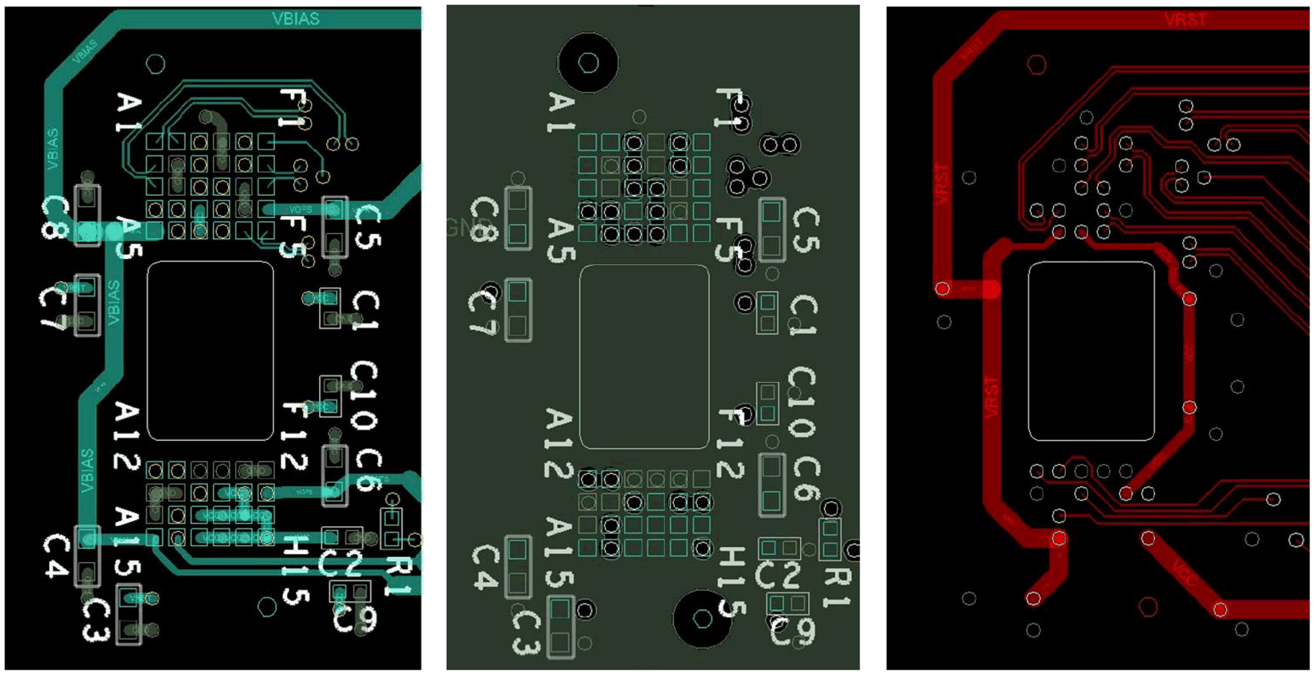



**図 10-1. Power Supply Connections**

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 11.1.2 Device Nomenclature

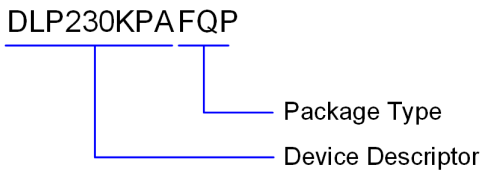



**図 11-1. Part Number Description**

### 11.1.3 Device Markings

The device marking includes the legible character string GHJJJJK. DLP230KPAFQP is the device marking.

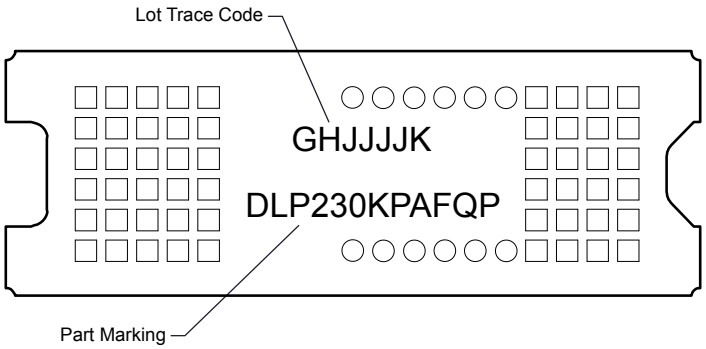



**図 11-2. DMD Marking**

## 11.2 Chipset Resources

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 11-1. Chipset Resources**

| Chipset Devices | Product folder | Ordering & quality | Technical documents | Design & development | Support & training |
|---|---|---|---|---|---|
| DLP230KP | Click here | Click here | Click here | Click here | Click here |
| DLPC3434 | Click here | Click here | Click here | Click here | Click here |
| DLPA3000 | Click here | Click here | Click here | Click here | Click here |
| DLPA2000 | Click here | Click here | Click here | Click here | Click here |
| DLPA2005 | Click here | Click here | Click here | Click here | Click here |

## 11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。


Copyright © 2023 Texas Instruments Incorporated

## 11.4 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

## 11.5 Trademarks

IntelliBright™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of TI.
すべての商標は、それぞれの所有者に帰属します。

## 11.6 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

Copyright © 2023 Texas Instruments Incorporated

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2023 Texas Instruments Incorporated

## 12.1 Package Option Addendum

### 12.1.1 Packaging Information

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking(4) (5) |
|---|---|---|---|---|---|---|---|---|---|---|
| DLP230KPAFQP | ACTIVE | CLGA | FQP | 54 | 100 | RoHS & Green | Call TI | Level-1-NC-NC | –40°C to 90°C | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Copyright © 2023 Texas Instruments Incorporated

### 12.1.1 Packaging Information

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking(4) (5) |
|---|---|---|---|---|---|---|---|---|---|---|
| DLP230KPAFQP | ACTIVE | CLGA | FQP | 54 | 100 | RoHS & Green | Call TI | Level-1-NC-NC | –40°C to 90°C | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PRE_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br)**: TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

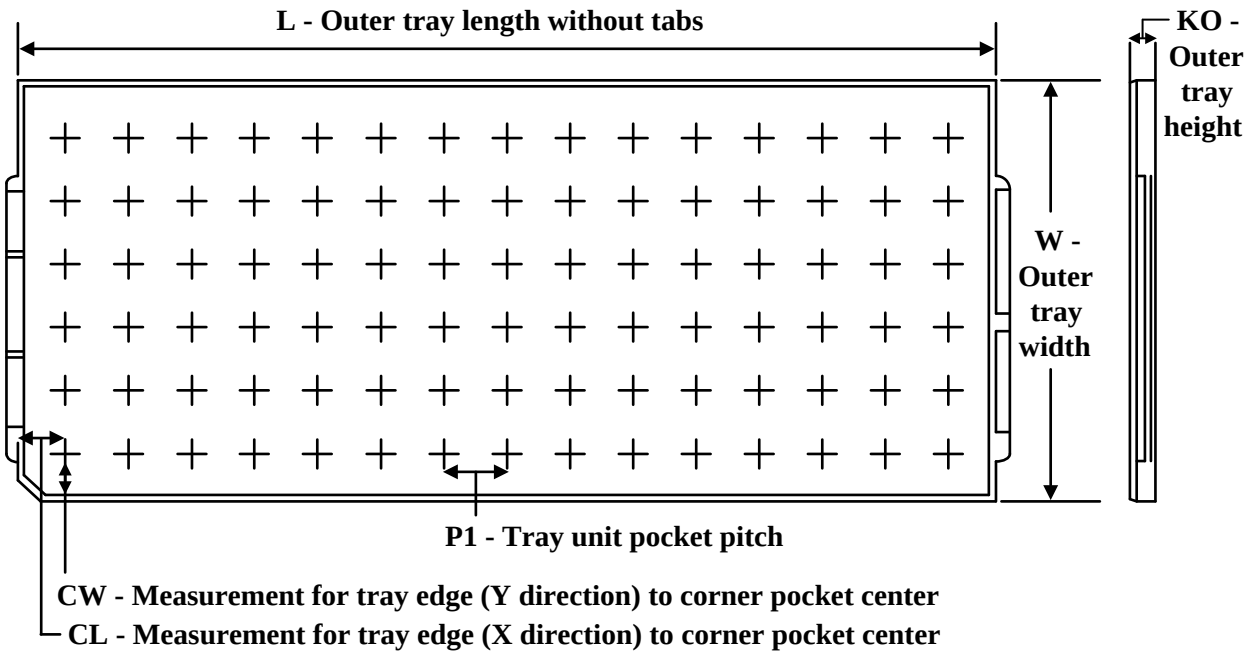
(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.


Copyright © 2023 Texas Instruments Incorporated

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

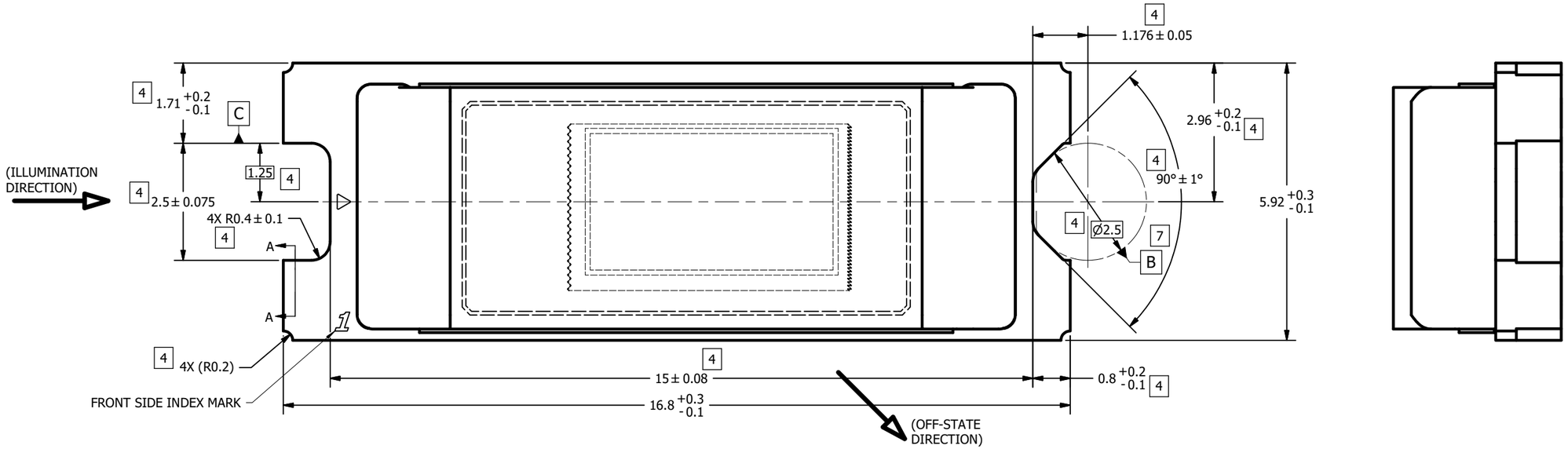
| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DLP230KPAFQP | FQP | CLGA | 54 | 140 | 10 x 14 | 150 | 315 | 135.9 | 12190 | 21.9 | 15.15 | 16.2 |
| DLP230KPAFQP.A | FQP | CLGA | 54 | 140 | 10 x 14 | 150 | 315 | 135.9 | 12190 | 21.9 | 15.15 | 16.2 |
| DLP230KPAFQP.B | FQP | CLGA | 54 | 140 | 10 x 14 | 150 | 315 | 135.9 | 12190 | 21.9 | 15.15 | 16.2 |

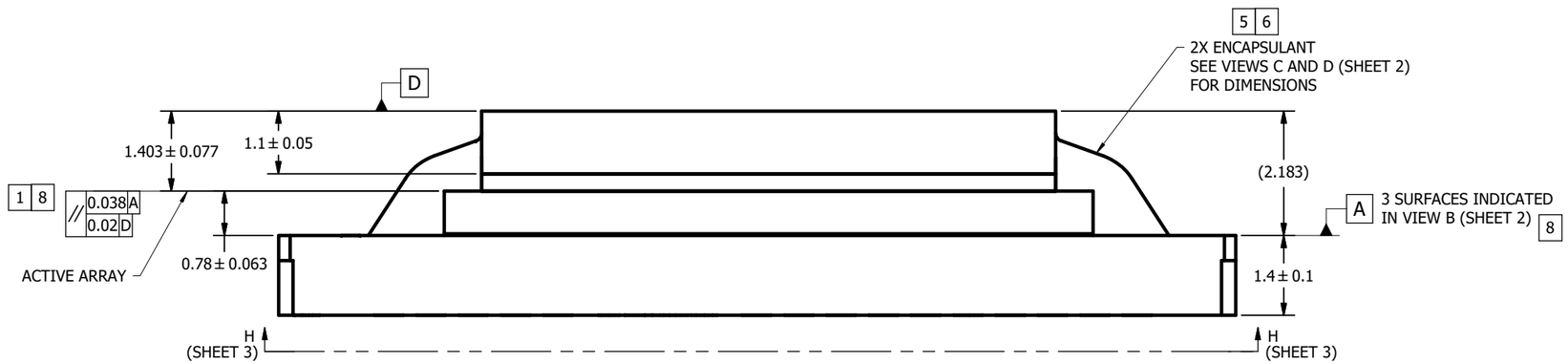
© COPYRIGHT 2017 TEXAS INSTRUMENTS
UN-PUBLISHED, ALL RIGHTS RESERVED.

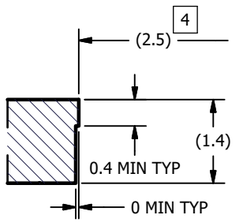
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | BY |
| A | ECO 2168534: INITIAL RELEASE | 9/5/2017 | BMH |
| B | ECO 2168970: CORRECT SUBSTRATE THICKNESS TOL; ENLARGE APERTURE SLIGHTLY | 9/15/17 | BMH |
| C | ECO 2186788: ADD APERTURE SLOT PICTORIALLY | 4/7/2020 | BMH |

NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.




SECTION A-A
(ROTATED 90°)
SCALE 20 : 1

| | |
|---|---|
| | |
| | |
| | |
| | |
| | |
| | 0314DA |
| NEXT ASSY | USED ON |
| APPLICATION | |

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

| | | DATE |
|---|---|---|
| DRAWN | B. HASKETT | 9/5/2017 |
| ENGINEER | B. HASKETT | 9/5/2017 |
| QA/CE | P. KONRAD | 9/10/2017 |
| CM | J. GRIMMETT | 9/6/2017 |
| | M. DORAK | 9/5/2017 |
| APPROVED | R. LONG | 9/11/2017 |

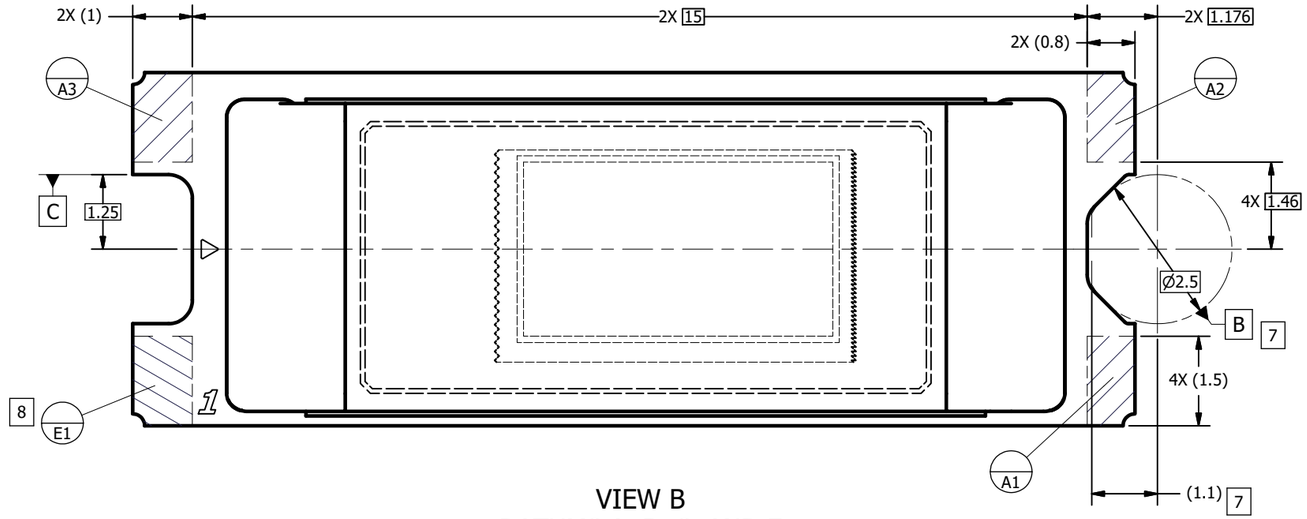
TEXAS INSTRUMENTS
Dallas Texas

TITLE: ICD, MECHANICAL, DMD, .23 TRP SERIES 246 (FQP PACKAGE)

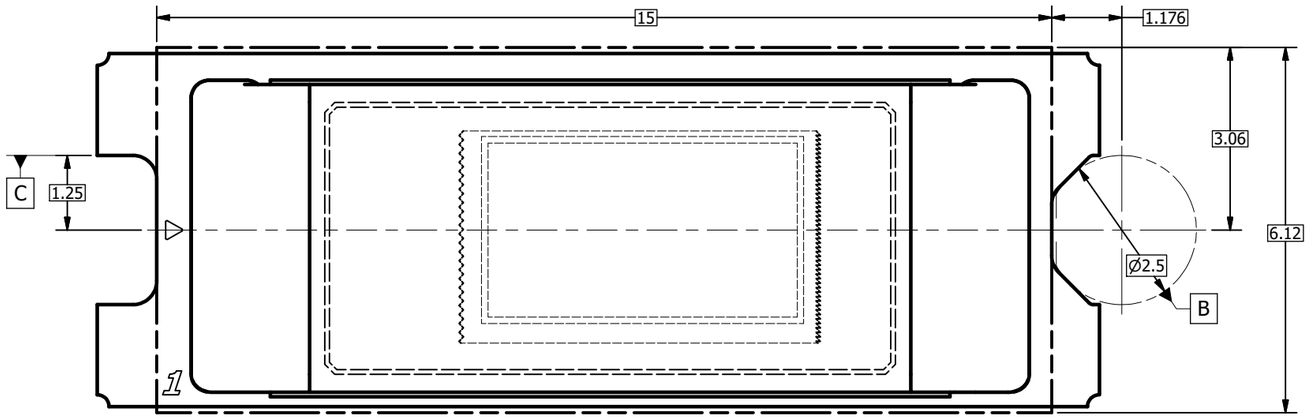
| SIZE | DWG NO | REV |
|---|---|---|
| D | 2515699 | C |

SCALE 20:1 SHEET 1 OF 3

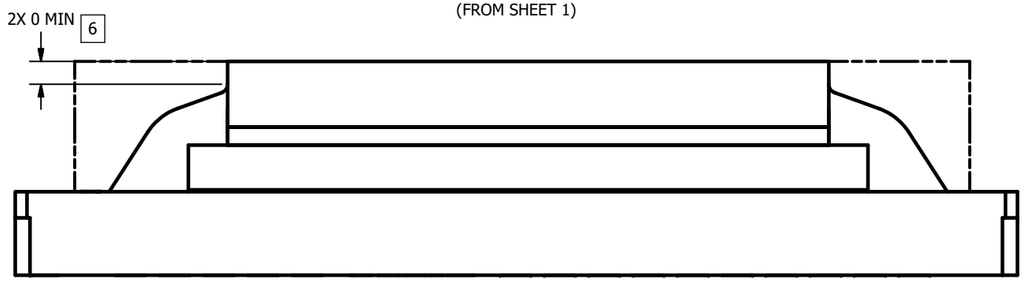
INV11-2006a




VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



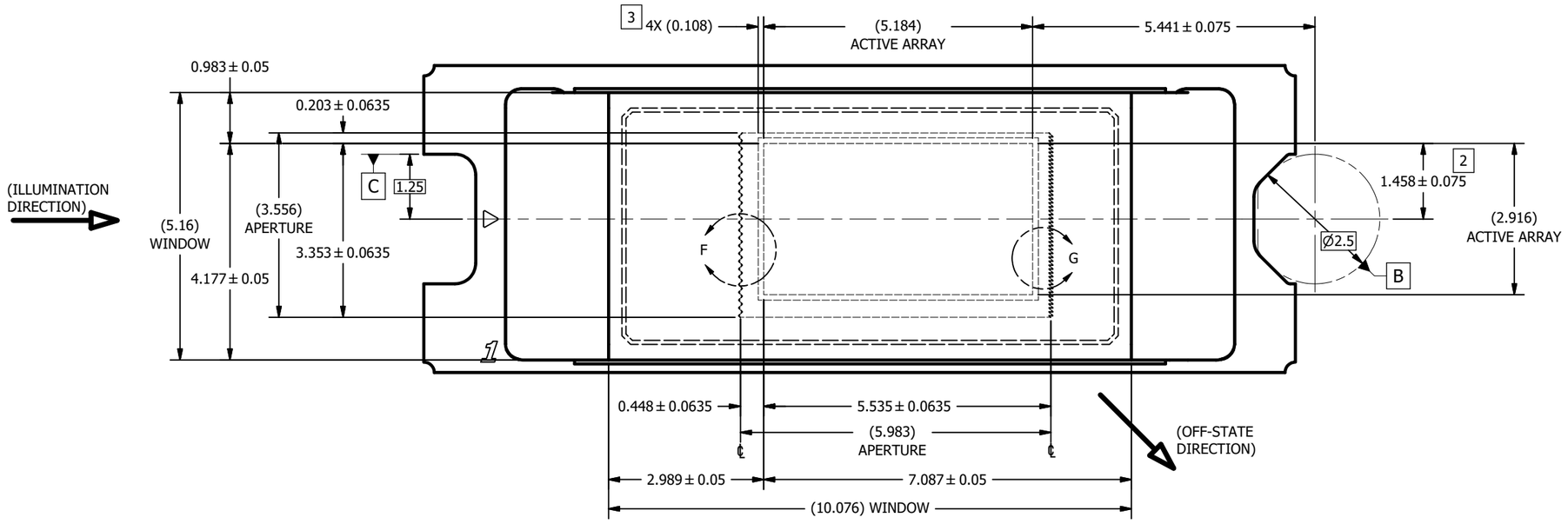

VIEW C 5
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



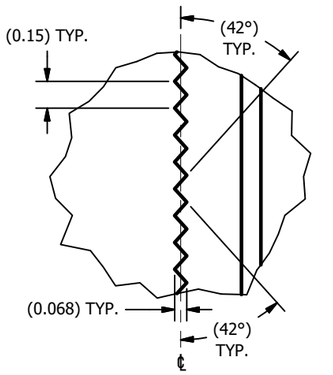

VIEW D
ENCAPSULANT MAXIMUM HEIGHT

| | | | | | |
|---|---|---|---|---|---|
| TEXAS INSTRUMENTS Dallas Texas | DRAWN B. HASKETT | DATE 9/5/2017 | SIZE D | DWG NO 2515699 | REV C |
| | | | SCALE | SHEET 2 OF 3 | |

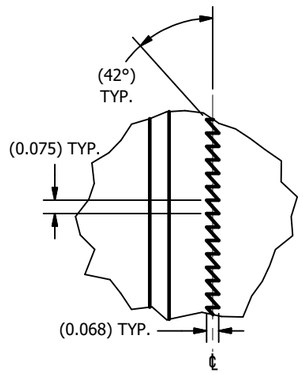
INV11-2006a



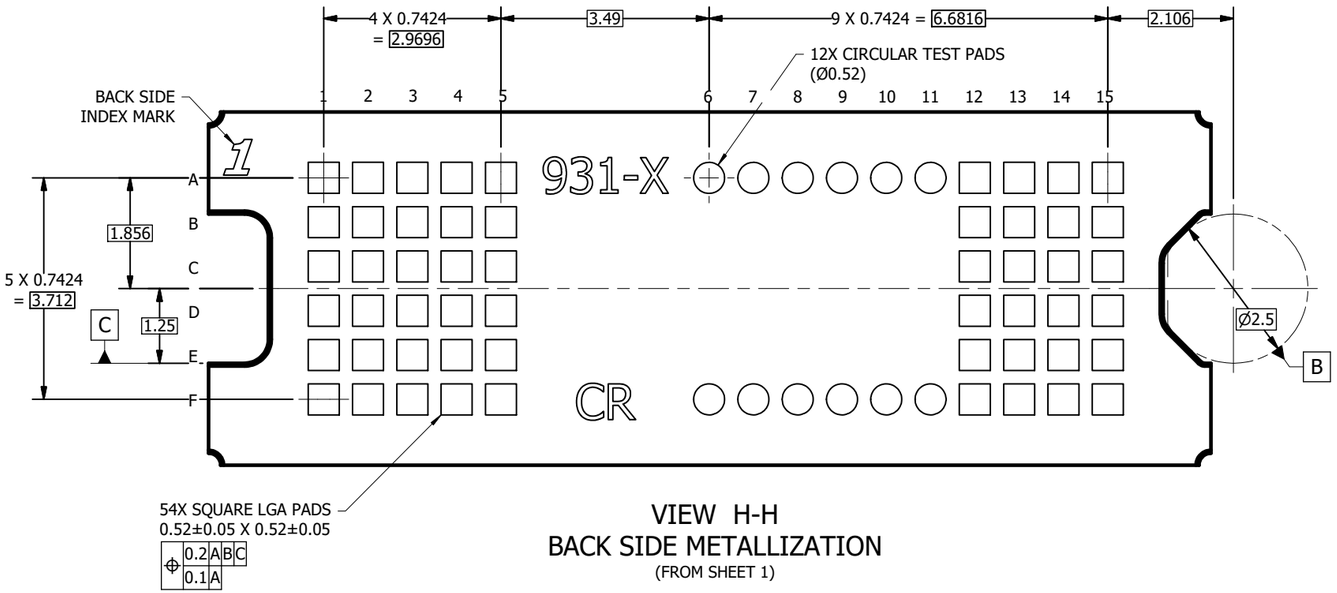

VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)




DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1




DETAIL G
APERTURE RIGHT EDGE
SCALE 60 : 1




VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

| | | | | | |
|---|---|---|---|---|---|
| Texas Instruments, Dallas Texas | DRAWN B. HASKETT | DATE 9/5/2017 | SIZE D | DWG NO 2515699 | REV C |
| | | | SCALE | SHEET 3 OF 3 | |

INV11-2006a

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、 TI の販売条件 、 TI の総合的な品質ガイドライン 、 ti.com または TI 製品などに関連して提供される他の適用条件に従い提供されます。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。 TI がカスタム、またはカスタマー仕様として明示的に指定していない限り、TI の製品は標準的なカタログに掲載される汎用機器です。

お客様がいかなる追加条項または代替条項を提案する場合も、TI はそれらに異議を唱え、拒否します。

Copyright © 2026, Texas Instruments Incorporated

最終更新日：2025 年 10 月