DLPA1000 電源管理およびLEDドライバIC

1 特長

- 降圧-昇圧DC/DCコンバータ付き、MOSFET内蔵の、高効率のRGB LEDドライバ
- 6つの低インピーダンス(100mΩ未満) MOSFETスイッチによるチャネル選択
- チャネルごとに独立の10ビット電流制御
- DMDレギュレータ
  - インダクタ1つだけで動作
  - VOFS: 8.5V
  - VBIAS: 16V
  - VRST: -10V
- リセット生成および電源シーケンシング
- RGB LEDストローブ・デコーダによりサポート
  - 共通アノードRGB
  - カソード-カソード-アノードRGB
- 33MHzのシリアル・ペリフェラル・インターフェイス(SPI)
- マルチプレクサによるアナログ信号の測定
  - バッテリ電圧
  - LED電圧、LED電流
  - 光センサ(ホワイト・ポイント修正用)
  - 外部温度センサ
- 監視および保護回路
  - ダイの過熱警告およびサーマル・シャットダウン
  - 低バッテリおよび低電圧誤動作防止
  - 過電流および低電圧保護
- 49ボール、0.4mmピッチのDSBGAパッケージ

2 アプリケーション

- DLP® Pico™プロジェクター
- 組み込みモバイル・プロジェクション
  - スマートフォン
  - タブレット
  - カメラ
  - ノートPC
- モバイル・アクセサリ
- ウェアラブル(目の近く)の表示
- バッテリ動作のプロジェクター

3 概要

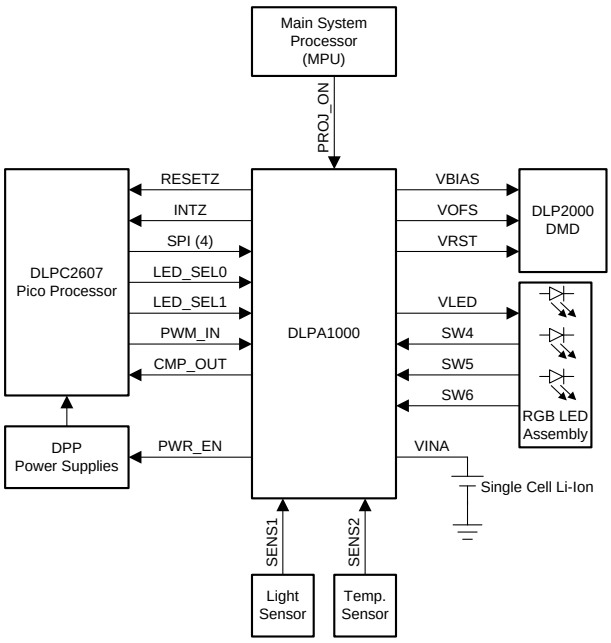
DLPA1000は、DLPC2607DLPデジタル・コントローラとともに使用するDLP2000デジタル・マイクロミラー・デバイス(DMD)専用のPMIC/RGB LEDドライバです。これらのチップセットを高い信頼性で使用するには、DLPA1000の使用が必須です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DLPA1000	DSBGA (49)	2.40mm×2.40mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



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4 改訂履歴

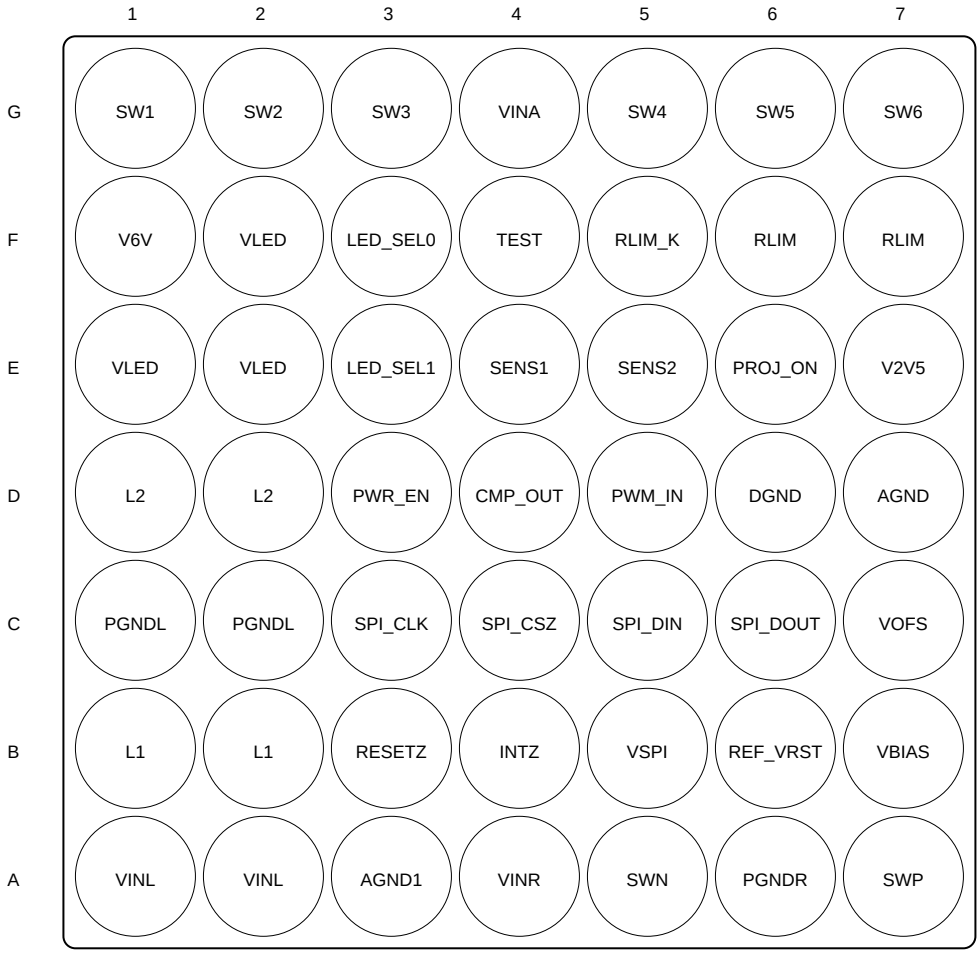
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5 Pin Configuration and Functions

YFF
49-Pin DSBGA
Bottom View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VINL	A1	POWER	Power supply input for VLED BUCK-BOOST power stage. Connect to system power.
VINL	A2	POWER	Power supply input for VLED BUCK-BOOST power stage. Connect to system power.
AGND1	A3	GND	Analog ground. Connect to ground plane.
VINR	A4	POWER	Power supply input for DMD switch mode power supply. Connect to system power.
SWN	A5	IN (A)	Connection for the DMD SMPS-inductor (high-side switch).
PGNDR	A6	GND	Power ground for DMD SMPS. Connect to ground plane.
SWP	A7	IN(A)	Connection for the DMD SMPS-inductor (low-side switch).
L1	B1	IN (A)	Connection for VLED BUCK-BOOST inductor.
L1	B2	IN(A)	Connection for VLED BUCK-BOOST inductor.
RESETZ	B3	OUT(D)	Reset output to the DLP system (active low). Pin is held low to reset DLP system.
INTZ	B4	OUT(D)	Interrupt output signal (open drain). Connect to pull-up resistor or short to ground.
VSPI	B5	POWER	Power Supply input for SPI interface. Connect to system I/O voltage.
REF_VRST	B6	IN(A)	Reference pin for the VRST regulator. Connect to VRST rail through 100-kΩ resistor.

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VBIAS	B7	OUT(A)	VBIAS output rail. Connect to ceramic capacitor.
PGNDL	C1	GND	Power ground for VLED BUCK-BOOST. Connect to ground plane.
PGNDL	C2	GND	Power ground for VLED BUCK-BOOST. Connect to ground plane.
SPI_CLK	C3	IN(D)	Clock input for SPI interface.
SPI_CSZ	C4	IN(D)	SPI chip select (active low).
SPI_DIN	C5	IN(D)	SPI data input.
SPI_DOUT	C6	OUT(D)	SPI data output.
VOFS	C7	OUT(A)	VOFS output rail. Connect to ceramic capacitor.
L2	D1	IN(A)	Connection for VLED BUCK-BOOST inductor.
L2	D2	IN(A)	Connection for VLED BUCK-BOOST inductor.
PWR_EN	D3	OUT(D)	Enable pin for the external power supplies (active high).
CMP_OUT	D4	OUT(A)	Analog-comparator output.
PWM_IN	D5	IN(D)	Reference voltage input for analog comparator.
DGND	D6	GND	Digital ground. Connect to ground plane.
AGND	D7	GND	Analog ground. Connect to ground plane.
VLED	E1	OUT (A)	VLED BUCK-BOOST converter output pin.
VLED	E2	OUT(A)	VLED BUCK-BOOST converter output pin.
LED_SEL1	E3	IN(D)	Digital input to the RGB STROBE DECODER.
SENS1	E4	IN(A)	Input signal from light sensor.
SENS2	E5	IN(A)	Input signal from temperature sensor.
PROJ_ON	E6	IN(D)	Input signal to enable/disable the IC and DLP projector.
V2V5	E7	OUT (D)	Internal supply filter pin for digital logic. Typical 2.45 V.
V6V	F1	OUT(D)	Internal supply filter pin for gate driver circuitry. Typical 6 V.
VLED	F2	OUT(A)	VLED BUCK-BOOST converter output pin.
LED_SEL0	F3	IN(D)	Digital input to the RGB STROBE DECODER.
TEST	F4	IN(D)	Test pin for digital, must be tied to the output capacitor of V2V5.
RLIM_K	F5	IN(A)	Kelvin sense connection for LED current sense resistor. For best accuracy, route signal with a dedicated trace separated from F6/F7 and connect directly at sense resistor.
RLIM	F6	OUT(A)	Connection to LED current sense resistor. Connect to a 100-mΩ resistor.
RLIM	F7	OUT(A)	Connection to LED current sense resistor. Connect to pin F6.
SW1	G1	OUT(A)	High-side MOSFET switch for LED anode. Connect to RGB LED assembly. If output is not used, short to VLED.
SW2	G2	OUT(A)	High-side MOSFET switch for LED anode. Connect to RGB LED assembly. If output is not used, short to VLED.
SW3	G3	OUT(A)	High-side MOSFET switch for LED anode. Connect to RGB LED assembly. If output is not used, short to VLED.
VINA	G4	POWER	Power supply input for sensitive analog circuitry.
SW4	G5	OUT(A)	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
SW5	G6	OUT(A)	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.
SW6	G7	OUT(A)	Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Input voltage	VINL, VINA, VINR	–0.3	7	V
	Ground pins to system ground		–0.3	0.3	V
	Voltage	SWN	–18	7	V
		SWP, VBIAS	–0.3	20	
		VOFS	–0.3	10	
		V6V, VLED, L1, L2, SW1, SW2, SW3, SW4, SW5, SW6, INTZ, PROJ_ON	–0.3	7	
	All pins unless noted otherwise		–0.3	3.6	V
	Source current	RESETZ, PWR_EN, CMP_OUT	1		mA
		SPI_DOUT	5.5		
	Sink current	RESETZ, PWR_EN, CMP_OUT	1		mA
		SPI_DOUT, INTZ	5.5		
	Peak output current		Internally limited		mA
	Continuous total power dissipation		Internally limited		W
T_A	Operating ambient temperature		–30	85	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Input voltage at VINL, VINA, VINR	Full functional and parametric performance	2.7	3.6	6	V
		Extended operation, limited parametric performance	2.3	3.6	6	
	Voltage at VSPI		1.7	1.8	3.6	V
T_A	Operating ambient temperature		–10		85	°C
T_J	Operating junction temperature		–10		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		DLPA1000 YFF (DSBGA) 49 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 3.6 V, T_A = –10°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{IN}	Input voltage range	VINA, VINR, VINL	2.7	3.6	6	V
	Extended input voltage range[1]		2.3	3.6	6	
V_{LOW_BAT}	Low battery warning threshold	V_{INA} falling		3		V
	Hysteresis	V_{INA} rising		100		mV
V_{UVLO}	Undervoltage lockout threshold	V_{INA} falling		2.3		V
	Hysteresis	V_{INA} rising		100		mV
$V_{STARTUP}$	Startup voltage	VBIAS, VOFS, VRST loaded with 2 mA	2.5			V
INPUT CURRENT						
I_Q		ACTIVE2 mode		12		mA
I_{STD}		STANDBY mode		360		µA
I_{SLEEP}		SLEEP mode		10		µA
INTERNAL SUPPLIES						
V_{V6V}	Internal supply, analog			6.25		V
C_{LDO_V6V}	Filter capacitor for V6V LDO			100		nF
V_{V2V5}	Internal supply, logic			2.5		V
C_{LDO_V2V5}	Filter capacitor for V2V5 LDO			2.2		µF
DMD REGULATOR						
$R_{DS(ON)}$	MOSFET on resistance	Switch E (from VINR to SWN)		1000		mΩ
		Switch F (from SWP to PGND)		320		
V_{FW}	Forward voltage drop	Switch G (from SWP to VBIAS)[2] VINR = 5 V, VSWP = 2 V, I_F = 100 mA		1.3		V
		Switch H (from SWP to VOFS) VINR = 5 V, VSWP = 2 V, I_F = 100 mA		1.3		
R_{DIS}	Discharge resistor (SWP to GND)	Active when all rails are disabled		2		kΩ
t_{PG}	Power-good timeout	Not tested in production		6		ms
I_{LIMIT}	Switch current limit			200[3]		mA
L	Inductor value			10		µH

(1) Full functional but limited parametric performance.
(2) Including rectifying diode.
(3) Contact factory for 100-mA and 300-mA options.

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_A = –10°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OFS} REGULATOR						
V_{OFS}	Output voltage			8.5		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–2%		2%	
	DC load regulation	V_{IN} = 3.6 V, I_{OUT}= 0 mA to 4 mA		–19		V/A
	DC line regulation	VINA, VINL, VINR 2.7 V to 6 V, I_{OUT} = 2 mA		35		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 4 mA, C_{OUT} = 220 nF		240		mV
I_{OUT}	Output current		0		3	mA
PG	Power-good threshold (fraction of nominal output voltage)	V_{OFS} rising		85%		
		V_{OFS} falling		62%		
R_{DIS}	Output discharge resistor	Active when rail is disabled		2		kΩ
C	Output capacitor	Recommended value	110	220		nF
V_{BIAS} REGULATOR						
V_{BIAS}	Output voltage			16		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–2%		2%	
	DC load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 mA to 4 mA		–14		V/A
	DC line regulation	VINA, VINL, VINR 2.7 V to 6 V, I_{OUT} = 2 mA		18		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 4 mA, C_{OUT} = 220 nF		240		mV
I_{OUT}	Output current		0		4	mA
PG	Power-good threshold (fraction of nominal output voltage)	V_{OFS} rising		85%		
		V_{OFS} falling		62%		
R_{DIS}	Output discharge resistor	Active when rail is disabled		2		kΩ
C	Output capacitor	Recommended value	110	220		nF
V_{RST} REGULATOR						
V_{RST}	Output voltage			–10		V
	DC output voltage accuracy	I_{OUT} = 2 mA	–2%		2%	
	DC load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 mA to 4 mA		13		V/A
	DC line regulation	VINA, VINL, VINR 2.7 V to 6 V, I_{OUT} = 2 mA		–21		mV/V
V_{RIPPLE}	Output ripple	V_{IN} = 3.6 V, I_{OUT} = 4 mA, C_{OUT} = 220 nF		240		mV
V_{REF_VRST}	Reference voltage			500		mV
I_{OUT}	Output current		0		4	mA
PG	Power-good threshold			–9.1		V
C	Output capacitor	Recommended value	110	220		nF
V_{LED} BUCK-BOOST						
V_{LED}	Output voltage range		1.2		5.9	V
	Default output voltage	SW4/5/6 in OPEN position		3.5		
V_{OVP}	Output overvoltage protection	Clamps buck-boost output		5.9		V
V_{LED_OVP}	Fault detection threshold	Triggers VLED_OVP interrupt		5.4		V
I_{SW}	Switch current limit		1.65	2.2	2.5	A
$R_{DS(ON)}$	MOSFET on resistance	Switch A (from VINL to L1)		100		mΩ
		Switch B (from L1 to GND)		100		
		Switch C (from L2 to GND)		100		
		Switch D (from L2 to VLED)		100		
f_{SW}	Switching frequency			2.25		MHz
C_{OUT}	Output capacitance			2 × 10		µF

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_A = –10°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RGB STROBE CONTROLLER SWITCHES						
$R_{DS(ON)}$	Drain-source on resistance	SW1, SW2, SW3		50	100	mΩ
		SW4, SW5, SW6		40	100	
I_{LEAK}	Off-state leakage current	VDS = 5 V			1	µA
LED CURRENT CONTROL						
V_f	LED forward voltage	I_{LED} = 1 A			4.8	V
I_{LED}	Maximum LED drive current	V_{IN} = 3.1 V, V_{LED} = 4.4 V		700		mA
		V_{IN} = 4 V, V_{LED} = 4.4 V		1000		
	DC current accuracy, SW4, 5, 6	SWx_IDAC[9:0] = 0x100h R_{LIM} = 100 mΩ, 0.1%, T_A = 25°C	258	272	286	mA
	Transient LED current limit range	ILIM[2:0] = 000		260		mA
		ILIM[2:0] = 111		1250		
t_{rise}	Current rise time(4)	I_{LED} from 5% to 95%, I_{LED} = 300 mA, transient current limit disabled			50	µs
MEASUREMENT SYSTEM (AFE)						
G	Amplifier gain (PGA)	AFE_GAIN[1:0] = 01		1		V/V
		AFE_GAIN[1:0] = 10		9.5		
		AFE_GAIN[1:0] = 11		18		
V_{OFS}	Input referred offset voltage(4)	PGA, AFE_CAL_DIS = 1	–1		1	mV
		Comparator	–1.5		1.5	
t_{settle}	Settling time(4)	To 1% of final value		15		µs
		To 0.1% of final value		52		
f_{sample}	Sampling rate(4)				19	kHz
LOGIC LEVELS AND TIMING CHARACTERISTICS						
V_{OL}	Output low-level	I_O = 0.5 mA, sink current (RESETZ, PWR_EN, CMP_OUT)	0		0.3	V
		I_O = 5 mA, sink current (SPI_DOUT, INTZ)	0		0.3	
V_{OH}	Output high-level	I_O = 0.5 mA, source current (RESETZ, PWR_EN, CMP_OUT)	1.3		2.5	V
		I_O = 5 mA, sink current (SPI_DOUT)	1.3		2.5	
V_{IL}	Input low-level	TEST, PROJ_ON, LED_SEL0, LED_SEL1, SPI_CSZ, SPI_CLK, SPI_DIN			0.4	V
V_{IH}	Input high-level	TEST, PROJ_ON, LED_SEL0, LED_SEL1, SPI_CSZ, SPI_CLK, SPI_DIN	1.2			V
$I_{(bias)}$	Input bias current	V_{IO} = 3.3 V Any input pin			0.5	µA
$t_{deglitch}$	Deglitch time(4)	(PROJ_ON, TEST) pins		1		ms
		(LED_SEL0, LED_SEL1) pins		300		ns

(4) Not tested in production.

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_A = –10°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A = –40°C to 85°C	–10%		10%	
THERMAL SHUTDOWN						
T_{WARN}	Thermal warning (HOT threshold)			120		°C
	Hysteresis			10		
T_{SHTDWN}	Thermal shutdown (TSD threshold)			150		°C
	Hysteresis			15		

6.6 Timing Requirements

V_{BAT} = 3.6 V ±5%, T_A = 25°C, C_L = 10 pF (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
f_{CLK}	Serial clock frequency	0		33.34	MHz
t_{CLKL}	Pulse width low, SPI_CLK, 50% level	10			ns
t_{CLKH}	Pulse width high, SPI_CLK, 50% level	10			ns
t_t	Transition time, 20% to 80% level, all signals	0.2		4	ns
t_{CSCR}	SPI_CSZ falling to SPI_CLK rising, 50% level	8			ns
t_{CFCS}	SPI_CLK falling to SPI_CSZ rising, 50% level			1	ns
t_{CDS}	SPI_DIN data setup time, 50% level	7			ns
t_{CDH}	SPI_DIN data hold time, 50% level	6			ns
t_{iS}	SPI_DOUT data setup time(1), 50% level	10			ns
t_{iH}	SPI_DOUT data hold time(1), 50% level	0			ns
t_{CFDO}	SPI_CLK falling to SPI_DOUT data valid, 50% level			13	ns
t_{CSZ}	SPI_CSZ rising to SPI_DOUT HiZ			6	ns

(1) The DPPxxxx processors send and receive data on the falling edge of the clock.

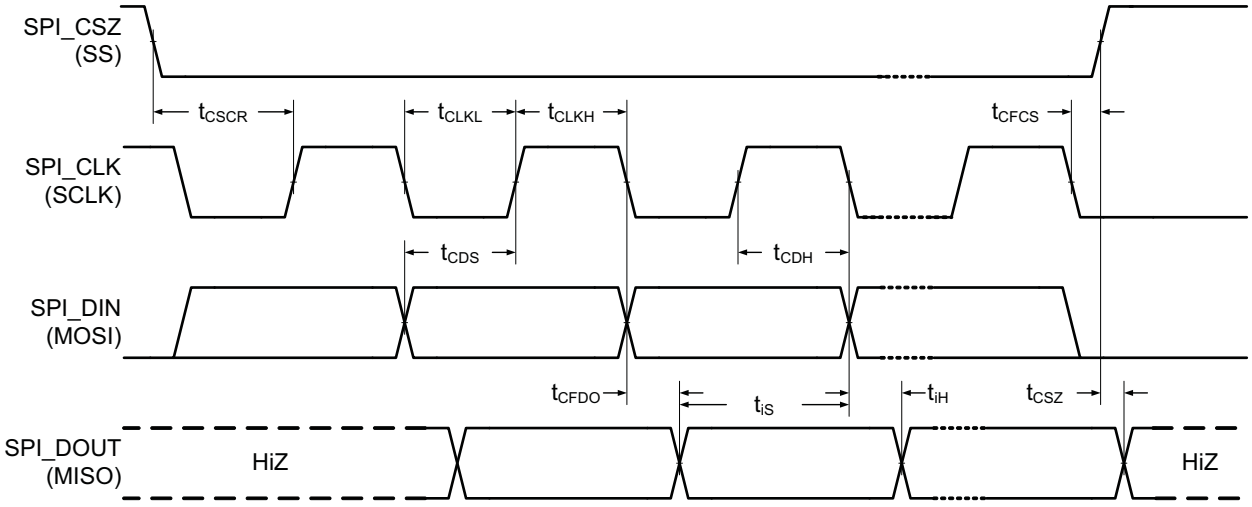
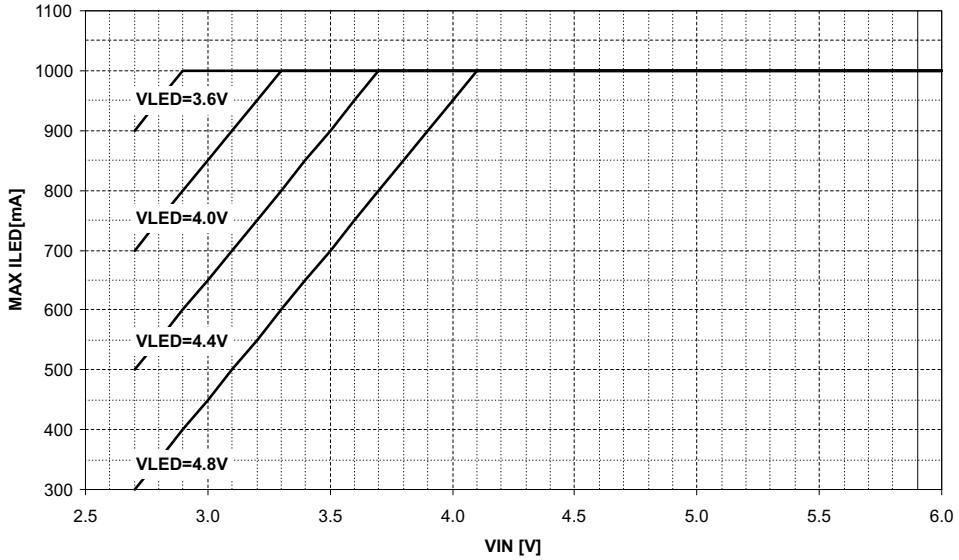


Figure 1. SPI Timing Diagram

6.7 Typical Characteristics

The maximum output current of the buck-boost is a function of input voltage (VIN), and output voltage (VLED). The relationship between VIN, VLED, and MAX ILED is shown in Figure 2. Please note that VLED is the output of the buck-boost regulator which includes the voltage drop across the sense resistor (100 mΩ), internal strobe control switch (100-mΩ max), and the forward voltage of the LED. For example, to drive 1-A of current through a LED with V_f = 4.2 V, the minimum input voltage needs to be ≥ 3.7 V (V_{LED} = 4.2 V + 1 A × 100 mΩ + 1 A × 100 mΩ = 4.4 V). For an input voltage of 3.1 V and a drive current of 700 mA, the max VLED voltage cannot exceed 4.4 V.



Measured on a typical unit. Note that VLED is the output of the buck-boost regulator and includes the voltage drop across the sense resistor, internal strobe control switch, and the forward voltage of the LED.

Figure 2. Maximum LED Output Current as a Function of Input Voltage (VIN) and BB Output Voltage (VLED)

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7 Detailed Description

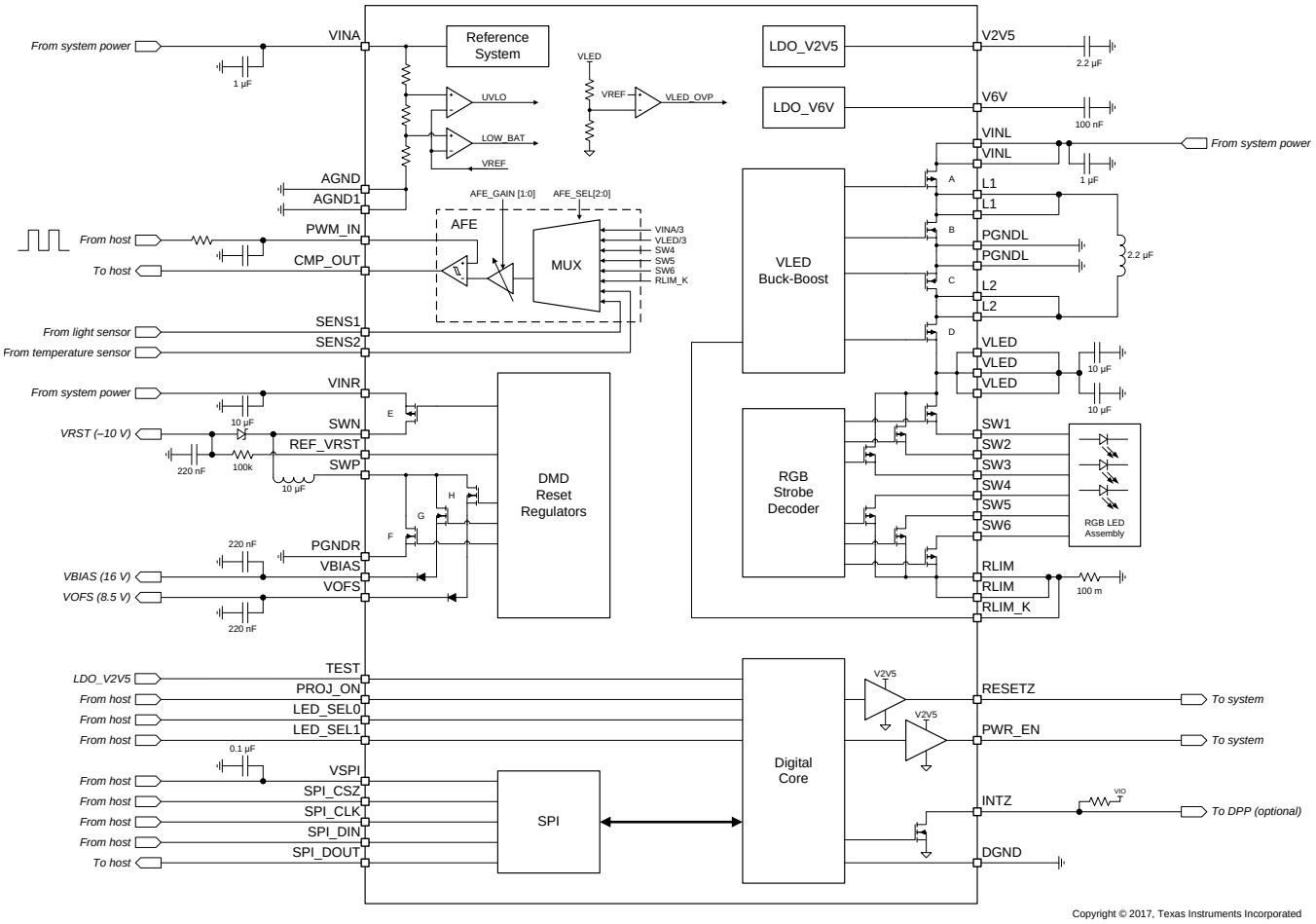
7.1 Overview

DLPA1000 is a power management IC optimized for TI DLP® Pico™ Projector systems and meant for use in either embedded or accessory mobile phone applications. For embedded applications, the projector is built into the mobile phone and operates from the mobile phone's single cell battery. In accessory applications, the projector resides in its own enclosure and has its own battery or external power supply and operates as a stand-alone device.

DLPA1000 contains a complete LED driver and can supply up to 1 A per LED. Integrated high-current switches are included for sequentially selecting a red, green, or blue LED. The DLPA1000 also contains three regulated DC supplies for the DMD: VBIAS, VRST and VOFS.

The DLPA1000 contains a serial periphery interface (SPI) used for setting the configuration. Using SPI, currents can be set independently for each LED with 10-bit resolution. Other features included are the generation of the system reset, power sequencing, input signals for sequentially selecting the active LED, IC self-protection, and an analog multiplexer and comparator to support A/D conversion of system parameters.

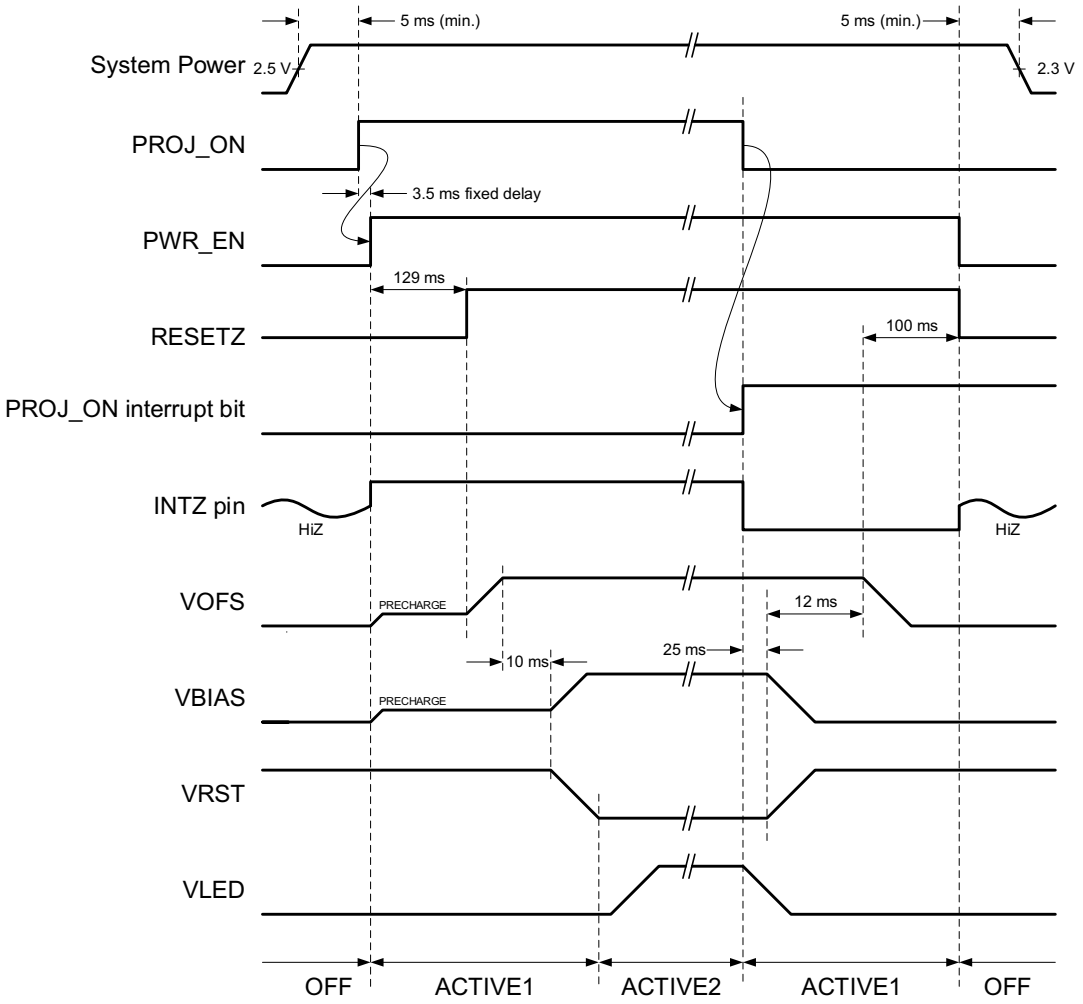
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 DMD Regulators

DLPA1000 contains three switch-mode power supplies that power the DMD. These rails are VOFS, VBIAS, and VRST. 100 ms after pulling the PROJ_ON pin high, VOFS is powered up, followed by VBIAS and VRST with an additional 10-ms delay. Only after all three rails are enabled can the LED driver and STROBE DECODER circuit be enabled. If any one of the rails encounters a fault such as an output short, all three rails are disabled simultaneously. The detailed power-up and power-down diagram is shown in Figure 3.



Power-up or down is initiated by pulling the PROJ_ON pin high or low, respectively. Upon pulling PROJ_ON high, the device enters ACTIVE2 mode immediately because DMD_EN and VLED_EN bits default to 1.

Figure 3. Power-Up and Power-Down Timing of the DMD REGULATOR and VLED Supplies

7.3.2 RGB Strobe Decoder

DLPA1000 contains RGB color-sequential circuitry that is composed of six NMOS switches, the LED driver, the strobe decoder and the LED current control. The NMOS switches are connected to the terminals of the external LED package and turn the currents through the LEDs on and off. The strobe decoder controls the gates of the NMOS switches according to the LED_SEL[1:0] input signals and the MAP bit of the SYSTEM register. The MAP bit selects one of two package configurations. A ‘1’ indicates a cathode-cathode-anode package and a ‘0’ indicates the common anode package. The two package connections are shown in Figure 4 and the corresponding switch map in Table 1 and Table 2.

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Feature Description (continued)

The LED_SEL[1:0] signals typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. When the LED_SEL[1:0] input signals select a specific color, the NMOSFETs are controlled based on the color selected, and a 10-bit current control DAC for this color is selected that provides a color correction current to the RGB LEDs feedback control network.

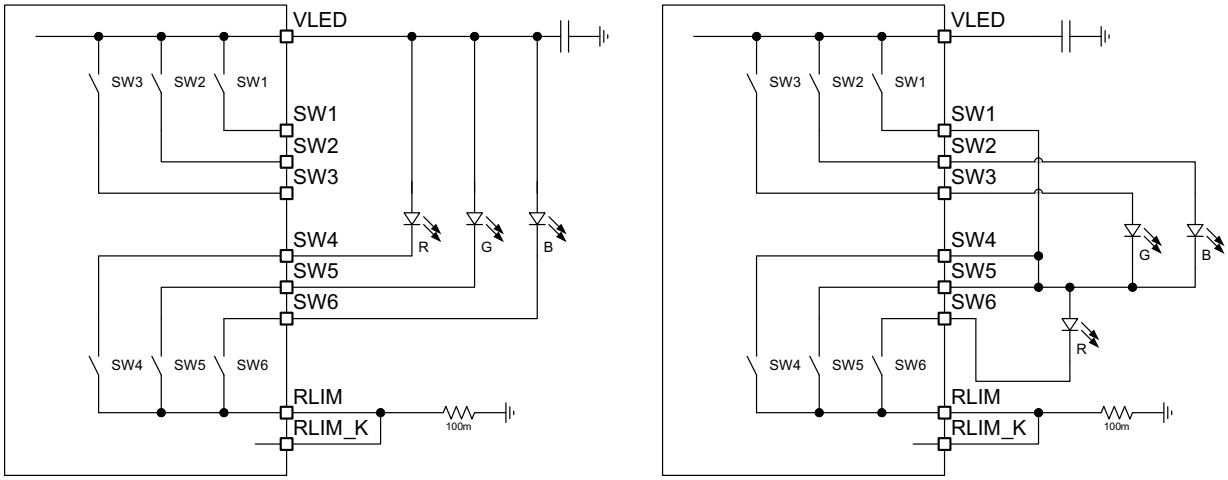


Figure 4. LEFT: Switch Connection for a Common-Anode LED Assembly
RIGHT: Switch Connection for a Cathode-Cathode-Anode LED Assembly

Table 1. Switch Positions for Common Anode RGB LEDs (MAP = 0)

MAP = 0 (Common Anode, Default)							
LED_SEL[1:0]	**SW6**	**SW5**	**SW4**	**SW3**	**SW2**	**SW1**	**IDAC input**
0x00h	open	open	open	closed	closed	closed	N/A
0x01h	open	open	closed	closed	closed	closed	SW4_IDAC[9:0]
0x02h	open	closed	open	closed	closed	closed	SW5_IDAC[9:0]
0x03h	closed	open	open	closed	closed	closed	SW6_IDAC[9:0]

Table 2. Switch Positions for Cathode-Cathode-Anode RGB LEDs (MAP = 1)

MAP = 1 (Cathode-Cathode-Anode LED Arrangement)							
LED_SEL[1:0]	**SW6**	**SW5**	**SW4**	**SW3**	**SW2**	**SW1**	**IDAC input**
0x00h	open	open	open	open	open	open	N/A
0x01h	closed	open	open	open	open	closed	SW4_IDAC[9:0]
0x02h	open	closed	closed	closed	open	open	SW5_IDAC[9:0]
0x03h	open	closed	closed	open	closed	open	SW6_IDAC[9:0]

The switching of the six NMOS switches is controlled such that switches are returned to the OPEN position first before the CLOSED connections are made (Break Before Make). The dead time between opening and closing switches is controlled through the BBM register. Switches that already are in the CLOSED position and are to remain in the CLOSED state according to the SWCNTRL register, are not opened during the BBM delay time.

7.3.3 LED Current Control

DLPA1000 provides time-sequential circuitry to drive three LEDs with independent current control. A system based on a common anode LED configuration is shown in Figure 6 and consists of a buck-boost converter which provides the voltage to drive the LEDs, three switches connected to the cathodes of the LEDs, a 100-mΩ resistor used to sense the LED current, and a current DAC to control the LED current.

The STROBE DECODER controls the switch positions as described in the section above. With all switches in the OPEN position, the buck-boost output assumes an output voltage of 3.5 V.

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For a common-anode RGB LED configuration (MAP = 0, default), the BUCK-BOOST output voltage (VLED) assumes a value such that the voltage drop across the sense resistor equals (SW4_IDAC[9:0] × 100 mΩ) when SW4 is closed. The exact value of VLED depends on the current setting and the voltage drop across the LED but is limited to 6.5 V. When the STROBE decoder switches from SW4 to SW5, the Buck-Boost assumes a new output voltage such that the sense voltage equals (SW5_IDAC[9:0] × 100 mΩ), and finally, when SW6 is selected, $V_{(RLIM_K)}$ is regulated to (SW6_IDAC[9:0] × 100 mΩ).

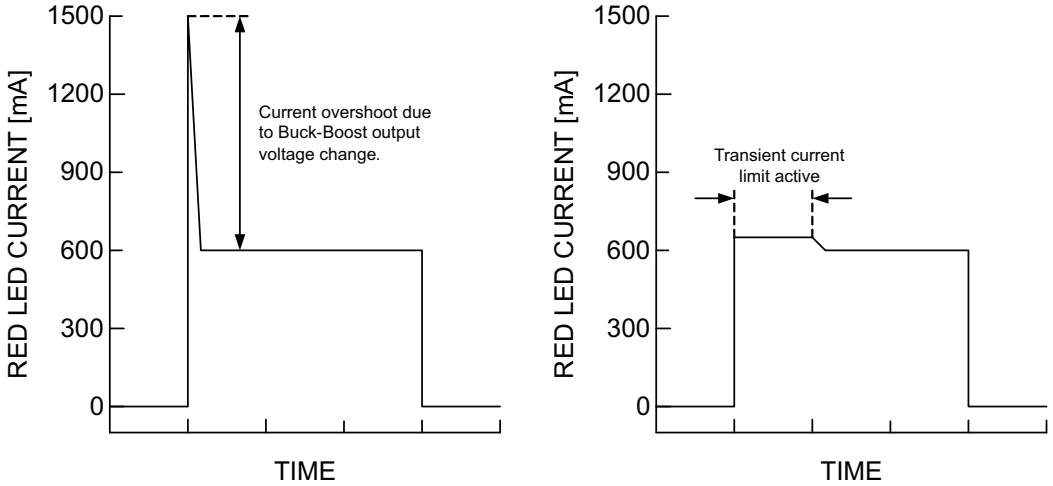
Similarly, the regulation current setting switches from SW4_IDAC[9:0] to SW5_IDAC[9:0] to SW6_IDAC[9:0] depending on the LED_SEL[1:0] setting with a MAP setting of 1 (cathode-cathode-anode configuration). See Table 2 for details.

7.3.3.1 LED Current Accuracy

LED drive current is controlled by a current DAC (digital to analog converter) and can be set independently for switch SW4, SW5, and SW6. The DAC is trimmed to achieve a LED drive current of 272 mA at code 0x100h with an accuracy of ±14 mA. The first order gain-error of the DAC can be neglected, therefore the LED driver current accuracy of ±14 mA can be assumed over the full current range. For example, at full-scale (SWx_IDAC[9:0] = 0x3FFh) the LED current is regulated to 1030 mA ±14 mA or ±1.4%. At the lowest setting (0x001h) the LED current is regulated to 20 mA ±14 mA and the resulting relative error is large; however this is not a typical operating point for a projector application. A typical drive current for projection LEDs is 300 mA and the resulting regulation error is < 5%.

7.3.3.2 Transient Current Limiting

Typically the forward voltages of the GREEN and BLUE diodes are close to each other (~3 V to 4 V) but V_f of the RED diode is significantly lower (1.8 V to 2.5 V). This can lead to a current spike in the RED diode when the strobe controller switches from GREEN or BLUE to RED because VLED is regulated to a higher voltage than required to drive the RED diode. DLPA1000 provides transient current limiting for each switch to limit the current in the LEDs during the transition. The transient current limit value is controlled through the ILIM[2:0] bits in the IREG register. The same register also contains three bits to select which switch employs the transient current limiting feature. In a typical application it is required only for the RED diode and the ILIM[2:0] value should be set approximately 10% higher than the DC regulation current. The effect that the transient current limit has on the LED current is shown in Figure 5.



LEFT: RED LED current without transient current limit. The current overshoots because the buck-boost voltage starts at the (higher) level of the GREEN or BLUE LED.

RIGHT: LED current with transient current limit.

Figure 5. RED LED Current With and Without Transient Current Limit

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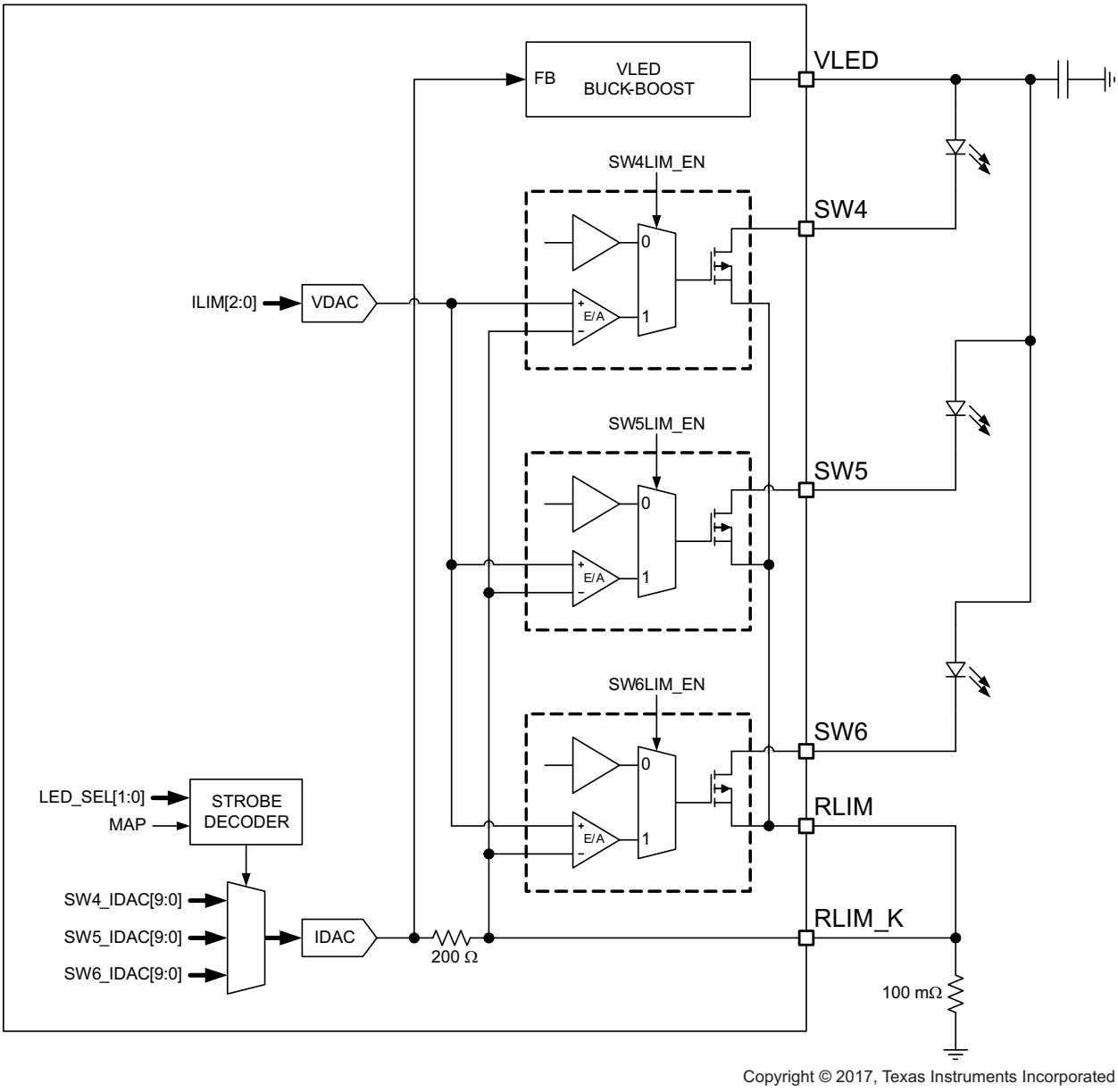


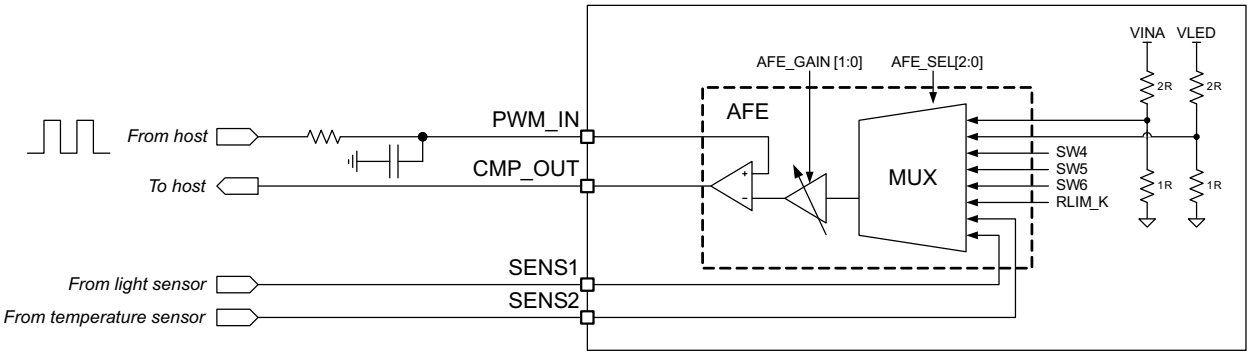
Figure 6. Block Diagram of the LED Driver Circuitry

7.3.4 Measurement System

The measurement system is composed of a 8:1 analog multiplexer (MUX), a programmable-gain amplifier and a comparator. It works together with the DPP processor to provide:

- White-point correction (WPC) by independently adjusting the R/G/B LED currents, after measuring the brightness of each color from an external light sensor.
- A measurement of the battery voltage.
- A measurement of the LED forward voltage.
- A measurement of the exact LED current.
- A measurement of temperature as derived by measuring the voltage across an external thermistor.

A block diagram of the measurement system is shown in Figure 7.



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Figure 7. Block Diagram of the Measurement System

Table 3. Recommended Configuration of the AFE for Different Input Selections

AFE_SEL[2:0]	SELECTED INPUT	RECOMMENDED GAIN SETTING AFE-GAIN[1:0]	RECOMMENDED SETTING OF AFE_CAL_DIS BIT
0x00h	SENS2	0x01h (1x)	Setting has no effect on measurement
0x01h	VLED	0x01h (1x)	Setting has no effect on measurement
0x02h	VINA	0x01h (1x)	Setting has no effect on measurement
0x03h	SENS1	0x01h (1x)	Setting has no effect on measurement
0x04h	RLIM_K	0x03h (18x)	Set to 1 if sense voltage is > 100 mV, otherwise set to 0 (default).
0x05h	SW4	0x02h (9.5x)	Set to 1 if sense voltage is > 200 mV, otherwise set to 0 (default).
0x06h	SW5	0x02h (9.5x)	Set to 1 if sense voltage is > 200 mV, otherwise set to 0 (default).
0x07h	SW6	0x02h (9.5x)	Set to 1 if sense voltage is > 200 mV, otherwise set to 0 (default).

7.3.5 Protection Circuits

DLPA1000 has several protection circuits to protect the IC as well as the system from damage due to excessive power consumption, die temperature, or over-voltages. These circuits are described below.

7.3.5.1 Thermal Warning (HOT) and Thermal Shutdown (TSD)

DLPA1000 continuously monitors the junction temperature and issues a HOT interrupt if temperature exceeds the HOT threshold. If the temperature continues to increase above the thermal shutdown threshold, all rails are disabled and the TSD bit in the INT register is set. Once the temperature drops by 15°C, the output rails are powered up in sequence and normal operation resumes (DMD_EN bit is not reset by TSD fault).

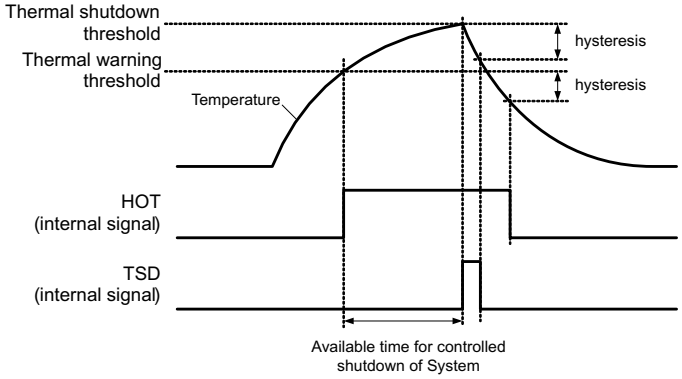


Figure 8. Definition of the Thermal Shutdown and Hot-Die Temperature Warning

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7.3.5.2 Low Battery Warning (BAT_LOW) and Undervoltage Lockout (UVLO)

If the battery voltage drops below the BAT_LOW threshold (typically 3 V) the BAT_LOW interrupt is issued but normal operation continues. Once the battery drops below the undervoltage threshold (typically 2.3 V) the UVLO interrupt is issued, all rails are powered down in sequence, the DMD_EN bit is reset, and the part enters STANDBY mode. The power rails cannot be re-enabled before the input voltage recovers to > 2.4 V. To re-enable the rails, the PROJ_ON pin must be toggled.

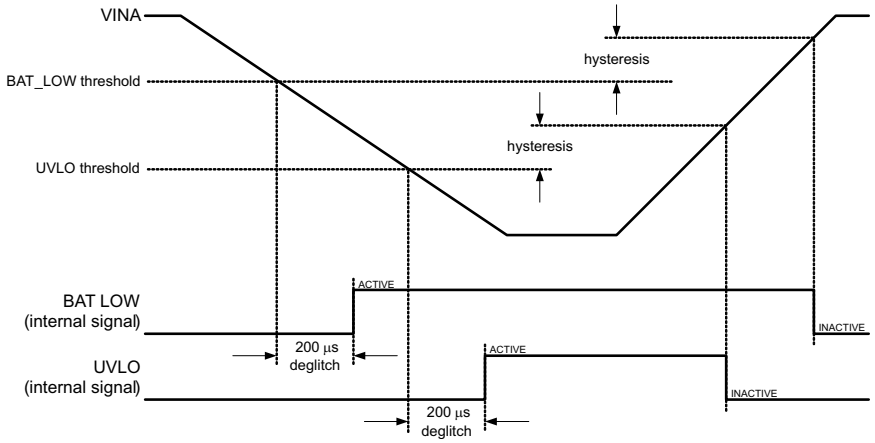


Figure 9. Undervoltage Lockout is Asserted When the Input Supply Drops Below the UVLO Threshold

7.3.5.3 DMD Regulator Fault (DMD_FLT)

The DMD regulator is continuously monitored to check if the output rails are in regulation and if the inductor current increases as expected during a switching cycle. If either one of the output rails drops out of regulation (e.g. due to a shorted output) or the inductor current does not increase as expected during a switching cycle (due to a disconnected inductor), the DMD_FLT interrupt bit is set in the INT register, the DMD_EN bit is reset, and the DMD regulator is shut down. Resetting the DMD_EN bit also causes the LED driver to power down. To restart the system, the PROJ_ON pin must be toggled.

7.3.5.4 V6V Power-Good (V6V_PGF) Fault

The VLED buck-boost requires the V6V rail for proper operation. The rail is continuously monitored and should the output drop below the power-good threshold, the V6V_PGF bit is set. The buck-boost is disabled and attempts to restart automatically.

7.3.5.5 VLED Over-Voltage (VLED_OVP) Fault

If the buck-boost output voltage rises above 6.5 V, the VLED_OVP interrupt is set but the buck-boost regulator is not turned off. A typical condition to cause this fault is an open LED.

7.3.6 Interrupt Pin (INTZ)

The interrupt pin is used to signal events and fault conditions to the host processor. Whenever a fault or event occurs in the IC, the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The INTZ pin is released (returns to HiZ state) and fault bits are cleared when the INT register is read by the host. However, if a failure persists, the corresponding INT bit remains set and the INTZ pin is pulled low again after a maximum of 32 µs.

Interrupt events include fault conditions such as power-good faults, over-voltage, over-temperature shut-down, and under-voltage lock-out.

The MASK register is used to mask events from generating interrupts, i.e. from pulling the INTZ pin low. The MASK settings affect the INTZ pin only and have no impact on protection and monitor circuits themselves. When an interrupt is masked, the event causing the interrupt still sets the corresponding bit in the INT register. However, it does not pull the INTZ pin low.

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Note that persisting fault conditions such as thermal shutdown can cause the INTZ pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT register to see when the fault condition has disappeared. After the fault is resolved, unmask the interrupt bit again.

7.3.7 Serial Peripheral Interface (SPI)

DLPA1000 provides a 4-wire SPI port that supports high-speed serial data transfers up to 33.3 MHz. Register and data buffer write and read operations are supported. The SPI_CSZ input serves as the active low chip select for the SPI port. The SPI_CSZ input must be forced low in order to write or read registers and data buffers. When SPI_CSZ is forced high, the data at the SPI_DIN input is ignored, and the SPI_DOUT output is forced to a high-impedance state. The SPI_DIN input serves as the serial data input for the port; the SPI_DOUT output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data is latched at the SPI_DIN input on the rising edge of SPI_CLK, while data is clocked out of the SPI_DOUT output on the falling edge of SPI_CLK. Figure 10 illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in Figure 10, the auto-increment mode is invoked by simply holding the SPI_CSZ input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

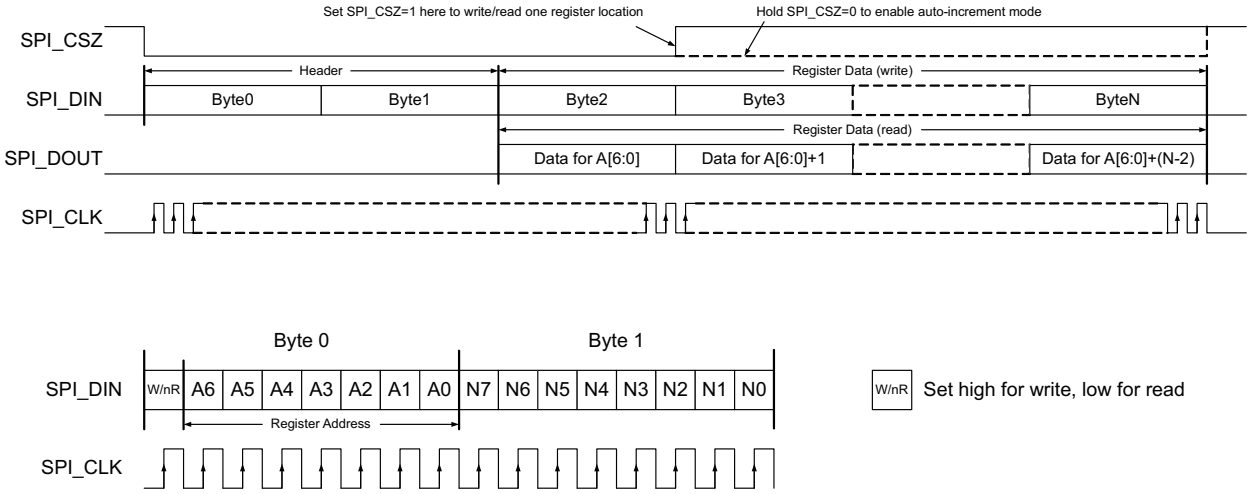


Figure 10. SPI Protocol

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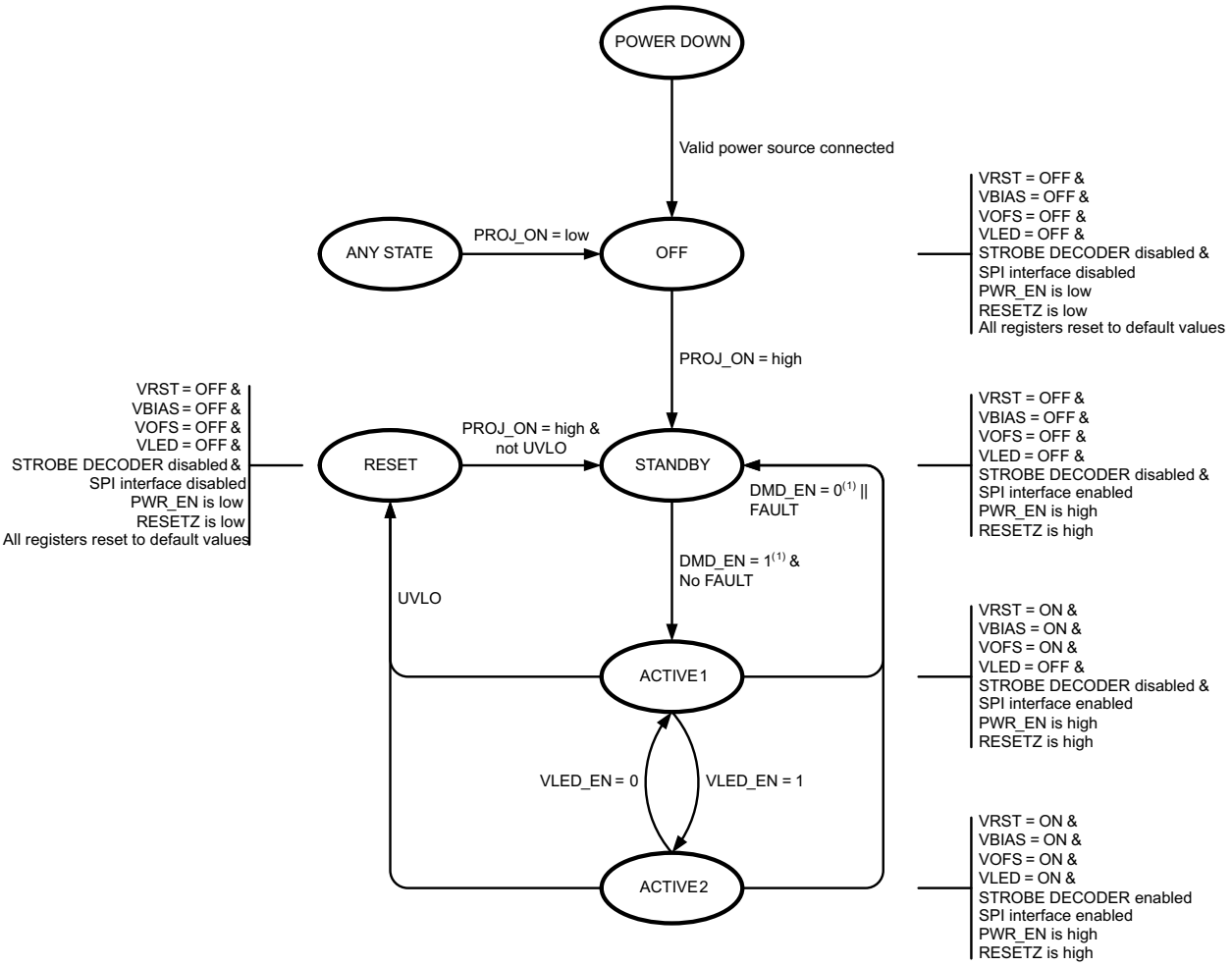
7.4 Device Functional Modes

Table 4. Modes of Operation

MODE	DESCRIPTION
OFF	This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values and the IC does not respond to SPI commands. RESETZ and PWR_EN pins are pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is pulled low.
RESET	Logic core and registers are reset to default values, the IC does not respond to SPI commands, RESETZ and PWR_EN pins are pulled low, but the analog reference system is kept alive. The device enters RESET state when the input voltage drops below the UVLO threshold.
STANDBY	All power functions are turned off but the IC does respond to the SPI interface. The device enters STANDBY mode when PROJ_ON pins is high, but DMD_EN bit is set to 0. Also, device enters STANDBY mode when a fault on the DMD regulator occurs or the temperature increases above thermal shutdown threshold (TSD).(1)
ACTIVE1	The DMD supplies are powered up but LED power (VLED) and the STROBE DECODER are disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and VLED_EN bit set to 0.
ACTIVE2	DMD supplies, LED power and STROBE DECODER are enabled. PROJ_ON pin must be high and DMD_EN and VLED_EN bits must both be set to 1.

(1) DMD_EN power-up default is 1. Once the bit is set to 0, the PROJ_ON pin must be toggled to recover the bit to 1.

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NOTES:
|| = OR, & = AND, (↑) = rising edge, (↓) = falling edge

FAULT = Undervoltage on VRST, VBIAS, VOFS, or DMD regulator current-limit fault (DMD_FLT) || Thermal Shut Down (TSD)

DMD_PG and UVLO faults reset the DMD_EN bit and keep the part in STANDBY mode
TSD does not reset DMD_EN bit, so part resumes normal operation after the part has cooled off

(1) : DMD_EN bit power-up default is 1. The bit can be reset by writing to the ENABLE register but to set the bit back to 1 requires toggling of PROJ_ON

Figure 11. State Diagram

7.5 Programming

7.5.1 Password Protected Registers

Register address 0x11h through 0x27h can be read-accessed the same way as any other register but are protected against accidental write operations through the PASSWORD register (address 0x10h). To write to a protected register, first:

- Write data 0xBAh to register address 0x10h, then
- Write data 0xBEh to register address 0x10h.

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Programming (continued)

Both writes must be consecutive, i.e. there must be no other read or write operation in between sending the two bytes. Once the password has been successfully written, register 0x11h through 0x27h are unlocked and can be write accessed using the regular SPI protocol. They remain unlocked until any byte other than 0xBAh is written to the PASSWORD register or the part is power cycled.

To check if the registers are unlocked, read back the PASSWORD register. If the data returned is 0x00h, the registers are locked. If the PASSWORD register returns 0x01h, the registers are unlocked.

7.6 Register Maps

Table 5. Register Address Map

Address	Acronym	Register Name	Section
0x00h	CHIPID	Chip revision register	Go
0x01h	ENABLE	Enable register	Go
0x02h	IREG	Transient-current limit settings	Go
0x03h	SW4MSB	Regulation current MSBs, SW4	Go
0x04h	SW4LSB	Regulation current LSBs, SW4	Go
0x05h	SW5MSB	Regulation current MSBs, SW5	Go
0x06h	SW5LSB	Regulation current LSBs, SW5	Go
0x07h	SW6MSB	Regulation current MSBs, SW6	Go
0x08h	SW6LSB	Regulation current LSBs, SW6	Go
0x09h	RESERVED	Reserved	
0x0Ah	AFE	AFE (MUX) control	Go
0x0Bh	BBM	Break before make timing	Go
0x0Ch	INT	Interrupt register	Go
0x0Dh	INT MASK	Interrupt mask register	Go
0x10h	PASSWORD	Password register	Go
0x11h	SYSTEM	System configuration register	Go
0x20h	BYTE0	User EEPROM, Byte0	Go
0x21h	BYTE1	User EEPROM, Byte1	Go
0x22h	BYTE2	User EEPROM, Byte2	Go
0x23h	BYTE3	User EEPROM, Byte3	Go
0x24h	BYTE4	User EEPROM, Byte4	Go
0x25h	BYTE5	User EEPROM, Byte5	Go
0x26h	BYTE6	User EEPROM, Byte6	Go
0x27h	BYTE7	User EEPROM, Byte7	Go

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7.6.1 Chip ID (CHIPID) Register (address = 0x00h) [reset = A6h]

Figure 12. CHIPID Register

7	6	5	4	3	2	1	0
CHIPID[7:0]							
R-A6h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 6. CHIPID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIPID	R	A6h	1010 0000b = DLPA1000 (Rev 1p0) 1010 0010b = DLPA1000 (Rev 1p1) 1010 0110b = DLPA1000 (Rev 1p2)

7.6.2 Enable (ENABLE) Register (address = 0x01h) [reset = 3h]

Figure 13. ENABLE Register

7	6	5	4	3	2	1	0
RESERVED						DMD_EN	VLED_EN
R-0h						R/W-1h	R/W-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7. ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	N/A
1	DMD_EN	R/W	1h	DMD Regulator enable/status bit 0b = disabled (OFF) 1b = enabled (ON) NOTE: Power-up default is 1. Once set to 0, the PROJ_ON pin must be toggled to set the bit back to 1. If bit is set to 0, VLED buck-boost will automatically be disabled.
0	VLED_EN	R/W	1h	VLED Buck-Boost enable bit 0b = disabled (OFF) 1b = enabled (ON) NOTE: Bit does not reflect current status of VLED buck-boost. NOTE: If VLED is disabled, RGB Strobe Decoder will automatically be disabled

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7.6.3 Switch Transient Current Limit (IREG) Register (address = 0x02h) [reset = 28h]

Figure 14. IREG Register

7	6	5	4	3	2	1	0
RESERVED		ILIM[2:0]			SW6LIM_EN	SW5LIM_EN	SW4LIM_EN
R-0h		R/W-5h			R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 8. IREG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	N/A
5-3	ILIM[2:0]	R/W	5h	Transient current-limit 000b = 260 mA 001b = 300 mA 010b = 345 mA 011b = 385 mA 100b = 440 mA 101b = 660 mA 110b = 880 mA 111b = 1250 mA NOTE: Transient current limit should always be set higher than regulation current
2	SW6LIM_EN	R/W	0h	Transient current-limit enable for SW6 0b = transient current-limit is disabled 1b = transient current-limit is enabled
1	SW5LIM_EN	R/W	0h	Transient current-limit enable for SW5 0b = transient current-limit is disabled 1b = transient current-limit is enabled
0	SW4LIM_EN	R/W	0h	Transient current-limit enable for SW4 0b = transient current-limit is disabled 1b = transient current-limit is enabled

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7.6.4 SW4 LED DC Regulation Current, MSB (SW4MSB) Register (address = 0x03h) [reset = 0h]

Figure 15. SW4MSB Register

7	6	5	4	3	2	1	0
RESERVED						SW4_IDAC[9:8]	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9. SW4MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	N/A
1-0	SW4_IDAC[9:8]	R/W	0h	Switch4 DC regulation, most significant byte (MSB)

7.6.5 SW4 LED DC Regulation Current, LSB (SW4LSB) Register (address = 0x04h) [reset = 0h]

Figure 16. SW4LSB Register

7	6	5	4	3	2	1	0
SW4_IDAC[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 10. SW4LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW4_IDAC[7:0]	R/W	0h	Switch4 DC current limit, least significant byte (MSB)

SW4_IDAC[9:0]	LED CURRENT(1)	SW4_IDAC[9:0]	LED CURRENT(1)	SW4_IDAC[9:0]	LED CURRENT(1)	SW4_IDAC[9:0]	LED CURRENT(1)
0x000h	0 mA	0x100h	272 mA	0x200h	525 mA	0x300h	777.99 mA
0x001h	19.99 mA	0x101h	272.99 mA	0x201h	525.98 mA	0x301h	778.98 mA
0x002h	20.98 mA	0x102h	273.98 mA	0x202h	526.97 mA	0x302h	779.97 mA
...	...	...	...	...	...	...	...
0x0FEh	270.02 mA	0x1FEh	523.602 mA	0x2FEh	776.02 mA	0x3FEh	1029.01 mA
0x0FFh	271.01 mA	0x1FFh	524.01 mA	0x2FFh	777 mA	0x3FFh	1030 mA

(1) Values shown are for a typical unit at T_A = 25°C. Typical step size is 988 µA.

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7.6.6 SW5 LED DC Regulation Current, MSB (SW5MSB) Register (address = 0x05h) [reset = 0h]

Figure 17. SW5MSB Register

7	6	5	4	3	2	1	0
RESERVED						SW5_IDAC[9:8]	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 11. SW5MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	N/A
1-0	SW5_IDAC[9:8]	R/W	0h	Switch5 DC regulation, most significant byte (MSB)

7.6.7 SW5 LED DC Regulation Current, LSB (SW5LSB) Register (address = 0x06h) [reset = 0h]

Figure 18. SW5LSB Register

7	6	5	4	3	2	1	0
SW5_IDAC[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 12. SW5LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW5_IDAC[7:0]	R/W	0h	Switch5 DC current limit, least significant byte (LSB)

SW5_IDAC[9:0]	LED CURRENT(1)	SW5_IDAC[9:0]	LED CURRENT(1)	SW5_IDAC[9:0]	LED CURRENT(1)	SW5_IDAC[9:0]	LED CURRENT(1)
0x000h	0 mA	0x100h	272 mA	0x200h	525 mA	0x300h	777.99 mA
0x001h	19.99 mA	0x101h	272.99 mA	0x201h	525.98 mA	0x301h	778.98 mA
0x002h	20.98 mA	0x102h	273.98 mA	0x202h	526.97 mA	0x302h	779.97 mA
...	...	...	...	...	...	...	...
0x0FEh	270.02 mA	0x1FEh	523.602 mA	0x2FEh	776.02 mA	0x3FEh	1029.01 mA
0x0FFh	271.01 mA	0x1FFh	524.01 mA	0x2FFh	777 mA	0x3FFh	1030 mA

(1) Values shown are for a typical unit at T_A = 25°C. Typical step size is 988 µA.

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7.6.8 SW6 LED DC Regulation Current, MSB (SW6MSB) Register (address = 0x07h) [reset = 0h]

Figure 19. SW6MSB Register

7	6	5	4	3	2	1	0
RESERVED						SW6_IDAC[9:8]	
R-0h						R/W-0h	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 13. SW6MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	N/A
1-0	SW6_IDAC[9:8]	R/W	0h	Switch6 DC regulation, most significant byte (MSB)

7.6.9 SW6 LED DC Regulation Current, LSB (SW6LSB) Register (address = 0x08h) [reset = 0h]

Figure 20. SW6LSB Register

7	6	5	4	3	2	1	0
SW6_IDAC[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 14. SW6LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SW6_IDAC[7:0]	R/W	0h	Switch6 DC current limit, least significant byte (LSB)

SW6_IDAC[9:0]	LED CURRENT(1)	SW6_IDAC[9:0]	LED CURRENT(1)	SW6_IDAC[9:0]	LED CURRENT(1)	SW6_IDAC[9:0]	LED CURRENT(1)
0x000h	0 mA	0x100h	272 mA	0x200h	525 mA	0x300h	777.99 mA
0x001h	19.99 mA	0x101h	272.99 mA	0x201h	525.98 mA	0x301h	778.98 mA
0x002h	20.98 mA	0x102h	273.98 mA	0x202h	526.97 mA	0x302h	779.97 mA
...	...	...	...	...	...	...	...
0x0FEh	270.02 mA	0x1FEh	523.602 mA	0x2FEh	776.02 mA	0x3FEh	1029.01 mA
0x0FFh	271.01 mA	0x1FFh	524.01 mA	0x2FFh	777 mA	0x3FFh	1030 mA

(1) Values shown are for a typical unit at T_A = 25°C. Typical step size is 988 µA.

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7.6.10 Analog Front End Control (AFE) Register (address = 0x0Ah) [reset = 0h]

Figure 21. AFE Register

7	6	5	4	3	2	1	0
RESERVED	AFE_EN	AFE_CAL_DIS	AFE_GAIN[1:0]		AFE_SEL[2:0]		
R-0h	R-0h	R/W-0h	R/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. AFE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	N/A
6	AFE_EN	R	0h	Enable bit for AFE 0b = AFE is disabled 1b = AFE is enabled NOTE: Comparator output is in HiZ state when disabled.
5	AFE_CAL_DIS	R/W	0h	Calibration disable bit. Set this bit high to disable the factory calibration setting. May result in lower offset error if sensed input voltage level is significantly greater than 40 mV (see Table 3). 0b = Factory calibration setting is enabled 1b = Factory calibration setting is disabled
4-3	AFE_GAIN	R/W	0h	Gain setting of the programmable gain amplifier 00b = amplifier is off 01b = 1x 10b = 9.5x 11b = 18x
2-0	AFE_SEL[2:0]	R/W	0h	AFE Multiplexer control 000b = SENS2 001b = VLED 010b = VINA 011b = SENS1 100b = RLIM_K 101b = SW4 110b = SW5 111b = SW6

7.6.11 Strobe Decode - Break Before Make Timing Control (BBM) Register (address = 0x0Bh) [reset = 0h]

Figure 22. BBM Register

7	6	5	4	3	2	1	0
BBM[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. BBM Register Field Descriptions

Bit	Field	Type	Reset	Description			
7-0	BBM[7:0]	R/W	0h	Break before make timing. Time between opening one set of switches and closing the next set.(1)			
				0x00 = 222 ns 0x01 = 333 ns 0x02 = 444 ns ... 0x3E = 7104 ns 0x3F = 7215 ns	0x40 = 7326 ns 0x41 = 7437 ns 0x42 = 7548 ns ... 0x7E = 14208 ns 0x7F = 14319 ns	0x80 = 14430 ns 0x81 = 14451 ns 0x82 = 14652 ns ... 0xBE = 21312 ns 0xBF = 21423 ns	0xC0 = 21534 s 0xC1 = 21645 ns 0xC2 = 21756 ns ... 0xFE = 28416 ns 0xFF = 28527 ns

(1) It takes 333 ns to 444 ns to turn off the switches from the time a change occurs on LED_SEL[1:0].

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7.6.12 Interrupt (INT) Register (address = 0x0Ch) [reset = X]

Figure 23. INT Register

7	6	5	4	3	2	1	0
VLED_OVP	V6V_PGF	PROJ_ON	DMD_FLT	UVLO	BAT_LOW	TSD	HOT
R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset; X = undefined

Table 17. INT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VLED_OVP	R	X	VLED BUCK_BOOST over-voltage fault interrupt (normal operation resumes) 0b = No fault 1b = BUCK-BOOST output is above OVP threshold
6	V6V_PGF	R	X	V6V power-good fault interrupt. (normal operation resumes) 0b = No fault 1b = V6V is not in regulation
5	PROJ_ON	R	X	PROJ_ON interrupt (part enters OFF mode) 0b = PROJ_ON pin is pulled high, normal mode 1b = PROJ_ON pin is pulled low. Alerts the DPP that DMD regulator is about to shut down.
4	DMD_FLT	R	X	DMD REGULATOR FAULT (part enters STANDBY mode and DMD_EN bit is cleared) 0b = No fault 1b = The inductor current is not increasing at the correct rate. Likely to be caused by an open inductor or one of the regulator outputs has dropped below the power-good threshold. Likely to be caused by a short. NOTE: DMD_FLT resets DMD_EN bit to 0.
3	UVLO	R	X	Undervoltage lockout threshold (sensed at VINA pin) (part enters RESET state) 0b = Battery voltage is above the UVLO threshold 1b = Battery voltage has dropped below the UVLO threshold NOTE: UVLO resets DMD_EN bit to 0. 25ms after UVLO interrupt part enters RESET state with SPI disabled.
2	BAT_LOW	R	X	Low-Battery warning (sensed at VINA pin) (normal operation resumes) 0b = Battery voltage is above the low-battery threshold 1b = Battery voltage has dropped below the low-battery threshold
1	TSD	R	X	Thermal Shutdown interrupt (part enters STANDBY mode, DMD_EN bit is not cleared) 0b = Die temperature is below the thermal shut-down threshold 1b = Die temperature is above thermal shut-down threshold or has not cooled down enough to recover from TSD
0	HOT	R	X	Thermal warning interrupt (normal operation resumes) 0b = Die temperature is normal operating range 1b = Die temperature is above the HOT threshold or has not cooled down enough to recover from HOT

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7.6.13 Interrupt Mask (MASK) Register (address = 0x0Dh) [reset = 0h]

Figure 24. MASK Register

7	6	5	4	3	2	1	0
VLED_OVPM	V6V_PGM	PROJ_ONM	DMD_FLTM	UVLOM	BAT_LOWM	TSDM	HOTM
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 18. MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7	VLED_OVPM	R/W	0h	VLED BUCK_BOOST over-voltage fault interrupt mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
6	V6V_PGM	R/W	0h	VLED BUCK_BOOST power-good fault interrupt mask 0b = no fault 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
5	PROJ_ONM	R/W	0h	PROJ_ON interrupt mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
4	DMD_FLTM	R/W	0h	DMD REGULATOR fault mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
3	UVLOM	R/W	0h	Undervoltage lockout threshold (sensed at VINA pin) mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
2	BAT_LOWM	R/W	0h	Low-Battery warning (sensed at VINA pin) mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
1	TSDM	R/W	0h	Thermal Shutdown interrupt mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.
0	HOTM	R/W	0h	Thermal warning interrupt mask 0b = interrupt is not masked. 1b = Interrupt is masked. INTZ pin is not pulled low when interrupt bit is set.

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7.6.14 Password (PASSWORD) Register (address = 0x10h) [reset = 0h]

Figure 25. PASSWORD Register

7	6	5	4	3	2	1	0
PASSWORD[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. PASSWORD Register Field Descriptions

Bit	Field	Type	Reset	Description(1)
7-0	PASSWORD[7:0]	R/W	0h	To write-access protected registers write 0xBAh followed by 0xBEh to the register. Both writes need to be consecutive. To lock protected registers, write 0x00h. Reading the PASSWORD register returns 0x00h if the protected registers are locked for write access and 0x01h if they are unlocked.

(1) Protected registers can be read-accessed without writing to the PASSWORD register.

7.6.15 System Configuration (SYSTEM) Register (address = 0x11h) [reset = 0h]

Figure 26. SYSTEM Register

7	6	5	4	3	2	1	0
RESERVED					EEPROG	RESERVED	MAP
R-0h					R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 20. SYSTEM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0h	N/A
2	EEPROG	R/W	0h	EEPROM programming bit. When set high, BYTE0 through BYTE7 settings are committed to EEPROM and become new power-up default values. To program the EEPROM, set this bit high and back low after 50 ms. Power must not be interrupted during EEPROM programming to prevent loss of data.
1	RESERVED	R/W	0h	This bit should always be set to 0.
0	MAP	R/W	0h	Switch map selector bit: 0b = Common anode configuration 1b = Cathode-cathode-anode configuration NOTE: See switch control section for details.

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7.6.16 EEPROM User Register, Byte0 (BYTE0) (address = 0x20h) [reset = 0h]

Figure 27. BYTE0 Register

7	6	5	4	3	2	1	0
BYTE0[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. BYTE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE0[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

7.6.17 EEPROM User Register, Byte1 (BYTE1) (address = 0x21h) [reset = 0h]

Figure 28. BYTE1 Register

7	6	5	4	3	2	1	0
BYTE1[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 22. BYTE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE1[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

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7.6.18 EEPROM User Register, Byte2 (BYTE2) (address = 0x22h) [reset = 0h]

Figure 29. BYTE2 Register

7	6	5	4	3	2	1	0
BYTE2[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 23. BYTE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE2[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

7.6.19 EEPROM User Register, Byte3 (BYTE3) (address = 0x23h) [reset = 0h]

Figure 30. BYTE3 Register

7	6	5	4	3	2	1	0
BYTE3[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. BYTE3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE3[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

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7.6.20 EEPROM User Register, Byte4 (BYTE4) (address = 0x24h) [reset = 0h]

Figure 31. BYTE4 Register

7	6	5	4	3	2	1	0
BYTE4[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 25. BYTE4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE4[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

7.6.21 EEPROM User Register, Byte5 (BYTE5) (address = 0x25h) [reset = 0h]

Figure 32. BYTE5 Register

7	6	5	4	3	2	1	0
BYTE5[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 26. BYTE5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE5[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

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7.6.22 EEPROM User Register, Byte6 (BYTE6) (address = 0x26h) [reset = 0h]

Figure 33. BYTE6 Register

7	6	5	4	3	2	1	0
BYTE6[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 27. BYTE6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE6[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

7.6.23 EEPROM User Register, Byte7 (BYTE7) (address = 0x27h) [reset = 0h]

Figure 34. BYTE7 Register

7	6	5	4	3	2	1	0
BYTE7[7:0]							
R/W-0h							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 28. BYTE7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BYTE7[7:0]	R/W	0h	User programmable EEPROM. See Table 20 for detail on how to program EEPROM.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

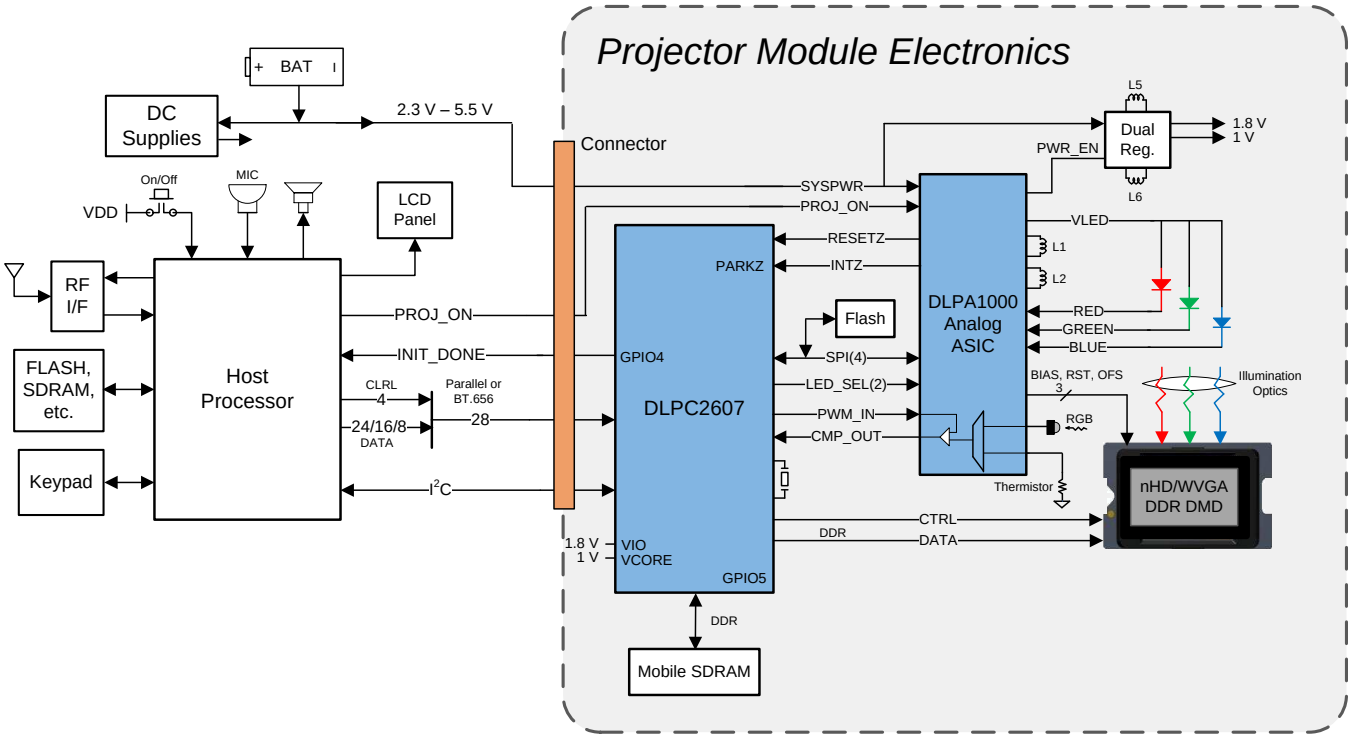
8.1 Application Information

A DLPC2607 controller can be used with a DLP2000 DMD to provide a compact, reliable, high-efficiency display solution for many different video display applications. DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions with the primary direction being into collection optics within a projection lens. The projection lens sends the light to the destination needed for the application. Each application is derived primarily from the optical architecture of the system and the format of the pixel data being input into the DLPC2607.

In display applications using the DLP2000 DMD, the DLPA1000 provides necessary analog functions including analog power supplies and an RGB LED driver to provide a robust and efficient display solution. Display applications of interest include pico-projectors embedded in display devices like smart phones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery-powered mobile accessory, interactive display, low latency gaming displays, and digital signage.

8.2 Typical Application

A common application when using DLPA1000 with DLP2000 DMD and DLPC2607 controller is creating a pico-projector embedded in a handheld product. For example, a pico-projector may be embedded in a smart phone, a tablet, a camera, or camcorder. The DLPC2607 in the pico-projector embedded module typically receives images from a host processor within the product as shown in Figure 35. DLPA1000 provides power supply sequencing and controls the LED currents as required by the application.



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Figure 35. Typical Standalone Projector System Block Diagram

Typical Application (continued)

8.2.1 Design Requirements

A pico-projector is created by using a DLP chipset comprised of a DMD such as the DLP2000, a controller such as the DLPC2607, and a PMIC/LED driver such as the DLPA1000. The DLPA1000 provides the needed analog functions for the projector, the DLPC2607 does the digital image processing, and the DMD is the display device for producing the projected image. In addition to the three critical DLP components, other chips may be needed for the full system design, such as the battery (SYSPWR), a regulated 1.8-V supply for the controller VIO, and a regulated 1-V supply for the controller VCORE.

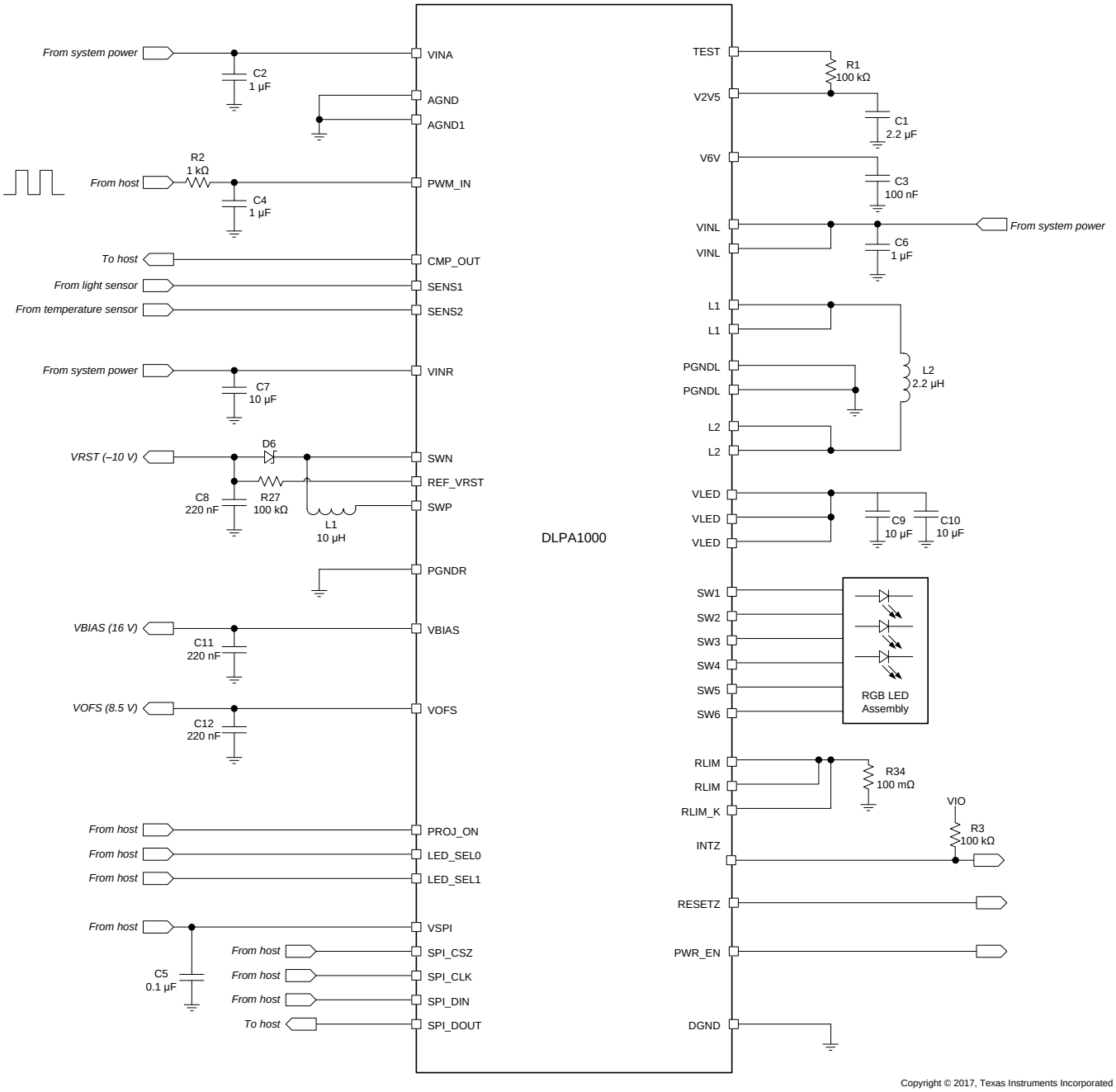
The DLPA1000 provides power to the illumination source for the DMD, typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector. The entire pico-projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V and 1-V supplies can remain active to be used by other non-projector sections of the product.

8.2.2 Detailed Design Procedure

The DLPA1000 contains a buck-boost regulator for the LEDs, boost regulators for the DMD rails, and internal LDOs for logic state control and operation. Each regulator requires a few external components to operate, referenced by their designators in Figure 36 and Figure 38, and all capacitors should maintain the recommended values at expected operating temperatures and bias voltages.

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Typical Application (continued)



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Figure 36. Schematic

8.2.2.1 VLED Buck-Boost

The VLED buck-boost provides the necessary voltages for the LED array capable of supporting both common anode and cathode-cathode-anode RGB LEDs. Configurations for both packages are detailed in the *RGB Strobe Decoder* section. Alternatively, a design could utilize an optical engine from an OEM that specializes in designing optics for DLP projectors, which typically integrate the LEDs and DMD into a single module. Current sensing through the LEDs is accomplished with a high-precision (0.1%) 100-mΩ sense resistor (R34) connecting RLIM to GND, with a separate trace providing a Kelvin connection to RLIM_K directly from the pad of the sense resistor.

Typical Application (continued)

The VLED buck-boost utilizes a single 2.2-µH inductor (L2) to generate the voltages for the LED array, bridging the pins labeled L1 to the pins labeled L2. The buck-boost also requires a 1-µF input bypass capacitor (C6) connecting VINL to GND, and two 10-µF output filter capacitors (C9 and C10) connecting VLED to GND. Ensure the inductor can handle the expected operating currents and refer to Calculating Inductor Peak Current to calculate the expected peak current for a design that can saturate the inductor's core.

8.2.2.1.1 Calculating Inductor Peak Current

To properly configure the DLPA1000 device, a 2.2-µH inductor (L2) must be connected between pins L1 and L2. The peak current for the inductor in steady state operation can be calculated.

Equation 1 shows how to calculate the peak current I_1 in step down mode operation and Equation 2 shows how to calculate the peak current I_2 in boost mode operation. VIN1 is the maximum input voltage VIN2 is the minimum input voltage, f is the switching frequency (2.25 MHz) and L the inductor value (2.2 µH).

$$I_1 = \frac{I_{OUT}}{0.8} + \frac{V_{OUT}\left(V_{IN1} - V_{OUT}\right)}{2 \times V_{IN1} \times f \times L} \quad (1)$$

$$I_2 = \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN2}} + \frac{V_{IN2}\left(V_{OUT} - V_{IN2}\right)}{2 \times V_{OUT} \times f \times L} \quad (2)$$

The critical current value for selecting the right inductor is the higher value of I_1 and I_2. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents. This also needs to be taken into account when selecting an appropriate inductor. Internally the switching current is limited to 2.2 A.

8.2.2.2 DMD Supplies

The PMIC also utilizes a single inductor (L1) to generate the low-current –10-V, 16-V, and 8.5-V supplies. Connect the inductor from SWP to SWN, and use a Schottky diode (D6) to generate the –10 V by connecting the cathode of the diode to the SWN side of the inductor and the anode of the diode to the load (VRST). Place a 220-nF filter cap (C8) from VRST to GND and bridge VRST to the feedback pin (REF_VRST) using a 100-kΩ resistor (R27). Bypass VINR to GND using a 10-µF capacitor (C7), and ensure VBIAS and VOFS each have dedicated 220-nF output filter capacitors (C11 and C12).

8.2.2.3 LDOs and Digital Logic

Ensure V2V5 has a 2.2-µF output capacitor (C1), and that V6V has a 100-nF output capacitor (C3). It is critical that V2V5 externally connects to the TEST pin (R1), otherwise the PMIC will be unable to operate. UVLO for this device is typically 2.3 V.

8.2.3 Application Curve

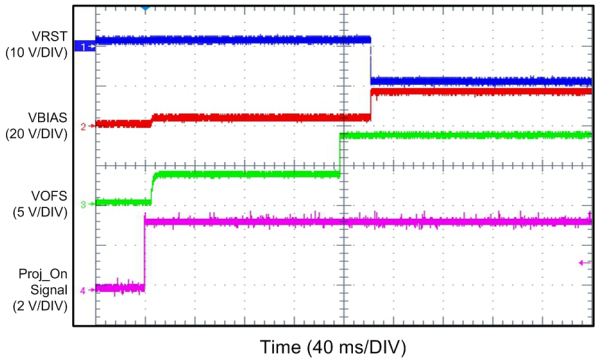


Figure 37. Power-Up Sequence: PROJ_ON Asserted

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9 Power Supply Recommendations

The DLPA1000 is designed to operate from a 2.3-V to 6-V input voltage supply or battery. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminal, or supply peak current limitations, additional bulk capacitance may be required. Electrolytic or tantalum type capacitors can dampen ringing often caused by ceramic input capacitors. The amount of bulk capacitance required should be evaluated such that the input voltage can remain in specification long enough for a proper fast shutdown to occur for the VOFS, VRST, and VBIAS supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply or battery supply is suddenly removed from the system.

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10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

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10.2 Layout Example

Place L2 (VLED) as close to the IC as possible. Route on top level and avoid vias. Max current is 2 A.

C6 and C7 should be placed close to the IC (supply caps). Keep traces separated and star-connect to system power.

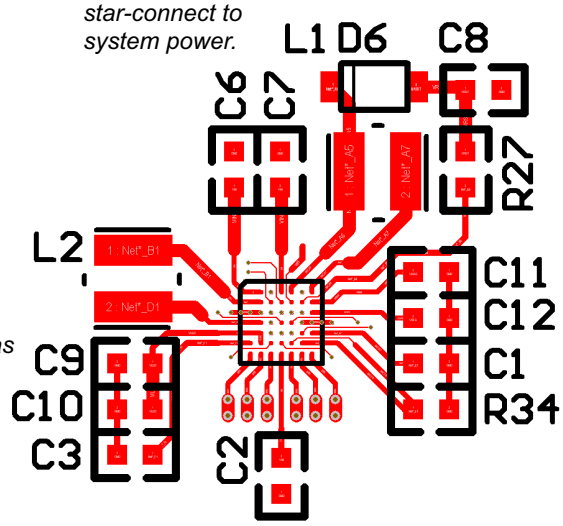
Place L1 as close to the IC as possible. Max trace current is 200 mA.

Place D6 close to L1 and C8 close to D6.

Keep trace from R27 to pin [B6] shielded from [A5]-L1 trace as much as possible to avoid noise coupling.

Place C11, and C12, (VBIAS, VOFS) close to the IC. Average current is <5 mA.

Place C9 and C10 (VLED) as close to the IC as possible. Use wide metal (1 A current) and avoid vias.



Place C1, as close to the IC as possible. This is an internal reference pin and needs to be shielded from noise.

Place C3 (V6V) close to IC and route on top metal. This is low-current trace.

Place C2 (supply cap) as close to the IC as possible. Star-connect to system power.

Keep trace [F5] R34 separated from trace [F6, F7] - R34 and connect them directly at R34. R34 is the LED sense resistor.

Figure 38. Layout

Table 29. Layout Components

LABEL	DESCRIPTION
C1	V2V5 output filter cap
C2	VINA input cap
C3	V6V output filter cap
C6	VINL input cap
C7	VINR input cap
C8	VRST output filter cap
C9	VLED output filter cap
C10	VLED output filter cap
C11	VBIAS output filter cap
C12	VOFS output filter cap
D6	VRST rectifying diode
L1	DMD supply inductor
L2	VLED buck-boost inductor
R27	100k VRST feedback resistor
R34	100m RLIM sense resistor

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『*DLPC2607 DLP PICOプロセッサ2607 ASIC*』

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPA1000YFFR	Active	Production	DSBGA (YFF) | 49	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	100
DLPA1000YFFR.B	Active	Production	DSBGA (YFF) | 49	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	100
DLPA1000YFFT	Active	Production	DSBGA (YFF) | 49	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	100
DLPA1000YFFT.B	Active	Production	DSBGA (YFF) | 49	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-10 to 85	100

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

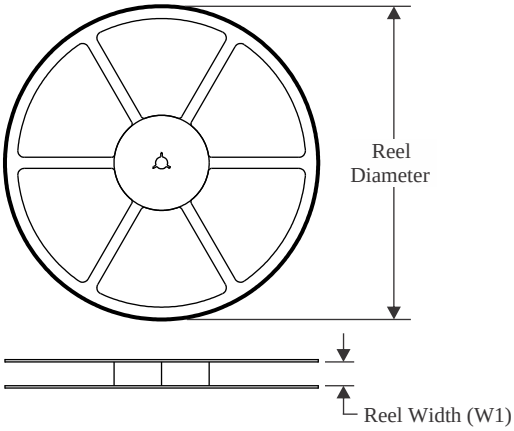
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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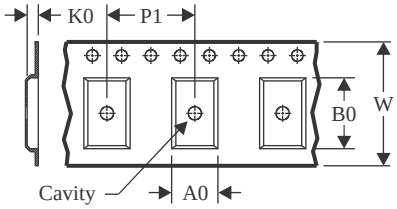
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

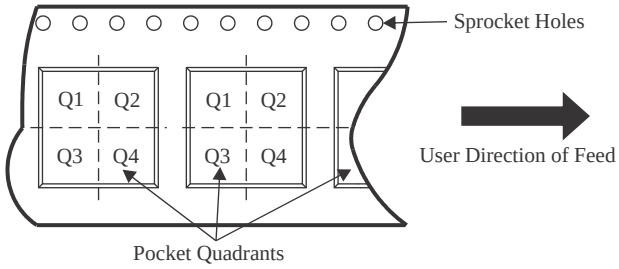


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

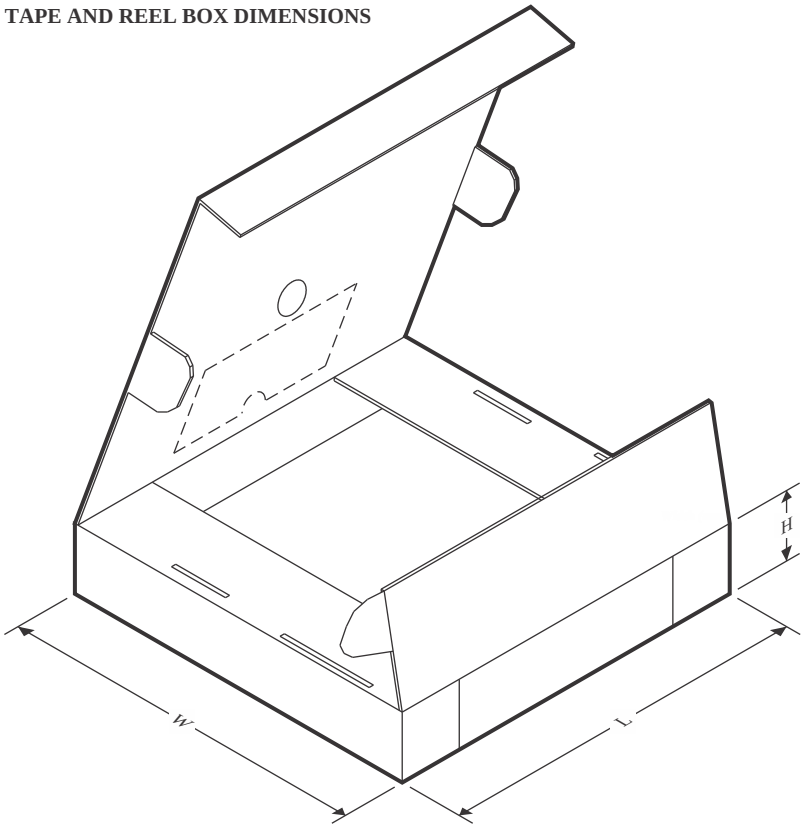
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DLPA1000YFFR	DSBGA	YFF	49	3000	180.0	8.4	3.16	3.16	0.71	4.0	8.0	Q1
DLPA1000YFFT	DSBGA	YFF	49	250	180.0	8.4	3.16	3.16	0.71	4.0	8.0	Q1

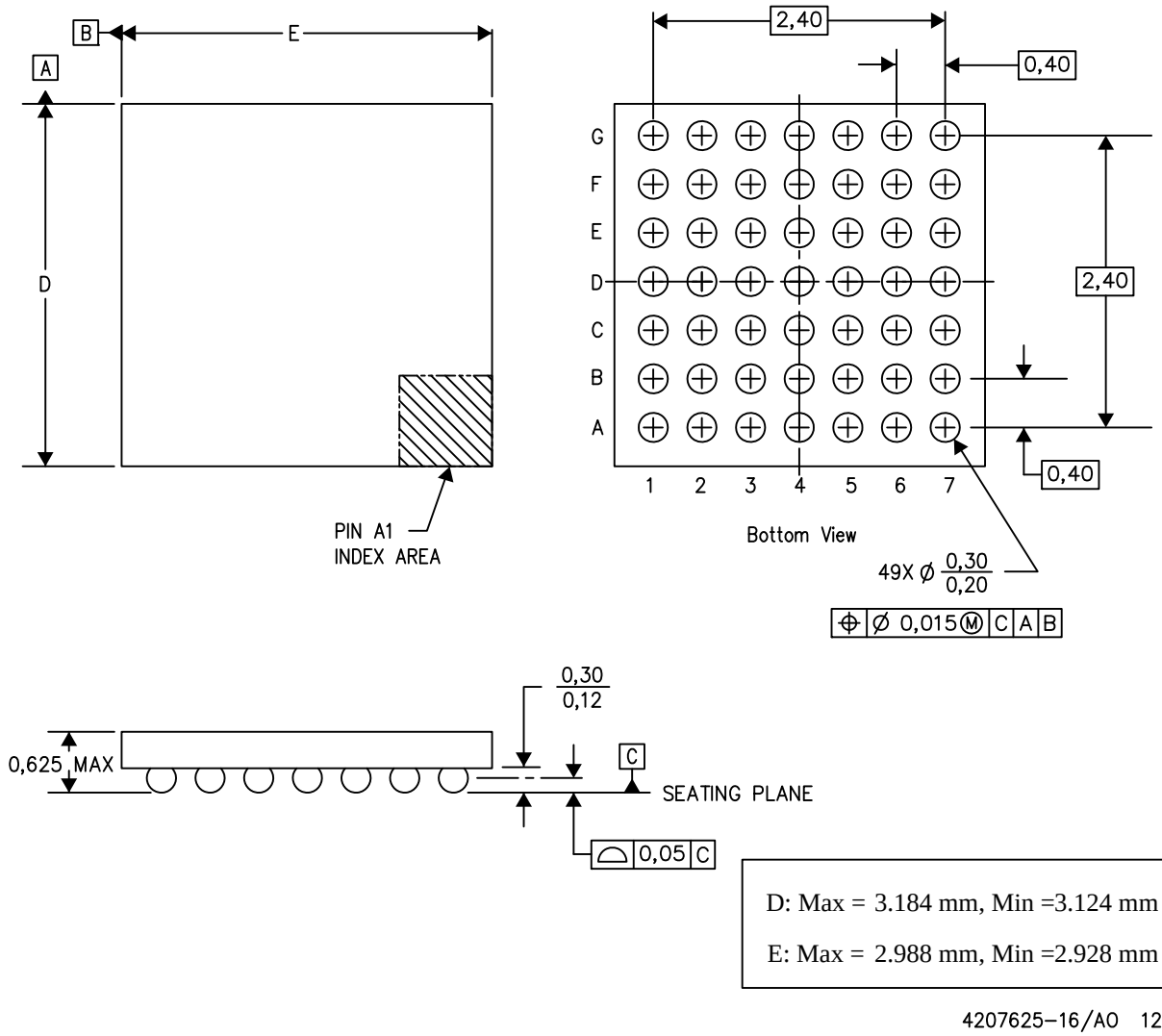
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DLPA1000YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
DLPA1000YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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