DLPC120-Q1 車載用 DMD コントローラ

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 2:周囲温度:-40℃～105℃
- 3 つの DMD デバイスとの互換性:
  - DLP3030-Q1: 0.3 WVGA S450
  - DLP3020-Q1:0.3 WVGA S247
  - DLP3021-Q1:0.3 WVGA S247
- ビデオ入力インターフェイス:
  - 24 ビット・パラレル (RGB888、RGB666、または RGB565)
  - 60Hz のフレーム・レート
  - QVGA から WVGA までの入力解像度
  - 最高 40 MHz のピクセル・クロック
- ビデオ処理:
  - 画像スケーリング
  - プログラム可能なデガンマ曲線
  - ベゼル調整
  - 水平および垂直の画像反転
- DMD インターフェイス:
  - 78-MHz DDR DMD インターフェイス
  - 一貫性のある DMD データ・ロードとリセットにより、過熱動作範囲を制御
  - パワー・ダウン時の 自動 DMD パーキング
  - DMD 温度 管理
- 外部メモリのサポート
  - DDR2:312MHz クロック (624MHz のデータ ・レート)
  - シリアル ・フラッシュ 39MHz クロック
- システム制御
  - I^2C 通信インターフェイス
  - スプラッシュ・スクリーンをプログラム可能
  - DMD 電源およびリセット・ドライバ制御
  - プログラマブルなフラッシュ・ベースの構成
- テストのサポート
  - テスト・パターン・ジェネレータを内蔵
  - JTAG バウンダリ・スキャン・テストに対応
- 216 ピン、1.0mm ピッチの BGA パッケージ

2 アプリケーション

- 広視野の拡張現実ヘッドアップ・ディスプレイ (HUD)
- 車内投影ディスプレイおよび照明
- デジタル・クラスタ、ナビゲーション、インフォテインメント用のフロントガラス・ディスプレイ
- 車載用スモールランプ
- ダイナミック地表投影

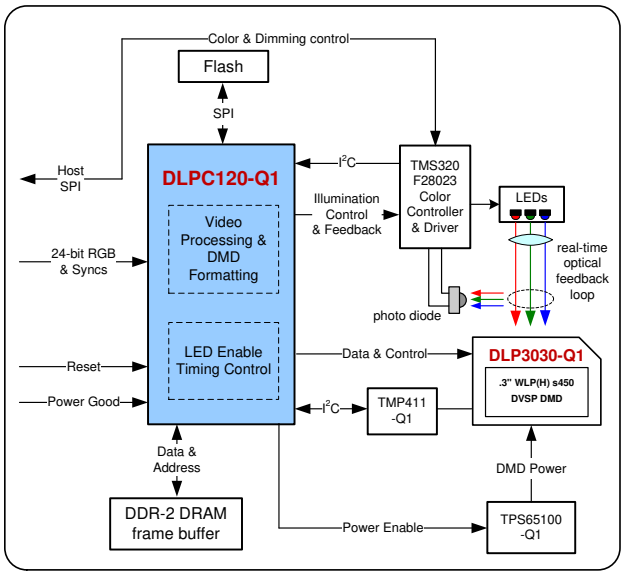
3 概要

DLPC120-Q1 車載アプリケーション用 DMD ディスプレイ・コントローラは、3 つのデジタル・マイクロミラー・デバイス (DMD) (DLP3030-Q1 、DLP3020-Q1 、または DLP3021-Q1) のいずれかと互換性を持つチップセットの一部です。コア DLPC120-Q1 ロジックはビデオ入力を受け付け、データをフォーマットして DMD に表示するとともに、RGB LED を制御してリアルタイムの画像を作成します。また、DLPC120-Q1 は外部のシステム制御または DMD からの温度入力に基づいて、DMD の電源オンおよび電源オフ・イベントの制御も行います。外部の調光回路およびマイクロコントローラと組み合わせることで、DLPC120-Q1 は HUD アプリケーションで 5000:1 を超える広い調光範囲をサポートします。一般に、DLPC120-Q1 はホスト・プロセッサとの I^2C インターフェイスでスレーブ・デバイスとなります。

デバイス情報

部品番号(1)	パッケージ	本体サイズ (公称)
DLPC120-Q1	NFBGA (216)	17.00mm × 17.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なシステム図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (March 2018) to Revision B (April 2022) — **Page**

- サポート対象デバイスとして DLP3020-Q1 および DLP3021-Q1 を追加。DLP3000-Q1 を削除 ... 1
- デジタル・クラスタ、ナビゲーション、インフォテインメント用のフロントガラス・ディスプレイ、車載用スモールランプ、ダイナミック地表投影 アプリケーションを追加。 ... 1
- このドキュメントは、最新のテキサス・インスツルメンツおよび業界データシート標準に準拠して更新されています。 ... 1
- 本体サイズを 16mm × 16mm から 17mm × 17mm に更新し、サポート対象デバイスとして DLP3020-Q1 および DLP3021-Q1 デバイスを追加。DLP3000 を削除 ... 1
- This document is updated per the latest Texas Instruments and industry inclusive terminologies. All occurrences of MISO are now POCI; all occurrences of MOSI are now PICO ... 3
- Updated LED Driver Interface ... 5
- Updated Design Requirements ... 27
- Updated General PCB Recommendations ... 31

Changes from Revision * (November 2017) to Revision A (March 2018) — **Page**

- デバイス・ステータスを「事前情報」から「量産データ」に変更 ... 1
- Changed case-to-junction thermal coefficient from 0.77°C/W : to 0.28°C/W in *Thermal Information* table ... 12
- Updated Temperature Monitor Function ... 25
- Updated Application Information ... 26

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5 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	VCCIO_2	DMD_SAC_CLK	DMD_SAC_BUS	DMD_DAD_OEZ	DMD_DCLK	DMD_D14	DMD_D11	DMD_D10	DMD_D8	DMD_D5	DMD_D2	DMD_D1	HUD_INTR	AUX BIT_2	VSS	A
B	MEM_A10	VCCIO_1	VSS	DMD_JTCK	DMD_DAD_BUS	DMD_SCTRL	DMD_TRC	DMD_D12	DMD_D9	DMD_D7	DMD_D3	DMD_D0	AUX BIT_7	AUX BIT_1	VCCIO_3	LED_S_EN	B
C	MEM_A1	MEM_WEZ	MEM_RST	DMD_JTDO	DMD_JTMS	VSS	DMD_LOADB	DMD_D13	VSS	DMD_D4	DMD_PWR_EN	VSS	AUX BIT_0	HTR_ENABLE	LED_B_EN	LED_R_EN	C
D	MEM_A11	MEM_A3	MEM_RASZ	VCCIO_1	DMD_JTDI	VCCIO_2	DMD_DAD_STRB	VCCIO_2	DMD_D6	VCCIO_2	AUX BIT_6	VCCIO_2	LED_COMPZ	LED_G_EN	LEDDRV_ON	LED_B_PWM	D
E	MEM_A9	MEM_A12	VSS	MEM_ODT								VCCIO_3	LED_D_EN	LED_R_PWM	FLASH_PICO	FLASH_SCLK	E
F	MEM_CLKZ	MEM_CLK	MEM_A8	MEM_A2								VSSA (PLL)	LED_G_PWM	FLASH_POCI	FLASH_CSZ	LED_EN	F
G	MEM_A5	MEM_A6	MEM_A7	VCCIO_1			VSS	VDD	VDD	VSS		VCCA (PLL)	PWR GOOD	PLL_REFCLK_O	PLL_REFCLK_I	HW TEST_EN	G
H	MEM_A0	MEM_A4	VSS	MEM_VREF0			VDD	VSS	VSS	VDD		TSTPT_6	RESETZ	TSTPT_7	TSTPT_5	TSTPT_4	H
J	MEM_BA0	MEM_BA1	MEM_CASZ	MEM_ZQ			VDD	VSS	VSS	VDD		VDDQ	JTAG RSTZ	TSTPT_1	TSTPT_2	TSTPT_3	J
K	MEM_CKE	MEM_CSZ	MEM_ATO	VCCIO_1			VSS	VDD	VDD	VSS		VSS	TMP_SDA	JTAG TDO	JTAG TDI	TSTPT_0	K
L	MEM_DQ7	MEM_DQ6	MEM_DQ4	VSS								AST_CLR0	AST_INTR0	VCCIO_3	JTAG TCK	JTAG TMS	L
M	MEM_DQ5	MEM_DQ3	VCCIO_1	MEM_DTO0								AST_CLR1	AST_HLD0	AST_INTR1	I2C_SCL_2	TMP_SCL	M
N	MEM_DQS0	MEM_DQSZ0	VSS	MEM_DTO1	VCCIO_1	MEM_VREF1	VSS	P_DATAEN	PDATA [4]	VCCIO_3	PDATA [14]	PDATA [19]	PDATA [21]	VSS	I2C_SDA_1	I2C_SDA_2	N
P	MEM_DQ2	MEM_DQ0	VCCIO_1	VSS	MEM_DQ12	VSS	P_VSYNC	P_HSYNC	VSS	PDATA [7]	PDATA [10]	PDATA [13]	VCCIO_3	PDATA [22]	PDATA [23]	I2C_SCL_1	P
R	MEM_DQ1	VSS	MEM_DQ15	MEM_DQS1	MEM_DQ11	MEM_DQ9	VCCIO_1	PDATA [0]	PDATA [2]	PDATA [5]	PDATA [8]	PDATA [11]	PDATA [15]	PDATA [18]	PDATA [20]	AST_HLD1	R
T	VSS	MEM_DQ14	MEM_DQ13	MEM_DQSZ1	MEM_DQ10	MEM_DQ8	VSS	PCLK	PDATA [1]	PDATA [3]	PDATA [6]	PDATA [9]	PDATA [12]	PDATA [16]	PDATA [17]	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

図 5-1. ZXS Package 216-Pin BGA Top View

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表 5-1. DLPC120-Q1 Device Initialization and Programming Pin Descriptions

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
RESETZ	H13	3.30 V	I_2	Async	Functional Reset (Active Low). Resets internal logic and causes PLL startup and PLL locking. Assertion is required after power supplies are within limits. See セクション 6.7 for timing requirements.
PWRGOOD	G13		I_2	Async	System Power Good indicator. Should be held low until all DLPC120-Q1 power has been within operating limits. See セクション 6.7 for timing requirements. Must be set high to enable normal operation. When set low, the DLPC120-Q1 begins the parking routine for the DMD. Together with pin E14 (LED_R_PWM / PWRGOOD_CNTRL), this signal is critical for DLP30xx-Q1 parking as part of the Pre-Conditioning Sequence and subsequent un-parking. See *DLPC120-Q1 Programmer's Guide* for implementation details.
PLL_REFCLK_I	G15		I_2	N/A	Reference Clock Input (16 MHz). Can be driven by crystal across this pin and PLL_REFCLK_O or by external oscillator. See セクション 6.7 for timing requirements.
PLL_REFCLK_O	G14		O_6	N/A	Crystal output. Used with PLL_REFCLK_I.
HUD_INTR	A14		O_6	N/A	Interrupt signal. This active high signal indicates one of the interrupt sources in the controller has been triggered.
IIC_SCL_1	P16		B_8	N/A	I^2C Clock for Device configuration and control. Requires external pull-up. Port 1 peripheral command/control interface.
IIC_SDA_1	N15		B_8	N/A	I^2C Data for Device configuration and control. Requires external pull-up. Port 1 peripheral command/control interface.
IIC_SCL_2	M15		B_8	N/A	I^2C Clock Debug Port. Requires external pull-up. Port 2 peripheral command/control interface.
IIC_SDA_2	N16		B_8	N/A	I^2C Data Debug Port. Requires external pull-up. Port 2 peripheral command/control interface.
FLASH_POCI	F14		I_2	FLASH_SCLK	Serial Data input from the external SPI Flash device. This provides device logical programming data as well as functional configuration parameter data.
FLASH_CSZ	F15		O_6	FLASH_SCLK	Chip Select output for the external SPI Flash device. Active low.
FLASH_SCLK	E16		O_6	N/A	Clock for the external SPI Flash device.
FLASH_PICO	E15		O_6	FLASH_SCLK	Serial Data output to the external SPI Flash device. This pin sends address and control information as well as data when programming.

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5.1 LED Driver Interface

PIN		I/O	I/O	CLOCK	DESCRIPTION
NAME	NO.	POWER	TYPE	SYSTEM	
LED_B_PWM	D16	3.30 V	O_6	N/A	Function reserved for future use.
LED_R_PWM (PWRGOOD_CNTRL)	E14		O_6	N/A	Repurposed for power good control. Together with pin G13 (PWRGOOD), this signal is used for DLP30xx-Q1 parking as part of the preconditioning sequence and subsequent unparking. See the *DLPC120-Q1 Programmer's Guide* for implementation details.
LED_G_PWM	F13		O_6	N/A	Function reserved for future use.
LED_B_EN	C15		O_6	N/A	Blue LED enable strobe. Controlled by programmable DMD sequence timing (active high)
LED_R_EN	C16		O_6	N/A	Red LED enable strobe. Controlled by programmable DMD sequence timing (active high)
LED_G_EN	D14		O_6	N/A	Green LED enable strobe. Controlled by programmable DMD sequence timing (active high)
LED_S_EN	B16		O_6	N/A	LED shunt enable. Controlled by programmable DMD sequence timing (active high)
LED_D_EN	E13		O_6	N/A	LED drive enable. Controlled by programmable DMD sequence timing (active high)
LEDDRV_ON	D15		O_6	Async	LED driver enable. Active high output control to external LED drive logic
LED_EN	F16		I_2	Async	LED enable (active high input). A logic low on this signal forces LEDDRV_ON low and RGB strobes low. These signals are enabled 100 ms after LED_EN transitions to a high (assuming corresponding SW parameters are also set to enable LED operation).
LED_COMPZ	D13		I_2	Async	LED threshold compare (active low input). A logic low on this signal indicates a threshold is reached, and in discontinuous mode controls shunt enable (LED_S_EN).
AST_CLR0	L12		O_6	N/A	Function reserved for future use
AST_HLD0	M13		O_6	N/A	Function reserved for future use
AST_INTR0	L13		O_6	N/A	Sequence timer interrupt port
AST_CLR1	M12		O_6	N/A	Function reserved for future use
AST_HLD1	R16		O_6	N/A	Function reserved for future use
AST_INTR1	M14		O_6	N/A	Function reserved for future use

5.2 DMD Temperature Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
TMP_SDA	K13	3.30 V	B_8	Async	Temperature control serial data. This signal is used to communicate with the TMP411 to read the temperature values. Follows I^2C protocol as required by TMP411.
TMP_SCL	M16		B_8	Async	Temperature control serial clock. This signal is used to communicate with the TMP411 to read the temperature values. Follows I^2C protocol as required by TMP411.
HTR_ENABLE	C14		O_6	Async	Reserved pin

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General Purpose I/O

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
AUXBIT_0 (FLICKER_SELECT)	C13	3.30 V	O_6	Async	This pin is configured by default to be asserted at the lowest brightness mode to activate flicker reduction logic in the LED driver circuit. It is deasserted, otherwise, to deactivate the flicker reduction logic for normal operation. Contact a TI Applications Engineer for implementation details.
AUXBIT_1	B14		O_6	Async	DMD sequencer reset AUX Bit 1. Intended for system debug. Can be routed to a testpoint or left unconnected
AUXBIT_2	A15		O_6	Async	DMD sequencer reset AUX Bit 2. Intended for system debug. Can be routed to a testpoint or left unconnected
AUXBIT_6	D11		O_6	Async	DMD sequencer reset AUX Bit 6. Intended for system debug. Can be routed to a testpoint or left unconnected
AUXBIT_7	B13		O_6	Async	DMD sequencer reset AUX Bit 7. Intended for system debug. Can be routed to a testpoint or left unconnected

5.3 Main Video and Data Control Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
PCLK	T8	3.30 V	I_2	N/A	Pixel clock(1)
P_VSYNC	P7		I_2	PCLK	Vertical sync(2)
P_HSYNC	P8		I_2		Horizontal sync(2)
P_DATAEN	N8		I_2		Data valid(2)
PDATA[0]	R8		I_2		Data(3)
PDATA[1]	T9		I_2		
PDATA[2]	R9		I_2		
PDATA[3]	T10		I_2		
PDATA[4]	N9		I_2		
PDATA[5]	R10		I_2		
PDATA[6]	T11		I_2		
PDATA[7]	P10		I_2		
PDATA[8]	R11		I_2		
PDATA[9]	T12		I_2		
PDATA[10]	P11		I_2		
PDATA[11]	R12		I_2		
PDATA[12]	T13		I_2		
PDATA[13]	P12		I_2		
PDATA[14]	N11		I_2		
PDATA[15]	R13		I_2		
PDATA[16]	T14		I_2		
PDATA[17]	T15		I_2		
PDATA[18]	R14		I_2		
PDATA[19]	N12		I_2		
PDATA[20]	R15		I_2		
PDATA[21]	N13		I_2		
PDATA[22]	P14		I_2		
PDATA[23]	P15		I_2		

(1) Pixel clock capture edge is software programmable.

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(2) VSYNC, HSYNC, and data valid polarity are software programmable.
(3) The 24-bit PDATA bus can be mapped based on pixel format. By default PDATA[23-16]=Red[7-0], PDATA[15-8]=Green[7-0], and PDATA[7-0]=Blue[7-0]. See the *DLPC120-Q1 Programmer's Guide* for more information.

5.4 DMD Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
DMD_D0	B12	1.80 V	O_5	DMD_DCLK	DMD data pins. DMD data pins are DDR (Double Data Rate) signals that are clocked on both edges of DMD_DCLK.
DMD_D1	A13				
DMD_D2	A12				
DMD_D3	B11				
DMD_D4	C10				
DMD_D5	A11				
DMD_D6	D9				
DMD_D7	B10				
DMD_D8	A10				
DMD_D9	B9				
DMD_D10	A9				
DMD_D11	A8				
DMD_D12	B8				
DMD_D13	C8				
DMD_D14	A7				
DMD_DCLK	A6		O_5	N/A	DMD data clock (DDR)
DMD_LOADB	C7		O_5	DMD_DCLK	DMD data load signal (active low)
DMD_SCTRL	B6		O_5	DMD_DCLK	DMD data serial control signal
DMD_TRC	B7		O_5	DMD_DCLK	DMD data toggle rate control
DMD_DAD_OEZ	A5		O_5	Async	DMD DAD output enable (active low). A pullup (10 kΩ to 100 kΩ) to the 1.8-V rail for the DMD interface is needed to keep this signal inactive when tristated.
DMD_DAD_BUS	B5		O_5	DMD_SAC_CLK	DMD DAD bus data
DMD_DAD_STRB	D7		O_5	DMD_DCLK	DMD DAD bus strobe.
DMD_SAC_BUS	A4		O_5	DMD_SAC_CLK	DMD SAC bus data
DMD_SAC_CLK	A3		O_5	N/A	DMD SAC bus clock
DMD_JTCK	B4		O_4	N/A	DMD interface test clock. Signal connected to DMD JTAG interface to allow the verification of the interface. The interface is tristated when not active.
DMD_JTMS	C5		O_4	N/A	DMD interface test mode. Signal connected to DMD JTAG interface to allow the verification of the interface. The interface is tristated when not active.
DMD_JTDI	D5		O_4	N/A	DMD interface test data output. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDI. The interface is tristated when not active.
DMD_JTDO	C4		I_1	N/A	DMD interface test data input. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDO. Internal pulldown.
DMD_PWR_EN	C11	3.30 V	O_6	Async	DMD power regulator enable (active high)

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5.5 Memory Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
MEM_CLK	F2	1.80 V	O_s	N/A	DDR memory, Differential Memory Clock.
MEM_CLKZ	F1				
MEM_A0	H1		O_s	MEM_CLK	DDR memory, Multiplexed Row and Column Address.
MEM_A1	C1				
MEM_A2	F4				
MEM_A3	D2				
MEM_A4	H2				
MEM_A5	G1				
MEM_A6	G2				
MEM_A7	G3				
MEM_A8	F3				
MEM_A9	E1				
MEM_A10	B1				
MEM_A11	D1				
MEM_A12	E2				
MEM_BA0	J1		O_s	MEM_CLK	DDR memory, Bank Select.
MEM_BA1	J2				
MEM_RASZ	D3		O_s	MEM_CLK	DDR memory, Row Address Strobe (Active low).
MEM_CASZ	J3		O_s	MEM_CLK	DDR memory, Column Address Strobe (Active low).
MEM_WEZ	C2		O_s	MEM_CLK	DDR memory, Write Enable (Active low).
MEM_CSZ	K2		O_s	MEM_CLK	DDR memory, Chip Select (Active low).
MEM_CKE	K1		O_s	MEM_CLK	DDR memory, Clock Enable (Active high).
MEM_ODT	E4		O_s	MEM_CLK	DDR memory, On die termination (ODT). ODT is not verified and supported operational mode. This pin should be left open or connected to corresponding DDR2 pin.
MEM_RST	C3		O_s	MEM_CLK	DDR memory, Reset. Do Not connect.
MEM_ZQ	J4		O_s	MEM_CLK	DDR memory, External pad where to connect the external impedance calibration resistor. The user connects the PAD pin through an external 240 Ω ± 1% resistor to ground.
MEM_DQS0	N1		B_{SD}	N/A	DDR memory, Lower Byte, R/W Data Strobe.
MEM_DQSZ0	N2		B_{SD}	N/A	DDR memory, Lower Byte, R/W Data Strobe, inverted.
MEM_DQ0	P2		B_s	MEM_DQS0	DDR memory, Lower Byte, Bidirectional R/W Data.
MEM_DQ1	R1				
MEM_DQ2	P1				
MEM_DQ3	M2				
MEM_DQ4	L3				
MEM_DQ5	M1				
MEM_DQ6	L2				
MEM_DQ7	L1				

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PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
MEM_DQS1	R4	1.80 V	B_s	N/A	DDR memory, Upper Byte, R/W Data Strobe.
MEM_DQSZ1	T4		B_{SD}	N/A	DDR memory, Upper Byte, R/W Data Strobe, inverted.
MEM_DQ8	T6		B_s	MEM_DQS1	DDR memory, Upper Byte, Bidirectional R/W Data.
MEM_DQ9	R6				
MEM_DQ10	T5				
MEM_DQ11	R5				
MEM_DQ12	P5				
MEM_DQ13	T3				
MEM_DQ14	T2				
MEM_DQ15	R3				

Board Level Test and Debug

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
JTAGRSTZ	J13	3.30 V	I_2	Async	JTAG, Reset. Includes weak internal pull-up. Holds TAP controller and associated JTAG logic in idle state under normal operation. **This pin should be pulled down with a 5 kΩ or smaller resistor for normal operation.**
JTAGTDI	K15		I_2	JTAGTCK	JTAG, Serial Data In. Includes weak internal pull-up.
JTAGTCK	L15		I_2	N/A	JTAG, Serial Data Clock. Includes weak internal pull-up.
JTAGTMS	L16		I_2	JTAGTCK	JTAG, Test Mode Select. Includes weak internal pull-up.
JTAGTDO	K14		O_6	JTAGTCK	JTAG, Serial Data Out.

Manufacturing Test Support

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
HWTEST_EN	G16	3.30 V	I_2	N/A	Manufacturing Test Enable signal. Should be connected directly to ground on the PCB for normal operation. Weak Internal Pulldown.
MEM_ATO	K3	N/A	O	N/A	Memory Controller Analog Test Output. Factory Test purposes only, should be left unconnected in system.
MEM_DTO0	M4	3.30 V	O_s	N/A	Memory Controller Digital Test Output #1. Factory Test purposes only, should be left unconnected in system.
MEM_DTO1	N4	3.30 V	O_s	N/A	Memory Controller Digital Test Output #2. Factory Test purposes only, should be left unconnected in system.

Test Point Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
TSTPT_0	K16	3.30 V	B_8	Async	Reserved for Test Outputs. These test I/O should be left open or unconnected for normal operation in final product design. (DO NOT tie to GND), Internal Pullup on all signals. **TSTPT_4 should be pulled up using external 10 kΩ resistor to ensure proper initialization**.
TSTPT_1	J14				
TSTPT_2	J15				
TSTPT_3	J16				
TSTPT_4	H16				
TSTPT_5	H15				
TSTPT_6	H12				

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PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
TSTPT_7 (CM_DM)	H14	3.30 V	B_8	Async	This pin is configured by default to indicate whether the system is in Continuous Mode (High) or Discontinuous Mode (Low). Contact a TI Applications Engineer for implementation details. It can also be reserved as a Test Output.

Power and Ground

PIN		I/O	
NAME	NO.		DESCRIPTION
VCCIO_1	B2, D4, G4, K4, M3, N5, P3, R7	PWR	1.8 V (DDR2 MEM).
VCCIO_2	BA2, D10, D12, D6, D8	PWR	1.8 V (DMD I/F).
VCCIO_3	B15, E12, L14, N10, P13	PWR	3.3 V (MISC IO).
MEM_VREF0	H4		Voltage Referenced Input (50% of DDR Memory Voltage).
MEM_VREF1	N6		Voltage Referenced Input (50% of DDR Memory Voltage).
VCCA	G12	PWR	PLL Power Input.
VSSA	F12		PLL R-C Return Path (NOT a GND).
VDD	G8, G9, H7, H10, J7, J10, K8, K9	PWR	1.2-V core logic power supply.
VDDQ	J12	GND	EFUSE Programming voltage (Used in Manufacturing Test only.) Should be tied to GND.
GND	A1, A16, B3, C6, C9, C12, E3, G7, G10, H3, H8, H9, J8, J9, K7, K10, K12, L4, N3, N7, N14, P4, P6, P9, R2, T1, T7, T16	GND	Common Ground (I/O Ground).

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表 5-2. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE
SUBSCRIPT	**DESCRIPTION**	
1	1.8 V	VDD
2	3.3 V	VCCIO_3
4	8 mA	VDD
5	6, 10, or 12 mA	VCCIO_2
6	8 mA	VCCA
S	SSTL_18	VCCIO_1
8	8 mA	VCCIO_3
SD	SSTL_18 Differential	VCCIO_1
TYPE		
I	Input	N/A
O	Output	
B	Bidirectional	
PWR	Power	
GND	Ground return	

表 5-3. Internal Pullup and Pulldown Characteristics

INTERNAL PULL-UP AND PULL-DOWN RESISTOR CHARACTERISTICS	VCCIO	MIN	TYP	MAX	UNIT
Weak pull-up resistance	3.3 V	27	39	61	kΩ
Weak pull-down resistance	3.3 V	32	46	79	kΩ
	1.8 V	52	91	180	kΩ

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)				
VCCIO_1		0	1.98	V
VCCIO_2		0	3.6	V
VCCIO_3		0	3.6	V
VCCA (PLL)		0	1.32	V
VDD		0	1.32	V
GENERAL				
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to GND.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 — All pins	±500	
		Charged-device model (CDM), per AEC Q100-011 — Corner pins (A1, A16, T1, and T16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	1.2-V supply voltage, core logic	1.14	1.2	1.26	V
VCCA	Analog voltage for PLL	1.14	1.2	1.26	V
VCCIO_0	DDR2 memory interface	1.71	1.8	1.89	V
VCCIO_1	1.8-V supply voltage for DMD	1.71	1.8	1.89	V
VCCIO_2	Pixel interface supply voltage	3.135	3.3	3.465	V
VDDQ	EFuse programming voltage	0.0	0.0	0.0	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature(1)	–40		105	°C

(1) Operating ambient temperature is dependent on system thermal design. Operating junction temperature may not exceed its specified range across ambient temperature conditions.

6.4 Thermal Information

THERMAL METRIC(1)		DLPC120-Q1 ZXS (BGA) 216 PINS	UNIT
ψ_{JT}	Case-to-junction thermal coefficient	0.28	°C/W

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6.4 Thermal Information (continued)

THERMAL METRIC[1]		DLPC120-Q1 ZXS (BGA) 216 PINS	UNIT
T_{JA}	Junction-to-ambient thermal coefficient	26.32	°C/W

(1) For more information about traditional and new thermal metrics, see the , *Semiconductor and IC Package Thermal Metrics Application Report* (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Logic core power (1.2 V)			140	186	mA
I_{VCCA}	PLL power (1.2 V)			3	10	mA
$I_{VCCIO_0/1}$	DDR2 memory and DMD interface I/O power (1.8 V)			180	245	mA
I_{VCCIO_2}	Pixel data input power (3.3 V)			4	10	mA
	Total power			469	724	mW

6.6 Electrical Characteristics for I/O

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	1.8-V LVCMOS (I/O Type 1)		1.17		VCCIO + 0.3	V
		3.3-V LVCMOS (I/O Type 2, 8)		2.0		VCCIO + 0.3	
		SSTL_18 (I/O Type S, SD)		1.08		VCCIO + 0.3	
V_{IL}	Low-level input threshold voltage	1.8-V LVCMOS (I/O Type 1)		–0.3		0.63	V
		3.3-V LVCMOS (I/O Type 2, 8)		–0.3		0.8	
		SSTL_18 (I/O Type S, SD)		–0.3		0.73	
V_{OH}	High-level output voltage	1.8-V LVCMOS fixed current (I/O Type 4)		1.35			V
		1.8-V LVCMOS variable current (I/O Type 5)		1.35			
		3.3-V LVCMOS fixed current (I/O Type 6, 8)		2.4			
		SSTL_18 (I/O Type S, SD)		VCCIO – 0.28			
V_{OL}	Low-level output voltage	1.8-V LVCMOS fixed current (I/O Type 4)				0.45	V
		1.8-V LVCMOS variable current (I/O Type 5)				0.45	
		3.3-V LVCMOS fixed current (I/O Type 6, 8)				0.4	
		SSTL_18 (I/O Type S, SD)				0.28	

6.7 Power Supply and Reset Timing Requirements

			MIN	MAX	UNIT
t_{ramp}	Time for all DLPC120-Q1 power rails to be applied	Power supplies can be applied in any order if they occur within this maximum timing. Otherwise, refer to Note (1).		10	ms
t_{pwr_en}	RESETZ rising edge (or PWRGOOD rising edge—whichever comes second) to DMD_PWR_EN rising edge	PWRGOOD shall be controlled by LED_R_PWM / PWRGOOD_CNTRL signal, which is an output of the DLPC120-Q1 and will automatically be asserted after the device releases from reset.		150	µs

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6.7 Power Supply and Reset Timing Requirements (continued)

			MIN	MAX	UNIT
t_{dly}	External delay between DMD_PWR_EN and DMD mirror supply voltages	This delay is not required for supported devices.			ms
t_{oez}	DMD_PWR_EN rising edge to falling edge of DMD_OEZ			5	ms
$t_{precondition}$	DMD preconditioning timeI	It is required that the DMD executes a Pre-Conditioning Sequence prior to parking. The final action of this sequence is the de-assertion of the LED_R_PWM / PWRGOOD_CNTRL signal, which shall drive the PWRGOOD signal low. See the *DLPC120-Q1 Programmer's Guide* for instructions on how to execute the Pre-Conditioning Sequence.	800		µs
t_{park}	DMD park time (approximate)		200	200	µs
t_{pd_dmd}	PWRGOOD low to falling edge of DMD_PWR_EN			500	µs
t_{fall}	Time for DLPC120-Q1 power supplies to be removed	Power supplies can be removed in any order if they occur within this maximum timing. Otherwise, they shall be removed in the reverse order they were applied, per the t_{ramp} specification and Note (1).		10	ms

(1) If the DLPC120-Q1 supplies cannot be applied according to this timing specification, then they must be applied in the following order, spanning no longer than 100 ms (shall be removed in the reverse order for power down):

a. Apply VCCIO_2 (3.3 V)
b. Apply VCCIO_0, VCCIO_1 (1.8 V) DDR Memory and DMD, in any order
c. Apply VDD (1.2 V) DLPC120-Q1 core supply voltage

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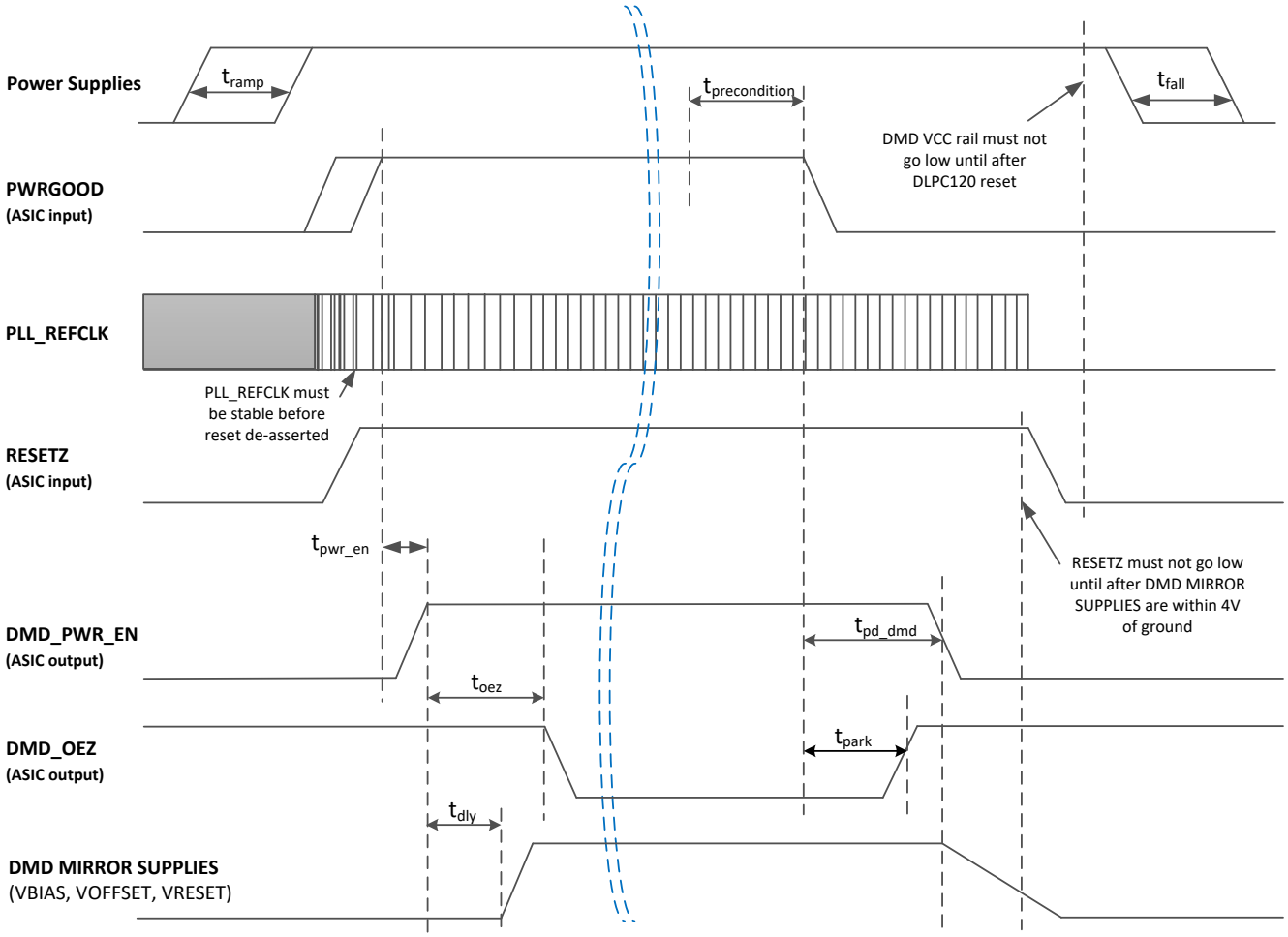


図 6-1. Power Supply and RESETZ Timing

6.8 Reference Clock PLL Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency			16.00		MHz
t_c	Cycle time	No clock spreading(1)		62.5		ns
		With clock spreading(1)		1.02 × t_c		ns
t_w(H)	Pulse duration, high	50% to 50% reference points	0.4 x t_c			ns
t_w(L)	Pulse duration, low	50% to 50% reference points	0.4 x t_c			ns
t_{jp}	Period jitter, PLL_REFCLK_I		–250		250	ps

(1) PLL clock spreading is configurable. See *DLPC120-Q1 Programmer's Guide* for a description of how to select spread spectrum options.

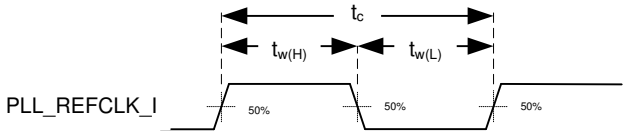


図 6-2. PLL Reference Clock Timing

6.9 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK(1)		3.1	40.0	MHz
t_{p_clkper}	Clock period, PCLK	VIH/VIL	25.0	320.0	ns
t_{p_wh}	Pulse width low, PCLK	VIH/VIL	6.0		ns
t_{p_wl}	Pulse width high, PCLK	VIH/VIL	6.0		ns
t_{p_su}	Setup time - HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK(2)	VIH/VIL	2.0		ns
t_{p_h}	Hold time - HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK(2)	VIH/VIL	2.0		ns
t_t	Transition time - PCLK	10% to 90% reference points	0.2	6	ns

(1) This range includes the 200 ppm of the external oscillator.
(2) The active (capture) edge of PCLK for HSYNC, DATEN, and PDATA(23:0) is software programmable, but defaults to rising edge.

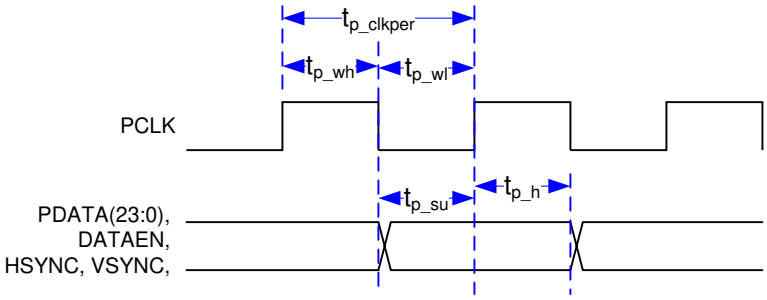


図 6-3. Parallel Video Interface General Timing

6.10 Parallel Interface Frame Timing Requirements

			MIN	MAX	UNIT
t_{p_vsw}	Vertical sync width	50% reference points	1		Lines
t_{p_vbp}	Vertical back porch	50% reference points	6		Lines
t_{vfp}	Vertical front porch	50% reference points	4(1)		Lines
t_{hsw}	Horizontal sync width	50% reference points	5		PCLKs
t_{hbp}	Horizontal back porch	50% reference points	4		PCLKs
t_{hfp}	Horizontal front porch	50% reference points	40(1)		PCLKs

(1) Values depend on many factors and may need to be higher depending on scaling ratio and other factors. See resolution table for typical values that have been verified.

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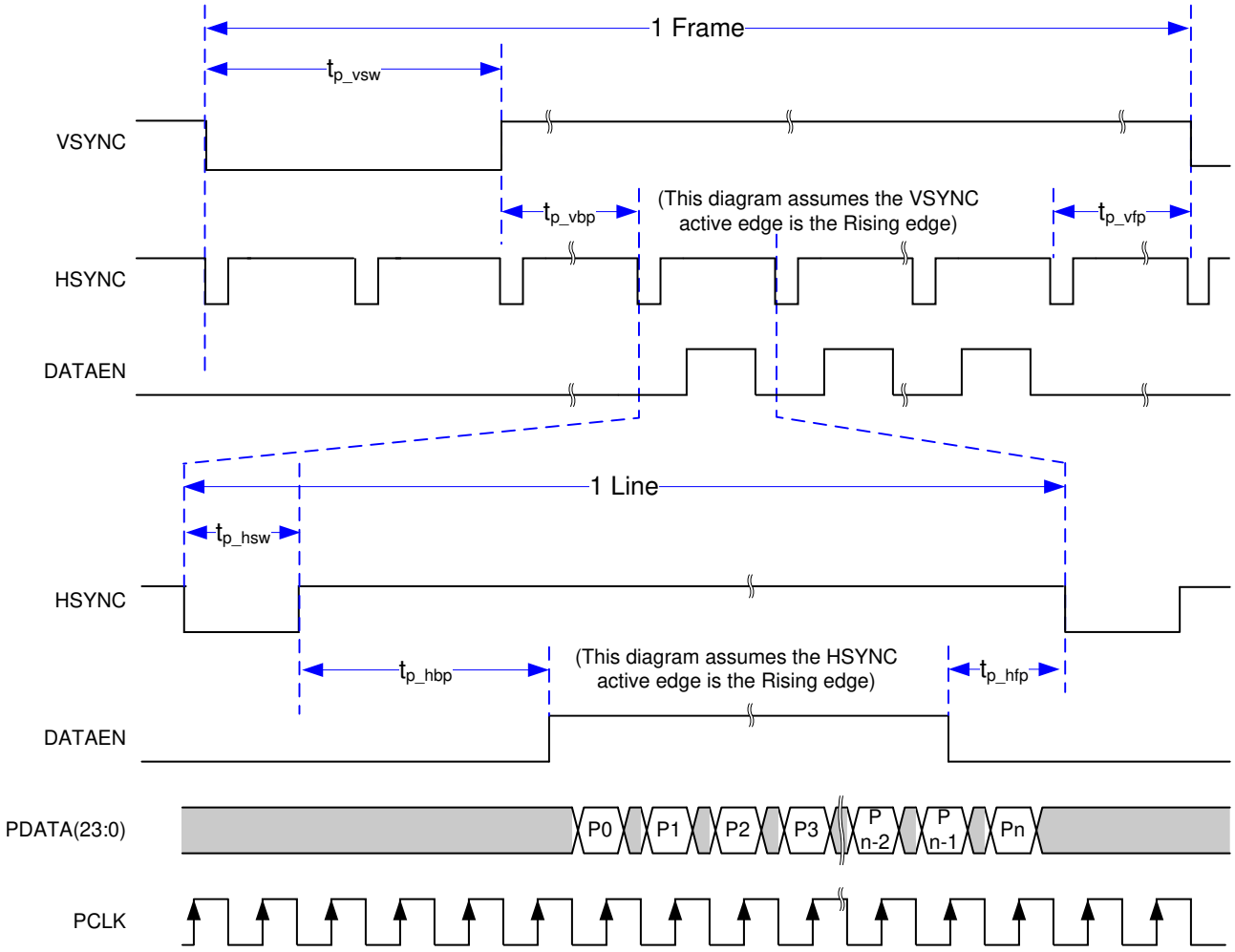


図 6-4. Parallel Interface Frame Timing

6.11 Flash Memory Interface Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, FLASH_SCLK(1)			39.00		MHz
t_{clkper}	Clock period, FLASH_SCLK	50% reference points		25.64		ns
t_{wh}	Pulse width high, FLASH_SCLK	50% reference points	10			ns
t_{wl}	Pulse width low, FLASH_SCLK	50% reference points	10			ns
t_t	Transition time, all signals	20% to 80% reference points, C_{load} = 20 pF	1		3	ns
t_{valid_POCI}	Flash POCI valid data max delay after FLASH_SCLK falling edge	50% reference points			10	ns
$t_{valid_PICO_b}$	PICO valid before rising edge of FLASH_SCLK	50% reference points	2.2			ns
$t_{valid_PICO_a}$	PICO valid after rising edge of FLASH_SCLK	50% reference points	5.2			ns

(1) Spread Spectrum clock modulation, when enabled, will affect the nominal frequency of the FLASH_SCLK.

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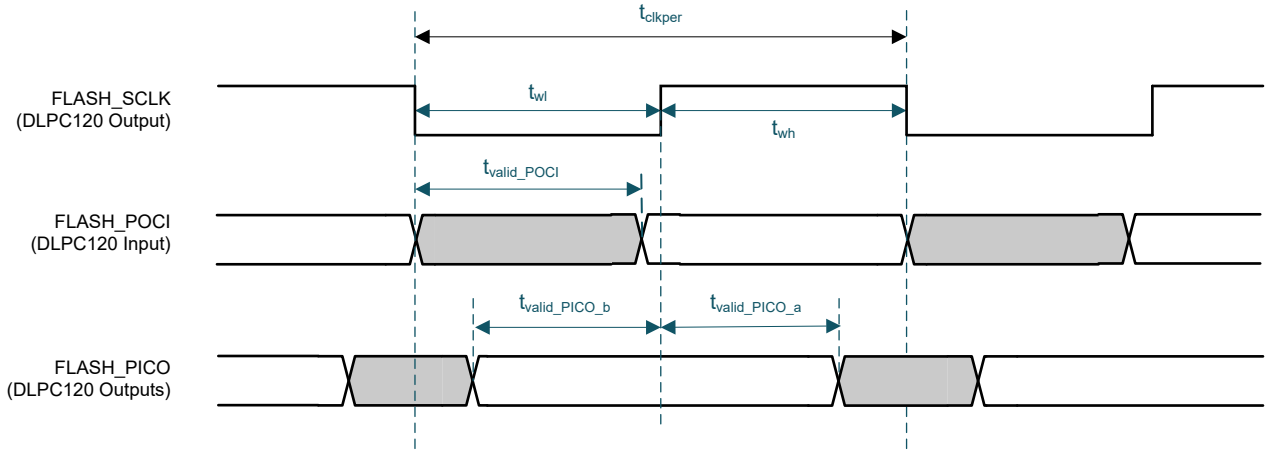


図 6-5. Flash Interface Timing

6.12 DMD Interface Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK and DMD_SAC_CLK(1)		75.00	78.00	80.00	MHz
t_{p_clkper}	Clock period, DMD_DCLK and DMD_SAC_CLK	50% reference points	12.5		15.0	ns
t_{p_clkjit}	Clock jitter, DMD_DCLK and DMD_SAC_CLK	Maximum f_{clock}			200	ps
t_{p_wh}	Pulse width high, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2			ns
t_{p_wl}	Pulse width low, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2			ns
t_t	Transition time, all signals	20% to 80% reference points	0.5		1.5	ns
t_{p_su}	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC relative to both rising and falling edges of DMD_DCLK(2)	50% reference points			1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC signals relative to both rising and falling edges of DMD_DCLK(2)	50% reference points			1.5	ns
$t_{p_d1_skew}$	DMD data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC signals relative to each other	50% reference points			0.20	ns
$t_{p_d2_skew}$	DAD/ SAC data skew - DMD_SAC_BUS, DMD_DAD_OEZ and DMD_DAD_BUS signals relative to DMD_SAC_CLK	50% reference points			1.65	ns
$t_{p_d3_skew}$	DMD_DAD_STRB signal relative to DMD_DCLK	50% reference points			1.65	ns
$t_{p_clk_skew}$	Clock skew – DMD_DCLK and DMD_SAC_CLK relative to each other	50% reference points			0.25	ns

(1) This range includes the 200 PPM of the external oscillator.
(2) Output setup and hold numbers already account for ASIC clock jitter. Only routing skew and DMD setup/ hold need be considered in system timing analysis.

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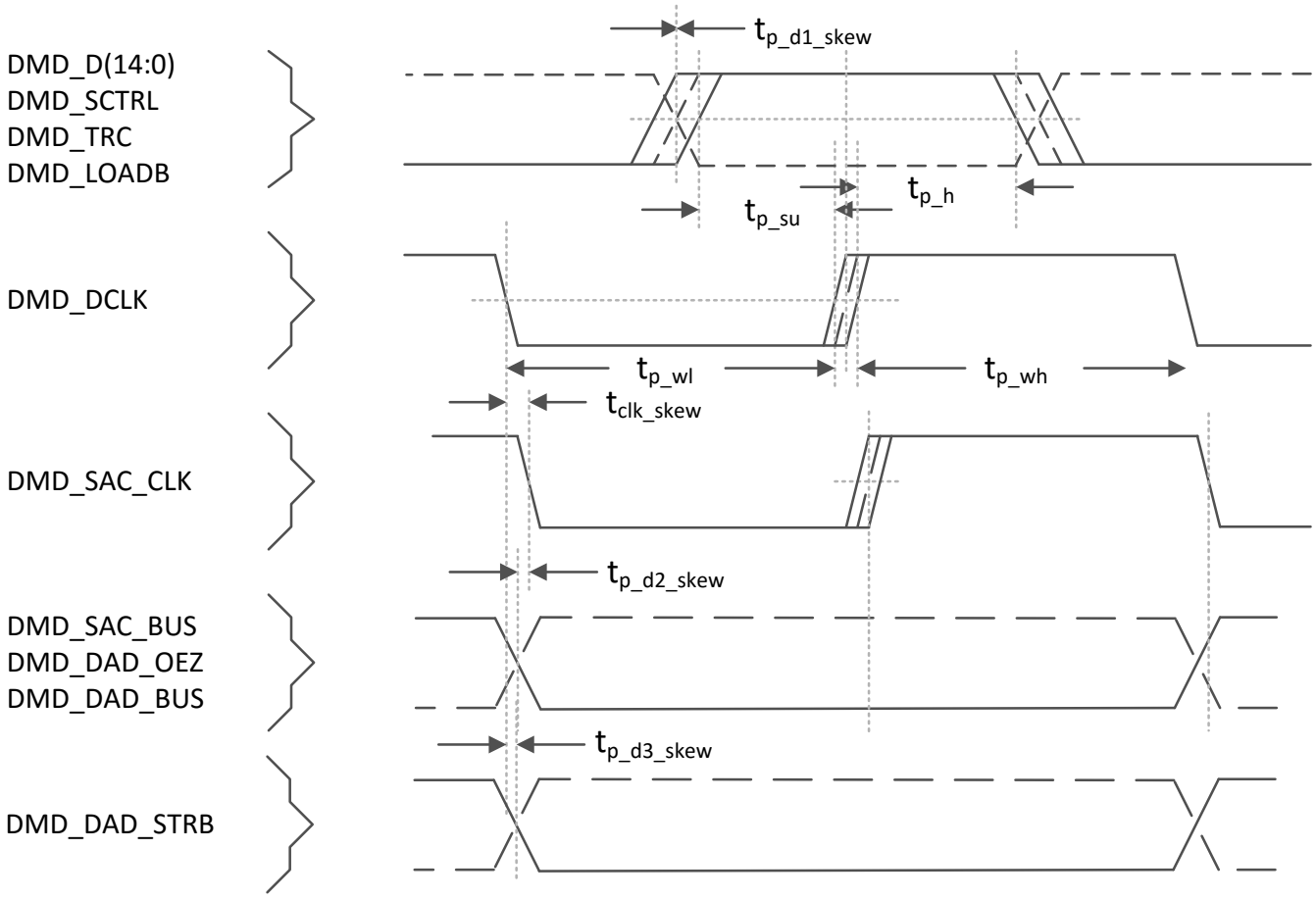


図 6-6. DMD Interface Timing

6.13 JTAG Interface Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, JTAGTCK			10	MHz
t_c	Cycle time, JTAGTCK		100		ns
$t_{w(H)}$	Pulse duration high	50% to 50% reference points	40		ns
$t_{w(L)}$	Pulse duration low	50% to 50% reference points	40		ns
t_t	Transition time, $t_t = t_f = t_r$	20% to 80% reference points		5	ns
t_{su}	Setup time, JTAGTDI valid before JTAGTCK rising edge, and JTAGTMS valid before JTAGTCK rising edge		10		ns
t_h	Hold time, JTAGTDI valid after JTAGTCK, and JTAGTMS valid after JTAGTCK		10		ns
t_{pd}	Output propagation, clock to Q. JTAGTCK falling edge to JTAGTDO		3	20	ns

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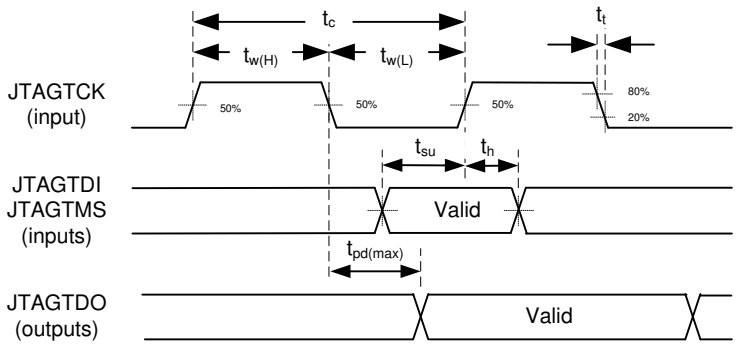


図 6-7. JTAG Interface Timing

6.14 I²C Interface Timing Requirements

		MIN	MAX	UNIT
f_{scl}	Clock frequency	20	400	kHz
t_{sch}	Clock duration high	0.6		µs
t_{scl}	Clock duration low	1.3		µs
t_{sp}	Spike time	0	400	ns
t_{sds}	Setup time	100(3)		ns
t_{sdh}	Hold time	0(1)	0.9(2)	µs
t_{icr}	Input rise time	20 + 0.1 x C_b (4)	300	ns
t_{ocf}	Output fall time	1 + 0.1 x C_b (4)	300	ns
t_{buf}	Bus free time between stop and start conditions	1.3		µs
t_{sts}	Start or repeated start condition setup	0.6		µs
t_{sth}	Start or repeated start condition hold	0.6		µs
t_{sph}	Stop condition hold	0.6		µs

(1) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(2) The maximum t_{HD_DAT} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(3) A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This is automatically the case since the device does not stretch the LOW period of the SCL signal.
(4) C_b = total capacitance of one bus line in pF.

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7 Parameter Measurement Information

7.1 Parallel Interface Input Source Timing

The supported sources with typical timings are shown in 表 7-1.

表 7-1. Parallel Interface Supported Resolutions (Typical Timing)

RESOLUTION		HORIZONTAL			VERTICAL			CLOCK
HORIZONTAL	VERTICAL	FP	BP	SYNC WIDTH	FP	BP	SYNC WIDTH	MHz
320	120	40	32	6	4	7	1	3.1
320	160	42	32	6	7	7	1	4.2
320	240	42	32	6	15	7	1	6.3
400	240	48	50	6	16	6	1	7.8
480	240	96	24	6	8	14	1	9.4
500	250	50	24	6	36	15	1	10.2
640	160	41	41	6	11	19	1	8.3
640	240	104	50	6	14	8	1	12.6
640	480	84	70	6	35	9	1	25.2
800	480	144	50	6	35	9	1	31.5
852	480	68	74	6	35	9	1	31.5
853	480	67	74	6	35	9	1	31.5
854	240	68	72	6	14	9	1	15.8
854	480	68	72	6	35	9	1	31.5
864	480	60	70	6	35	9	1	31.5
960	160	164	70	6	5	9	1	12.6
960	240	164	70	6	13	9	1	18.9
960	250	164	70	6	14	9	1	19.7
960	480	164	70	6	35	9	1	37.8
608	684(1)	46	40	6	104	30	1	33.33

(1) Optical Bypass Mode.

7.2 Design for Test Functions

The DLPC120-Q1 has several built-in test features. These tests can be run to verify ASIC functionality on startup or during normal operation. Refer to *DLPC120-Q1 Programmer's Guide* for more detail regarding test usage. 表 7-2 defines the execution time of each test.

表 7-2. Test Execution Times

TEST NAME	LENGTH (ms)	SUMMARY
DDR2 BIST (Short)	145	The Short DDR2 BIST implements a memory check using a March13 Algorithm to verify the external DDR2 SDRAM frame buffer space. It runs at power-up or also can be executed on demand, but it is recommended to run only at power-up, since the image will flash if executed on demand. The short version runs a portion of the long test.
DDR2 BIST (Long)	470	The Long DDR2 BIST is the same as the Short DDR2 BIST, but it runs the test multiple times.
FLASH BIST (1 MByte)	215	The Flash BIST calculates configuration memory checksum (32 bits) for data integrity of the Flash data and interface. Flash checksum is recommended to be done at power-up to verify configuration settings. The Flash BIST memory range to perform checksum is programmable to up to 32M.
System BIST(2)	See(1)	The System BIST validates the DLPC120-Q1 internal logic. It sends a known test pattern image through the ASIC to verify the checksum at the last stage before the data reaches the DMD. When enabled, the checksum for each frame of data is calculated and stored in an I^2C register.

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表 7-2. Test Execution Times (continued)

TEST NAME	LENGTH (ms)	SUMMARY
DMD Interface Test	6.93	The DMD JTAG BIST validates the connection between the ASIC and DMD. It uses the DMD JTAG interface to sample the ASIC pins and compare against expected values, and it also tries to detect shorts between signals. The BIST is run on demand.
Front End Video Checksum	See(1)	The Front End Video Checksum is used to verify that the video is received correctly at the front end on the specified region of the frame. When enabled, it calculates the checksum for the specified region of the video frame and stored in an I^2C register.
Video Detect Test	See(1)	The Video Detect test shall be used to monitor external video VSYNC. **If external video is not valid, the DMD must be put into a safe state (e.g. switched to an internal black test pattern).**

(1) The length of these tests will vary depending on frame rate but will not exceed 2 frames.
(2) Some processing options must be turned off for this test.

8 Detailed Description

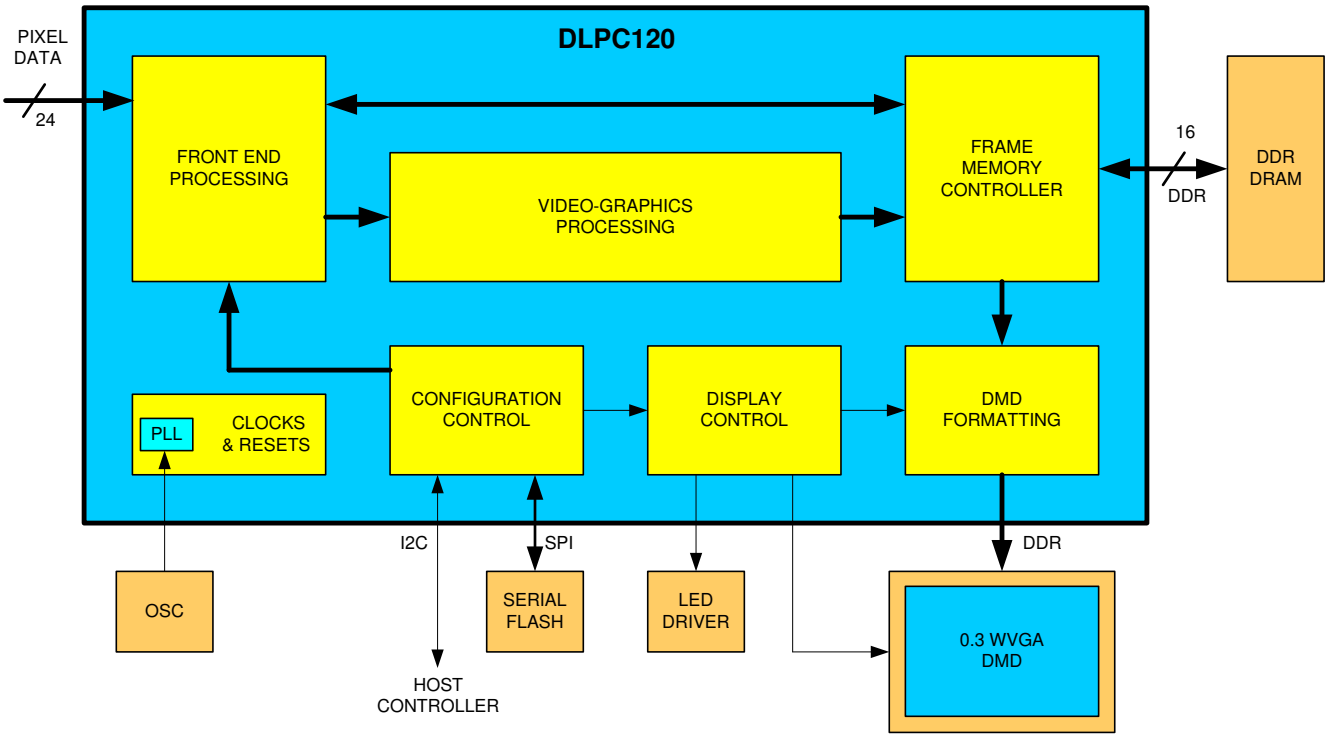
8.1 Overview

The DLPC120-Q1 is compatible with three DMD components:

- DLP3030-Q1 - 0.3 WVGA S450 DMD
- DLP3020-Q1 - 0.3 WVGA FQR DMD
- DLP3021-Q1 - 0.3 WVGA FQR DMD

The DLPC120-Q1 formats incoming video data from a parallel interface and drives the DMD timing to display the video. It also controls illumination enables to strobe illuminators synchronously with the DMD mirror movement. The DLPC120-Q1 is designed for automotive applications with a wide operating temperature range and diagnostic features to identify certain failure modes.

8.2 Functional Block Diagram



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図 8-1. Functional Block Diagram

8.3 Feature Description

8.3.1 Serial Flash Interface

The DLPC120-Q1 utilizes an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of Sequences, CMT tables, and Splash options, while the maximum supported size is 64 Mb. The DLPC120-Q1 can be used to Read, Erase, and program the serial flash. Refer to *DLPC120-Q1 Programmer's Guide* for details of Flash configuration information.

The DLPC120-Q1 utilizes a single SPI interface, employing SPI mode 0 protocol, operating at a frequency of 39.0 MHz. All read operations assume the Flash supports address auto-incrementing. The DLPC120-Q1 should support any flash device that meets these criteria plus the criteria listed in 表 8-1.

表 8-1. SPI Flash Instruction Op Code Compatibility Requirements

FLASH COMMAND	OPCODE
Fast Read (Single Output)	0x0B
Read Electronic Signature	0xAB
Others	May vary

The DLPC120-Q1 does not have any specific Page, Block or Sector size requirements. If the user would like to use a portion of the serial flash for storing external data (such as calibration data) via the I^2C interface, then the minimum sector size needs to be considered as it will drive minimum erase size. Note that use of serial flash for storing external data may impact the number of features that can be supported.

The DLPC120-Q1 does not drive the /HOLD (active low Hold) or /WP (active low Write Protect) pins on the flash device and thus these pins should be tied to a logic high on the PCB via an external pull-up.

表 8-2. DLPC120-Q1 Compatible SPI Flash Device Options

VENDOR	PART NUMBER	DENSITY (Mb)	SUPPLY VOLTAGE SUPPORTED(1)
ISSI	IS25LP064A-JMLE	64	3.3 V
Winbond	W25Q64CVSFAG	64	3.3 V
Spansion	S25FL064P0XMFV000	64	3.3 V
Micron	M25P64-VMF3TPB	64	3.3 V

(1) The Flash supply voltage must match VCCIO_2 on the DLPC120-Q1. Multiple voltage options are often available under the same base part number.

8.3.2 Serial Flash Programming

The external serial flash may also be programmed via the same SPI interface which is connected to the DLPC120-Q1. In order to avoid conflicting data on this interface, the DLPC120-Q1 must be held in reset while the flash memory is programmed. See flash specification for details of the programming configuration.

8.3.3 DDR2 Memory Interface

The DLPC120-Q1 ASIC DDR2 Memory interface consists of a 16-bit wide, 312-MHz (nominal) DDR2 interface with standard signaling. The DLPC120-Q1 only support DDR2 interface with external termination. The DDR2 interface is a very high speed signaling interface.

A DDR2 memory should be selected that supports the 312-MHz clock frequency and compliant to the JEDEC standard for DDR2 memories (JESD79-2A).

表 8-3. Compatible JEDEC DDR2 Devices

PARAMETER	MIN	MAX	UNITS
JEDEC DDR2 device speed grade(1)	DDR2-800		
JEDEC DDR2 device bit width	X16		Bits
JEDEC DDR2 device count	1		Device(s)
JEDEC DDR2 Memory size	512	1024	MByte

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表 8-3. Compatible JEDEC DDR2 Devices (continued)

PARAMETER	MIN	MAX	UNITS
CAS Latency	5	5	

(1) The DDR2 interface operates with a clock frequency of 312 MHz, higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.

表 8-4. DLPC120-Q1 Compatible DDR2 Device Options

VENDOR	PART NUMBER	SIZE	ORGANIZATION	SPEED GRADE	C_L
ISSI	IS46DR16320C-25DBLA2	512 Mb	32Mx16	DDR2-800	5
Micron	MT47H64M16HR-25E AAT	1 Gb	32Mx16	DDR2-800	5
Micron	MT47H32M16HR-25E AAT	512 Mb	32Mx16	DDR2-800	5

8.3.4 JTAG and DMD Interface Test

The DLPC120-Q1 has two test interfaces using JTAG protocol:

- A standard JTAG (IEEE-1149) function of the ASIC is provided. The TI-provided BSDL file contains the details of the DLPC120-Q1 boundary scan chain. This JTAG interface is provided to enable system level validation of proper assembly of the DLPC120-Q1 onto a PCB.
- The DLPC120-Q1's DMD interface is designed to be the controller for an in-system DMD interface test. The DMD interface should be connected directly to the DMD's JTAG pins. This interface is exclusively designed and verified to support the DLP3030-Q1, DLP3020-Q1 and DLP3021-Q1.

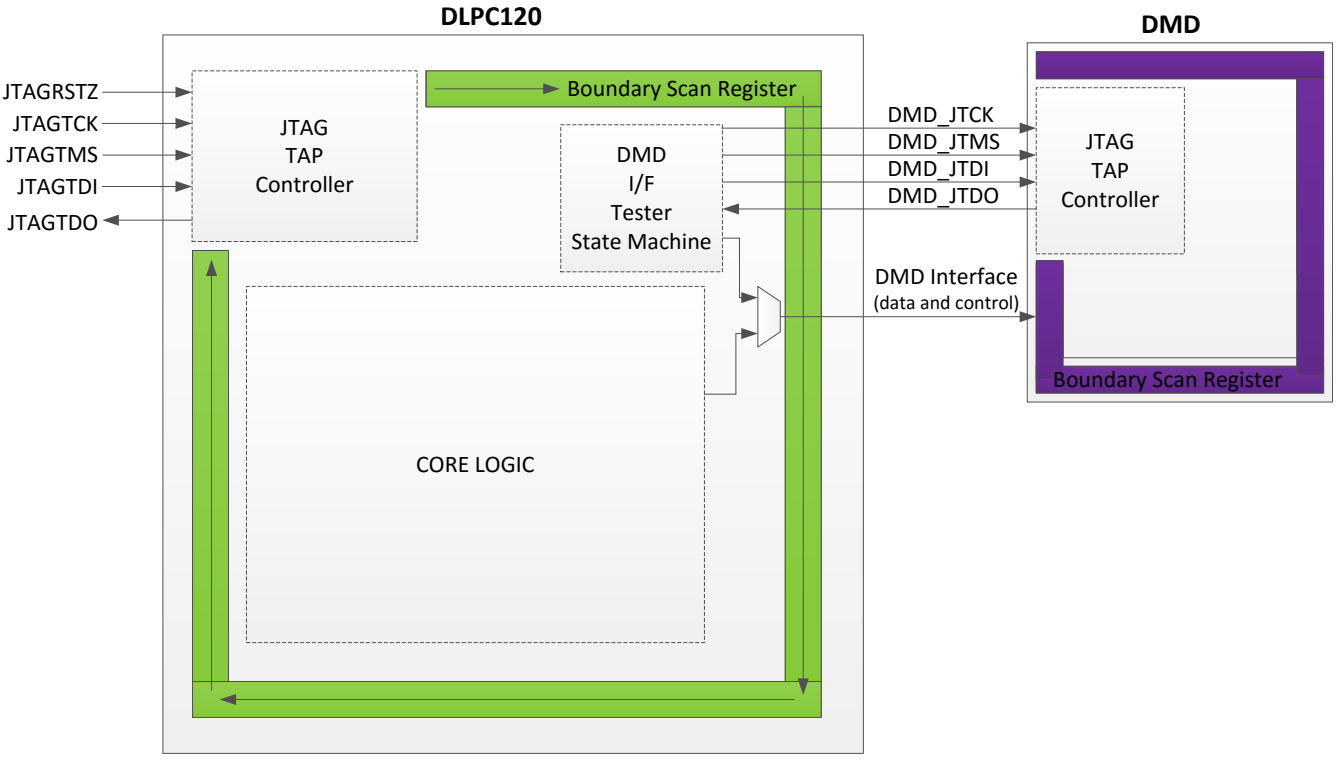


図 8-2. JTAG and DMD Interface Test

Using the DMD JTAG function, the DMD interface signals are toggled, and the connection at the DMD is verified by using the DMD JTAG signals to sample the inputs, and then toggled back to the DLPC120-Q1 for comparison to expected values. All DMD logic signals, except DAD OEZ, are tested individually for stuck high or low independently. Alternating data pattern for adjacent pins, as well as "walking 1's" and "walking 0's" patterns are used during the test. The DAD_OEZ is only tested in the high state as asserting this signal and toggling the inputs could cause damage to the DMD. Refer to 図 8-3 for recommended connections for the DLPC120-Q1 boundary scan test configuration. Refer to 図 8-4 for recommended connections of the DLPC120-Q1 to DMD

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interface test. For additional information about the DMD Boundary scan function refer to the specific DMD device datasheet.

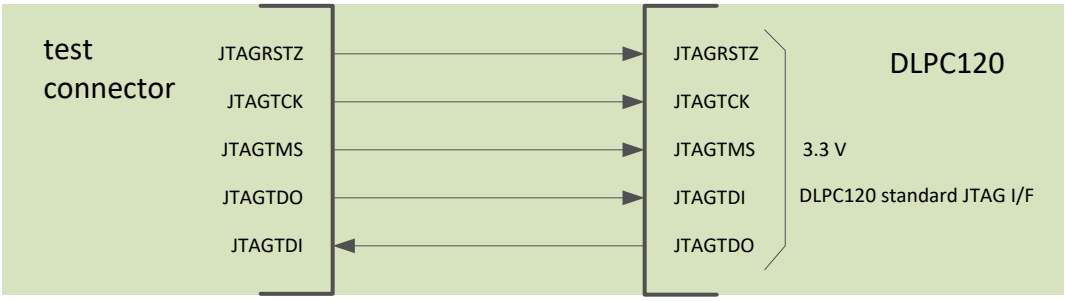


図 8-3. DLPC120-Q1 JTAG Boundary Scan Connection Example

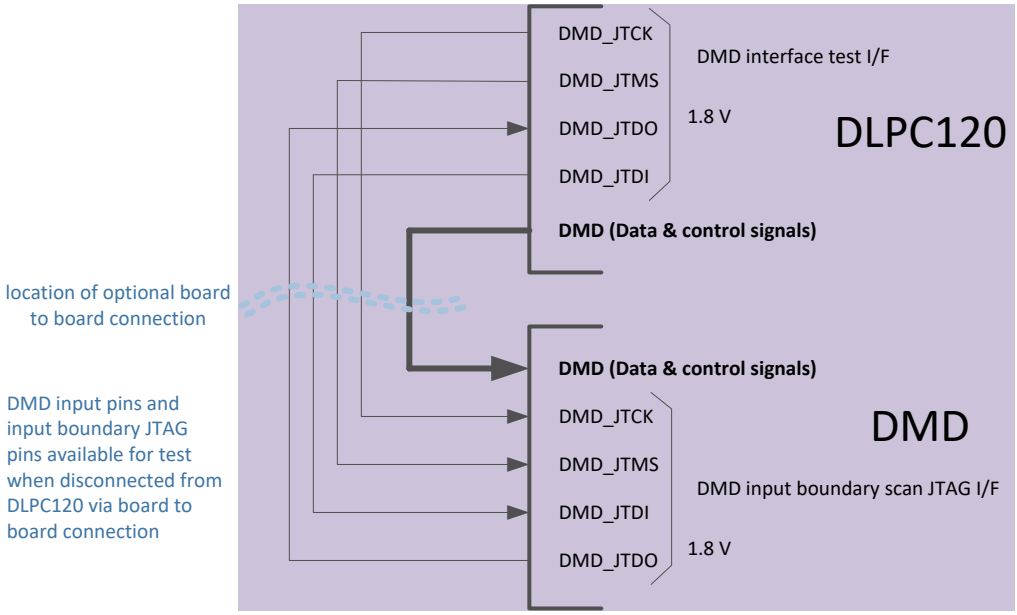


図 8-4. DLPC120-Q1 JTAG to DMD Interface Connection Example

8.3.5 Temperature Monitor Function

The DLPC120-Q1 connects with the TMP411 through a standard I^2C bus protocol using the TMP_SDA and TMP_SCL pins. The internal temperature controller initializes the TMP411 to read the temperature of the DMD.

The TMP controller issues a set of read commands at eight times per second through the I^2C interface to read the remote temperature (DMD) and local temperature from the TMP411.

The TMP411 monitors the DMD temperature and controls the DMD park operation when the DMD is operated beyond the required specification. See the *DLP3030-Q1, DLP3020-Q1 and DLP3021-Q1 Data Sheet* for the DMD operating temperature. If the DMD park operation is used, then a 1-degree hysteresis is applied. See the *DLPC120-Q1 Programmer's Guide* for description of this function.

8.3.6 Host Command Interface

The DLPC120-Q1 provides two I^2C interface port for host commands. Only one of these ports is intended to be used at a time. The unused port is meant for system debug or development purposes. The I^2C protocol and register definitions are defined in the *DLPC120-Q1 Programmer's Guide*.

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8.4 Device Functional Modes

The DLPC120-Q1 has three operational display modes, which are selected with command list execution via the Host control interface. These display modes are External Video, Splash Screen, and Test Pattern.

8.4.1 External Video Mode

Upon the release of reset and initialization, the DLPC120-Q1 will automatically enter in External Video mode. This mode will process the video source on the parallel RGB input interface at a given resolution and frame rate. The system supports multiple input video resolutions, and the resolution expected by the DLPC120-Q1 can be configured via command list execution. See 表 7-1 for the different external video resolutions supported by the system.

8.4.2 Splash Screen Mode

This mode displays a custom, static image, which is stored in the DLPC120-Q1 Application Serial Flash memory. The content of the splash image is configurable. The Flash memory can store multiple Splash Screens, where the quantity is limited by the size of the splash images, size of the memory chip, and capacity of the remaining memory contents. Splash Screens are displayed via command list execution. Contact a TI Applications Engineer in order to change the splash images stored in the Flash memory.

8.4.3 Test Pattern Mode

This mode displays a fixed, static image, which is stored in the DLPC120-Q1 Application Serial Flash memory. The content of the test patterns are pre-defined, limited by the design of the DLPC120-Q1. Test Patterns are displayed via command list execution. See *DLPC120-Q1 Programmer's Guide* for a list and image of the supported Test Patterns.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC120-Q1 is a DLP display processor that supports automotive head-up display (HUD) applications. It accepts data from a variety of video input resolutions and provides the digital image processing and control necessary to drive an LED based DLP display system. This document reflects the operation, pinout, and timing associated with the DLPC120-Q1 device only.

The DLPC120-Q1 is compatible with three DMD components:

- DLP3030-Q1 – 0.3 WVGA S-450 DMD
- DLP3020-Q1 – 0.3 WVGA FQR DMD
- DLP3021-Q1 – 0.3 WVGA FQR DMD

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9.2 Typical Application

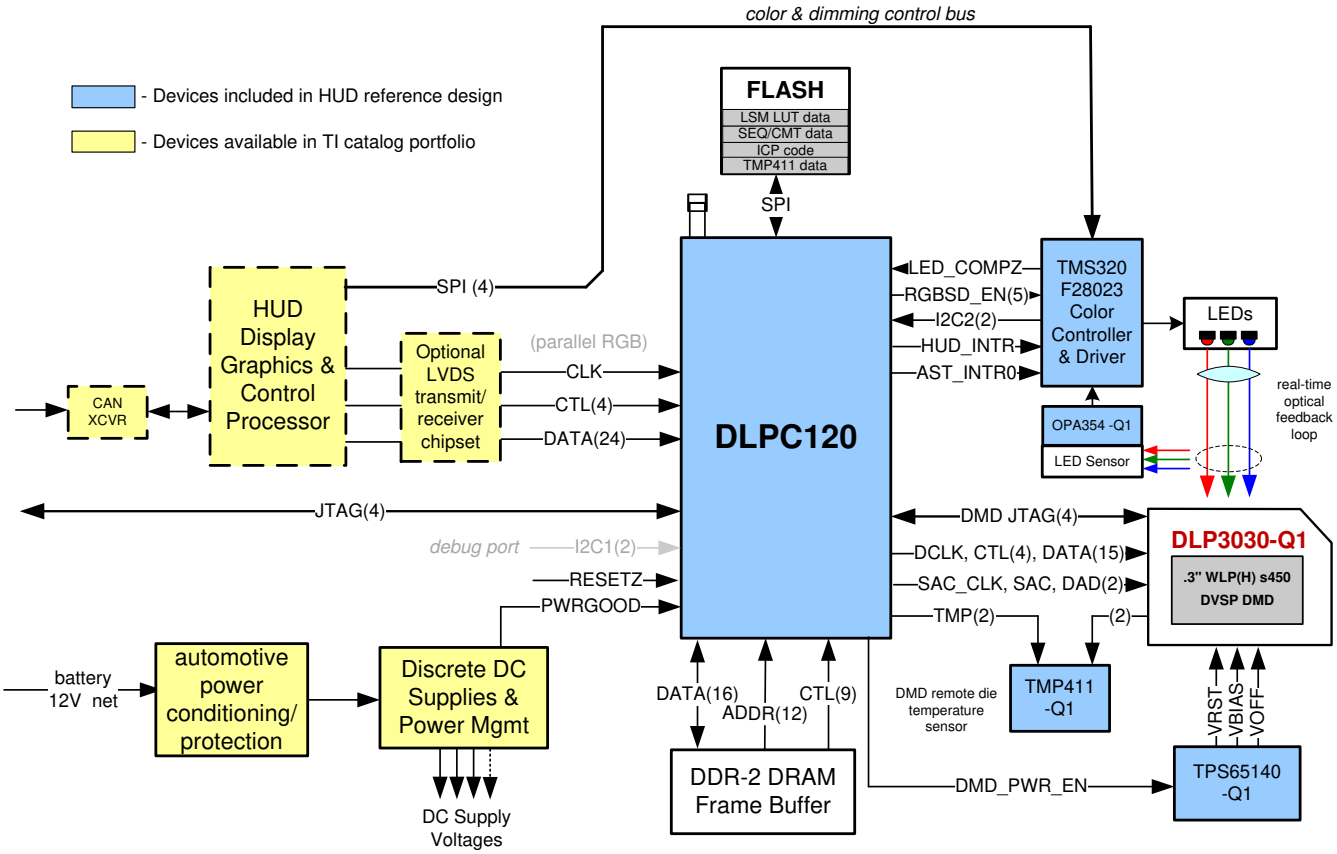


図 9-1. DLPC120-Q1 System Block Diagram

9.2.1 Design Requirements

The 図 9-1 shows a typical projector application. For this application, the DLPC120-Q1 is controlled by a separate control processor, and the image data is received through the parallel RGB interface.

As with prior DLP® electronics solutions, image data is 100% digital from the DLPC120-Q1 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC120-Q1 processes the digital input image and converts the data into a bit-plane format, as needed by the DMD. The DMD then reflects light to the screen using binary pulse-width-modulation (PWM) for each pixel mirror. The viewer's eyes integrate this light to form brilliant, crisp images.

The DLPC120-Q1 provides signals that enable red, green, and blue LEDs to synchronize to the DMD PWM bit planes. These signals combined with an external MCU (TMS320F28023) can be used to create a very high dynamic dimming range necessary for automotive heads-up display (HUD) applications.

The DLPC120-Q1 also features temperature monitoring of the DMD in order to automatically park the micromirrors when the DMD temperature is beyond the operating range.

The DLPC120-Q1 uses the DDR2 SDRAM as a frame buffer to convert RGB video data into the necessary bit plane format required by the DMD. The DLPC120-Q1 also supports multiple input resolutions and scales them to match the native .3" WVGA DMD format. These images can also be electronically bezel-adjusted on the DMD, which could allow the displayed image to be electronically adjusted for mechanical misalignment. The DLPC120-Q1 is configured at power up with data stored in the Flash memory via SPI. The Flash interface is the primary method to configure the controller.

The DLPC120-Q1 supports system diagnostic and self-check features, such as video detection, DDR2 memory Built-in Self Test (BIST), System BIST, Flash BIST, and JTAG (in system and DMD interface).

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Due to the mechanical nature of the micromirrors, the latency of the DMD and DLPC120-Q1 chipset is fixed across all temperature and operating conditions. The observed video latency is one frame, or 16.67 ms at an input frame rate of 60 Hz. However, please note that the use of the DLPC120-Q1 bezel adjustment feature, if enabled, requires an additional frame of processing.

Contact a TI Applications Engineer in order to gain access to a fully functional reference design based on the DLP30xx-Q1 chipset.

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10 Power Supply Recommendations

10.1 Power Supply Filtering

The following filtering circuits are recommended for the various supply inputs.

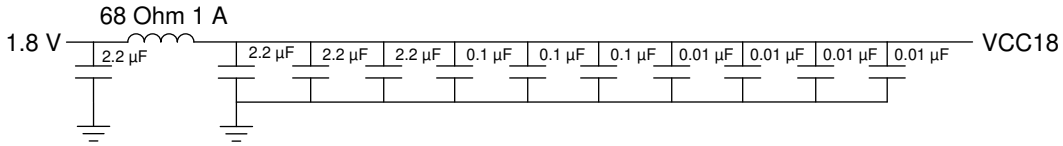


図 10-1. VCC18 Recommended Filter

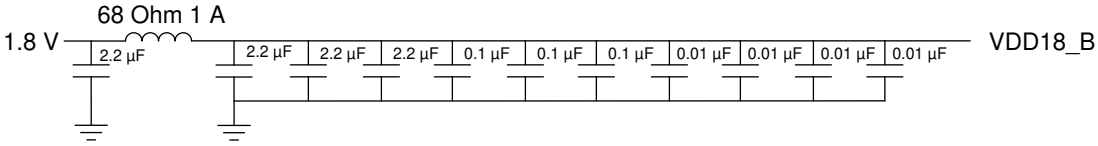


図 10-2. VDD18_B Recommended Filter

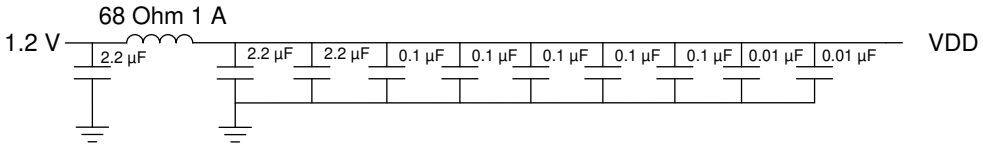


図 10-3. VDD Recommended Filter

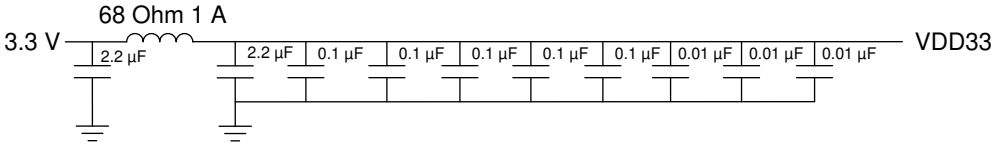


図 10-4. VDD33 Recommended Filter

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11 Layout

11.1 Layout Guidelines

11.1.1 PCB layout guidelines for internal ASIC PLL power

The PLL's two analog supplies, VCCA and VSSA, shall be filtered with two series ferrite beads and two shunt 0.1-µF and 0.01-µF capacitors. The ferrite on VSSA is preferred but optional.

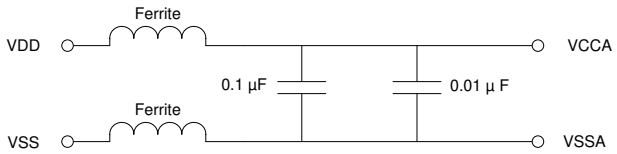


図 11-1. PLL Power Guidelines

表 11-1. Recommended PLL Filter Components

COMPONENT	PARAMETER	RECOMMENDED VALUE	UNIT
Shunt Capacitor	Capacitance	0.1	µF
Shunt Capacitor	Capacitance	0.01	µF
Series Ferrite	Impedance at 10 MHz	>= 180	Ω
	Impedance at 100 MHz	>= 600	Ω
	DC Resistance	< 0.40	Ω

Example ferrite bead recommendations are listed in 表 11-2.

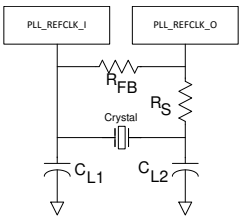
表 11-2. PLL Power Ferrite Bead Recommendations

PART NUMBER	R @ DC	Z @ 10 MHz	Z @ 100 MHz	Z @1-GHz SIZE
BLM18EG601SN1	0.35	200	600	0603
BLM15AX601SN1	0.34	190	600	0402

The capacitors should be mounted as close to the package balls as possible.

11.1.2 DLPC120-Q1 Reference Clock

The DLPC120-Q1 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. The recommended crystal configurations and reference clock frequencies are listed in 表 11-3, with additional required discrete components shown in 図 11-2 and defined in 表 11-3.



A. C_L = Crystal load capacitance
B. R_{FB} = Feedback Resistor

図 11-2. Discrete Components Required When Using Crystal

11.1.2.1 Recommended Crystal Oscillator Configuration

表 11-3. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	

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表 11-3. Recommended Crystal Configuration (continued)

PARAMETER	RECOMMENDED	UNIT
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum crystal equivalent series resistance (ESR)	80	Ω
Temperature range	–40°C to +105°C	°C
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See equation in (1)	pF
C_{L2} external crystal load capacitor	See equation in (2)	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) CL1 = 2 × (CL – Cstray_pll_refclk_i), where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin PLL_REFCLK_I. PLL_REFCLK_I device capacitance is approximately 3 pF.
(2) CL2 = 2 × (CL – Cstray_pll_refclk_o), where: Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin PLL_REFCLK_O. PLL_REFCLK_O device capacitance is approximately 3 pF.

11.1.3 General PCB Recommendations

TI provides PCB design files that serve as a reference for DLPC120-Q1 and DLP30xx-Q1 chipset PCB schematics and layout designs. Please contact a TI Applications Engineer to access these files.

11.1.4 PCB Routing Guidelines

All signals should follow a 0.005-in width 0.015-in spacing design rule. Minimum trace clearance from the ground ring around the PCB shall be 0.1-in minimum. Actual trace widths and clearances will be determined based on an analysis of impedance and stack-up requirements, some variation is expected.

表 11-4. PCB Trace Matching Recommendations

GROUP	SIGNAL	CONSTRAINTS(1)
DDR2 I/F	MEM_CLK MEM_CLKZ MEM_DQS0 MEM_DQSZ0 MEM_DQS1 MEM_DQSZ1	Lengths Matched to 25 mils Max Total Length: 1500 mils Impedance: 100-Ω differential (± 10%)
	MEM_DQ[0:15]	Lengths Matched to 50 mils Max Total Length: 1500 mils Impedance: 50 Ω (± 10%)
	MEM_RASZ MEM_CASZ MEM_WEZ MEM_CSZ MEM_CKE MEM_A[0:12]	Lengths Matched to 100 mils Max Total Length: 1500 mils Impedance: 50 Ω (± 10%)
DMD I/F	DMD_D[0:14] DMD_DCLK DMD_BUS DMD_STRB DMD_OEZ DMD_LOADB DMD_SAC_CLK DMD_SAC_BUS DMD_SCTRL DMD_TRC DMD_JTCK DMD_JTDI DMD_JTDO DMD_JTMS	Lengths Matched to 50 mils Max Total Length: 10000 mils Impedance: 50 Ω (± 10%)

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表 11-4. PCB Trace Matching Recommendations (continued)

GROUP	SIGNAL	CONSTRAINTS(1)
Serial Flash I/F	FLASH_DCLK, FLASH_POCI, FLASH_PICO, FLASH_CSZ	Lengths Matched to 100 mils Max Total Length: 2500 mils Impedance: 50 Ω (± 10%)

(1) Trace lengths on Layers 1 and 10 should be less than 50 mils.

11.1.5 Number of Layer Changes

- As a reference, the TI design uses no more than three layer changes per trace.
- Individual differentially matched signal pairs can be routed on different layers, but the signals of a given pair should not change.

11.1.6 Terminations

- All DMD I/F signals should be terminated at the source with a 20-Ω series resistor.
- MEM_CLK and MEM_CLKZ should be terminated with an external 100-Ω differential resistor across the two signals as close to the DRAM as possible. All other DDR2 control and data signals should be pulled to VTT(0.9 V) with a 56-Ω resistor as close to the DRAM as possible.

11.1.7 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended that unused ASIC input pins be tied through a pull-up resistor to its associated power supply or a pull-down to ground. For ASIC inputs with an internal pull-up or pull-down resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pull-up and pull-down resistors are weak and should not be expected to drive the external line. The DLPC120-Q1 implements very few internal resistors and these are noted in the pin list.

Unused output-only pins can be left open. When possible, it is recommended that unused Bi-directional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or down) using an appropriate resistor.

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12 Device and Documentation Support

12.1 Third-Party Products Disclaimer

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12.2 Device Support

12.2.1 Device Nomenclature

12.2.1.1 Device Markings

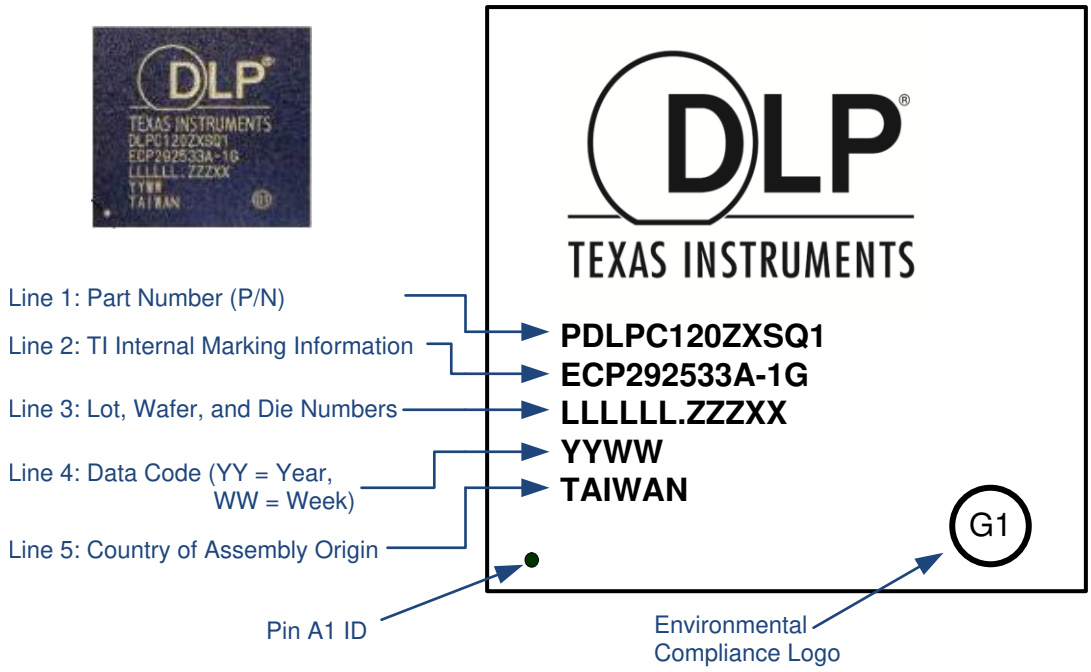


図 12-1. Device Marking

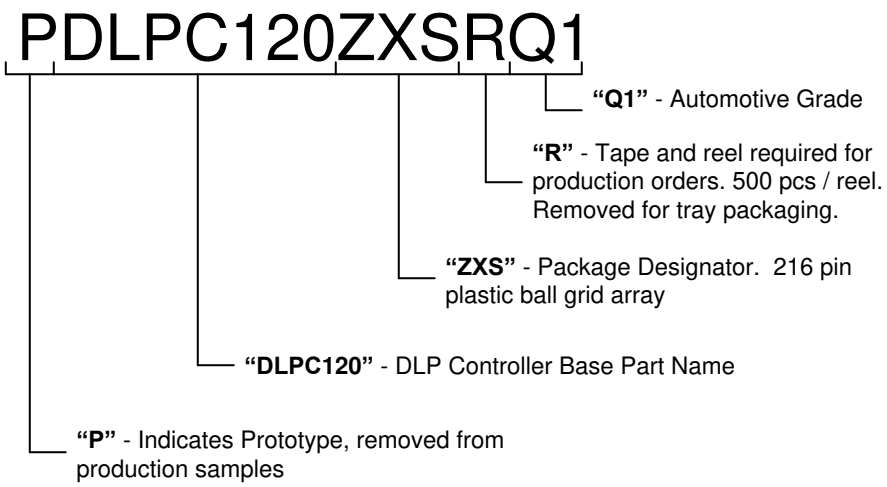


図 12-2. Part Number Definition

12.3 Documentation Support

12.3.1 Related Documentation

For related documentation see the following:

- DLP3030-Q1 product folder for the *DLP3030-Q1 Data Sheet.*
- DLP3020-Q1 product folder *for the DLP3020-Q1 Data Sheet.*
- DLP3021-Q1 product folder *for the DLP3021-Q1 Data Sheet.*

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DLPC120ZXSQ1	Active	Production	NFBGA (ZXS) | 216	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	DLPC120ZXSQ1 ECP292533A-1G
DLPC120ZXSQ1.B	Active	Production	NFBGA (ZXS) | 216	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	DLPC120ZXSQ1 ECP292533A-1G
DLPC120ZXSRQ1	Active	Production	NFBGA (ZXS) | 216	500 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	DLPC120ZXSQ1 ECP292533A-1G
DLPC120ZXSRQ1.B	Active	Production	NFBGA (ZXS) | 216	500 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 105	DLPC120ZXSQ1 ECP292533A-1G

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

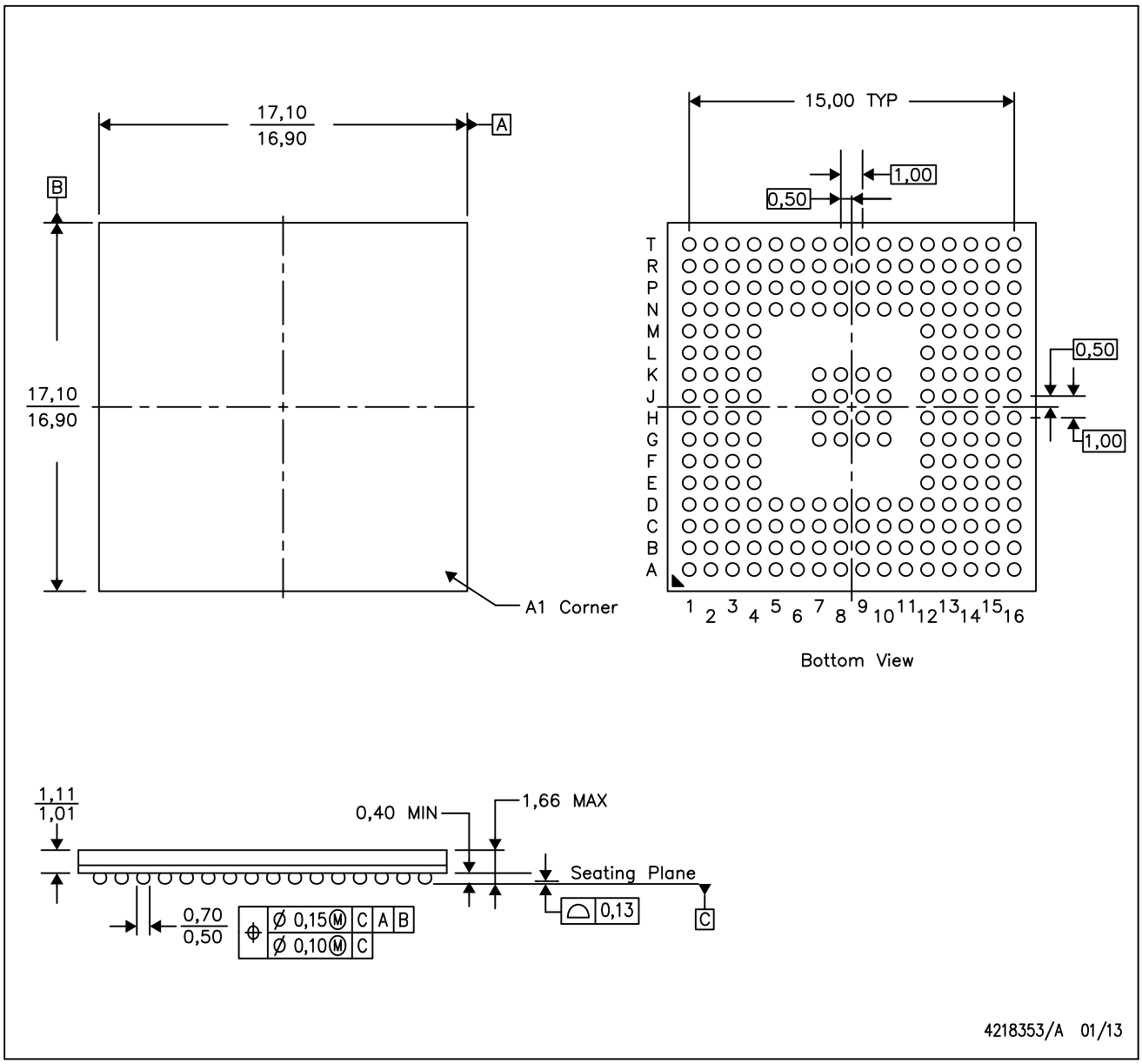
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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ZXS (S–PBGA–N216) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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