TEXAS INSTRUMENTS
DP83561-SP
JAJSLL2B – APRIL 2021 – REVISED NOVEMBER 2021

DP83561-SP 放射線耐性保証 (RHA)、10/100/1000 イーサネット PHY トランシーバ、SEFI 処理サブシステム付き

1 特長

- QML Class V (QMLV)、RHA、SMD 5962-20216
- ミリタリー温度範囲:-55℃～125℃
- 耐放射線性能
  - RHA (最大 TID = 300krad(Si))
  - SEL 耐性 (LET = 121MeV·cm^2/mg)
- シングル・イベント機能割り込み (SEFI) モニタ・スイート
  - モニタ
    - IEEE PCS ステート・マシン・モニタ
    - ECC 構成レジスタ・モニタ
    - PLL ロック・モニタ
    - オンチップ温度モニタ
  - アクション
    - イベント監視用の割り込みピン
  - 補正
    - ECC 保護付き構成レジスタ
    - ピンによる構成が可能な SEFI 自動回復
    - シリアル・マネージメント・インターフェイス (SMI) 無効
- IEEE802.3 1000BASE-T、100BASE-TX および 10BASE-Te 仕様との完全な互換性
- 短い RGMII レイテンシ (TX < 90ns、RX < 290ns)
- TSN (Time Sensitive Network) 準拠
- MAC インターフェイス:RGMII、MII
- MDI 終端抵抗を内蔵
- RGMII 終端インピーダンスをプログラム可能
- 電源:2.5V、1.8V、1.1V
- I/O 電圧:1.8V、2.5V、3.3V
- 25MHz または 125MHz の同期クロック出力
- ケーブル診断:TDR を使用した開放、短絡
- JTAG のサポート

2 アプリケーション

- コマンド・データおよび処理 (CD および H)
- 通信ペイロード
- レーダー画像処理ペイロード
- 光学画像処理ペイロード
- レーザー通信ペイロード
- 科学的探査ペイロード

3 概要

DP83561-SP は、宇宙の高放射線環境向けに設計された高信頼性ギガビット・イーサネット PHY です。DP83561-SP は、必要な機能がすべて揃った低消費電力の物理層トランシーバで、PMD サブレイヤを内蔵し、10BASE-Te、100BASE-TX、1000BASE-T の各イーサネット・プロトコルをサポートしています。

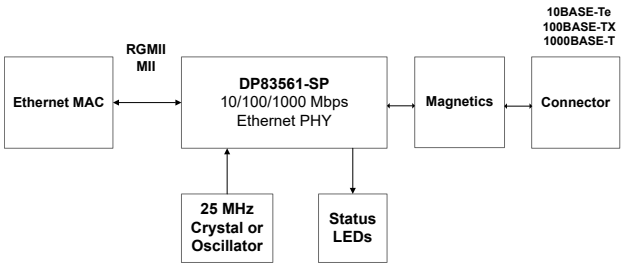
DP83561-SP は、極めて過酷な環境でも 10/100/1000Mbps のイーサネット LAN を簡単に実装できるよう設計されています。外部の変圧器を通して、ツイストペアのメディアへ直接接続が可能です。このデバイスは、Reduced GMII (RGMII) および MII により、MAC 層へ直接接続されます。

このデバイスは、テキサス・インスツルメンツが CMOS プロセスで製造する放射線耐性強化設計 (RHBD) を採用し、ボディ・サイズ 11mm × 11mm（公称値）の 64 ピン・セラミック・クワッド・フラット・パック (CQFP) パッケージで供給されます。

製品情報

型番	グレード	パッケージ	本体サイズ (公称)
5962F2021601VXC	フライト・モデル (QMLV) RHA ～ 300krad (Si)	CQFP (64)	11.00mm × 11.00mm
DP83561HBE/EM	エンジニアリング・モデル(1)	CQFP (64)	11.00mm × 11.00mm

(1) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフロー (バーンインがないなど) に従って処理されており、25℃の温度定格のみがテストされています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。部品は、MIL に規定されている温度範囲全体 (–55℃～125℃) にわたる性能も動作寿命全体にわたる性能も保証されていません。エンジニアリング・モデルの詳細については、『Texas Instruments Engineering Evaluation Units versus MIL-PRF-38535 QML Class V Processing』を参照してください。



標準的なイーサネット・システムのブロック図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2021) to Revision B (November 2021)	Page
• 事前情報から量産データのリリースに変更	1

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5 Pin Configuration and Functions

For Assembly, please refer to package drawing section

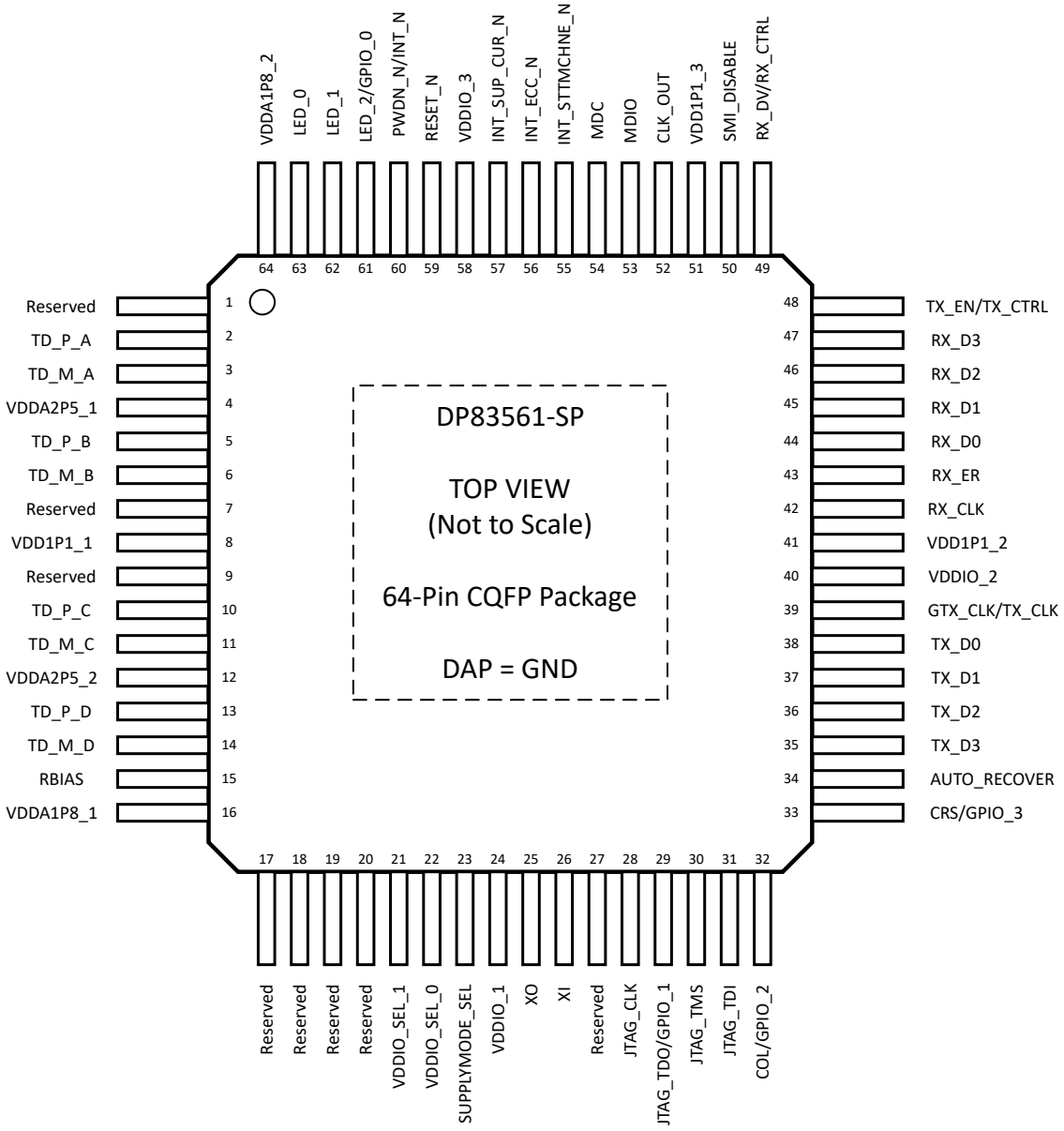


図 5-1. HBE Package 64-Pin CQFP Top View

表 5-1. Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	Reserved	I/O		Reserved. Keep it NC
2	TD_P_A	I/O	A	Differential Transmit and Receive Signals
3	TD_M_A	I/O	A	Differential Transmit and Receive Signals
4	VDDA2P5_1	I	A	2.5-V Analog Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
5	TD_P_B	I/O	A	Differential Transmit and Receive Signals
6	TD_M_B	I/O	A	Differential Transmit and Receive Signals
7	Reserved	I	A	Reserved. Keep it NC
8	VDD1P1_1	I	A	1.1-V Digital Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
9	Reserved	I	A	Reserved. Keep it NC
10	TD_P_C	I/O	A	Differential Transmit and Receive Signals
11	TD_M_C	I/O	A	Differential Transmit and Receive Signals
12	VDDA2P5_2	I	A	2.5-V Analog Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
13	TD_P_D	I/O	A	Differential Transmit and Receive Signals
14	TD_M_D	I/O	A	Differential Transmit and Receive Signals
15	RBIAS	I	A	Bias Resistor Connection. A 10-kΩ ±1% resistor should be connected from RBIAS to GND. A 90-pF ±10% capacitor should be connected in parallel with the bias resistor.
16	VDDA1P8_1	I	A	In three-supply mode, an external 1.8-V (±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details. In two supply mode, no external supply is required for this pin. When unused, no connections should be made to these pins.
17	Reserved	-	A	Reserved. Keep it NC
18	Reserved	-	A	Reserved. Keep it NC
19	Reserved	-	A	Reserved. Keep it NC
20	Reserved	-	A	Reserved. Keep it NC
21	VDDIO_SEL_1	I	A, S	VDDIO_SEL1/ VDDIO_SEL0: 00 (Default): VDDIO 3V3 01: Reserve 10: VDDIO 2V5 11: VDDIO 1V8
22	VDDIO_SEL_0	I	A, S	
23	SUPPLYMODE_SEL		S	0 = Dual supply mode (VDDA1P8 left floating) (Default) 1 = Triple supply mode (VDDA1P8 supplied by system)
24	VDDIO_1	I	A	I/O Power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
25	XO	O	A	CRYSTAL OSCILLATOR OUTPUT: Second terminal for 25-MHz crystal. Must be left floating if a clock oscillator is used.
26	XI	I	A	CRYSTAL OSCILLATOR INPUT: 25-MHz oscillator or crystal input.
27	Reserved	-	A	Reserved. Keep it NC
28	JTAG_CLK	I	PU	JTAG TEST CLOCK: IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity.

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE[1]	DESCRIPTION
NO.	NAME			
29	JTAG_TDO/GPIO_1	O	PD	JTAG TEST DATA OUTPUT: IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device through TDO. General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details. This pin should be pulled down by a 2.49-kΩ resistor.
30	JTAG_TMS	I	PU	JTAG TEST MODE SELECT: IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. TI recommends that the user apply 3 clock cycles with JTAG_TMS high to reset the JTAG.
31	JTAG_TDI	I	PU	JTAG TEST DATA INPUT: IEEE 1149.1 Test Data Input pin, test data is scanned into the device through the TDI.
32	COL/GPIO_2	I/O	PD	COLLISION DETECT: Asserted high to indicate detection of a collision condition (assertion of CRS due to simultaneous transmit and receive activity) in Half-Duplex modes. This signal is not synchronous to either MII clock (GTX_CLK, TX_CLK or RX_CLK). (Default) General Purpose I/O: This signal provides a multi-function configurable I/O. Refer to the GPIO_MUX_CTRL register for details.
33	CRS/GPIO_3	I/O	PD, S	CARRIER SENSE: CRS is asserted high to indicate the presence of a carrier due to receive or transmit activity in Half-Duplex mode. (Default) General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
34	AUTO_RECOVER	I	PD, S	0 = DP83561-SP will take no automatic action based on SEFI. SEFI event interrupts will be generated normally. (Default) 1 = Configures the DP83561-SP to automatically apply RESET signal to PHY logic when a SEFI is detected by one of the monitors configured (STATE_MACHINE, temperature monitor, PLL lock, ECC registers). Default register values will be reloaded and pin options. SEFI event interrupts will be generated normally.
35	TX_D3	I	PD	TRANSMIT DATA: Signal TX_D [3:0] carries data from the MAC to the PHY in RGMII mode and MII mode. Data is synchronous to the transmit clock.
36	TX_D2	I	PD	
37	TX_D1	I	PD	
38	TX_D0	I	PD	
39	GTX_CLK/TX_CLK	I/O	PD/O	RGMII TRANSMIT CLOCK: This continuous clock signal is sourced from the MAC layer to the PHY. Nominal frequency is 125 MHz in 1000-Mbps mode. This pin will be Input in RGMII mode. MII TRANSMIT CLOCK: In MII mode, this pin provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. This pin will be output in MII mode. This pin will be GTX_CLK by default and can be changed to TX_CLK by register configurations. Selection of the MII MAC interface also changes the GTX_CLK/TX_CLK selection without any additional register writes needed.
40	VDDIO_2	I	A	I/O Power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
41	VDD1P1_2	I	A	1.1-V Digital Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE[1]	DESCRIPTION
NO.	NAME			
42	RX_CLK	O	PD	RECEIVE CLOCK: Provides the recovered receive clocks for different modes of operation: 125 MHz in 1000-Mbps RGMII mode. 25 MHz in 100-Mbps RGMII/MII mode. 2.5 MHz in 10-Mbps RGMII/MII mode. When PHY is not linked, this pin provides 2.5-MHz clock for both RGMII/MII mode.
43	RX_ER	O	PD	MII Mode: In MII mode this pin will be configured as RX_ER. This pin is asserted high synchronously to rising edge of RX_CLK. Use of this pin is optional.
44	RX_D0	O	PD, S	RECEIVE DATA: Signal RX_D [3:0] carries data from the PHY to the MAC in RGMII mode and in MII mode. Symbols received on the cable are decoded and presented on these pins synchronous to RX_CLK. RX_D2 and RX_D3 should be pulled down by a 2.49-kΩ resistor.
45	RX_D1	O	PD, S	
46	RX_D2	O	PD	
47	RX_D3	O	PD	
48	TX_EN/TX_CTRL	I	PD	TX_EN: In MII mode, this pin will function as TX_EN. TRANSMIT CONTROL: In RGMII mode, TX_CTRL combines the transmit enable and the transmit error signal inputs from the MAC using both clock edges.
49	RX_DV/RX_CTRL	O	PD, S	RX_DV: In MII mode, this pin will function as RX_DV. RECEIVE CONTROL: In RGMII mode, the receive data available and receive error are combined (RXDV_ER) using both rising and falling edges of the receive clock (RX_CLK).
50	SMI_DISABLE	I	PD, S	0 = SMI (MDIO) writes are enabled. (Default) 1 = Station Management Interface (MDIO) writes are disabled.
51	VDD1P1_3	I	A	1.1-V Digital Supply (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
52	CLK_OUT	O	O	CLOCK OUTPUT: Output clock
53	MDIO	I/O	-	MANAGEMENT DATA I/O: Bidirectional management instruction/data signal that may be sourced by the management station or the PHY. This open-drain pin requires a 2.2- kΩ pullup resistor.
54	MDC	I	-	MANAGEMENT DATA CLOCK: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 24 MHz. There is no minimum clock rate.
55	INT_STTMCHNE_N	O	OD	STATE MACHINE INTERRUPT: This pin will be asserted low when an invalid state machine transition, condition, or other invalid condition is detected. When operating this pin as an open-drain interrupt, an external 2.2-kΩ resistor connected to the VDDIO supply is recommended.
56	INT_ECC_N	O	OD	ECC INTERRUPT:This pin will be asserted low when a configuration register error is detected or corrected by register ECC. When operating this pin as an open-drain interrupt, an external 2.2-kΩ resistor connected to the VDDIO supply is recommended.

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表 5-1. Pin Functions (continued)

PIN		I/O	TYPE[1]	DESCRIPTION
NO.	NAME			
57	INT_SUP_CUR_N	O	OD	SUPPLY CURRENT INTERRUPT: This pin will be asserted low when an abnormal supply current is detected during normal operation. When operating this pin as an open-drain interrupt, an external 2.2-kΩ resistor connected to the VDDIO supply is recommended.
58	VDDIO_3	I	A	I/O Power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
59	RESET_N	I	PU, S	RESET_N: This pin is an active-low reset input that initializes or re-initializes all the internal registers of the DP83561-SP. Asserting this pin low for at least 1 µs will force a reset process to occur.
60	PWDN_N/INT_N	I/O	PU	PWDN_N (Default): This is an Active Low Input. Asserting this signal low enables the power-down mode of operation. In this mode, the device powers down and consumes minimum power. Register access is available through the Management Interface to configure and power up the device. INT_N: The interrupt pin is an open-drain, active low output signal indicating an interrupt condition has occurred. Register access is required to determine which event caused the interrupt. TI recommends using an external 2.2-kΩ resistor connected to the VDDIO supply. When register access is disabled through pin option, the interrupt will be asserted for 500 ms before self-clearing.
61	LED_2/GPIO_0	O	S	LED_2: This pin is part of the VDDIO voltage domain. Default functionality is RX/TX activity General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
62	LED_1	O	S	LED_1: This pin is part of the VDDIO voltage domain. Default functionality is 1000BT link is up.
63	LED_0	O	S	LED_0: This pin is part of the VDDIO voltage domain. Default functionality is Link OK.
64	VDDA1P8_2	I	A	No external supply is required for this pin in two-supply mode. When unused, no connections should be made to these pins. In three-supply mode, an external 1.8-V (±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND. Refer to セクション 9 for more details.
DAP	DAP	-	GND	DIE ATTACH PAD, connect to GND[2]

(1) The functionality of the pins are defined below:
- Type I: Input
- Type O: Output
- Type I/O: Input /Output
- Type PD or PU: Internal Pull-down or Pull-up
- Type S: Strap Configuration Pin
- Type A: Analog pins

(2) The metal lid is internally grounded and attached to the DAP

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5.1 Pin States

表 5-2. Pin States-1

PIN		RESET		MII		RGMII	
NO.	NAME	PIN STATE	PULLS/HI-Z	PIN STATE	PULLS/HI-Z	PIN STATE	PULLS/HI-Z
28	JTAG_CLK	Input	PullUp	Input	PullUp	Input	PullUp
29	JTAG_TDO/GPIO_1	Input	PullDown	Output	Hi-Z	Output	Hi-Z
30	JTAG_TMS	Input	PullUp	Input	PullUp	Input	PullUp
31	JTAG_TDI	Input	PullUp	Input	PullUp	Input	PullUp
32	COL/GPIO_2	Input	Hi-Z	Output	Hi-Z	Output	Hi-Z
33	CRS/GPIO_3	Input	PullDown	Output	Hi-Z	Output	Hi-Z
34	AUTO_RECOVER	Input	PD	Input	PD	Input	PD
35	TX_D3	Input	PullDown	Input	PullDown	Input	PullDown
36	TX_D2	Input	PullDown	Input	PullDown	Input	PullDown
37	TX_D1	Input	PullDown	Input	PullDown	Input	PullDown
38	TX_D0	Input	PullDown	Input	PullDown	Input	PullDown
39	GTX_CLK/TX_CLK	Input	PullDown	Output	Hi-Z	Input	PullDown
42	RX_CLK	Input	PullDown	Output	Hi-Z	Output	Hi-Z
43	RX_ER	Input	Hi-Z	Output	Hi-Z	Output	Hi-Z
44	RX_D0	Input	PullDown	Output	Hi-Z	Output	Hi-Z
45	RX_D1	Input	PullDown	Output	Hi-Z	Output	Hi-Z
46	RX_D2	Input	PullDown	Output	Hi-Z	Output	Hi-Z
47	RX_D3	Input	PullDown	Output	Hi-Z	Output	Hi-Z
48	TX_EN/TX_CTRL	Input	PullDown	Input	PullDown	Input	PullDown
49	RX_DV/RX_CTRL	Input	PullDown	Output	Hi-Z	Output	Hi-Z
50	SMI_DISABLE	Input	PD	Input	PD	Input	PD
52	CLK_OUT	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
53	MDIO	Input	Hi-Z	Input/Output	Hi-Z	Input/Output	Hi-Z
54	MDC	Input	Hi-Z	Input	Hi-Z	Input	Hi-Z
55	INT_STTMCHNE_EN	HI-Z	PU	Output	OD-PU	Output	OD-PU
56	INT_ECC_N	HI-Z	PU	Output	OD-PU	Output	OD-PU
57	INT_SUP_CUR_N	HI-Z	PU	Output	OD-PU	Output	OD-PU
59	RESET_N	Input	PullUp	Input	PullUp	Input	PullUp
60	PWDN_N/INT_N	Input	PullUp	Input/Output	PullUp/OD-PU	Input/Output	PullUp/OD-PU
61	LED_2/GPIO_0	Input	PullDown	Input/Output	Hi-Z	Input/Output	Hi-Z
62	LED_1	Input	PullDown	Output	Hi-Z	Output	Hi-Z
63	LED_0	Input	PullDown	Output	Hi-Z	Output	Hi-Z

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表 5-3. Pin States-2

PIN		MII ISOLATE		IEEE POWER DOWN		DEEP POWER DOWN	
NO.	NAME	PIN STATE	PULLS/HI-Z	PIN STATE	PULLS/HI-Z	PIN STATE	PULLS/HI-Z
28	JTAG_CLK	Input	PullUp	Input/Ouput	PullUp	Input	PullUp
29	JTAG_TDO/GPIO_1	Output	Hi-Z	Output	HI-Z	Output	Hi-Z
30	JTAG_TMS	Input	PullUp	Input	PullUp	Input	PullUp
31	JTAG_TDI	Input	PullUp	Input	PullUp	Input	PullUp
32	COL/GPIO_2	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
33	CRS/GPIO_3	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
34	AUTO_RECOVER	Input	PD	Input	PD	Input	PD
35	TX_D3	Input	PullDown	Input	PullDown	Input	PullDown
36	TX_D2	Input	PullDown	Input	PullDown	Input	PullDown
37	TX_D1	Input	PullDown	Input	PullDown	Input	PullDown
38	TX_D0	Input	PullDown	Input	PullDown	Input	PullDown
39	GTX_CLK/TX_CLK	Input	Pull Down	Input	PullDown	Input	PullDown
42	RX_CLK	Input	PullDown	Output	Hi-Z	Output	Hi-Z
43	RX_ER	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
44	RX_D0	Input	PullDown	Output	Hi-Z	Output	Hi-Z
45	RX_D1	Input	PullDown	Output	Hi-Z	Output	Hi-Z
46	RX_D2	Input	PullDown	Output	Hi-Z	Output	Hi-Z
47	RX_D3	Input	PullDown	Output	Hi-Z	Output	Hi-Z
48	TX_EN/TX_CTRL	Input	PullDown	Input	PullDown	Input	PullDown
49	RX_DV/RX_CTRL	Input	PullDown	Output	Hi-Z	Output	Hi-Z
50	SMI_DISABLE	Input	PD	Input	PD	Input	PD
52	CLK_OUT	Output	Hi-Z	Output	HI-Z	Output	Hi-Z
53	MDIO	Input/Output	Hi-Z	Input	PullDown	Input	PullDown
54	MDC	Input	Hi-Z	Input	Hi-Z	Input	Hi-Z
55	INT_STTMCHNE_EN	Output	OD-PU	Output	OD-PU	Output	OD-PU
56	INT_ECC_N	Output	OD-PU	Output	OD-PU	Output	OD-PU
57	INT_SUP_CUR_N	Output	OD-PU	Output	OD-PU	Output	OD-PU
59	RESET_N	Input	PullUp	Input	PullDown	Input	PullDown
60	PWDN_N/INT_N	Input/Output	PullUp/OD-PU	Input/Output	PullUp/OD-PU	Input/Output	PullUp/OD-PU
61	LED_2/GPIO_0	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
62	LED_1	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z
63	LED_0	Output	Hi-Z	Output	Hi-Z	Output	Hi-Z

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Supply voltage	VDD1P1	-0.3	1.4	V
	VDD1P8	-0.3	2.16	V
	VDD2P5	-0.3	3	V
	VDDIO (3V3)	-0.3	4	V
	VDDIO (2V5)	-0.3	3	V
	VDDIO (1V8)	-0.3	2.1	V
Pins	MDI	-0.3	6.5	V
Pins	MAC Interface, MDIO, MDC, GPIO	-0.3	VDDIO + 0.3	V
Pins	INT/PWDN, RESET	-0.3	VDDIO + 0.3	V
Pins	JTAG	-0.3	VDDIO + 0.3	V
Storage temperature	Tstg	-60	150	C
Pins	XI Oscillator Input	-0.3	VDDIO+0.3	V

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

Parameter				VALUE	UNIT
$V_{(ESD)}$	V(ESD) Electrostatic discharge	Human-body model (HBM), perANSI/ESDA/JEDEC JS-001(1)	All pins except MDI	+/-2500	V
$V_{(ESD)}$	V(ESD) Electrostatic discharge	Human-body model (HBM), perANSI/ESDA/JEDEC JS-001(1)	MDI pins(2)	+/-8000	V
$V_{(ESD)}$	V(ESD) Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	All Pins	+/-1000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500 V HBM is possible with the necessary precautions. Pins listed as ±8 kV and/or ± 2 kV may actually have higherperformance.
(2) MDI Pins tested as per IEC 61000-4-2 standards.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 250 V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
VDDIO	Digital Supply Voltage, 1.8V operation	1.71	1.8	1.89	V
	Digital Supply Voltage, 2.5V operation	2.375	2.5	2.625	
	Digital Supply Voltage, 3.3V operation	3.145	3.3	3.465	
VDD1P1	Digital Supply	1.045	1.1	1.155	V
VDDA1P8	Analog Supply	1.71	1.8	1.89	V
VDDA2P5	Analog Supply	2.375	2.5	2.625	V
T_A	Operating Ambient Temperature	-55		125	℃

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6.4 Thermal Information

THERMAL METRIC(1)		64 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IEEE Tx CONFORMANCE (1000BaseT)						
	Output Differential Voltage	Normal Mode, All channels	0.67	0.745	0.82	V
IEEE Tx CONFORMANCE (100BaseTx)						
	Output Differential Voltage	Normal Mode, Channels A and B (2)	0.95	1.00	1.05	V
IEEE Tx CONFORMANCE (10BaseTe)						
	Output Differential Voltage			1.75		V

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION Copper mode (100m cable)						
I(1V1)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		215		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		115		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		100		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		120		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		90		mA
I(1V8)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		60		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		25		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		15		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		25		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		15		mA
I(2V5)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		90		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		50		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		76		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		50		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		85		mA
I(VDDIO =3.3V)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		80		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		45		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		35		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		50		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		35		mA
I(VDDIO =1.8V)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		35		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		20		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		15		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		16		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		11		mA

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I(VDDIO =2.5V)	RGMII to Copper (1G)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		50		mA
	RGMII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		27		mA
	RGMII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		20		mA
	MII to Copper (100M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		26		mA
	MII to Copper (10M)	Traffic: 100%, Packet Size: 1512, Content: Random, VT range		17		mA
POWER CONSUMPTION Low power modes						
I(1V1)	IEEE Power Down			90		mA
	Active Sleep			110		mA
	RESET			95		mA
I(1V8)	IEEE Power Down			1		mA
	Active Sleep			10		mA
	RESET			1		mA
I(2V5)	IEEE Power Down			5		mA
	Active Sleep			30		mA
	RESET			5		mA
I(VDDIO =3.3)	IEEE Power Down			20		mA
	Active Sleep			20		mA
	RESET			20		mA
Monitors						
Temperature Sensor	Temperature Sensor Range	-55ºC to 125ºC	-55		125C	℃
	Temperature Sensor Resolution (LSB)	-55ºC to 125ºC			9	℃
	Temperature Sensor Accuracy (Voltage and Temperature Variation on single part)	-55ºC to 125ºC			9.5	℃
	Temperature Sensor Accuracy Part-to-Part (Voltage, Temperature and part to part variation)	-55ºC to 125ºC			12	℃
BOOTSTRAP DC CHARACTERISTICS (4 Level) (PHY address pins)						
V_{MODE0}	Mode 0 Strap Voltage Range		0		0.093 x VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range		0.136 x VDDIO		0.184 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range		0.219 x VDDIO		0.280 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range		0.6 x VDDIO		0.888 x VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE0}	Mode 0 Strap Voltage Range		0		0.18 x VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range		0.5 x VDDIO		0.88 x VDDIO	V

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6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)(1) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IO CHARACTERISTICS (DC Specifications)						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±5%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±5%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±5%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±5%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±5%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±5%	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ±5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±5%	0.65*VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±5%			0.35*VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±5%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±5%			0.45	V
I_{IH}	Input High Current	Input High Current	-55		55	µA
I_{IL}	Input Low Current	T_A = -55℃ to 125℃, VIN=GND	-35		35	µA
Iozh	Tri-state Output High Current	T_A = -55℃ to 125℃, VOUT=VDDIO	-55		55	µA
Iozl	Tri-state Output Low Current	T_A = -55℃ to 125℃, VOUT=GND	-35		35	µA
R_{pulldn}	Internal Pull Down Resistor		6.75	9	13.5	kΩ
R_{pullup}	Internal Pull Up Resistor		6	10	14	kΩ
XI V_{IH}	High Level Input Voltage		1.2		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.6	V
C_{IN}	Input Capacitance XI			1.5		pF
C_{IN}	Input Capacitance INPUT PINS			5.5		pF
C_{OUT}	Output Capacitance XO			1.5		pF
C_{OUT}	Output Capacitance OUTPUT PINS			5.5		pF
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK		50		Ω

(1) Power Dissipation Measurements :Traffic : 100%, Packet Size: 1512, Random Content, Temp : -55 to 125C, Voltage Range : +/-5%
(2) In Mirror Mode, Channel D & C are used for Tx and Rx. Please refer to Mirror Mode section for additonal configuration for Output Differential Voltage
(3) For RGMII interface, please refer to section "Reduced GMII" forRGMII timing and IBIS model based Signal Integrity simulation guidelines

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6.6 Timing Requirements

(1)

PARAMETER		MIN	NOM	MAX	UNIT
POWER-UP TIMING (2, 3 supply mode)					
	Supply ramp rate: For all supplies	0.5		100	ms
	Supply delay offset between fully ramped (2V5, 1V1) and (VDDIO, 1V8) (3)	0		50	ms
T1	Last Supply power rail ramp to RESET_N	200			ms
T2	Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access		200		ms
T3	Powerup to Strap latchin: Hardware configuration pins transition to output drivers		200		ms
	Powerup to FLP		2000		ms
RESET TIMING					
T1	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access	30			us
T3	RESET PULSE Width: Miminum Reset pulse width to be able to reset	720			ns
T4	Reset to FLP		1750		ms
T4	Reset to 100M signaling (strapped mode)		194		us
T4	Reset to MAC clock		195		us
COPPER LINK TIMING					
T1	Loss of Idles to Link LED low in Fast link down mode (100M)		10		us
	Loss of Idles to Link LED low in Fast link down mode (1000M)		10		us
MII 100M TIMING					
T1	TX_CLK High / Low Time	16	20	24	ns
T2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	10			ns
T3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
T1	RX_CLK High / Low Time	16	20	24	ns
T2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	10		30	ns
MII 10M Timings					
10M	TX_CLK High / Low Time	190	200	210	ns
	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	25			ns
	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
	RX_CLK High / Low Time	160	200	240	ns
	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	100		300	ns
RGMII OUTPUT TIMING (1G)					
T_{skewT}	Data to Clock Output Skew (Non-Delay Mode)(2)	-600		625	ps
$T_{skewT(Delay)}$	Data to Clock Output Skew (Delay Mode : 2 ns default)	1.5	2	2.5	ns
T_{setupT}	Data to Clock Output Setup (Delay Mode)	1.2			ns
T_{holdT}	Data to Clock Output Hold (Delay Mode)	1.2			ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
	Duty Cycle	45	50	58	%
	Rise / Fall Time (20% to 80%) : with 5 pF Capacitive load			0.85	ns
RGMII INPUT TIMING (1G)					
T_{setupR}	TX data to clock input setup	1			ns
T_{holdR}	TX clock to data input hold	1			ns
	DLL delay TX Input step		250		ps
SMI TIMING					

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6.6 Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
T1	MDC to MDIO (Output) Delay Time (25 pF Load)	0		20	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency (25 pF Load)		2.5	24	MHz

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6.6 Timing Requirements (continued)

(1)

PARAMETER		MIN	NOM	MAX	UNIT
OUTPUT CLOCK TIMING (25MHz clockout)					
	Frequency (PPM)	-100		100	-
	Duty Cycle	40		60	%
	Rise Time (5 pF Load)		5000		ps
	Fall Time (5 pF Load)		5000		ps
	Jitter (RMS)			40	ps
	Jitter (Long Term)		375		ps
25MHz INPUT CLOCK tolerance					
	Frequency Tolerance	-100		+100	ppm
	Rise / Fall Time (10%-90%)			8	ns
	Jitter Tolerance (Accumulated)		75		ps
	Duty Cycle	40		60	%
TRANSMIT LATENCY TIMING					
Copper	RGMII to Cu (10M) : Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		2560		ns
Copper	MII to Cu (10M): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI		525		ns
Copper	RGMII to Cu (100M): Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		169		ns
Copper	MII to Cu (100M): Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI		64		ns
Copper	RGMII to Cu (1G): Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		106		ns
RECEIVE LATENCY TIMING					
Copper	Cu to RGMII (10M): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_CTRL		3000		ns
Copper	Cu to MII (10M): SSD symbol on MDI to Rising edge of RX_CLK with assertion of RX_DV		1650		ns
Copper	Cu to RGMII (100M): SSD symbol on MDI to a) Rising edge of RX_DV with assertion of RX_CTRL b) Rising edge of RX_DV with assertion of RX_Dx		192		ns
Copper	Cu to MII (100M): SSD symbol on MDI to a) Rising edge of RX_DV with assertion of RX_CTRL b) Rising edge of RX_DV with assertion of RX_Dx		220		ns
Copper	Cu to RGMII (1G): SSD symbol on MDI to a) Rising edge of RX_DV with assertion of RX_CTRL b) Rising edge of RX_DV with assertion of RX_Dx		278		ns

(1) MII and RGMII Timing, Output Clock Timing, Input Clock jitter tolerance, Input Clock rise/fall time are characteristed by Design Simulation
(2) For RGMII interface, please refer to section "Reduced GMII" forRGMII timing and IBIS model based Signal Integrity simulation guidelines
(3) Ramp of all 4 supplies (2V5, 1V1, VDDIO, 1V8) together is preferred. VDDIO and 1V8 (3 supply config) can be delayed if needed. Refer to section "Power Supply recomendation"

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6.6.1 Timing Requirement Diagrams

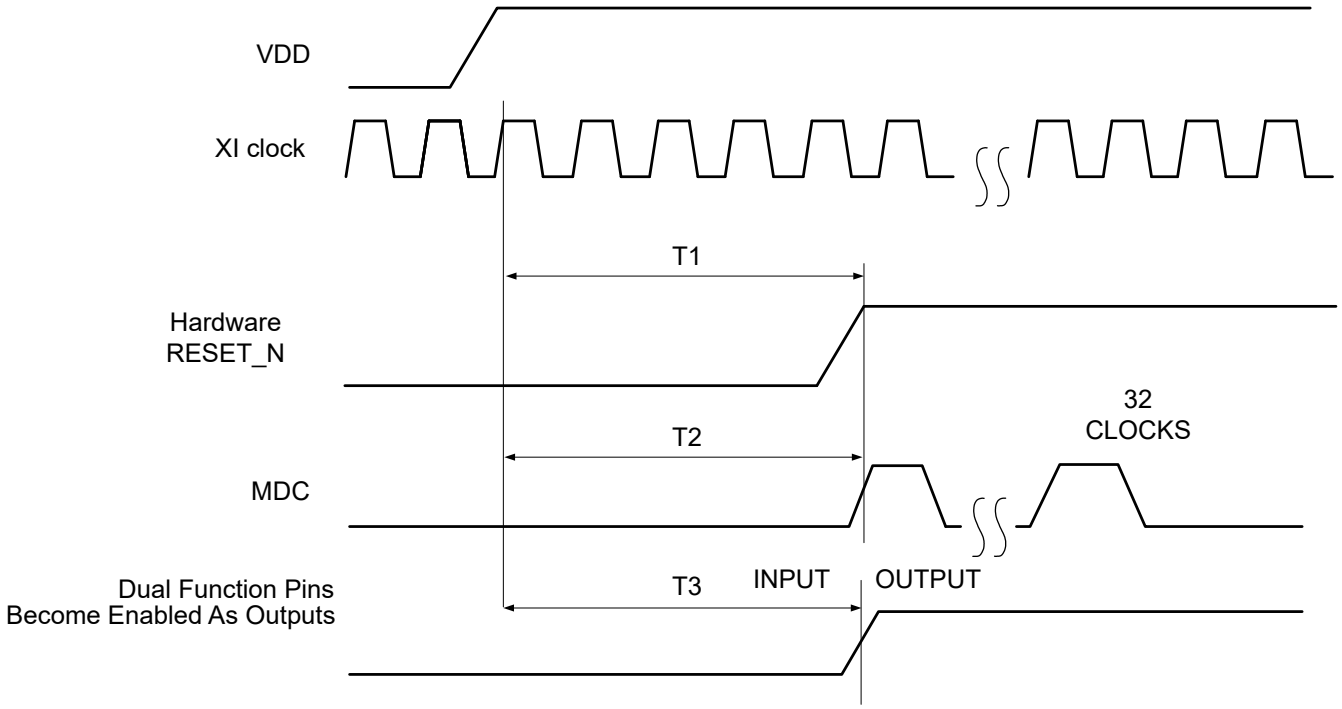


図 6-1. Power-Up Timing

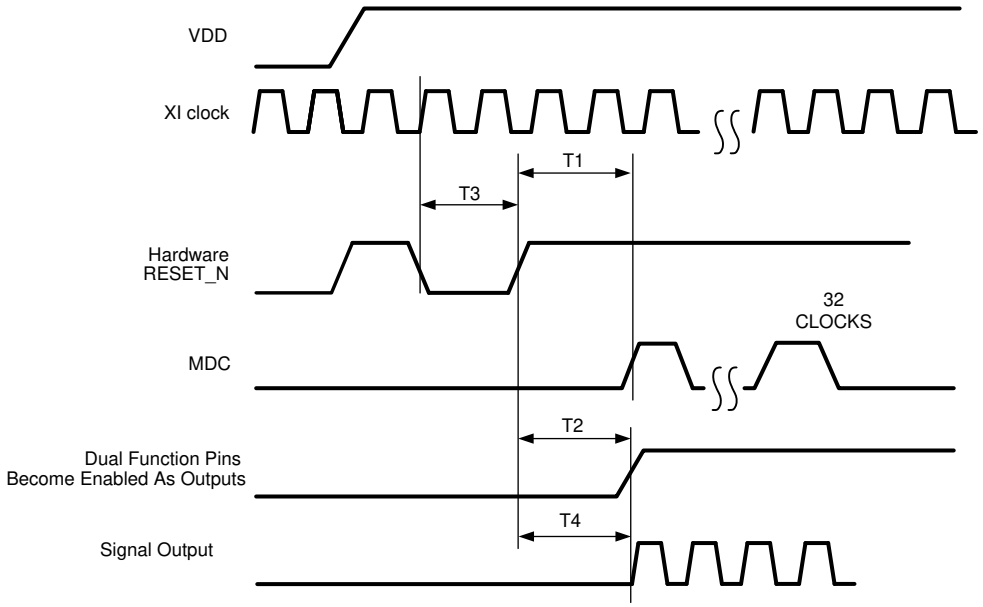


図 6-2. Reset Timing

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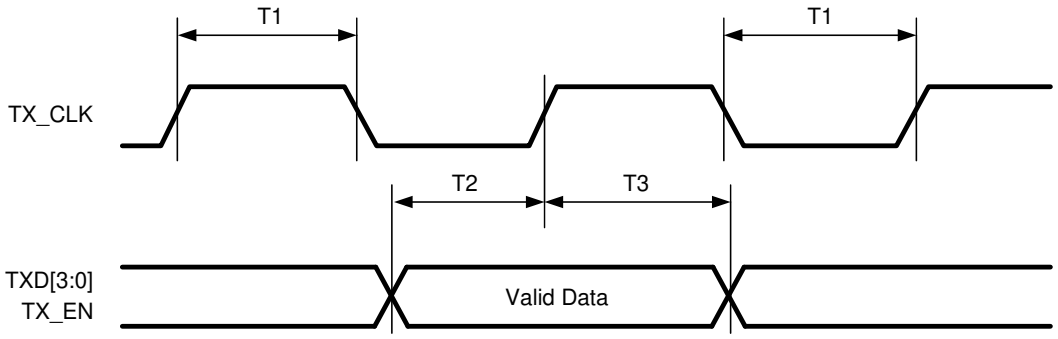


図 6-3. 100-Mbps MII Transmit Timing

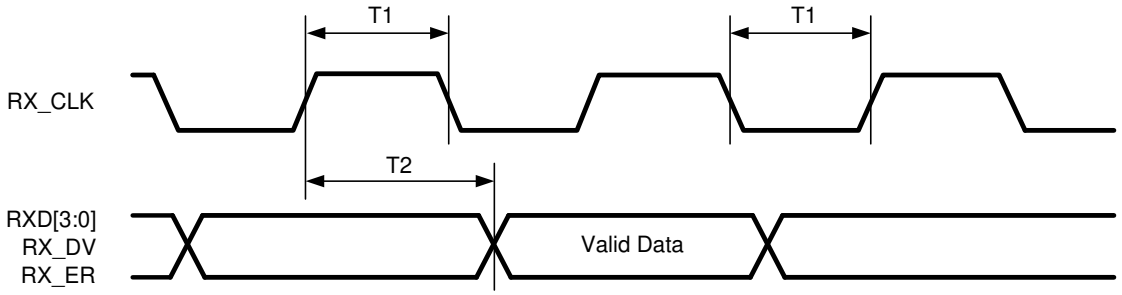


図 6-4. 100-Mbps MII Receive Timing

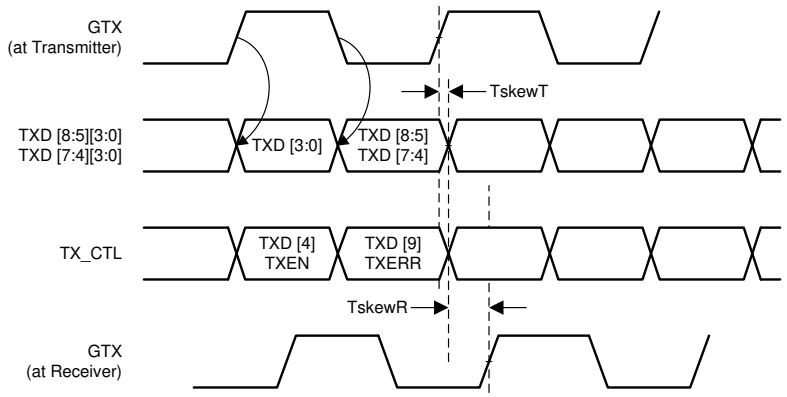


図 6-5. RGMII Transmit Multiplexing and Timing Diagram

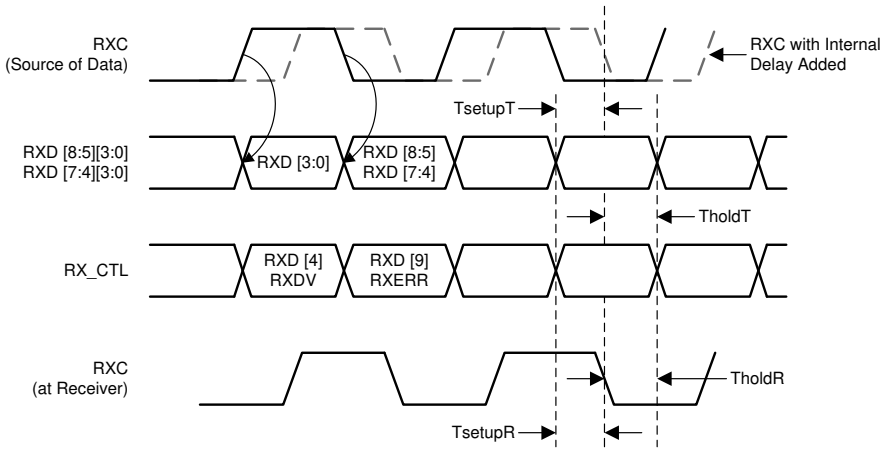


図 6-6. RGMII Receive Multiplexing and Timing Diagram

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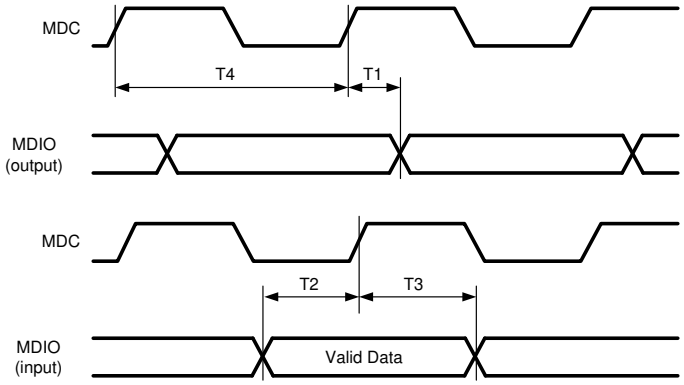


図 6-7. Serial Management Interface Timing

6.7 Typical Characteristics

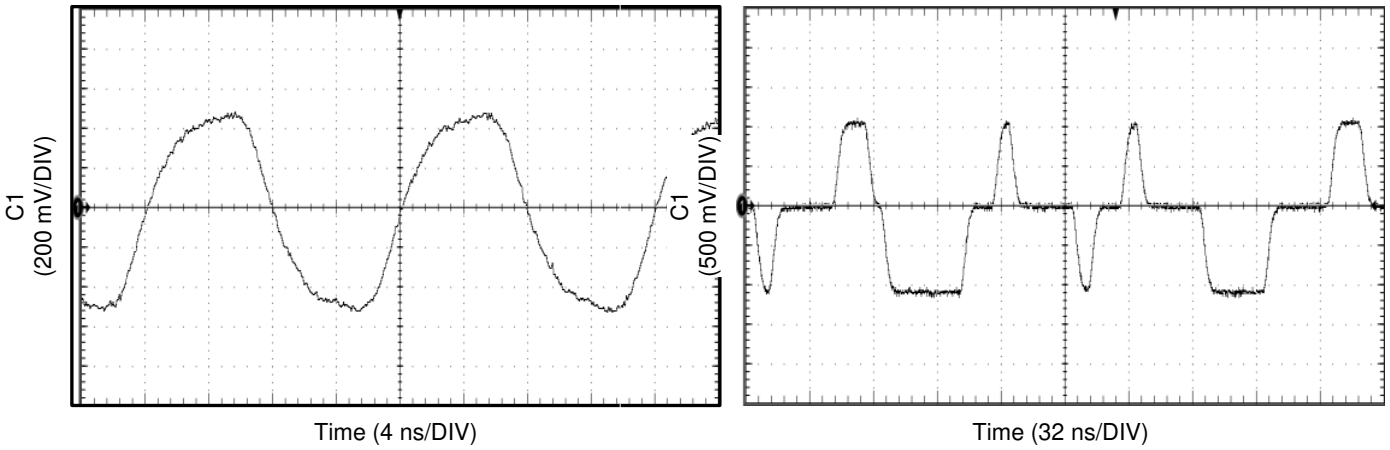


図 6-8. 1000Base-T Test Mode 2 Signal

図 6-9. 100Base-TX Signal

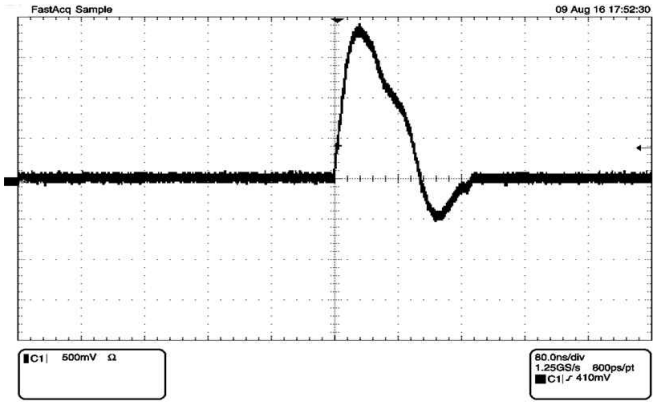


図 6-10. 10Base-Te Link Pulse

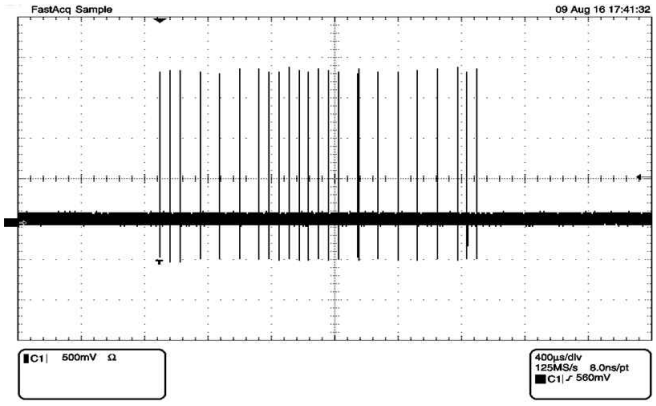


図 6-11. Auto-Negotiation FLP

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7 Detailed Description

7.1 Overview

The DP83561-SP offers SEL immunity up to LET = 121MeV·cm^2/mg, 300 krad(Si) TID (Total Ionizing Dose) and ambient temperature rating from –55°C to 125°C. The DP83561-SP is a fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. The DP83561-SP also features a SEFI (Single Event Functional Interrupt) monitoring suite, alerting the system that a SEFI has occurred. SEFI monitoring takes care of both Control and Data path of the PHY. Control path monitors included are IEEE PCS state machine monitors and configuration register monitors. There is an internal auto recovery mechanism (configurable) that gets trigger when one of the two previously mentioned monitors detect issues. The auto recovery mechanism is a soft reset generated by the PHY for itself. Data path is monitored using PLL lock monitor and temperature monitor. The DP83561-SP can also be configured (optional) to automatically reset the logic core to provide SEFI protection. It also has configurable option to disable SMI (serial management interface) to block any unwanted configuration changes from host MAC.

The DP83561-SP interfaces directly to twisted pair media through an external transformer. This device interfaces directly to the MAC layer through Reduced GMII (RGMII) and MII.

The DP83561-SP provides precision clock synchronization, including a synchronous Ethernet clock output. It has low jitter, low latency, and provides IEEE 1588 Start of Frame Detection.

7.1.1 Engineering Model (Parts With /EM Suffix)

Engineering evaluation or engineering model (/EM) devices are available for order and are identified by the "/EM" in the orderable device name (see the Ordering Information table on the front page of the datasheet). These devices meet the performance specifications of the datasheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

For a comparison of the QMLV and Engineering Model production flows, see TI Engineering Evaluation Units vs. MIL-PRF-38535 QML Class V Processing (SLYB235).

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7.2 Functional Block Diagram

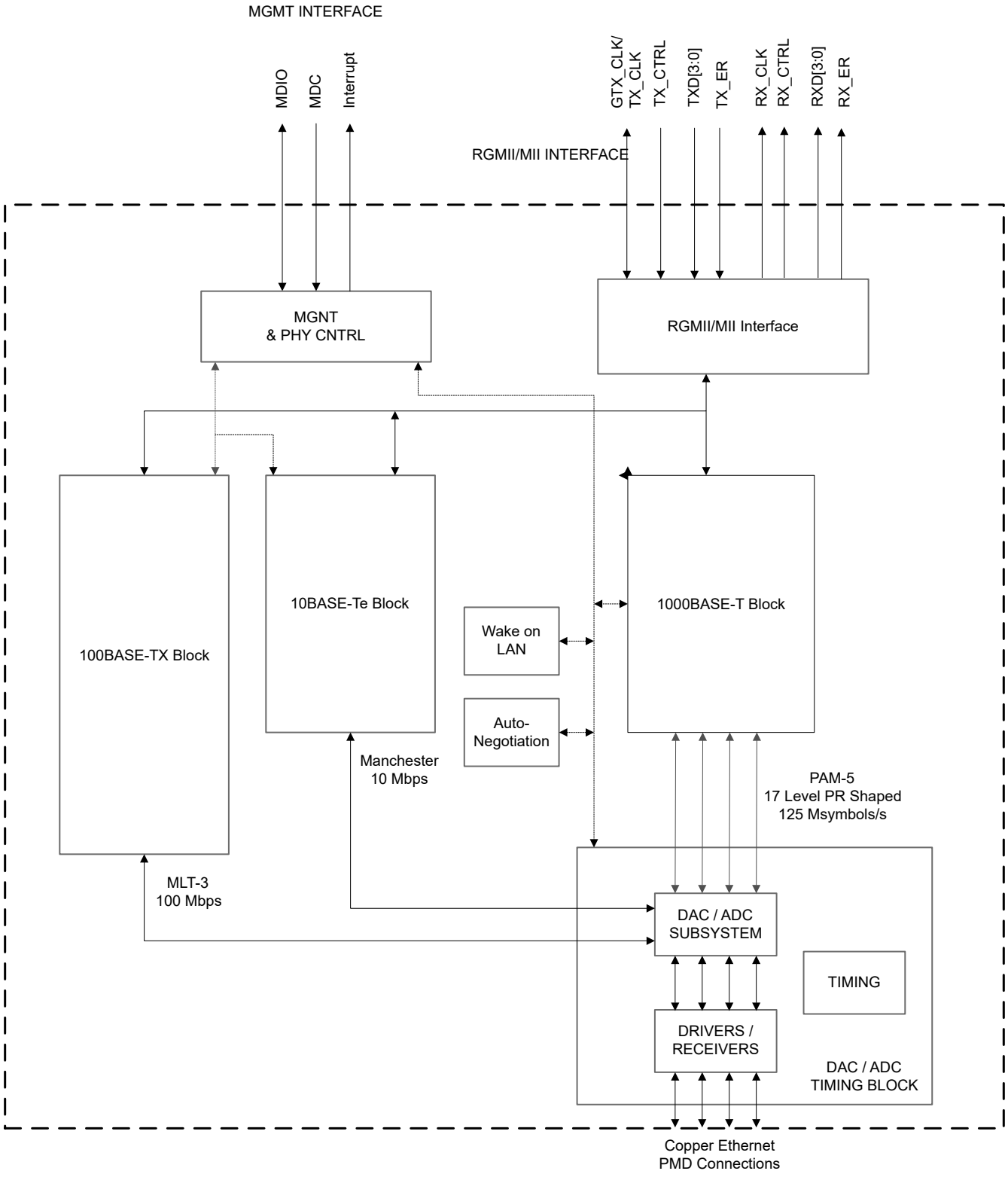


図 7-1. DP83561-SP Functional Block Diagram

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7.3 Feature Description

7.3.1 Copper Ethernet

7.3.1.1 1000BASE-T

The DP83561-SP supports the 1000BASE-T standard as defined by the IEEE 802.3 standard. In 1000M mode, the PHY will use four MDI channels for communication. The 1000BASE-T can work in Auto-Negotiation mode. The PHY can be configured in 1000BASE-T through the register settings or strap settings.

7.3.1.2 100BASE-TX

The DP83561-SP supports the 100BASE-TX standard as defined by the IEEE 802.3 standard. In 100M mode, the PHY will use two MDI channels for communication. The 100BASE-TX can work in Auto-Negotiation mode or in force mode. The PHY can be configured in 100BASE-TX through the register settings or strap settings. When using DP83561-SP in force 100Base-TX mode, it is required to enable Robust Auto-MDIX feature from register 0x1E.

7.3.1.3 10BASE-Te

The DP83561-SP supports the 10BASE-Te standard as defined by the IEEE 802.3 standard. In 100M mode, the PHY will use two MDI channels for communication. The 10BASE-Te can work in Auto-Negotiation mode or in force mode. The PHY can be configured in 10BASE-Te through the register settings or strap settings.

7.3.2 MAC Interfaces

The DP83561-SP supports connection to an Ethernet MAC through MII or RGMII.

7.3.2.1 Reduced GMII (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII relative to 24 pins for GMII). To accomplish this goal, the data paths and all associated control signals are reduced and are multiplexed. Both rising and trailing edges of the clock are used. For Gigabit operation the GTX_CLK and RX_CLK clocks are 125 MHz, and for 10- and 100-Mbps operation, the clock frequencies are 2.5 MHz and 25 MHz, respectively.

The following register writes are needed at initialization for proper operation:

- Write 0x0170 to value 0x0C1F

For more information about RGMII timing, see the *RGMII Interface Timing Budgets* application report (SNLA243).

RGMII MAC Interface for Gigabit Ethernet has stringent timing requirements to meet system level performance. To meet these timing requirements and to operate with different MACs over RGMII, it is advised to take the following requirements into consideration when designing PCB. It is also recommended to check board level signal integrity by using the DP83TG720 IBIS model.

7.3.2.1.1 RGMII-TX Requirements

- RGMII TX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- 図 7-2 shows a RGMII interface requirements for TX* signals. MAC RGMII driver output impedance should be 50 Ohm+/-20%.
- Skew for all RGMII TX signals at TP2, in 図 7-2, should be <±500ps.
- Signal Integrity at TP1 and TP2, in 図 7-2, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP2, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP2.

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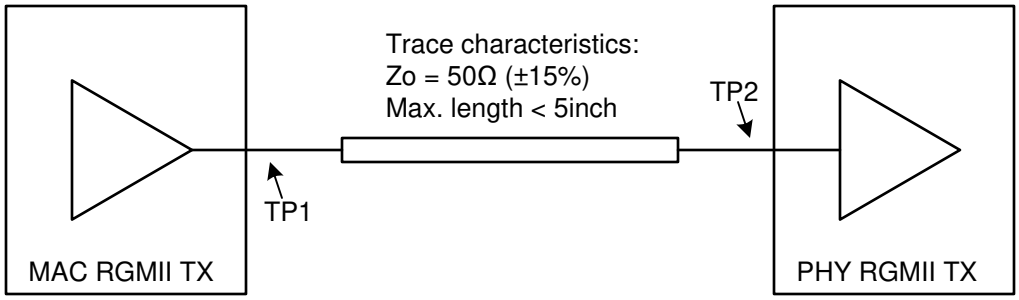


図 7-2. RGMII TX Requirements

7.3.2.1.2 RGMII-RX Requirements

- RGMII RX signals should be routed on board with control impedance of 50Ohm +/-15%.
- Max routing length should be limited to 5inch for better signal integrity performance.
- No damping resistors should be added at TP3/TP4, in 図 7-3, as that will impact signal integrity of RX signals.
- 図 7-3 shows a RGMII interface requirements for RX* signals. MAC RGMII driver output impedance should be 50Ohm+/-20%.
- Signal Integrity at TP3 and TP4, in 図 7-3, should be verified with IBIS model simulation and ensured conformance to following requirements:
  - At TP4, signal should meet rise/fall time of 1ns (20-80%) of signal amplitude.
  - Rise/fall time should be monotonic between VIH/VIL level at TP4.

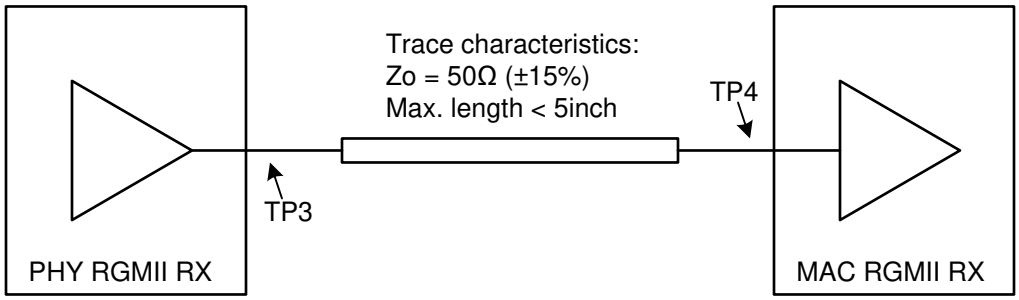


図 7-3. RGMII RX Requirements

Note

1. We recommend routing RGMII on buried traces to minimize EMC emissions.
2. Buried traces should be connected with via placement as close as possible to the PHY and MAC.

7.3.2.1.3 1000-Mbps Mode Operation

All RGMII signals are positive logic. The 8-bit data is multiplexed by taking advantage of both clock edges. The lower 4 bits are latched on the positive clock edge and the upper 4 bits are latched on trailing clock edge. The control signals are multiplexed into a single clock cycle using the same technique.

To reduce power consumption of RGMII interface, TXEN_ER and RXDV_ER are encoded in a manner that minimizes transitions during normal network operation. This is done by following encoding method. Note that the value of GMII_TX_ER and GMII_TX_EN are valid at the rising edge of the clock. In RGMII mode, GMII_TX_ER is presented on TX_CTRL at the falling edge of the GTX_CLK clock. RX_CTRL coding is implemented the same fashion.

$$TX_ERR = GMII_TX_ER \text{ (XOR) } GMII_TX_EN \quad (1)$$

where

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- GMII_TX_ER and GMII_TX_EN are logical equivalent signals in GMII standard.

$$RX_ERR = GMII_RX_ER \text{ (XOR) } GMII_RX_DV \quad (2)$$

where

- GMII_RX_ER, and GMII_RX_DV are logical equivalent signals in GMII standard.

When receiving a valid frame with no error, *RX_CTRL = True* is generated as a logic high on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic high at the falling edge of RX_CLK. When no frame is being received, *RX_CTRL = False* is generated as a logic low on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic low on the falling edge of RX_CLK.

TX_CTRL is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of GTX_CLK and during the period between frames where no error is indicated, the signal stays low for both edges.

7.3.2.1.4 1000-Mbps Mode Timing

The DP83561-SP provides configurable clock skew for the GTX_CLK and RX_CLK to optimize timing across the interface. The transmit and receive paths can be optimized independently. Both the transmit and receive path support 16 programmable RGMII delay modes through register configuration.

The timing paths can either be configured for Aligned mode or Shift mode. In Aligned mode, no clock skew is introduced. In Shift mode, the clock skew can be introduced in 0.25 ns increments (through register configuration). Configuration of the Aligned mode or Shift mode is accomplished through the RGMII Control Register (RGMIICTL), address 0x0032. In Shift mode, the clock skew can be adjusted using the RGMII Delay Control Register (RGMIIDCTL), address 0x0086.

7.3.2.1.5 10- and 100-Mbps Mode

When the RGMII interface is operating in the 100-Mbps mode, the Ethernet Media Independent Interface (MII) is implemented by reducing the clock rate to 25 MHz. For 10-Mbps operation, the clock is further reduced to 2.5 MHz. In the RGMII 10/100 mode, the transmit clock RGMII TX_CLK is generated by the MAC and the receive clock RGMII RX_CLK is generated by the PHY. During the packet receiving operation, the RGMII RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free-running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitch is allowed on the clock signals during clock speed transitions.

This interface operates at 10- and 100-Mbps speeds the same way it does at 1000-Mbps mode with the exception that the data may be duplicated on the falling edge of the appropriate clock.

The MAC holds the RGMII TX_CLK low until it has ensured that it is operating at the same speed as the PHY.

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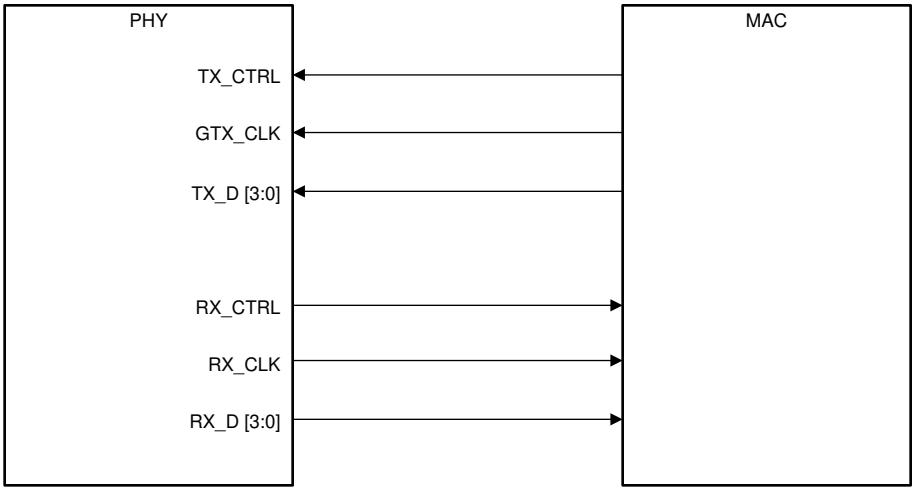


図 7-4. RGMII Connections

7.3.2.2 Media Independent Interface (MII)

DP83561-SP also supports MII mode when the PHY is working in 100M and 10M speeds. The user will have to ensure that the PHY links in either 100-Mbps or 10-Mbps mode. MII mode cannot be used in 1000-Mbps mode. When using auto-negotiation to resolve MDI speed, TI recommends to turn off the gigabit speed advertisement through register 0x9 to ensure that the PHY does not link up at 1000-Mbps speed. The Media Independent Interface is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100BASE-TX and 10BASE-Te modes. The MII is fully compliant with IEEE 802.3-2002 clause 22.

When using the PHY in 10/100M MII Auto-negotiation mode, it is required to disable 1G advertisement by writing register 0x9 = 0x0.

The MII signals are summarized in 表 7-1:

表 7-1. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN, TX_ER
	RX_DV, RX_ER

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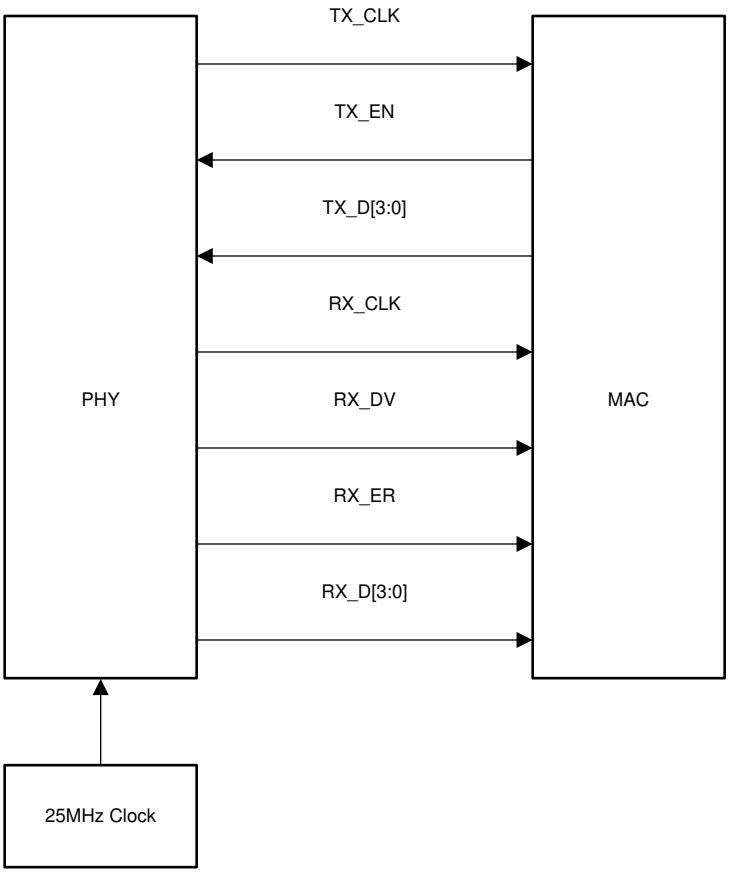


図 7-5. MII Signaling

7.3.3 Auto-Negotiation

All 1000BASE-T PHYs are required to support Auto-Negotiation. The Auto-Negotiation function in 1000BASE-T has three primary purposes:

- Auto-Negotiation of Speed and Duplex Selection
- Auto-Negotiation of Master or Slave Resolution
- Auto-Negotiation of Pause or Asymmetrical Pause Resolution

7.3.3.1 Speed and Duplex Selection - Priority Resolution

The Auto-Negotiation function provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the signaling used to communicate the abilities between two devices at each end of a link segment. For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification. The DP83561-SP supports 1000BASE-T, 100BASE-TX, and 10BASE-Te modes of operation. The process of Auto-Negotiation ensures that the highest performance protocol is selected (that is, priority resolution) based on the advertised abilities of the Link Partner and the local device.

7.3.3.2 Master and Slave Resolution

If 1000BASE-T mode is selected during the priority resolution, the second goal of Auto-Negotiation is to resolve Master or Slave configuration. The Master mode priority is given to the device that supports multiport nodes, such as switches and repeaters. Single node devices such as a DTE or NIC card takes lower Master mode priority.

7.3.3.3 Pause and Asymmetrical Pause Resolution

When Full-Duplex operation is selected during priority resolution, the Auto-Negotiation also determines the Flow Control capabilities of the two link partners. Flow control was originally introduced to force a busy station's Link Partner to stop transmitting data in Full-Duplex operation. Unlike Half-Duplex mode of operation where a link partner could be forced to back off by simply generating collisions, the Full-Duplex operation needed a mechanism to slow down transmission from a link partner in the event that the receiving station's buffers are becoming full. A new MAC control layer was added to handle the generation and reception of Pause Frames. Each MAC Controller has to advertise whether it is capable of processing Pause Frames. In addition, the MAC Controller advertises if Pause frames can be handled in both directions, that is, receive and transmit. If the MAC Controller only generates Pause frames but does not respond to Pause frames generated by a link partner, it is called Asymmetrical Pause. The advertisement of Pause and Asymmetrical Pause capabilities is enabled by writing 1 to bits 10 and 11 of ANAR (register address 0x0004). The link partner's Pause capabilities is stored in ANLPAR (register address 0x0005) bits 10 and 11. The MAC Controller has to read from ANLPAR to determine which Pause mode to operate. The PHY layer is not involved in Pause resolution other than simply advertising and reporting of Pause capabilities.

7.3.3.4 Next Page Support

The DP83561-SP supports the Auto-Negotiation Next Page protocol as required by IEEE 802.3 clause 28.2.4.1.7. The ANNPTR 0x07 allows for the configuration and transmission of the Next Page. Refer to clause 28 of the IEEE 802.3 standard for detailed information regarding the Auto-Negotiation Next Page function.

7.3.3.5 Parallel Detection

The DP83561-SP supports the Parallel Detection function as defined in the IEEE 802.3 specification. Parallel Detection requires the 10/100-Mbps receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 10BASE-Te or 100BASE-X PMA recognize as valid link signals.

If the DP83561-SP completes Auto-Negotiation as a result of Parallel Detection, without Next Page operation, bits 5 and 7 of ANLPAR (register address 0x0005) are set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR are also set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that the negotiation is completed through Parallel Detection by reading 0 in bit 0 of ANER (register address 0x0006) after Auto-Negotiation Complete, bit 5 of

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BMSR (register address 0x0001), is set. If the PHY is configured for parallel detect mode and any condition other than a good link occurs, the parallel detect fault, bit 4 of ANER (register address 0x0006), sets.

7.3.3.6 Restart Auto-Negotiation

If a link is established by successful Auto-Negotiation and then lost, the Auto-Negotiation process resumes to determine the configuration for the link. This function ensures that a link can be re-established if the cable becomes disconnected and reconnected. After Auto-Negotiation is completed, it may be restarted at any time by writing 1 to bit[9] of the BMCR (register address 0x0000). A restart Auto-Negotiation request from any entity, such as a management agent, causes DP83561-SP to halt data transmission or link pulse activity until the break_link_timer expires. Consequently, the Link Partner goes into link fail mode and the resume Auto-Negotiation. The DP83561-SP resumes Auto-Negotiation after the break_link_timer has expired by transmitting FLP (Fast Link Pulse) bursts.

7.3.3.7 Enabling Auto-Negotiation Through Software

If Auto-Negotiation is disabled by MDIO access, and the user desires to restart Auto-Negotiation, this could be accomplished by software access. Bit 12 of BMCR (register address 0x00) should be cleared and then set for Auto-Negotiation operation to take place.

If Auto-Negotiation is disabled by strap option, Auto-Negotiation can not be reenabled.

7.3.3.8 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation typically take 2-3 seconds to complete. In addition, Auto-Negotiation with next page exchange takes approximately 2-3 seconds to complete, depending on the number of next pages exchanged. Refer to Clause 28 of the IEEE 802.3 standard for a full description of the individual timers related to Auto-Negotiation.

7.3.3.9 Auto-MDIX Resolution

The DP83561-SP can determine if a *straight* or *crossover* cable is used to connect to the link partner. It can automatically re-assign channel A and B to establish link with the link partner, (and channel C and D in 1000BASE-T mode). Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX.

Auto-MDIX can be enabled or disabled by strap, using the AMDIX Disable strap, or by register configuration, using bit 6 of the PHYCR register (address 0x0010). When Auto-MDIX is disabled, the PMA is forced to either MDI (*straight*) or MDIX (*crossed*). Manual configuration of MDI or MDIX can also be accomplished by strap, using the Force MDI/X strap, or by register configuration, using bit 5 of the PHYCR register.

For 10/100, Auto-MDIX is independent of Auto-Negotiation. Auto-MDIX works in both Auto-Negotiation mode and manual forced speed mode.

7.3.4 Speed Optimization

Speed optimization, also known as link downshift, enables fallback to 100M operation after multiple consecutive failed attempts at Gigabit link establishment. Such a case could occur if cabling with only four wires (two twisted pairs) were connected instead of the standard cabling with eight wires (four twisted pairs).

The number of failed link attempts before falling back to 100M operation is configurable. By default, four failed link attempts are required before falling back to 100M.

Speed optimization also supports fallback to 10M if link establishment fails in Gigabit and in 100M mode.

Speed optimization can be enabled through register configuration.

7.3.5 Radiation Performance

7.3.5.1 Total Ionizing Dose (TID)

DP83561-SP is a Radiation-Hardness-Assured (RHA) QML Class V (QMLV) product, and has a Total Ionizing Dose (TID) level at 300 krad(Si). Testing and qualification of DP83561-SP is done on a wafer level according to

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MIL-STD-883, Test Method 1019. Radiation Lot Acceptance Testing (RLAT) is performed at the 300 krad(Si) TID level.

Group E (TID) Radiation Lot Acceptance (RLAT) data is available with lot shipments as part of the QCI Summary Reports, for information on finding QCI Summary Reports see QML Flow, Its Importance, and Obtaining Lot Information (SBOA143).

7.3.5.2 Single-Event Effects (SEE)

One time Single-Event Effects characterization was performed according to EIA/JEDEC Standard, EIA/JEDEC57 to linear energy transfer (LET) = 85MeV·cm^2/mg, during the testing no Single-Event Latch-up (SEL) was observed, characterisation is published in radiataion test report.

7.3.5.3 Single Event Functional Interrupt (SEFI) Monitor Suite

With deployment of Ethernet devices to space systems, the need for PHYs to be radiation hardened by design for high performance and reliability is becoming more important. The myriad of problems that could occur due to SEU and SEFI results in the need to properly detect, act upon, and correct any faults. The DP83561-SP offers a suite of monitors to detect SEFI events occurring in system critical areas of the device and to correct faults caused by them.

7.3.5.3.1 PCS State Machine Monitors

The DP83561-SP SEFI support functionality will monitor internal IEEE PCS states.

If any invalid state changes are made, the DP83561-SP will indicate a SEFI has occurred and raise a signal on pin INT_STTMCHNE_N (pin 55). Refer to register 0x1D8 bits[11:0] for status.

When the AUTO_RECOVER bit is set, an internal state error will cause the DP83561-SP to assert an internal reset signal. The INT_STTMCHNE_N signal will be asserted regardless of AUTO_RECOVER setting. Interrupt on INT_STTMCHNE_N pin can be masked using bits[1:0] in register 0x1D8.

7.3.5.3.2 Configuration Register Monitors

The DP83561-SP implements an ECC scheme for the configuration registers to detect SEFI events. If any change in the configuration registers are detected or corrected by the ECC, an interrupt will be raised for indication to the higher level system. Status is indicated by the PHY on register 0x01D8 bits[15:12]. To enable ECC, refer to register 0x1EE bits[9:7].

During POR, or on the rising edge of SMI_DISABLE signal, the DP83561-SP will calculate a checksum of the bits in all configuration registers sequentially by address. The resulting checksum will then be stored in SEFI immune memory as value CHECKSUM_VALUE.

While SMI_DISABLE signal remains asserted, the DP83561-SP will continuously calculate the checksum for all configuration registers, kept as CHECKSUM_CHK. If CHECKSUM_VALUE and CHECKSUM_CHK ever differ, the INT_ECC_N signal will be asserted.

When SMI_DISABLE signal is deasserted, the CHECKSUM_VALUE will be cleared and the checksum function will not be performed on the configuration registers.

When the AUTO_RECOVER bit is set, the configuration registers will be reset to default values including the currently selected pin options. The INT_ECC_N signal will be asserted regardless of AUTO_RECOVER setting.

7.3.5.3.3 Temperature Monitor

The DP83561-SP has an on chip temperature monitor. DP83561-SP offers the option to configure the percentage of sudden change in output from the temperature sensors. When temperature changes exceed that percentage, the INT_SUP_CUR_N signal will be asserted.

Refer to registers 0x1E8 and 0x1EA on how to read data from the temperature sensor.

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7.3.5.3.4 PLL Lock Monitor

The DP83561-SP has phase lock detector to continuously monitor the PLL an raises a instantaneous interrupt when it goes out of lock. When the phase difference is higher than a programmable delay window, the lock detector output is deasserted.

Once they align again, the lock detector waits for a programmable number of reference cycles before asserting the lock signal again. This monitor can particularly be used to monitor any impact on the data transmission due to SEU.

To enable the PLL lock interrupt, bit[11] of register 0x01D7 needs to be set to 0 to unmask the interrupt. Then, one of the GPIO pins must be configured to the functionality of SEFI_INTERRUPT.

7.3.6 WoL (Wake-on-LAN) Packet Detection

Wake-on-LAN provides a mechanism to detect specific frames and notify the connected MAC through either a register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83561-SP allows for connected devices placed above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet, Magic Packet with SecureOn, and Custom Pattern Match. When a qualifying WoL frame is received, the DP83561-SP WoL logic circuit is able to generate a user-defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred.

The Wake-on-LAN feature includes the following functionality:

- Identification of magic packets in all supported speeds
- Wake-up interrupt generation upon receiving a valid magic packet
- CRC checking of magic packets to prevent interrupt generation for invalid packets

In addition to the basic magic packet support, the DP83561-SP also supports:

- Magic packets that include a SecureOn password
- Pattern match – one configurable 64-byte pattern of that can wake up the MAC similar to magic packet
- Independent configuration for Wake on Broadcast and Unicast packet types.

7.3.6.1 Magic Packet Structure

When configured for Magic Packet mode, the DP83561-SP scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

Note

The Magic Packet should be byte aligned.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST address), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions, followed by secure-on password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh.

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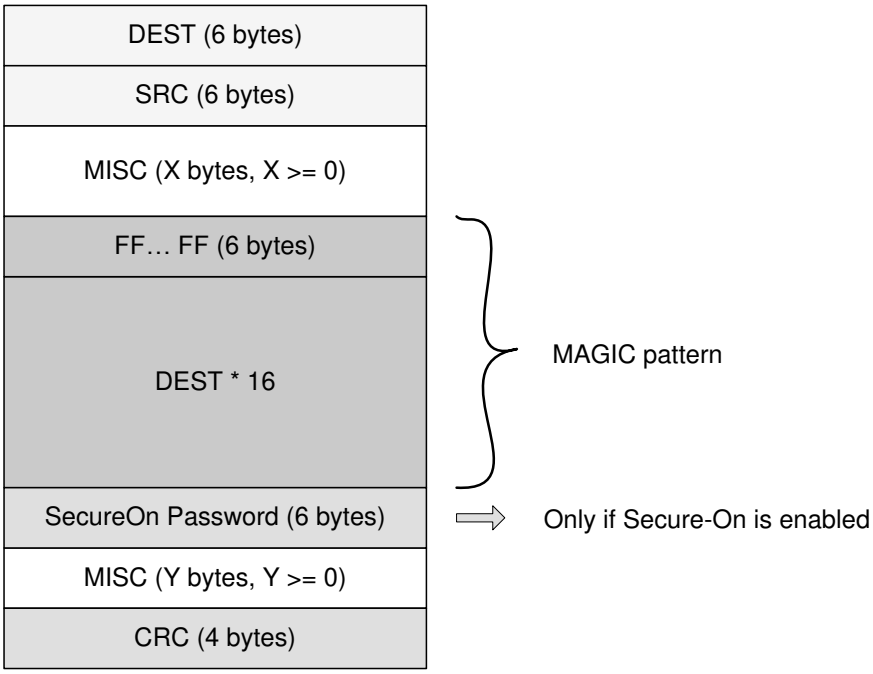


図 7-6. Magic Packet Structure

7.3.6.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a SecureOn Password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
 DESTINATION SOURCE MISC FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11
22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44
55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11
22 33 44 55 66 11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

7.3.6.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the RXFCFG register (address 0x0134). Wake-on-LAN status is reported in the RXFSTS register (address 0x0135).

7.3.7 Start of Frame Detect for IEEE 1588 Time Stamp

The DP83561-SP supports an IEEE 1588 indication pulse at the SFD (start frame delimiter) for the receive and transmit paths. The pulse can be delivered to various pins. The pulse indicates the actual time the symbol is presented on the MAC I/O lines (for transmit), or the first symbol received (for receive). This signal toggles after some latency from the MDI lines. The exact timing of the pulse can be adjusted through register. Each increment of phase value is an 8-ns step.

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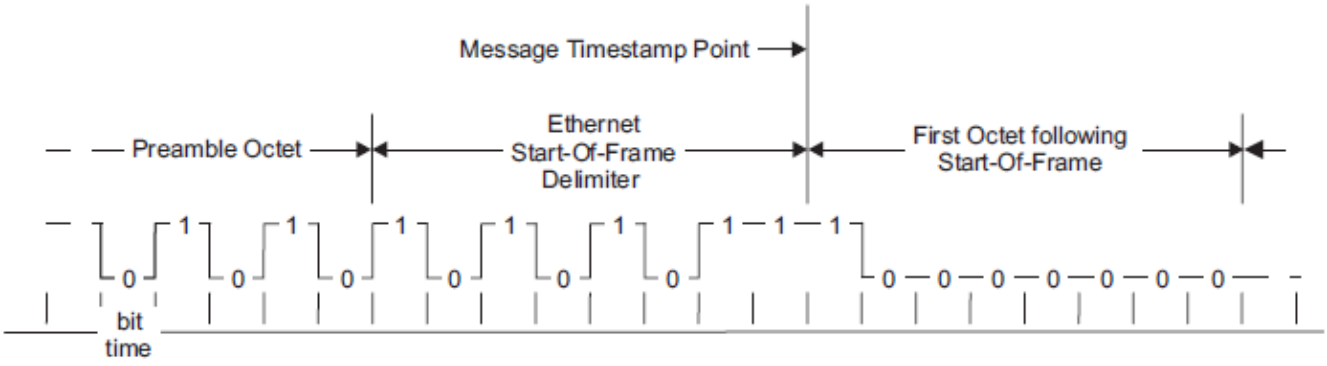


図 7-7. IEEE 1588 Message Timestamp Point

The SFD pulse output can be configured using the GPIO Mux Control register GPIO_MUX_CTRL (register address 0x1E0). The ENHANCED_MAC_SUPPORT bit in RXCFG (register address 0x134) must also be set to allow output of the SFD.

7.3.7.1 SFD Latency Variation and Determinism

Time stamping packet transmission and reception using the RX_CTRL and TX_CTRL signals of RGMII is not accurate enough for latency sensitive protocols. SFD pulses offers system designers a method to improve the accuracy of packet time stamping. The SFD pulse, while varying less than RGMII signals inherently, still exhibits latency variation due to the defined architecture of 1000BASE-T. This section provides a method to determine when an SFD latency variation has occurred and how to compensate for the variation in system software to improve timestamp accuracy.

In the following section the terms baseline latency and SFD variation are used. Baseline latency is the time measured between the TX_SFD pulse to the RX_SFD pulse of a connected link partner, assuming an Ethernet cable with all 4 pairs perfectly matched in propagation time. In the scenario where all 4 pairs being perfectly matched, a 1000BASE-T PHY will not have to align the 4 received symbols on the wire and will not introduce extra latency due to alignment.

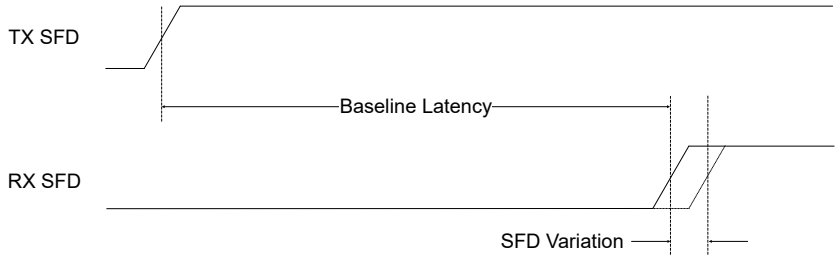


図 7-8. Baseline Latency and SFD Variation in Latency Measurement

SFD variation is additional time added to the baseline latency before the RX_SFD pulse when the PHY must introduce latency to align the 4 symbols from the Ethernet cable. Variation can occur when a new link is established either by cable connection, auto-negotiation restart, PHY reset, or other external system effects. During a single, uninterrupted link, the SFD variation will remain constant.

The DP83561-SP can limit and report the variation applied to the SFD pulse while in the 1000M operating mode. Before a link is established in 1000M mode, the Sync FIFO Control Register (register address 0x00E9) must be set to value 0xDF22. The below SFD variation compensation method can only be applied after the Sync FIFO Control Register has been initialized and a new link has been established. It is acceptable to set the Sync FIFO Control register value and then perform a software restart by setting the SW_RESTART bit[14] in the Control Register (register address 0x001F) if a link is already present.

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7.3.7.1.1 1000M SFD Variation in Master Mode

When the DP83561-SP is operating in 1000M master mode, variation of the RX_SFD pulse can be estimated using the Skew FIFO Status register (register address 0x0055) bit[7:4]. The value read from the Skew FIFO Status register bit[7:4] must be multiplied by 8 ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in master 1000M mode, a value of 0x2 is read from the Skew FIFO register bit[7:4]. 2 × 8 ns = 16 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

7.3.7.1.2 1000M SFD Variation in Slave Mode

When the DP83561-SP is operating in 1000M slave mode, the variation of the RX_SFD pulse can be determined using the Skew FIFO Status register (register address 0x0055) bit[3:0].The value read from the Skew FIFO Status register bit[3:0] should be multiplied by 8 ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in slave 1000M mode, a value of 0x1 is read from the Skew FIFO register bit[3:0]. 1 × 8 ns = 8 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

7.3.7.1.3 100M SFD Variation

The latency variation in 100M mode of operation is determined by random process and does not require any register readout or system level compensation of SFD pulses.

7.3.8 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed results in the need to non-intrusively identify and report cable faults. The DP83561-SP offers Time Domain Reflectometry (TDR) for Cable Diagnostics.

7.3.8.1 TDR

The DP83561-SP uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The DP83561-SP transmits a test pulse of known amplitude down each of the 4 pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector, and from the end of the cable itself. After the pulse transmission, the DP83561-SP measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), improperly-terminated cables, and crossed pairs wires with ±1-m accuracy.

The DP83561-SP also uses data averaging to reduce noise and improve accuracy. The DP83561-SP can record up to 5 reflections within the tested pair. If more than 5 reflections are recorded, the DP83561-SP saves the first 5 of them. If a cross fault is detected, the TDR saves the first location of the cross fault and up to 4 reflections in the tested channel. The DP83561-SP TDR can measure cables beyond 100 m in length.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition, and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the DP83561-SP in the following scenarios:

- While Link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains *quiet* (for example, in power-down mode)
- TDR could be automatically activated when the link fails or is dropped by setting bit 7 of register 0x9 (CFG1). The results of the TDR run after the link fails are saved in the TDR registers.

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Software could read these registers at any time to apply post processing on the TDR results. This mode is designed for cases when the link is dropped due to cable disconnections. After a link failure, for instance, the line is quiet to allow a proper function of the TDR.

7.3.8.2 Fast Link Drop

The DP83561-SP includes advanced link-down capabilities that support various real-time applications. The link down mechanism is configurable and includes enhanced modes that allow extremely fast reaction times to link drops.

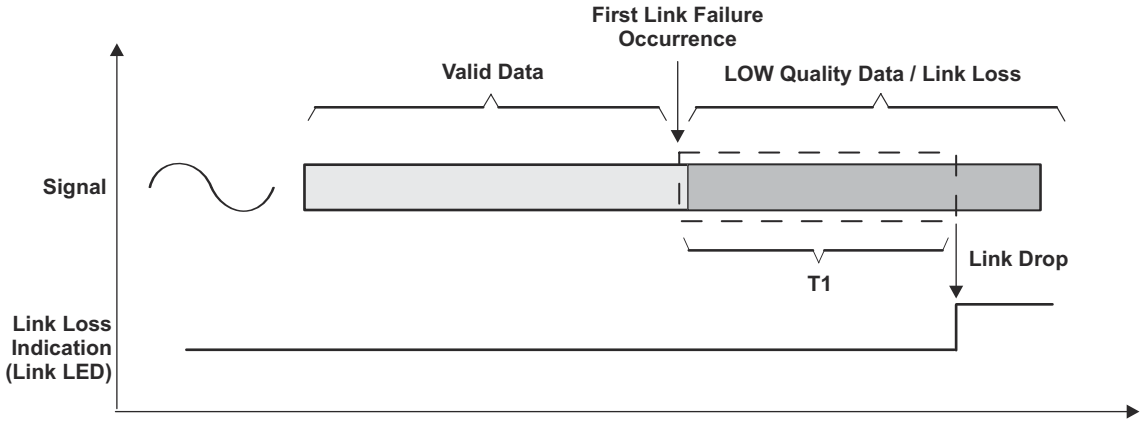


図 7-9. Fast Link Drop Mechanism

As described in 図 7-9, the link loss mechanism is based on a time window search period in which the signal behavior is monitored. The T1 window is set by default to reduce typical link drops to less than 1 ms in 100M mode and 0.5 ms in 1000M mode.

The DP83561-SP supports enhanced modes that shorten the window called Fast Link Down mode. In this mode, the T1 window is shortened significantly, in most cases less than 10 µs. In this period of time, there are several criteria allowed to generate link loss event and drop the link:

1. Loss of descrambler sync
2. Receive errors
3. MLT3 errors
4. Mean Squared Error (MSE)
5. Energy loss

The Fast Link Down functionality allows the use of each of these options separately or in any combination. Note that because this mode enables extremely quick reaction time, it is more exposed to temporary bad link quality scenarios.

7.3.8.3 Fast Link Detect

Several advanced modes are available for fast link establishment. Unlike the Auto-Negotiation and Auto-MDIX mechanisms defined by the IEEE 802.3 specification, these modes are specific to the DP83561-SP. Take care when implementing these modes. For best operation, TI recommends implementing these modes with a DP83561-SP on both ends of the link.

These advanced link and crossover modes depend on the speed selected for the link. Some modes are intended for use in 1000Base-T operation. Others are intended for use in 100Base-TX operation.

Fast Link Detect functionality can be configured using the Configuration Register 3 (CFG3), address 0x001E.

7.3.8.4 Energy Detect

The energy-detector module provides signal-strength indication in various scenarios. Because it is based on an IIR filter, this robust energy detector has excellent reaction time and reliability. The filter output is compared to predefined thresholds to decide the presence or absence of an incoming signal. The energy detector also

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implements hysteresis to avoid jittering in signal-detect indication. Additionally, it has fully-programmable thresholds and listening-time periods, enabling shortening of the reaction time if required.

7.3.8.5 IEEE 802.3 Test Modes

IEEE 802.3 specification for 1000BASE-T requires that the PHY layer be able to generate certain well defined test patterns on TX outputs. Clause 40 section 40.6.1.1.2 *Test Modes* describes these tests in detail. There are four test modes as well as the normal operation mode. These modes can be selected by writing to the CFG1 register (address 0x0009). In addition, writing 0x1002 to register 0x00A8 is a required configuration when using any of the test modes.

See IEEE 802.3 section 40.6.1.1.2 *Test modes* for more information on the nature of the test modes. The DP83561-SP provides a test clock synchronous to the IEEE test patterns. The test patterns are output on the MDI pins of the device and the transmit clock is output on the CLK_OUT pin.

For more information about configuring the DP83561-SP for IEEE 802.3 compliance testing, see the *How to Configure DP838XX for Ethernet Compliance Testing* application report (SNLS239).

7.3.8.6 Jumbo Frames

Conventional Ethernet frames have a maximum size of about 1518 bytes. Jumbo Frames are special packets with size higher than 1518 bytes, often ranging into several thousands of bytes. Jumbo frames allow Ethernet systems to transfer large chunks of data in a single frame reducing the processor overhead and increasing bandwidth efficiency. DP83561-SP supports Jumbo frames up to 13 KB in 1000-Mbps and 100-Mbps speeds.

7.3.9 Clock Output

The DP83561-SP has several internal clocks, including the local reference clock, the Ethernet transmit clock, and the Ethernet receive clock. An external crystal or oscillator provides the stimulus for the local reference clock. The local reference clock acts as the central source for all clocking in the device.

The local reference clock is embedded into the transmit network packet traffic and is recovered from the network packet traffic at the receiver node. The receive clock is recovered from the received Ethernet packet data stream and is locked to the transmit clock in the partner.

Using the I/O Configuration register (address 0x170), the DP83561-SP can be configured to output these internal clocks through the CLK_OUT pin. For the I/O Configuration register (address 0x170) settings to work, an additional configuration of writing register 0x00C6 to value of 0x0010 is required. By default, the output clock is synchronous to the XI oscillator / crystal input. The default output clock is suitable for use as the reference clock of another DP83561-SP device. Through registers, the output clock can be configured to be synchronous to the receive data at the 125-MHz data rate or at the divide by 5 rate of 25 MHz. It can also be configured to output the line driver transmit clock. When operating in 1000Base-T mode, the output clock can be configured for any of the four transmit or receive channels.

It is important to note that when the clock output of DP83561-SP is used as a clock input for another device, for example two DP83561-SP devices in a daisy chain, then the primary DP838561-SP should not be reset through the RESET pin. If reset is required then it should be performed through the software. The output clock can be disabled using the CLK_O_DISABLE bit of the I/O Configuration register.

7.4 Device Functional Modes

7.4.1 Mirror Mode

In some applications, the orientation of the cable connector can require Copper PMD traces to cross over each other. This complicates the board layout. The DP83561-SP can resolve this issue by implementing mirroring of the ports inside the device. Normal and Mirror modes offer flexibility to mount the RJ45 connector on either the top or bottom layer without any undesired cross-overs of differential signals, as shown in 図 7-10.

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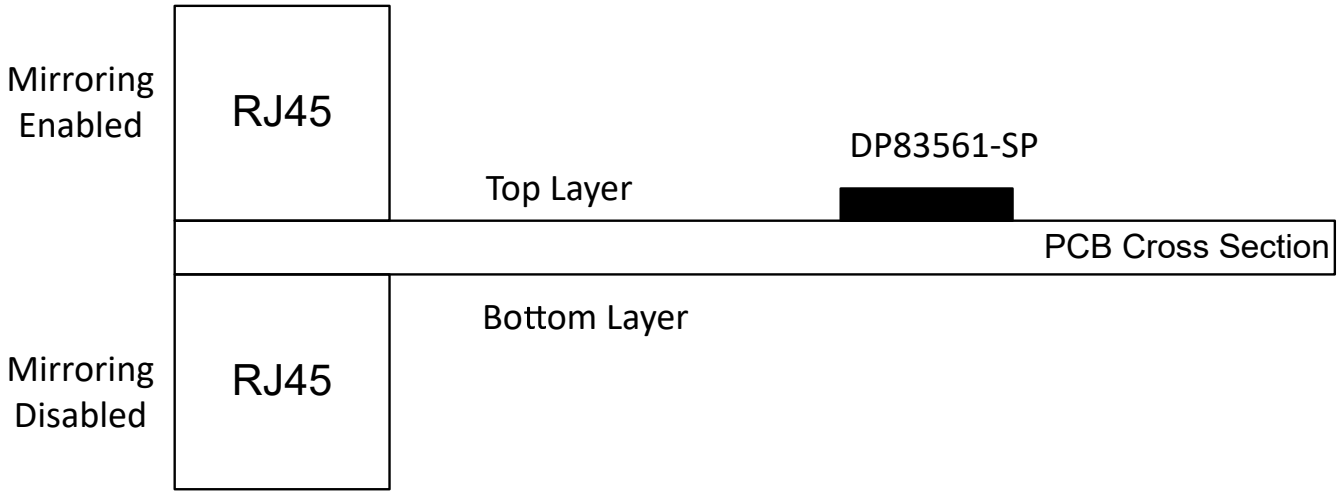


図 7-10. Normal and Mirror Mode RJ45 Mounting Orientation

In 10/100 operation, the mapping of the port mirroring is shown in 表 7-2. When using mirror mode in 100-Mbps mode, TI recommends that the user read register 0xA1 and write the same value in register 0xA0. The steps are as follows:

- Read register 0xA1 bits[12:8] and write to register 0xA0 bits[4:0]
- Read register 0xA1 bits[4:0] and write to register 0xA0 bits[12:8]

表 7-2. 10/100-Mbps Mirror Mode Map

MDI MODE	MIRROR PORT CONFIGURATION
MDI	A → D
	B → C
MDIX	A → D
	B → C

In Gigabit operation, the mapping of the port mirroring is:

表 7-3. Gigabit Mirror Mode Map

MDI MODE	MIRROR PORT CONFIGURATION
MDI or MDIX	A → D
	B → C
	C → B
	D → A

Mirror mode can be enabled through strap or through register configuration using the Port Mirror Enable bit in the CFG4 register (address 0x0031). In Mirror mode, the polarity of the signals is also reversed.

表 7-4 shows which pin/channel corresponds to which signal line in normal and mirror mode.

表 7-4. Normal/Mirror Mode Pin-to-Channel Map

DP83561-SP		Normal Mode			Mirror Mode		
Pin	Channel	1000 M Mode	100M MDI Mode	100M MDIX Mode	1000 M Mode	100M MDI Mode	100M MDIX Mode
1	A	Td_P_A (+)	Td_P_A (Tx+)	Td_P_A (Rx+)	Td_M_D(-)		
2	A	Td_M_A (-)	Td_M_A (Tx-)	Td_M_A (Rx-)	Td_P_D(+)		
4	B	Td_P_B(+)	Td_P_B (Rx+)	Td_P_B (Tx+)	Td_M_C (-)		

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表 7-4. Normal/Mirror Mode Pin-to-Channel Map (continued)

DP83561-SP		Normal Mode			Mirror Mode		
5	B	Td_M_B (-)	Td_M_B (Rx-)	Td_M_B (Tx-)	Td_P_C(+)		
7	C	Td_P_C(+)			Td_M_B (-)	Td_M_B (Rx-)	Td_M_A (Tx-)
8	C	Td_M_C (-)			Td_P_B(+)	Td_P_B (Rx+)	Td_P_A (Tx+)
10	D	Td_P_D(+)			Td_M_A (-)	Td_M_A (Tx-)	Td_M_B (Rx-)
11	D	Td_M_D(-)			Td_P_A (+)	Td_P_A (Tx+)	Td_P_B (Rx+)

7.4.2 Loopback Mode

There are several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83561-SP may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback. MII Loopback is configured using the BMCR (register address 0x0). All other loopback modes are enabled using the BIST_CONTROL (register address 0x16). Except where otherwise noted, loopback modes are supported for all speeds (10/100/1000) and all MAC interfaces (MII and RGMII).

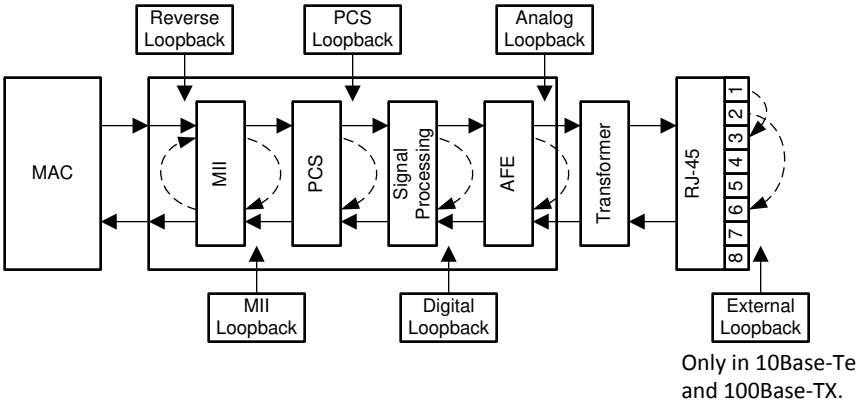


図 7-11. Loopbacks

7.4.2.1 Near-End Loopback

Near-end loopback provides the ability to loop the transmitted data back to the receiver through the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits with several options being provided.

When configuring loopback modes, the Loopback Configuration Register (LOOPCR), address 0x00FE, should be set to 0xE720.

To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting the Near-End Loopback mode. This constraint does not apply for external-loopback mode.

Auto-MDIX should be disabled before selecting the Near-End Loopback mode. MDI or MDIX configuration should be manually configured.

7.4.2.1.1 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. While in MII Loopback mode the data is looped back, and can also be configured through register to transmit onto the media.

7.4.2.1.2 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

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7.4.2.1.3 Digital Loopback

Digital Loopback includes the entire digital transmit – receive path. Data is looped back prior to the analog circuitry.

7.4.2.1.4 Analog Loopback

Analog Loopback includes the entire analog transmit-receive path.

7.4.2.1.5 External Loopback

When operating in 10BASE-Te or 100Base-T mode, signals can be looped back at the RJ-45 connector by wiring the transmit pins to the receive pins. Due to the nature of the signaling in 1000Base-T mode, this type of external loopback is not supported. Analog loopback provides a way to loop data back in the analog circuitry when operating in 1000Base-T mode. For proper operation in Analog Loopback mode, attach 100-Ω terminations to the RJ45 connector.

7.4.2.1.6 Far-End (Reverse) Loopback

Far-end (Reverse) Loopback is a special test mode to allow testing the PHY from the link-partner side. In this mode, data that is received from the link partner passes through the PHY's receiver, is looped back at the MAC interface and is transmitted back to the link partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored. Through register configuration, data can also be transmitted onto the MAC Interface.

7.4.2.2 Loopback Availability Exception

The availability of Loopback depends on the operational mode of the PHY. The Link Status in these loopback modes is also affected by the operational mode. 表 7-5 lists out the exceptions where Loopbacks are not available.

表 7-5. Loopback Availability Exception

OP MODE	LOOPBACK	EXCEPTION
Copper	PCS	10M

7.4.3 Power-Saving Modes

DP83561-SP supports four power saving modes. The details are provided below.

7.4.3.1 IEEE Power Down

The PHY is powered down but access to the PHY through MDIO-MDC pins is retained. This mode can be activated by asserting external PWDN pin or by setting bit 11 of BMCR (Register 0x00).

The PHY can be taken out of this mode by a power cycle, software reset, or by clearing the bit 11 in BMCR register. However, the external PWDN pin should be deasserted. If the PWDN pin is kept asserted then the PHY remains in power down.

7.4.3.2 Deep Power-Down Mode

This is same as IEEE power down but the XI pad is also turned off. To enable this mode, the following sequence of register writes need to be performed.

- Enable Deep Power-Down Mode by setting bit 7 of PHYCR (register 0x10)
- Enable IEEE Power-Down by setting bit 11 of BMCR (register 0x0) (This can also be enabled by asserting the external PWDN pin)
- Write 0x0010 to register 0x00C6

If Deep Power Down Mode is activated through a register write, then clearing the power-down bit will bring the PHY back to normal mode. If the power-down mode is activate through PWDN pin assertion, then the PWDN pin must be deasserted followed by a valid Reset pulse to bring the PHY back to normal operation.

The Power Down Input pin is a shared pin which also acts an Interrupt Output pin. The nature of the pin can be changed through Register 0x1E bit[7]. When changing the pin from Interrupt Output to Power Down Input, the following sequence of register writes must be performed.

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- Disable all interrupts by writing registers 0x12 = 0x0 and register 0xC18 = 0x0.
- Clear all interrupts by reading registers 0x13 and 0xC19.
- Wait for 5 µs.
- Clear register 0x1E[7] to switch from Interrupt Input to Power Down Output.

7.4.3.3 Active Sleep

In this mode, all the digital and analog blocks are powered down. The PHY is automatically powered up when a link partner is detected. This mode is useful for saving power when the link partner is down or inactive, but PHY cannot be powered down. In Active Sleep mode, the PHY still routinely sends NLP to the link partner. This mode can be active by writing binary 10 to bits [9:8] for PHYCR (Register 0x10). Active sleep mode cannot be used when Auto-MDIX is on.

7.4.3.4 Passive Sleep

This is just like Active sleep except the PHY does not send NLP. This mode can be activated by writing binary 11 to bits [9:8] PHYCR (Register 0x10). Passive sleep mode cannot be used when Auto-MDIX is on.

7.5 Programming

7.5.1 Serial Management Interface

The Serial Management Interface (SMI), provides access to the DP83561-SP internal register space for status information and configuration. The SMI is compatible with IEEE 802.3-2002 clause 22. The implemented register set consists of the registers required by the IEEE 802.3, plus several others to provide additional visibility and controllability of the DP83561-SP device.

The SMI includes the MDC management clock input and the management MDIO data pin. The MDC clock is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 24 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

The MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC clock. The MDIO pin requires a pullup resistor (2.2 kΩ) which, during IDLE and turnaround, pulls MDIO high.

Up to 16 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up reset, the DP83561-SP latches the PHY_ADD configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83561-SP drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. 図 7-12 shows the timing relationship between MDC and the MDIO as driven and received by the Station (STA) and the DP83561-SP (PHY) for a typical register read access.

For write transactions, the station-management entity writes data to the addressed DP83561-SP, thus eliminating the requirement for MDIO turnaround. The turnaround time is filled by the management entity by inserting <10>. 図 7-13 shows the timing relationship for a typical MII register write access. The frame structure and general read and write transactions are shown in 表 7-6, 図 7-12, and 図 7-13.

表 7-6. Typical MDIO Frame Format

TYPICAL MDIO FRAME FORMAT	<idle><start><op code><device addr><reg addr><turnaround><data<idle>
Read Operation	<idle><01><10><AAAA><RRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01<01><AAAA><RRRR><10><xxxx xxxx xxxx xxxx><idle>

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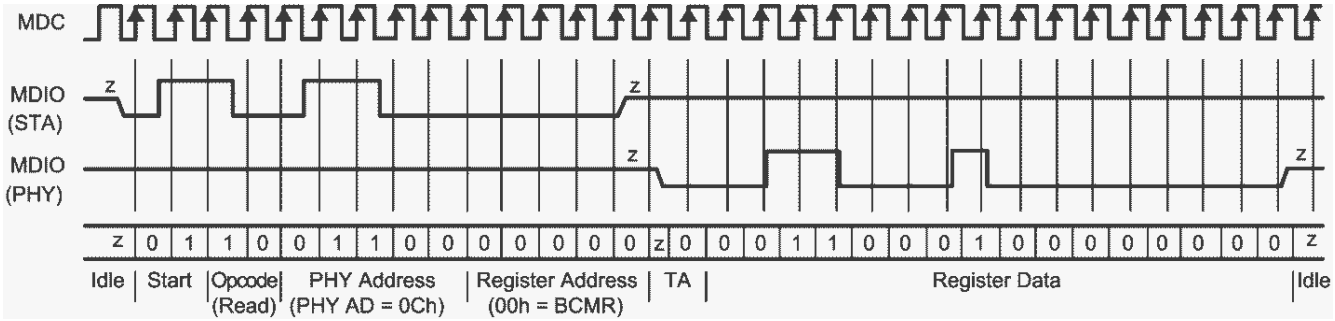


図 7-12. Typical MDC/MDIO Read Operation

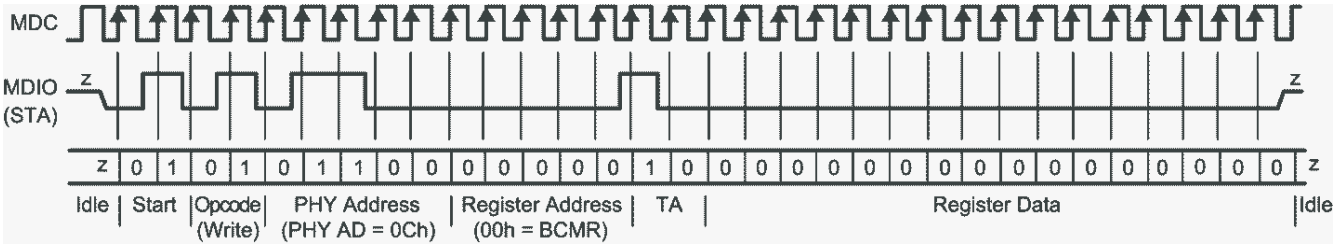


図 7-13. Typical MDC/MDIO Write Operation

7.5.1.1 Extended Address Space Access

The DP83561-SP SMI function supports read or write access to the extended register set using registers REGCR (0xDh) and ADDAR (0xEh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR (0xDh) and ADDAR (0xEh) which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR (0xDh) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR (0xEh) register to the appropriate MMD.

The DP83561-SP supports one MMD device address. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.

All accesses through registers REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:1] is 00, then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to 00, accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to 01, accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to 10, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to 11, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

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The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111).

7.5.1.1.1 Write Address Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

7.5.1.1.2 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

7.5.1.1.3 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.5.1.1.4 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note

Steps (1) and (2) can be skipped if the address register was previously configured.

7.5.1.1.5 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address from register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.5.1.1.6 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

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1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.5.1.1.7 Example of Read Operation Using Indirect Register Access

Read register 0x0170.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Read register 0x0E.

The expected default value is 0x0C10.

7.5.1.1.8 Example of Write Operation Using Indirect Register Access

Write register 0x0170 to value 0x0C50.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Write register 0x0E to value 0x0C50.

This write disables the output clock on the CLK_OUT pin.

7.5.2 Interrupt

The DP83561-SP can be configured to generate an interrupt when changes of internal status occur. The interrupt allows a MAC to act upon the status in the PHY without polling the PHY registers. The interrupt source can be selected through the interrupt register MICR (0x12). The interrupt status can be read from the ISR (0x13) register. Some interrupts are enabled by default and can be disabled through register access. Both the interrupt status registers must be read in order to clear pending interrupts. Until the pending interrupts are cleared, new interrupts may not be routed to the interrupt pin.

7.5.3 BIST Configuration

The device incorporates an internal PRBS Built-in Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. The BIST can be performed using both internal loopback (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and of the IPG.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for the BIST. The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass or fail status. The number of error bytes that the PRBS checker received is stored in the BICSR2 register (0x0072). The status of whether the PRBS checker is locked to the incoming receive bit stream, whether the PRBS has lost sync, and whether the packet generator is busy, can be read from the STS2 register (0x0017h). While the lock and sync indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the BICSR2 register (0x0072). The number of received bytes are stored in BICSR1 (0x0071).

The PRBS test can be put in a continuous mode by using bit 14 of the BISCR register (0x0016h). In continuous mode, when one of the PRBS counters reaches the maximum value, the counter starts counting from zero again. Packet transmission can be configured for one of two types, 64 and 1518 bytes, through register bit 13 of the BISCR register (0x0016).

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7.5.4 Strap Configuration

The DP83561-SP uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below.

Configuration of the device may be done through strap pins or through the management register interface. A pullup resistor and/or a pulldown resistor of suggested values may be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes.

The MAC interface pins must support I/O voltages of 3.3 V, 2.5 V, and 1.8 V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3-V, 2.5-V, and 1.8-V supplies depending on what voltage was selected for I/O. RX_D0 and RX_D1 pins are 4 level strap pins. All other strap pins have two levels.

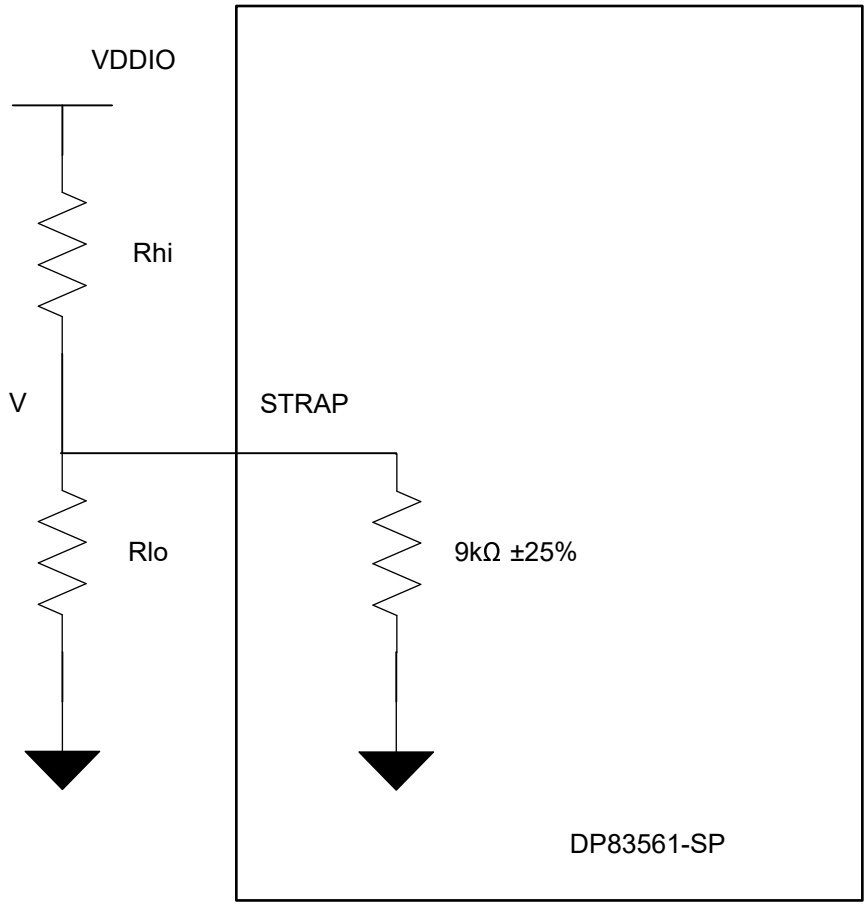


図 7-14. Strap Circuit

表 7-7. 4-Level Strap Resistor Ratio

MODE	TARGET VOLTAGE			IDEAL RESISTORS	
	Vmin (V)	Vtyp (V)	Vmax (V)	Rhi (kΩ)	Rlo (kΩ)
0	0	0	0.093 × VDDIO	OPEN	OPEN
1	0.136 × VDDIO	0.165 × VDDIO	0.184 × VDDIO	10	2.49
2	0.219 × VDDIO	0.255 × VDDIO	0.280 × VDDIO	5.76	2.49
3	0.6 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

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表 7-8. 2-Level Strap Resistor Ratio

MODE	TARGET VOLTAGE			IDEAL RESISTORS	
	Vmin (V)	Vtyp (V)	Vmax (V)	Rhi (kΩ)	Rlo (kΩ)
0	0		0.18 x VDDIO	OPEN	2.49
1	0.5 x VDDIO		0.88 x VDDIO	2.49	OPEN

表 7-9. Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	FUNCTION		
RX_D0	PHY_ADD[1:0]	44	0		PHY_ADD1	PHY_ADD0
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1
RX_D1	PHY_ADD[3:2]	45	0		PHY_ADD3	PHY_ADD2
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1
VDDIO_SEL_0	VDDIO_SEL_0	22	0	VDDIO level indication from system		
				VDDIO_SEL_1	VDDIO_SEL_0	Function
				0	0	VDDIO = 3.3 V
VDDIO_SEL_1	VDDIO_SEL_1	21	0	0	1	Reserved
				1	0	VDDIO = 2.5 V
				1	1	VDDIO = 1.8 V
SUPPLYMODE_SEL	SUPPLYMODE_SEL	23	0	Triple or dual supply setting from system		
				0 = Dual supply mode (VDDA1P8 left floating)		
				1 = Triple supply mode (VDDA1P8 supplied by system)		
CRS/GPIO_3	RGMII/MII_SEL	33	0	0 = RGMII		
				1 = MII		
AUTO_RECOVER	AUTO_RECOVER	34	0	0 = DP83561-SP will take no automatic action based on SEFI. SEFI event interrupts will be generated normally.		
				1 = Configures the DP83561-SP to automatically apply RESET signal to PHY logic when a SEFI is detected. Default register values will be reloaded and pin options. SEFI event interrupts will be generated normally.		
RX_DV/ RX_CTRL	MIRROR_EN	49	0	0 = Port Mirroring Disabled		
				1 = Port Mirroring Enabled		
SMI_DISABLE	SMI_DISABLE	50	0	0 = SMI(MDIO) writes are enabled.		
				1 = Station Management Interface (MDIO) writes are disabled.		
LED_0	ANEG_DIS	63	0	0 = DP83561-SP will auto-negotiate link as defined in IEEE 802.3 Clause 28		
				1 = DP83561-SP set to forced link speed operation. Speed settings are controlled by ANEGSEL_0 and ANEGSEL_1 pin options.		

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表 7-9. Strap Table (continued)

PIN NAME	STRAP NAME	PIN #	DEFAULT	FUNCTION			
LED_1	ANEGSEL_0	62	0	ANEG_DIS	ANEGSEL_1	ANEGSEL_0	Function
				0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
				0	1	0	Auto-negotiation, 100/10 advertised,Auto-MDI-X
				0	1	1	Reserved
LED_2/GPIO_0	ANEGSEL_1	61	0	1	0	0	Forced 1000M, master, MDI mode
				1	0	1	Forced 1000M, slave, MDI mode
				1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode

7.5.5 LED Configuration

The DP83561-SP supports four configurable Light Emitting Diode (LED) pins: LED_0, LED_1, LED_2, and RXD7/GPIO. Several functions can be multiplexed onto the LEDs for different modes of operation. The LED operation mode can be selected using the LEDCR1 register (address 0x0018).

Because the LED output pins are also used as straps, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power up or reset.

If a given strap input is resistively pulled low then the corresponding output is configured as an active high driver. In the context of the 4-level straps, this occurs for modes 1, 2, and 3. Conversely, if a given strap input is resistively pulled high, then the corresponding output is configured as an active low driver. In the context of the 4-level straps, this occurs only for mode 4.

Refer to 図 7-15 for an example of strap connections to external components. In this example, the strapping results in Mode 1 for LED_0 and Mode 4 for LED_1.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual-purpose pins.

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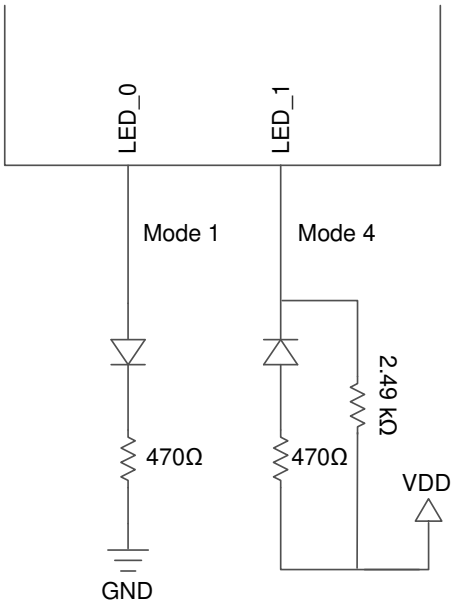


図 7-15. Example Strap Connections

7.5.6 LED Operation From 1.8-V I/O VDD Supply

Operation of LEDs from a 1.8-V supply results in dim LED lighting. For best results, the recommendation is to operate from a higher supply (2.5 V or 3.3 V). Refer to 図 7-16 for a possible implementation of this functionality.

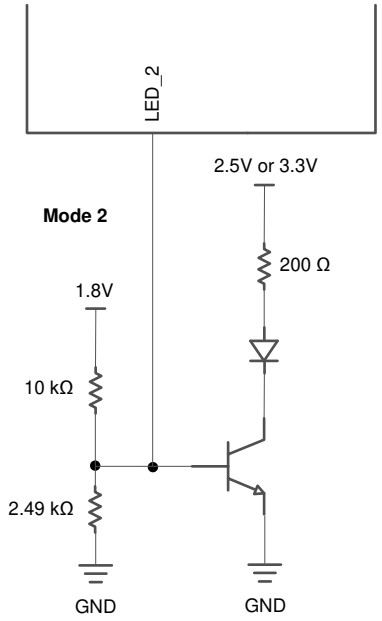


図 7-16. LED Operation From 1.8-V I/O VDD Supply

7.5.7 Reset Operation

The DP83561-SP includes an internal power-on reset (POR) function and therefore does not need to be explicitly reset for normal operation after power up. If required during normal operation, the device can be reset by a hardware or software reset.

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7.5.7.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse, with a duration of at least 1 µs, to the RESET_N pin. This resets the device such that all registers are reinitialized to default values and the hardware configuration values are re-latched into the device (similar to the power up or reset operation).

7.5.7.2 IEEE Software Reset

An IEEE registers software reset is accomplished by setting the reset bit (bit 15) of the BMCR register (address 0x0000). This bit resets the IEEE-defined standard registers.

7.5.7.3 Global Software Reset

A global software reset is accomplished by setting bit 15 of register CTRL (address 0x001F) to 1. This bit resets all the internal circuits in the PHY including IEEE-defined registers and all the extended registers. The global software reset resets the device such that all registers are reset to default values and the hardware configuration values are maintained.

7.5.7.4 Global Software Restart

A global software restart is accomplished by setting bit 14 of register CTRL (0x1F) to 1. This action resets all the PHY circuits except the registers in the Register File.

7.5.7.5 PCS Restart

A PCS reset is accomplished by setting bit 15 of register MMD3_PCS_CTRL (MMD3 register 0x1000). Setting this bit resets the MMD3 and MMD7 registers. This bit subsequently cause a soft reset through the BMCR RESET bit (bit 15 of register address 0x0).

7.6 Register Maps

7.6.1 DP83561SP Registers

表 7-10 lists the DP83561SP registers. All register offset addresses not listed in 表 7-10 should be considered as reserved locations and the register contents should not be modified.

表 7-10. DP83561SP Registers

Offset	Acronym	Register Name	Section
0x0	BMCR	Basic Mode Control Register	Go
0x1	BMSR	Basic Mode Status Register	Go
0x2	PHYIDR1	PHY Identifier Register #1	Go
0x3	PHYIDR2	PHY Identifier Register #2	Go
0x4	ANAR	Auto-Negotiation Advertisement Register	Go
0x5	ALNPAR	Auto-Negotiation Link Partner Ability Register	Go
0x6	ANER	Auto-Negotiate Expansion Register	Go
0x7	ANNPTR	Auto-Negotiation Next Page Transmit Register	Go
0x8	ANLNPTR	Auto-Negotiation Link Partner Next Page Receive Register	Go
0x9	GEN_CFG1	Configuration Register 1	Go
0xA	GEN_STATUS1	Status Register 1	Go
0xD	REGCR	Register Control Register	Go
0xE	ADDAR	Address or Data Register	Go
0xF	1KSCR	1000BASE-T Status Register	Go
0x10	PHY_CONTROL	PHY Control Register	Go
0x11	PHY_STATUS	PHY Status Register	Go
0x12	INTERRUPT_MASK	MII Interrupt Control Register	Go
0x13	INTERRUPT_STATUS	Interrupt Status Register	Go
0x14	GEN_CFG2	Configuration Register 2	Go

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表 7-10. DP83561SP Registers (continued)

Offset	Acronym	Register Name	Section
0x15	RX_ERR_CNT		Go
0x16	BIST_CONTROL	BIST Control Register	Go
0x17	GEN_STATUS2	Status Register 2	Go
0x18	LEDS_CFG1	LED Configuration Register 1	Go
0x19	LEDS_CFG2	LED Configuration Register 2	Go
0x1A	LEDS_CFG3	LED Configuration Register 3	Go
0x1E	GEN_CFG4	Configuration Register 3	Go
0x1F	GEN_CTRL	Control Register	Go
0x25	ANALOG_TEST_CTRL	Testmode Channel Control Register	Go
0x2C	GEN_CFG_ENH_AMIX		Go
0x2D	GEN_CFG_FLD		Go
0x2E	GEN_CFG_FLD_THR		Go
0x31	GEN_CFG3	Configuration Register 4	Go
0x32	RGMII_CTRL	RGMII Control Register	Go
0x33	RGMII_CTRL2		Go
0x39	PRBS_TX_CHK_CTRL		Go
0x3A	PRBS_TX_CHK_BYTE_CNT		Go
0x43	G_100BT_REG0		Go
0x55	G_1000BT_PMA_STATUS	Skew FIFO Status Register	Go
0x6E	STRAP_STS	Strap Status Register	Go
0x71	DBG_PRBS_BYTE_CNT		Go
0x72	DBG_PRBS_ERR_CNT		Go
0x7B	DBG_PKT_LEN_PRBS		Go
0x86	ANA_RGMII_DLL_CTRL	RGMII Delay Control Register	Go
0xC6	ANA_PLL_PROG_PI		Go
0xFE	LOOPCR	Loopback Configuration Register	Go
0x134	RXF_CFG		Go
0x135	RXF_STATUS		Go
0x170	IO_MUX_CFG		Go
0x180	TDR_GEN_CFG1		Go
0x181	TDR_GEN_CFG2		Go
0x182	TDR_SEG_DURATION1		Go
0x183	TDR_SEG_DURATION2		Go
0x184	TDR_GEN_CFG3		Go
0x185	TDR_GEN_CFG4		Go
0x190	TDR_PEAKS_LOC_A_0_1		Go
0x191	TDR_PEAKS_LOC_A_2_3		Go
0x192	TDR_PEAKS_LOC_A_4_B_0		Go
0x193	TDR_PEAKS_LOC_B_1_2		Go
0x194	TDR_PEAKS_LOC_B_3_4		Go
0x195	TDR_PEAKS_LOC_C_0_1		Go
0x196	TDR_PEAKS_LOC_C_2_3		Go
0x197	TDR_PEAKS_LOC_C_4_D_0		Go
0x198	TDR_PEAKS_LOC_D_1_2		Go
0x199	TDR_PEAKS_LOC_D_3_4		Go

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表 7-10. DP83561SP Registers (continued)

Offset	Acronym	Register Name	Section
0x1A4	TDR_GEN_STATUS		Go
0x1A5	TDR_PEAKS_SIGN_A_B		Go
0x1A6	TDR_PEAKS_SIGN_C_D		Go
0x1D6	MASK_SOFT_RST		Go
0x1D7	MASK_EXTERNAL_INT		Go
0x1D8	SEU_STATUS_REG		Go
0x1D9	REF_CLK_PPM_MONITOR_CNT		Go
0x1DA	MON_CLK_PPM_MONITOR_CNT		Go
0x1DB	MAX_PLUS_PPM_MON_CNT		Go
0x1DC	MAX_MINUS_PPM_MON_CNT		Go
0x1DD	SYS_CLK_PPM_STATUS		Go
0x1DE	PLL_CLK_PPM_STATUS		Go
0x1DF	OP_MODE_DECODE		Go
0x1E0	GPIO_MUX_CTRL		Go
0x1E2	MONITOR_REGISTERS_0		Go
0x1E7	MONITOR_REGISTERS_1		Go
0x1E8	MONITOR_REGISTERS_2		Go
0x1E9	MONITOR_REGISTERS_3		Go
0x1EA	MONITOR_REGISTERS_RD_0		Go
0x1EE	LOCK_DET_REG		Go

Complex bit access types are encoded to fit into small table cells. 表 7-11 shows the codes that are used for access types in this section.

表 7-11. DP83561SP Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	R C	Read to Clear
RH	R H	Read Set or cleared by hardware
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WoP	W	Write
WtoP	W	Write
Reset or Default Value		
- *n*		Value after reset or the default value

7.6.1.1 BMCR Register (Offset = 0x0) [Reset = 0x1140]

BMCR is shown in 表 7-12.

Return to the Summary Table.

IEEE defined register to control PHY functionality.

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表 7-12. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESET	R/W	0x0	This bit controls the MII reset function. This bit is self cleared after reset is completed. 0x0 = Normal Operation 0x1 = Reset.
14	MII_LOOPBACK	R/W	0x0	This bit controls the MII Loopback. When enabled, this will send data back to the MAC 0x0 = Disable 0x1 = Enable
13	SPEED_SEL_LSB	R/W	0x0	Speed selection bits LSB[13] and MSB[6] are used to control the data rate of the ethernet link when auto-negotiation is disabled. 0x0 = 10Mbps 0x1 = 100Mbps 0x2 = 1000Mbps 0x3 = Reserved
12	AUTONEG_EN	R/W	0x1	Controls autonegotiation feature 0x0 = Autonegotiation off 0x1 = Autonegotiation on
11	PWD_DWN	R	0x0	Controls IEEE power down feature 0x0 = Normal Mode 0x1 = IEEE power down mode
10	ISOLATE	R/W	0x0	Isolate MAC interface pins. 0x0 = Normal mode 0x1 = MAC Isolate mode enabled
9	RSTRT_AUTONEG	RH/WtoP	0x0	Restart auto-negotiation 0x0 = Normal mode 0x1 = Restart autonegotiation
8	DUPLEX_EN	R/W	0x1	Controls Half and Full duplex mode of the ethernet link 0x0 = Half Duplex mode 0x1 = Full Duplex mode
7	COL_TST	R/W	0x0	Controls Collision Signal Test 0x0 = Disable Collision Signal Test 0x1 = Enable Collision Signal Test
6	SPEED_SEL_MSB	R	0x1	Controls data rate of ethernet link when autonegotiation is disabled. See bit 13 description for morw information.
5-0	RESERVED	R	0x0	Reserved

7.6.1.2 BMSR Register (Offset = 0x1) [Reset = 0x7949]

BMSR is shown in 表 7-13.

Return to the Summary Table.

IEEE defined register to show status of PHY

表 7-13. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	100M_FDUP	R	0x1	100Base-TX full duplex 0x0 = PHY not able to perform full duplex 100Base-X 0x1 = PHY able to perform full duplex 100Base-X
13	100M_HDUP	R	0x1	100Base-TX halfduplex 0x0 = PHY not able to perform half duplex 100Base-X 0x1 = PHY able to perform half duplex 100Base-X
12	10M_FDUP	R	0x1	10Base-Te full duplex 0x0 = PHY not able to operate at 10Mbps in full duplex 0x1 = PHY able to operate at 10Mbps in full duplex

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表 7-13. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	10M_HDUP	R	0x1	10Base-Te half duplex 0x0 = PHY not able to operate at 10Mbps in half duplex 0x1 = PHY able to operate at 10Mbps in half duplex
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	EXT_STS	R	0x1	Extended status for 1000Base T abilities in register 15 0x1 = Extended status information in register 0x0F
7	RESERVED	R	0x0	Reserved
6	MF_PREAMBLE_SUP	R	0x1	Ability to accept management frames with preamble suppressed. For the Preamble suppression mode - a minimum of 1 preamble is required for DP83561-SP PHY 0x0 = PHY will not accept management frames with preamble suppressed 0x1 = PHY will accept management frames with preamble suppressed
5	AUTONEG_COMP	R	0x0	Status of Autonegotiation 0x0 = Auto Negotiation process not completed 0x1 = Auto Negotiation process completed
4	REMOTE_FAULT	RC	0x0	Remote fault detection 0x0 = No remote fault condition detected 0x1 = Remote fault condition detected
3	AUTONEG_ABL	R	0x1	Autonegotiation ability 0x0 = PHY is not able to perform Auto-Negotiation 0x1 = PHY is able to perform Auto-Negotiation
2	LINK_STS1	R	0x0	Link Status This is latch low and needs to be read twice for valid link up 0x0 = Link down 0x1 = Link up
1	JABBER_DTCT	RC	0x0	Jabber detected 0x0 = No jabber detected 0x1 = Jabber detected
0	EXT_CAPBLTY	R	0x1	Extended register capabilities 0x0 = Basic register set capabilities 0x1 = Extended register set capabilities

7.6.1.3 PHYIDR1 Register (Offset = 0x2) [Reset = 0x2000]

PHYIDR1 is shown in 表 7-14.

Return to the Summary Table.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83561SP. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management. Texas Instruments' IEEE assigned OUI is 080028h.

表 7-14. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OUI_MSB	R	0x2000	OUI Most Significant Bits: Bits 3 to 18 of the OUI (080028h,) are stored in bits 15 to 0 of this register respectively. Bit numbering for OUI goes from 1 (MSB) to 24(LSB). The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

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7.6.1.4 PHYIDR2 Register (Offset = 0x3) [Reset = 0xA1A4]

PHYIDR2 is shown in 表 7-15.

Return to the Summary Table.

表 7-15. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	OUI_LSB	R	0x28	OUI Least Significant Bits: Bits 19 to 24 of the OUI (080028h) are mapped from bits 15 to 10 of this register respectively.
9-4	MODEL_NUM	R	0x1A	Model number: The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3-0	REVISION_NUM	R	0x4	Revision number: Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

7.6.1.5 ANAR Register (Offset = 0x4) [Reset = 0x1E1]

ANAR is shown in 表 7-16.

Return to the Summary Table.

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation. Any writes to this register prior to completion of Auto-Negotiation (as indicated in the Basic Mode Status Register (address 01h) Auto-Negotiation Complete bit, BMSR[5]) should be followed by a renegotiation. This will ensure that the new values are properly used in the Auto-Negotiation.

表 7-16. ANAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_1_ADV	R/W	0x0	Next Page Advertisement 0x0 = Do not advertise desire to send additional SW next pages 0x1 = Advertise desire to send additional SW next pages
14	RESERVED	R	0x0	Reserved
13	REMOTE_FAULT_ADV	R/W	0x0	Remote Fault Advertisement 0x0 = Do not advertise remote fault event detection 0x1 = Advertise remote fault event detection
12	ANAR_BIT12	R/W	0x0	
11	ASYMMETRIC_PAUSE_ADV	R/W	0x0	1b = Advertise asymmetric pause ability 0b = Do not advertise asymmetric pause ability
10	PAUSE_ADV	R/W	0x0	0x0 = Do not advertise pause ability 0x1 = Advertise pause ability
9	G_100BT_4_ADV	R/W	0x0	100BT-4 is not supported
8	G_100BTX_FD_ADV	R/W	0x1	100Base-TX Full Duplex. Default depends on strap, non strap default '1'. 0x0 = Do not advertise 100Base-TX Full Duplex ability 0x1 = Advertise 100Base-TX Full Duplex ability
7	G_100BTX_HD_ADV	R/W	0x1	100Base-TX Half Duplex. Default depends on strap, non strap default '1'. 0x0 = Do not advertise 100Base-TX Half Duplex ability 0x1 = Advertise 100Base-TX Half Duplex ability
6	G_10BT_FD_ADV	R/W	0x1	Default depends on strap, non strap default '1' 0x0 = Do not advertise 10Base-T Full Duplex ability 0x1 = Advertise 10Base-T Full Duplex ability
5	G_10BT_HD_ADV	R/W	0x1	Default depends on strap, non strap default '1' 0x0 = Do not advertise 10Base-T Half Duplex ability 0x1 = Advertise 10Base-T Half Duplex ability
4-0	SELECTOR_FIELD_ADV	R/W	0x1	Technology selector field (802.3 == 00001)

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7.6.1.6 ALNPAR Register (Offset = 0x5) [Reset = 0x0]

ALNPAR is shown in 表 7-17.

Return to the Summary Table.

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful Auto-Negotiation if Next pages are supported.

表 7-17. ALNPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_1_LP	R	0x0	0x0 = Link Partner does not advertise desire to send additional SW next pages 0x1 = Link Partner advertises desire to send additional SW next pages
14	ACKNOWLEDGE_1_LP	R	0x0	0x0 = Link Partner does not acknowledge reception of link partner's link code word 0x1 = Link Partner acknowledges reception of link partner's link code word
13	REMOTE_FAULT_LP	R	0x0	0x0 = Link Partner does not advertise remote fault event detection 0x1 = Link Partner advertises remote fault event detection
12	RESERVED	R	0x0	Reserved
11	ASYMMETRIC_PAUSE_LP	R	0x0	0x0 = Link Partner does not advertise asymmetric pause ability 0x1 = Link Partner advertises asymmetric pause ability
10	PAUSE_LP	R	0x0	0x0 = Link Partner does not advertise pause ability 0x1 = Link Partner advertises pause ability
9	G_100BT4_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-T4 ability 0x1 = Link Partner advertises 100Base-T4 ability
8	G_100BTX_FD_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-TX Full Duplex ability 0x1 = Link Partner advertises 100Base-TX Full Duplex ability
7	G_100BTX_HD_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-TX Half Duplex ability 0x1 = Link Partner advertises 100Base-TX Half Duplex ability
6	G_10BT_FD_LP	R	0x0	0x0 = Link Partner does not advertise 10Base-T Full Duplex ability 0x1 = Link Partner advertises 10Base-T Full Duplex ability
5	G_10BT_HD_LP	R	0x0	0x0 = Link Partner does not advertise 10Base-T Half Duplex ability 0x1 = Link Partner advertises 10Base-T Half Duplex ability
4-0	SELECTOR_FIELD_LP	R	0x0	Technology selector field

7.6.1.7 ANER Register (Offset = 0x6) [Reset = 0x64]

ANER is shown in 表 7-18.

Return to the Summary Table.

This register contains additional Local Device and Link Partner status information.

表 7-18. ANER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0x0	Reserved
6	RX_NEXT_PAGE_LOC_ABLE	R	0x1	0x0 = Received Next Page storage location is not specified by bit 6.5 0x1 = Received Next Page storage location is specified by bit 6.5
5	RX_NEXT_PAGE_STOR_LOC	R	0x1	0x0 = Link Partner Next Pages are stored in register 5 0x1 = Link Partner Next Pages are stored in register 8
4	PRLL_TDCT_FAULE	RC	0x0	THIS STATUS IS LH (Latched-High) 0x0 = A fault has not been detected during the parallel detection process 0x1 = A fault has been detected during the parallel detection process

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表 7-18. ANER Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	LP_NP_ABLE	R	0x0	0x0 = Link partner is not able to exchange next pages 0x1 = Link partner is able to exchange next pages
2	LOCAL_NP_ABLE	R	0x1	0x0 = Local device is not able to exchange next pages 0x1 = Local device is able to exchange next pages
1	PAGE_RECEIVED_1	RC	0x0	THIS STATUS IS LH (Latched-High) 0x0 = A new page has not been received 0x1 = A new page has been received
0	LP_AUTONEG_ABLE	R	0x0	0x0 = Link partner is not Auto-Negotiation able 0x1 = Link partner is Auto-Negotiation able

7.6.1.8 ANNPTR Register (Offset = 0x7) [Reset = 0x2001]

ANNPTR is shown in 表 7-19.

Return to the Summary Table.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

表 7-19. ANNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_2_ADV	R/W	0x0	0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages
14	RESERVED	R	0x0	Reserved
13	MESSAGE_PAGE	R/W	0x1	0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	ACKNOWLEDGE2	R/W	0x0	0x0 = Do not set the ACK2 bit 0x1 = Set the ACK2 bit
11	TOGGLE	R	0x0	Toggles every page. Initial value is !4.11
10-0	MESSAGE_UNFORMATTED	R/W	0x1	Contents of the message/unformatted page

7.6.1.9 ANLNPTR Register (Offset = 0x8) [Reset = 0x2001]

ANLNPTR is shown in 表 7-20.

Return to the Summary Table.

This register contains the next page information sent by the Link Partner during Auto-Negotiation.

表 7-20. ANLNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_2_LP	R	0x0	0x0 = Link partner does not advertise desire to send additional next pages 0x1 = Link partner advertises desire to send additional next pages
14	ACKNOWLEDGE_2_LP	R	0x0	0x0 = Link partner does not acknowledge reception of link code work 0x1 = Link partner acknowledges reception of link code word
13	MESSAGE_PAGE_LP	R	0x1	0x0 = Received page is an unformatted page 0x1 = Received page is a message page
12	ACKNOWLEDGE2_LP	R	0x0	0x0 = Link partner does not set the ACK2 bit 0x1 = Link partner sets the ACK2 bit
11	TOGGLE_LP	R	0x0	Toggles every page. Initial value is !5.11
10-0	MESSAGE_UNFORMATTED_LP	R	0x1	Contents of the message/unformatted page

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7.6.1.10 GEN_CFG1 Register (Offset = 0x9) [Reset = 0x300]

GEN_CFG1 is shown in 表 7-21.

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表 7-21. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	TEST_MODE	R/W	0x0	0x0 = Normal Mode 0x1 = Test Mode 1 - Transmit Waveform Test 0x2 = Test Mode 2 - Transmit Jitter Test (Master Mode) 0x3 = Test Mode 3 - Transmit Jitter Test (Slave Mode) 0x4 = Test Mode 4 - Transmit Distortion Test 0x5 = Test Mode 5 - Scrambled MLT3 Idles 0x6 = Test Mode 6 - Repetitive 0001 sequence 0x7 = Test Mode 7 - Repetitive {Pulse, 63 zeros}
12	MASTER_SLAVE_MAN_CFG_EN	R/W	0x0	1 = Enable manual Master/Slave configuration 0 = Do not enable manual Master/Slave configuration
11	MASTER_SLAVE_MAN_CFG_VAL	R/W	0x0	1 = Manual configure as Master 0 = Manual configure as Slave
10	PORT_TYPE	R/W	0x0	1 = Multi-port device 0 = Single-port device
9	G_1000BT_FD_ADV	R/W	0x1	Default depends on strap 0x0 = Do not advertise 1000Base-T Full Duplex ability 0x1 = Advertise 1000Base-T Full Duplex ability
8	G_1000BT_HD_ADV	R/W	0x1	Default depends on strap 0x0 = Do not advertise 1000Base-T Half Duplex ability 0x1 = Advertise 1000Base-T Half Duplex ability
7	TDR_AUTO_RUN	R/W	0x0	TDR Auto Run at link down: 0x0 = Disable automatic execution of TDR 0x1 = Enable execution of TDR procedure after link down event
6-0	RESERVED	R	0x0	Reserved

7.6.1.11 GEN_STATUS1 Register (Offset = 0xA) [Reset = 0x0]

GEN_STATUS1 is shown in 表 7-22.

Return to the Summary Table.

表 7-22. GEN_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MS_CONFIG_FAULT	RC	0x0	1 = Master/Slave configuration fault detected 0 = No Master/Slave configuration fault detected THIS STATUS IS LH (Latched-High)
14	MS_CONFIG_RES	R	0x0	1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	LOC_RCVR_STATUS_1	R	0x0	1 = Local receiver is OK 0 = Local receiver is not OK
12	REM_RCVR_STATUS	R	0x0	1 = Remote receiver is OK 0 = Remote receiver is not OK
11	LP_1000BT_FD_ABILITY	R	0x0	1 = Link partner supports 1000Base-T Full Duplex ability 0 = Link partner does not support 1000Base-T Full Duplex ability
10	LP_1000BT_HD_ABILITY	R	0x0	1 = Link partner supports 1000Base-T Half Duplex ability 0 = Link partner does not support 1000Base-T Half Duplex ability
9-8	RESERVED	R	0x0	Reserved
7-0	IDLE_ERR_COUNT	R	0x0	1000Base-T Idle Error Counter

7.6.1.12 REGCR Register (Offset = 0xD) [Reset = 0x0]

REGCR is shown in 表 7-23.

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Return to the Summary Table.

This register is the MDIO Manageable MMD access control. In general, register REGCR (4:0) is the device address DEVAD that directs any accesses of the ADDAR (0x000E) register to the appropriate MMD. REGCR also contains selection bits for auto increment of the data register. This register contains the device address to be written to access the extended registers. Write 0x1F into bits 4:0 of this register. REGCR also contains selection bits (15:14) for the address auto-increment mode of ADDAR.

表 7-23. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	G_FUNCTION	R/W	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved
4-0	DEVAD	R/W	0x0	Device Address

7.6.1.13 ADDAR Register (Offset = 0xE) [Reset = 0x0]

ADDAR is shown in 表 7-24.

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This register is the address/data MMD register. ADDAR is used in conjunction with REGCR register (0x000D) to provide the access by indirect read/write mechanism to the extended register set.

表 7-24. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDR_DATA	R/W	0x0	If register 13.15:14 = 00, holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data register

7.6.1.14 1KSCR Register (Offset = 0xF) [Reset = 0xF000]

1KSCR is shown in 表 7-25.

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表 7-25. 1KSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	G_1000BX_FD	R	0x1	1 = PHY supports 1000Base-X Full Duplex capability 0 = PHY does not support 1000Base-X Full Duplex capability
14	G_1000BX_HD	R	0x1	1 = PHY supports 1000Base-X Half Duplex capability 0 = PHY does not support 1000Base-X Half Duplex capability
13	G_1000BT_FD	R	0x1	1 = PHY supports 1000Base-T Full Duplex capability 0 = PHY does not support 1000Base-T Full Duplex capability
12	G_1000BT_HD	R	0x1	1 = PHY supports 1000Base-T Half Duplex capability 0 = PHY does not support 1000Base-T Half Duplex capability
11-0	RESERVED	R	0x0	Reserved

7.6.1.15 PHY_CONTROL Register (Offset = 0x10) [Reset = 0x5048]

PHY_CONTROL is shown in 表 7-26.

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表 7-26. PHY_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TX_FIFO_DEPTH	R/W	0x1	FIFO is enabled only in the following modes: 1000BaseT + GMII 0x0 = 3 bytes/nibbles (1000Mbps/Other Speeds) 0x1 = 4 bytes/nibbles (1000Mbps/Other Speeds) 0x2 = 6 bytes/nibbles (1000Mbps/Other Speeds) 0x3 = 8 bytes/nibbles (1000Mbps/Other Speeds)
13-12	RX_FIFO_DEPTH	R/W	0x1	FIFO is enabled only when SGMII is used 0x0 = 3 bytes/nibbles (1000Mbps/Other Speeds) 0x1 = 4 bytes/nibbles (1000Mbps/Other Speeds) 0x2 = 6 bytes/nibbles (1000Mbps/Other Speeds) 0x3 = 8 bytes/nibbles (1000Mbps/Other Speeds)
11	RESERVED	R	0x0	Reserved
10	FORCE_LINK_GOOD	R/W	0x0	0x0 = Do Normal operation 0x1 = Force Link OK if speed is 1G
9-8	POWER_SAVE_MODE	R/W	0x0	0x0 = Normal mode 0x1 = Reserved 0x2 = Active Sleep mode 0x3 = Passive Sleep mode
7	RESERVED	R	0x0	Reserved
6-5	MDI_CROSSOVER_MODE	R/W	0x2	Default depends on strap 0x0 = Manual MDI configuration 0x1 = Manual MDI-X configuration 0xA = Enable automatic crossover 0xB = Enable automatic crossover
4	DISABLE_CLK_125	R/W	0x0	0x0 = Enable CLK125 0x1 = Disable CLK125
3	TEST_CLKOUT_SEL	R/W	0x1	0x0 = Test clock is output through GMII_RX_CLK pin 0x1 = Test clock is output through CLK_125_OUT pin
2	RESERVED	R	0x0	Reserved
1	LINE_DRIVER_INV_EN	R/W	0x0	This bit is not applicable in Mirror mode 0x0 = Do not Invert LD transmission 0x1 = Invert LD transmission
0	DISABLE_JABBER	R/W	0x0	0x0 = Enable Jabber function 0x1 = Disable Jabber function

7.6.1.16 PHY_STATUS Register (Offset = 0x11) [Reset = 0x0]

PHY_STATUS is shown in 表 7-27.

Return to the Summary Table.

表 7-27. PHY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SPEED_SEL	R	0x0	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved
13	DUPLEX_MODE_ENV	R	0x0	1 = Full duplex 0 = Half duplex
12	PAGE_RECEIVED_2	RC	0x0	1 = Page received 0 = Page not received THIS BIT IS LH (Latched-High)
11	SPEED_DUPLEX_RESOLVED	R	0x0	1 = Auto-Negotiation completed or disabled 0 = Auto-Negotiation enabled and not completed
10	LINK_STATUS_2	R	0x0	1 = Link is up 0 = Link is down
9	MDI_X_MODE_CD_1	R	0x0	1 = MDI-X 0 = MDI
8	MDI_X_MODE_AB_1	R	0x0	1 = MDI-X 0 = MDI
7	SPEED_OPT_STATUS	R	0x0	1 = Auto-Negotiation is currently being performed with Speed Optimization masking 1000BaseT abilities (Valid only during Auto-Negotiation) 0 = Auto-Negotiation is currently being performed without Speed Optimization

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表 7-27. PHY_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	SLEEP_MODE	R	0x0	1 = Sleep 0 = Active
5-2	WIRE_CROSS	R	0x0	Indicates channels [D,C,B,A] polarity in 1000BT link 1 = Channel polarity is reversed 0 = Channel polarity is normal
1	DATA_POLARITY	R	0x0	1 = 10BT is in normal polarity 0 = 10BT is in reversed polarity
0	JABBER_DTCT_2	R	0x0	1 = Jabber 0 = No Jabber

7.6.1.17 INTERRUPT_MASK Register (Offset = 0x12) [Reset = 0x0]

INTERRUPT_MASK is shown in 表 7-28.

Return to the Summary Table.

This register implements the Interrupt PHY Specific Control register. The individual interrupt events must be enabled by setting bits in the MII Interrupt Control Register (MICR). If the corresponding enable bit in the register is set, an interrupt is generated if the event occurs.

表 7-28. INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTONEG_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
14	SPEED_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
13	DUPLEX_MODE_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
12	PAGE_RECEIVED_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
11	AUTONEG_COMP_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
10	LINK_STATUS_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
9	EEE_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
8	FALSE_CARRIER_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
7	ADC_FIFO_OVF_UNF_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
6	MDI_CROSSOVER_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
5	SPEED_OPT_EVENT_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
4	SLEEP_MODE_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
3	WOL_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
2	XGMII_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
1	POLARITY_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
0	JABBER_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt

7.6.1.18 INTERRUPT_STATUS Register (Offset = 0x13) [Reset = 0x0]

INTERRUPT_STATUS is shown in 表 7-29.

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This register contains event status for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. The status indications in this register will be set even if the interrupt is not enabled.

表 7-29. INTERRUPT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTONEG_ERR	RC	0x0	1 = Auto-Negotiation error has occurred 0 = Auto-Negotiation error has not occurred THIS BIT IS LH (Latched-High)
14	SPEED_CHNG	RC	0x0	1 = Link speed has changed 0 = Link speed has not changed THIS BIT IS LH (Latched-High)
13	DUPLEX_MODE_CHNG	RC	0x0	1 = Duplex mode has changed 0 = Duplex mode has not changed THIS BIT IS LH (Latched-High)
12	PAGE_RECEIVED	RC	0x0	1 = Page has been received 0 = Page has not been received THIS BIT IS LH (Latched-High)
11	AUTONEG_COMP	RC	0x0	1 = Auto-Negotiation has completed 0 = Auto-Negotiation has not completed THIS BIT IS LH (Latched-High)
10	LINK_STATUS_CHNG	RC	0x0	1 = Link status has changed 0 = Link status has not changed THIS BIT IS LH (Latched-High)
9	EEE_ERR_STATUS	R	0x0	1 = EEE error has been detected
8	FALSE_CARRIER	RC	0x0	1 = Enable interrupt 0 = Disable interrupt THIS BIT IS LH (Latched-High)
7	ADC_FIFO_OVF_UNF	RC	0x0	1 = Overflow / underflow has been detected in one of ADC's FIFOs THIS BIT IS LH (Latched-High)
6	MDI_CROSSOVER_CHNG	RC	0x0	1 = MDI crossover has changed 0 = MDI crossover has not changed THIS BIT IS LH (Latched-High)
5	SPEED_OPT_EVENT	RC	0x0	1 = MDI crossover has changed 0 = MDI crossover has not changed THIS BIT IS LH (Latched-High)
4	SLEEP_MODE_CHNG	RC	0x0	1 = Sleep mode has changed 0 = Sleep mode has not changed THIS BIT IS LH (Latched-High)
3	WOL_STATUS	R	0x0	1 = WoL (or pattern) packet has been received
2	XGMII_ERR_STATUS	R	0x0	1 = Overflow / underflow has been detected in one of GMII / RGMII buffers NOTE: this indication have issue, recommend to not put on DS, unless proven otherwise on the lab, CDDS #475
1	POLARITY_CHNG	R	0x0	1 = Data polarity has changed 0 = Data polarity has not changed THIS BIT IS LH (Latched-High)
0	JABBER	RC	0x0	1 = Jabber detected 0 = Jabber not detected THIS BIT IS LH (Latched-High)

7.6.1.19 GEN_CFG2 Register (Offset = 0x14) [Reset = 0x2947]

GEN_CFG2 is shown in 表 7-30.

Return to the Summary Table.

表 7-30. GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PD_DETECT_EN	RH/WtoP	0x0	0x0 = Disable PD detection 0x1 = Enable PD (Powered Device) detection
14	RESERVED	R	0x0	Reserved
13	INTERRUPT_POLARITY	R/W	0x1	0x0 = Interrupt pin is active high 0x1 = Interrupt pin is active low
12	RESERVED	R	0x0	Reserved

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表 7-30. GEN_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-10	SPEED_OPT_ATTEMPT_CNT	R/W	0x2	Selects the number of 1G link establishment attempt failures prior to performing Speed Optimization: 0x0 = 1 attempt 0x1 = 2 attempts 0x2 = 4 attempts 0x3 = 8 attempts
9	SPEED_OPT_EN	R/W	0x0	0x0 = Disable Speed Optimization 0x1 = Enable Speed Optimization
8	SPEED_OPT_ENHANCED_EN	R/W	0x1	In enhanced mode, speed is optimized if energy is not detected in channels C and D 0x0 = Disable Speed Optimization enhanced mode 0x1 = Enable Speed Optimization enhanced mode
7	RESERVED	R	0x0	Reserved
6	SPEED_OPT_10M_EN	R/W	0x1	0x0 = Disable speed optimization to 10M 0x1 = Enable speed optimization to 10M (If link establishments of 1G and 100M fail)
5-4	MII_CLK_CFG	R/W	0x0	Selects frequency of GMII_TX_CLK in 1G mode: 0x0 = 2.5Mhz 0x1 = 25Mhz 0x2 = Disabled 0x3 = Disabled
3	COL_FD_EN	R/W	0x0	0x0 = Disable COL indication in full duplex mode 0x1 = Enable COL indication in full duplex mode
2	LEGACY_CODING_TXMODE_EN	R/W	0x1	0x0 = Disable automatic selection of Legacy scrambler mode in 1G, Master mode 0x1 = Enable automatic selection of Legacy scrambler mode in 1G, Master mode
1	MASTER_SEMI_CROSS_EN	R/W	0x1	0x0 = Disable semi-cross mode in 1G Master mode 0x1 = Enable semi-cross mode in 1G Master mode
0	SLAVE_SEMI_CROSS_EN	R/W	0x1	0x0 = Disable semi-cross mode in 1G Slave mode 0x1 = Enable semi-cross mode in 1G Slave mode

7.6.1.20 RX_ERR_CNT Register (Offset = 0x15) [Reset = 0x0]

RX_ERR_CNT is shown in 表 7-31.

Return to the Summary Table.

表 7-31. RX_ERR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX_ERROR_COUNT	R/W1C	0x0	Receive Error Counter

7.6.1.21 BIST_CONTROL Register (Offset = 0x16) [Reset = 0x0]

BIST_CONTROL is shown in 表 7-32.

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This register is used for Build-In Self Test (BIST) configuration. The BIST functionality provides Pseudo Random Bit Stream (PRBS) mechanism including packet generation generator and checker. Selection of the exact loopback point in the signal chain is also done in this register.

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表 7-32. BIST_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	PACKET_GEN_EN_3:0	R/W	0x0	These bits along controls PRBS generator. Other values are not applicable. 0x0 = Disable PRBS 0xF = Enable Continuous PRBS
11-10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	REV_LOOP_RX_DATA_CTRL	R/W	0x0	Reverse Loopback Receive Data Control: This bit may only be set in Reverse Loopback mode 0x0 = Suppress RX packets to MAC in reverse loop 0x1 = Send RX packets to MAC in reverse loop
6	MII_LOOP_TX_DATA_CTRL	R/W	0x0	MII Loopback Transmit Data Control: This bit may only be set in MII Loopback mode 0x0 = Suppress data to MDI in MII loop 0x1 = Transmit data to MDI in MII loop
5-2	LOOP_TX_DATA_MIX	R/W	0x0	Loopback Mode Select: PCS loopback must be disabled (Bits[1:0] = 00) 0x0 = No Loopback 0x1 = Digital Loopback 0x2 = Analog Loopback 0x4 = External Loopback 0x8 = Reverse Loopback
1-0	LOOPBACK_MODE	R/W	0x0	PCS Loopback Select When configured in 1000Base-T x1b = Loop before 1000Base-T signal processing. When configured in 100Base-TX 0x0 = See bits [5:2] 01b = Loop before scrambler 10b = Loop after scrambler, before MLT3 encoder 11b = Loop after MLT3 encoder

7.6.1.22 GEN_STATUS2 Register (Offset = 0x17) [Reset = 0x40]

GEN_STATUS2 is shown in 表 7-33.

Return to the Summary Table.

表 7-33. GEN_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PD_PASS	RC	0x0	1b = PD (Powered Device) has been successfully detected 0b = PD has not been detected
14	PD_PULSE_DET_ZERO	RC	0x0	1b = PD detection mechanism has received no signal 0b = PD detection mechanism has received signal
13	PD_FAIL_WD	RC	0x0	1b = PD detection mechanism watchdog has expired 0b = PD detection mechanism watchdog has not expired
12	PD_FAIL_NON_PD	RC	0x0	1b = PD detection mechanism has detected a non-powered device 0b = PD detection mechanism has not detected a non-powered device
11	PRBS_LOCK	R	0x0	1b = PRBS checker is locked sync) on received byte stream 0b = PRBS checker is not locked
10	PRBS_SYNC_LOSS	R	0x0	1b = PRBS checker has lost sync 0b = PRBS checker has not lost sync LH - clear on read register
9	PKT_GEN_BUSY	R	0x0	1b = Packet generator is in process 0b = Packet generator is not in process
8	SCR_MODE_MASTER_1G	R	0x0	1b = 1G PCS (master) is in legacy encoding mode 0b = 1G PCS (master) is in normal encoding mode
7	SCR_MODE_SLAVE_1G	R	0x0	1b = 1G PCS (slave) is in legacy encoding mode 0b = 1G PCS (slave) is in normal encoding mode

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表 7-33. GEN_STATUS2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CORE_PWR_MODE	R	0x1	1b = Core is in normal power mode 0b = Core is powered down or in sleep mode
5-0	RESERVED	R	0x0	Reserved

7.6.1.23 LEDS_CFG1 Register (Offset = 0x18) [Reset = 0x6150]

LEDS_CFG1 is shown in 表 7-34.

Return to the Summary Table.

表 7-34. LEDS_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LED_GPIO_SEL	R/W	0x6	Source of GPIO LED, same as bits 3:0
11-8	LED_2_SEL	R/W	0x1	Source of LED_2 (LED 2) , same as bits 3:0
7-4	LED_1_SEL	R/W	0x5	Source of LED_1 (LED 1) , same as bits 3:0
3-0	LED_0_SEL	R/W	0x0	Source of LED_0 (LED 0) 0x0 = link OK 0x1 = RX/TX activity 0x2 = TX activity 0x3 = RX activity 0x4 = collision detected 0x5 = 1000BT link is up 0x6 = 100 BTX link is up 0x7 = 10BT link is up 0x8 = 10/100BT link is up 0x9 = 100/1000BT link is up 0xA = full duplex 0xB = link OK + blink on TX/RX activity 0xC = NA 0xD = RX_ER or TX_ER 0xE = RX_ER

7.6.1.24 LEDS_CFG2 Register (Offset = 0x19) [Reset = 0x4444]

LEDS_CFG2 is shown in 表 7-35.

Return to the Summary Table.

表 7-35. LEDS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	LED_GPIO_POLARITY	R/W	0x1	GPIO LED polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
13	LED_GPIO_DRV_VAL	R/W	0x0	If bit #12 is set, this is the value of GPIO LED
12	LED_GPIO_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #13 0x0 = LED_GPIO is in normal operation mode 0x1 = Force the value of LED_GPIO
11	RESERVED	R	0x0	Reserved
10	LED_2_POLARITY	R/W	0x1	LED_2 polarity. Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
9	LED_2_DRV_VAL	R/W	0x0	If bit #8 is set, this is the value of LED_2

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表 7-35. LEDS_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	LED_2_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #9 0x0 = LED_2 is in normal operation mode 0x1 = Drive the value of LED_2
7	RESERVED	R	0x0	Reserved
6	LED_1_POLARITY	R/W	0x1	LED_1 polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
5	LED_1_DRV_VAL	R/W	0x0	If bit #4 is set, this is the value of LED_1
4	LED_1_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #5 0x0 = LED_1 is in normal operation mode 0x1 = Drive the value of LED_1
3	RESERVED	R	0x0	Reserved
2	LED_0_POLARITY	R/W	0x1	LED_0 polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
1	LED_0_DRV_VAL	R/W	0x0	If bit #1 is set, this is the value of LED_0
0	LED_0_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #1 0x0 = LED_0 is in normal operation mode 0x1 = Drive the value of LED_0

7.6.1.25 LEDS_CFG3 Register (Offset = 0x1A) [Reset = 0x2]

LEDS_CFG3 is shown in 表 7-36.

Return to the Summary Table.

表 7-36. LEDS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0x0	Reserved
2	LEDS_BYPASS_STRETCHING	R/W	0x0	0b = Normal Operation 1b = Bypass LEDs stretching
1-0	LEDS_BLINK_RATE	R/W	0x2	00b = 20Hz (50mSec) 01b = 10Hz (100mSec) 10b = 5Hz (200mSec) 11b = 2Hz (500mSec)

7.6.1.26 GEN_CFG4 Register (Offset = 0x1E) [Reset = 0x2]

GEN_CFG4 is shown in 表 7-37.

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表 7-37. GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	CFG_FAST_ANEG_EN	R/W	0x0	Enable Fast ANEG mode
13-12	CFG_FAST_ANEG_SEL_VAL	R/W	0x0	when Fast ANEG mode enabled, value will select short timer duration 0x0 will be the shortest timers config and 0x2 the longest
11	CFG_ANEG_ADV_FD_EN	R/W	0x0	this but enables to declare FD also in parallel detect link, the IEEE define on parallel detect to always declare HD, this bit allows also to declare FD in this scenario
10	RESTART_STATUS_BITS_EN	R/W	0x0	reset enable 1b = clear all the phy status bits (part of register 0x11) 0b = do not clear the status bit

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表 7-37. GEN_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
9	CFG_ROBUST_AMDIX_EN	R/W	0x0	Enable Robust Auto MDI/MDIX resolution
8	CFG_FAST_AMDIX_EN	R/W	0x0	Enabe Fast Auto MDI-X mode
7	INT_OE	R/W	0x0	Interrupt Output Enable: 1b = INTN/PWDNN Pad is an Interrupt Output 0b = INTN/PWDNN Pad in an Power Down Input
6	FORCE_INTERRUPT	R/W	0x0	1b = Assert interrupt pin 0b = Normal interrupt mode
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	FORCE_1G_AUTONEG_EN	R/W	0x0	1b = Invoke Auto-Negotiation with only 1G advertised when manual speed in register 0 is 1G 0b = Do not invoke Auto-Negotiation when manual speed in register 0 is 1G
2	TDR_FAIL	R	0x0	
1	TDR_DONE	R	0x1	
0	TDR_START	RH/WtoP	0x0	1b = Start TDR 0b = TDR Completed

7.6.1.27 GEN_CTRL Register (Offset = 0x1F) [Reset = 0x0]

GEN_CTRL is shown in 表 7-38.

Return to the Summary Table.

表 7-38. GEN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SW_RESET	RH/WtoP	0x0	Software Reset This will reset the PHY and return registers to their default values. Registers controlled via strap pins will return back to their last strapped values. 0x0 = Normal mode 0x1 = Reset PHY
14	SW_RESTART	RH/WtoP	0x0	Soft Restart Restarts the PHY without affecting registers. 0x0 = Normal Operation 0x1 = Software Reset
13	RESERVED	R	0x0	Reserved
12-7	RESERVED	R	0x0	Reserved
6-0	RESERVED	R	0x0	Reserved

7.6.1.28 ANALOG_TEST_CTRL Register (Offset = 0x25) [Reset = 0x480]

ANALOG_TEST_CTRL is shown in 表 7-39.

Return to the Summary Table.

表 7-39. ANALOG_TEST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-10	TM7_PULSE_SEL	R/W	0x1	Selects pulse amplitude and polarity for Test Mode 7 (See register 0x9): 00b = +2 01b = -2 10b = +1 11b = -1
9	EXTND_TM7_100BT_MSB	R/W	0x0	MSB of configurable length for 100BT extended TM7 For 100BT Test Mode: repetitive sequence of "1" with configurable number of "0". Bits { 9,[3:0] } define the number of "0" to follow the "1", from 1 to 31. 0,0001 - 1,1111 : single "0" to 31 zeros. 0,0000 - clear the shiftreg.

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表 7-39. ANALOG_TEST_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	EXTND_TM7_100BT_EN	R/W	0x0	Enable extended TM7 for 100M. NOTE1: bit 4 must be "0" for 100BT TestMode. NOTE2: 100BT testmode must be Clear before appling new Value. e.g, one need to write 0x0 before configuring new value. NOTE3: use FORCE100 for 100BT testing, via Reg0x0.
7-5	STIM_CH_SEL	R/W	0x4	Selects the channel(s) that outputs the test mode: If bit #7 is set, test mode is driven to all channels. If bit #7 is cleared, test mode is driven according to bits 6:5 - 00b = Channel A 01b = Channel B 10b = Channel C 11b = Channel D
4-0	ANALOG_TEST	R/W	0x0	Bit [4] enables 10BaseT test modes. Bits [3:0] select the 10BaseT test pattern, as follows: To operate extended TM7 for 100BT, bits 3:0 shall be configured as well - more details in bit #9 0000b = Single NLP 0001b = Single Pulse 1 0010b = Single Pulse 0 0011b = Repetitive 1 0100b = Repetitive 0 0101b = Preamble (repetitive "10") 0110b = Single 1 followed by TP_IDLE 0111b = Single 0 followed by TP_IDLE 1000b = Repetitive "1001" sequence 1001b = Random 10Base-T data 1010b = TP_IDLE_00 1011b = TP_IDLE_01 1100b = TP_IDLE_10 1101b = TP_IDLE_11 0110b = Proprietary T.M for amplitude, RFT, DCD and template for FT on tester (1000) ---> need to write register 0 0x2000

7.6.1.29 GEN_CFG_ENH_AMIX Register (Offset = 0x2C) [Reset = 0x141F]

GEN_CFG_ENH_AMIX is shown in 表 7-40.

Return to the Summary Table.

表 7-40. GEN_CFG_ENH_AMIX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-9	CFG_FLD_WINDW_CNT	R/W	0xA	Counter to define the window to look for fast link down criteria, default 10 µs
8-4	CFG_FAST_AMDIX_VAL	R/W	0x1	Timer of the mdi/x switch countering force 100m fast amdix mode, very fast as it need only to allow far end to detect energy ~4ms in default
3-0	CFG_ROBUST_AMDIX_VAL	R/W	0xF	The value of the timer that switch mdi/x in robust mode, this should be long timer to allow far end to still do parallel detect with the IEEE ANEG timers... default ~0.5s

7.6.1.30 GEN_CFG_FLD Register (Offset = 0x2D) [Reset = 0x0]

GEN_CFG_FLD is shown in 表 7-41.

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表 7-41. GEN_CFG_FLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_FORCE_DROP_LINK_EN	R/W	0x0	Drop link (stop transmitting) when no signal is received
14	FLD_BYPASS_MAX_WAIT_TIMER	R/W	0x0	If set, MAX_WAIT_TIMER is skipped (and therefore link is dropped faster)
13	SLICER_OUT_STUCK	R	0x0	indicate slicer)out_stuck status
12-8	FLD_STATUS	R	0x0	Fast link down status LH - clear on read register
7-5	RESERVED	R	0x0	Reserved

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表 7-41. GEN_CFG_FLD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4-0	CFG_FAST_LINK_DOWN_MODES	R/W	0x0	5 bits for different fast link down option (can all work simultaniously): bit [0] - energy lost bit [1] - mse bit [2] - mlt3 errors bit [3] - rx_err bit [4] - descrambler sync loss

7.6.1.31 GEN_CFG_FLD_THR Register (Offset = 0x2E) [Reset = 0x221]

GEN_CFG_FLD_THR is shown in 表 7-42.

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表 7-42. GEN_CFG_FLD_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-8	ENERGY_WINDOW_LEN_FLD	R/W	0x2	window length in FLD energy lost mode for energy detection accumulator
7	RESERVED	R	0x0	Reserved
6-4	ENERGY_ON_FLD_THR	R/W	0x2	energy lost threshold for FLD energy lost mode. energy_detected indication will be asserted when energy detector accumulator exceeds this threshold.
3	RESERVED	R	0x0	Reserved
2-0	ENERGY_LOST_FLD_THR	R/W	0x1	energy lost threshold for FLD energy lost mode energy_lost indication will be asserted if energy detector accumulator falls below this threshold.

7.6.1.32 GEN_CFG3 Register (Offset = 0x31) [Reset = 0x0]

GEN_CFG3 is shown in 表 7-43.

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表 7-43. GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11-9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R	0x0	Reserved
6-5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PORT_MIRRORING_MODE	R/W	0x0	Port mirroring mode: 0 - Disabled 1 - Enabled

7.6.1.33 RGMII_CTRL Register (Offset = 0x32) [Reset = 0xD0]

RGMII_CTRL is shown in 表 7-44.

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表 7-44. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	RESERVED	R	0x0	Reserved
7	RESERVED	R/W	0x1	unused, default value should remain unchanged.
6-5	RGMII_RX_HALF_FULL_THR	R/W	0x2	RGMII RX sync FIFO half full threshold 2 lsbs [1:0], msb [2] in reg 0x33 In the RX our default is recovered mode (can change in reg 0x0060 #4 below) In recovered mode we can reduce the threshold in from 2 to 1, this will save 8 ns in 1G, and 40/400 in 100/10M
4-3	RGMII_TX_HALF_FULL_THR	R/W	0x2	RGMII TX sync FIFO half full threshold 2 lsbs [1:0], - the msb is on reg 0x33 - [2]
2	SUPPRESS_TX_ERR_EN	R/W	0x0	
1	RGMII_TX_CLK_DELAY	R/W	0x0	RGMII Transmit Clock Delay 0x0 = RGMII transmit clock is shifted with respect to transmit data. 0x1 = RGMII transmit clock is aligned with respect to transmit data.
0	RGMII_RX_CLK_DELAY	R/W	0x0	RGMII Receive Clock Delay 0x0 = RGMII receive clock is shifted with respect to receive data. 0x1 = RGMII transmit clock is aligned with respect to receive data.

7.6.1.34 RGMII_CTRL2 Register (Offset = 0x33) [Reset = 0x0]

RGMII_CTRL2 is shown in 表 7-45.

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表 7-45. RGMII_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4	RGMII_AF_BYPASS_EN	R/W	0x0	RGMII Async FIFO Bypass Enable: 1 = Enable RGMII Async FIFO Bypass. 0 = Normal operation.
3	RGMII_AF_BYPASS_DLY_EN	R/W	0x0	RGMII Async FIFO Bypass Delay Enable: 1 = Delay RX_CLK when operating in 10/100 with RGMII. 0 = Normal operation
2	LOW_LATENCY_10_100_EN	R/W	0x0	Low Latency 10/100 Enable: 1 = Enable low latency in 10/100 operation. 0 = Normal operation.
1	RESERVED	R	0x0	Reserved
0	RESERVED	R	0x0	Reserved

7.6.1.35 PRBS_TX_CHK_CTRL Register (Offset = 0x39) [Reset = 0x0]

PRBS_TX_CHK_CTRL is shown in 表 7-46.

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表 7-46. PRBS_TX_CHK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved

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表 7-46. PRBS_TX_CHK_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-7	PRBS_TX_CHK_ERR_CNT	R	0x0	Holds number of errored bytes that received by the PRBS TX checker. When TX PRBS Count Mode (see bit [1]) set to 0, count stops on 0xFF. Notes: Writing bit 7 generates a lock signal for the PRBS TX counters. Writing bit 8 generates a lock and clear signal for the PRBS TX counters
6	RESERVED	R	0x0	Reserved
5	PRBS_TX_CHK_SYNC_LOSS	R	0x0	1b = PRBS TX checker has lost sync 0b = PRBS TX checker has not lost sync This bit is LH
4	PRBS_TX_CHK_LOCK_STS	R	0x0	1b = PRBS TX checker is locked on received byte stream 0b = PRBS TX checker is not locked
3	RESERVED	R	0x0	Reserved
2	PRBS_TX_CHK_BYTE_CNT_OVF	R	0x0	If set, bytes counter reached overflow
1	PRBS_TX_CHK_CNT_MODE	R/W	0x0	PRBS Checker Mode 1b = Continuous mode 0b = Single Mode.
0	PRBS_TX_CHK_EN	R/W	0x0	If set, PRBS TX checker is enabled (PRBS TX checker is used in external reverse loop)

7.6.1.36 PRBS_TX_CHK_BYTE_CNT Register (Offset = 0x3A) [Reset = 0x0]

PRBS_TX_CHK_BYTE_CNT is shown in 表 7-47.

Return to the Summary Table.

表 7-47. PRBS_TX_CHK_BYTE_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS_TX_CHK_BYTE_CNT	R	0x0	Holds number of total bytes that received by the PRBS TX checker. Value in this register is locked when write is done to register PRBS_TX_CHK_CTRL bit[7]or bit[8]. When PRBS Count Mode set to zero, count stops on 0xFFFF (see register 0x0016)

7.6.1.37 G_100BT_REG0 Register (Offset = 0x43) [Reset = 0x0]

G_100BT_REG0 is shown in 表 7-48.

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表 7-48. G_100BT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	RESERVED	R	0x0	Reserved
10-7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved
2	RESERVED	R	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	FAST_RX_DV	R/W	0x0	Enable Fast RX_DV for low latency in 100Mbps mode. 0x0 = Fast rx dv disable 0x1 = Fast rx dv enable

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7.6.1.38 G_1000BT_PMA_STATUS Register (Offset = 0x55) [Reset = 0x0]

G_1000BT_PMA_STATUS is shown in 表 7-49.

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表 7-49. G_1000BT_PMA_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7-4	PMA_MASTER_FIFO_CTRL	R	0x0	1000-Mb SFD Variation in Master Mode
3-0	PMA_SLAVE_FIFO_CTRL	R	0x0	1000-Mb SFD Variation in Slave Mode

7.6.1.39 STRAP_STS Register (Offset = 0x6E) [Reset = 0x0]

STRAP_STS is shown in 表 7-50.

Return to the Summary Table.

表 7-50. STRAP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	STRAP_LINK_LOSS_PASS_THRU	R	0x0	Link Loss Pass Through Enable Strap 0x0 = Enable 0x1 = Disable
12	STRAP_MIRROR_EN	R	0x0	Mirror Mode Enable Strap. 0x0 = Disable 0x1 = Enable
11-9	STRAP_OPMODE	R	0x0	OPMODE Strap 0x0 = RGMII To Copper
8-4	STRAP_PHY_ADD	R	0x0	PHY Address Strap
3-2	STRAP_ANEGSEL	R	0x0	Auto Negotiation Mode Select Strap. Refer to Strap Configuration Section
1	STRAP_ANEG_EN	R	0x0	Auto Negotiation Enable Strap 0x0 = Enable 0x1 = Disable
0	STRAP_RGMII_MII_SEL	R	0x0	RGMII to MII Enable Strap 0x0 = RGMII mode 0x1 = MII Mode

7.6.1.40 DBG_PRBS_BYTE_CNT Register (Offset = 0x71) [Reset = 0x0]

DBG_PRBS_BYTE_CNT is shown in 表 7-51.

Return to the Summary Table.

表 7-51. DBG_PRBS_BYTE_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS_BYTE_CNT	R	0x0	Holds number of total bytes that received by the PRBS checker. Value in this register is locked when write is done to register DBG_PRBS_ERR_CNT bit[0] or bit[1]. When PRBS Count Mode set to zero, count stops on 0xFFFF (see register 0x0016)

7.6.1.41 DBG_PRBS_ERR_CNT Register (Offset = 0x72) [Reset = 0x0]

DBG_PRBS_ERR_CNT is shown in 表 7-52.

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表 7-52. DBG_PRBS_ERR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10	PRBS_PKT_CNT_OVF	R	0x0	If set, packet counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1of this register
9	PRBS_BYTE_CNT_OVF	R	0x0	If set, bytes counter reached overflow Overflow is cleared when PRBS counters are cleared - done by setting bit #1of this register
8	RESERVED	R	0x0	Reserved
7-0	PRBS_ERR_CNT	R	0x0	Holds number of errored bytes that received by the PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] (see bellow). When PRBS Count Mode set to zero, count stops on 0xFF (see register 0x0016) Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

7.6.1.42 DBG_PKT_LEN_PRBS Register (Offset = 0x7B) [Reset = 0x5DC]

DBG_PKT_LEN_PRBS is shown in 表 7-53.

Return to the Summary Table.

表 7-53. DBG_PKT_LEN_PRBS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PKT_LEN_PRBS	R/W	0x5DC	Length (in bytes) of PRBS packets, this effect the PRBS packets and not

7.6.1.43 ANA_RGMII_DLL_CTRL Register (Offset = 0x86) [Reset = 0x77]

ANA_RGMII_DLL_CTRL is shown in 表 7-54.

Return to the Summary Table.

表 7-54. ANA_RGMII_DLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	DLL_EN_FORCE_VAL	R/W	0x0	If dll_en_force_en is set, this is the value of DLL_EN
8	DLL_EN_FORCE_CTRL	R/W	0x0	Force DLL_EN value
7-4	DLL_TX_DELAY_CTRL_SL	R/W	0x7	Steps of 250ps, affects the CLK_90 output. - same behavior as bit [3:0]
3-0	DLL_RX_DELAY_CTRL_SL	R/W	0x7	Steps of 250ps, affects the CLK_90 output. b[3], b[2], b[1], b[0], shift, mode please note - the actual delay is also effected by the shift mode in reg 0x32 0x3 = 1.0ns, Shift 0x5 = 1.5ns, Shift 0x7 = 2.0 ns, Shift(*) - default 0x9 = 2.5ns, Shift 0xB = 3.0 ns,Shift 0xD = 3.5ns, Shift 0xF = 0ns, Align(**)

7.6.1.44 ANA_PLL_PROG_PI Register (Offset = 0xC6) [Reset = 0x0]

ANA_PLL_PROG_PI is shown in 表 7-55.

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表 7-55. ANA_PLL_PROG_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_PROG_PI	R/W	0x0	

7.6.1.45 LOOPCR Register (Offset = 0xFE) [Reset = 0xE721]

LOOPCR is shown in 表 7-56.

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表 7-56. LOOPCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	FB_AEQ_CNT	R/W	0x7	AEQ max number of fallbacks
12-8	AEQ_MAX_STEP	R/W	0x7	The maximum step in aeq table
7-5	AEQ_STEP_SIZE	R/W	0x1	Increment step for aeq table
4-1	RESERVED	R	0x0	
0	AEQ_BEG	R/W	0x1	Starting index for aeq table 0x0 = near-end loopback 0x1 = normal operation

7.6.1.46 RXF_CFG Register (Offset = 0x134) [Reset = 0x0]

RXF_CFG is shown in 表 7-57.

Return to the Summary Table.

表 7-57. RXF_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	WOL_OUT_CLEAN	RH/WoP	0x0	If WOL out is in level mode in bit 8, writing to this bit will clear it.
10-9	WOL_OUT_STRETCH	R/W	0x0	If WOL out is in pulse mode in bit 8, this is the pulse length: 0x0 = 8 clock cycles 0x1 = 16 clock cycles 0x2 = 32 clock cycles 0x3 = 64 clock cycles
8	WOL_OUT_MODE	R/W	0x0	Mode of the wake up that goes to GPIO pin: 0x0 = Pulse Mode. 0x1 = Level Mode
7	ENHANCED_MAC_SUPPORT	R/W	0x0	Enables enhanced RX features. This bit should be set when using wakeup abilities, CRC check or RX 1588 indication
6	RESERVED	R	0x0	Reserved
5	RESERVED	R	0x0	Reserved
4	WAKE_ON_UCAST	R/W	0x0	If set, issue an interrupt upon reception of unicast packets
3	RESERVED	R	0x0	Reserved
2	WAKE_ON_BCAST	R/W	0x0	If set, issue an interrupt upon reception of broadcast packets
1	WAKE_ON_PATTERN	R/W	0x0	If set, issue an interrupt upon reception of a packet with configured pattern
0	WAKE_ON_MAGIC	R/W	0x0	If set, issue an interrupt upon reception of magic packet

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7.6.1.47 RXF_STATUS Register (Offset = 0x135) [Reset = 0x0]

RXF_STATUS is shown in 表 7-58.

Return to the Summary Table.

表 7-58. RXF_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7	SFD_ERR	RC	0x0	SFD Error Detected
6	BAD_CRC	RC	0x0	Bad CRC Packet Received
5	RESERVED	R	0x0	Reserved
4	UCAST_RCVD	RC	0x0	Unicast Packet Received
3	RESERVED	R	0x0	Reserved
2	BCAST_RCVD	RC	0x0	Broadcast Packet Received
1	PATTERN_RCVD	RC	0x0	Pattern Match Packet Received
0	MAGIC_RCVD	RC	0x0	Magic Packet Received

7.6.1.48 IO_MUX_CFG Register (Offset = 0x170) [Reset = X]

IO_MUX_CFG is shown in 表 7-59.

Return to the Summary Table.

表 7-59. IO_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12-8	CLK_O_SEL	R/W	0xC	Select clock output source 0x0 = Channel A receive clock 0x1 = Channel B receive clock 0x2 = Channel C receive clock 0x3 = Channel D receive clock 0x4 = Channel A receive clock divided by 5 0x5 = Channel B receive clock divided by 5 0x6 = Channel C receive clock divided by 5 0x7 = Channel D receive clock divided by 5 0x8 = Channel A transmit clock 0x9 = Channel B transmit clock 0xA = Channel C transmit clock 0xB = Channel D transmit clock 0xC = Reference clock (synchronous to XI input clock)
7	RESERVED	R	0x0	Reserved
6	CLK_O_DISABLE	R/W	X	Clock Out Disable 0x0 = Clock Out Enable 0x1 = Clock Out Disable
5	RESERVED	R	0x0	Reserved
4-0	MAC_IMPEDANCE_CTRL	R/W	0x10	Impedance Control for MAC I/Os: Output impedance approximate range from 35-70 Ω in 32 steps. Lowest being 11111 and highest being 00000. Range and Step size will vary with process. Default is set to 50 Ω by trim but the default register value can vary by process. Non default values of MAC I/O impedance can be used based on trace impedance. Mismatch between device and trace impedance can cause voltage overshoot and undershoot. For RGMII mode, this should be set to 35 Ω (set to 11111)

7.6.1.49 TDR_GEN_CFG1 Register (Offset = 0x180) [Reset = 0x752]

TDR_GEN_CFG1 is shown in 表 7-60.

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Return to the Summary Table.

表 7-60. TDR_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12	TDR_CH_CD_BYPASS	R/W	0x0	Bypass channel C and D in TDR tests
11	TDR_CROSS_MODE_DIS	R/W	0x0	If set, disable cross mode option - never check the cross (Listen only to the same channel you transmit)
10	TDR_NLP_CHECK	R/W	0x1	If set, check for NLPs during silence
9-7	TDR_AVG_NUM	R/W	0x6	Number Of TDR Cycles to Average: 000b = 1 TDR cycle 001b = 2 TDR cycles 010b = 4 TDR cycles 011b = 8 TDR cycles 100b = 16 TDR cycles 101b = 32 TDR cycles 110b = 64 TDR cycles (default) 111b = Reserved
6-4	TDR_SEG_NUM	R/W	0x5	Number of TDR segments to check
3-0	TDR_CYCLE_TIME	R/W	0x2	Number of micro-seconds in each TDR cycle

7.6.1.50 TDR_GEN_CFG2 Register (Offset = 0x181) [Reset = 0xC850]

TDR_GEN_CFG2 is shown in 表 7-61.

Return to the Summary Table.

表 7-61. TDR_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_SILENCE_TH	R/W	0xC8	Energy detection threshold
7-6	TDR_POST_SILENCE_TIME	R/W	0x1	timer for tdr to look for energy after TDR transaction, if energy detected this is fail tdr
5-4	TDR_PRE_SILENCE_TIME	R/W	0x1	timer for tdr to look for energy before starting , if energy detected this is fail tdr
3-0	RESERVED	R	0x0	Reserved

7.6.1.51 TDR_SEG_DURATION1 Register (Offset = 0x182) [Reset = 0x5326]

TDR_SEG_DURATION1 is shown in 表 7-62.

Return to the Summary Table.

表 7-62. TDR_SEG_DURATION1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-10	TDR_SEG_DURATION_SEG3	R/W	0x14	Number of 125MHz clock cycles to run for segment #3
9-5	TDR_SEG_DURATION_SEG2	R/W	0x19	Number of 125MHz clock cycles to run for segment #2
4-0	TDR_SEG_DURATION_SEG1	R/W	0x6	Number of 125MHz clock cycles to run for segment #1

7.6.1.52 TDR_SEG_DURATION2 Register (Offset = 0x183) [Reset = 0xA01E]

TDR_SEG_DURATION2 is shown in 表 7-63.

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表 7-63. TDR_SEG_DURATION2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_SEG_DURATION_SEG5	R/W	0xA0	Number of 125MHz clock cycles to run for segment #5
7-6	RESERVED	R	0x0	Reserved
5-0	TDR_SEG_DURATION_SEG4	R/W	0x1E	Number of 125MHz clock cycles to run for segment #4

7.6.1.53 TDR_GEN_CFG3 Register (Offset = 0x184) [Reset = 0xE976]

TDR_GEN_CFG3 is shown in 表 7-64.

Return to the Summary Table.

表 7-64. TDR_GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	TDR_FWD_SHADOW_SEG4	R/W	0xE	Indicates how much time to wait after max level before declaring we found a peak in segment #4
11-8	TDR_FWD_SHADOW_SEG3	R/W	0x9	Indicates how much time to wait after max level before declaring we found a peak in segment #3
7	RESERVED	R	0x0	Reserved
6-4	TDR_FWD_SHADOW_SEG2	R/W	0x7	Indicates how much time to wait after max level before declaring we found a peak in segment #2
3	RESERVED	R	0x0	Reserved
2-0	TDR_FWD_SHADOW_SEG1	R/W	0x6	Indicates how much time to wait after max level before declaring we found a peak in segment #1

7.6.1.54 TDR_GEN_CFG4 Register (Offset = 0x185) [Reset = 0x19CF]

TDR_GEN_CFG4 is shown in 表 7-65.

Return to the Summary Table.

表 7-65. TDR_GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-11	TDR_SDW_AVG_LOC	R/W	0x3	how much to look between segments to search average peak
10-9	RESERVED	R	0x0	Reserved
8	TDR_TX_TYPE_SEG5	R/W	0x1	the tx type (10/100) for this segment
7	TDR_TX_TYPE_SEG4	R/W	0x1	the tx type (10/100) for this segment
6	TDR_TX_TYPE_SEG3	R/W	0x1	the tx type (10/100) for this segment
5	TDR_TX_TYPE_SEG2	R/W	0x0	the tx type (10/100) for this segment
4	TDR_TX_TYPE_SEG1	R/W	0x0	the tx type (10/100) for this segment
3-0	TDR_FWD_SHADOW_SEG5	R/W	0xF	Indicates how much time to wait after max level before declaring we found a peak in segment #5

7.6.1.55 TDR_PEAKS_LOC_A_0_1 Register (Offset = 0x190) [Reset = 0x0]

TDR_PEAKS_LOC_A_0_1 is shown in 表 7-66.

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表 7-66. TDR_PEAKS_LOC_A_0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_A_1	R	0x0	Found peak location 1 in channel A
7-0	TDR_PEAKS_LOC_A_0	R	0x0	Found peak location 0 in channel A

7.6.1.56 TDR_PEAKS_LOC_A_2_3 Register (Offset = 0x191) [Reset = 0x0]

TDR_PEAKS_LOC_A_2_3 is shown in 表 7-67.

Return to the Summary Table.

表 7-67. TDR_PEAKS_LOC_A_2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_A_3	R	0x0	Found peak location 3 in channel A
7-0	TDR_PEAKS_LOC_A_2	R	0x0	Found peak location 2 in channel A

7.6.1.57 TDR_PEAKS_LOC_A_4_B_0 Register (Offset = 0x192) [Reset = 0x0]

TDR_PEAKS_LOC_A_4_B_0 is shown in 表 7-68.

Return to the Summary Table.

表 7-68. TDR_PEAKS_LOC_A_4_B_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_0	R	0x0	Found peak location 0 in channel B
7-0	TDR_PEAKS_LOC_A_4	R	0x0	Found peak location 4 in channel A

7.6.1.58 TDR_PEAKS_LOC_B_1_2 Register (Offset = 0x193) [Reset = 0x0]

TDR_PEAKS_LOC_B_1_2 is shown in 表 7-69.

Return to the Summary Table.

表 7-69. TDR_PEAKS_LOC_B_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_2	R	0x0	Found peak location 2 in channel B
7-0	TDR_PEAKS_LOC_B_1	R	0x0	Found peak location 1 in channel B

7.6.1.59 TDR_PEAKS_LOC_B_3_4 Register (Offset = 0x194) [Reset = 0x0]

TDR_PEAKS_LOC_B_3_4 is shown in 表 7-70.

Return to the Summary Table.

表 7-70. TDR_PEAKS_LOC_B_3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_4	R	0x0	Found peak location 4 in channel B
7-0	TDR_PEAKS_LOC_B_3	R	0x0	Found peak location 3 in channel B

7.6.1.60 TDR_PEAKS_LOC_C_0_1 Register (Offset = 0x195) [Reset = 0x0]

TDR_PEAKS_LOC_C_0_1 is shown in 表 7-71.

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表 7-71. TDR_PEAKS_LOC_C_0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_C_1	R	0x0	Found peak location 1 in channel C
7-0	TDR_PEAKS_LOC_C_0	R	0x0	Found peak location 0 in channel C

7.6.1.61 TDR_PEAKS_LOC_C_2_3 Register (Offset = 0x196) [Reset = 0x0]

TDR_PEAKS_LOC_C_2_3 is shown in 表 7-72.

Return to the Summary Table.

表 7-72. TDR_PEAKS_LOC_C_2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_C_3	R	0x0	Found peak location 3 in channel C
7-0	TDR_PEAKS_LOC_C_2	R	0x0	Found peak location 2 in channel C

7.6.1.62 TDR_PEAKS_LOC_C_4_D_0 Register (Offset = 0x197) [Reset = 0x0]

TDR_PEAKS_LOC_C_4_D_0 is shown in 表 7-73.

Return to the Summary Table.

表 7-73. TDR_PEAKS_LOC_C_4_D_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_0	R	0x0	Found peak location 0 in channel D
7-0	TDR_PEAKS_LOC_C_4	R	0x0	Found peak location 4 in channel C

7.6.1.63 TDR_PEAKS_LOC_D_1_2 Register (Offset = 0x198) [Reset = 0x0]

TDR_PEAKS_LOC_D_1_2 is shown in 表 7-74.

Return to the Summary Table.

表 7-74. TDR_PEAKS_LOC_D_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_2	R	0x0	Found peak location 2 in channel D
7-0	TDR_PEAKS_LOC_D_1	R	0x0	Found peak location 1 in channel D

7.6.1.64 TDR_PEAKS_LOC_D_3_4 Register (Offset = 0x199) [Reset = 0x0]

TDR_PEAKS_LOC_D_3_4 is shown in 表 7-75.

Return to the Summary Table.

表 7-75. TDR_PEAKS_LOC_D_3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_4	R	0x0	Found peak location 4 in channel D
7-0	TDR_PEAKS_LOC_D_3	R	0x0	Found peak location 3 in channel D

7.6.1.65 TDR_GEN_STATUS Register (Offset = 0x1A4) [Reset = 0x0]

TDR_GEN_STATUS is shown in 表 7-76.

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表 7-76. TDR_GEN_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	TDR_P_LOC_CROSS_MODE_D	R	0x0	Peak found at cross mode in channel D
10	TDR_P_LOC_CROSS_MODE_C	R	0x0	Peak found at cross mode in channel C
9	TDR_P_LOC_CROSS_MODE_B	R	0x0	Peak found at cross mode in channel B
8	TDR_P_LOC_CROSS_MODE_A	R	0x0	Peak found at cross mode in channel A
7	TDR_P_LOC_OVERFLOW_D	R	0x0	Total number of peaks in current segment reached max value of 5 in channel D
6	TDR_P_LOC_OVERFLOW_C	R	0x0	Total number of peaks in current segment reached max value of 5 in channel C
5	TDR_P_LOC_OVERFLOW_B	R	0x0	Total number of peaks in current segment reached max value of 5 in channel B
4	TDR_P_LOC_OVERFLOW_A	R	0x0	Total number of peaks in current segment reached max value of 5 in channel A
3	TDR_SEG1_HIGH_CROSS_D	R	0x0	Peak crossed high threshold of segment #1 in channel D
2	TDR_SEG1_HIGH_CROSS_C	R	0x0	peak crossed high threshold of segment #1 in channel C
1	TDR_SEG1_HIGH_CROSS_B	R	0x0	peak crossed high threshold of segment #1 in channel B
0	TDR_SEG1_HIGH_CROSS_A	R	0x0	peak crossed high threshold of segment #1 in channel A

7.6.1.66 TDR_PEAKS_SIGN_A_B Register (Offset = 0x1A5) [Reset = 0x0]

TDR_PEAKS_SIGN_A_B is shown in 表 7-77.

Return to the Summary Table.

表 7-77. TDR_PEAKS_SIGN_A_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	TDR_PEAKS_SIGN_B_4	R	0x0	found peaks sign 4 in channel B
8	TDR_PEAKS_SIGN_B_3	R	0x0	found peaks sign 3 in channel B
7	TDR_PEAKS_SIGN_B_2	R	0x0	found peaks sign 2 in channel B
6	TDR_PEAKS_SIGN_B_1	R	0x0	found peaks sign 1 in channel B
5	TDR_PEAKS_SIGN_B_0	R	0x0	found peaks sign 0 in channel B
4	TDR_PEAKS_SIGN_A_4	R	0x0	found peaks sign 4 in channel A
3	TDR_PEAKS_SIGN_A_3	R	0x0	found peaks sign 3 in channel A
2	TDR_PEAKS_SIGN_A_2	R	0x0	found peaks sign 2 in channel A
1	TDR_PEAKS_SIGN_A_1	R	0x0	found peaks sign 1 in channel A
0	TDR_PEAKS_SIGN_A_0	R	0x0	found peaks sign 0 in channel A

7.6.1.67 TDR_PEAKS_SIGN_C_D Register (Offset = 0x1A6) [Reset = 0x0]

TDR_PEAKS_SIGN_C_D is shown in 表 7-78.

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表 7-78. TDR_PEAKS_SIGN_C_D Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	TDR_PEAKS_SIGN_D_4	R	0x0	found peaks sign 4 in channel D
8	TDR_PEAKS_SIGN_D_3	R	0x0	found peaks sign 3 in channel D
7	TDR_PEAKS_SIGN_D_2	R	0x0	found peaks sign 2 in channel D
6	TDR_PEAKS_SIGN_D_1	R	0x0	found peaks sign 1 in channel D
5	TDR_PEAKS_SIGN_D_0	R	0x0	found peaks sign 0 in channel D
4	TDR_PEAKS_SIGN_C_4	R	0x0	found peaks sign 4 in channel C
3	TDR_PEAKS_SIGN_C_3	R	0x0	found peaks sign 3 in channel C
2	TDR_PEAKS_SIGN_C_2	R	0x0	found peaks sign 2 in channel C
1	TDR_PEAKS_SIGN_C_1	R	0x0	found peaks sign 1 in channel C
0	TDR_PEAKS_SIGN_C_0	R	0x0	found peaks sign 0 in channel C

7.6.1.68 MASK_SOFT_RST Register (Offset = 0x1D6) [Reset = 0xFFFF]

MASK_SOFT_RST is shown in 表 7-79.

Return to the Summary Table.

表 7-79. MASK_SOFT_RST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASK_SOFTRST	R/W	0xFFFF	Mask for inputs which can trigger internal soft reset recovery mechanism

7.6.1.69 MASK_EXTERNAL_INT Register (Offset = 0x1D7) [Reset = 0xFFFF]

MASK_EXTERNAL_INT is shown in 表 7-80.

Return to the Summary Table.

表 7-80. MASK_EXTERNAL_INT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	MASK_EXT_INT	R/W	0xFFFF	Mask for inputs which can trigger external recovery mechanism(INT_STTMCHNE_N)

7.6.1.70 SEU_STATUS_REG Register (Offset = 0x1D8) [Reset = 0x0]

SEU_STATUS_REG is shown in 表 7-81.

Return to the Summary Table.

表 7-81. SEU_STATUS_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	USE_LATER	R	0x0	Currently connected to 0. Will be used later.
11	PLL_LOCK_DET_FAIL	R	0x0	
10	SYS_CLK_FREQ_LOCK_LOST	R	0x0	status bit latched high when frequency lock is lost on sys_clk. Cleared when you write 1 to this bit or on POR or on pin reset
9	SYS_CLK_PPM_LOCK_LOST	R	0x0	status bit latched high when ppm lock is lost on sys_clk. Cleared when you write 1 to this bit or on POR or on pin reset
8	SYS_CLK_INACTIVE	R	0x0	status bit latched high when sys_clk is inactive. Cleared when you write 1 to this bit or on POR or on pin reset

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表 7-81. SEU_STATUS_REG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	LD_TX_CLK_INACTIVE	R	0x0	status bit latched high when ld_tx_clk is inactive. Cleared when you write 1 to this bit or on POR or on pin reset
6	PLL_CLK_FREQ_LOCK_LOST	R	0x0	status bit latched high when frequency lock is lost on pll clock (125Mhz). Cleared when you write 1 to this bit or on POR or on pin reset
5	PLL_CLK_PPM_LOCK_LOST	R	0x0	status bit latched high when ppm lock is lost for pll clock (125Mhz). Cleared when you write 1 to this bit or on POR or on pin reset
4	PLL_CLK_INACTIVE	R	0x0	status bit latched high when pll clock (125Mhz) is inactive. Cleared when you write 1 to this bit or on POR or on pin reset
3	PLL_250_RECV_CLK_INACTIVE	R	0x0	status bit latched high when 250M pll recovered clock is inactive. Cleared when you write 1 to this bit or on POR or on pin reset
2	ADC_CLK_INACTIVE	R	0x0	status bit latched high when adc clock on any channel is inactive. Cleared when you write 1 to this bit or on POR or on pin reset
1	FAULT_DET_PM_TOP	R	0x0	status bit latched high when a fault is detected in ep_pm_top block. Cleared when you write 1 to this bit or on POR or on pin reset
0	FAULT_DET_RESET_CTRL	R	0x0	status bit latched high when a fault is detected in ep_reset_ctrl block. Cleared when you write 1 to this bit or on POR or on pin reset

7.6.1.71 REF_CLK_PPM_MONITOR_CNT Register (Offset = 0x1D9) [Reset = 0x30D3]

REF_CLK_PPM_MONITOR_CNT is shown in 表 7-82.

Return to the Summary Table.

表 7-82. REF_CLK_PPM_MONITOR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-0	CFG_REF_CLK_PPM_MONITOR_COUNT	R/W	0x30D3	Number of cycles for which counter running on reference(25Mhz) clock should run to calculate ppm (By default counter takes 0.5ms)

7.6.1.72 MON_CLK_PPM_MONITOR_CNT Register (Offset = 0x1DA) [Reset = 0xF423]

MON_CLK_PPM_MONITOR_CNT is shown in 表 7-83.

Return to the Summary Table.

表 7-83. MON_CLK_PPM_MONITOR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CFG_MON_CLK_PPM_MONITOR_COUNT	R/W	0xF423	Number of cycles for which counter running on clock which has to be monitored(125Mhz) should run by the time reference counter does a rollback (By default counter takes 0.5ms if there is zero ppm)

7.6.1.73 MAX_PLUS_PPM_MON_CNT Register (Offset = 0x1DB) [Reset = 0x44]

MAX_PLUS_PPM_MON_CNT is shown in 表 7-84.

Return to the Summary Table.

表 7-84. MAX_PLUS_PPM_MON_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CFG_PLUS_PPM_MAX_MON_CNT	R/W	0x44	when the reference counter goes to zero value, the maximum value of mon_cnt(as it is + ppm, mon_cnt rolls back) for a threshold of 1000ppm

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7.6.1.74 MAX_MINUS_PPM_MON_CNT Register (Offset = 0x1DC) [Reset = 0xF3DF]

MAX_MINUS_PPM_MON_CNT is shown in 表 7-85.

Return to the Summary Table.

表 7-85. MAX_MINUS_PPM_MON_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CFG_MINUS_PPM_MAX_MON_CNT	R/W	0xF3DF	when the reference counter goes to zero value, the minimum value of mon_cnt(as it is - ppm, mon_cnt doesn't roll back) for a threshold of 1000ppm

7.6.1.75 SYS_CLK_PPM_STATUS Register (Offset = 0x1DD) [Reset = 0xF423]

SYS_CLK_PPM_STATUS is shown in 表 7-86.

Return to the Summary Table.

表 7-86. SYS_CLK_PPM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	SYS_CLK_PPM_STATUS	R	0xF423	every time reference counter rolls back, the value of monitor count is latched into this status register. Use this register to get an approximate value of ppm. Don't use this register to calculate ppm if seu_stat[10]==1

7.6.1.76 PLL_CLK_PPM_STATUS Register (Offset = 0x1DE) [Reset = 0xF423]

PLL_CLK_PPM_STATUS is shown in 表 7-87.

Return to the Summary Table.

表 7-87. PLL_CLK_PPM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PLL_CLK_PPM_STATUS	R	0xF423	every time reference counter rolls back, the value of monitor count is latched into this status register. Use this register to get an approximate value of ppm. Don't use this register to calculate ppm if seu_stat[6]==1

7.6.1.77 OP_MODE_DECODE Register (Offset = 0x1DF) [Reset = 0x0]

OP_MODE_DECODE is shown in 表 7-88.

Return to the Summary Table.

表 7-88. OP_MODE_DECODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Reserved
8-7	RESERVED	R	0x0	Reserved
6	RESERVED	R	0x0	Reserved
5	RGMII_MII_SEL	R/W	0x0	0x0 = RGMII 0x1 = MII
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

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表 7-88. OP_MODE_DECODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	CFG_OPMODE	R/W	0x0	Operation Mode 0x0 = RGMII to Copper 0x1 = Reserved 0x2 = Reserved 0x3 = Reserved 0x4 = Reserved 0x5 = Reserved 0x6 = Reserved 0x7 = Reserved

7.6.1.78 GPIO_MUX_CTRL Register (Offset = 0x1E0) [Reset = 0x7A]

GPIO_MUX_CTRL is shown in 表 7-89.

Return to the Summary Table.

表 7-89. GPIO_MUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-8	RESERVED	R	0x0	Reserved
7-4	JTAG_TDO_GPIO_1_CTRL	R/W	0x7	See bits [3:0] for GPIO control options. If either type of SFD is enabled, this pin will be automatically configured to TX_SFD.
3-0	LED_2_GPIO_0_CTRL	R/W	0xA	Following options are available for GPIO control. If either type of SFD is enabled, this pin will be automatically configured to RX_SFD. 0x0 = CLK_OUT 0x1 = RESERVED 0x2 = INT 0x3 = Link status 0x4 = RESERVED 0x5 = Transmit SFD 0x6 = Receive SFD 0x7 = WOL 0x8 = Energy detect(1000Base-T and 100Base-TX only) 0x9 = PRBS errors 0xA = LED_2 0xB = LED_GPIO(3) 0xC = CRS 0xD = COL 0xE = constant '0' 0xF = constant '1'

7.6.1.79 MONITOR_REGISTERS_0 Register (Offset = 0x1E2) [Reset = 0x25]

MONITOR_REGISTERS_0 is shown in 表 7-90.

Return to the Summary Table.

表 7-90. MONITOR_REGISTERS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_SNSR_DC_OFFSET_SEL	R/W	0x0	Controls the DC offset value for monitors 0x0 = DC offset is from calibration logic 0x1 = DC offset is taken from 0x1E7[15-8]
14	CFG_SNSR_SEFIINT_EN	R/W	0x0	Reserved
13-11	CFG_SNSR_SEFIDET_THRESH	R/W	0x0	Reserved
10-9	CFG_SNSR_HISTDET_THRESH	R/W	0x0	Reserved

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表 7-90. MONITOR_REGISTERS_0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	CFG_SNSR_SCALE_ADC_INP	R/W	0x0	Reserved
6	CFG_SNSR_HIST_CLR	R/W	0x0	Writing 1 to this bit clears the history of monitor data samples collected to detect SEFI event. This is not a self-clear bit. Write 0 to clear this bit
5	CFG_SNSR_DISCARD_SAMPLE_NUM	R/W	0x1	Controls number of sensor ADC symbols to discard after enabling the ADC and before starting the averaging for further logging 0x0 = 3 samples 0x1 = 6 samples
4	CFG_SNSR_AVG_SAMPLE_NUM	R/W	0x0	Controls number of sensor ADC symbols to average for further logging 0x0 = 3 samples 0x1 = 5 samples
3-2	CFG_SNSR_ADC_CLK_DIV	R/W	0x1	Controls the frequency of sensor ADC input clock 0x0 = 12.5MHz 0x1 = 6.25MHz 0x2 = 3.125MHz 0x3 = 3.125MHz
1	CFG_SNSR_FORCE_START	R/W	0x0	Set this bit to forcefully enable the sensor monitors. Normally the monitors are enabled after Link up on MDI
0	CFG_SNSR_RESET	R/W	0x1	Set this bit to manually put the monitors in a reset state

7.6.1.80 MONITOR_REGISTERS_1 Register (Offset = 0x1E7) [Reset = 0x12]

MONITOR_REGISTERS_1 is shown in 表 7-91.

Return to the Summary Table.

表 7-91. MONITOR_REGISTERS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	CFG_SNSR_DC_OFFSET_2C	R/W	0x0	Controls the Sensor DC offset if 0x1E2[15] is set to 1.
7-6	CFG_SNSR_CIC_GAIN12_ARITH	R/W	0x0	
5-3	CFG_SNSR_CIC_GAIN2	R/W	0x2	
2-0	CFG_SNSR_CIC_GAIN1	R/W	0x2	

7.6.1.81 MONITOR_REGISTERS_2 Register (Offset = 0x1E8) [Reset = 0x920]

MONITOR_REGISTERS_2 is shown in 表 7-92.

Return to the Summary Table.

表 7-92. MONITOR_REGISTERS_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_SNSR_BYPASS_RESET_SENSOR_VAL	R/W	0x0	Controls the reset value to sensor if monitor FSM is bypassed by setting register bit 0x1E9[14] 0x0 = sensor is in reset state 0x1 = Sensor is not in reset

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表 7-92. MONITOR_REGISTERS_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14-12	CFG_SNSR_RD_DATA	R/W	0x0	Controls the sensor from which data is read from register 0x1EA 0x0 = data is read from VDDA2P5 sensor 0x1 = data is read from VDDA1P8 sensor 0x2 = data is read from VDD1P1 sensor 0x3 = data is read from VDDIO sensor 0x4 = data is read from Temperature sensor 0x5 = reserved 0x6 = reserved 0x7 = reserved
11-9	CFG_SNSR_DEC_FACTOR_SENSORS	R/W	0x4	Controls the decimation factor for sensor ADC when the monitor is working in normal mode and out of calibration phase
8-6	CFG_SNSR_DEC_FACTOR_GAIN_CALIB	R/W	0x4	Controls the decimation factor for sensor ADC when the monitor is in gain calibration stage
5-3	CFG_SNSR_DEC_FACTOR_DC_CALIB	R/W	0x4	Controls the decimation factor for sensor ADC when the monitor is in DC calibration stage
2-0	CFG_SNSR_BYPASS_SEL_NUM	R/W	0x0	This field selects the sensor to be monitored when FSM is bypassed by setting register bit 0x1E9[14]

7.6.1.82 MONITOR_REGISTERS_3 Register (Offset = 0x1E9) [Reset = 0x36D]

MONITOR_REGISTERS_3 is shown in 表 7-93.

Return to the Summary Table.

表 7-93. MONITOR_REGISTERS_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_SNSR_GAIN_NOTFROM_EFUSE	R/W	0x0	If set, selects the gain for sensors from configuration registers and not from efuse. Refer to registers 0x1E7[7:0] 0x0 = Gain values are taken from EFUSE 0x1 = Gain values are not taken from EFUSE
14	CFG_SNSR_BYPASS_FSM	R/W	0x0	Control bit to bypass the monitor FSM logic 0x0 = Monitor FSM is controlling the sensors 0x1 = Monitor FSM is bypassed
13-12	CFG_SNSR_ITER_TIMES	R/W	0x0	This field determines the number of times the sensors programmed in 0x1E9[11:0] should be cycled through before checking all sensors
11-9	CFG_SNSR_ITER_SLOT_3	R/W	0x1	selects the sensor for slot 3 in each iteration before all sensors are checked
8-6	CFG_SNSR_ITER_SLOT_2	R/W	0x5	selects the sensor for slot 2 in each iteration before all sensors are checked
5-3	CFG_SNSR_ITER_SLOT_1	R/W	0x5	selects the sensor for slot 1 in each iteration before all sensors are checked
2-0	CFG_SNSR_ITER_SLOT_0	R/W	0x5	selects the sensor for slot 0 in each iteration before all sensors are checked

7.6.1.83 MONITOR_REGISTERS_RD_0 Register (Offset = 0x1EA) [Reset = 0x0]

MONITOR_REGISTERS_RD_0 is shown in 表 7-94.

Return to the Summary Table.

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表 7-94. MONITOR_REGISTERS_RD_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	STAT_SNSR_RD_RDATA	R	0x0	Read back data from sensors can be logged from this register. Data from particular sensor can be read by bypassing the FSM using register bit 0x1E9[14] and selecting particular sensor by programming 0x1E8[2:0]

7.6.1.84 LOCK_DET_REG Register (Offset = 0x1EE) [Reset = 0x35]

LOCK_DET_REG is shown in 表 7-95.

Return to the Summary Table.

表 7-95. LOCK_DET_REG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	NEWBITFIELD	R/W	0x0	
9	CFG_CRC_EN	R/W	0x0	
8	CFG_ECC_EN	R/W	0x0	Harsh Industrial only: In harsh industrial mode, enable the ECC and Checksum protection of programmable register bank.
7	CFG_ECC_ERR_EN	R/W	0x0	Harsh Industrial only: In harsh industrial mode, enable the ECC and Checksum protection of programmable register bank. When cfg_ecc_en is set, setting this bit, will create error.
6-4	CFG_PROG_LOCKDET_WINDOW	R/W	0x3	
3-2	CFG_PROG_LOCKDET_WAIT	R/W	0x1	
1	CFG_FORCE_PLL_LOCK_DET_MON_EN	R/W	0x0	
0	CFG_PLL_LOCK_DET_MON_EN	R/W	0x1	

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DP83561-SP is a 10/100/1000 Copper Ethernet PHY. It supports connections to an Ethernet MAC through RGMII. MII is also supported but only for 100M and 10M speeds. For MII to operate correctly, 1000M advertisement should be disabled. Connections to the Ethernet media are made through the IEEE 802.3 defined Media Dependent Interface.

When using the device for Ethernet application, it is necessary to meet certain requirements for normal operation of the device. The following typical application and design requirements can be used for selecting appropriate component values for the DP83561-SP.

8.2 Typical Application

図 8-1 shows a copper Ethernet typical application.

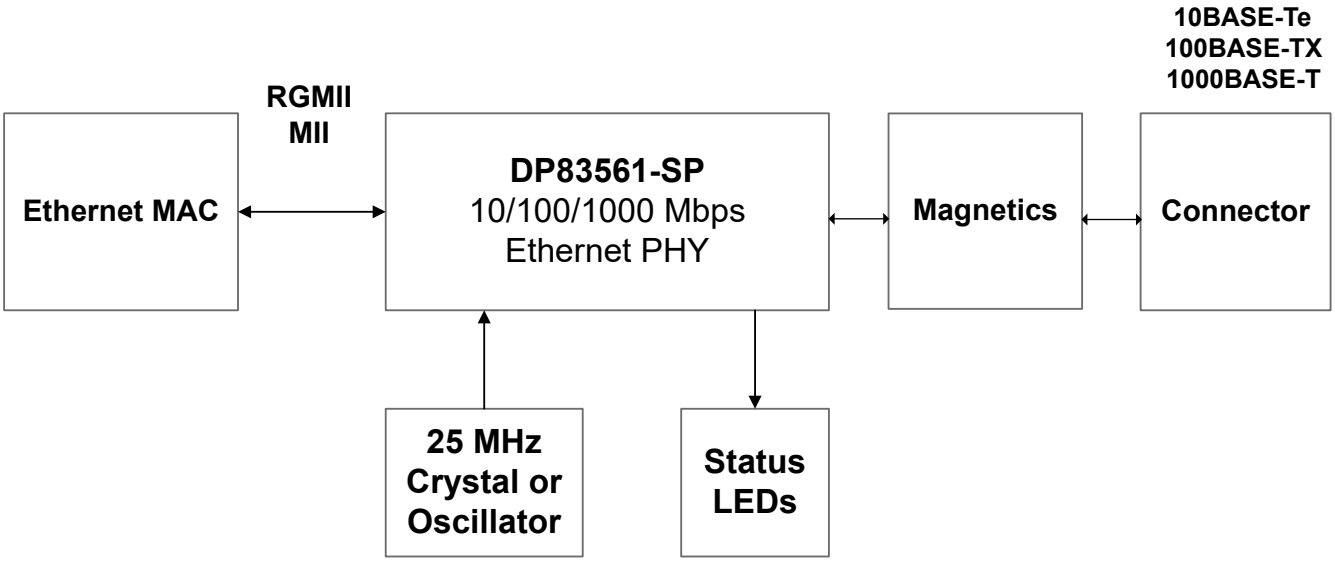


図 8-1. Typical Copper Ethernet Application

8.2.1 Design Requirements

The design requirements for the DP83561-SP are:

- VDDA2P5 = 2.5 V
- VDD1P1 = 1.1 V
- VDDIO = 3.3 V, 2.5 V, or 1.8 V
- VDDA1P8_x = 1.8 V (optional)
- Clock Input = 25 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Clock Input

Input reference clock requirements are same in all functional modes.

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8.2.2.1.1 Crystal Recommendations

A 25-MHz, parallel, 15-pF to 40-pF load crystal resonator should be used if a crystal source is desired. 図 8-2 shows a typical connection for a crystal resonator circuit. The load capacitor values vary with the crystal vendors. Check with the vendor for the recommended loads.

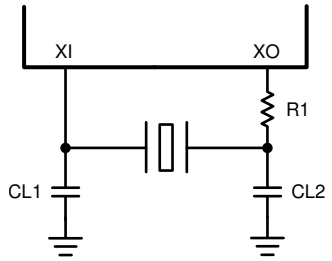


図 8-2. Crystal Oscillator Circuit

As a starting point for evaluating the oscillator performance, the value of CL1 and CL2 should each be equal to 2x the specified load capacitance from the crystal vendor's data sheet. For example, if the specified load capacitance of the crystal is 10 pF, set CL1 = CL2 = 20 pF. CL1, CL2 value may need to be adjusted based on the parasitic capacitance. Depending on the crystal drive level, R1 may or may not be needed.

表 8-1 lists the 25-MHz crystal specifications.

表 8-1. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Including Operational Temperature, Aging, and Other Factors			±100	ppm
Load Capacitance		15		40	pF
ESR				50	ohm

8.2.2.1.2 External Clock Source Recommendations

If an external clock oscillator is used, then it should be directly connected to XI. XO should be left floating.

表 8-2 lists the CMOS 25-MHz oscillator specifications.

表 8-2. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Including operational temperature, aging, and other factors			±100	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	

8.2.2.2 MAC Interface

The Media Independent Interface (RGMII / GMII) connects the DP83561-SP to the Media Access Controller (MAC). The MAC may in fact be a discrete device, integrated into a microprocessor, CPU, or FPGA.

8.2.2.2.1 RGMII Layout Guidelines

- RGMII signals are single-ended signals.
- Traces must be routed with impedance of 50 Ω to ground.
- Skew between TXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Skew between RXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Keep trace lengths as short as possible; less than 2 inches is recommended with less than 6 inches as maximum length.

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- Configurable clock skew for GTX_CLK and RX_CLK.
  - Clock skew for RX and TX paths can be optimized independently.
  - Clock skew is adjustable in 0.25-ns increments (through register).

8.2.2.2.2 MII Layout Guidelines

1. MII signals are single-ended signals.
2. Traces should be routed with 50-Ω impedance to ground.
3. Keep trace lengths as short as possible, less than two inches (approximately 5 cm) is recommended and less than six inches (approximately 15 cm) maximum.

8.2.2.3 Media Dependent Interface (MDI)

The Media Dependent Interface (MDI) connects the DP83561-SP to the transformer and the Ethernet network.

8.2.2.3.1 MDI Layout Guidelines

- MDI traces must be 50 Ω to ground and 100 Ω-differential controlled impedance.
- Route MDI traces to transformer on the same layer.
- Use a metal shielded RJ-45 connector, and connect the shield to chassis ground.
- Use magnetics with integrated common-mode choking devices.
- Void supplies and ground beneath magnetics.
- Do not overlap the circuit and chassis ground planes, keep them isolated. Instead, make chassis ground an isolated island and make a void between the chassis and circuit ground. Connecting circuit and chassis planes using a size 1206 resistor and capacitor on either side of the connector is a good practice.

8.2.2.4 Magnetics Requirements

In applications where copper Ethernet interface is used, magnetic isolation is required. Magnetics can be discrete or integrated in the Ethernet cable connector. The DP83869HM will operate with discrete and integrate magnetics if they meet the electrical specifications listed in 表 8-3.

表 8-3. Magnetics Electrical Specification

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Insertion Loss	1-100 MHz	-1	dB
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-80 MHz	-10	dB
Differential to Common Mode Rejection	1-50 MHz	-30	dB
	60-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Open Circuit Inductance	8-mA DC Bias	350	µH
Isolation	HPOT	1500	Vrms

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8.2.2.4.1 Magnetics Connection

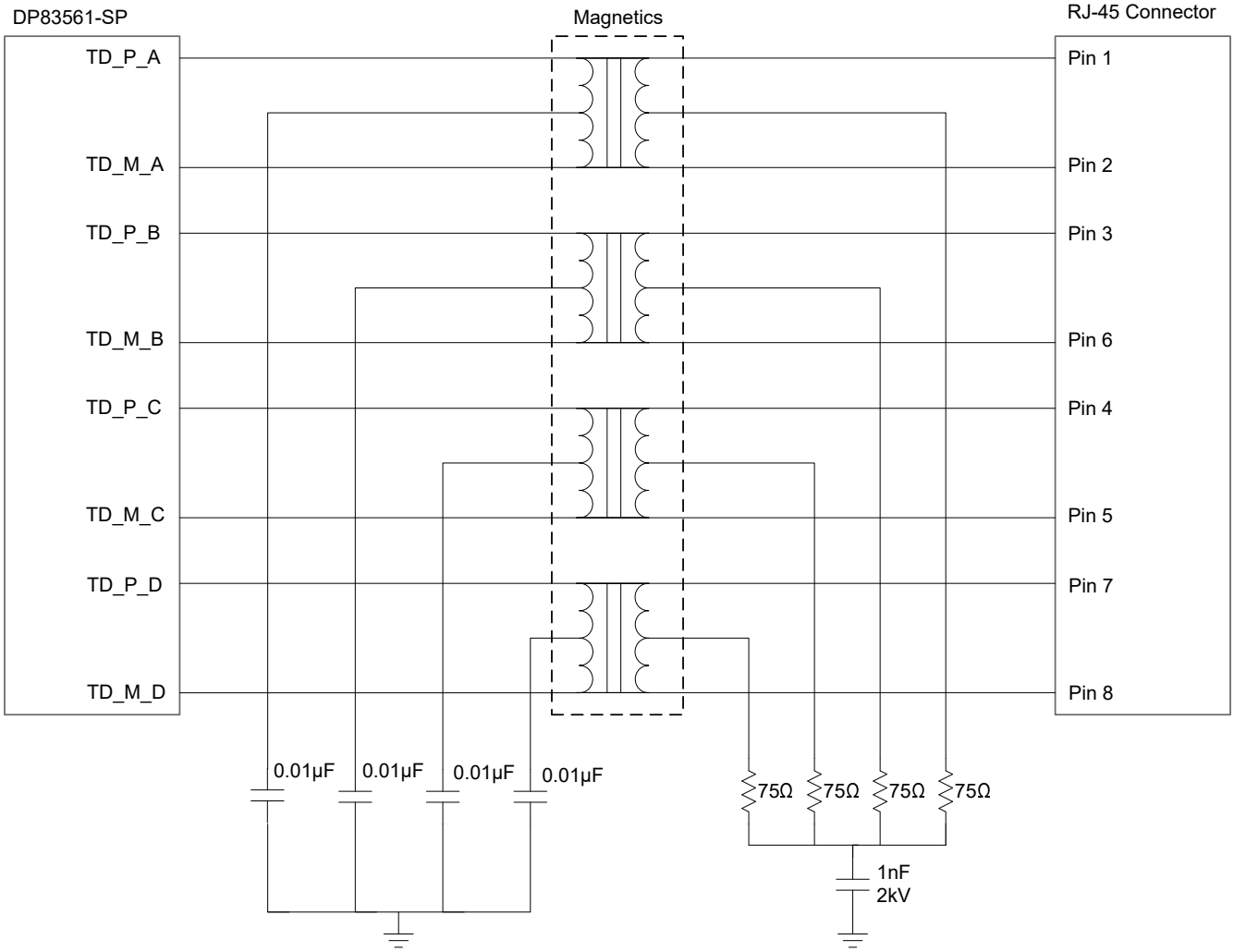


図 8-3. Magnetics Connection

A. Each center tap on the side connected to the PHY, must be isolated from one another and connected to ground through a decoupling capacitor (0.01 µF recommended).

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9 Power Supply Recommendations

The DP83561-SP is capable of operating with as few as two or three supplies. The I/O power supply can also be operated independently of the main device power supplies to provide flexibility for the MAC interface. There are two possible supply configurations that can be used: Two Supply and Three Supply. In the Two-Supply Configuration, no power rail is connected to VDDA1P8_x pins (pin 13, 48). When unused, pin 13 and 48 should be left floating with no components attached to them.

9.1 Two-Supply Configuration

図 9-1 shows the connection diagram for a two-supply configuration.

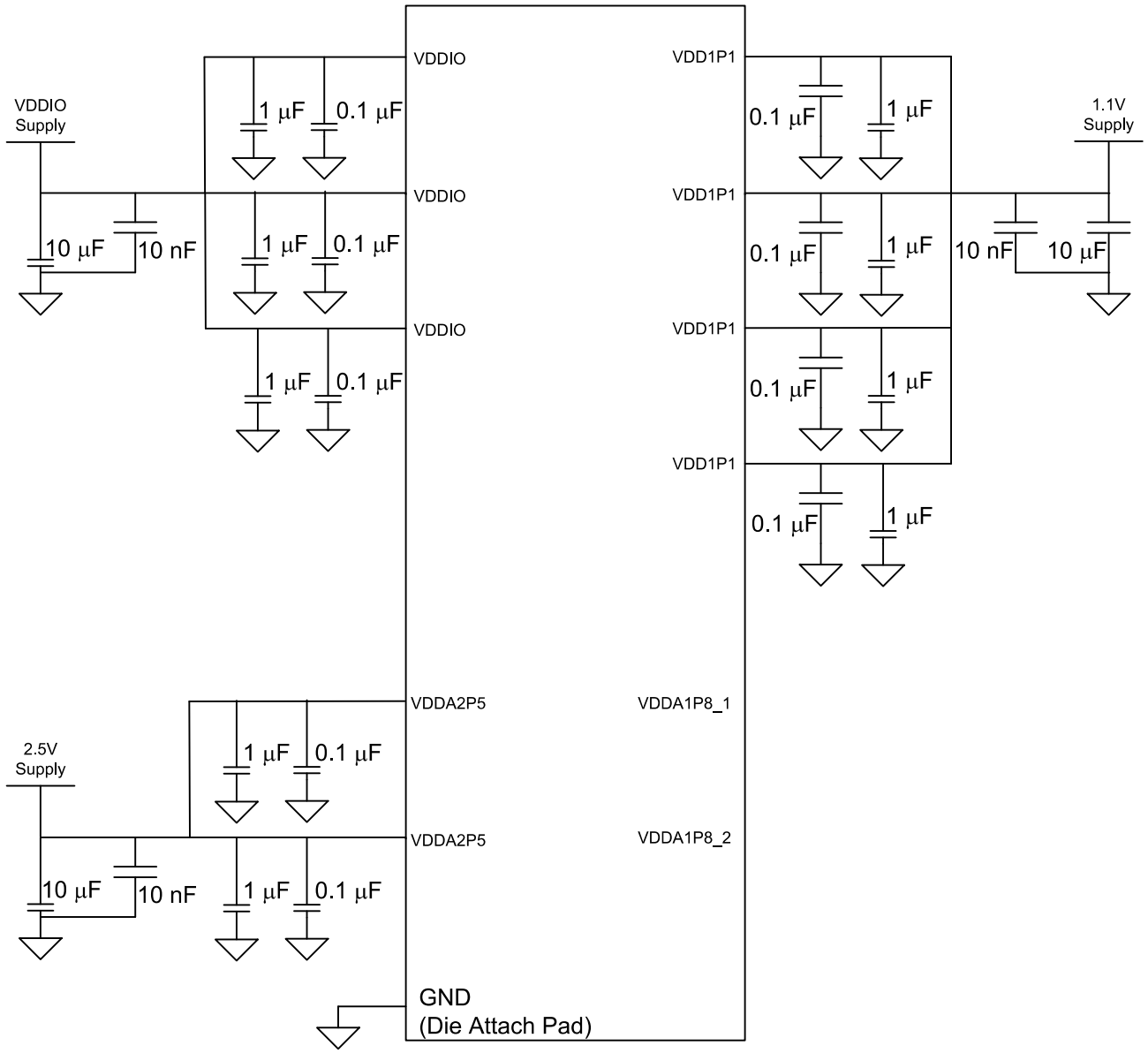


図 9-1. Two-Supply Configuration

For a two-supply configuration, both VDDA1P8 pins must be left unconnected.

Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

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The strap (SUPPLYMODE_SEL, pin 23) shall be pulled low to set double supply mode. VDDIO may be 3.3 V, 2.5 V, or 1.8 V. VDDIO_SEL strap shall be selected appropriately to VDDIO voltage applied.

For two-supply configuration, the recommendation is to power all supplies together. If that is not possible, then the following power sequencing must be used.

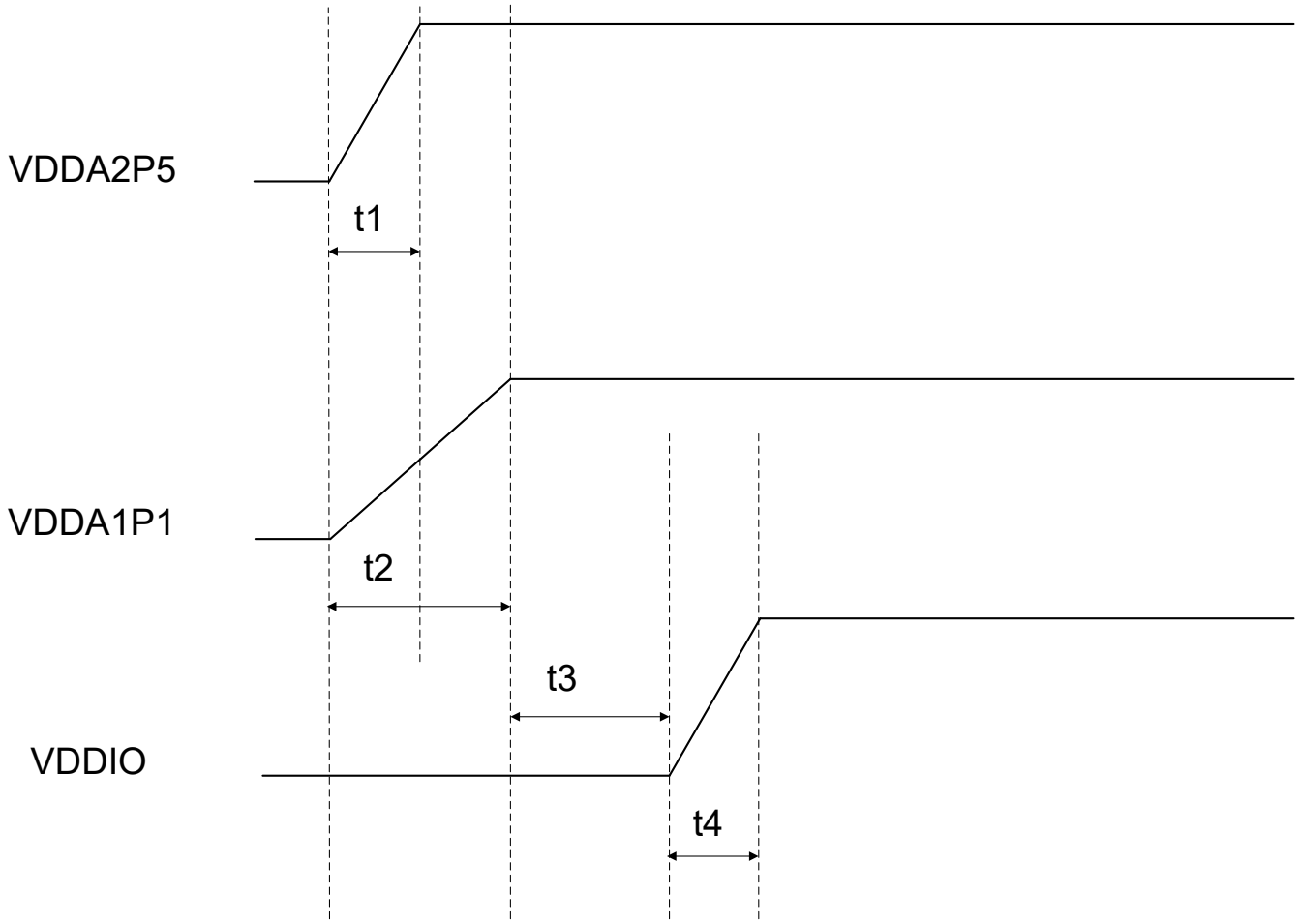


図 9-2. Two-Supply Sequence Diagram

表 9-1. Two-Supply Sequence

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1 - VDDA2P5 ramp time		0.5		100	ms
t2 - VDD1P1 ramp time		0.5		100	ms
t3 - Delay	Measured W.r.t stable VDDA2P5 and VDD1P1	0		50	ms
t4 - VDDIO ramp time		0.5		100	ms

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9.2 Three-Supply Configuration

図 9-3 shows the connection diagram for the three-supply configuration.

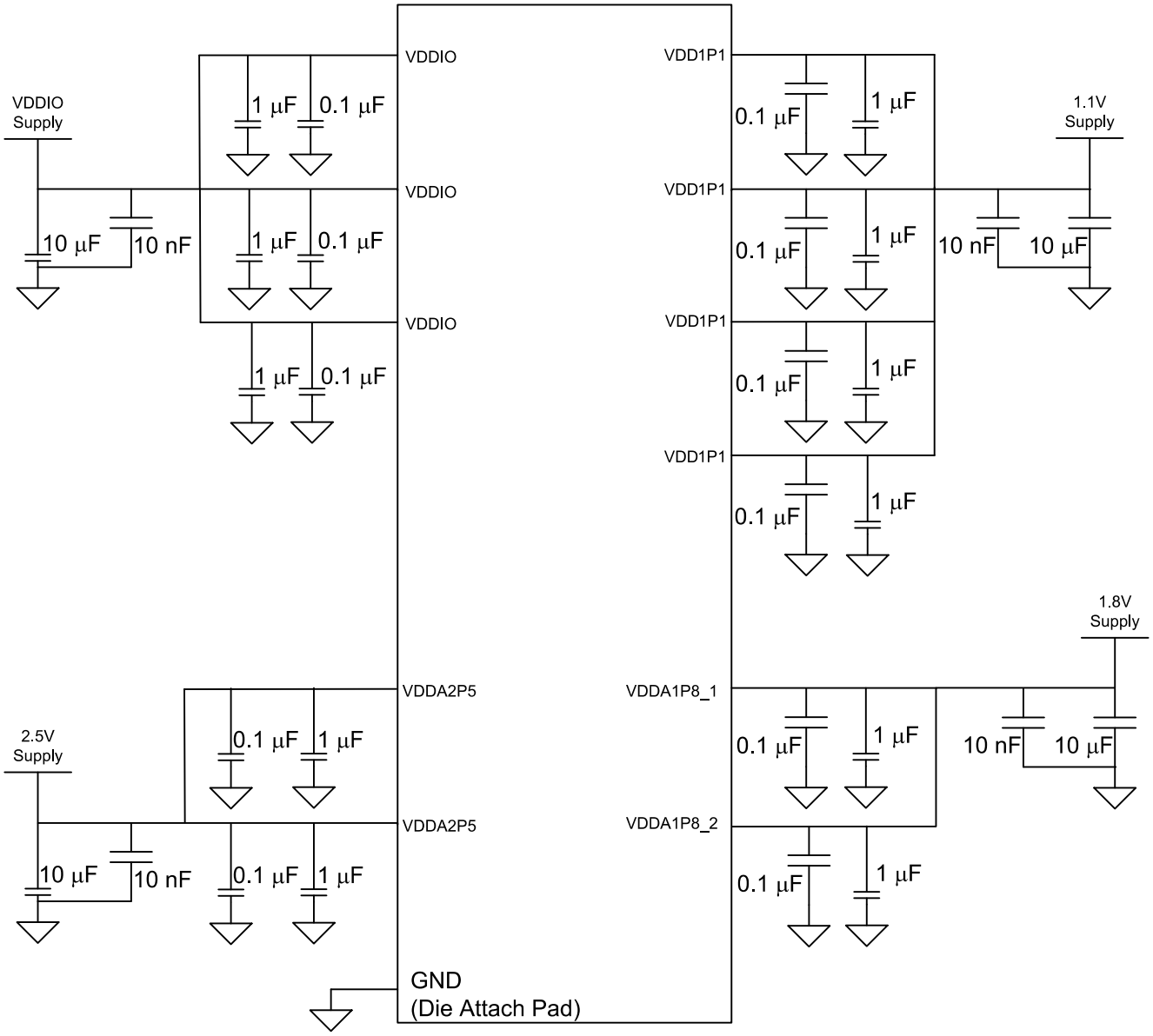


図 9-3. Three-Supply Configuration

Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins, placing the 0.1-µF capacitor closest to the pin.

Note

The strap (SUPPLYMODE_SEL, pin 23) shall be pulled high to set triple-supply mode. VDDIO may be 3.3 V, 2.5 V, or 1.8 V. VDDIO strap shall be selected appropriately to VDDIO voltage applied.

For three-supply configuration, the recommendation is to power all supplies together. If that is not possible, then the following power sequencing must be used.

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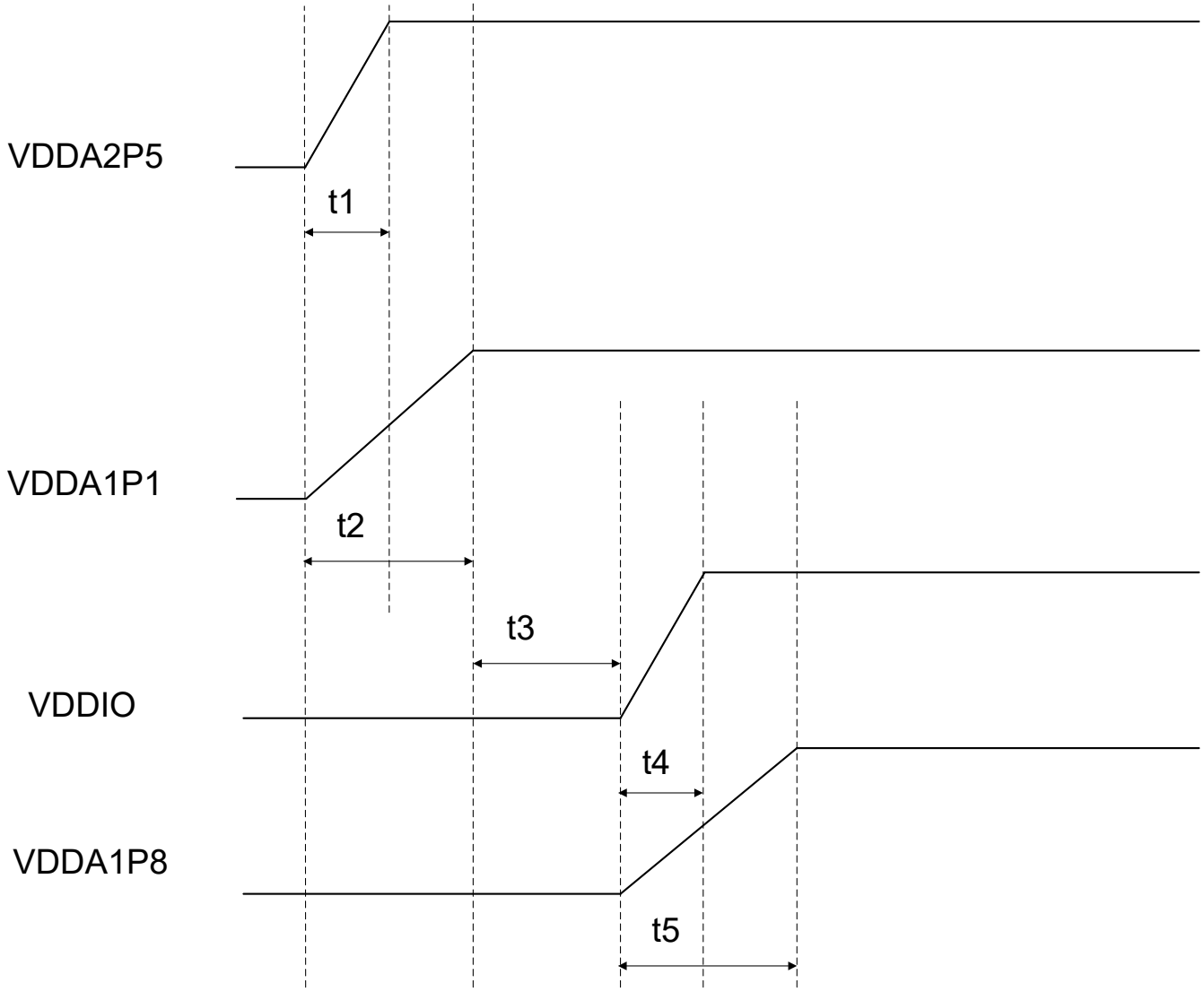


図 9-4. Three-Supply Sequence Diagram

表 9-2. Three-Supply Sequence

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1 - VDDA2P5 ramp time		0.5		100	ms
t2 - VDD1P1 ramp time		0.5		100	ms
t3 - Delay	Measured W.r.t stable VDDA2P5 and VDD1P1	0		50	ms
t4 - VDDIO ramp time		0.5		100	ms
t5 - VDDA1P8 ramp time		0.5		100	ms

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10 Layout

10.1 Layout Guidelines

10.1.1 Signal Traces

PCB traces are lossy and long traces can degrade the signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω single-ended impedance. Differential traces should be 50-Ω single-ended and 100-Ω differential. Take care that the impedance is constant throughout. Impedance discontinuities cause reflections leading to EMI & signal integrity problems. Stubs must be avoided on all signal traces, especially the differential signal pairs. See 図 10-1.

Within the differential pairs, the trace lengths must run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI.

Length matching is also important on MAC interface. All Transmit signal trace lengths must match to each other and all Receive signal trace lengths must match to each other.

Ideally, there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible.

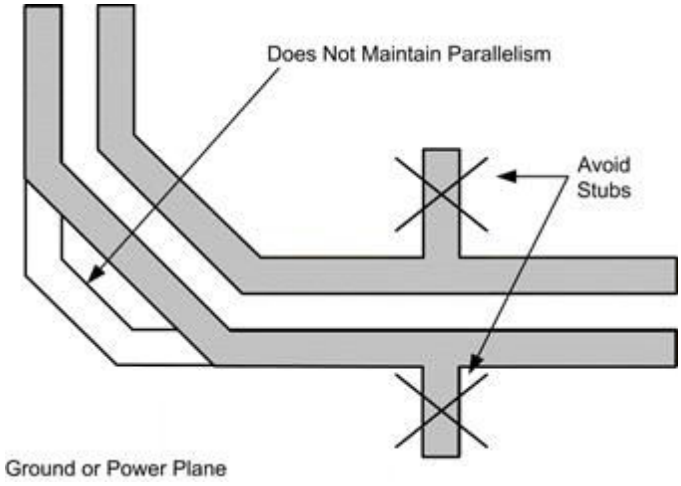


図 10-1. Avoiding Stubs in a Differential Signal Pair

Signals on different layers should not cross each other without at least one return path plane between them.

Coupling between traces is also an important factor. Unwanted coupling can cause cross talk problems. Differential pairs on the other hand, should have a constant coupling distance between them.

For convenience and efficient layout process, start by routing the critical signals first.

10.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path width can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path beneath the signal traces should be avoided at all cost. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems. See 図 10-2.

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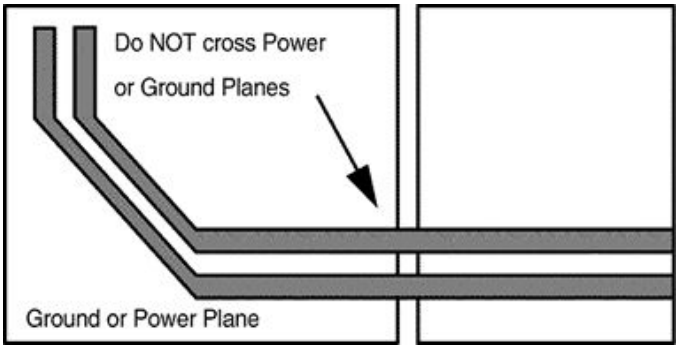


図 10-2. Differential Signal Pair-Plane Crossing

10.1.3 Transformer Layout

There should be no metal layer running beneath the transformer. Transformers can inject noise in metal beneath them which can affect the performance of the system.

10.1.4 Metal Pour

All metal pours which are not signals or power should be tied to ground. There should be no floating metal on the system. There should be no metal between the differential traces.

10.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a 4-layer PCB should be used. However a 6-layer board is recommended. See 図 10-3 for the recommended layer stack ups for 4, 6, and 8-layer boards. These are recommendations not requirements, other configurations can be used as per system requirements.

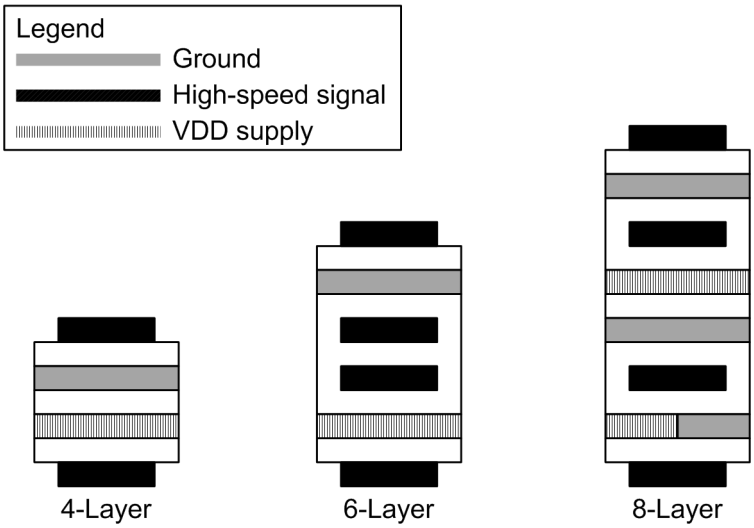


図 10-3. Recommended Layer Stack Up

Within a PCB, it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. 図 10-4 shows alternative PCB stacking options.

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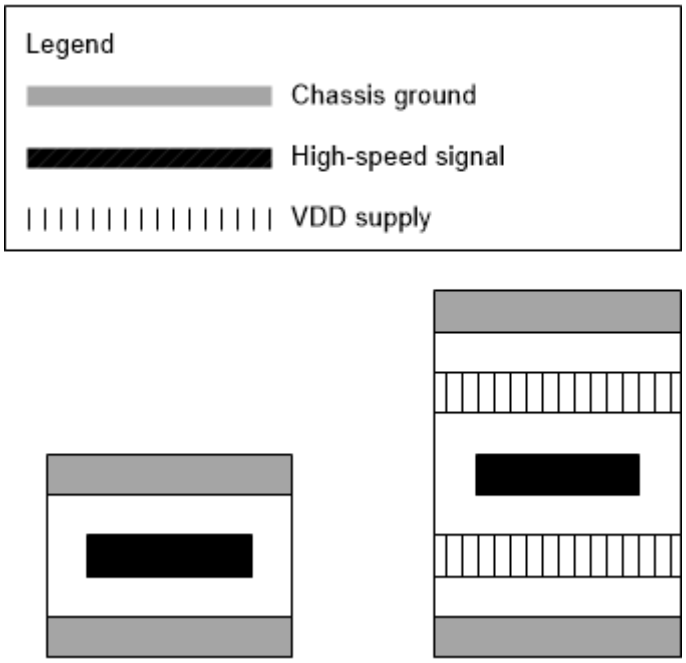


図 10-4. Alternative Layer Stack Up

10.2 Layout Example

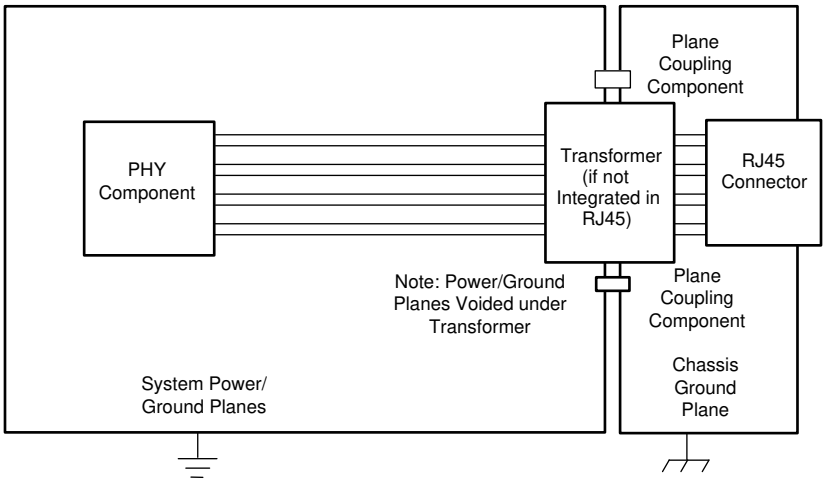


図 10-5. Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *DP83867 Troubleshooting Guide* (SNLA246)
- *How to Configure DP838XX for Ethernet Compliance Testing* (SNLA239)
- *Configuring Ethernet Devices with 4-Level Straps* (SNLA258)
- *RGMII Interface Timing Budgets* (SNLA243)
- *DP83867E/IS/CS/IR/CR RGZ Power Consumption Data* (SNLA241)
- *How to Configure DP83867 Start of Frame* (SNLA242)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

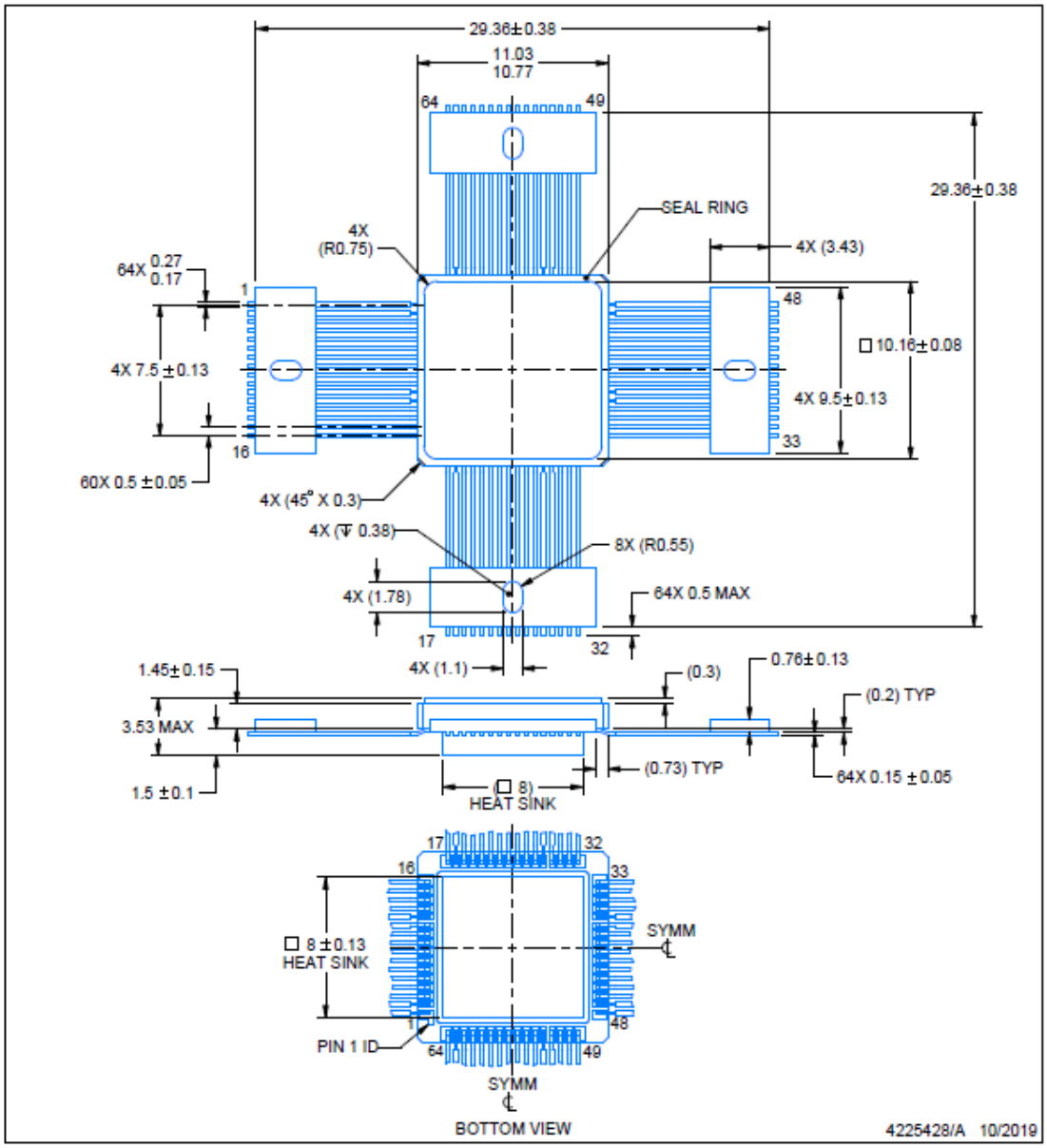
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PACKAGE OUTLINE

HBE0064B

CFP - 3.53 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. Ground pad to be electronic connected to heat sink and seal ring.
5. The leads are gold plated and can be solder dipped.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962F2021601VXC	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	-55 to 125	5962F2021601VXC DP83561-SP
5962F2021601VXC.A	Active	Production	CFP (HBE) | 64	14 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	-55 to 125	5962F2021601VXC DP83561-SP
DP83561HBE/EM	Active	Production	CFP (HBE) | 64	24 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	25 to 25	DP83561HBE/EM
DP83561HBE/EM.A	Active	Production	CFP (HBE) | 64	24 | TUBE	ROHS Exempt	NIAU	Level-1-NA-UNLIM	25 to 25	DP83561HBE/EM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

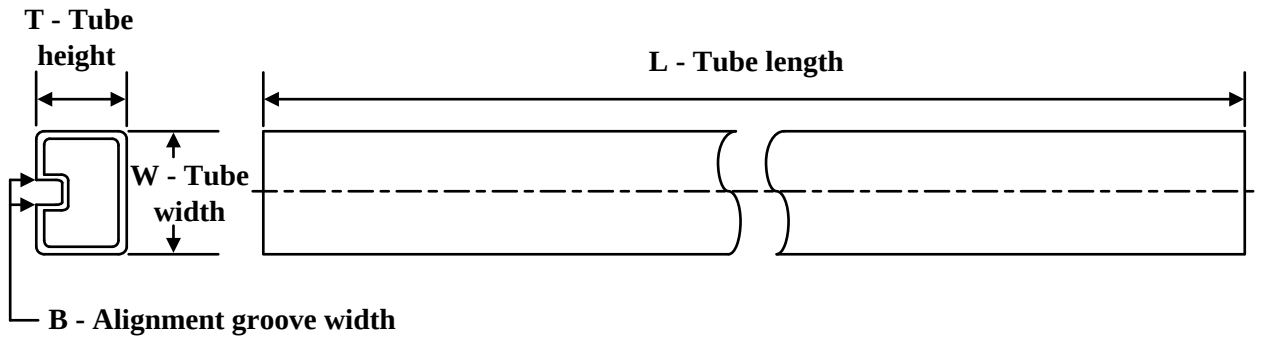
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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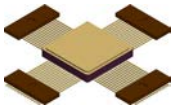
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962F2021601VXC	HBE	CFP (HSL)	64	14	495	33	11176	16.51
5962F2021601VXC.A	HBE	CFP (HSL)	64	14	495	33	11176	16.51

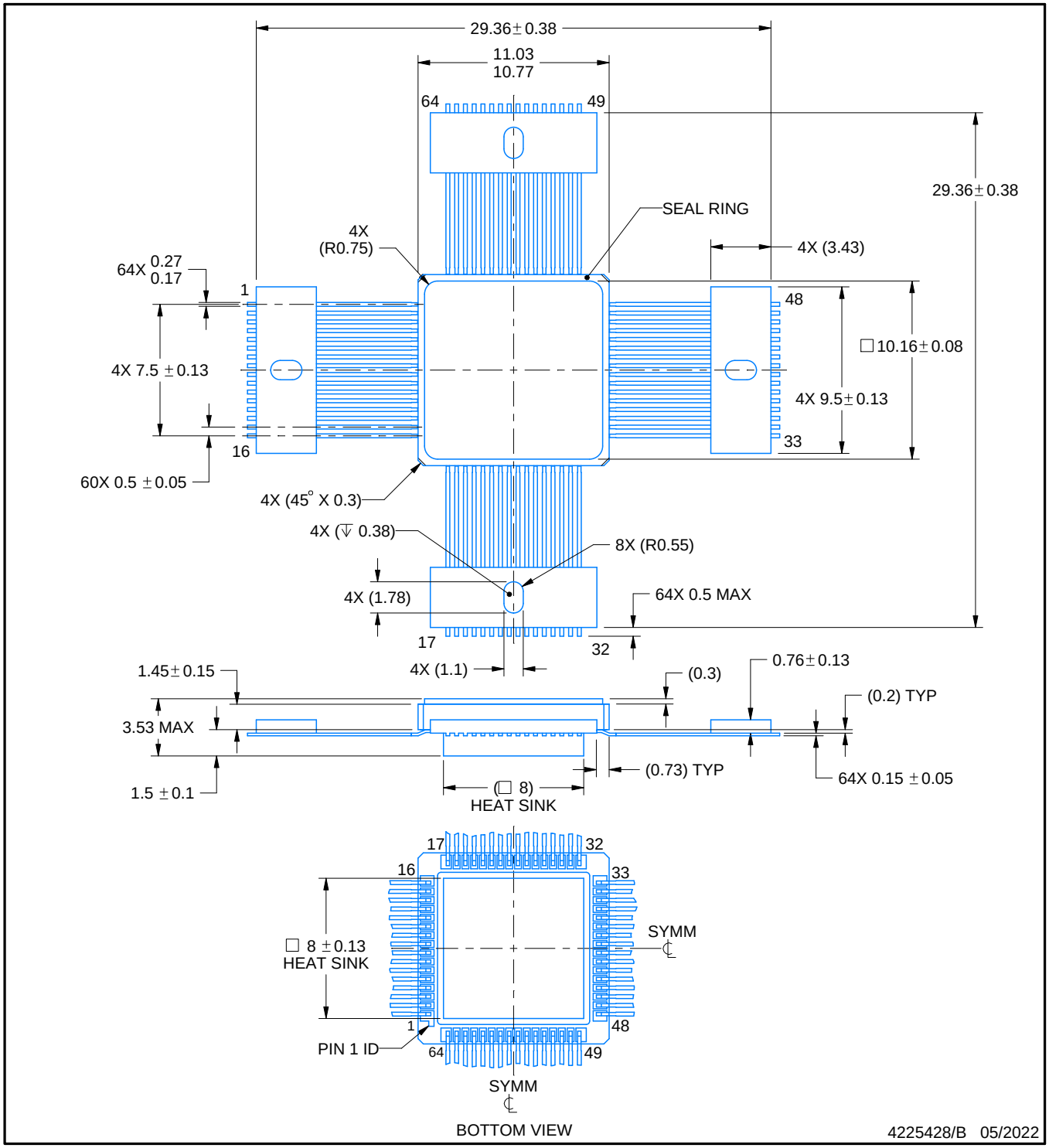
HBE0064B



PACKAGE OUTLINE

CFP - 3.53 mm max height

CERAMIC FLATPACK



NOTES:

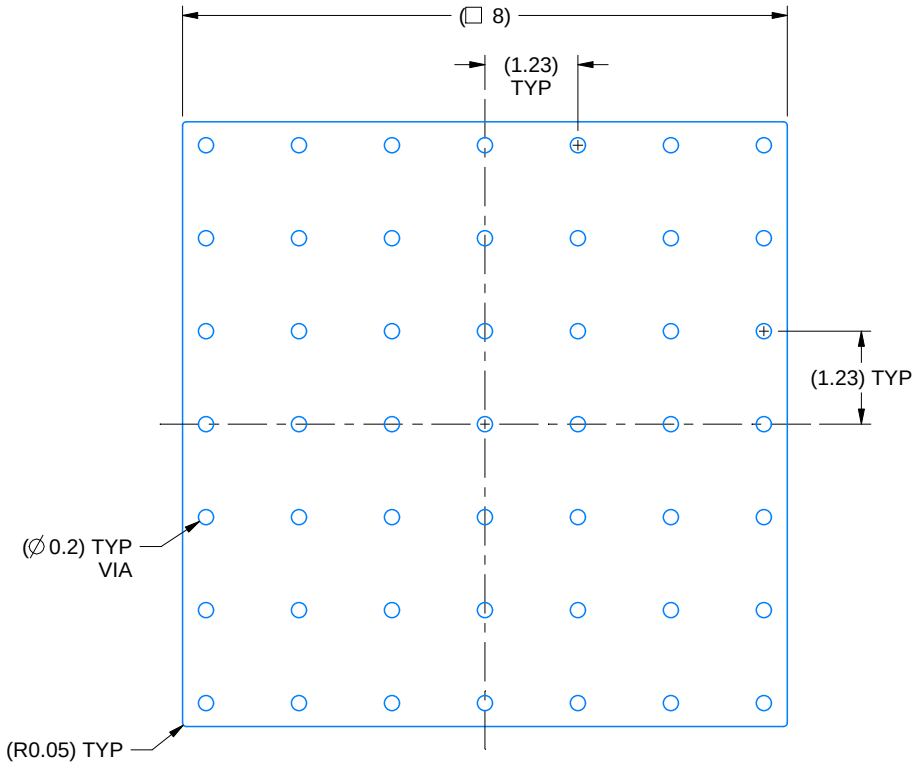
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
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EXAMPLE BOARD LAYOUT

HBE0064B

CFP - 3.53 mm max height

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
SCALE: 10X

4225428/B 05/2022

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最終更新日：2025 年 10 月