DP83TC811-Q1 低消費電力、車載用 100BASE-T1 イーサネット物理層トランシーバ

1 特長

- 100BASE-T1 – IEEE 802.3bw 準拠
  - OPEN Alliance 認定済み
  - BroadR-Reach および 100BASE-T1 の PHY と相互運用可能
- 車載アプリケーション用に AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～+125 ℃
  - デバイス HBM ESD 分類レベル 3A
  - ピン 5 を除くすべてのピンについてデバイス CDM ESD 分類レベル C5
  - ピン 5 についてデバイス CDM ESD 分類レベル C3
  - ピン 12 および 13 についてデバイス IEC61000-4-2 ESD 分類レベル 4±8kV 接触放電
- MAC インターフェイス:MII、RMII、RGMII、SGMII
- VQFN、ウェッタブル フランク パッケージ
- IEEE 1588 SFD のサポート
- AVB/TSN の短い送信および受信レイテンシ
- 低い動作時消費電力: < 230mW
- 設定可能な I/O 電圧:3.3V、2.5V、1.8V
- パワー セービング機能:
  - スリープ、スタンバイ、ディセーブル
  - Wake-on-LAN (WoL)
- 診断ツール キット
  - 信号品質表示 (SQI)
  - 時間領域反射計測 (TDR)
  - 静電放電センサ
  - 電圧センサ
  - 温度センサ
  - PRBS 内蔵セルフテスト (BIST)

2 アプリケーション

- 先進運転支援システム (ADAS)
- ゲートウェイおよび車体制御
- テレマティクス

3 概要

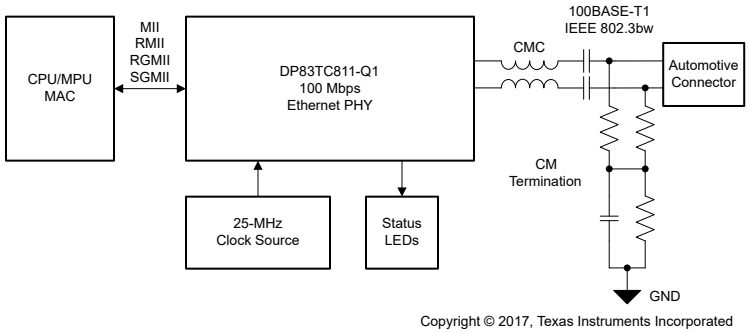
DP83TC811-Q1 デバイスは、IEEE 802.3bw 準拠の車載用 PHYTER™ イーサネット物理層トランシーバです。シールドなしの単一ツイストペア ケーブル上でデータを送受信するために必要な、すべての物理層機能が搭載されています。このデバイスは xMII の柔軟性があり、標準の MII、RMII、RGMII、SGMII MAC インターフェイスをサポートします。

このデバイスには診断ツールキットが含まれており、広範なリアルタイム監視ツール、デバッグ ツール、テスト モードが用意されています。ツール キットには、初めて内蔵された静電放電 (ESD) 監視ツールが含まれています。このツールは xMII と MDI の両方で ESD イベントをカウントでき、プログラム可能な割り込みを使用してリアルタイム監視も行えます。さらに、DP83TC811-Q1 には、疑似ランダム バイナリ シーケンス (PRBS) フレーム生成ツールが含まれており、内部ループバックと完全に互換性があり、MAC を使用せずデータを送受信します。DP83TC811-Q1 は、6.00mm × 6.00mm、36 ピンの VQFN ウェッタブル フランク パッケージに収容されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)(2)
DP83TC811RWRHA-Q1	RHA - VQFN (36)	6.00mm × 6.00mm
DP83TC811SWRHA-Q1	RHA - VQFN (36)	6.00mm × 6.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



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概略回路図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Device Comparison Table

PART NUMBER	SGMII SUPPORT	OPERATING TEMPERATURE
DP83TC811RWRHA-Q1	No	–40°C to 125°C
DP83TC811SWRHA-Q1	Yes	–40°C to 125°C

5 Pin Configuration and Functions

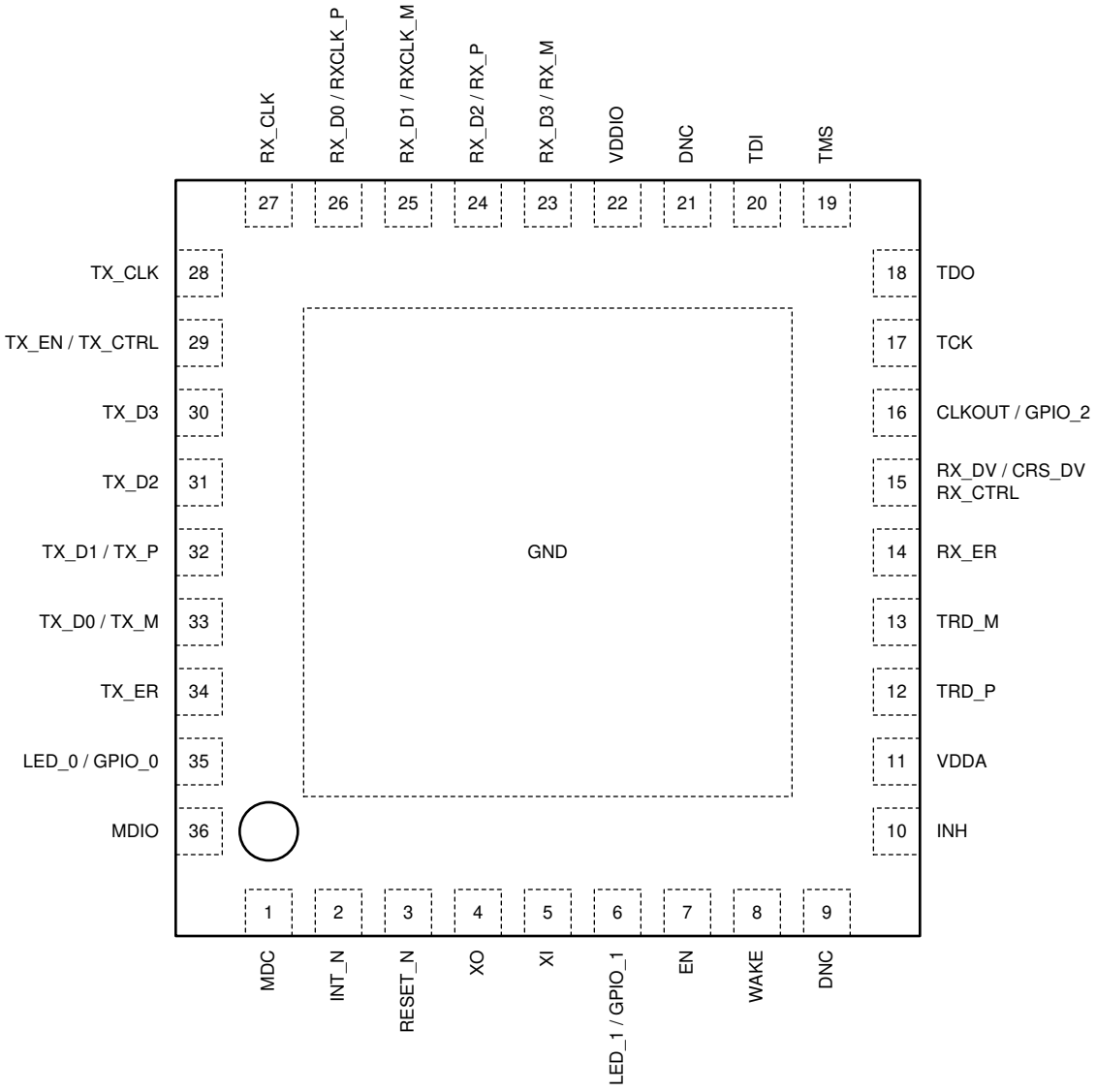


図 5-1. RND Package
36-Pin VQFN
Top View

5.1 Pin Functions

表 5-1. Pin Functions (2)

PIN		STATE(1)	DESCRIPTION
NAME	NO.		
MAC INTERFACE			
RX_D3 RX_M	23	S, PD, O	**Receive Data:** Symbols received on the cable are decoded and transmitted out of these pins synchronous to the rising edge of RX_CLK. They contain valid data when RX_DV is asserted. A data nibble, RX_D[3:0], is transmitted in MII and RGMII modes. 2 bits; RX_D[1:0], are transmitted in RMII mode. RX_D[3:2] are not used when in RMII mode. If the PHY is bootstrapped to RMII Master mode, a 50MHz clock reference is automatically outputted on RX_D3. This clock should be fed to the MAC. **RX_M / RX_P:** Differential SGMII Data Output. These pins transmit data from the PHY to the MAC. This data is synchronous to the differential SGMII clock output. **RXCLK_M / RXCLK_P:** Differential SGMII Clock Output. This signal is a continuous 625MHz clock signal driven by the PHY in 6-wire SGMII mode. *(configurable through register access)*
RX_D2 RX_P	24		
RX_D1 RXCLK_M	25		
RX_D0 RXCLK_P	26		
RX_CLK	27	O	**Receive Clock:** In MII and RGMII modes, the receive clock provides a 25MHz reference clock. **Unused in RMII and SGMII modes**
RX_ER	14	S, PD, O	**Receive Error:** In MII and RMII modes, this pin indicates a receive error symbol has been detected within a received packet. In MII mode, RX_ER is asserted high synchronously to the rising edge of RX_CLK. In RMII mode, RX_ER is asserted high synchronously to the rising edge of the reference clock. This pin is not required to be used by the MAC in MII or RMII because the PHY will automatically corrupt data on a receive error. **Unused in RGMII and SGMII modes**
RX_DV CRS_DV RX_CTRL	15	S, PD, O	**Receive Data Valid:** This pin indicates when valid data is presented on RX_D[3:0] for MII mode. **Carrier Sense Data Valid:** This pin combines carrier sense and data valid into an asynchronous signal. When CRS_DV is asserted, data is presented on RX_D[1:0] in RMII mode. **RGMII Receive Control:** Receive control combines receive data valid indication and receive error indication into a single signal. RX_DV is presented on the rising edge of RX_CLK and RX_ER is presented on the falling edge of RX_CLK. **Unused in SGMII mode**
TX_CLK	28	PD, I, O	**Transmit Clock:** In MII mode, the transmit clock is a 25MHz output and has constant phase referenced to the reference clock. In RGMII mode, this clock is sourced from the MAC layer to the PHY. A 25MHz clock should be provided (not required to have constant phase to the reference clock unless synchronous RGMII is enabled in *セクション 7.6.15*). **Unused in RMII and SGMII modes**
TX_EN TX_CTRL	29	PD, I	**Transmit Enable:** In MII mode, transmit enable is presented prior to the rising edge of the transmit clock. TX_EN indicates the presence of valid data inputs on TX_D[3:0]. In RMII mode, transmit enable is presented prior to the rising edge of the reference clock. TX_EN indicates the presence of valid data inputs on TX_D[1:0]. **RGMII Transmit Control:** Transmit control combines transmit enable and transmit error indication into a single signal. TX_EN is presented prior to the rising edge of TX_CLK; TX_ER is presented prior to the falling edge of TX_CLK. **Unused in SGMII mode**
TX_D3	30	PD, I	**Transmit Data:** In MII and RGMII modes, the transmit data nibble, TX_D[3:0], is received from the MAC prior to the rising edge of TX_CLK. In RMII mode, TX_D[1:0] is received from the MAC prior to the rising edge of the reference clock. TX_D[3:2] are not used in RMII mode. **TX_M / TX_P:** Differential SGMII Data Input. These pins receive data that is transmitted from the MAC to the PHY.
TX_D2	31		
TX_D1 TX_P	32		
TX_D0 TX_M	33		
TX_ER	34	PD, I	**Transmit Error:** In MII mode, this pin indicates a transmit error symbol has been detected within a transmitted packet. TX_ER is received prior to the rising edge of TX_CLK. **Unused in RMII, RGMII and SGMII modes**

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表 5-1. Pin Functions [2] (続き)

PIN		STATE[1]	DESCRIPTION
NAME	NO.		
SERIAL MANAGEMENT INTERFACE			
MDC	1	I	**Management Data Clock:** Synchronous clock to the MDIO serial management input and output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25MHz. There is no minimum clock rate.
MDIO	36	OD, IO	**Management Data Input/Output:** Bidirectional management data signal that may be sourced by the management station or the PHY. This pin requires a pullup resistor. Recommended to use a resistor between 2.2kΩ and 9kΩ.
CONTROL INTERFACE			
$\overline{\text{INT}}$	2	PU, OD, O	**Interrupt:** Active-LOW output, which will be asserted LOW when an interrupt condition occurs. This pin has a weak internal pullup. Register access is necessary to enable various interrupt triggers. Once an interrupt event flag is set, register access is required to clear the interrupt event. **Note:** Power-on-RESET (POR) Done interrupt is enabled by default. POR Done interrupt can be cleared by reading register *セクション 7.6.16*. This pin can be configured as an Active-HIGH output using register *セクション 7.6.9*.
$\overline{\text{RESET}}$	3	PU, I	**Reset:** Active-LOW input, which initializes or reinitializes the DP83TC811-Q1. Asserting this pin LOW for at least 1µs will force a reset process to occur. All internal registers will reinitialize to their default states as specified for each bit in the *セクション 7.6* section. All bootstrap pins are resampled upon deassertion of reset.
EN	7	PD, I	**Enable:** Active-HIGH input, which will disable the DP83TC811-Q1 when pulled LOW and power down all internal blocks. Disable state is equivalent to a power-down state. This pin can be directly tied to VDDIO; enabling the device.
WAKE	8	PD, I	**WAKE:** Active-HIGH input, which wakes the PHY from SLEEP. Asserting this pin HIGH at power-up will prevent the PHY from going to SLEEP. This pin can be directly tied to VDDIO to wake the device.
INH	10	O	**INH:** Active-HIGH output, which will be asserted HIGH when the PHY is in SLEEP or DISABLED. This pin is LOW for all other PHY states.
CLOCK INTERFACE			
XI	5	I	**Reference Clock Input (MII / RGMII / SGMII):** Reference clock 25MHz crystal or oscillator input. The device supports either an external crystal resonator connected across pins XI and XO, or an external CMOS-level oscillator connected to pin XI only and XO left floating. **Reference Clock Input (RMII):** Reference clock 50MHz CMOS-level oscillator in RMII Slave mode. Reference clock 25MHz crystal or oscillator in RMII Master mode. This is a fail-safe pin. When the PHY is not powered, an external oscillator is allowed to be powered and driving into this pin. Fail-safe prevents pin back-driving.
XO	4	O	**Reference Clock Output:** XO pin is used for crystal only. This pin should be left floating when a CMOS-level oscillator is connected to XI.
LED/GPIO INTERFACE			
LED_0 / GPIO_0	35	S, PD, IO	**LED_0:** Link Status
LED_1 / GPIO_1	6	S, PD, IO	**LED_1:** Link Status and BLINK for TX/RX Activity
CLKOUT / GPIO_2	16	IO	**Clock Output:** 25MHz reference clock
MEDIUM DEPENDENT INTERFACE			
TRD_M	13	IO	**Differential Transmit and Receive:** Bidirectional differential signaling configured for 100BASE-T1 operation, IEEE 802.3bw compliant.
TRD_P	12		
JTAG (IEEE 1149.1)			

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表 5-1. Pin Functions (2) (続き)

PIN		STATE(1)	DESCRIPTION
NAME	NO.		
TCK	17	PU, I	**Test Clock:** Primary clock source for all test logic input and output. This pin is controlled by the testing entity. This pin can be left unconnected if not used.
TDO	18	O	**Test Data Output:** Test results are scanned out. This pin can be left unconnected if not used.
TMS	19	PU, I	**Test Mode Select:** Sequences the Tap Controller (16-state FSM) to select the desired test instruction. TI recommends applying three clock cycles with TMS HIGH to reset JTAG. This pin can be left unconnected if not used.
TDI	20	PU, I	**Test Data Input:** Test data is scanned into the device. This pin can be left unconnected if not used.
POWER CONNECTIONS			
VDDA	11	SUPPLY	**Core Supply:** 3.3V Recommend using 10nF, 100nF, 1µF, and 10µF ceramic decoupling capacitors; optional ferrite bead.
VDDIO	22	SUPPLY	**IO Supply:** 1.8V, 2.5V, 3.3V Recommend using 10nF, 100nF, 1µF, and 10µF ceramic decoupling capacitors; optional ferrite bead.
GROUND	DAP	GROUND	**Ground**
DO NOT CONNECT			
DNC	9		**DNC:** Do not connect (leave floating)
DNC	21		**DNC:** Do not connect (leave floating)

(1) Pin Type:
I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup
S = Bootstrap configuration pin (all configuration pins have weak internal pullups or pulldowns)

(2) When pins are unused, follow the recommended connection requirements provided in the table above. If pins do not have required termination, they may be left floating.

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表 5-2. Pin States(1)

PIN NAME	POWER-UP / RESET			NORMAL OPERATION: MII / RMII / RGMII / SGMII		
	PIN STATE	PULL TYPE	PULL VALUE (kΩ)	PIN STATE	PULL TYPE	PULL VALUE (kΩ)
MDC	I	none	none	I	none	none
$\overline{\text{INT}}$	I	PU	9	OD, O	PU	9
$\overline{\text{RESET}}$	I	PU	9	I	PU	9
XO	O	none	none	O	none	none
XI	I	none	none	I	none	none
LED_1	HI-Z	PD	9	O	none	none
EN	I	PD	500	I	PD	500
WAKE	I	PD	500	I	PD	500
DNC	FLOAT	none	none	FLOAT	none	none
INH	O	none	none	O	none	none
VDDA	SUPPLY	none	none	SUPPLY	none	none
TRD_P	IO	none	none	IO	none	none
TRD_M	IO	none	none	IO	none	none
RX_ER	HI-Z	PD	9	O	none	none
RX_DV	HI-Z	PD	9	O	none	none
CLKOUT	O	none	none	O	none	none
TCK	I	PU	9	I	PU	9
TDO	O	none	none	O	none	none
TMS	I	PU	9	I	PU	9
TDI	I	PU	9	I	PU	9
DNC	FLOAT	none	none	FLOAT	none	none
VDDIO	SUPPLY	none	none	SUPPLY	none	none
RX_D3	HI-Z	PD	9	O	none	none
RX_D2	HI-Z	PD	9	O	none	none
RX_D1	HI-Z	PD	9	O	none	none
RX_D0	HI-Z	PD	9	O	none	none
RX_CLK	O	none	none	O	none	none
TX_CLK	I	PD	9	O I(2)	none PD(2)	none 9(2)
TX_EN	I	PD	9	I	PD	9
TX_D3	I	PD	9	I	PD	9
TX_D2	I	PD	9	I	PD	9
TX_D1	I	PD	9	I	PD	9
TX_D0	I	PD	9	I	PD	9
TX_ER	I	PD	9	I	PD	9
LED_0	HI-Z	PD	9	O	none	none
MDIO	OD, IO	none	none	OD, IO	none	none

(1) Type: I = Input
O = Output
IO = Input/Output
OD = Open Drain
PD = Internal pulldown
PU = Internal pullup

(2) Pin operation only for RGMII operation.

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5.2 Pin Multiplexing

GPIOs are controlled using *セクション 7.6.39* and *セクション 7.6.40*.

LED: Pin configured as LED indication. *セクション 7.6.37* determines LED function.
CLKOUT: Pin configured as a clock output signal
WoL: Pin configured to output WoL interrupt
UV: Pin configured to output undervoltage interrupt
1588_TX: Pin configured to output transmit 1588 SFD indication
1588_RX: Pin configured to output receive 1588 SFD indication
0s: Pin configured LOW (ground)
1s: Pin configured HIGH (VDDIO)
RMII_REF: Pin configured to output RMII 50MHz reference clock

表 5-3. Pin Multiplexing

FIELD	PIN	0b000	0b001	0b010	0b011	0b100	0b101	0b110	0b111	STRAP
LED_0 / GPIO_0	35	LED_0	CLKOUT_0	WoL	UV	Reserved	Reserved	0s	1s	
LED_1 / GPIO_1	6	LED_1	CLKOUT_1							
CLKOUT / GPIO_2	16	LED_2	CLKOUT_2							
RX_D3	23	RX_D3								RMII_REF

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VDDA	–0.3	4.0	V
Input voltage	VDDIO	–0.3	4.0	V
Input voltage	Other pins	–0.3	4.0	V
Input Voltage	MDI	-0.3	4.0	V
Input Voltage	All pins except MDI	-0.3	VDDIO + 0.3	V
DC output voltage	MDI	–0.3	VDDA + 0.3	V
DC output voltage	All Pins except MDI	–0.3	VDDIO + 0.3	V
DC output voltage	All Pins	–0.3	4.0	V
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±4000	V
		Charged device model (CDM), per AEC Q100-011	All pins except XI pin	±750	
			XI pin(2)	±250	
		IEC 61000-4-2 contact discharge	TRD_N, TRD_P pins	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) XI pin is a fail-safe input.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DDIO}	IO Supply Voltage, 1.8V operation	1.62	1.8	1.98	V
V_{DDIO}	IO Supply Voltage, 2.5V operation	2.25	2.5	2.75	V
V_{DDIO}	IO Supply Voltage, 3.3V operation	2.97	3.3	3.63	V
V_{DDA}	Core Supply Voltage	2.97	3.3	3.63	V
T_A	Operating Free Air Temperature	–40		125	°C

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6.4 Thermal Information

THERMAL METRIC[1]		DP83TC811-Q1 VQFN - RHA 36 pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	14.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
XI pin, WAKE pin and EN pin						
V_{IH}	High Level Input Voltage		1.3			V
V_{IL}	High Level Input Voltage				0.5	V
3.3V VDDIO[1]						
V_{OH}	High Level Output Voltage	IOH = -2mA VDDIO = 3.3V +/- 10%	2.4			V
V_{OL}	Low Level Output Voltage	IOL = 2mA VDDIO = 3.3V +/- 10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 3.3V +/- 10%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V +/- 10%			0.8	V
2.5V VDDIO[1]						
V_{OH}	High Level Output Voltage	IOH = -2mA VDDIO = 2.5V +/- 10%	2			V
V_{OL}	Low Level Output Voltage	IOL = 2mA VDDIO = 2.5V +/- 10%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V +/- 10%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V +/- 10%			0.7	V
1.8V VDDIO[1]						
V_{OH}	High Level Output Voltage	IOH = -2mA VDDIO = 1.8V +/- 10%	VDDIO – 0.45			V
V_{OL}	Low Level Output Voltage	IOL = 2mA VDDIO = 1.8V +/- 10%			0.45	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V +/- 10%	0.65 * VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V +/- 10%			0.35 * VDDIO	V
DC CHARACTERISTICS						
I_{IH}	Input High Current	VIN = VDDIO	-30		30	µA
I_{IL}	Input Low Current	VIN = GND	-30		30	µA
I_{OZ}	TRI-STATE Output Current[2]	VOUT = VDDIO, VOUT = GND	-75		75	µA
C_{IN}	Input Capacitance	Input pins		5		pF
		XI		1		pF
C_{OUT}	Output Capacitance	Output pins		5		pF
		XO		1		pF
$R_{pull-up}$	Integrated Pull-Up Resistance	$\overline{RESET}$, $\overline{INT}$, TCK, TMS and TDI	6.5	9	12.5	kΩ

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6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{pull-down}$	Integrated Pull-Down Resistance	RX_D[3:0], RX_ER, RX_DV, TX_EN, TX_D[3:0], TX_ER, LED_0 and LED_1	6.75	9	11.25	kΩ
		WAKE and EN		500		kΩ
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV and RX_CLK		50		Ω
CURRENT CONSUMPTION						
$I_{DDIO-1V8-ACT}$	IO Supply Current, 1.8V operation, Active/ Normal Mode	MII		18	22	mA
		RMII		6	12	
		RGMII		10	13	
$I_{DDIO-SGMII-1V8-ACT}$	IO Supply Current, 1.8V operation, Active/ Normal Mode	SGMII 6-wire		32	40	mA
		SGMII 4-wire		24	31	
$I_{DDIO-1V8-STBY}$	IO Supply Current, 1.8V operation, Standby	MII		13	17	mA
		RMII		3	10	
		RGMII		8	10	
$I_{DDIO-SGMII-1V8-STBY}$	IO Supply Current, 1.8V operation, Standby	SGMII 6-wire		7	10	mA
		SGMII 4-wire		7	10	
$I_{DDIO-1V8-RST}$	IO Supply Current, 1.8V operation, Reset	All Interfaces		6	10	mA
$I_{DDIO-1V8-SLP}$	IO Supply Current, 1.8V operation, Sleep	All Interfaces		8	90	µA
$I_{DDIO-1V8-DIS}$	IO Supply Current, 1.8V operation, Disable	All Interfaces		8	85	µA
$I_{DDIO-2V5-ACT}$	IO Supply Current, 2.5V operation, Active/ Normal Mode	MII		24	28	mA
		RMII		14	24	
		RGMII		12	17	
$I_{DDIO-SGMII-2V5-ACT}$	IO Supply Current, 2.5V operation, Active/ Normal Mode	SGMII 6-wire		36	44	mA
		SGMII 4-wire		28	34	
$I_{DDIO-2V5-STBY}$	IO Supply Current, 2.5V operation, Standby	MII		18	22	mA
		RMII		11	21	
		RGMII		10	13	
$I_{DDIO-SGMII-2V5-STBY}$	IO Supply Current, 2.5V operation, Standby	SGMII 6-wire		9	12	mA
		SGMII 4-wire		9	12	
$I_{DDIO-2V5-RST}$	IO Supply Current, 2.5V operation, Reset	All Interfaces		8	18	mA
$I_{DDIO-2V5-SLP}$	IO Supply Current, 2.5V operation, Sleep	All Interfaces		11	95	µA
$I_{DDIO-2V5-DIS}$	IO Supply Current, 2.5V operation, Disable	All Interfaces		11	93	µA
$I_{DDIO-3V3-ACT}$	IO Supply Current, 3.3V operation, Active/ Normal Mode	MII		31	37	mA
		RMII		22	36	
		RGMII		16	21	
$I_{DDIO-SGMII-3V3-ACT}$	IO Supply Current, 3.3V operation, Active/ Normal Mode	SGMII 6-wire		40	50	mA
		SGMII 4-wire		31	39	

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6.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DDIO-3V3-STBY}$	IO Supply Current, 3.3V operation, Standby	MII		24	29	mA
		RMII		19	33	
		RGMII		13	17	
$I_{DDIO-SGMII-3V3-STBY}$	IO Supply Current, 3.3V operation, Standby	SGMII 6-wire		12	15	mA
		SGMII 4-wire		12	15	
$I_{DDIO-3V3-RST}$	IO Supply Current, 3.3V operation, Reset	All Interfaces		15	30	mA
$I_{DDIO-3V3-SLP}$	IO Supply Current, 3.3V operation, Sleep	All Interfaces		14	100	µA
$I_{DDIO-3V3-DIS}$	IO Supply Current, 3.3V operation, Disable	All Interfaces		14	100	µA
$I_{DDA-ACT}$	Core Supply Current; MII, RMII, RGMII	Active/Normal Mode		65	110	mA
$I_{DDA-STBY}$		Standby		20	55	mA
$I_{DDA-SGMII-ACT}$	Core Supply Current; Active/Normal mode	SGMII 4-wire		89	130	mA
		SGMII 6-wire		93	135	
$I_{DDA-SGMII-STBY}$	Core Supply Current; Standby	SGMII 4-wire		12	55	mA
		SGMII 6-wire		12	55	
$I_{DDA-RST}$	Core Supply Current; All Interfaces	Reset		13	44	mA
$I_{DDA-SLP}$		Sleep		51	186	µA
$I_{DDA-DIS}$		Disable		51	185	µA
MDI CHARACTERISTICS						
V_{OD-MDI}	Output Differential Voltage				2.2	V
R_{mdi_diff}	Integrated Differential MDI Termination	TRD_P and TRD_M		100		Ω
SGMII DRIVER DC SPECIFICATIONS						
$V_{OD-SGMII}$	Output Differential Voltage		150		400	mV
R_{out_diff}	Integrated Differential Output Termination	RX_P and RX_M, RXCLK_P and RXCLK_M		100		Ω
SGMII RECEIVER DC SPECIFICATIONS						
V_{idth}	Input Differential Threshold		100			mV
R_{in_diff}	Integrated Differential Input Termination	TX_P and TX_M		100		Ω
BOOTSTRAP DC CHARACTERISTICS						
V_{bs_1}	Bootstrap Threshold	Mode 1	0	0	0.08 x VDDIO	V
V_{bs_2}		Mode 2	0.148 x VDDIO	0.165 x VDDIO	0.181 x VDDIO	V
V_{bs_3}		Mode 3	0.235 x VDDIO	0.252 x VDDIO	0.277 x VDDIO	V
V_{bs_4}		Mode 4	0.694 x VDDIO	VDDIO	VDDIO	V

(1) For pins: MDC, INT_N, RESET_N, XO, LED_1, RX_ER, RX_DV, CLKOUT, TCK, TDO, TMS, TDI, RX_D[3:0], RX_CLK, TX_CLK, TX_EN, TX_D[3:0], TX_ER, LED_0, and MDIO
(2) For pins: RX_D[3:0], RX_CLK, RX_ER, RX_DV, TX_CLK, MDIO, INT_N, XO, and TDO

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6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
MII TIMING					
T1.1	TX_CLK High / Low Time	16	20	24	ns
T1.2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	10			ns
T1.3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
T2.1	RX_CLK High / Low Time	16	20	24	ns
T2.2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	14	20	26	ns
RMII SLAVE TIMING					
T3.1	Reference Clock Period		20		ns
	Reference Clock Duty Cycle	35	50	65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to XI Clock	4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from XI Clock	2			ns
T3.4	RX_D[1:0], RX_ER Delay from XI Clock rising(2)	3	6	12	ns
RMII MASTER TIMING(1)					
T3.1	RMII Master Clock Period		20		ns
	RMII Master Clock Duty Cycle	35	50	65	%
T3.2	TX_D[1:0], TX_ER, TX_EN Setup to RMII Master Clock	4			ns
T3.3	TX_D[1:0], TX_ER, TX_EN Hold from RMII Master Clock	2			ns
T3.4	RX_D[1:0], RX_ER Delay from RMII Master Clock rising(2)	4	6	12	ns
RGMII TIMING					
$T_{skew\ (Align)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Align Mode Enabled)	–600	0	600	ps
$T_{skew\ (Shift)}$	RX_D[3:0], RX_CTRL Delay from RX_CLK (Shift Mode Enabled)	1.2	2		ns
$T_{setup\ (Align)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Align Mode Enabled)	1			ns
$T_{setup\ (Shift)}$	TX_D[3:0], TX_CTRL Setup to TX_CLK (Shift Mode Enabled)	–1			ns
$T_{hold\ (Align)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Align Mode Enabled)	1			ns
$T_{hold\ (Shift)}$	TX_D[3:0], TX_CTRL Hold from TX_CLK (Shift Mode Enabled)	3			ns
T_{cyc}	Clock Cycle Duration	36	40	44	ns
	Duty Cycle	40	50	60	%
Tr/Tf	Rise / Fall Time (20% - 80%)(3)		750	1200	ps
SGMII DRIVER AC SPECIFICATIONS					
	Clock signal duty cycle at 625MHz	48		52	%
T_{rise}	Vod Rise Time	100		200	ps
T_{fall}	Vod Fall Time	100		200	ps
tskew1	Skew between two members of a differential pair			20	ps
Jitter	Output Jitter			300	ps
tclock2q	Clock to Data relationship: from either edges of the clock to valid data	250		500	ps
SMI TIMING					
T4.1	MDC to MDIO (Output) Delay Time	0	6	12.5	ns
T4.2	MDIO (Input) to MDC Setup Time	10			ns
T4.3	MDIO (Input) to MDC Hold Time	10			ns
	MDC Frequency		2.5	25	MHz
POWER-UP TIMING					
T5.1	VDDA ramp rate	0.165		33	V/ms
T5.1	VDDIO ramp rate	0.165		33	V/ms
T5.2	VDDA and VDDIO ramp delay offset	–50		50	ms

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6.6 Timing Requirements (続き)

		MIN	NOM	MAX	UNIT
T5.3	Crystal stabilization time post power-up		350		µs
T5.4	Osillator stabilization time post power-up			40	ms
T5.5	Post power-up stabilization-time prior to MDC preamble for register access			60	ms
T5.6	Hardware configuration latch-in time from power-up			60	ms
T5.7	Hardware configuration pins transition to functional mode from latch-in completion			200	ns
T5.8	PAM3 IDLE Stream from power-up (Master Mode)			60	ms
RESET TIMING (RESET_N)					
T6.1	RESET pulse width	1			µs
T6.2	Post reset stabilization-time prior to MDC preamble for register access			2.5	µs
T6.3	Hardware configuration latch-in time from reset			700	ns
T6.4	Hardware configuration pins transition to functional mode from latch-in completion			200	ns
T6.5	PAM3 IDLE Stream from reset (Master Mode)			300	µs
TRANSMIT LATENCY TIMING					
T7.1	MII Rising edge TX_CLK with assertion TX_EN to SSD symbol on MDI	140		172	ns
	Slave RMII Rising edge XI clock with assertion TX_EN to SSD symbol on MDI	304		372	ns
	Master RMII Rising edge clock with assertion TX_EN to SSD symbol on MDI	322		382	ns
	RGMII Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI	134			ns
	Bit sequence 0b1101101000 to SSD symbol on MDI	401		440	ns
RECEIVE LATENCY TIMING					
T8.1	SSD symbol on MDI to MII Rising edge of RX_CLK with assertion of RX_DV	366		406	ns
	SSD symbol on MDI to Slave RMII Rising edge of XI clock with assertion of CRS_DV	434		513	ns
	SSD symbol on MDI to Master RMII Rising edge of Master clock with assertion of CRS_DV	438		525	ns
	SSD symbol on MDI to Rising edge of RGMII RX_CLK with assertion of RX_CTRL	385		417	ns
	SSD symbol on MDI to SFD (/S/) comprising bit sequence 0b1101101000	582		643	ns
25MHz OSCILLATOR REQUIREMENTS					
	Frequency		25		MHz
	Frequency Tolerance and Stability Over temperature and aging	–100		100	ppm
	Rise / Fall Time (10% - 90%)			8	ns
	Jitter (Short-term, Cycle-to-Cycle)			800	ps
	Jitter (Long-term, Accumulative over 10ms)			2	ns
	Duty Cycle	40		60	%
50MHz OSCILLATOR REQUIREMENTS					
	Frequency		50		MHz
	Frequency Tolerance and Stability Over temperature and aging	–100		100	ppm
	Rise / Fall Time (10% - 90%)			4	ns
	Jitter (Short-term, Cycle-to-Cycle)			800	ps
	Jitter (Long-term, Accumulative over 10ms)			2.5	ns
	Duty Cycle	40		60	%

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6.6 Timing Requirements (続き)

		MIN	NOM	MAX	UNIT
25MHz CRYSTAL REQUIREMENTS					
	Frequency		25		MHz
	Frequency Tolerance and Stability Over temperature and aging	–100		100	ppm
	Equivalent Series Resistance			50	Ω
OUTPUT CLOCK TIMING (CLKOUT)					
	Frequency		25		MHz
	Duty Cycle	45		55	%
	Rise / Fall Time (20% - 80%)			1	ns
	Jitter (Short-term, Cycle-to-Cycle)			200	ps
	Jitter (Long-term, Accumulative over 10ms)			125	ps

(1) RMII Master Clock is in reference to the 50MHz clock output on RX_D3 when the device is configured for RMII Master mode through hardware bootstrap.
(2) CRS_DV is an asynchronous signal as defined by the RMII version 1.2 specification.
(3) RGMII rise/fall time control register configurable

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6.7 Timing Diagrams

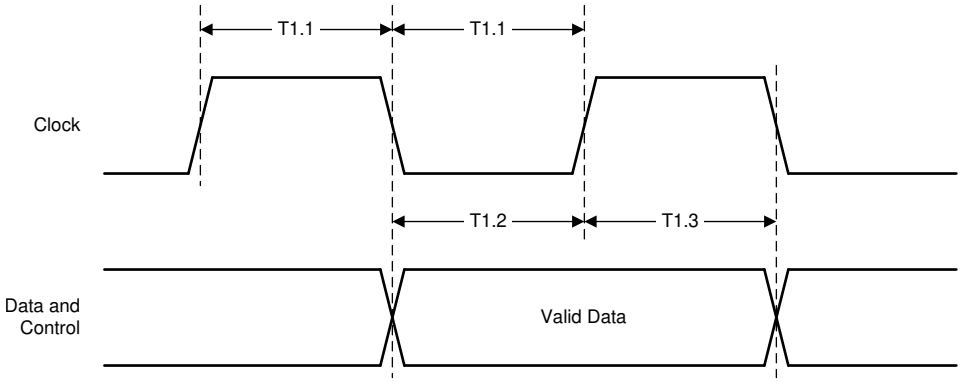


図 6-1. MII Transmit Timing

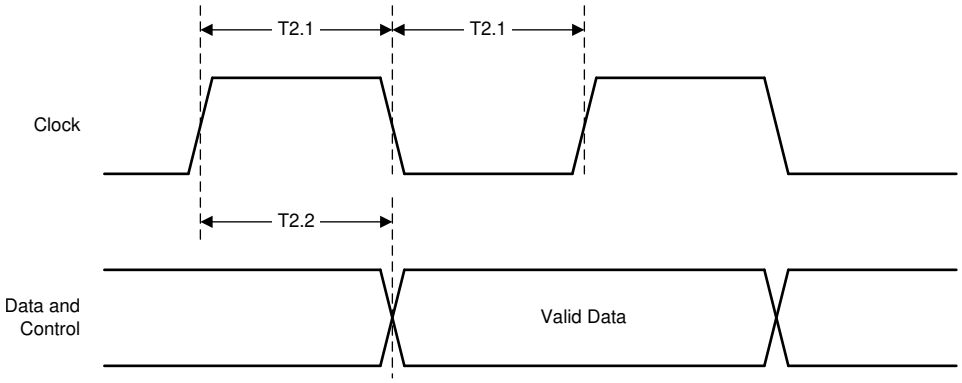


図 6-2. MII Receive Timing

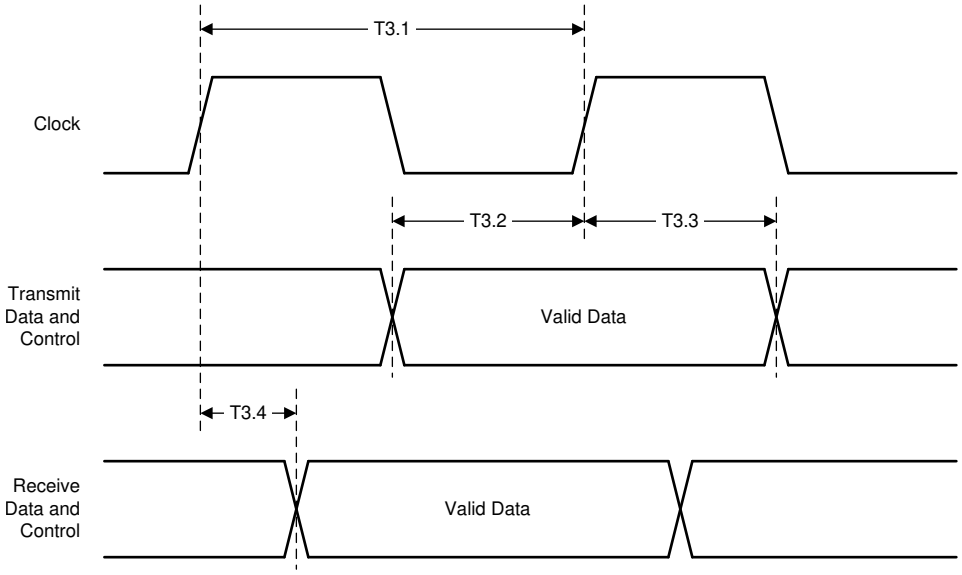


図 6-3. RMII Transmit and Receive Timing

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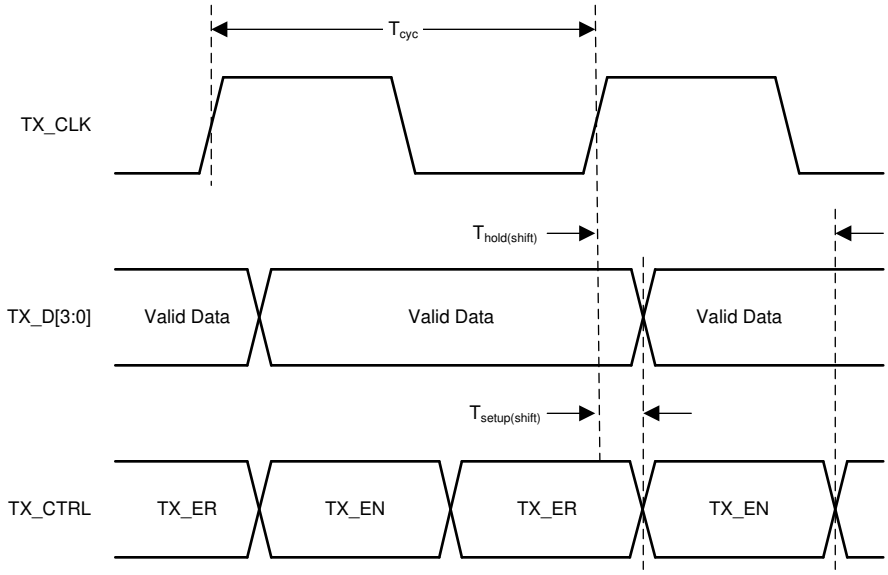


図 6-4. RGMII Transmit Timing (Internal Delay Enabled)

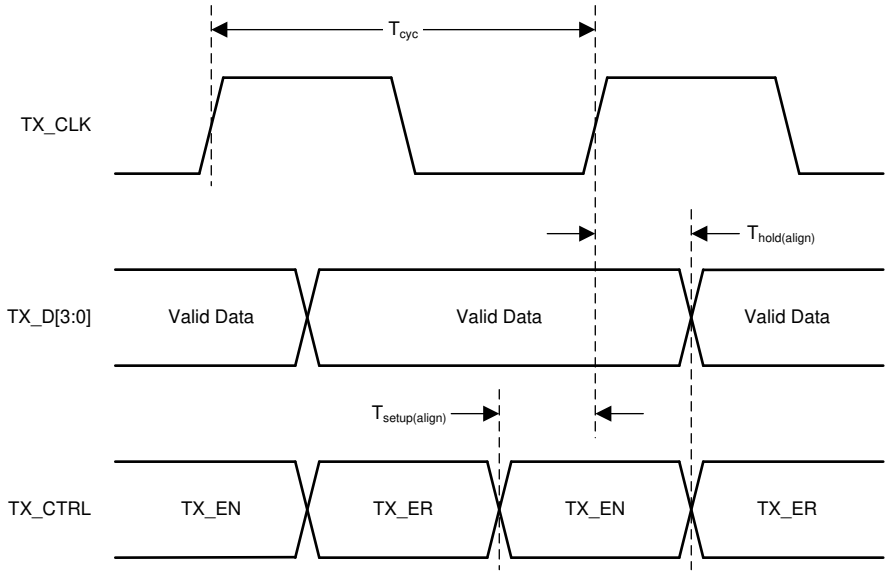


図 6-5. RGMII Transmit Timing (Internal Delay Disabled)

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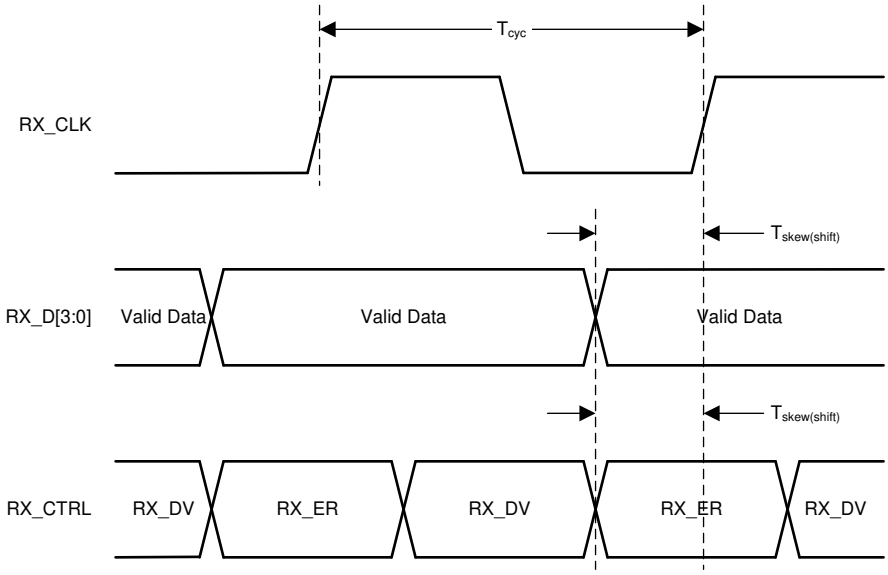


図 6-6. RGMII Receive Timing (Internal Delay Enabled)

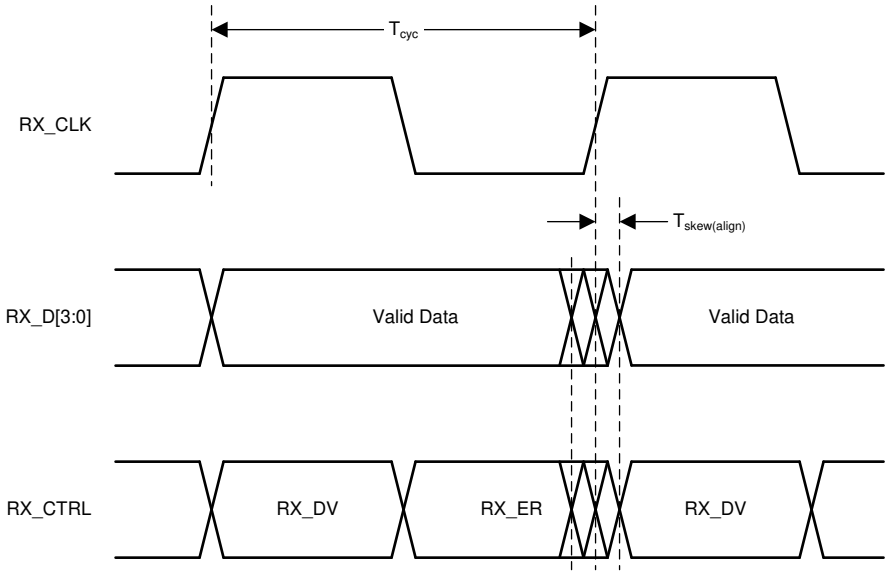


図 6-7. RGMII Receive Timing (Internal Delay Disabled)

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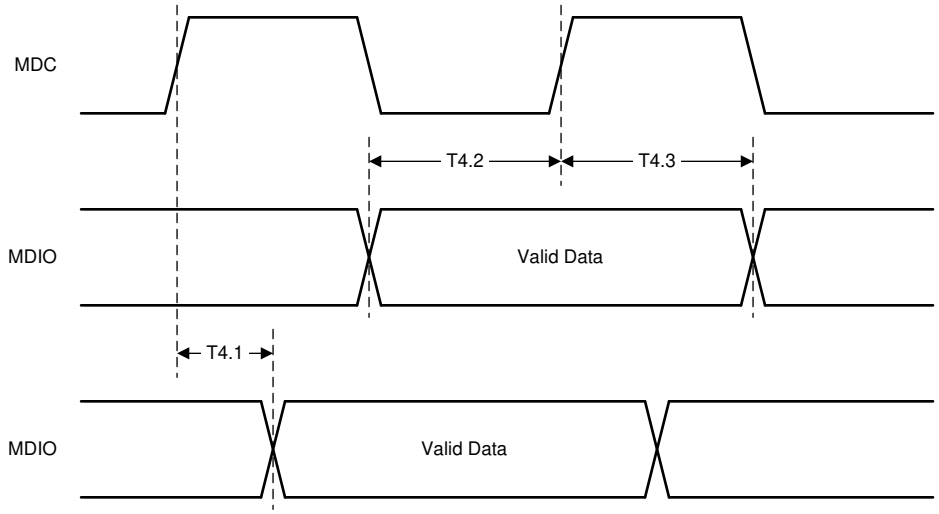


図 6-8. Serial Management Timing

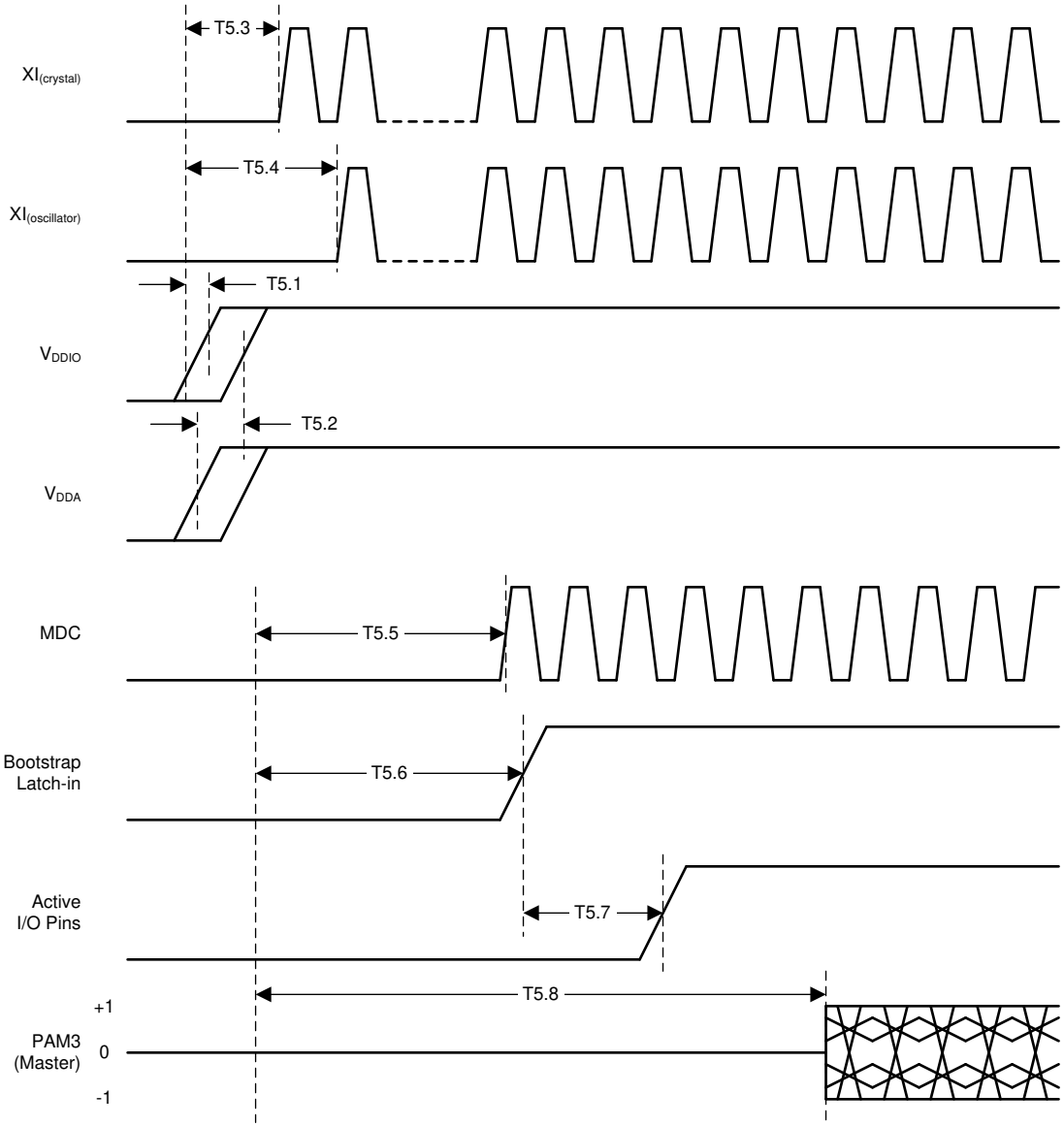


図 6-9. Power-Up Timing

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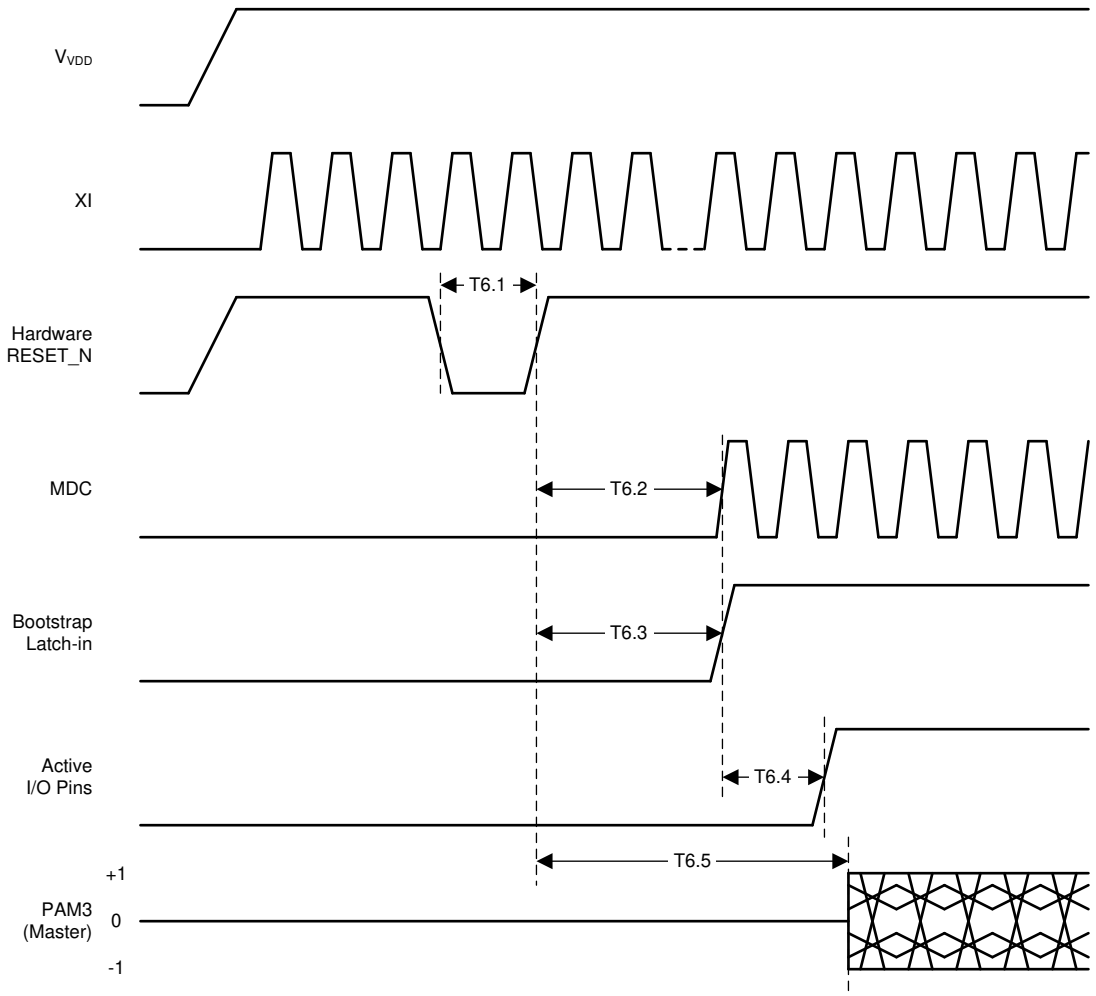


図 6-10. Reset Timing

7 Detailed Description

7.1 Overview

The DP83TC811-Q1 is a 100BASE-T1 automotive Ethernet Physical Layer transceiver. It is IEEE 802.3bw compliant and AEC-Q100 qualified for automotive applications. The DP83TC811-Q1 is interoperable with both BroadR-Reach PHYs and 100BASE-T1 PHYs.

This device is specifically designed to operate at 100Mbps speed while meeting CISPR-25 Level 5 limits. The DP83TC811-Q1 transmits PAM3 ternary symbols at 66.667MHz over unshielded single twisted-pair cable. It is application flexible; supporting MII, RMII, RGMII, and SGMII in a single 36-pin VQFN wettable flank package.

There is an extensive Diagnostic Tool Kit within the DP83TC811-Q1 for both in-system use as well as debug, compliance and system prototyping for bring-up. Not only is the DP83TC811-Q1 designed for IEC61000-4-2 Level 4 electrostatic discharge limits, but also includes an on-chip ESD sensor for detecting ESD events in real-time.

The DP83TC811-Q1 is built for minimal thermal footprint with low active power as well multiple low-power modes. It supports Wake-on-LAN Magic Packets and Custom Pattern detection, allowing upstream devices an option for entering into their own low-power state. Additionally, the device can enter into Sleep state and remain until energy is detected on the MDI or locally woken through the WAKE pin.

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7.2 Functional Block Diagram

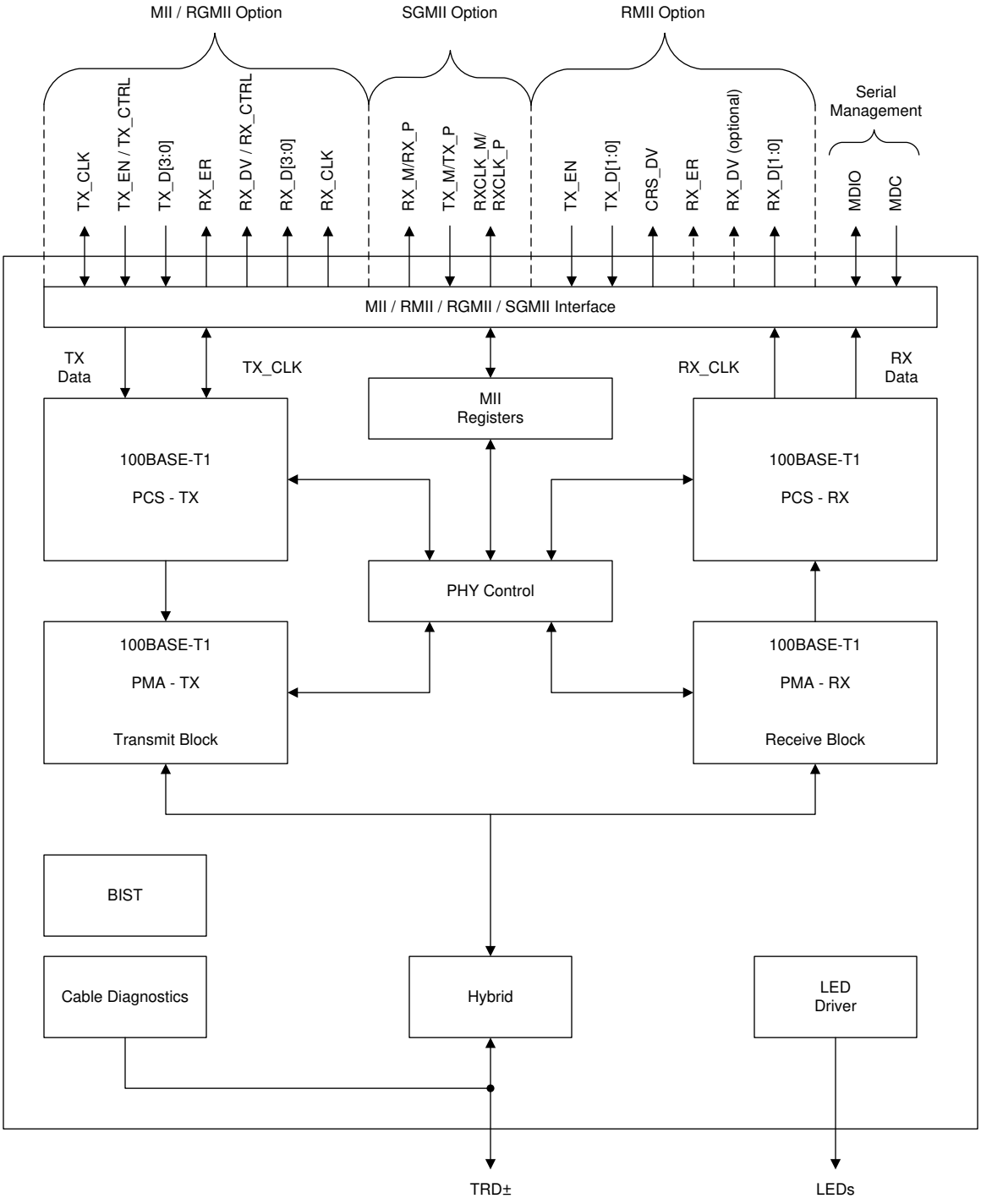


図 7-1. DP83TC811-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Wake-on-LAN (WoL) Packet Detection

Wake-on-LAN provides a mechanism to detect specific frames and notify the connected controller through either register status change, GPIO indication or an interrupt flag. WoL within the DP83TC811-Q1 allows for connected devices residing above the Physical Layer to remain in a low-power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet, Magic Packet with Secure-ON, and Custom Pattern Match. When a qualifying WoL frame is received, the DP83TC811-Q1 WoL logic circuit is able to generate a user defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred. Additionally, the DP83TC811-Q1 includes a CRC Gate to prevent invalid packets from triggering a wake-up event.

The WoL feature set includes:

- Wake-up interrupt generation upon receiving a valid Magic Packet or Pattern
- CRC checking of Magic Packets to prevent interrupt generation for invalid packets
- Magic Packets with Secure-ON password and 64-byte Custom Pattern Match

7.3.1.1 Magic Packet Structure

When configured for Magic Packet mode, the DP83TC811-Q1 scans all incoming frames addressed to the node for a specific sequence. This sequence identifies the frame as a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station's IEEE address or a BROADCAST ADDRESS), and CRC. The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions, followed by Secure-ON password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6-bytes of FFh.

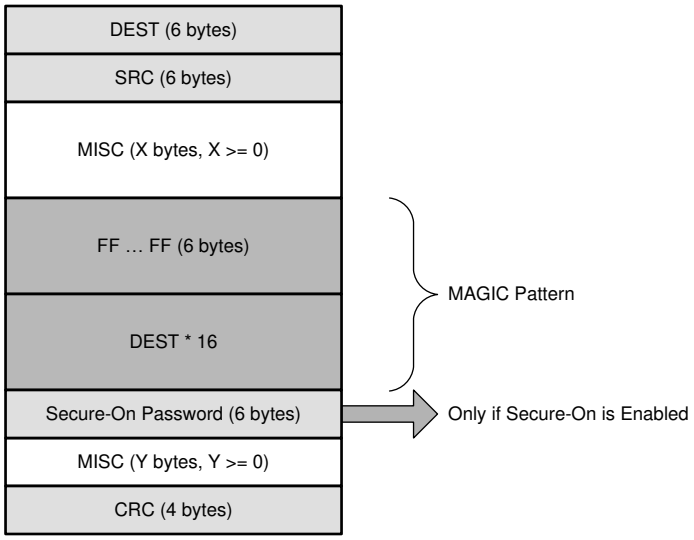


図 7-2. Magic Packet Structure

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7.3.1.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a Secure-ON password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

DESTINATION SOURCE MISC FF FF FF FF FF FF

11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66

11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC

7.3.1.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the *セクション 7.6.56*. Wake-on-LAN status is reported in the *セクション 7.6.57*. Wake-on-LAN interrupt flag configuration and status is located in the *セクション 7.6.10*.

7.3.2 Start of Frame Detect for IEEE 1588 Time Stamp

IEEE 802.3bw uses 4B3B encoding (3B4B decoding), reducing a 4-bit data path operating at 25MHz down to a 3-bit data path operating at 33.334MHz. For frames and inter-packet gaps that are not divisible by three, one to two stuff bits are added at the end of a transmitted frame. These stuff bits are removed by the link partner before the data is routed to the MAC, making it completely transparent to layers above the Physical layer. These stuff bits cause frame jitter.

The DP83TC811-Q1 supports an IEEE 1588 indication pulse at the SFD (start of frame delimiter) for receive and transmit paths. The 1588 SFD pulse indicates the actual time the symbol is presented on the lines (for transmit), or the first symbol received (for receive), which provides a deterministic reference point. The pulse can be transmitted out of any of the following pins: LED_0 (GPIO_0), LED_1 (GPIO_1), or CLKOUT (GPIO_2).

There are two registers that are able to control the routing of the IEEE 1588 transmit and receive indications. The *セクション 7.6.39* is able to route both transmit and receive indications to LED_0 (GPIO_0) and LED_1 (GPIO_1). CLKOUT transmit and receive 1588 SFD indication is found in the *セクション 7.6.40*.

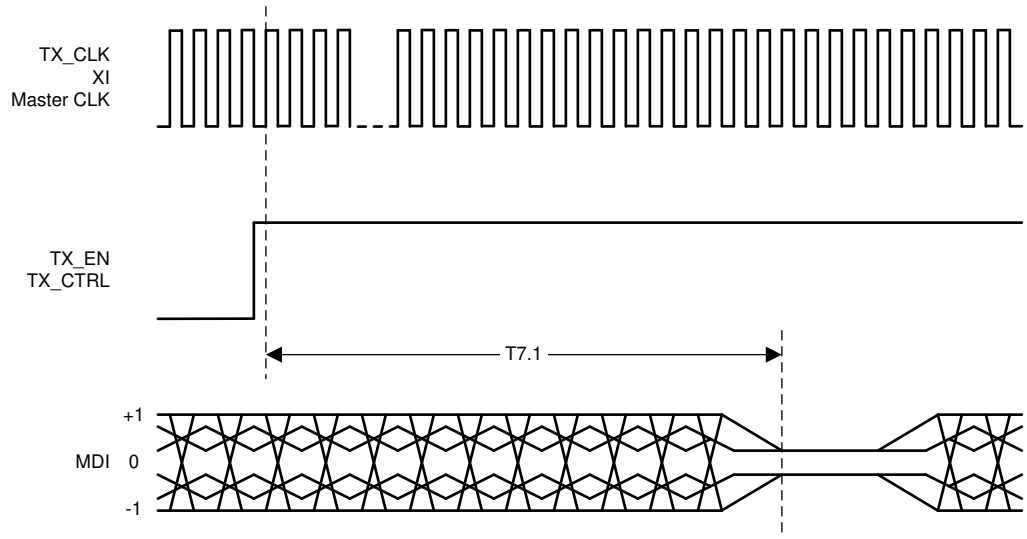


図 7-3. Transmit Latency

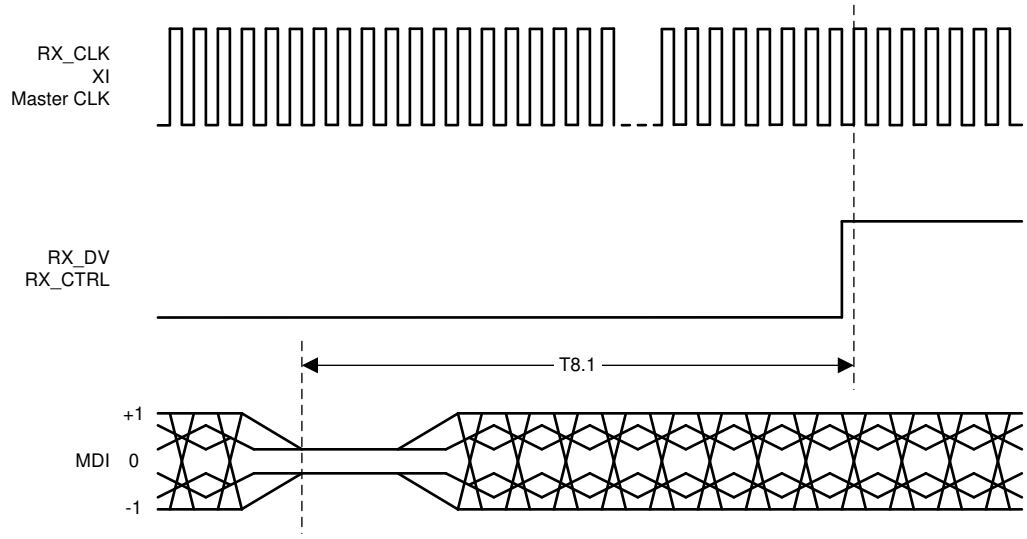


図 7-4. Receive Latency

7.3.3 Diagnostic Tool Kit

The DP83TC811-Q1 diagnostic tool kit provides mechanisms for monitoring normal operation, device-level debugging, system-level debugging, fault detection, and compliance testing. This tool kit includes a built-in self-test with PRBS data, various loopback modes, Signal Quality Indicator (SQI), Time Domain Reflectometry (TDR), undervoltage monitor, overtemperature monitor, electrostatic discharge monitor, and IEEE 802.3bw test modes.

7.3.3.1 Signal Quality Indicator

When the DP83TC811-Q1 is active, the Signal Quality Indicator may be used to determine the quality of link based on SNR readings made by the device. SQI is presented as both a four-level indication and a percentage based on the calculated SNR value. Signal quality indication is accessible through the *セクション 7.6.29*. SQI is continuously monitored by the DP83TC811-Q1 to allow for real-time link signal quality status.

Bits[9:8] in register 0x198 provide signal quality status. For SQI value, convert bits[7:0] to decimal form.

表 7-1. Signal Quality Indicator

BIT[9]	BIT[8]	SIGNAL QUALITY STATUS	SIGNAL QUALITY INDICATION
0	0	No Link	SQI ≤ 40
0	1	Intermittent/Poor Link	
1	0	Good Link	40 < SQI ≤ 70
1	1	Excellent Link	SQI > 70

Signal-to-noise ratio is accessible through the *セクション 7.6.28*. To convert this binary register field to dB, follow these steps:

1. Convert bits[7:0] in register 0x197 to decimal form
2. Divide decimal value by 10
3. Result is SNR (dB) reading

7.3.3.2 Electrostatic Discharge Sensing

Electrostatic discharge is a serious issue for electronic circuits and if not properly mitigated can create short-term issues (signal integrity, link drops, packet loss) as well as long-term reliability faults. The DP83TC811-Q1 has robust integrated ESD circuitry and offers an ESD sensing architecture. ESD events can be detected on both the xMII and MDI pins independently for further analysis and debug.

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Additionally, the DP83TC811-Q1 provides an interrupt status flag; bit[11] in the セクション 7.6.10 when an ESD event is logged in the セクション 7.6.34. Hardware and software resets are ignored by the ESDS register to prevent unwarranted clearing.

7.3.3.3 Time Domain Reflectometry

Time domain reflectometry helps determine the quality of the cable, connectors and terminations in addition to estimating OPEN and SHORT faults along a cable. The DP83TC811-Q1 transmits a test pulse down the attached twisted-pair cable. Transmitted pulses continue down the cable and reflect from each imperfection and fault, allowing the device to measure the time to return and strength (amplitude) of all reflections. This technique enables the DP83TC811-Q1 to identify cable OPENs and SHORTs.

TDR is activated by setting bit[15] in the セクション 7.6.19. Cable diagnostic status is obtained by reading bits[1:0] in the TDR register. TDR runs are stored in the セクション 7.6.22. When more than one fault is present, additional locations are identified by the セクション 7.6.23 and the セクション 7.6.25.

7.3.3.4 Temperature and Voltage Sensing

Overtemperature and undervoltage monitoring are always active in the DP83TC811-Q1 by default. If an overtemperature condition, an undervoltage condition, or both conditions are detected, interrupt status flags are set in the セクション 7.6.11. Additionally, temperature and voltage monitoring cycle period can be adjusted using the セクション 7.6.44 bits[2:0]. By default, sample time is set to 31ms, but also has a configurable range of 16ms to 240ms. Single-run temperature and voltage monitoring is also supported when bit[1] is set to 0b0 in the セクション 7.6.45, disabling period monitoring. To activate a single run, bit[0] in MON_CFG2 register must be set after disabling period monitoring. Temperature monitor results are available in the セクション 7.6.47. VDDA and VDDIO supply monitor results are available in the セクション 7.6.48.

7.3.3.5 Built-In Self-Test

The DP83TC811-Q1 incorporates an internal PRBS Built-in Self-Test (BIST) circuit to accommodate in-circuit testing and diagnostics. The BIST circuit can be used to test the integrity of transmit and receive data paths. BIST can be enabled while using internal loopbacks (MII, PCS or analog) or external loopback when using a Link Partner configured for Reverse Loopback. BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. It allows full control over packet lengths and IPG.

BIST Packet Length is controlled using bits[10:0] in the セクション 7.6.18. BIST IPG Length is controlled using bits[7:0] in the セクション 7.6.17.

BIST is implemented with independent transmit and receive paths, with the transmit clock generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for BIST. Received data is compared to the generated pseudo-random data to determine pass or fail status. The number of error bytes that the PRBS checker received is stored in bits[15:8] of the BICSR1 register. PRBS lock status and sync can be read from the セクション 7.6.14.

PRBS test can be put in continuous mode using bit[14] in the BISCR register. In continuous mode, when the BIST error counter reaches its maximum value, the counter starts counting from zero again. To read the BIST error count, bit[15] in the BICSR1 register must be set to 0b1. This will lock the current number of BIST errors for read-back. Note that setting bit[15] also clears the BIST error counter.

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7.3.3.6 Loopback Modes

There are several loopback options within the DP83TC811-Q1 that test and verify various functional blocks within the PHY. Loopback modes also provide on-board and system level verification testing and debug.

7.3.3.6.1 xMII Loopback

xMII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. When in xMII Loopback, data transmitted from a connected MAC on the TX path is internally looped back in the DP83TC811-Q1 to the RX pins where it can be checked by the MAC. There is no link indication when in xMII loopback.

xMII Loopback is enabled by setting bit[14] in the *セクション 7.6.2*.

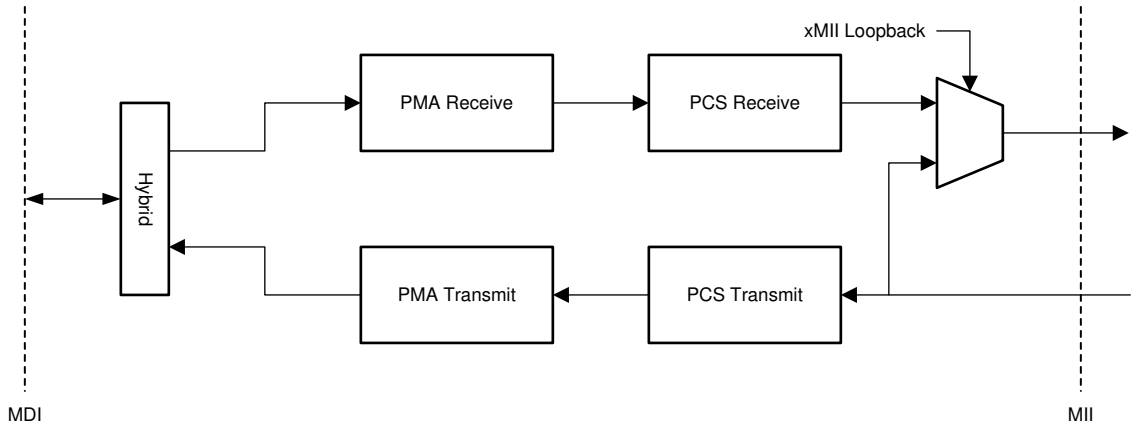


図 7-5. xMII Loopback

7.3.3.6.2 PCS Loopback

PCS Loopback will loop back data prior to it exiting the PCS and entering the PMA. Data received from the MAC on the transmit path is brought through the digital block within the PHY where it is then routed back to the MAC through the receive path. The DP83TC811-Q1 receive PMA circuitry is configured for isolation to prevent contention.

PCS Loopback is enabled by setting bits[6:2] = 0b0001 in the *セクション 7.6.14*.

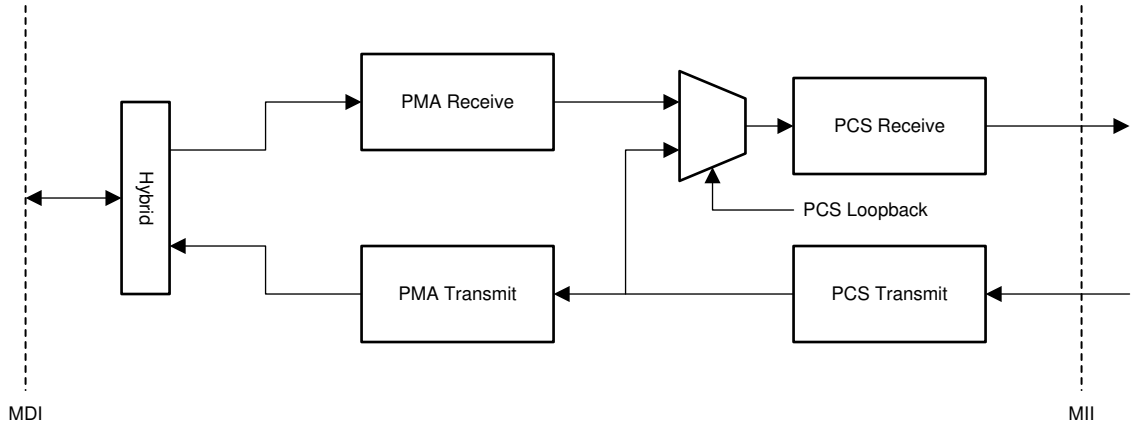


図 7-6. PCS Loopback

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7.3.3.6.3 Analog Loopback

Analog Loopback uses the echoed signals from the unterminated MDI and decodes these signals in the Hybrid to return the data to the MAC.

Analog Loopback is enabled by setting bits[6:2] = 0b0010 in the BISTCR register.

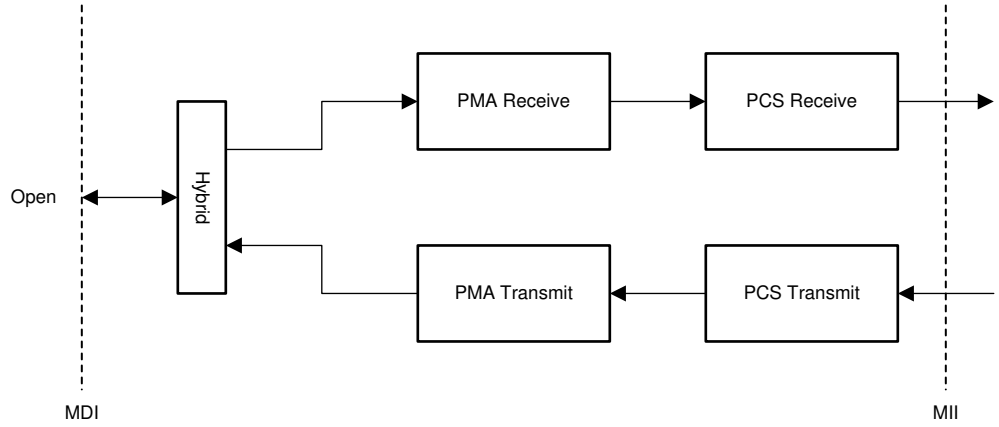


図 7-7. Analog Loopback

7.3.3.6.4 Reverse Loopback

Reverse Loopback receives data on the MDI and passes it through the entire receive block where it is then looped back within the PCS layer to the transmit block. The data is transmitted back out on the MDI to the attached Link Partner. To avoid contention, MAC transmit path is isolated.

Reverse Loopback is enable by setting bits[6:2] = 0b0100 in the BISTCR register.

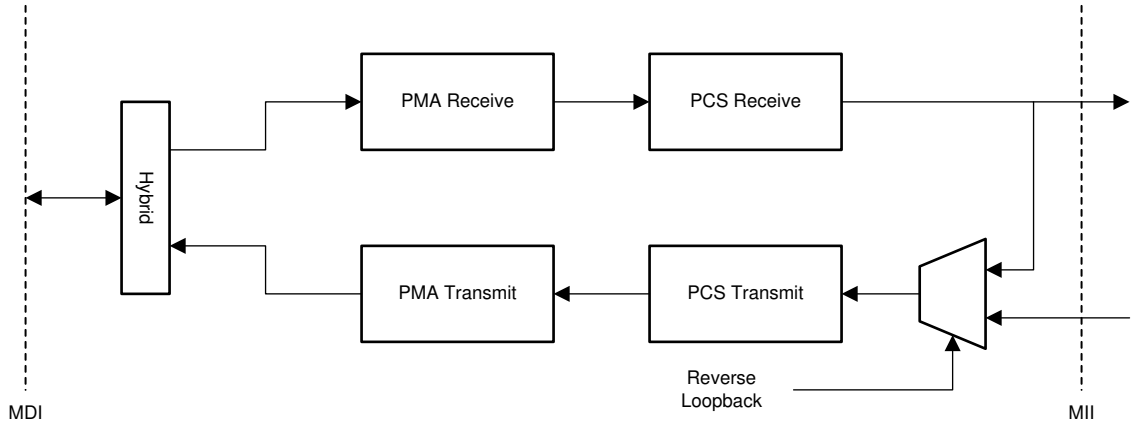


図 7-8. Reverse Loopback

7.3.4 Compliance Test Modes

There are four PMA compliance test modes required in IEEE 802.3bw, sub-clause 96.5.2, which are all supported by the DP83TC811-Q1. These compliance test modes include: transmitter waveform Power Spectral Density (PSD) mask, amplitude, distortion, 100BASE-T1 Master jitter, 100BASE-T1 Slave jitter, droop, transmitter frequency, frequency tolerance, return loss, and mode conversion. Any of the three GPIOs can be used to output TX_TCLK for the 100BASE-T1 Slave jitter measurement.

7.3.4.1 Test Mode 1

Test mode 1 evaluates transmitter droop. In test mode 1, the DP83TC811-Q1 transmits '+1' symbols for a minimum of 600ns followed by '–1' symbols for a minimum of 600ns. This pattern is repeated continuously until the test mode is disabled.

Test mode 1 is enabled by setting bits[15:13] = 0b001 in the *セクション 7.6.108*.

Additionally, transmit symbol width can be controlled using bits[9:4] in the *セクション 7.6.55*.

7.3.4.2 Test Mode 2

Test mode 2 evaluates the transmitter 100BASE-T1 Master mode jitter. In test mode 2, the DP83TC811-Q1 transmits a {+1,-1} data symbol sequence. The transmitter synchronizes the transmitted symbols from the local reference clock.

Test mode 2 is enabled by setting bits[15:13] = 0b010 in TEST_CTRL register.

7.3.4.3 Test Mode 4

Test mode 4 evaluates the transmitter distortion. In test mode 4, the DP83TC811-Q1 transmits the sequence of symbols generated by 式 1:

$$g(x) = 1 + x^9 + x^{11} \quad (1)$$

The bit sequences, x0n and x1n, are generated from combinations of the scrambler in accordance to and :

$$'x0_n = Scr_n[0] \quad (2)$$

$$x1_n = Scr_n[1] \text{ ^ } Scr_n[4] \quad (3)$$

Example streams of the 3-bit nibbles are shown in 表 7-2.

表 7-2. Transmitter Test Mode 4 Symbol Mapping

x1n	x0n	PAM3 SYMBOL
0	0	0
0	1	+1
1	0	0
1	1	–1

Test mode 4 is enabled by setting bits[15:13] = 0b100 in TEST_CTRL register.

7.3.4.4 Test Mode 5

Test mode 5 evaluates the transmitter PSD mask. In test mode 5, the DP83TC811-Q1 transmits a pseudo-random sequence of PAM3 symbols.

Test mode 5 is enabled by setting bits[15:13] = 0b101 in TEST_CTRL register.

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7.4 Device Functional Modes

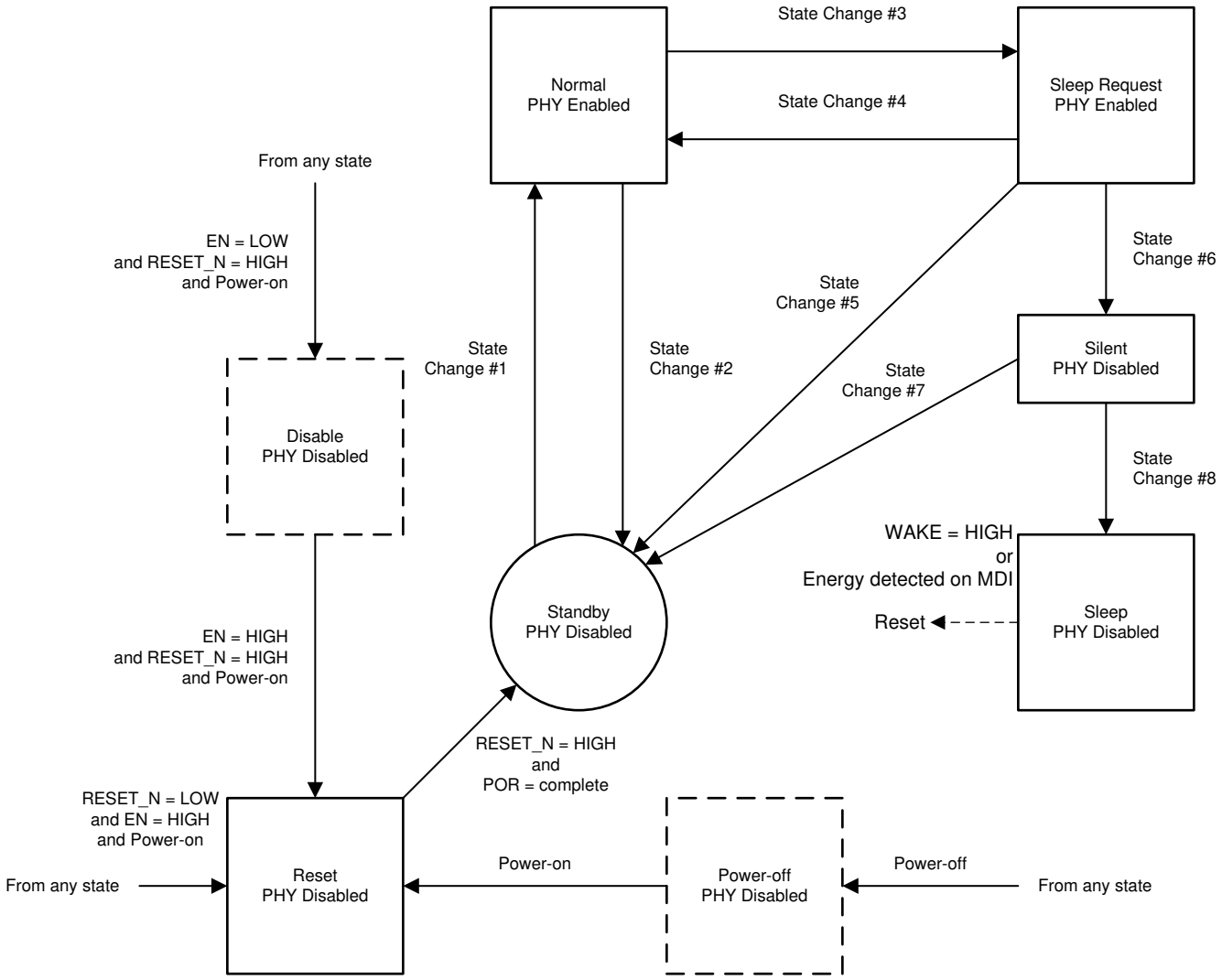


図 7-9. PHY Operation State Diagram

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7.4.1 Power Down

When VDDA is below the POR threshold (1V), the DP83TC811-Q1 is in a power-down state. All digital IOs will remain in high impedance states and analog blocks are disabled. PMA termination is not present when powered down.

7.4.2 Reset

Reset is activated upon power-up, when $\overline{\text{RESET}}$ is pulled LOW (for the minimum reset pulse time) or if hardware reset is initiated by setting bit[15] in the セクション 7.6.20. All digital circuitry is cleared along with register settings during reset. Once reset completes, device bootstraps are re-sampled and associated bootstrap registers are set accordingly. PMA termination is not present in reset.

7.4.3 Disable

To disable the PHY, EN pin must be held LOW. When disabled, the PHY behaves the same as it does in power-down. PMA termination is not present when the PHY is disabled.

7.4.4 Standby

The device (100BASE-T1 Master mode only) automatically enters into standby post power-up and reset so long that EN is held HIGH and the device is bootstrapped for managed operation.

In standby, all PHY functions are operational except for PCS and PMA blocks. Link establishment is not possible in standby and data cannot be transmitted or received. SMI functions are operational and register configurations are maintained.

If the device is configured for autonomous operation through bootstrap setting, the PHY automatically switches to normal operation once POR is complete.

7.4.5 Normal

Normal mode can be entered from either autonomous or managed operation. When in autonomous operation, the PHY will automatically try to establish a link with a valid Link Partner once POR is complete.

In managed operation, SMI access is required to allow the device to exit standby (100BASE-T1 Master mode only); commands issued through the SMI allow the device to exit standby and enables both the PCS and PMA blocks. All device features are operational in normal mode.

Autonomous operation can be enabled through SMI access by setting bit[6] in the セクション 7.6.26.

7.4.6 Sleep Request

Sleep request is entered when switching from normal mode to sleep mode. This is an intermediate state and is used to for a smooth transition into sleep mode. In sleep request mode, the PHY transmits LPS code-groups, informing the Link Partner that sleep is requested.

PHY sleep_rqst_timer (default = 1ms) begins once the PHY enters into sleep request mode. LPS decoding at the Link Partner will trigger the LPS RECEIVED interrupt. Once sleep_rqst_timer expires, the device transitions to silent mode prior to entering sleep mode. During sleep request, any frame received on the MDI or xMII enables the DP83TC811-Q1; the PHY exits sleep request and enters normal mode.

7.4.7 Silent

The DP83TC811-Q1 enters silent mode once the sleep_rqst_timer expires or the PHY no longer detects activity on the MDI, indicating that the Link Partner has already moved to silent mode.

Silent mode is only an intermediate state prior to sleep. The PHY sets tx_mode = SEND_Z and (0,0) are transmitted on the MDI. If sleep enable, bit[1] in the セクション 7.6.26, is set and no energy is detected on the MDI for the duration of silent_timer (default = 8ms), the DP83TC811-Q1 will enter sleep mode. However, if energy is detected on the MDI prior to silent_timer expiration, the PHY enters standby mode.

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7.4.8 Sleep

If sleep enable is set, the PHY transitions to sleep mode after silent_timer expires; however, if sleep enable is not set, the device transitions to standby once silent_timer expires. By default, sleep enable is set. Once in sleep mode, all PHY blocks are disabled except for energy detection on the MDI. All register configurations are lost in sleep mode. No link can be established, data cannot be transmitted or received and SMI access is not available when in sleep mode.

7.4.9 Low-Power Sleep

Low-Power Sleep code-groups are used to inform the Link Partner that sleep mode is requested. The DP83TC811-Q1 uses the *Sdn[1]* scrambler stream for LPS.

Sdn[1] scrambler stream must be set prior to LPS use, found in *セクション 7.6.102*.

7.4.10 Wake-Up

The user can wake up the DP83TC811-Q1 remotely through energy detection on the MDI or locally using the WAKE pin. For local wake, the WAKE pin must be pulled HIGH. If the WAKE pin is tied LOW, the PHY will only exit sleep if energy is detected on the MDI.

7.4.11 State Transitions

7.4.11.1 State Transition #1 - Standby to Normal

Autonomous Operation: The PHY will automatically transition to Normal state upon POR completion.

Managed Operation: The PHY will transition to Normal state out of Standby if any of the following occurs:

7.4.11.2

1. Energy detection, when energy is detected on the MDI
2. Register access, enabling Autonomous operation by setting bit[6] in the *セクション 7.6.26*
3. Register access, forcing Normal state by setting bit[0] in the *セクション 7.6.27*

7.4.11.3 State Transition #2 - Normal to Standby

This state transition is not supported.

7.4.11.4 State Transition #3 - Normal to Sleep Request

Sleep Request state can be entered when valid LPS code-groups are received on the MDI from a Link Partner.

注

The PHY will not be permitted to transmit LPS code-groups unless the registers below are set.

To enable LPS code-group transmission, the LPS transmission enable bit[0] must be set in *セクション 7.6.26*.

The *Sdn[1]* scrambler stream must be enabled by setting bits[9:8] = 0b11 in *セクション 7.6.102*.

LPS code-group identification within the PCS layer must be enabled by setting bit[0] in *セクション 7.6.51*.

LPS code-groups are sent once Sleep Request is enabled by setting bit[1] in *セクション 7.6.27*.

7.4.11.5 State Transition #4 - Sleep Request to Normal

Sleep Request can be terminated and the device re-enter Normal state by any of the following methods:

1. Register access, forcing Normal state by setting bit[0] in the *セクション 7.6.27*
2. Frame detection, when a valid frame is transmitted or received before sleep_rqst_timer expires

7.4.11.6 State Transition #5 - Sleep Request to Standby

This state transition is not supported.

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7.4.11.7 State Transition #6 - Sleep Request to Silent

Silent state can be entered by any of the following methods:

1. Valid LPS code-groups are received on the MDI *and* sleep_rqst_timer expired
2. Quiet MDI, SEND_Z [ternary symbol vectors of (0,0)] detected on the MDI

WAKE pin must be LOW for the PHY to enter Silent state.

7.4.11.8 State Transition #7 - Silent to Standby

Standby state can be entered by any of the following methods:

1. Standby enable, sleep is disabled by setting bit[1] = 0b0 in the *セクション 7.6.26 and* silent_timer expired
2. MDI Detection, Non-SEND_Z code-groups detected on the MDI prior to silent_timer expiration

7.4.11.9 State Transition #8 - Silent to Sleep

The PHY will exit Silent state and enter into Sleep state once the silent_timer expires or no activity is detected on the transmitter or receiver.

7.4.12 Media Dependent Interface

7.4.12.1 100BASE-T1 Master and 100BASE-T1 Slave Configuration

100BASE-T1 Master and 100BASE-T1 Slave are configured using either hardware bootstraps or through register access.

LED_0 controls the 100BASE-T1 Master and 100BASE-T1 Slave bootstrap configuration. By default, 100BASE-T1 Slave mode is configured because there is an internal pulldown resistor on LED_0 pin. If 100BASE-T1 Master mode configuration through hardware bootstrap is preferred, an external pullup resistor is required.

Additionally, bit[14] in the *セクション 7.6.107* controls the 100BASE-T1 Master and 100BASE-T1 Slave configuration. When this bit is set, 100BASE-T1 Master mode is enabled.

7.4.12.2 Auto-Polarity Detection and Correction

During the link training process, the DP83TC811-Q1 100BASE-T1 Slave device is able to detect polarity reversal and automatically corrects the error. If polarity reversal is detected, the 100BASE-T1 Slave will invert its own transmitted signals to account for the error and ensure compatibility with the 100BASE-T1 Master. Polarity at the 100BASE-T1 Master is always observed as correct because polarity detection and correction is handled entirely by the 100BASE-T1 Slave.

Auto-polarity correction may be disabled in cases where it is not required. Disabling of auto-polarity correction is achieved by setting bit[12] in the *セクション 7.6.43* to 1.

7.4.12.3 Jabber Detection

The jabber function prevents the PCS Receive state machine from locking up into a DATA state if the End-of-Stream Delimiters, ESD1 and ESD2, are never detected or received within the rcv_max_timer. When the maximum receive DATA state timer expires, the PCS Receive state machine is reset and transitions into IDLE state. IEEE 802.3bw specifies that jabber timeout be set to 1.08ms ± 54µs. By default, jabber timeout in the DP83TC811-Q1 is set to 1.1ms. This timer is configurable in *セクション 7.6.54*.

7.4.12.4 Interleave Detection

The interleave function allows for the DP83TC811-Q1 to detect and de-interleave the serial stream from a connected link partner. The two possible interleave sequences of ternary symbols include: (TA_n, TB_n) or (TB_n, TA_n).

7.4.13 MAC Interfaces

7.4.13.1 Media Independent Interface

The Media Independent Interface (MII) is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC. The MII is fully compliant with IEEE 802.3-2015 clause 22.

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The MII signals are summarized in 表 7-3:

表 7-3. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_EN, TX_ER
	RX_DV, RX_ER
Clock Signals	TX_CLK
	RX_CLK

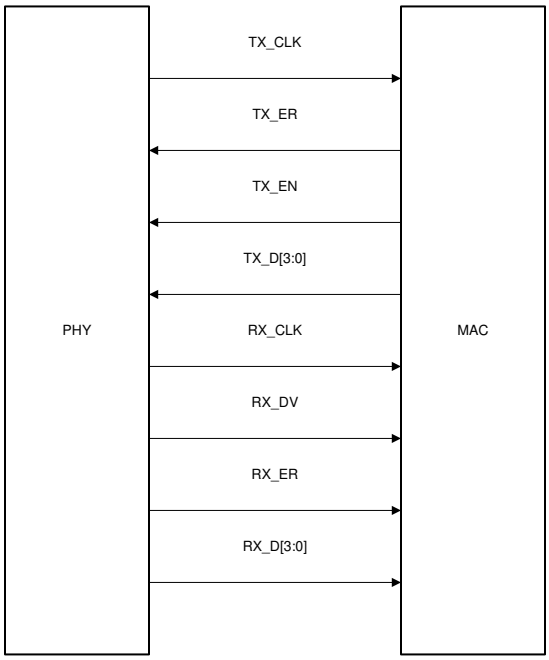


図 7-10. MII Signaling

表 7-4. MII Transmit Encoding

TX_EN	TX_ER	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission
1	1	0000 through 1111	Transmit Error Propagation

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表 7-5. MII Receive Encoding

RX_DV	RX_ER	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000	Normal Inter-Frame
0	1	0001 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

7.4.13.2 Reduced Media Independent Interface

The DP83TC811-Q1 incorporates the Reduced Media Independent Interface (RMII) as defined in the RMII Revision 1.2 and 1.0 from the RMII consortium. The purpose of this interface is to provide a reduced pin count alternative to the IEEE 802.3u MII as specified in Clause 22. Architecturally, the RMII specification provides an additional reconciliation layer on either side of the MII, but can be implemented in the absence of an MII.

The DP83TC811-Q1 offers two types of RMII operations: RMII Slave and RMII Master. In RMII Slave Mode, the DP83TC811-Q1 operates off a 50MHz CMOS-level oscillator, which is either provided by the MAC or synchronous to the MAC's reference clock. In RMII Master operation, the DP83TC811-Q1 operates off of either a 25MHz CMOS-level oscillator connected to XI pin or a 25MHz crystal connected across XI and XO pins. When bootstrapping to RMII Master Mode, a 50MHz output clock will automatically be enabled on RX_D3. This 50MHz output clock should be routed to the MAC.

The RMII specification has the following characteristics:

- Single clock reference shared between MAC and PHY
- Provides independent 2-bit wide transmit and receive data paths

In this mode, data transfers are two bits for every clock cycle using the 50MHz reference clock for both transmit and receive paths.

The RMII signals are summarized in 表 7-6:

表 7-6. RMII Signals

FUNCTION	PINS
Data Signals	TX_D[1:0]
	RX_D[1:0]
Control Signals	TX_EN
	CRS_DV

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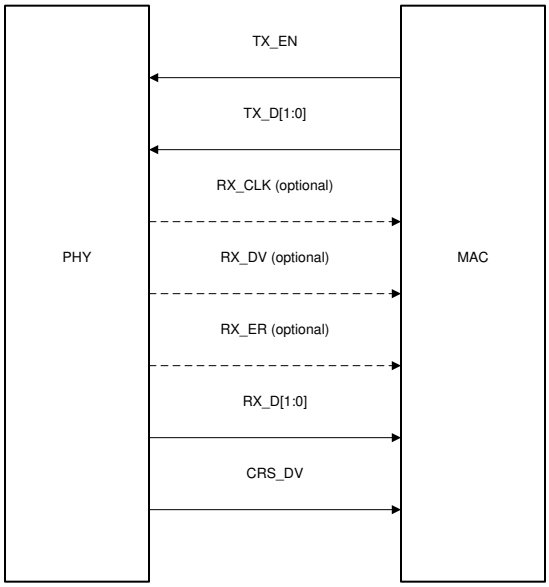


図 7-11. RMII Signaling

表 7-7. RMII Transmit Encoding

TX_EN	TX_D[1:0]	DESCRIPTION
0	00 through 11	Normal Inter-Frame
1	00 through 11	Normal Data Transmission

表 7-8. RMII Receive Encoding

CRS_DV	RX_ER	RX_D[1:0]	DESCRIPTION
0	0	00 through 11	Normal Inter-Frame
0	1	00	Normal Inter-Frame
0	1	01 through 11	Reserved
1	0	00 through 11	Normal Data Reception
1	1	00 through 11	Data Reception with Errors

RMII Slave: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the XI pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the XI pin.

RMII Master: Data on TX_D[1:0] are latched at the PHY with reference to the rising edge of the reference clock at the RX_D3 pin. Data is presented on RX_D[1:0] with reference to the same rising clock edges at the RX_D3 pin.

The DP83TC811-Q1 RMII supplies an RX_DV signal, which provides a simpler method to recover receive data without the need to separate RX_DV from the CRS_DV indication. RX_ER is also supported even though it is not required by the RMII specification.

RMII includes a programmable FIFO to adjust for the frequency differences between the reference clock and the recovered clock. The programmable FIFO, located in the *セクション 7.6.15* , minimizes internal propagation delay based on expected maximum packet size and clock accuracy.

表 7-9 indicates how to program the FIFO based on the expected maximum packet size and clock accuracy. This table is based on the assumption that the local reference clock and link partner reference clock have the same accuracy.

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表 7-9. Recommended RMII Packet Sizes

START THRESHOLD	RECOMMENDED PACKET SIZE AT ±100ppm
2-bits	1250 bytes
3-bits	3750 bytes
4-bits	6250 bytes
5-bits	8750 bytes

7.4.13.3 Reduced Gigabit Media Independent Interface

The DP83TC811-Q1 also supports Reduced Gigabit Media Independent Interface (RGMII) as specified by RGMII version 2.0 with LVCMOS. RGMII is designed to reduce the number of pins required to connect MAC and PHY. To accomplish this goal, the control signals are multiplexed. Both rising and falling edges of the clock are used to sample the control signal pin on transmit and receive paths. Data is samples on just the rising edge of the clock. For 100Mbps operation, RX_CLK and TX_CLK operate at 25MHz.

The RGMII signals are summarized in 表 7-10:

表 7-10. RGMII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Control Signals	TX_CTRL
	RX_CTRL
Clock Signals	TX_CLK
	RX_CLK

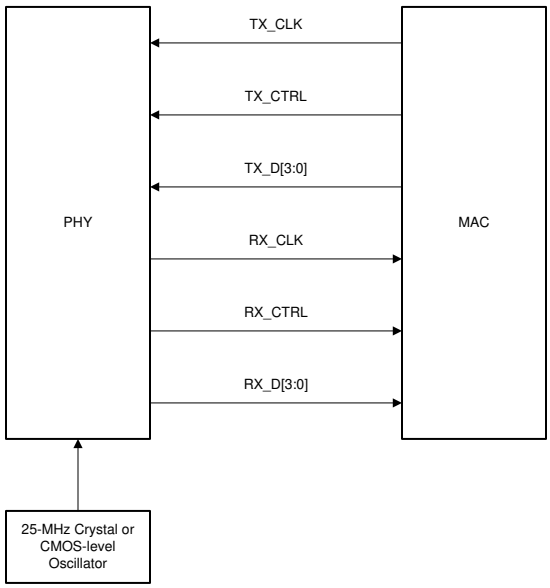


図 7-12. RGMII Connections

表 7-11. RGMII Transmit Encoding

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1111	Reserved
1	0	0000 through 1111	Normal Data Transmission

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表 7-11. RGMII Transmit Encoding (続き)

TX_CTRL (POSITIVE EDGE)	TX_CTRL (NEGATIVE EDGE)	TX_D[3:0]	DESCRIPTION
1	1	0000 through 1111	Transmit Error Propagation

表 7-12. RGMII Receive Encoding

RX_CTRL (POSITIVE EDGE)	RX_CTRL (NEGATIVE EDGE)	RX_D[3:0]	DESCRIPTION
0	0	0000 through 1111	Normal Inter-Frame
0	1	0000 through 1101	Reserved
0	1	1110	False Carrier Indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal Data Reception
1	1	0000 through 1111	Data Reception with Errors

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the internal free running clock to a recovered clock (data synchronous). Data may be duplicated on the falling edge of the clock because double data rate (DDR) is only required for 1-Gbps operation, which is not supported by the DP83TC811-Q1.

The DP83TC811-Q1 supports in-band status indication to help simplify link status detection. Inter-frame signals on RX_D[3:0] pins as specified in 表 7-13.

表 7-13. RGMII In-Band Status

RX_CTRL	RX_D3	RX_D[2:1]	RX_D0
00 **Note:** In-band status is only valid when RX_CTRL is low	**Duplex Status:** 0 = Half-Duplex 1 = Full-Duplex	**RX_CLK Clock Speed:** 00 = 2.5MHz 01 = 25MHz 10 = 125MHz 11 = Reserved	**Link Status:** 0 = Link not established 1 = Valid link established

7.4.13.4 Serial Gigabit Media Independent Interface

The Serial Gigabit Media Independent Interface (SGMII) provides a means for data transfer between MAC and PHY with significantly less signal pins (4 pins or 6 pins) compared to MII (14 pins), RMII (7 pins) or RGMII (12 pins). SGMII uses low-voltage differential signaling (LVDS) to reduce emissions and improve signal quality.

The DP83TC811SWRHA-Q1 SGMII is capable of operating in either 4-wire or 6-wire mode. Only 4-wire SGMII is configurable through hardware bootstraps. To enable 6-wire SGMII, bit[14] in the セクション 7.6.32 must be set. In 4-wire operation, two differential pairs are used to transmit and receive data. Clock and data recovery are performed in the MAC and in the PHY. If the MAC is not capable of recovering the clock from the receive data stream, 6-wire operation can be enabled to output a differential clock that is synchronous with receive data.

Because the DP83TC811SWRHA-Q1 operates at 100Mbps, the 1.25-Gbps rate of the SGMII is excessive. The SGMII specification allows for 100Mbps operation by replicating each byte within a frame 10 times. Frame elongation takes place above the IEEE 802.3 PCS layer, which prevents the start-of-frame delimiter from appearing more than once.

Because the DP83TC811SWRHA-Q1 only supports 100Mbps speed, SGMII Auto-Negotitation can be disabled by setting bit[13] = 0b0 in the セクション 7.6.6.

The SGMII signals are summarized in 表 7-14.

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表 7-14. SGMII Signals

FUNCTION	PINS
Data Signals	TX_M, TX_P
	RX_M, RX_P
Clock Signal (6-Wire)	RXCLK_M, RXCLK_P

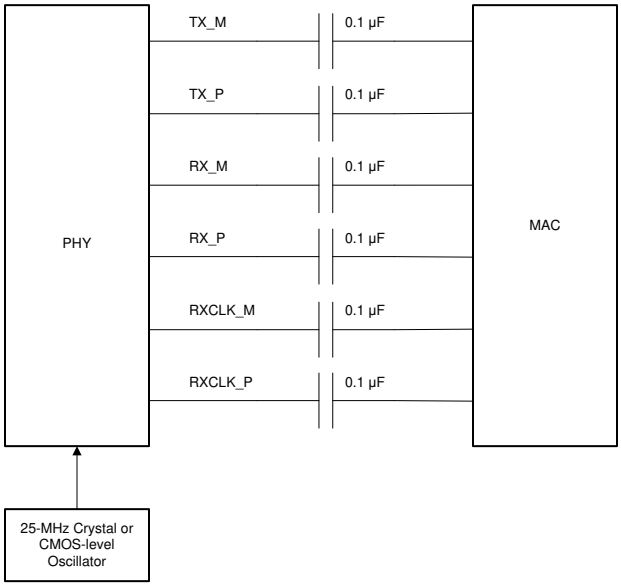


図 7-13. SGMII Connections

7.4.14 Serial Management Interface

The Serial Management Interface (SMI) provides access to the DP83TC811-Q1 internal register space for status information and configuration. The SMI frames and base registers are compatible with IEEE 802.3 clause 22. The implemented register set consists of the registers required by the IEEE 802.3 plus several others to provide additional visibility and controllability of the DP83TC811-Q1. Additionally, the DP83TC811-Q1 includes control and status registers added to clause 45 as defined by IEEE 802.3bw. Access to clause 45 register field is achieved using clause 22 access.

The SMI includes the management clock (MDC) and the management input and output data pin (MDIO). MDC is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC. MDIO pin requires a pullup resistor (2.2 KΩ), which pulls MDIO high during IDLE and turnaround.

Up to 16 DP83TC811-Q1 PHYs can share a common SMI bus. To distinguish between the PHYs, a 4-bit address is used. During power-up-reset, the DP83TC811-Q1 latches the PHYAD[3:0] configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up-reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read

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transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83TC811-Q1 drives the MDIO with a zero for the second bit of turnaround and follows this with the required data.

For write transactions, the station-management entity writes data to the addressed DP83TC811-Q1, thus eliminating the requirement for MDIO Turnaround. The turnaround time is filled by the management entity by inserting <10>.

表 7-15. SMI Protocol Structure

SMI PROTOCOL	<idle> <start> <op code> <device address> <reg address> <turnaround> <data> <idle>
Read Operation	<idle><01><10><AAAAA><RRRRR><Z0><XXXX XXXX XXXX XXXX><idle>
Write Operation	<idle><01><01><AAAAA><RRRRR><10><XXXX XXXX XXXX XXXX><idle>

7.4.15 Direct Register Access

Direct register access can be used for the first 31 registers (0x0 through 0x1F).

7.4.16 Extended Register Space Access

The DP83TC811-Q1 SMI function supports read and write access to the extended register set using registers REGCR (0xD) and ADDAR (0xE) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for Clause 22 for accessing the Clause 45 extended register set.

REGCR (0xD) is the MDIO Manageable MMD access control. In general, register REGCR[4:0] is the device address DEVAD that directs any accesses of ADDAR (0xE) register to the appropriate MMD.

The DP83TC811-Q1 supports two MMD device addresses:

1. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.
2. DEVAD[4:0] = 00001 is used for 100BASE-T1 PMA MMD register accesses. Register names for registers accessible at this device address are preceded by MMD1.

All accesses through register REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVADs are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:14] is (00), then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to (00), accesses to register ADDAR modify the extended register set address register. This address register must always be initialized in order to access any of the registers within the extended register set.
- When REGCR[15:14] is set to (01), accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to (10), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to (11), access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write access only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR.

7.4.17 Write Address Operation

To set the address register:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.

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2. Write the register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

7.4.17.1 MMD1 - Write Address Operation

For writing register addresses within MMD1 field:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the register address to register ADDAR.

7.4.18 Read Address Operation

To read the address register:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Read the register address from register ADDAR.

Subsequent reads to register ADDAR (step 2) continue to read the address register.

7.4.18.1 MMD1 - Read Address Operation

For reading register addresses within MMD1 field:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Read the register address from register ADDAR.

7.4.19 Write Operation (No Post Increment)

To write a register in the extended register set:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

7.4.19.1 MMD1 - Write Operation (No Post Increment)

To write a register in the MMD1 extended register set:
1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.20 Read Operation (No Post Increment)

To read a register in the extended register set:
1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) continue to reading the register selected by the value in the address register.

注

Steps (1) and (2) can be skipped if the address register was previously configured.

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7.4.20.1 MMD1 - Read Operation (No Post Increment)

To read a register in the MMD1 extended register set:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x4001 (data, no post increment function field = 01, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

7.4.21 Write Operation (Post Increment)

To write a register in the extended register set with post increment:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') or the value 0xC01F (data, post increment on writes function field = 11, DEVAD = '11111') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.21.1 MMD1 - Write Operation (Post Increment)

To write a register in the MMD1 extended register set with post increment:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') or the value 0xC001 (data, post increment on writes function field = 11, DEVAD = '00001') to register REGCR.
4. Write the content of the desired extended register set to register ADDAR.

7.4.22 Read Operation (Post Increment)

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1F (address function field = 00, DEVAD = '11111') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment function field = 10, DEVAD = '11111') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register; the address register is incremented after each access.

7.4.22.1 MMD1 - Read Operation (Post Increment)

To read a register in the MMD1 extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x1 (address function field = 00, DEVAD = '00001') to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x8001 (data, post increment function field = 10, DEVAD = '00001') to register REGCR.
4. Read the content of the desired extended register set in register ADDAR.

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7.5 Programming

7.5.1 Strap Configuration

The DP83TC811-Q1 uses functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up and hardware reset (through either the $\overline{\text{RESET}}$ pin or register access). The strap pins support 4 levels, which are described in greater detail below. Configuration of the device may be done through 4-level strapping or through serial management interface.

注

Because strap pins are functional pins after reset is deasserted, they should not be connected directly to VDDIO or GND. Either pullup resistors, pulldown resistors, or both are required for proper operation.

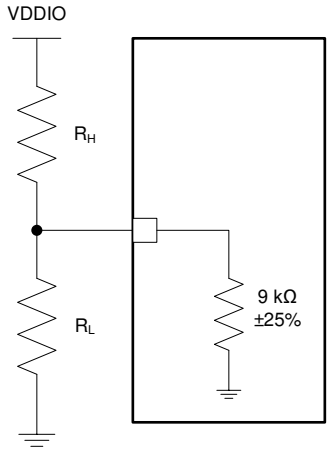


図 7-14. Strap Circuit

表 7-16. Recommended 4-Level Strap Resistor Ratios(1) (2)

MODE	IDEAL RH (kΩ)	IDEAL RL (kΩ)
1	OPEN	OPEN
2	10	2.49
3	5.76	2.49
4	2.49	OPEN

(1) Strap resistors with 1% tolerance are recommended.
(2) Resistor ratios are only a recommendation. Use the bootstrap threshold values contained within the セクション 6.5 table for more precise mode selections.

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The following table describes the DP83TC811-Q1 configuration bootstraps:

表 7-17. 4-Level Bootstraps

PIN NAME	PIN NO.	DEFAULT MODE	STRAP FUNCTION			DESCRIPTION
RX_DV	15	1	**MODE**	**PHY_AD[0]**	**PHY_AD[2]**	PHY_AD: PHY Address ID
			1	0	0	
			2	0	1	
			3	1	1	
			4	1	0	
RX_ER	14	1	**MODE**	**PHY_AD[1]**	**PHY_AD[3]**	PHY_AD: PHY Address ID
			1	0	0	
			2	0	1	
			3	1	1	
			4	1	0	
RX_D0	26	1	**MODE**	**MAC[0]**	**TEST[0]**	MAC: MAC Interface Selection TEST: Test Mode Selection
			1	0	0	
			2	0	1	
			3	1	1	
			4	1	0	
RX_D1	25	1	**MODE**	**MAC[1]**	**TEST[1]**	MAC: MAC Interface Selection TEST: Test Mode Selection
			1	0	0	
			2	0	1	
			3	1	1	
			4	1	0	
RX_D2	24	1	**MODE**	**MAC[2]**	**TEST[2]**	MAC: MAC Interface Selection TEST: Test Mode Selection
			1	0	0	
			2	0	1	
			3	1	1	
			4	1	0	
RX_D3	23	1	**MODE**	**RESERVED**	**RESERVED**	**RX_D3 must be strapped to MODE 1**
			1	0	0	
			Reserved			
			Reserved			
			Reserved			
LED_0	35	1	**MODE**	**MS**	**RESERVED**	MS: 100BASE-T1 Master & 100BASE-T1 Slave Selection **Note:** LED_0 must only be set for bootstrap MODE 1 or MODE 4.
			1	0		
			Reserved			
			Reserved			
			4	1		
LED_1	6	1	**MODE**	**$\overline{\text{AUTO}}$**	**RESERVED**	$\overline{\text{AUTO}}$: Autonomous Disable **Note 1:** LED_1 must only be set for bootstrap MODE 1 or MODE 4. **Note 2:** Autonomous bootstrap is only active for 100BASE-T1 Master mode PHYs. This bootstrap is ignored when the PHY is bootstrapped for 100BASE-T1 Slave mode operation.
			1	0		
			Reserved			
			Reserved			
			4	1		

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表 7-18. 100BASE-T1 Master and 100BASE-T1 Slave Selection Bootstrap

MS	DESCRIPTION
0	100BASE-T1 Slave Configuration
1	100BASE-T1 Master Configuration

表 7-19. MAC Interface Selection Bootstraps

MAC[2]	MAC[1]	MAC[0]	DESCRIPTION
0	0	0	SGMII (4-wire)
0	0	1	MII
0	1	0	RMII Slave
0	1	1	RMII Master
1	0	0	RGMII (Align Mode)
1	0	1	RGMII (TX Internal Delay Mode)
1	1	0	RGMII (TX and RX Internal Delay Mode)
1	1	1	RGMII (RX Internal Delay Mode)

表 7-20. Test Mode Bootstraps

TEST[2]	TEST[1]	TEST[0]	Description
0	0	0	Normal Operation
0	0	1	Test Mode 1
0	1	0	Test Mode 2
0	1	1	RESERVED
1	0	0	Test Mode 4
1	0	1	Test Mode 5
1	1	0	RESERVED
1	1	1	RESERVED

表 7-21. PHY Address Bootstraps

PHY_AD[3]	PHY_AD[2]	PHY_AD[1]	PHY_AD[0]	DESCRIPTION
0	0	0	0	PHY Address: 0b00000 (0)
0	0	0	1	PHY Address: 0b00001 (1)
0	0	1	0	PHY Address: 0b00010 (2)
0	0	1	1	PHY Address: 0b00011 (3)
0	1	0	0	PHY Address: 0b00100 (4)
0	1	0	1	PHY Address: 0b00101 (5)
0	1	1	0	PHY Address: 0b00110 (6)
0	1	1	1	PHY Address: 0b00111 (7)
1	0	0	0	PHY Address: 0b01000 (8)
1	0	0	1	PHY Address: 0b01001 (9)
1	0	1	0	PHY Address: 0b01010 (10)
1	0	1	1	PHY Address: 0b01011 (11)
1	1	0	0	PHY Address: 0b01100 (12)
1	1	0	1	PHY Address: 0b01101 (13)
1	1	1	0	PHY Address: 0b01110 (14)
1	1	1	1	PHY Address: 0b01111 (15)

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表 7-22. Autonomous Mode Bootstrap

AUTO	DESCRIPTION
0	Autonomous Mode, PHY able to establish link after power-up
1	Managed Mode, PHY must be allowed to establish link after power-up based on register write

7.5.2 LED Configuration

The DP83TC811-Q1 supports up to three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2 (CLKOUT). Several functions can be multiplexed onto the LEDs for different modes of operation. LED operations are selected using the *セクション 7.6.37*.

Because the LED output pins are also used as strap pins, external components required for strapping and the user must consider the LED usage to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding input upon power up or hardware reset.

図 7-15 shows the two proper ways of connecting LEDs directly to the DP83TC811-Q1.

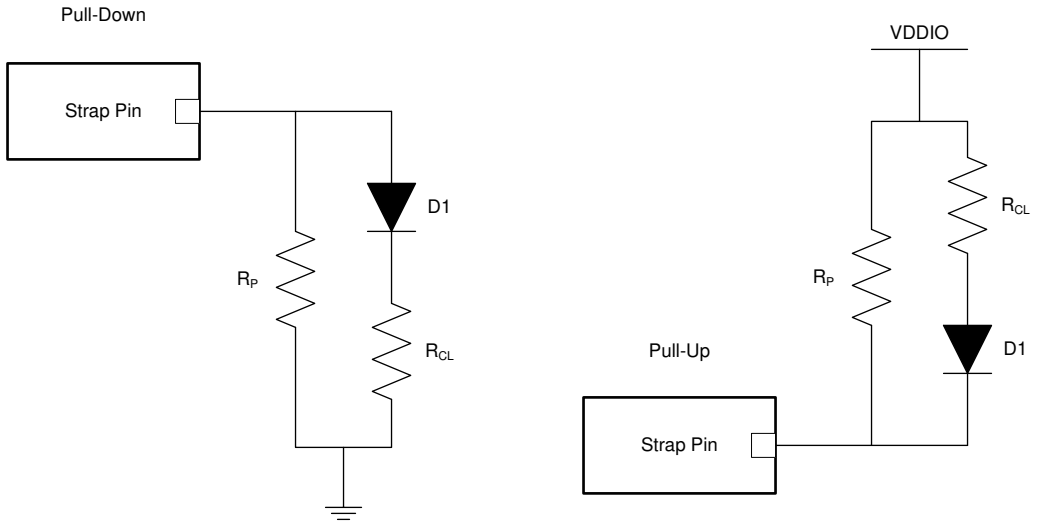


図 7-15. Example Strap Connections

7.5.3 PHY Address Configuration

The DP83TC811-Q1 can be set to respond to any of 16 possible PHY addresses through bootstrap pins. The PHY address is latched into the device upon power-up or hardware reset. Each DP83TC811-Q1 or port sharing PHY on the serial management bus in the system must have a unique PHY address. The DP83TC811-Q1 supports PHY address strapping values 0 (<0b00000>) through 15 (<0b01111>).

By default, the DP83TC811-Q1 will latch to a PHY address of 0 (<0b00000>). This address can be changed by adding pullup resistors to bootstrap pins found in 表 7-17.

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7.6 Register Maps

In the register definitions under the 'TYPE' heading, the following definitions apply:

COR	Clear on read
Strap	Default value loaded from bootstrap pin after reset
LH	Latched high and held until read
LL	Latched low and held until read
RO	Read only access
RW	Read write access
SC	Register sets on event occurrence and self-clears when event ends

7.6.1 Register Access Summary

There are two different methods for accessing registers within the field. Direct register access method is only allowed for the first 31 registers (0x0 through 0x1F). Registers beyond 0x1F must be accessed by use of the Indirect Method (Extended Register Space) described in *セクション 7.4.16*.

表 7-23. Register Access Summary

REGISTER FIELD	REGISTER ACCESS METHODS
0x0 through 0x1F	Direct Access
	Indirect Access, MMD1F = '11111' **Example:** to read register 0x17 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x17 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1F Field 0x20 - 0xFFF	Indirect Access, MMD1F = '11111' **Example:** to read register 0x462 in MMD1F field with no post increment Step 1) write 0x1F to register 0xD Step 2) write 0x462 to register 0xE Step 3) write 0x401F to register 0xD Step 4) read register 0xE
MMD1 Field 0x0 - 0xFFF	Indirect Access, MMD1 = '00001' **Example:** to read register 0x7 in MMD1 field with no post increment Step 1) write 0x1 to register 0xD Step 2) write 0x7 to register 0xE Step 3) write 0x4001 to register 0xD Step 4) read register 0xE

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7.6.2 BMCR Register 0x0000 – Basic Mode Control Register

図 7-16. Basic Mode Control Register (BMCR)

15	14	13	12	11	10	9	8
Reset	xMII Loopback	Speed Selection	Auto-Negotiation Enable	IEEE Power Down	Isolate	**Reserved**	
RW/SC-0	RW-0	RO-1	RO-0	RW-0	RW-0	RO-01	
7	6	5	4	3	2	1	0
Reserved							
RO-0							

表 7-24. BMCR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reset	RW, SC	0	**PHY Software Reset:** 1 = Initiate software Reset / Reset in Progress 0 = Normal Operation Writing a 1 to this bit resets the PHY PCS registers. When the reset operation is done, this bit is cleared to 0 automatically. PHY Vendor Specific registers will not be cleared.
14	xMII Loopback	RW	0	**xMII Loopback:** 1 = xMII Loopback enabled 0 = Normal Operation When xMII loopback mode is activated, the transmitted data presented on xMII TXD is looped back to xMII RXD internally. There is no LINK indication generated when xMII loopback is enabled.
13	Speed Selection	RO	1	**Speed Selection:** Always 100Mbps Speed
12	Auto-Negotiation Enable	RO	0	**Auto-Negotiation:** Not supported
11	IEEE Power Down	RW	0	**Power Down:** 1 = IEEE Power Down 0 = Normal Operation The PHY is powered down after this bit is set. Only register access is enabled during this power down condition. To control the power down mechanism, this bit is OR'ed with the input from the INT/PWDN_N pin. When the active low INT/PWDN_N is asserted, this bit is set.
10	Isolate	RW	0	**Isolate:** 1 = Isolates the port from the xMII with the exception of the serial management interface 0 = Normal Operation
9:0	Reserved	RO	01 0000 0000	Reserved

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7.6.3 BMSR Register 0x0001 – Basic Mode Status Register

図 7-17. Basic Mode Status Register (BMSR)

15	14	13	12	11	10	9	8
100Base-T4	100Base-TX Full-Duplex	100Base-TX Half-Duplex	10Base-T Full-Duplex	10Base-T Half-Duplex	**Reserved**		
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0		
7	6	5	4	3	2	1	0
	SMI Preamble Suppression	Auto-Negotiation Complete	Remote Fault	Auto-Negotiation Ability	Link Status	Jabber Detect	Extended Capability
	RO-1	RO-1	RO/LH-0	RO-0	RO/LL-1	RO/LH-1	RO-1

表 7-25. BMSR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	100Base-T4	RO	0	**100Base-T4 Capable:** This protocol is not available. Always reads as 0.
14	100Base-TX Full-Duplex	RO	0	**100Base-TX Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 100Base-TX 0 = Device not able to perform Full-Duplex 100Base-TX
13	100Base-TX Half-Duplex	RO	0	**100Base-TX Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 100Base-TX 0 = Device not able to perform Half-Duplex 100Base-TX
12	10Base-T Full-Duplex	RO	0	**10Base-T Full-Duplex Capable:** 1 = Device able to perform Full-Duplex 10Base-T 0 = Device not able to perform Full-Duplex 10Base-T
11	10Base-T Half-Duplex	RO	0	**10Base-T Half-Duplex Capable:** 1 = Device able to perform Half-Duplex 10Base-T 0 = Device not able to perform Half-Duplex 10Base-T
10:7	Reserved	RO	0	Reserved
6	SMI Preamble Suppression	RO	1	**Preamble Suppression Capable:** 1 = Device able to perform management transaction with preamble suppressed 0 = Device not able to perform management transaction with preambles suppressed If this bit is set to 1, 32-bits of preamble needed only once after reset, invalid opcode or invalid turnaround.
5	Auto-Negotiation Complete	RO	1	**Auto-Negotiation Complete:** 1 = Auto-Negotiation process completed 0 = Auto Negotiation process not completed (either still in process, disabled or reset)
4	Remote Fault	RO, LH	0	**Remote Fault:** 1 = Remote fault condition detected 0 = No remote fault condition detected Far End Fault indication or notification from Link Partner of Remote Fault. This bit is cleared on read or reset.
3	Auto-Negotiation Ability	RO	0	**Auto-Negotiation Ability:** 1 = Device is able to perform Auto-Negotiation 0 = Device is not able to perform Auto-Negotiation
2	Link Status	RO, LL	0	**Link Status:** 1 = Valid link established (for either 10Mbps or 100Mbps operation) 0 = Link not established
1	Jabber Detect	RO, LH	0	**Jabber Detect:** 1 = Jabber condition detected 0 = No jabber condition detected

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表 7-25. BMSR Field Descriptions (続き)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	Extended Capability	RO	1	**Extended Capability:** 1 = Extended register capabilities 0 = Basic register set capabilities only

7.6.4 PHYID1 Register 0x0002 – PHY Identifier Register #1

図 7-18. PHY Identifier Register #1 (PHYID1)

15	14	13	12	11	10	9	8
Organizationally Unique Identifier Bits 21:6							
RO-0010 0000							
7	6	5	4	3	2	1	0
Organizationally Unique Identifier Bits 21:6							
RO-0010 0000							

表 7-26. PHYID1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Organizationally Unique Identifier Bits 21:6	RO	0010 0000 0000 0000	

7.6.5 PHYID2 Register 0x0003 – PHY Identifier Register #2

図 7-19. PHY Identifier Register #2 (PHYID2)

15	14	13	12	11	10	9	8
Organizationally Unique Identifier Bits 5:0						Model Number	
RO-1010 00						RO-10 0101	
7	6	5	4	3	2	1	0
				Revision Number			
				RO-0011			

表 7-27. PHYID2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10	Organizationally Unique Identifier Bits 5:0	RO	1010 00	
9:4	Model Number	RO	10 0101	**Vendor Model Number:** The six bits of vendor model number are mapped from bits 9 to 4
3:0	Revision Number	RO	0011	**Model Revision Number:** Four bits of the vendor model revision number are mapped from bits 3 to 0. This field is incremented for all major device changes.

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7.6.6 SGMII_CFG Register 0x0009 – SGMII Configuration Register

図 7-20. SGMII Configuration Register (SGMII_CFG)

15	14	13	12	11	10	9	8
SGMII Soft Reset	SGMII Transmit Error Disable	SGMII Auto-Negotiation Enable	SGMII Enable	**Reserved**			TDR Auto-Run
RW/SC-0	RW-0	RW-1	RW/Strap	RW-0			RW-0
7	6	5	4	3	2	1	0
Reserved							
RW-0							

表 7-28. SGMII_CFG Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	SGMII Soft Reset	RW, SC	0	**SGMII Soft Reset:** 1 = Reset pulse generated 0 = normal operation
14	SGMII Transmit Error Disable	RW	0	**SGMII Transmit Error Disable:** 1 = Disable SGMII Transmit Error indiation 0 = Enable SGMII Transmit Error indication
13	SGMII Auto-Negotiation Enable	RW	1	**SGMII Auto-Negotiation:** 1 = Enable SGMII Auto-Negotiation 0 = Disable SGMII Auto-Negotiation
12	SGMII Enable	RW	Strap	**SGMII Enable:** 1 = Enable SGMII 0 = Disable SGMII
11:9	Reserved	RW	0	Reserved
8	TDR Auto-Run	RW	0	**TDR Auto-Run:** 1 = TDR will automatically run when link is lost 0 = TDR auto-run disabled
7:0	Reserved	RW	0	Reserved

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7.6.7 REGCR Register 0x000D – Register Control Register

図 7-21. Register Control Register (REGCR)

15	14	13	12	11	10	9	8
Extended Register Command		Reserved					
RW-0		RO-0					
7	6	5	4	3	2	1	0
DEVAD							
RW-0							

表 7-29. REGCR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Extended Register Command	RW	0	**Extended Register Command:** 00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13:5	Reserved	RO	0	Reserved
4:0	DEVAD	RW	0	**Device Address:** Bits[4:0] are the device address, DEVAD, that directs any accesses of *セクション 7.6.8* to the appropriate MMD. Specifically, the DP83TC811-Q1 uses the vendor specific DEVAD [4:0] = "11111" for accesses to registers 0x04D1 and lower. For MMD1 access, the DEVAD[4:0] = '00001'. All accesses through registers REGCR and ADDAR should use the DEVAD for either MMD or MMD1. Transactions with other DEVAD are ignored.

7.6.8 ADDAR Register 0x000E – Address/Data Register

図 7-22. Address/Data Register (ADDAR)

15	14	13	12	11	10	9	8
Address/Data							
RW-0							
7	6	5	4	3	2	1	0
Address/Data							
RW-0							

表 7-30. ADDAR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Address/Data	RW	0	If REGCR register 15:14 = '00', holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data.

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7.6.9 INT_TEST Register 0x0011 – Interrupt Test Register

図 7-23. Interrupt Test Register (INT_TEST)

15	14	13	12	11	10	9	8
Reserved							
RW-0000 0001 0000							
7	6	5	4	3	2	1	0
				Interrupt Polarity	Test Interrupt	**Reserved**	
				RW-1	RW-0	RW-11	

表 7-31. INT_TEST Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:4	Reserved	RW	0000 0001 0000	Reserved
3	Interrupt Polarity	RW	1	**Interrupt Polarity:** 1 = Steady state (normal operation) without an interrupt is logical 1; during interrupt, pin is logical 0 0 = Steady state (normal operation) without an interrupt is logical 0; during interrupt, pin is logical 1
2	Test Interrupt	RW	0	**Test Interrupt:** 1 = Generate an interrupt 0 = Do not generate interrupt Forces the PHY to generate an interrupt to facilitate interrupt testing. Interrupts will continue to be generated as long as this bit remains set.
1:0	Reserved	RW	11	Reserved

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7.6.10 INT_STAT1 Register 0x0012 – Interrupt Status Register #1

図 7-24. Interrupt Status Register #1 (INT_STAT1)

15	14	13	12	11	10	9	8
Link Quality Interrupt	Energy Detect Interrupt	Link Status Changed Interrupt	WoL Interrupt	ESD Event Interrupt	100BASE-T1 Master / 100BASE-T1 Slave Training Complete Interrupt	False Carrier Counter Half-Full Interrupt	Receive Error Counter Half-Full Interrupt
RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0
7	6	5	4	3	2	1	0
Link Quality Interrupt Enable	Energy Detect Interrupt Enable	Link Status Changed Enable	WoL Interrupt Enable	ESD Event Interrupt	MS Training Complete Interrupt	False Carrier HF Enable	Receive Error HF Enable
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0	RW-0

表 7-32. INT_STAT1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Link Quality Interrupt	RO, LH	0	**Change of Link Quality Status Interrupt:** 1 = Change of link quality when link is ON 0 = Link quality is Good
14	Energy Detect Interrupt	RO, LH	0	**Change of Energy Detection Status Interrupt:** 1 = Change of energy detected 0 = No change of energy detected
13	Link Status Changed Interrupt	RO, LH	0	**Change of Link Status Interrupt:** 1 = Change of link status interrupt is pending 0 = No change of link status
12	WoL Interrupt	RO, LH	0	**Detection of WoL Frame Interrupt:** 1 = WoL interrupt is pending 0 = No WoL frame detected
11	ESD Event Interrupt	RO, LH	0	**ESD Interrupt:** 1 = ESD event detected 0 = No ESD events detected
10	100BASE-T1 Master / 100BASE-T1 Slave Training Complete Interrupt	RO, LH	0	**100BASE-T1 Master and 100BASE-T1 Slave Training Complete Interrupt:** 1 = 100BASE-T1 Master and 100BASE-T1 Slave Training complete interrupt is pending 0 = MS Training is not pending
9	False Carrier Counter Half-Full Interrupt	RO, LH	0	**False Carrier Counter Half-Full Interrupt:** 1 = False Carrier counter (*セクション 7.6.12*) exceeds half-full interrupt is pending 0 = False Carrier half-full event is not pending
8	Receive Error Counter Half-Full Interrupt	RO, LH	0	**Receiver Error Counter Half-Full Interrupt:** 1 = Receive Error counter (*セクション 7.6.13*) exceeds half-full interrupt is pending 0 = Receive Error half-full event is not pending
7	Link Quality Interrupt Enable	RW	0	**Enable** interrupt on change of link quality
6	Energy Detect Interrupt Enable	RW	0	**Enable** interrupt on change of energy detection
5	Link Status Changed Enable	RW	0	**Enable** interrupt on change of link status
4	WoL Interrupt Enable	RW	0	**Enable** Interrupt on WoL frame detection
3	ESD Event Interrupt	RW	0	**Enable** Interrupt on ESD event detection
2	MS Training Complete Interrupt	RW	0	**Enable** Interrupt on 100BASE-T1 Master and 100BASE-T1 Slave Training Completion
1	False Carrier HF Enable	RW	0	**Enable** Interrupt on False Carrier Counter Register half-full event

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表 7-32. INT_STAT1 Field Descriptions (続き)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
0	Receive Error HF Enable	RW	0	**Enable** Interrupt on Receive Error Counter Register half-full event

7.6.11 INT_STAT2 Register 0x0013 – Interrupt Status Register #2

図 7-25. Interrupt Status Register #2 (INT_STAT2)

15	14	13	12	11	10	9	8
Undervoltage Interrupt	Overvoltage Interrupt	**Reserved**		Overtemperature Interrupt	Sleep Mode Interrupt	Polarity Change Interrupt	Jabber Detect Interrupt
RO/LH-0	RO/LH-0	RO/LH-0		RO/LH-0	RO/LH-0	RO/LH-0	RO/LH-0
7	6	5	4	3	2	1	0
Undervoltage Interrupt Enable	Overvoltage Interrupt Enable	**Reserved**		Overtemperature Interrupt Enable	Sleep Mode Event Enable	Polarity Change Interrupt Enable	Jabber Detect Interrupt Enable
RW-0	RW-0	RO-0		RW-0	RW-0	RW-0	RW-0

表 7-33. INT_STAT2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Undervoltage Interrupt	RO, LH	0	**Undervoltage Interrupt:** 1 = Undervoltage event interrupt pending 0 = No undervoltage event pending
14	Overvoltage Interrupt	RO, LH	0	**Overvoltage Interrupt:** 1 = Overvoltage event interrupt pending 0 = No overvoltage event pending
13:12	Reserved	RO, LH	0	Reserved
11	Overtemperature Interrupt	RO, LH	0	**Overtemperature Interrupt:** 1 = Overtemperature event interrupt pending 0 = No overtemperature event pending
10	Sleep Mode Interrupt	RO, LH	0	**Sleep Mode Interrupt:** 1 = Sleep mode event interrupt is pending 0 = No Sleep mode event pending
9	Polarity Change Interrupt	RO, LH	0	**Polarity Change Interrupt:** 1 = Data polarity change interrupt pending 0 = No Data polarity even pending
8	Jabber Detect Interrupt	RO, LH	0	**Jabber Detect Interrupt:** 1 = Jabber detect event interrupt pending 0 = No Jabber detect event pending
7	Undervoltage Interrupt Enable	RW	0	**Enable** interrupt on undervoltage event
6	Overvoltage Interrupt Enable	RW	0	**Enable** interrupt on overvoltage event
5 :4	Reserved	RO	0	Reserved
3	Overtemperature Interrupt Enable	RW	0	**Enable** interrupt on overtemperature event
2	Sleep Mode Event Enable	RW	0	**Enable** Interrupt on sleep mode event
1	Polarity Change Interrupt Enable	RW	0	**Enable** Interrupt on change of polarity status
0	Jabber Detect Interrupt Enable	RW	0	**Enable** Interrupt on Jabber detection event

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7.6.12 FCSCR Register 0x0014 – False Carrier Sense Counter Register

図 7-26. False Carrier Sense Counter Register (FCSCR)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
False Carrier Event Counter							
RO/COR-0							

表 7-34. FCSCR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Reserved	RO	0	Reserved
7:0	False Carrier Event Counter	RO, COR	0	**False Carrier Event Counter:** This 8-bit counter increments on every false carrier event. This counter stops when it reaches its maximum count (0xFF). When the counter exceeds half-full (0x7F), an interrupt event is generated. This register is cleared on read.

7.6.13 RECR Register 0x0015 – Receive Error Count Register

図 7-27. Receive Error Count Register (RECR)

15	14	13	12	11	10	9	8
Receive Error Counter							
RO/COR-0							
7	6	5	4	3	2	1	0
Receive Error Counter							
RO/COR-0							

表 7-35. RECR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Receive Error Counter	RO, COR	0	**RX_ER Counter:** When a valid carrier is presented (only while RX_DV is set), and there is at least one occurrence of an invalid data symbol, this 16-bit counter increments for each receive error detected. The RX_ER counter does not count in xMII loopback mode. The counter stops when it reaches its maximum count (0xFFFF). When the counter exceeds half-full (0x7FFF), an interrupt is generated. This register is cleared on read.

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7.6.14 BISTCR Register 0x0016 – BIST Control Register

図 7-28. BIST Control Register (BISTCR)

15	14	13	12	11	10	9	8
Reserved	BIST Error Counter Mode	PRBS Packet Type	Packet Generation Enable	PRBS Checker Lock/Sync	PRBS Checker Sync Loss	Packet Generator Status	**Reserved**
RO-0	RW-0	RW-0	RW-0	RO-0	RO/LH-0	RO-0	RO-10
7	6	5	4	3	2	1	0
	Loopback Select					**Reserved**	
	RW-0					RW-0	

表 7-36. BISTCR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14	BIST Error Counter Mode	RW	0	**BIST Error Counter Mode:** 1 = Continuous mode, when the BIST Error counter reaches its max value, a pulse is generated and the counter starts counting from zero again. 0 = Single mode, when BIST Error Counter reaches its max value, PRBS checker stops counting.
13	PRBS Packet Type	RW	0	**PRBS Packet Type:** 1 = When packet generator is enabled (Bit[12] = '1'), generate continuous packets with PRBS data. When packet generator is disabled, PRBS checker is still enabled. 0 = When packet generator is enabled, generate single packet with constant data. PRBS gen/check is disabled.
12	Packet Generation Enable	RW	0	**Packet Generation Enable:** 1 = Enable packet generator with PRBS data 0 = Disable packet generator
11	PRBS Checker Lock/Sync	RO	0	**PRBS Checker Lock/Sync Indication:** 1 = PRBS checker is locked and synced on received bit stream 0 = PRBS checker is not locked
10	PRBS Checker Sync Loss	RO, LH	0	**PRBS Checker Sync Loss Indication:** 1 = PRBS checker has lost sync 0 = PRBS checker has not lost sync
9	Packet Generator Status	RO	0	**Packet Generation Status Indication:** 1 = Packet Generator is active and generating packets 0 = Packet Generator is off
8:7	Reserved	RO	10	Reserved
6:2	Loopback Select	RW	0	**Loopback Select:** **Bits[5:2]** 0000 = Normal operation 0001 = PCS Loopback 0010 = Analog Loopback 0100 = Reverse Loopback 1000 = Reserved **Bit[6]:** 1 = Transmit data to the MDI in xMII Loopback 0 = Surpress data to the MDI in xMII Loopback **Note:** Bit[6] can only can be set in xMII Loopback
1:0	Reserved	RW	0	Reserved

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7.6.15 xMII_CTRL Register 0x0017 – xMII Control Register

図 7-29. xMII Control Register (xMII_CTRL)

15	14	13	12	11	10	9	8
Reserved	SGMII TX/RX Buffer Half-Full Threshold		RGMII RX Clock Internal Delay	RGMII TX Clock Internal Delay	**Reserved**	RGMII Mode	**Reserved**
RO-0	RW-0		RW/Strap	RW/Strap	RW-0	RW/Strap	RW-0
7	6	5	4	3	2	1	0
Clock Select	**Reserved**	RMII Mode	RMII Revision Select	RMII Overflow Status	RMII Underflow Status	RMII Receive Elasticity Buffer Size	
RW/Strap	RW-1	RW/Strap	RW-0	RO/COR-0	RO/COR-0	RW-01	

表 7-37. xMII_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14:13	SGMII TX/RX Buffer Half-Full Threshold	RW	10	**SGMII Buffer Half-Full Threshold:** 00 = 5-bit 01 = 2-bit 10 = 6-bit 11 = 10-bit
12	RGMII RX Clock Internal Delay	RW	Strap	**RGMII RX Clock Internal Delay:** 1 = Receive path internal clock delay is enabled 0 = Receive path internal clock delay is disabled **Note:** When enabled, receive path internal clock (RX_CLK) is delayed by 2ns relative to receive data. When disabled, data and clock are in align mode.
11	RGMII TX Clock Internal Delay	RW	Strap	**RGMII TX Clock Internal Delay:** 1 = Transmit path internal clock delay is enabled 0 = Transmit path internal clock delay is disabled **Note:** When enabled, transmit path internal clock (TX_CLK) is delayed by 2ns relative to transmit data. When disabled, data and clock are in align mode.
10	Reserved	RW	0	Reserved
9	RGMII Mode	RW	Strap	**RGMII Mode Enable:** 1 = Enable RGMII mode of operation 0 = Mode determined by Bit[5]
8	Reserved	RW	0	Reserved
7	Clock Select	RW	Strap	**Reference Clock Select:** Strap determines the clock reference requirement. 1 = 50MHz clock reference, CMOS-level oscillator 0 = 25MHz clock reference, crystal or CMOS-level oscillator
6	Reserved	RW	1	Reserved
5	RMII Mode	RW	Strap	**RMII Mode Enable:** 1 = Enable RMII mode of operation 0 = Enable MII mode of operation
4	RMII Revision Select	RW	0	**RMII Revision Select:** 1 = RMII Revision 1.0 0 = RMII Revision 1.2 RMII revision 1.0, CRS_DV will remain asserted until final data is transferred. CRS_DV will not toggle at the end of a packet. RMII revision 1.2, CRS_DV will toggle at the end of a packet to indicate de-assertion of CRS.
3	RMII Overflow Status	RO, COR	0	**RX FIFO Overflow Status:** 1 = Normal 0 = Overflow detected

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表 7-37. xMII_CTRL Field Descriptions (続き)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
2	RMII Underflow Status	RO, COR	0	**RX FIFO Underflow Status:** 1 = Normal 0 = Underflow detected
1:0	RMII Receive Elasticity Buffer Size	RW	01	**Receive Elasticity Buffer Size:** This field controls the Receive Elasticity Buffer which allows for frequency variation tolerance between the 50MHz RMII clock and the recovered data. The following values indicate the tolerance in bits for a single packet. The minimum setting allows for standard Ethernet frame sizes at ±100ppm accuracy. 00 = 5-bit tolerance (up to 8750 byte packets) 01 = 2-bit tolerance (up to 1250 byte packets) 10 = 3-bit tolerance (up to 3750 byte packets) 11 = 4-bit tolerance (up to 6250 byte packets)

7.6.16 INT_STAT3 Register 0x0018 – Interrupt Status Register #3

図 7-30. Interrupt Status Register #3 (INT_STAT3)

15	14	13	12	11	10	9	8
Reserved			POR Done Interrupt	No Frame Detected Interrupt	**Reserved**		LPS Interrupt
RO-0			RO/LH-0	RO/LH-0	RO/LH-0		RO/LH-0
7	6	5	4	3	2	1	0
Reserved			POR Done Interrupt Enable	No Frame Detected Interrupt Enable	**Reserved**		LPS Interrupt Enable
RO-0			RW-1	RW-0	RW-0		RW-0

表 7-38. INT_STAT3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13	Reserved	RO	0	Reserved
12	POR Done Interrupt	RO, LH	0	**POR Done Interrupt:** 1 = POR done event pending 0 = No POR done event pending
11	No Frame Detected Interrupt	RO, LH	0	**No Frame Detection Interrupt:** 1 = No Frame Detection event interrupt pending 0 = No event pending
10:9	Reserved	RO, LH	0	Reserved
8	LPS Interrupt	RO, LH	0	**LPS Interrupt:** 1 = LPS event interrupt is pending 0 = No LPS event pending
7:5	Reserved	RO	0	Reserved
4	POR Done Interrupt Enable	RW	1	**Enable** interrupt on POR Done event.
3	No Frame Detected Interrupt Enable	RW	0	**Enable** interrupt on No Frame Detection event
2:1	Reserved	RW	0	Reserved
0	LPS Interrupt Enable	RW	0	**Enable** interrupt on LPS event

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7.6.17 BICTSR1 Register 0x001B – BIST Control and Status Register #1

図 7-31. BIST Control and Status Register #1 (BICTSR1)

15	14	13	12	11	10	9	8
BIST Error Count							
RW-0							
7	6	5	4	3	2	1	0
BIST IPG Length							
RW-0111 1101							

表 7-39. BICTSR1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	BIST Error Count	RO	0	**BIST Error Count:** Holds number of errored bytes received by the PRBS checker. Value in this register is locked and cleared when write is done to Bit[15]. When BIST Error Counter Mode is set to '0', count stops on 0xFF (see register 0x16) Note: Writing '1' to Bit[15] will lock the counter's value for successive read operation and clear the BIST Error Counter.
7:0	BIST IPG Length	RW	0111 1101	**BIST IPG Length:** Inter Packet Gap (IPG) Length defines the size of the gap (in 4 byte increments) between any 2 successive packets generated by the BIST. Default value is 0x7D: 0x7D to decimal conversion = 125 125 * 4 bytes = 500 bytes (default)

7.6.18 BICTSR2 Register 0x001C – BIST Control and Status Register #2

図 7-32. BIST Control and Status Register #2 (BICTSR2)

15	14	13	12	11	10	9	8
Reserved					BIST Packet Length		
RO-0					RW-101 1110 1110		
7	6	5	4	3	2	1	0
BIST Packet Length							
RW-101 1110 1110							

表 7-40. BICTSR2 Field Description

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11	Reserved	RO	0	Reserved
10:0	BIST Packet Length	RW	101 1110 1110	**BIST Packet Length:** Length of the generated BIST packets. The value of this register defines the size (in bytes) of every packet that is generated by the BIST. Default value is 0x5EE, which is equal to 1514 bytes.

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7.6.19 TDR Register 0x001E – Time Domain Reflectometry Register

図 7-33. Time Domain Reflectometry Register (TDR)

15	14	13	12	11	10	9	8
TDR Start	**Reserved**						
RW/SC-0	RO-0						
7	6	5	4	3	2	1	0
						TDR Status	TDR Test Fail
						RO-0	RO-0

表 7-41. TDR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	TDR Start	RW, SC	0	**TDR Start:** 1 = Start cable measurement 0 = Cable Diagnostic is disabled
14:2	Reserved	RO	0	Reserved
1	TDR Status	RO	0	**TDR Done:** 1 = Indication that cable measurement process is complete 0 = Cable Diagnostic had not completed
0	TDR Test Fail	RO	0	**TDR Process Fail:** 1 = Indication that cable measurement process failed 0 = Cable Diagnostic has not failed

7.6.20 PHYRCR Register 0x001F – PHY Reset Control Register

図 7-34. PHY Reset Control Register (PHYRCR)

15	14	13	12	11	10	9	8
Hardware Reset	Software reset	**Reserved**					
RW/SC-0	RW/SC-0	RW-0					
7	6	5	4	3	2	1	0
Standby Mode	**Reserved**						
RW-0	RW-0						

表 7-42. PHYRCR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Hardware Reset	RW, SC	0	**Hardware Reset:** 1 = Reset PHY. This bit is self cleared and has the same effect as the $\overline{\text{RESET}}$ pin. 0 = Normal Operation
14	Software reset	RW, SC	0	**Software Restart:** 1 = Restart PHY. This bit is self cleared and resets all PHY circuitry except registers. 0 = Normal Operation
13:8	Reserved	RW	0	Reserved
7	Standby Mode	RW	0	**Standby Mode:** 1 = Standby mode enabled 0 = Normal operation
6:0	Reserved	RW	0	Reserved

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7.6.21 LSR Register 0x0133 – Link Status Results Register

図 7-35. Link Status Results Register (LSR)

15	14	13	12	11	10	9	8
Reserved			Link Status	**Reserved**			
RO-0			RO-0	RO-0101 1110 0			
7	6	5	4	3	2	1	0
					Scrambler Lock	Local Receiver Status	Remote Receiver Status
					RO-0	RO-0	RO-0

表 7-43. LSR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13	Reserved	RO	0	Reserved
12	Link Status	RO	0	**Unlatched Link Status:** 1 = Valid Link Established 0 = No Link
11:3	Reserved	RO	0101 1110 0	Reserved
2	Scrambler Lock	RO	0	**Scrambler Lock:** 1 = Scrambler Locked 0 = Scrambler Not Locked
1	Local Receiver Status	RO	0	**Local Receiver Status:** 1 = Local PHY received link valid 0 = Local PHY received link invalid
0	Remote Receiver Status	RO	0	**Remote Receiver Status:** 1 = Remote PHY received link valid 0 = Remote PHY received link invalid

7.6.22 TDRR Register 0x016B – TDR Results Register

図 7-36. TDR Results Register (TCRR)

15	14	13	12	11	10	9	8
Reserved						Fault Status	Fault Type
RO-0						RO-0	RO-0
7	6	5	4	3	2	1	0
Fault Location							
RO-0							

表 7-44. TDRR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10	Reserved	RO	0	Reserved
9	Fault Status	RO	0	**Fault Status:** 1 = Fault Detected 0 = No Fault Detected
8	Fault Type	RO	0	**Fault Type:** 1 = SHORT Fault 0 = OPEN Fault **Note:** Only valid when bit[9] = 1.
7:0	Fault Location	RO	0	**Fault Location:** To calculate fault location in meters, convert binary field to decimal form and multiply by 1.5. **Note:** Only valid when bit[9] = 1.

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7.6.23 TDRLR1 Register 0x0180 – TDR Location Result Register #1

図 7-37. TDR Location Result Register #1 (TDRLR1)

15	14	13	12	11	10	9	8
Location 2							
RO-0							
7	6	5	4	3	2	1	0
Location 1							
RO-0							

表 7-45. TDRLR1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Location 2	RO	0	Location of the Second peak discovered by the TDR mechanism. Distance in meters = 1.5 * (convert bit field to decimal - 4)
7:0	Location 1	RO	0	Location of the First peak discovered by the TDR mechanism. Distance in meters = 1.5 * (convert bit field to decimal - 4)

7.6.24 TDRLR2 Register 0x0181 – TDR Location Result Register #2

図 7-38. TDR Location Result Register #2

15	14	13	12	11	10	9	8
Location 4							
RO-0							
7	6	5	4	3	2	1	0
Location 3							
RO-0							

表 7-46. TDRLR2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Location 4	RO	0	Location of the Fourth peak discovered by the TDR mechanism. Distance in meters = 1.5 * (convert bit field to decimal - 4)
7:0	Location 3	RO	0	Location of the Third peak discovered by the TDR mechanism. Distance in meters = 1.5 * (convert bit field to decimal - 4)

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7.6.25 TDRPT Register 0x018A – TDR Peak Type Register

図 7-39. TDR Peak Type Register (TDRPT)

15	14	13	12	11	10	9	8
Reserved	Peak 4 Type	Peak 3 Type	Peak 2 Type	Peak 1 Type	**Reserved**		
RO-0	RO-0	RO-0	RO-0	RO-0	RO-0		
7	6	5	4	3	2	1	0
Reserved							
RO-0							

表 7-47. TDRPT Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14	Peak 4 Type	RO	0	**Peak 4 Polarity Detection:** 1 = Negative Polarity 0 = Positive Polarity Negative polarity detection can be caused by a SHORT. Positive polarity detection can be caused by an OPEN. **Note:**only valid when bits[15:8] in register 0x181 is not zero.
13	Peak 3 Type	RO	0	**Peak 3 Polarity Detection:** 1 = Negative Polarity 0 = Positive Polarity Negative polarity detection can be caused by a SHORT. Positive polarity detection can be caused by an OPEN. **Note:**only valid when bits[7:0] in register 0x181 is not zero.
12	Peak 2 Type	RO	0	**Peak 2 Polarity Detection:** 1 = Negative Polarity 0 = Positive Polarity Negative polarity detection can be caused by a SHORT. Positive polarity detection can be caused by an OPEN. **Note:**only valid when bits[15:8] in register 0x180 is not zero.
11	Peak 1 Type	RO	0	**Peak 1 Polarity Detection:** 1 = Negative Polarity 0 = Positive Polarity Negative polarity detection can be caused by a SHORT. Positive polarity detection can be caused by an OPEN. **Note:**only valid when bits[7:0] in register 0x180 is not zero.
10:0	Reserved	RO	0	Reserved

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7.6.26 AUTO_PHY Register 0x018B – Autonomous PHY Control Register

図 7-40. Autonomous PHY Control Register (AUTO_PHY)

15	14	13	12	11	10	9	8
Reserved							
RW-0							
7	6	5	4	3	2	1	0
	Autonomous Command	**Reserved**				Sleep Enable	LPS Transmission Enable
	RW/COR/Strap	RW-01 10				RW-1	RW-0

表 7-48. AUTO_PHY Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:7	Reserved	RW	0	Reserved
6	Autonomous Command	RW, COR	Strap	**Autonomous Command:** 1 = Device in Autonomous operation 0 = Device in Managed operation **Note:** This bit is a one-time event. Once written to or read, the bit will always read 0b0. Managed mode can only be entered at power-up or reset when the bootstrap is sampled.
5:2	Reserved	RW	01 10	Reserved
1	Sleep Enable	RW	1	**Sleep Enable:** 1 = Sleep enabled 0 = Standby enabled The device will transition to Sleep state after negotiating with a Link Partner if this bit is set. Otherwise, once LPS negotiation is complete, the device will transition to Standby.
0	LPS Transmission Enable	RW	0	**LPS Transmission Enable:** 1 = Device allowed to send LPS code-groups 0 = No LPS code-groups enabled Device is only allowed to send LPS code-groups when this bit is set.

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7.6.27 PWRM Register 0x018C – Power Mode Register

図 7-41. Power Mode Register (PWRM)

15	14	13	12	11	10	9	8
Reserved							
RW-0							
7	6	5	4	3	2	1	0
Reserved						Sleep Request Command	Normal Command
RW-0						RW-0	RW/SC-0

表 7-49. PWRM Register 0x018C – Power Mode Register

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:2	Reserved	RW	0	Reserved
1	Sleep Request Command	RW	0	**Sleep Request Command:** 1 = Device will transmit LPS code-groups 0 = Normal operation
0	Normal Command	RW, SC	0	**Normal Command:** 1 = Device forced to Normal state 0 = Normal operation Self-cleared only when PHY moves from Standby to Normal state. Bit is not cleared on any other transition.

7.6.28 SNR Register 0x0197 – Signal-to-Noise Ratio Result Register

図 7-42. Signal-to-Noise Ratio Result Register (SNR)

15	14	13	12	11	10	9	8
Reserved							SNR
RO-0							RO-0
7	6	5	4	3	2	1	0
SNR							
RO-0							

表 7-50. SNR Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:9	Reserved	RO	0	Reserved
8:0	SNR	RO	0	**Signal-to-Noise Ratio:**Value contained within bit field contains 10*SNR (dB). To obtain SNR (dB) convert binary value to decimal form and divide by 10. **Note:** Only valid when link is established.

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7.6.29 SQI Register 0x0198 – Signal Quality Indication Register

図 7-43. Signal Quality Indication Register (SQI)

15	14	13	12	11	10	9	8
Reserved						SQS	
RO-0						RO-0	
7	6	5	4	3	2	1	0
SQI							
RO-0							

表 7-51. SQI Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10	Reserved	RO	0	Reserved
9:8	SQS	RO	0	**Signal Quality Status:** 00 = No Link 01 = Poor Link, Intermittent Link 10 = Good Link quality 11 = Excellent Link quality
7:0	SQI	RO	0	**Signal Quality Indication:**Value contained within bit field contains SQI and directly relates to the Signal Quality Status bit field. Convert binary value to decimal to obtain SQI. SQI > 70 -- Excellent Link quality 40 < SQI < 70 -- Good Link quality SQI < 40 -- Intermittent or No Link

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7.6.30 LD_CTRL Register 0x0400 – Line Driver Control Register

図 7-44. Line Driver Control Register (LD_CTRL)

15	14	13	12	11	10	9	8
Reserved			Line Driver Series Termination				
RW-000			RW-1 0000				
7	6	5	4	3	2	1	0
Reserved							
RW-0000 0000							

表 7-52. LD_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13	Reserved	RW	000	Reserved
12:8	Line Driver Series Termination	RW	1 0000	**Line Driver Series Termination Control:** 0 0000 = 70Ω 0 0001 = 67.7Ω 0 0010 = 65.6Ω 0 0011 = 63.6Ω 0 0100 = 61.7Ω 0 0101 = 60Ω 0 0110 = 58.3Ω 0 0111 = 56.7Ω 0 1000 = 55.2Ω 0 1001 = 53.8Ω 0 1010 = 52.5Ω 0 1011 = 51.2Ω 0 1100 = 50Ω 0 1101 = 48.8Ω 0 1110 = 47.7Ω 0 1111 = 46.6Ω 1 0000 = 45.6Ω (default) 1 0001 = 44.7Ω 1 0010 = 43.7Ω 1 0011 = 42.8Ω 1 0100 = 42Ω 1 0101 = 41Ω 1 0110 = 40.4Ω 1 0111 = 39.6Ω 1 1000 = 38.9Ω 1 1001 = 38.2Ω 1 1010 = 37.5Ω 1 1011 = 36.8Ω 1 1100 = 36.2Ω 1 1101 = 35.6Ω 1 1110 = 35Ω 1 1111 = 34.4Ω
7:0	Reserved	RW	0000 0000	Reserved

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7.6.31 LDG_CTRL1 Register 0x0401 – Line Driver Gain Control Register #1

図 7-45. Line Driver Gain Control Register (LDG_CTRL1)

15	14	13	12	11	10	9	8
Reserved							
RW-0							
7	6	5	4	3	2	1	0
				Fine Gain Control - MDI			
				RW-1010			

表 7-53. LDG_CTRL1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:4	Reserved	RW	0	Reserved
3:0	Fine Gain Control - MDI	RW	1010	**Line Driver Differential Swing Control:** 0000 = - 16% change in gain 0001 = - 14% change in gain 0010 = - 12% change in gain 0011 = - 10% change in gain 0100 = - 8% change in gain 0101 = - 6% change in gain 0110 = - 4% change in gain 0111 = - 2% change in gain 1000 = No change in gain 1001 = + 2% change in gain 1010 = + 4% change in gain 1011 = + 6% change in gain 1100 = + 8% change in gain 1101 = + 10% change in gain 1110 = + 12% change in gain 1111 = + 14% change in gain

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7.6.32 SGMII_CTRL1 Register 0x0432 – SGMII Control Register #1

図 7-46. SGMII Control Register #1 (SGMII_CTRL1)

15	14	13	12	11	10	9	8
Reserved	SGMII Type Select	**Reserved**					
RO-0	RW-0	RO-0					
7	6	5	4	3	2	1	0

表 7-54. SGMII_CTRL1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14	SGMII Type Select	RW	0	**SGMII Type Select:** 1 = 6-wire SGMII (RXCLK_P and RXCLK_M enabled) 0 = 4-wire SGMII
13:0	Reserved	RW	0	Reserved

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7.6.33 DLL_CTRL 0x0446 – RGMII DLL Control Register

図 7-47. RGMII DLL Control Register (DLL_CTRL)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
DLL TX Internal Delay Control				DLL RX Internal Delay Control			
RW-0111				RW-0111			

表 7-55. DLL_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Reserved	RO	0	Reserved
7:4	DLL TX Internal Delay Control	RW	0111	**Transmit Internal Delay Control:** Controls the DLL value in 250ps steps for the transmit path. Value below is the amount of internal delay on the TX_CLK path induced. 0000 = 0.25ns 0001 = 0.50ns 0010 = 0.75ns 0011 = 1.00ns 0100 = 1.25ns 0101 = 1.50ns 0110 = 1.75ns 0111 = 2.00ns 1000 = 2.25ns 1001 = 2.50ns 1010 = 2.75ns 1011 = 3.00ns 1100 = 3.25ns 1101 = 3.50ns 1110 = 3.75ns 1111 = 4.00ns
3:0	DLL RX Internal Delay Control	RW	0111	**Receive Internal Delay Control:** Controls the DLL value in 250ps steps for the receive path. Value below is the amount of internal delay on the RX_CLK path induced. 0000 = 0.25ns 0001 = 0.50ns 0010 = 0.75ns 0011 = 1.00ns 0100 = 1.25ns 0101 = 1.50ns 0110 = 1.75ns 0111 = 2.00ns 1000 = 2.25ns 1001 = 2.50ns 1010 = 2.75ns 1011 = 3.00ns 1100 = 3.25ns 1101 = 3.50ns 1110 = 3.75ns 1111 = 4.00ns

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7.6.34 ESDS Register 0x0448 – Electrostatic Discharge Status Register

図 7-48. Electrostatic Discharge Status Register (ESDS)

15	14	13	12	11	10	9	8
Reserved		xMII ESD Event Counter					
RO-0		RO-0					
7	6	5	4	3	2	1	0
Reserved		MDI ESD Event Counter					
RO-0		RO-0					

表 7-56. ESDS Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RO	0	Reserved
13:8	xMII ESD Event Counter	RO	0	**xMII ESD Counter:** When the integrated ESD structure is activated on the xMII interface, the xMII ESD counter will increment. There is no ESD dead-time built into the counter, which means that even with a single pulse event more than one ESD event could be logged. Counter cleared on power cycle. It cannot be cleared by hardware reset.
7:6	Reserved	RO	0	Reserved
5:0	MDI ESD Event Counter	RO	0	**MDI ESD Counter:** When the integrated ESD structure is activated on the xMII interface, the MDI ESD counter will increment. There is no ESD dead-time built into the counter, which means that even with a single pulse event more than one ESD event could be logged. MDI is in reference to the TRD+ and TRD- pins. Counter cleared on power cycle. It cannot be cleared by hardware reset.

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7.6.35 SGMII_AUTO_TIMER Register 0x0456 – SGMII Auto-Negotiation Timer Configuration Register

図 7-49. SGMII Auto-Negotiation Timer Configuration Register (SGMII_AUTO_TIMER)

15	14	13	12	11	10	9	8
Reserved		SGMII Auto-Negotiation Timer		**Reserved**			
RO-0		RW-01		RO-0000 0000 1000			
7	6	5	4	3	2	1	0

表 7-57. SGMII_AUTO_TIMER Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RO	0	Reserved
13:12	SGMII Auto-Negotiation Timer	RW	01	**SGMII Auto-Negotiation Timer:** 00 = 1.6ms 01 = 2µs 10 = 800µs 11 = 11ms
11:0	Reserved	RO	0000 0000 1000	Reserved

7.6.36 SGMII_STAT Register 0x0459 – SGMII Auto-Negotiation Status Register

図 7-50. SGMII Auto-Negotiation Status Register (SGMII_STAT)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
						SGMII Page Received	SGMII Auto-Negotiation Complete
						RO-0	RO-0

表 7-58. SGMII_STAT Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:2	Reserved	RO	0	Reserved
1	SGMII Page Received	RO	0	**SGMII Page Received:** 1 = Auto-Negotiation page has been received 0 = No new page received
0	SGMII Auto-Negotiation Complete	RO	0	**SGMII Auto-Negotiation Complete:** 1 = SGMII Auto-Negotiation process completed 0 = SGMII Auto-Negotiation process not complete

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7.6.37 LED_CFG1 Register 0x0460 – LED Configuration Register #1

図 7-51. LED Configuration Register #1 (LED_CFG1)

15	14	13	12	11	10	9	8
Reserved		LED Blink Rate Control		LED_2 Control			
RW-0		RW-10		RW-0110			
7	6	5	4	3	2	1	0
LED_1 Control				LED_0 Control			
RW-0001				RW-0000			

表 7-59. LED_CFG1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RW	0	Reserved
13:12	LED Blink Rate Control	RW	10	**Blink Rate Control:** 00 = 20Hz (50ms) 01 = 10Hz (100ms) 10 = 5Hz (200ms) 11 = 2Hz (500ms)
11:8	LED_2 Control	RW	0110	**LED_2 Control:** Selects the source for LED_2. Use same reference as defined by bits [3:0] in this register.
7:4	LED_1 Control	RW	0001	**LED_1 Control:** Selects the source for LED_1. Use same reference as defined by bits [3:0] in this register.
3:0	LED_0 Control	RW	0000	**LED_0 Control:** Selects the source for LED_0. 0000 = LINK OK 0001 = LINK OK + RX/TX Activity 0010 = LINK OK + TX Activity 0011 = LINK OK + RX Activity 0100 = LINK OK + 100BASE-T1 100BASE-T1 Master 0101 = LINK OK + 100BASE-T1 100BASE-T1 Slave 0110 = TX/RX Activity 0111 = Reserved 1000 = Reserved 1001 = Link Lost (remains on until register 0x1 is read) 1010 = Blink for PRBS error (remains ON for single error, remains until counter is cleared) 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved

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7.6.38 xMII_IMP_CTRL Register 0x0461 – xMII Impedance Control Register

図 7-52. xMII Impedance Control Register (xMII_IMP_CTRL)

15	14	13	12	11	10	9	8
Reserved							
RW-0000 0100 000							
7	6	5	4	3	2	1	0
xMII Impedance Control							**Reserved**
RW-1 000							RW-0

表 7-60. xMII_IMP_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:5	Reserved	RW	0000 0100 000	Reserved
4:1	xMII Impedance Control	RW	1 000	**MAC Impedance Control:** MAC Impedance Control sets the series termination value within the DP83TC811-Q1. This field controls the following pins: RX_D[3:0], RX_CLK, RX_ER, and RX_DV. 0 000 = 99Ω 0 001 = 91Ω 0 010 = 84Ω 0 011 = 78Ω 0 100 = 73Ω 0 101 = 69Ω 0 110 = 65Ω 0 111 = 61Ω 1 000 = 58Ω (default) 1 001 = 55Ω 1 010 = 53Ω 1 011 = 50Ω 1 100 = 48Ω 1 101 = 46Ω 1 110 = 44Ω 1 111 = 42Ω Note: Individual pin control is not supported.
0	Reserved	RW	0	Reserved

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7.6.39 IO_CTRL1 Register 0x0462 – GPIO Control Register #1

図 7-53. GPIO Control Register #1 (IO_CTRL1)

15	14	13	12	11	10	9	8
Reserved	LED_1 Clock Select			**Reserved**	LED_1 GPIO Select		
RO-0	RW-000			RO-0	RW-000		
7	6	5	4	3	2	1	0
Reserved	LED_0 Clock Select			**Reserved**	LED_0 GPIO Select		
RO-0	RW-000			RO-0	RW-000		

表 7-61. IO_CTRL1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14:12	LED_1 Clock Select	RW	000	**LED_1 Clock Select:** 000 = XI Clock 001 = TX_TCLK Clock
11	Reserved	RO	0	Reserved
10:8	LED_1 GPIO Select	RW	000	**LED_1 GPIO Select:** 000 = LED_1 001 = Clock 010 = WoL 011 = Undervoltage Indication 100 = 1588 Transmit 101 = 1588 Receive 110 = Constant '0' 111 = Constant '1'
7	Reserved	RO	0	Reserved
6:4	LED_0 Clock Select	RW	000	**LED_0 Clock Select:** 000 = XI Clock 001 = TX_TCLK Clock
3	Reserved	RO	0	Reserved
2:0	LED_0 GPIO Select	RW	000	**LED_0 GPIO Select:** 000 = LED_0 001 = Clock 010 = WoL 011 = Undervoltage Indication 100 = 1588 Transmit 101 = 1588 Receive 110 = Constant '0' 111 = Constant '1'

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7.6.40 IO_CTRL2 Register 0x0463 – GPIO Control Register #2

図 7-54. GPIO Control Register #2 (IO_CTRL2)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
CLKOUT Clock Select				**Reserved**	CLKOUT GPIO Select		
RW-0000				RO-0	RW-001		

表 7-62. IO_CTRL2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Reserved	RO	0	Reserved
7:4	CLKOUT Clock Select	RW	0000	**CLKOUT Clock Select:** 0000 = XI Clock 0001 = TX_TCLK Clock
3	Reserved	RO	0	Reserved
2:0	CLKOUT GPIO Select	RW	001	**CLKOUT GPIO Select:** 000 = LED_2 001 = Clock 010 = WoL 011 = Undervoltage Indication 100 = 1588 Transmit 101 = 1588 Receive 110 = Constant '0' 111 = Constant '1'

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7.6.41 STRAP Register 0x0467 – Strap Configuration Register

図 7-55. Strap Configuration Register (STRAP)

15	14	13	12	11	10	9	8
LED_1 Bootstrap		RX_DV Bootstrap		RX_ER Bootstrap		LED_0 Bootstrap	
RO/Strap		RO/Strap		RO/Strap		RO/Strap	
7	6	5	4	3	2	1	0
RX_D0 Bootstrap		RX_D1 Bootstrap		RX_D2 Bootstrap		RX_D3 Bootstrap	
RO/Strap		RO/Strap		RO/Strap		RO/Strap	

表 7-63. STRAP Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	LED_1 Bootstrap	RO	Strap	**LED_1 Bootstrap Mode:** 00 = Mode 1; Autonomous Enabled 01 = Mode 2; RESERVED 10 = Mode 3; RESERVED 11 = Mode 4; Autonomous Disabled Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
13:12	RX_DV Bootstrap	RO	Strap	**RX_DV Bootstrap Mode:** 00 = Mode 1; PHY_AD[0] = 0, PHY_AD[2] = 0 01 = Mode 2; PHY_AD[0] = 0, PHY_AD[2] = 1 10 = Mode 3; PHY_AD[0] = 1, PHY_AD[2] = 1 11 = Mode 4; PHY_AD[0] = 1, PHY_AD[2] = 0 Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
11:10	RX_ER Bootstrap	RO	Strap	**RX_ER Bootstrap Mode:** 00 = Mode 1; PHY_AD[1] = 0, PHY_AD[3] = 0 01 = Mode 2; PHY_AD[1] = 0, PHY_AD[3] = 1 10 = Mode 3; PHY_AD[1] = 1, PHY_AD[3] = 1 11 = Mode 4; PHY_AD[1] = 1, PHY_AD[3] = 0 Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
9:8	LED_0 Bootstrap	RO	Strap	**LED_0 Bootstrap Mode:** 00 = Mode 1; 100BASE-T1 Slave Mode 01 = Mode 2; RESERVED 10 = Mode 3; RESERVED 11 = Mode 4; 100BASE-T1 Master Mode Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.

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表 7-63. STRAP Field Descriptions (続き)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:6	RX_D0 Bootstrap	RO	Strap	**RX_D0 Bootstrap Mode:** 00 = Mode 1; MAC[0] = 0, TEST[0] = 0 01 = Mode 2; MAC[0] = 0, TEST[0] = 1 10 = Mode 3; MAC[0] = 1, TEST[0] = 1 11 = Mode 4; MAC[0] = 1, TEST[0] = 0 Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
5:4	RX_D1 Bootstrap	RO	Strap	**RX_D1 Bootstrap Mode:** 00 = Mode 1; MAC[1] = 0, TEST[1] = 0 01 = Mode 2; MAC[1] = 0, TEST[1] = 1 10 = Mode 3; MAC[1] = 1, TEST[1] = 1 11 = Mode 4; MAC[1] = 1, TEST[1] = 0 Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
3:2	RX_D2 Bootstrap	RO	Strap	**RX_D2 Bootstrap Mode:** 00 = Mode 1; MAC[2] = 0, TEST[2] = 0 01 = Mode 2; MAC[2] = 0, TEST[2] = 1 10 = Mode 3; MAC[2] = 1, TEST[2] = 1 11 = Mode 4; MAC[2] = 1, TEST[2] = 0 Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.
1:0	RX_D3 Bootstrap	RO	Strap	**RX_D3 Bootstrap Mode:** 00 = Mode 1; Required Strap Mode 01 = Mode 2; RESERVED 10 = Mode 3; RESERVED 11 = Mode 4; RESERVED Refer to the strap section in the data sheet for information regarding PHY configuration. **Note:** Bit values ('00', '01', '10', '11') are just used to indicate the Strap Mode and do not reflect the same bit sequence that is defined in the strap section of the data sheet.

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7.6.42 LED_CFG2 Register 0x0469 – LED Configuration Register #2

図 7-56. LED Configuration Register #2 (LED_CFG2)

15	14	13	12	11	10	9	8
Reserved					LED_2 Polarity	LED_2 Override Value	LED_2 Override Enable
RO-0					RO-0	RO-0	RO-0
7	6	5	4	3	2	1	0
Reserved	LED_1 Polarity	LED_1 Override Value	LED_1 Override Enable	**Reserved**	LED_0 Polarity	LED_0 Override Value	LED_0 Override Enable
RO-0	RW/Strap	RO-0	RO-0	RO-0	RW/Strap		RO-0

表 7-64. LED_CFG2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11	Reserved	RO	0	Reserved
10	LED_2 Polarity	RW	0	**LED_2 Polarity:** 1 = Active HIGH 0 = Active LOW
9	LED_2 Override Value	RW	0	**LED_2 Override Value:** 1 = Force HIGH 0 = Force LOW
8	LED_2 Override Enable	RW	0	**LED_2 Override Enable:** 1 = Enable force override 0 = Normal operation
7	Reserved	RO	0	Reserved
6	LED_1 Polarity	RW	Strap	**LED_1 Polarity:** 1 = Active HIGH 0 = Active LOW
5	LED_1 Override Value	RW	0	**LED_1 Override Value:** 1 = Force HIGH 0 = Force LOW
4	LED_1 Override Enable	RW	0	**LED_1 Override Enable:** 1 = Enable force override 0 = Normal operation
3	Reserved	RO	0	Reserved
2	LED_0 Polarity	RW	Strap	**LED_0 Polarity:** 1 = Active HIGH 0 = Active LOW
1	LED_0 Override Value	RW	0	**LED_0 Override Value:** 1 = Force HIGH 0 = Force LOW
0	LED_0 Override Enable	RW	0	**LED_0 Override Enable:** 1 = Enable force override 0 = Normal operation

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7.6.43 PLR_CFG Register 0x0475 – Polarity Auto-Correction Configuration Register

図 7-57. Polarity Auto-Correction Configuration Register (PLR_CFG)

15	14	13	12	11	10	9	8
Reserved		Polarity Value	Force Polarity Enable	**Reserved**			
RW-0		RW-0	RW-0	RW-0			
7	6	5	4	3	2	1	0
Reserved							
RW-0							

表 7-65. PLR_CFG1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RW	0	Reserved
13	Polarity Value	RW	0	**Force Polarity Value:** 1 = Reverse polarity 0 = Normal polarity
12	Force Polarity Enable	RW	0	**Auto-Polarity Correction Override Enable:** 1 = Enable force polarity override (polarity of MDI commanded by bit[13]) 0 = Normal auto-polarity correction operation
11:0	Reserved	RW	0	Reserved

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7.6.44 MON_CFG1 Register 0x0480 – Monitor Configuration Register #1

図 7-58. Monitor Configuration Register #1 (MON_CFG1)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
				Monitors Configuration Cycle Period			
				RW-0010			

表 7-66. MON_CFG1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:4	Reserved	RO	0	Reserved
3:0	Monitors Configuration Cycle Period	RW	0010	**Monitors Configuration Cycle Period:** If monitors are set to periodic mode, bits[3:0] determine the sampling cycle time. Cycle time has a range of 16ms - 240ms. **Example:** If value of bits[3:0] = 0b0001, sample time is 16ms. **Note:** 0b0000 is invalid

7.6.45 MON_CFG2 Register 0x0481 – Monitor Configuration Register #2

図 7-59. Monitor Configuration Register #2 (MON_CFG2)

15	14	13	12	11	10	9	8
Reserved							
RO-0000 0000 1010 00							
7	6	5	4	3	2	1	0
						Temperature / Supply Monitor Periodic Mode	Temperature / Supply Monitor Start
						RW-1	RW/SC-0

表 7-67. MON_CFG2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:2	Reserved	RW	0000 0000 1010 00	Reserved
1	Temperature / Supply Monitor Periodic Mode	RW	1	**Temperature and Supply Monitor Periodic Mode:** 1 = Temperature and supply monitor are activated periodically 0 = Temperature and supply monitor is a single run **Note:** When temperature and supply monitor are activated periodically, cycle time is determined by bits[3:0] in register 0x480.
0	Temperature / Supply Monitor Start	RW, SC	0	**Temperature and Supply Monitor Start:** 1 = Start temperature and supply monitor function (this bit self-clears) 0 = Normal operation

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7.6.46 MON_CFG3 Register 0x0482 – Monitor Configuration Register #3

図 7-60. Monitor Configuration Register #3 (MON_CFG3)

15	14	13	12	11	10	9	8
Reserved	Undervoltage Threshold Configuration			**Reserved**	Overvoltage Threshold Configuration		
RW-0	RW-111			RW-0	RW-000		
7	6	5	4	3	2	1	0
Reserved					Overtemperature Threshold Configuration		
RW-0					RW-111		

表 7-68. MON_CFG3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RW	0	Reserved
14:12	Undervoltage Threshold Configuration	RW	111	**Undervoltage Threshold Configuration:** 000 = Voltage > VDD + 9% 001 = VDD + 1.5% < Voltage < VDD + 9% 010 = VDD - 4.5% < Voltage < VDD + 1.5% 011 = VDD - 7.5% < Voltage < VDD - 4.5% 100 = VDD - 10.5% < Voltage < VDD - 7.5% 101 = VDD - 13.5% < Voltage < VDD - 10.5% 110 = VDD - 16.5% < Voltage < VDD - 13.5% 111 = Voltage < VDD - 16.5% **Note 1:** VDD = 1.8V, 2.5V, 3.3V (for VDDIO), or 3.3V (for VDDA) **Note 2:** VDD +/- X% represents VDD +/- VDD*(X)/100
11	Reserved	RW	0	Reserved
10:8	Overvoltage Threshold Configuration	RW	000	**Overvoltage Threshold Configuration:** 000 = Voltage > VDD + 9% 001 = VDD + 1.5% < Voltage < VDD + 9% 010 = VDD - 4.5% < Voltage < VDD + 1.5% 011 = VDD - 7.5% < Voltage < VDD - 4.5% 100 = VDD - 10.5% < Voltage < VDD - 7.5% 101 = VDD - 13.5% < Voltage < VDD - 10.5% 110 = VDD - 16.5% < Voltage < VDD - 13.5% 111 = Voltage < VDD - 16.5% **Note 1:** VDD = 1.8V, 2.5V, 3.3V (for VDDIO), or 3.3V (for VDDA) **Note 2:** VDD +/- X% represents VDD +/- VDD*(X)/100
7:3	Reserved	RW	0	Reserved
2:0	Overtemperature Threshold Configuration	RW	111	**Overtemperature Threshold Configuration:** 000 = Temperature < -40°C 001 = -40°C < Temperature < 0°C 010 = 0°C < Temperature < 30°C 011 = 30°C < Temperature < 70°C 100 = 70°C < Temperature < 100°C 101 = 100°C < Temperature < 135°C 110 = 135°C < Temperature < 165°C 111 = Temperature > 165°C

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7.6.47 MON_STAT1 Register 0x0483 – Monitor Status Register #1

図 7-61. Monitor Status Register #1 (MON_STAT1)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
					Temperature Monitor Value		
					RO-000		

表 7-69. MON_STAT1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:3	Reserved	RO	0	Reserved
2:0	Temperature Monitor Value	RO	000	**Temperature Monitor Value:** 000 = Temperature < -40°C 001 = -40°C < Temperature < 0°C 010 = 0°C < Temperature < 30°C 011 = 30°C < Temperature < 70°C 100 = 70°C < Temperature < 100°C 101 = 100°C < Temperature < 135°C 110 = 135°C < Temperature < 165°C 111 = Temperature > 165°C

7.6.48 MON_STAT2 Register 0x0484 – Monitor Status Register #2

図 7-62. Monitor Status Register #2 (MON_STAT2)

15	14	13	12	11	10	9	8
Reserved	VDDIO Supply Monitor Value			**Reserved**	VDDA Supply Monitor Value		
RO-0	RO-000			RO-0	RO-000		
7	6	5	4	3	2	1	0
Reserved							
RO-0							

表 7-70. MON_STAT2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	0	Reserved
14:12	VDDIO Supply Monitor Value	RO	000	**VDDIO Supply Monitor Value:** 000 = Voltage > VDDIO + 9% 001 = VDDIO + 1.5% < Voltage < VDDIO + 9% 010 = VDDIO - 4.5% < Voltage < VDDIO + 1.5% 011 = VDDIO - 7.5% < Voltage < VDDIO - 4.5% 100 = VDDIO - 10.5% < Voltage < VDDIO - 7.5% 101 = VDDIO - 13.5% < Voltage < VDDIO - 10.5% 110 = VDDIO - 16.5% < Voltage < VDDIO - 13.5% 111 = Voltage < VDDIO - 16.5% **Note 1:** VDDIO = 1.8V, 2.5V, 3.3V **Note 2:** VDDIO +/- X% represents VDDIO +/- VDDIO*(X)/100
11	Reserved	RO	0	Reserved

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表 7-70. MON_STAT2 Field Descriptions (続き)

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
10:8	VDDA Supply Monitor Value	RO	000	**VDDA Supply Monitor Value:** 000 = Voltage > VDDA + 9% 001 = VDDA + 1.5% < Voltage < VDDA + 9% 010 = VDDA - 4.5% < Voltage < VDDA + 1.5% 011 = VDDA - 7.5% < Voltage < VDDA - 4.5% 100 = VDDA - 10.5% < Voltage < VDDA - 7.5% 101 = VDDA - 13.5% < Voltage < VDDA - 10.5% 110 = VDDA - 16.5% < Voltage < VDDA - 13.5% 111 = Voltage < VDDA - 16.5% **Note 1:** VDDA = 3.3V **Note 2:** VDDA +/- X% represents VDDA +/- VDDA*(X)/100
7:0	Reserved	RO	0	Reserved

7.6.49 PCS_CTRL1 Register 0x0485 – PCS Control Register #1

図 7-63. PCS Control Register #1 (PCS_CTRL1)

15	14	13	12	11	10	9	8
Reserved		IPG Scrambler Lock Check Disable	Link Control	**Reserved**			Link-Up Descrambler Lock Configuration
RW-0		RW-0	RW-1	RW-0			RW-0111 1000
7	6	5	4	3	2	1	0
Link-Up Descrambler Lock Configuration							
RW-0111 1000							

表 7-71. PCS_CTRL1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RW	0	Reserved
13	IPG Scrambler Lock Check Disable	RW	0	**IPG Scrambler Lock Check Diable:** 1 = Scrambler lock check is disabled during IPG 0 = Scrambler lock check is enabled during IPG
12	Link Control	RW	1	**Link Control:** 1 = Enable training and link-up to start 0 = Disable training and link-up
11:9	Reserved	RO	0	Reserved
8:0	Link-Up Descrambler Lock Configuration	RW	0111 1000	**Link-Up Descrambler Lock Configuration:** Determines the number of initial idle symbols to determine descrambler lock (LINK) Default set to 120 IDLES

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7.6.50 PCS_CTRL2 Register – 0x0486 PCS Control Register #2

図 7-64. PCS Control Register #2 (PCS_CTRL2)

15	14	13	12	11	10	9	8
Reserved		Descrambler Error Count Configuration					
RW-00		RW-00 1010					
7	6	5	4	3	2	1	0
Reserved			Remote Receiver Configuration				
RW-000			RW-0 0101				

表 7-72. PCS_CTRL2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Reserved	RW	00	Reserved
13:9	Descrambler Error Count Configuration	RW	00 101	**Descrambler Error Count Configuration:** Determines the number of error (non-idle) symbols to determine descrambler loss of lock (no LINK) Default set to 10 symbols
8:5	Reserved	RW	0 000	Reserved
4:0	Remote Receiver Configuration	RW	0 0101	**Remote Receiver Configuration:** Determines the number of error symbols for remote receiver status to go LOW. Default set to 5 symbols

7.6.51 LPS_CTRL2 Register 0x0487 – LPS Control Register #2

図 7-65. LPS Control Register #2 (LPS_CTRL2)

15	14	13	12	11	10	9	8
Reserved							
RW-0000 1010 0000 000							
7	6	5	4	3	2	1	0
							PCS LPS Enable
							RW--0

表 7-73. LPS_CTRL2 Register 0x0487 – LPS Control Register #2

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:1	Reserved	RW	0000 1010 0000 000	Reserved
0	PCS LPS Enable	RW	0	**PCS LPS Enable:** 1 = LPS enabled in PCS 0 = LPS disabled in PCS Device must have this bit enabled to transmit and receive LPS code-groups.

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7.6.52 INTER_CFG Register 0x0489 – Interleave Configuration

図 7-66. Interleave Configuration (INTER_CFG)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
					Force Interleave	Interleave Enable	Interleave Detection Enable
					RW-0	RW-0	RW-1

表 7-74. INTER_CFG Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:3	Reserved	RO	0	Reserved
2	Force Interleave	RW	0	**Force Interleave:** 1 = Force interleave on TX 0 = Normal operation
1	Interleave Enable	RW	0	**Interleave Enable:** 1 = Enable interleave on TX if interleave detected on RX 0 = Normal operation
0	Interleave Detection Enable	RW	1	**Interleave Detection Enable:** 1 = Enable interleave detection 0 = Disable interleave detection

7.6.53 LPS_CTRL3 Register 0x0493 – LPS Control Register #3

図 7-67. LPS Control Register #3 (LPS_CTRL3)

15	14	13	12	11	10	9	8
Reserved							
RW-0							
7	6	5	4	3	2	1	0
		sleep_rqst_timer Setting		**Reserved**			
		RW-01		RW-0100			

表 7-75. LPS_CTRL3 Register 0x0493 – LPS Control Register #3

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6	Reserved	RW	0	Reserved
5:4	sleep_rqst_timer	RW	01	**sleep_rqst_timer Setting:** 00 = 0.4ms 01 = 1ms 10 = 4ms 11 = 8ms
3:0	Reserved	RW	0100	Reserved

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7.6.54 JAB_CFG Register 0x0496 – Jabber Configuration Register

図 7-68. Jabber Configuration Register (JAB_CFG)

15	14	13	12	11	10	9	8
Reserved					Jabber Timout Configuration		
RO-0					RW-100 0100 1100		
7	6	5	4	3	2	1	0
Jabber Timout Configuration							
RW-100 0100 1100							

表 7-76. JAB_CFG Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:11	Reserved	RO	0	Reserved
10:0	Jabber Timout Configuration	RW	100 0100 1100	**Jabber Timout Configuration:** Sets time to determine a jabber condition. Default set to 1100us. **Note:** Convert value read in this register to decimal format to find the time in micro seconds

7.6.55 TEST_MODE_CTRL Register 0x0497 – Test Mode Control Register

図 7-69. Test Mode Control Register (TEST_MODE_CTRL)

15	14	13	12	11	10	9	8
Reserved						Test Mode 1 Symbol Control	
RO-0000 00						RW-01 1100	
7	6	5	4	3	2	1	0
				Reserved			
				RO-0000			

表 7-77. TEST_MODE_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10	Reserved	RO	0000 00	Reserved
9:4	Test Mode 1 Symbol Control	RW	01 1100	**Test Mode 1 Symbol Control:** Sets the number of +1/-1 symbols to send in Test Mode 1 Number of Symbols = (2*FIELD_VALUE + 2) Example: FIELD_VALUE = 28 Number of Symbols = (2*28 + 2) = 58 Time = 58*15ns = 870ns
3:0	Reserved	RW	0000	Reserved

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7.6.56 WOL_CFG Register 0x04A0 – WoL Configuration Register

図 7-70. WoL Configuration Register (WOL_CFG)

15	14	13	12	11	10	9	8
Bit Nibble Swap		SFD Byte	CRC Gate	WoL Level Change Indication Clear	WoL Pulse Indication Select		WoL Indication Select
RW-00		RW-0	RW-1	W/SC-0	RW-00		RW-0
7	6	5	4	3	2	1	0
WoL Enable	Bit Mask Flag	Secure-ON Enable	**Reserved**			WoL Pattern Enable	WoL Magic Packet Enable
RW-0	RW-0	RW-0	RW-0			RW-0	RW-0

表 7-78. WOL_CFG Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:14	Bit Nibble Swap	RW	00	**Bit Nibble Swap:** 00 = normal order, no swap (RXD [3:0]) 01 = swap bits order (RXD [0:3]) 10 = swap nibbles order (RXD [3:0] , RXD [7:4]) 11 = swap bits order in each nibble (RXD [4:7] , RXD [0:3])
13	SFD Byte	RW	0	**SFD Byte Search:** 1 = SFD is 0x5D (i.e. Receive module searches for 0x5D) 0 = SFD is 0xD5 (i.e. Receive module searches for 0xD5)
12	CRC Gate	RW	1	**CRC Gate:** 1 = Bad CRC gates Magic Packet and Pattern Indications 0 = Disable bad CRC gate **Note:** If Bad CRC gate is disabled, there will be no indication (status, interrupt, GPIO) if the device receives a bad CRC.
11	WoL Level Change Indication Clear	W, SC	0	**WoL Level Change Indication Clear:** If WoL Indication is set for Level change mode, this bit clears the level upon a write.
10:9	WoL Pulse Indication Select	RW	00	**WoL Pulse Indication Select:** Only valid when WoL Indication is set for Pulse mode. 00 = 8 clock cycles (of 100MHz clock) 01 = 16 clock cycles 10 = 32 clock cycles 11 = 64 clock cycles
8	WoL Indication Select	RW	0	**WoL Indication Select:** 1 = Level change mode 0 = Pulse mode
7	WoL Enable	RW	0	**WoL Enable:** 1 = Enable Wake-on-LAN (WoL) 0 = normal operation
6	Bit Mask Flag	RW	0	**Bit Mask Flag**
5	Secure-ON Enable	RW	0	**Enable** Secure-ON password for Magic Packets
4:2	Reserved	RW	0	Reserved
1	WoL Pattern Enable	RW	0	**Enable** Interrupt upon reception of packet with configured pattern
0	WoL Magic Packet Enable	RW	0	**Enable** Interrupt upon reception of Magic Packet

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7.6.57 WOL_STAT Register 0x04A1 – WoL Status Register

図 7-71. WoL Status Register (WOL_STAT)

15	14	13	12	11	10	9	8
Reserved			WoL Interrupt Source	**Reserved**			
RO-0			RW-0	RO-0			
7	6	5	4	3	2	1	0
SFD Error	Bad CRC	Secure-On Hack Flag	**Reserved**			WoL Pattern Status	WoL Magic Packet Status
RO/LH/SC-0	RO/LH/SC-0	RO/LH/SC-0	RO/LH/SC-0			RO/LH/SC-0	RO/LH/SC-0

表 7-79. WOL_STAT Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:13	Reserved	RO	0	Reserved
12	WoL Interrupt Source	RW	0	**WoL Interrupt Source:** Source of Interrupt for bit [1] of register 0x13. 1 = WoL Interrupt 0 = Data Polarity Interrupt When enabling WoL, this bit is automatically set to WoL Interrupt.
11:8	Reserved	RO	0	Reserved
7	SFD Error	RO, LH, SC	0	**SFD Error:** 1 = Packet with SFD error (without the SFD byte indicated in bit [13] register 0x4A0) 0 = No SFD error
6	Bad CRC	RO, LH, SC	0	**Bad CRC:** 1 = Bad CRC was received 0 = No bad CRC received
5	Secure-On Hack Flag	RO, LH, SC	0	**Secure-ON Hack Flag:** 1 = Invalid Password detected in Magic Packet 0 = Valid Secure-ON Password
4:2	Reserved	RO, LH, SC	0	Reserved
1	WoL Pattern Status	RO, LH, SC	0	**WoL Pattern Status:** 1 = Valid packet with configured pattern received 0 = No valid packet with configured pattern received
0	WoL Magic Packet Status	RO, LH, SC	0	**WoL Magic Packet Status:** 1 = Valid Magic Packet received 0 = No valid Magic Packet received

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7.6.58 WOL_DA1 Register 0x04A2 – WoL Destination Address Configuration Register #1

図 7-72. WoL Destination Address Configuration Register #1 (WOL_DA1)

15	14	13	12	11	10	9	8
MAC Destination Address Byte 4							
RW-0							
7	6	5	4	3	2	1	0
MAC Destination Address Byte 5							
RW-0							

表 7-80. WOL_DA1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	MAC Destination Address Byte 4	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 5	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

7.6.59 WOL_DA2 Register 0x04A3 – WoL Destination Address Configuration Register #2

図 7-73. WoL Destination Address Configuration Register #2 (WOL_DA2)

15	14	13	12	11	10	9	8
MAC Destination Address Byte 2							
RW-0							
7	6	5	4	3	2	1	0
MAC Destination Address Byte 3							
RW-0							

表 7-81. WOL_DA2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	MAC Destination Address Byte 2	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 3	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

7.6.60 WOL_DA3 Register 0x04A4 – WoL Destination Address Configuration Register #3

図 7-74. WoL Destination Address Configuration Register #3 (WOL_DA3)

15	14	13	12	11	10	9	8
MAC Destination Address Byte 0							
RW-0							
7	6	5	4	3	2	1	0
MAC Destination Address Byte 1							
RW-0							

表 7-82. WOL_DA3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	MAC Destination Address Byte 0	RW	0	**Perfect Match Data:** Configured for MAC Destination Address
7:0	MAC Destination Address Byte 1	RW	0	**Perfect Match Data:** Configured for MAC Destination Address

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7.6.61 RXSOP1 Register 0x04A5 – Receive Secure-ON Password Register #1

図 7-75. Receive Secure-ON Password Register #1 (RXSOP1)

15	14	13	12	11	10	9	8
Secure-ON Password Byte 1							
RW-0							
7	6	5	4	3	2	1	0
Secure-ON Password Byte 0							
RW-0							

表 7-83. RXSOP1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Secure-ON Password Byte 1	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 0	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

7.6.62 RXSOP2 Register 0x04A6 – Receive Secure-ON Password Register #2

表 7-84. Receive Secure-ON Password Register #2 (RXSOP2)

15	14	13	12	11	10	9	8
Secure-ON Password Byte 3							
RW-0							
7	6	5	4	3	2	1	0
Secure-ON Password Byte 2							
RW-0							

表 7-85. RXSOP2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Secure-ON Password Byte 3	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 2	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

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7.6.63 RXSOP3 Register 0x04A7 – Receive Secure-ON Password Register #3

図 7-76. Receive Secure-ON Password Register #3 (RXSOP3)

15	14	13	12	11	10	9	8
Secure-ON Password Byte 5							
RW-0							
7	6	5	4	3	2	1	0
Secure-ON Password Byte 4							
RW-0							

表 7-86. RXSOP3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Secure-ON Password Byte 5	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets
7:0	Secure-ON Password Byte 4	RW	0	**Secure-ON Password Select:** Secure-ON password for Magic Packets

7.6.64 RXPAT1 Register 0x04A8 – Receive Pattern Register #1

図 7-77. Receive Pattern Register #1 (RXPAT1)

15	14	13	12	11	10	9	8
Pattern Byte 1							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 0							
RW-0							

表 7-87. RXPAT1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 1	RW	0	**Pattern Configuration:** Configures byte 1 of the pattern
7:0	Pattern Byte 0	RW	0	**Pattern Configuration:** Configures byte 0 of the pattern

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7.6.65 RXPAT2 Register 0x04A9 – Receive Pattern Register #2

図 7-78. Receive Pattern Register #2 (RXPAT2)

15	14	13	12	11	10	9	8
Pattern Byte 3							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 2							
RW-0							

表 7-88. RXPAT2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 3	RW	0	**Pattern Configuration:** Configures byte 3 of the pattern
7:0	Pattern Byte 2	RW	0	**Pattern Configuration:.** Configures byte 2 of the pattern

7.6.66 RXPAT3 Register 0x04AA – Receive Pattern Register #3

図 7-79. Receive Pattern Register #3 (RXPAT3)

15	14	13	12	11	10	9	8
Pattern Byte 5							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 4							
RW-0							

表 7-89. RXPAT3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 5	RW	0	**Pattern Configuration:** Configures byte 5 of the pattern
7:0	Pattern Byte 4	RW	0	**Pattern Configuration:** Configures byte 4 of the pattern

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7.6.67 RXPAT4 Register 0x04AB – Receive Pattern Register #4

図 7-80. Receive Pattern Register #4 (RXPAT4)

15	14	13	12	11	10	9	8
Pattern Byte 7							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 6							
RW-0							

表 7-90. RXPAT4 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 7	RW	0	**Pattern Configuration:** Configures byte 7 of the pattern
7:0	Pattern Byte 6	RW	0	**Pattern Configuration:** Configures byte 6 of the pattern

7.6.68 RXPAT5 Register 0x04AC – Receive Pattern Register #5

図 7-81. Receive Pattern Register #5 (RXPAT5)

15	14	13	12	11	10	9	8
Pattern Byte 9							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 8							
RW-0							

表 7-91. RXPAT5 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 9	RW	0	**Pattern Configuration:** Configures byte 9 of the pattern
7:0	Pattern Byte 8	RW	0	**Pattern Configuration:** Configures byte 8 of the pattern

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7.6.69 RXPAT6 Register 0x04AD – Receive Pattern Register #6

図 7-82. Receive Pattern Register #6 (RXPAT6)

15	14	13	12	11	10	9	8
Pattern Byte 11							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 10							
RW-0							

表 7-92. RXPAT6 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 11	RW	0	**Pattern Configuration:** Configures byte 11 of the pattern
7:0	Pattern Byte 10	RW	0	**Pattern Configuration:** Configures byte 10 of the pattern

7.6.70 RXPAT7 Register 0x04AE – Receive Pattern Register #7

図 7-83. Receive Pattern Register #7 (RXPAT7)

15	14	13	12	11	10	9	8
Pattern Byte 13							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 12							
RW-0							

表 7-93. RXPAT7 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 13	RW	0	**Pattern Configuration:** Configures byte 13 of the pattern
7:0	Pattern Byte 12	RW	0	**Pattern Configuration:** Configures byte 12 of the pattern

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7.6.71 RXPAT8 Register 0x04AF – Receive Pattern Register #8

図 7-84. Receive Pattern Register #8 (RXPAT8)

15	14	13	12	11	10	9	8
Pattern Byte 15							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 14							
RW-0							

表 7-94. RXPAT8 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 15	RW	0	**Pattern Configuration:** Configures byte 15 of the pattern
7:0	Pattern Byte 14	RW	0	**Pattern Configuration:** Configures byte 14 of the pattern

7.6.72 RXPAT9 Register 0x04B0 – Receive Pattern Register #9

図 7-85. Receive Pattern Register #9 (RXPAT9)

15	14	13	12	11	10	9	8
Pattern Byte 17							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 16							
RW-0							

表 7-95. RXPAT9 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 17	RW	0	**Pattern Configuration:** Configures byte 17 of the pattern
7:0	Pattern Byte 16	RW	0	**Pattern Configuration:** Configures byte 16 of the pattern

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7.6.73 RXPAT10 Register 0x04B1 – Receive Pattern Register #10

図 7-86. Receive Pattern Register #10 (RXPAT10)

15	14	13	12	11	10	9	8
Pattern Byte 19							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 18							
RW-0							

表 7-96. RXPAT10 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 19	RW	0	**Pattern Configuration:** Configures byte 19 of the pattern
7:0	Pattern Byte 18	RW	0	**Pattern Configuration:** Configures byte 18 of the pattern

7.6.74 RXPAT11 Register 0x04B2 Receive Pattern Register #11

図 7-87. Receive Pattern Register #11 (RXPAT11)

15	14	13	12	11	10	9	8
Pattern Byte 21							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 20							
RW-0							

表 7-97. RXPAT11 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 21	RW	0	**Pattern Configuration:** Configures byte 21 of the pattern
7:0	Pattern Byte 20	RW	0	**Pattern Configuration:** Configures byte 20 of the pattern

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7.6.75 RXPAT12 Register 0x04B3 – Receive Pattern Register #12

図 7-88. Receive Pattern Register #12 (RXPAT12)

15	14	13	12	11	10	9	8
Pattern Byte 23							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 22							
RW-0							

表 7-98. RXPAT12 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 23	RW	0	**Pattern Configuration:** Configures byte 23 of the pattern
7:0	Pattern Byte 22	RW	0	**Pattern Configuration:** Configures byte 22 of the pattern

7.6.76 RXPAT13 Register 0x04B4 – Receive Pattern Register #13

図 7-89. Receive Pattern Register #13 (RXPAT13)

15	14	13	12	11	10	9	8
Pattern Byte 25							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 24							
RW-0							

表 7-99. RXPAT13 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 25	RW	0	**Pattern Configuration:** Configures byte 25 of the pattern
7:0	Pattern Byte 24	RW	0	**Pattern Configuration:** Configures byte 24 of the pattern

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7.6.77 RXPAT14 Register 0x04B5 – Receive Pattern Register #14

図 7-90. Receive Pattern Register #14 (RXPAT14)

15	14	13	12	11	10	9	8
Pattern Byte 27							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 26							
RW-0							

表 7-100. RXPAT14 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 27	RW	0	**Pattern Configuration:** Configures byte 27 of the pattern
7:0	Pattern Byte 26	RW	0	**Pattern Configuration:** Configures byte 26 of the pattern

7.6.78 RXPAT15 Register 0x04B6 – Receive Pattern Register #15

図 7-91. Receive Pattern Register #15 (RXPAT15)

15	14	13	12	11	10	9	8
Pattern Byte 29							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 28							
RW-0							

表 7-101. RXPAT15 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 29	RW	0	**Pattern Configuration:** Configures byte 29 of the pattern
7:0	Pattern Byte 28	RW	0	**Pattern Configuration:** Configures byte 28 of the pattern

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7.6.79 RXPAT16 Register 0x04B7 – Receive Pattern Register #16

図 7-92. Receive Pattern Register #16 (RXPAT16)

15	14	13	12	11	10	9	8
Pattern Byte 31							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 30							
RW-0							

表 7-102. RXPAT16 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 31	RW	0	**Pattern Configuration:** Configures byte 31 of the pattern
7:0	Pattern Byte 30	RW	0	**Pattern Configuration:** Configures byte 30 of the pattern

7.6.80 RXPAT17 Register 0x04B8 – Receive Pattern Register #17

図 7-93. Receive Pattern Register #17 (RXPAT17)

15	14	13	12	11	10	9	8
Pattern Byte 33							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 32							
RW-0							

表 7-103. RXPAT17 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 33	RW	0	**Pattern Configuration:** Configures byte 33 of the pattern
7:0	Pattern Byte 32	RW	0	**Pattern Configuration:** Configures byte 32 of the pattern

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7.6.81 RXPAT18 Register 0x04B9 – Receive Pattern Register #18

図 7-94. Receive Pattern Register #18 (RXPAT18)

15	14	13	12	11	10	9	8
Pattern Byte 35							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 34							
RW-0							

表 7-104. RXPAT18 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 35	RW	0	**Pattern Configuration:** Configures byte 35 of the pattern
7:0	Pattern Byte 34	RW	0	**Pattern Configuration:** Configures byte 34 of the pattern

7.6.82 RXPAT19 Register 0x04BA Receive Pattern Register #19

図 7-95. Receive Pattern Register #19 (RXPAT19)

15	14	13	12	11	10	9	8
Pattern Byte 37							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 36							
RW-0							

表 7-105. RXPAT19 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 37	RW	0	**Pattern Configuration:** Configures byte 37 of the pattern
7:0	Pattern Byte 36	RW	0	**Pattern Configuration:** Configures byte 36 of the pattern

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7.6.83 RXPAT20 Register 0x04BB – Receive Pattern Register #20

図 7-96. Receive Pattern Register #20 (RXPAT20)

15	14	13	12	11	10	9	8
Pattern Byte 39							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 38							
RW-0							

表 7-106. RXPAT20 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 39	RW	0	**Pattern Configuration:** Configures byte 39 of the pattern
7:0	Pattern Byte 38	RW	0	**Pattern Configuration:** Configures byte 38 of the pattern

7.6.84 RXPAT21 Register 0x04BC – Receive Pattern Register #21

図 7-97. Receive Pattern Register #21 (RXPAT21)

15	14	13	12	11	10	9	8
Pattern Byte 41							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 40							
RW-0							

表 7-107. RXPAT21 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 41	RW	0	**Pattern Configuration:** Configures byte 41 of the pattern
7:0	Pattern Byte 40	RW	0	**Pattern Configuration:** Configures byte 40 of the pattern

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7.6.85 RXPAT22 Register 0x04BD – Receive Pattern Register #22

図 7-98. Receive Pattern Register #22 (RXPAT22)

15	14	13	12	11	10	9	8
Pattern Byte 43							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 42							
RW-0							

表 7-108. RXPAT22 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 43	RW	0	**Pattern Configuration:** Configures byte 43 of the pattern
7:0	Pattern Byte 42	RW	0	**Pattern Configuration:** Configures byte 42 of the pattern

7.6.86 RXPAT23 Register 0x04BE – Receive Pattern Register #23

図 7-99. Receive Pattern Register #23 (RXPAT23)

15	14	13	12	11	10	9	8
Pattern Byte 45							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 44							
RW-0							

表 7-109. RXPAT23 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 45	RW	0	**Pattern Configuration:** Configures byte 45 of the pattern
7:0	Pattern Byte 44	RW	0	**Pattern Configuration:** Configures byte 44 of the pattern

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7.6.87 RXPAT24 Register 0x04BF – Receive Pattern Register #24

図 7-100. Receive Pattern Register #24 (RXPAT24)

15	14	13	12	11	10	9	8
Pattern Byte 47							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 46							
RW-0							

表 7-110. RXPAT24 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 47	RW	0	**Pattern Configuration:** Configures byte 47 of the pattern
7:0	Pattern Byte 46	RW	0	**Pattern Configuration:** Configures byte 46 of the pattern

7.6.88 RXPAT25 Register 0x04C0 – Receive Pattern Register #25

図 7-101. Receive Pattern Register #25 (RXPAT25)

15	14	13	12	11	10	9	8
Pattern Byte 49							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 48							
RW-0							

表 7-111. RXPAT25 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 49	RW	0	**Pattern Configuration:** Configures byte 49 of the pattern
7:0	Pattern Byte 48	RW	0	**Pattern Configuration:** Configures byte 48 of the pattern

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7.6.89 RXPAT26 Register 0x04C1 – Receive Pattern Register #26

図 7-102. Receive Pattern Register #26 (RXPAT26)

15	14	13	12	11	10	9	8
Pattern Byte 51							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 50							
RW-0							

表 7-112. RXPAT26 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 51	RW	0	**Pattern Configuration:** Configures byte 51 of the pattern
7:0	Pattern Byte 50	RW	0	**Pattern Configuration:** Configures byte 50 of the pattern

7.6.90 RXPAT27 Register 0x04C2 Receive Pattern Register #27

図 7-103. Receive Pattern Register #27 (RXPAT27)

15	14	13	12	11	10	9	8
Pattern Byte 53							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 52							
RW-0							

表 7-113. RXPAT27 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 53	RW	0	**Pattern Configuration:** Configures byte 53 of the pattern
7:0	Pattern Byte 52	RW	0	**Pattern Configuration:** Configures byte 52 of the pattern

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7.6.91 RXPAT28 Register 0x04C3 – Receive Pattern Register #28

図 7-104. Receive Pattern Register #28 (RXPAT28)

15	14	13	12	11	10	9	8
Pattern Byte 55							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 54							
RW-0							

表 7-114. RXPAT28 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 55	RW	0	**Pattern Configuration:** Configures byte 55 of the pattern
7:0	Pattern Byte 54	RW	0	**Pattern Configuration:** Configures byte 54 of the pattern

7.6.92 RXPAT29 Register 0x04C4 – Receive Pattern Register #29

図 7-105. Receive Pattern Register #29 (RXPAT29)

15	14	13	12	11	10	9	8
Pattern Byte 57							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 56							
RW-0							

表 7-115. RXPAT29 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 57	RW	0	**Pattern Configuration:** Configures byte 57 of the pattern
7:0	Pattern Byte 56	RW	0	**Pattern Configuration:** Configures byte 56 of the pattern

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7.6.93 RXPAT30 Register 0x04C5 – Receive Pattern Register #30

図 7-106. Receive Pattern Register #30 (RXPAT30)

15	14	13	12	11	10	9	8
Pattern Byte 59							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 58							
RW-0							

表 7-116. RXPAT30 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 59	RW	0	**Pattern Configuration:** Configures byte 59 of the pattern
7:0	Pattern Byte 58	RW	0	**Pattern Configuration:** Configures byte 58 of the pattern

7.6.94 RXPAT31 Register 0x04C6 – Receive Pattern Register #31

図 7-107. Receive Pattern Register #31 (RXPAT31)

15	14	13	12	11	10	9	8
Pattern Byte 61							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 60							
RW-0							

表 7-117. RXPAT31 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 61	RW	0	**Pattern Configuration:** Configures byte 61 of the pattern
7:0	Pattern Byte 60	RW	0	**Pattern Configuration:** Configures byte 60 of the pattern

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7.6.95 RXPAT32 Register 0x04C7 – Receive Pattern Register #32

図 7-108. Receive Pattern Register #32 (RXPAT32)

15	14	13	12	11	10	9	8
Pattern Byte 63							
RW-0							
7	6	5	4	3	2	1	0
Pattern Byte 62							
RW-0							

表 7-118. RXPAT32 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:8	Pattern Byte 63	RW	0	**Pattern Configuration:** Configures byte 63 of the pattern
7:0	Pattern Byte 62	RW	0	**Pattern Configuration:** Configures byte 62 of the pattern

7.6.96 RXPBM1 Register 0x04C8 – Receive Pattern Byte Mask Register #1

図 7-109. Receive Pattern Byte Mask Register #1 (RXPBM1)

15	14	13	12	11	10	9	8
Mask Bytes 0 to 15							
RW-0							
7	6	5	4	3	2	1	0
Mask Bytes 0 to 15							
RW-0							

表 7-119. RXPBM1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Mask Bytes 0 to 15	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 0 to 15. For each byte '1' means it is masked.

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7.6.97 RXPBM2 Register 0x04C9 – Receive Pattern Byte Mask Register #2

図 7-110. Receive Pattern Byte Mask Register #2 (RXPBM2)

15	14	13	12	11	10	9	8
Mask Bytes 16 to 31							
RW-0							
7	6	5	4	3	2	1	0
Mask Bytes 16 to 31							
RW-0							

表 7-120. RXPBM2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Mask Bytes 16 to 31	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 16 to 31. For each byte '1' means it is masked.

7.6.98 RXPBM3 Register 0x04CA – Receive Pattern Byte Mask Register #3

図 7-111. Receive Pattern Byte Mask Register #3 (RXPBM3)

15	14	13	12	11	10	9	8
Mask Bytes 32 to 47							
RW-0							
7	6	5	4	3	2	1	0
Mask Bytes 32 to 47							
RW-0							

表 7-121. RXPBM3 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Mask Bytes 32 to 47	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 32 to 47. For each byte '1' means it is masked.

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7.6.99 RXPBM4 Register 0x04CB – Receive Pattern Byte Mask Register #4

図 7-112. Receive Pattern Byte Mask Register #4 (RXPBM4)

15	14	13	12	11	10	9	8
Mask Bytes 48 to 63							
RW-0							
7	6	5	4	3	2	1	0
Mask Bytes 48 to 63							
RW-0							

表 7-122. RXPBM4 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:0	Mask Bytes 48 to 63	RW	0	**Pattern Byte Mask Configuration:** Configures masks for bytes 48 to 63. For each byte '1' means it is masked.

7.6.100 RXPATC Register 0x04CC – Receive Pattern Control Register

図 7-113. Receive Pattern Control Register (RXPATC)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
		Pattern Start Point					
		RW-0					

表 7-123. RXPATC Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6	Reserved	RO	0	Reserved
5:0	Pattern Start Point	RW	0	**Pattern Start Point:** Number of bytes after SFD where comparison begins on RX packets to the configured pattern. 00000 = Start compare on 1st byte after SFD 00001 = Start compare on 2nd byte after SFD … 01100 = Start compare on 13th byte (Default) Default setting is 0xC, which means the pattern comparision will begin after source and destination addresses since they are each 6 bytes.

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7.6.101 RXD3CLK Register 0x04E0 – RX_D3 Clock Control Register

図 7-114. RX_D3 Clock Control Register (RXD3CLK)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
					RX_D3 Clock Control		
					RW-Strap		

表 7-124. RXD3CLK Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:3	Reserved	RW	0	Reserved
2:0	RX_D3 Clock Control	RW	Strap	**RX_D3 Control:** 000 = RX_D3 operation 011 = 50MHz output clock (RMII Master mode)

7.6.102 LPS_CFG Register 0x04E5 – LPS Configuration Register

図 7-115. LPS Configuration Register (LPS_CFG)

15	14	13	12	11	10	9	8
Reserved						LPS Mode Selection	
RW-0000 00						RW-00	
7	6	5	4	3	2	1	0
Reserved							
RW-1100 0011							

表 7-125. LPS_CFG Register 0x04E5 – LPS Configuration Register

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:10	Reserved	RW	0000 00	Reserved
9:8	LPS Mode Selection	RW	00	**LPS Mode Selection:** 00 = Reserved 01 = Reserved 10 = Reserved 11 = Sdn[1] scrambled stream
7:0	Reserved	RW	1100 0011	Reserved

7.6.103

注

The following registers reside in the MMD1 register field. To access these registers, the DEVID must be 0x1.

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7.6.104 PMA_CTRL1 Register 0x0007 – MMD1 PMA Control Register #1

図 7-116. MMD1 PMA Control Register #1 (PMA_CTRL1)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
PMA / PMD Type							
RO-111101							

表 7-126. PMA_CTRL1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:6	Reserved	RO	0	Reserved
5:0	PMA / PMD Type	RO	111101	**100BASE-T1**

7.6.105 PMA_EXT1 Register 0x000B – MMD1 PMA Extended Ability Register #1

図 7-117. MMD1 PMA Extended Ability Register #1 (PMA_EXT1)

15	14	13	12	11	10	9	8
Reserved				100BASE-T1 Extended Abilities	PMA / PMD Type		
RO-0				RO-1	RO-0		
7	6	5	4	3	2	1	0
PMA / PMD Type							
RO-0							

表 7-127. PMA_EXT1 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12	Reserved	RO	0	Reserved
11	100BASE-T1 Extended Abilities	RO	1	**Extended Abilities:** 1 = PHY able to perform extended abilities listed in register 0x12 within MMD1 0 = PHY unable to perform extended abilities listed in register 0x12 within MMD1
10:0	PMA / PMD Type	RO	0	Reserved

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7.6.106 PMA_EXT2 Register 0x0012 – MMD1 PMA Extended Ability Register #2

図 7-118. MMD1 PMA Extended Ability Register #2 (PMA_EXT2)

15	14	13	12	11	10	9	8
Reserved							
RO-0							
7	6	5	4	3	2	1	0
							Ability
							RO-1

表 7-128. PMA_EXT2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:1	Reserved	RO	0	Reserved
0	100BASE-T1 Ability	RO	1	**100BASE-T1 Ability:** 1 = PHY supports 100BASE-T1 0 = PHY does not support 100BASE-T1

7.6.107 PMA_CTRL2 Register 0x0834 – MMD1 PMA Control Register #2

図 7-119. MMD1 PMA Control Register #2 (PMA_CTRL2)

15	14	13	12	11	10	9	8
Reserved	Master / Slave	**Reserved**					
RO-1	RW/Strap	RO-0					
7	6	5	4	3	2	1	0
Reserved							
RO-0							

表 7-129. PMA_CTRL2 Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15	Reserved	RO	1	Reserved
14	100BASE-T1 Master / 100BASE-T1 Slave Configuration	RW	Strap	**100BASE-T1 Master / 100BASE-T1 Slave Configuration:** 1 = PHY configured as a 100BASE-T1 Master 0 = PHY configured as a 100BASE-T1 Slave
13:0	Reserved	RO	0	Reserved

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7.6.108 TEST_CTRL Register 0x0836 – MMD1 100BASE-T1 PMA Test Control Register

図 7-120. MMD1 100BASE-T1 PMA Test Control Register (TEST_CTRL)

15	14	13	12	11	10	9	8
100BASE-T1 Test Modes				**Reserved**			
RW/Strap-0000				RO-0000 0000 0001			
7	6	5	4	3	2	1	0

表 7-130. TEST_CTRL Field Descriptions

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
15:12	100BASE-T1 Test Modes	RW	Strap	**100BASE-T1 Test Mode Control:** 0000 = Normal operation 0010 = Test Mode 1 0100 = Test Mode 2 1000 = Test Mode 4 1010 = Test Mode 5
11:0	Reserved	RO	0000 0000 0001	Reserved

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DP83TC811-Q1 is a single-port 100Mbps Automotive Ethernet PHY. It supports IEEE 802.3bw and allows for connections to an Ethernet MAC through MII, RMII, RGMII, or SGMII. When using the device for Ethernet applications, it is necessary to meet certain requirements for normal operation. The following subsections are intended to assist in appropriate component selection and required connections.

8.2 Typical Applications

図 8-1 through 図 8-5 show some the typical applications for the DP83TC811-Q1.

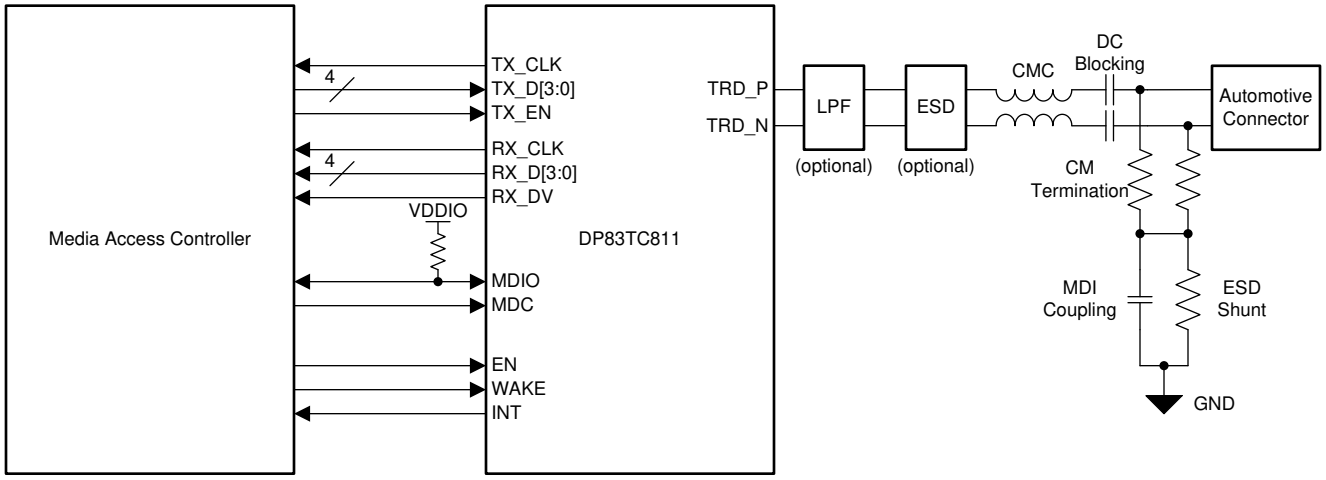


図 8-1. Typical Application (MII)

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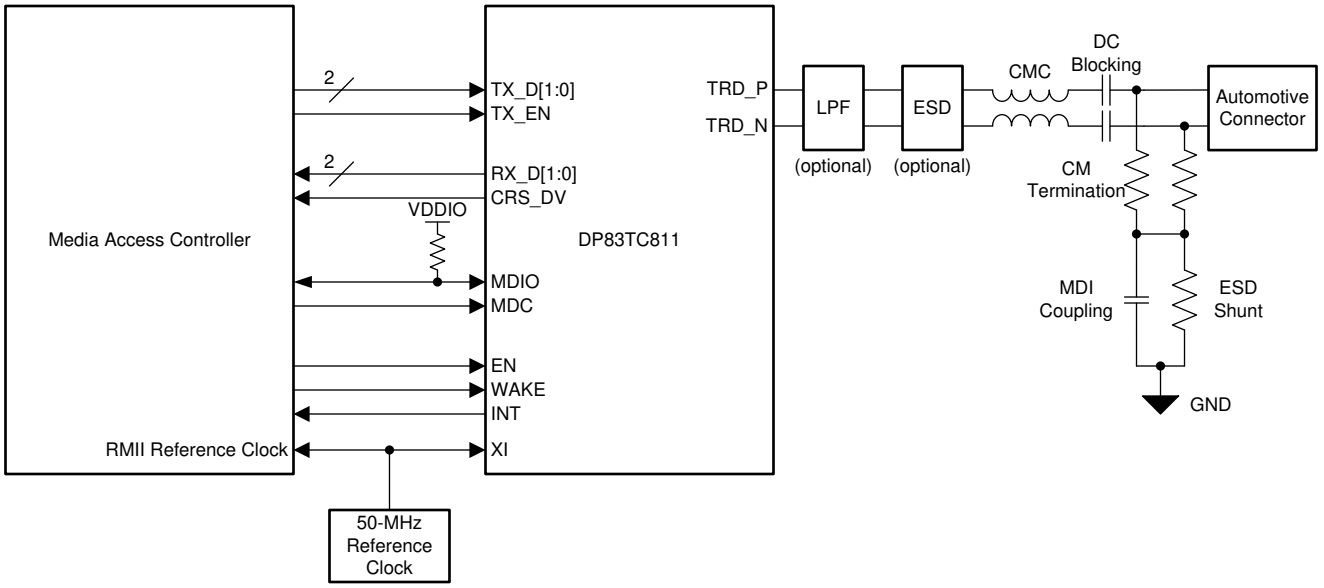


図 8-2. Typical Application (RMII Slave)

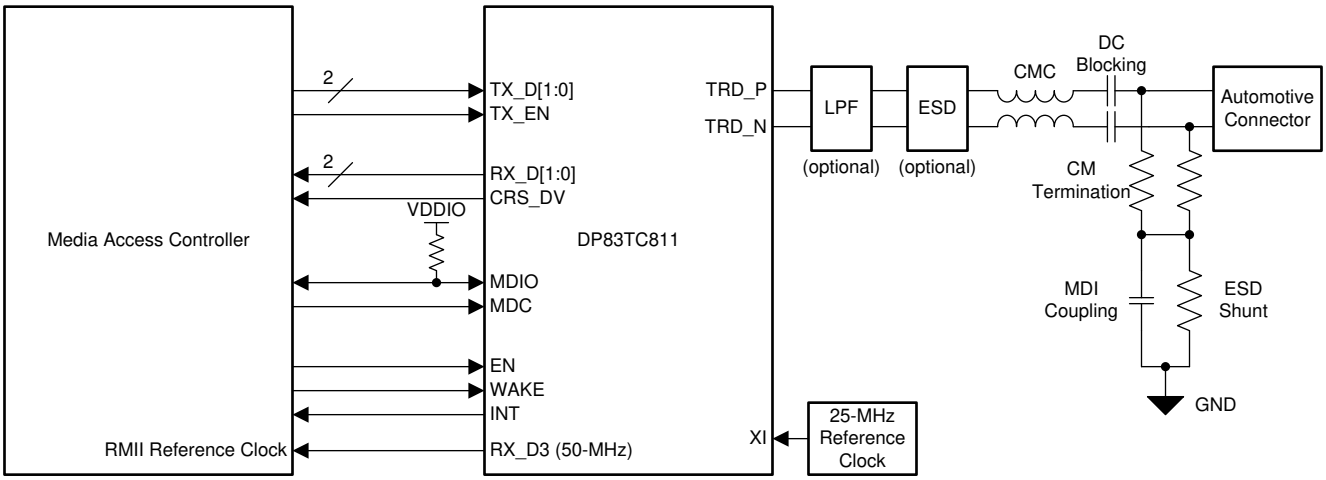


図 8-3. Typical Application (RMII Master)

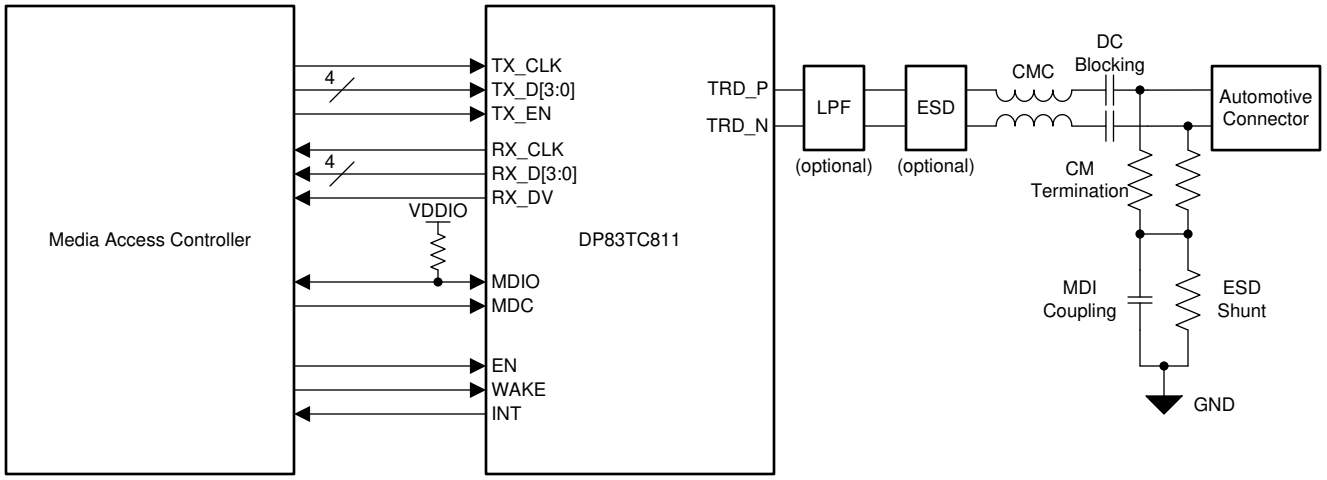


図 8-4. Typical Application (RGMII)

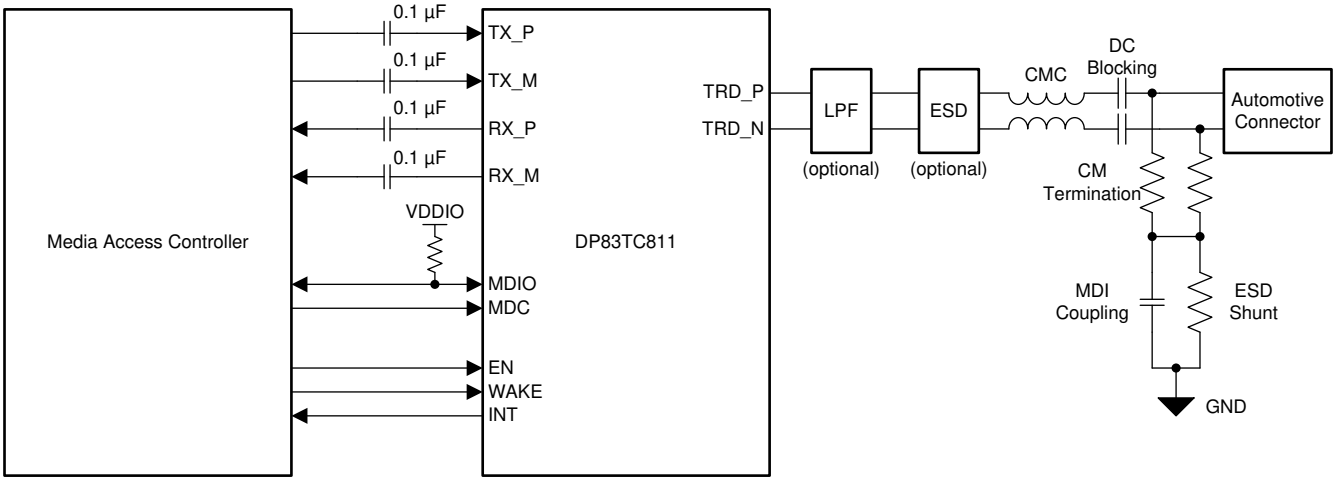


図 8-5. Typical Application (SGMII)

An optional external low-pass filter may be added to reduce radiated emissions and improve radiated immunity. Suggested values are located in 表 8-1.

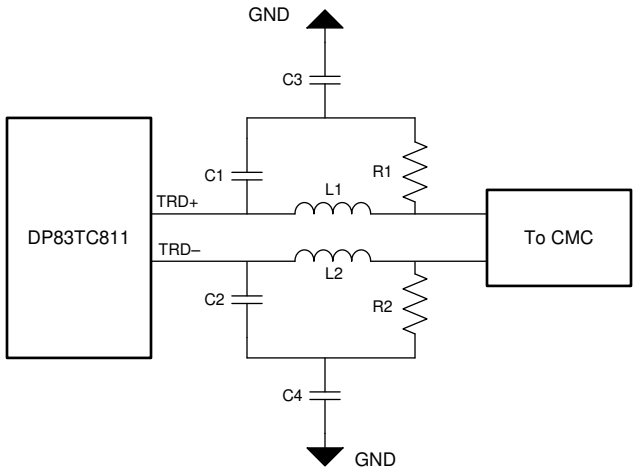


図 8-6. MDI Low-Pass Filter [1] [2]

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8.2.1 Design Requirements

For these typical applications, use the following as design parameters:

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{DDIO}	1.8V, 2.5V, 3.3V
V_{DDA}	3.3V
Decoupling capacitors V_{DDIO} (3)	10nF, 100nF, 1µF, 10µF
(Optional) ferrite bead for V_{DDIO}	1kΩ at 100MHz (BLM18AG102SH)
Decoupling capacitors V_{DDA} (3)	10nF, 100nF, 1µF, 10µF
(Optional) ferrite bead for V_{DDA}	1kΩ at 100MHz (BLM18AG102SH)
DC Blocking Capacitors (3)	0.1µF
Common-Mode Choke	200µH
Common Mode Termination Resistors(1)	1kΩ
MDI Coupling Capacitor (3)	4.7nF
ESD Shunt(3)	100kΩ
(Optional) MDI Low-Pass Filter(2)	120nH (L1 and L2), 47pF (C3 and C4), 22pF (C1 and C2), 27Ω (R1 and R2)
Reference Clock	25MHz

(1) 1% tolerance components are recommended.
(2) 2% tolerance components are recommended.
(3) 10% tolerance components are recommended.

8.2.1.1 Physical Medium Attachment

There must be no metal running beneath the common-mode choke. CMCs can inject noise into metal beneath them, which can affect the emissions and immunity performance of the system. Because the DP83TC811-Q1 is a voltage mode line driver, no external termination resistors are required. The ESD shunt and MDI coupling capacitor should be connected to ground. Ensure that the common mode termination resistors are 1% tolerance or better to improve differential coupling.

8.2.1.1.1 Common-Mode Choke Recommendations

The following CMCs have been tested with the DP83TC811-Q1:

表 8-2. Recommended CMCs

MANUFACTURER	PART NUMBER
Pulse Electronics	AE2002
Murata	DLW43MH201XK2L
Murata	DLW32MH201XK2
TDK	ACT45L-201
TDK	ACT1210L-201

表 8-3. CMC Electrical Specifications

PARAMETER	TYP	UNITS	CONDITIONS
Insertion Loss	–0.5	dB	1 – 30MHz
	–1.0	dB	30 – 60MHz
Return Loss	–26	dB	1 – 30MHz
	–20	dB	30 – 60MHz

[1] MDI low-pass filter is required to pass emissions and immunity testing per OPEN Alliance IEEE 100BASE-T1 EMC Test Specifications for Transceivers version 1.0.
[2] Please see SNLA293 application note for specific register configurations concerning OPEN Alliance IOP and EMC testing.

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表 8-3. CMC Electrical Specifications (続き)

PARAMETER	TYP	UNITS	CONDITIONS
Common-Mode Rejection	–24	dB	1MHz
	–42	dB	10 – 100MHz
	–25	dB	400MHz
Differential Common-Mode Rejection	–70	dB	1 – 10MHz
	–50	dB	100MHz
	–24	dB	1000MHz

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8.2.2 Detailed Design Procedure

When creating a new system design with an Ethernet PHY, follow this schematic capture procedure:

1. Select desired PHY hardware configurations in 表 7-17.
2. Use the *セクション 6.5* table and 表 7-16 to select the correct external bootstrap resistors.
3. If using LEDs, make sure the correct external circuit is applied as shown in 図 7-15.
4. Select an appropriate clock source that adheres to either the CMOS-level oscillator or crystal resonator requirements within the *セクション 6.5* table.
5. Select a CMC, a list of recommended CMCs are located in 表 8-2.
6. Add common-mode termination, DC-blocking capacitors, an MDI-coupling capacitor, and an ESD shunt found in 表 8-1.
7. Make sure that there is sufficient supply decoupling on VDDIO and VDDA supply pins.
8. Add an external pullup resistor (tie to VDDIO) on MDIO line.
9. If operating with SGMII, place 0.1µF, DC-blocking capacitors between the MAC and PHY SGMII pins.
10. If sleep modes are not desired, WAKE and EN pins must be tied to VDDIO directly or through an external pullup resistor.

The following layout procedure needs to be followed:

1. Locate the PHY near the edge of the board so that short MDI traces can be routed to the desired connector.
2. Place the MDI external components: CMC, DC-blocking capacitors, CM termination, MDI-coupling capacitor, and ESD shunt.
3. Create a top-layer metal pour keepout under the CMC.
4. Make sure that the MDI TRD_M and TRD_P traces are routed so that they are 100Ω differential.
5. Place the clock source near the XI and XO pins.
6. Make sure that when configured for MII, RMII, or RGMII operation, the xMII pins are routed 50Ω and are single-ended with reference to ground.
7. Make sure that transmit path xMII pins are routed such that setup and hold timing does not violate the PHY requirements.
8. Make sure that receive path xMII pins are routed such that setup and hold timing does not violate the MAC requirements.
9. Make sure that when configured for SGMII operation, the xMII RX_P, RX_M, TX_P, and TX_M pins are routed 100Ω differential.
10. Place the MDIO pullup close to the PHY.

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8.2.3 Application Curves

The following curves were obtained using the DP83TC811EVM under nominal conditions.

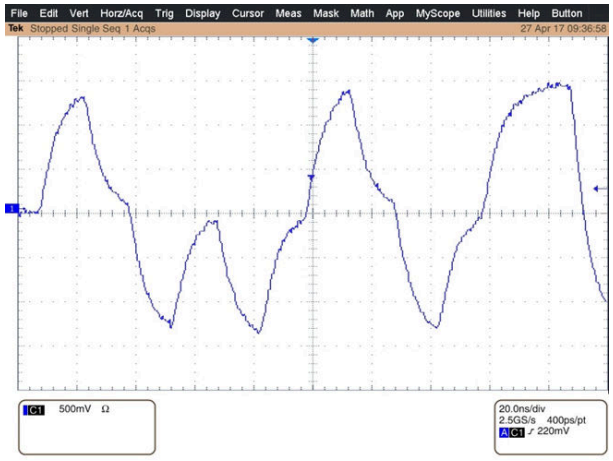


図 8-7. MDI IDLE Stream

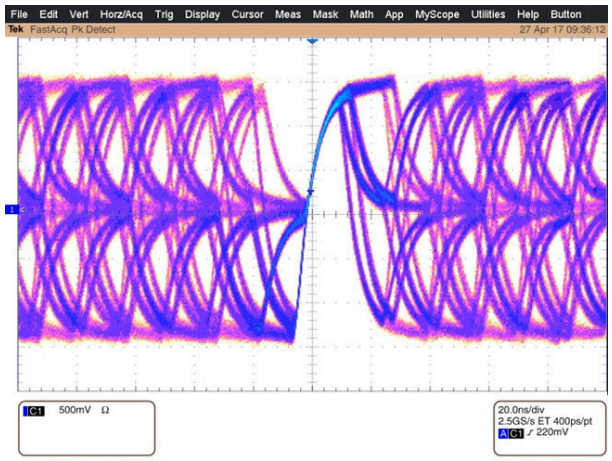


図 8-8. MDI IDLE Stream (Variable Persistence)

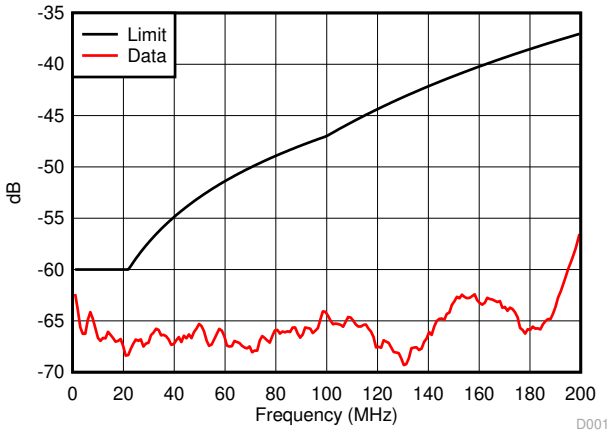


図 8-9. MDI Mode Conversion

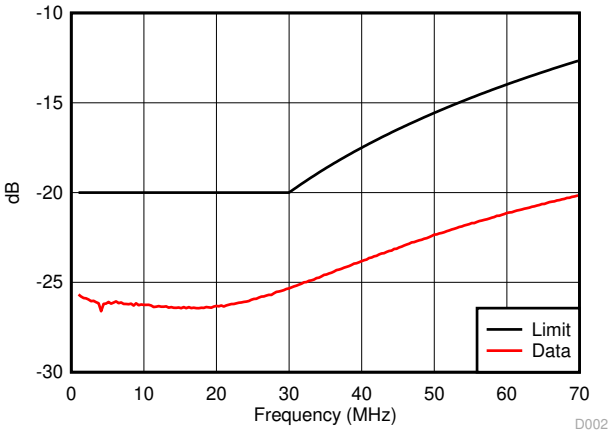


図 8-10. MDI Return Loss

8.3 Layout

8.3.1 Layout Guidelines

8.3.1.1 Signal Traces

PCB traces are lossy and long traces can degrade signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces must be 50Ω, single-ended impedance. Differential traces must be 50Ω single-ended and 100Ω differential. Make sure impedance is controlled throughout. Impedance discontinuities causes reflections leading to emissions and signal integrity issues. Stubs must be avoided on all signal traces, especially differential signal pairs.

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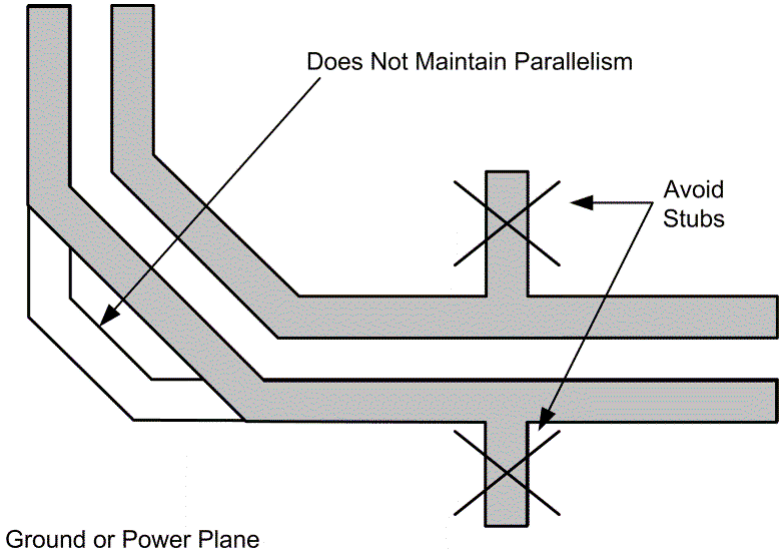


図 8-11. Differential Signal Trace Routing

Within the differential pairs, trace lengths must be run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common mode noise and emissions. Length matching is also important for MAC interface connections. All transmit signal traces must be length matched to each other and all receive signal traces must be length matched to each other.

There must not be crossover or vias on signal path traces. Vias present impedance discontinuities and must be minimized when possible. Route trace pairs on the same layer. Signals on different layers must not cross each other without at least one return path plane between them. Differential pairs must always have a constant coupling distance between them. For convenience and efficiency, TI recommends routing critical signals first (that is, MDI differential pairs, reference clock, and MAC IF traces).

8.3.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path between the signal traces should be avoided at all cost. A signal crossing a split plane may cause unpredictable return path currents and could impact signal quality and result in emissions issues.

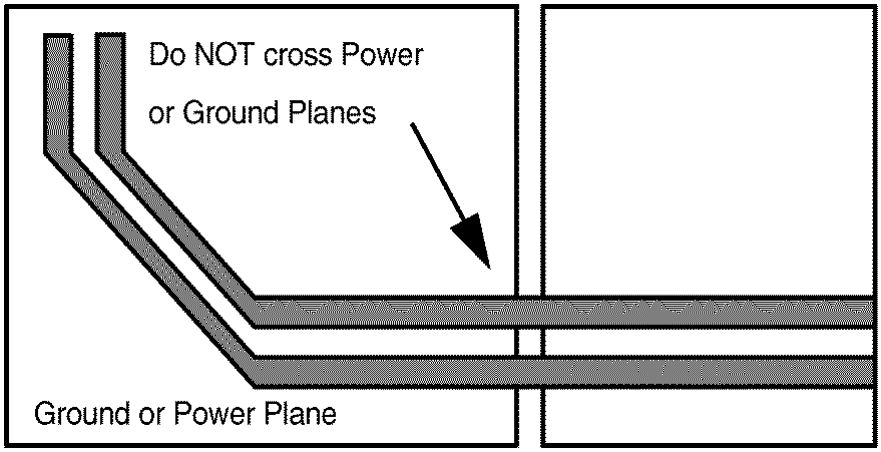


図 8-12. Power and Ground Plane Breaks

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8.3.1.3 Metal Pour

All metal pours that are not signals or power must be tied to ground. There must be no floating metal in the system, and there must be no metal between differential traces.

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8.3.1.4 PCB Layer Stacking

To meet signal integrity and performance requirements, minimum four-layer PCB is recommended. However, a six-layer PCB and above should be used when possible.

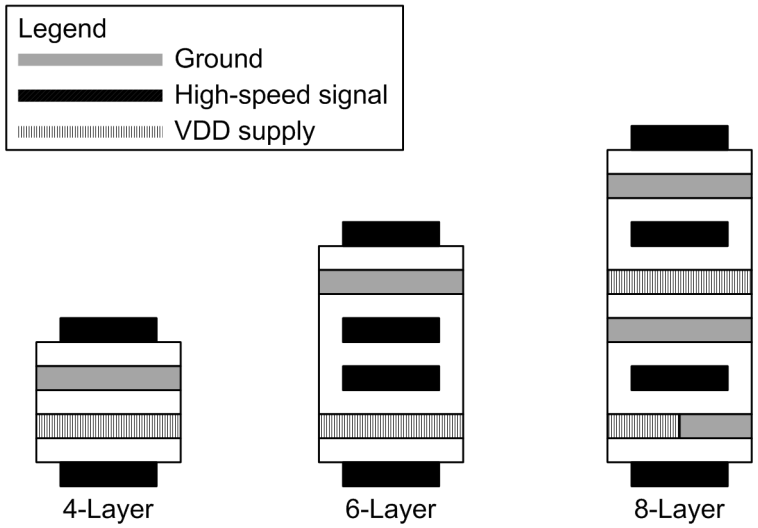


図 8-13. Recommended PCB Layer Stack-Up

8.3.2 Layout Example

The figures below show the recommendations of the layout of power and sensitive signals of DP83TC811-Q1.

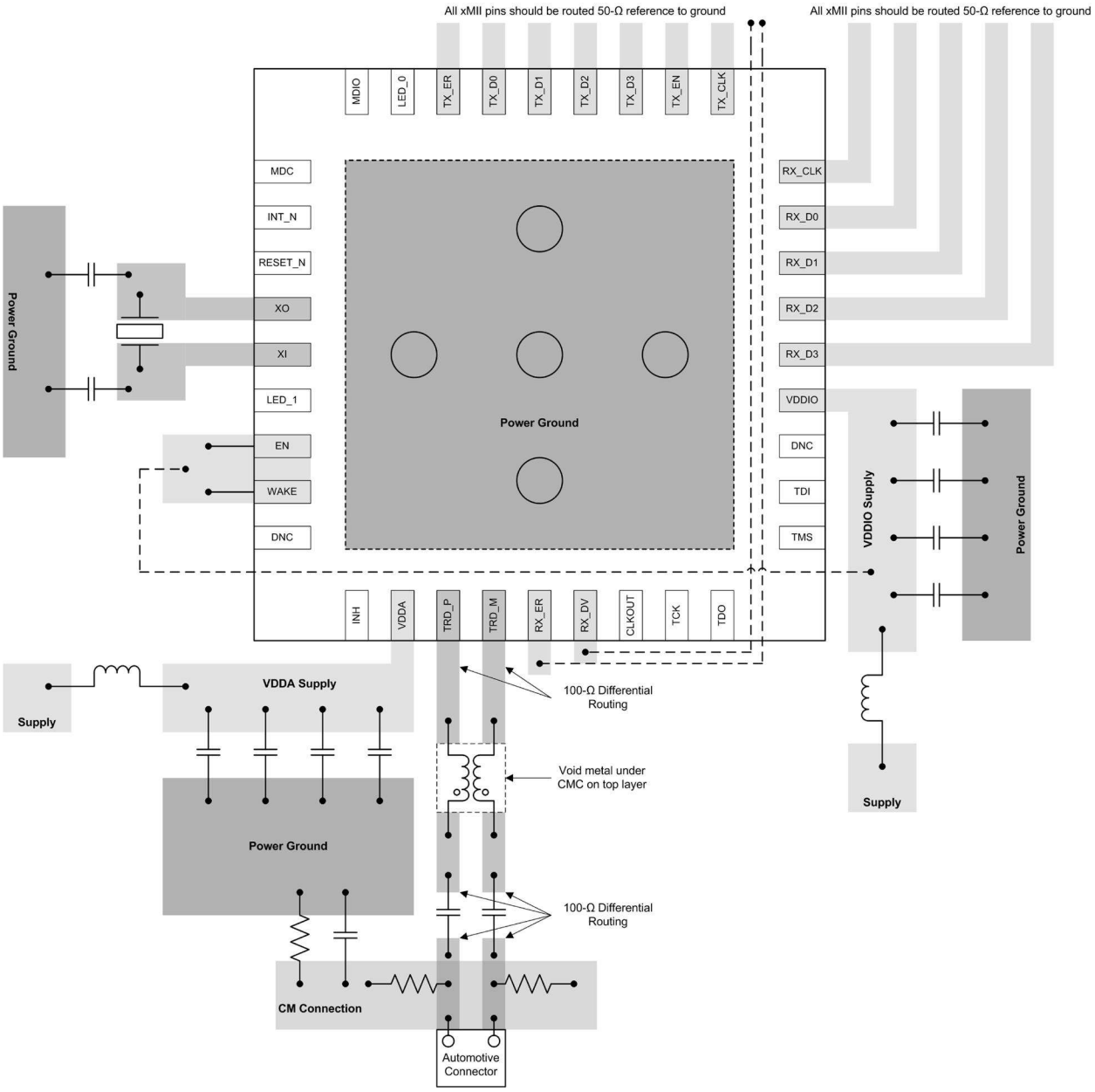


図 8-14. DP83TC811-Q1 MII / RMII / RGMII Layout Recommendation

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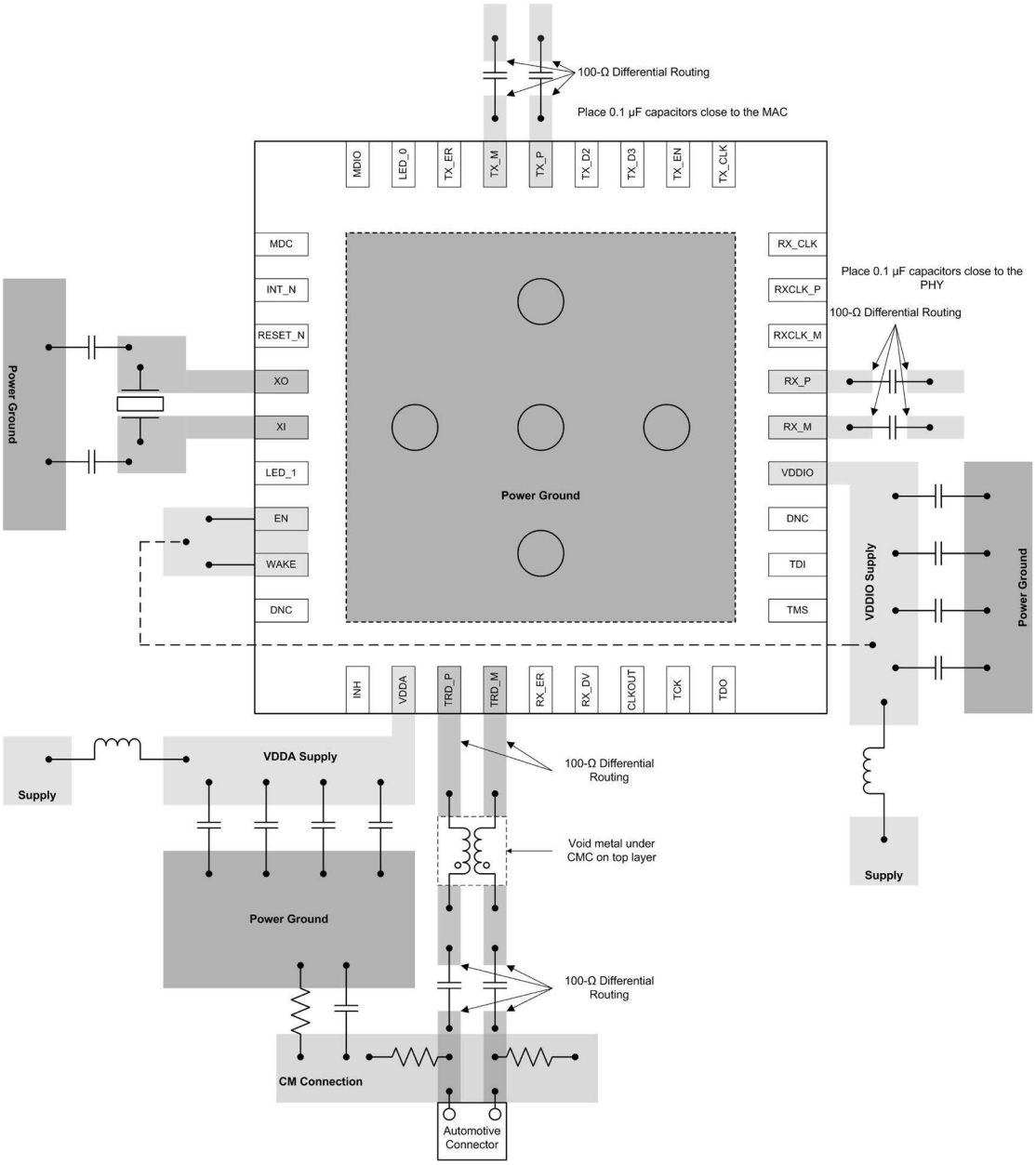


図 8-15. DP83TC811SWRHA-Q1 SGMII Layout Recommendation

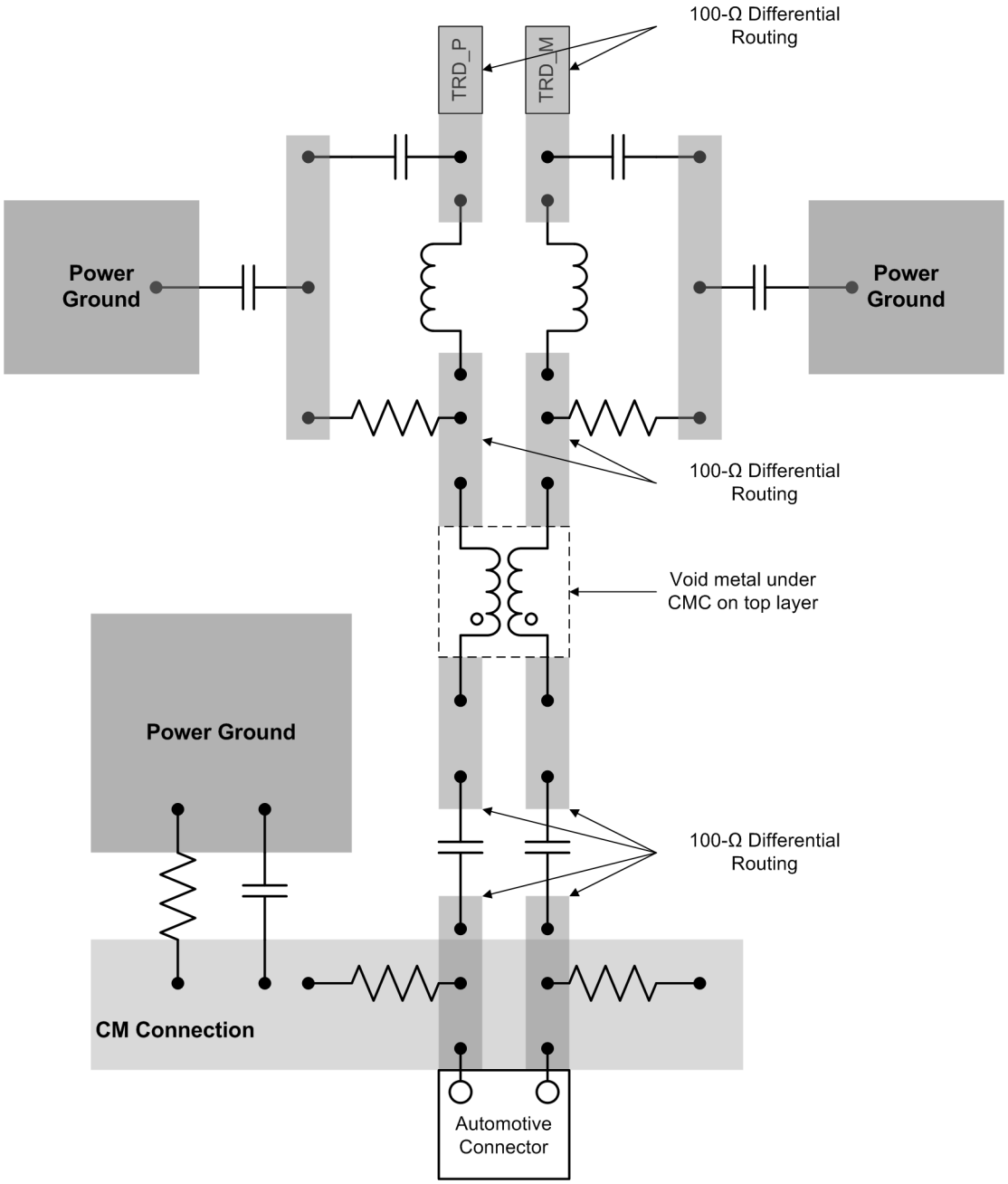
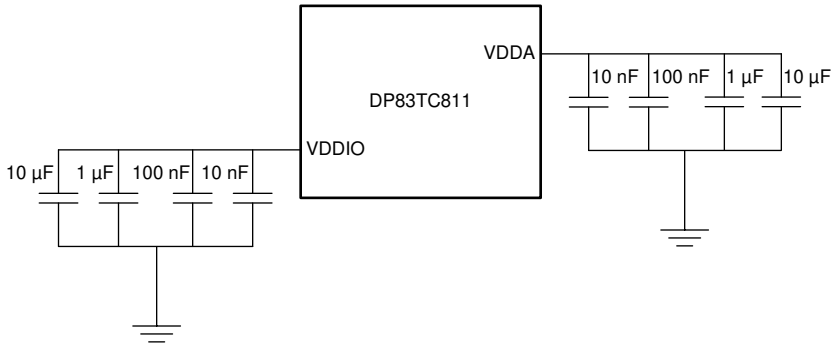


図 8-16. MDI Low-Pass Filter Layout Recommendation

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8.4 Power Supply Recommendations

The DP83TC811-Q1 is capable of operating with a wide range of IO supply voltages (3.3V, 2.5V, or 1.8V). No power supply sequencing is required. The recommended power supply de-coupling network is shown in 図 8-17. For improved conducted emissions, an optional ferrite bead can be placed between the supply and the PHY de-coupling network.



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図 8-17. Recommended Supply De-Coupling Network

9 Device and Documentation Support

注

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2023) to Revision A (January 2024)	Page
• ドキュメント全体を通して 2.5V、3.3V VDDIO のサポートを追加	1
• Updated Recommended Operating Conditions Table	9
• Added Electrical Characteristics corresponding to 2.5V, 3.3V VDDIO	9

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DP83TC811RWRHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811RWRHARQ1.A	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811RWRHARQ1.B	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811RWRHATQ1	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811RWRHATQ1.A	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811RWRHATQ1.B	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811R
DP83TC811SWRHARQ1	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811S
DP83TC811SWRHARQ1.A	Active	Production	VQFN (RHA) | 36	2500 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811S
DP83TC811SWRHATQ1	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811S
DP83TC811SWRHATQ1.A	Active	Production	VQFN (RHA) | 36	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	811S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

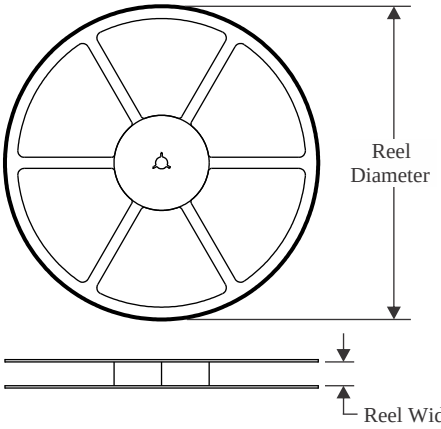
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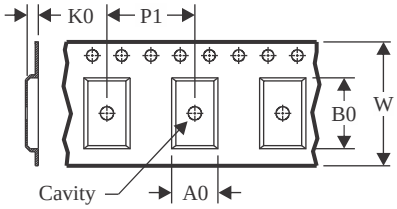
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

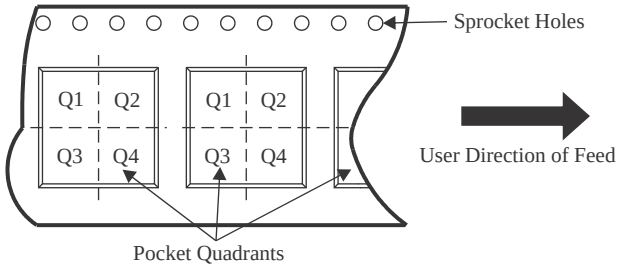


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

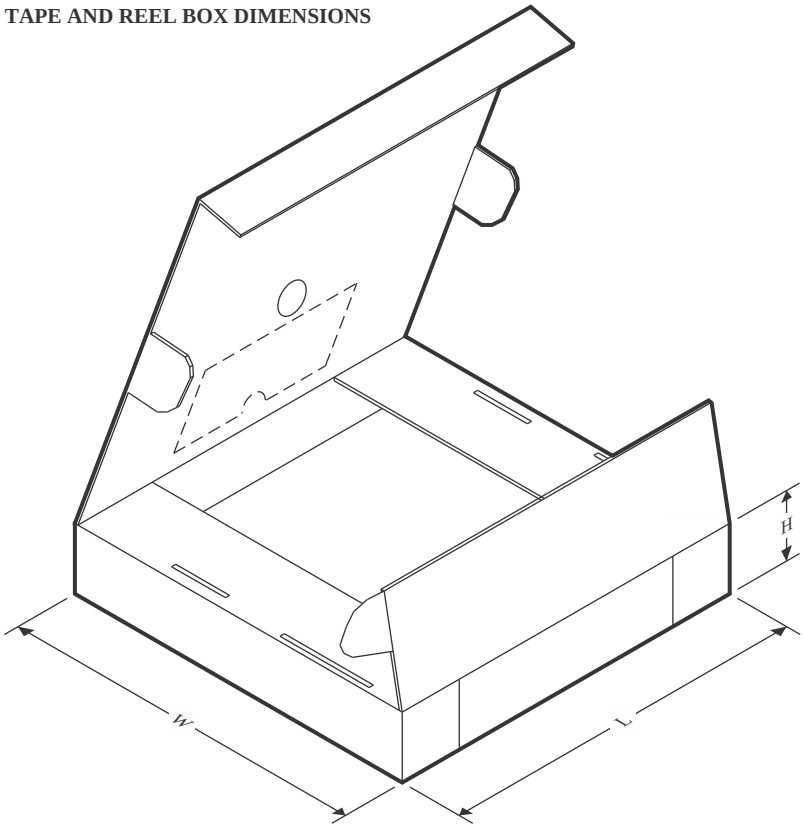
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83TC811RWRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811RWRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811RWRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811RWRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811SWRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811SWRHARQ1	VQFN	RHA	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811SWRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
DP83TC811SWRHATQ1	VQFN	RHA	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83TC811RWRHARQ1	VQFN	RHA	36	2500	367.0	367.0	38.0
DP83TC811RWRHARQ1	VQFN	RHA	36	2500	360.0	360.0	36.0
DP83TC811RWRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0
DP83TC811RWRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0
DP83TC811SWRHARQ1	VQFN	RHA	36	2500	367.0	367.0	35.0
DP83TC811SWRHARQ1	VQFN	RHA	36	2500	367.0	367.0	38.0
DP83TC811SWRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0
DP83TC811SWRHATQ1	VQFN	RHA	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

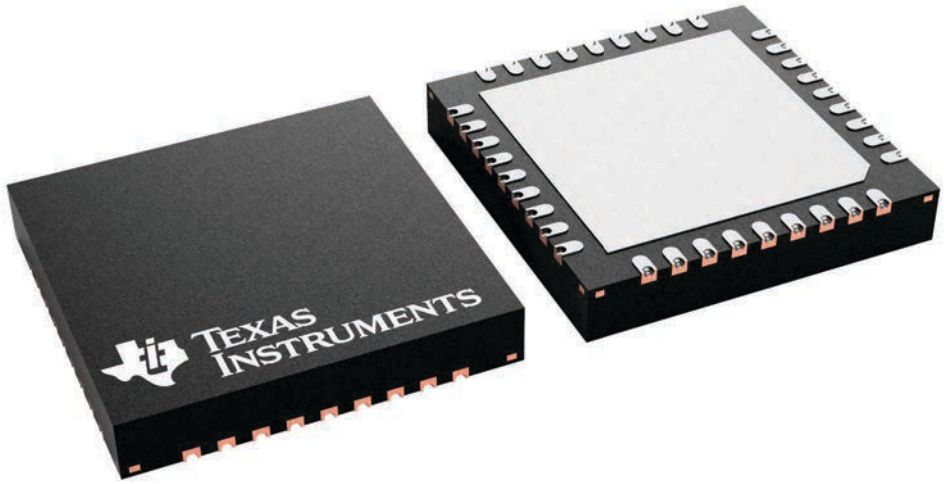
RHA 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



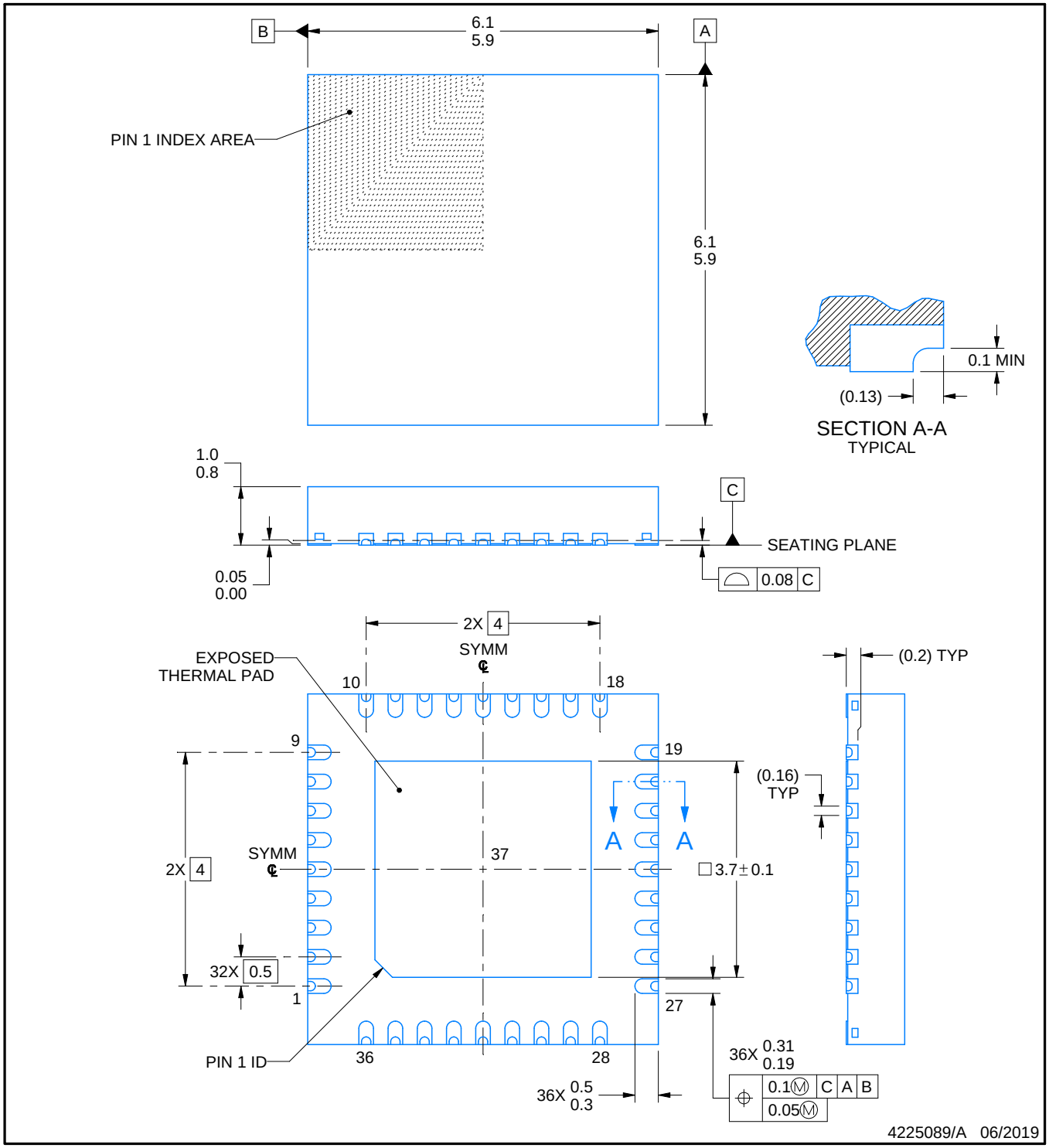
4228438/A

PACKAGE OUTLINE

RHA0036A

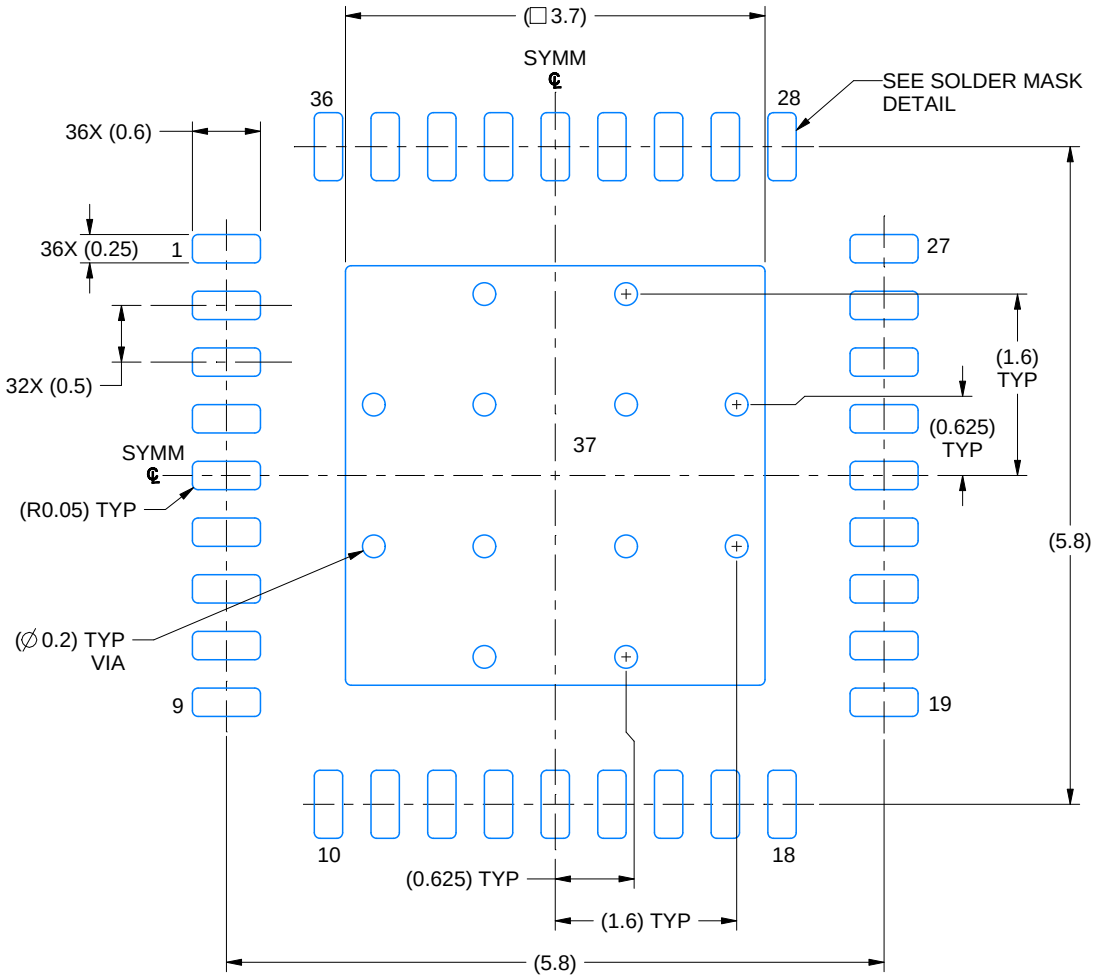
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

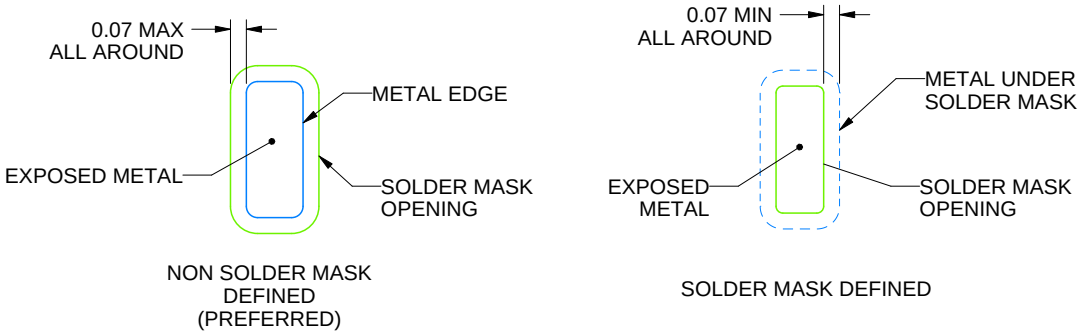


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

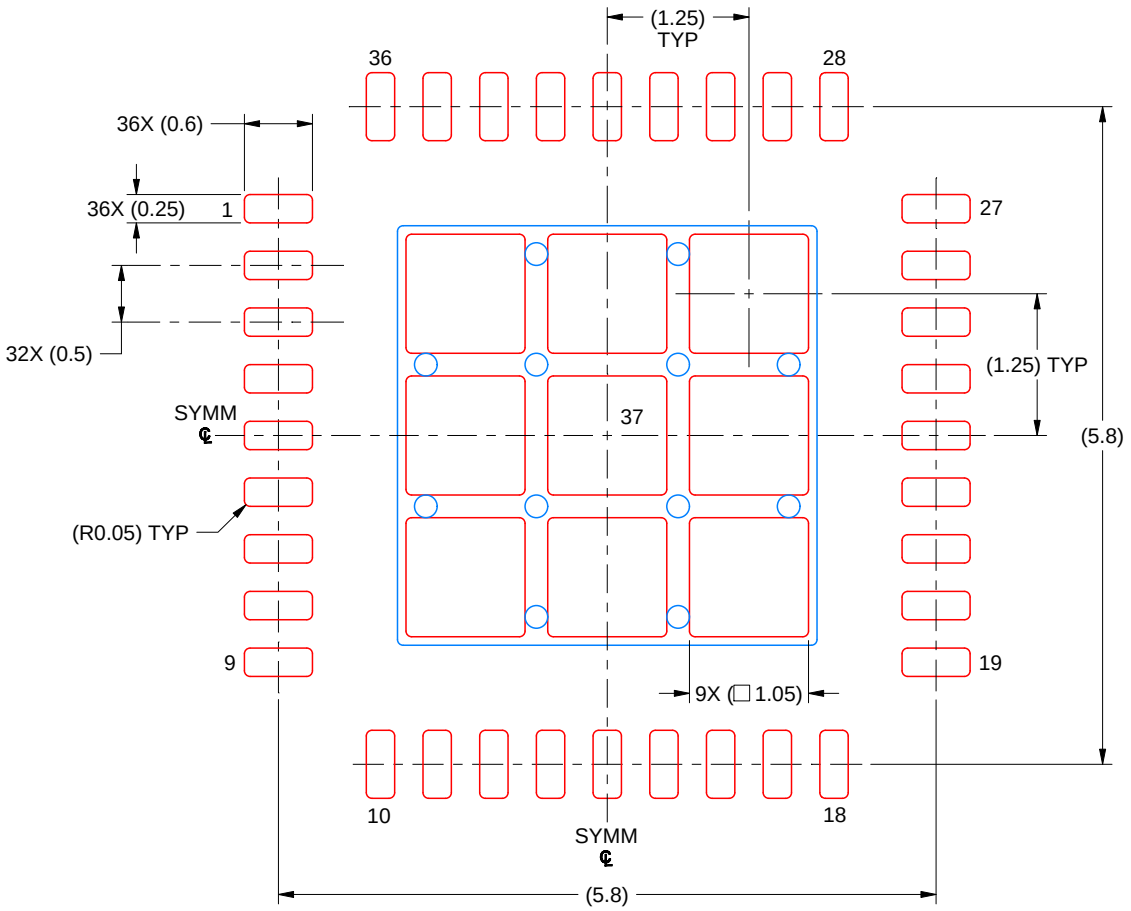


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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