DRV5053-Q1 車載用アナログ・バイポーラ、ホール効果センサ

1 特長

- 線形出力ホール・センサ
- 車載アプリケーション用にAEC-Q100認定済み
  - グレード1: T_A = -40℃～125℃ (Q、図17を参照)
  - グレード0: T_A = -40℃～150℃ (E、図17を参照)
- 優れた温度安定性
  - 温度範囲の全体で感度±10%
- 高感度オプション
  - -11mV/mT (OA、図17を参照)
  - -23mV/mT (PA)
  - -45mV/mT (RA)
  - -90mV/mT (VA)
  - +23mV/mT (CA)
  - +45mV/mT (EA)
- 広い範囲の電圧をサポート
  - 2.7～38V
  - 外部レギュレータ不要
- 出力段の増幅
  - 2.3mAシンク、300µAソース
- 出力電圧: 0.2～1.8V
  - B = 0mT、OUT = 1V
- 高速パワーオン: 35µs
- 小さなパッケージと占有面積
  - 表面実装の3ピンSOT-23 (DBZ)
    - 2.92mm×2.37mm
  - スルーホールの3ピンTO-92 (LPG)
    - 4.00mm×3.15mm
- 保護機能
  - 逆電圧保護(最大-22V)
  - 40Vまでの負荷ダンプをサポート
  - 出力短絡保護
  - 出力電流制限
  - OUTからバッテリへの短絡保護

2 アプリケーション

- 流量計
- ドッキング調整
- 振動補正
- ダンパー制御

3 概要

DRV5053-Q1デバイスはチョッパ安定化されたホールICで、全温度範囲で優れた感度安定性を持ち、保護機能が内蔵された磁気センシング・ソリューションです。

0～2Vのアナログ出力は、印加された磁束密度に対して線形的に応答し、磁界方向の極性を区別します。このデバイスは2.7～38Vの広い動作電圧範囲と、-22Vまでの逆極性保護を持つため、広範な車載用および民生用アプリケーションに適しています。

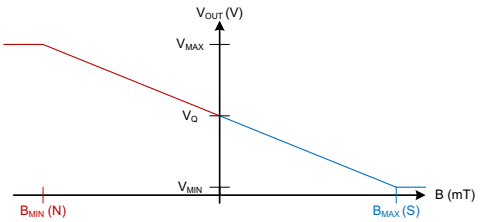
逆電圧の状態、負荷ダンプ、および出力短絡や過電流に対して、内部的な保護機能が搭載されています。

製品情報(1)

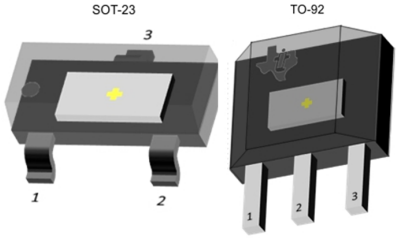
型番	パッケージ	本体サイズ(公称)
DRV5053-Q1	SOT-23 (3)	2.92mm×1.30mm
	TO-92 (3)	4.00mm×3.15mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

出力状態



デバイスのパッケージ



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4 改訂履歴

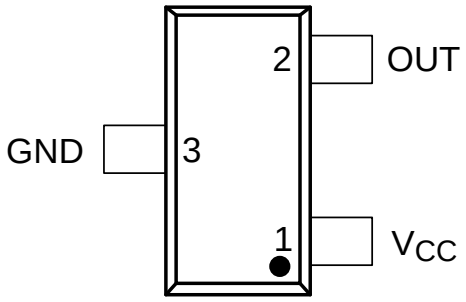
2014年12月発行のものから更新 **Page**

- SOT-23パッケージの本体サイズを訂正し、SIPパッケージ名をTO-92に訂正 ... 1
- Added B_{MAX} to *Absolute Maximum Ratings* ... 4
- Removed table notes regarding testing for the operating junction temperature in *Absolute Maximum Ratings* ... 4
- Updated the typical value for B_N and V_N for each version ... 5
- Updated Figure 6 ... 7
- Updated the *Functional Block Diagram* ... 8
- Updated *Output Stage* ... 11
- パッケージのテープ&リールに関するMとブランクのオプションを更新 ... 15
- コミュニティ・リソースを追加 ... 16

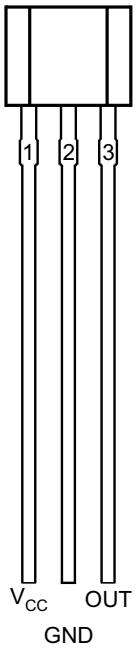
5 Pin Configuration and Functions

For additional configuration information, see デバイスのマーキング and メカニカル、パッケージ、および注文情報.

DBZ Package
3-Pin SOT-23
Top View



LPG Package
3-Pin TO-92
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	DBZ	LPG		
GND	3	2	GND	Ground pin
V_{CC}	1	1	Power	2.7 to 38 V power supply. Bypass this pin to the GND pin with a 0.01-μF (minimum) ceramic capacitor rated for V_{CC}.
OUT	2	3	Output	Hall sensor analog output. 1 V output corresponds to B = 0 mT

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22(2)	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output pin voltage		–0.5	2.5	V
Output pin reverse current during reverse supply condition		0	–20	mA
Magnetic flux density, B_{MAX}		Unlimited		
Operating junction temperature, T_J	Q, see 図 17	–40	150	°C
	E, see 図 17	–40	175	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Power supply voltage		2.7	38	V
V_{OUT}	Output pin voltage (OUT)		0	2	V
I_{SOURCE}	Output pin current source (OUT)		0	300	µA
I_{SINK}	Output pin current sink (OUT)		0	2.3	mA
T_A	Operating ambient temperature	Q, see 図 17	–40	125	°C
		E, see 図 17	–40	150	

6.4 Thermal Information

THERMAL METRIC(1)		DRV5053-Q1		UNIT
		DBZ (SOT-23)	LPG (TO-92)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	°C/W
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.7		38	V
I_{CC}	Operating supply current	V_{CC} = 2.7 to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.7 to 38 V, T_A = $T_{A, MAX}$ (1)		3	3.6	
t_{on}	Power-on time			35	50	µs
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
$I_{OCP,SOURCE}$	Overcurrent protection level	Sourcing current		300		µA
$I_{OCP,SINK}$	Overcurrent protection level	Sinking current		2.3		mA

(1) $T_{A, MAX}$ is 125°C for Q Grade 1 devices and 150°C for E Grade 0 devices (see 図 17)

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT (OUT)						
t_d	Output delay time	T_A = 25°C		13	25	µs

6.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT (1)
V_Q	Quiescent output	B = 0 mT	0.9	1.02	1.15	V
f_{BW}	Bandwidth (2)		20			kHz
B_N	Input-referred noise (3)	C_{OUT} = 50 pF	0.40	0.49	0.79	mT_{pp}
Le	Linearity (4)	$–B_{SAT}$ < B < B_{SAT}		1%		
$V_{OUT\ MIN}$	Output saturation voltage (min)	B < $–B_{SAT}$			0.2	V
$V_{OUT\ MAX}$	Output saturation voltage (max)	B > B_{SAT}	1.8			V
DRV5053OA: –11 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	–17.5	–11	–5	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		5		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		73		mT
DRV5053PA: –23 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	–35	–23	–10	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		11		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		35		mT

(1) 1 mT = 10 Gauss
(2) Bandwidth describes the fastest changing magnetic field that can be detected and translated to the output.
(3) Not tested in production; limits are based on characterization data.
(4) Linearity describes the change in sensitivity across the B-range. The sensitivity near B_{SAT} is typically within 1% of the sensitivity near B = 0.

Magnetic Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
DRV5053RA: –45 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	–70	–45	–20	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		22		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		18		mT
DRV5053VA: –90 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	–140	–90	–45	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		44		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		9		mT
DRV5053CA: 23 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	10	23	35	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		11		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		35		mT
DRV5053EA: 45 mV/mT						
S	Sensitivity	V_{CC} = 3.3 V	20	45	70	mV/mT
V_N	Output-referred noise	V_{CC} = 3.3 V; R_{OUT} = 10 kΩ; C_{OUT} = 50 pF		22		mV_{pp}
B_{SAT}	Input saturation field	V_{CC} = 3.3 V		18		mT

6.8 Typical Characteristics

T_A > 125°C data is valid for Grade 0 devices only (E, see 図 17)

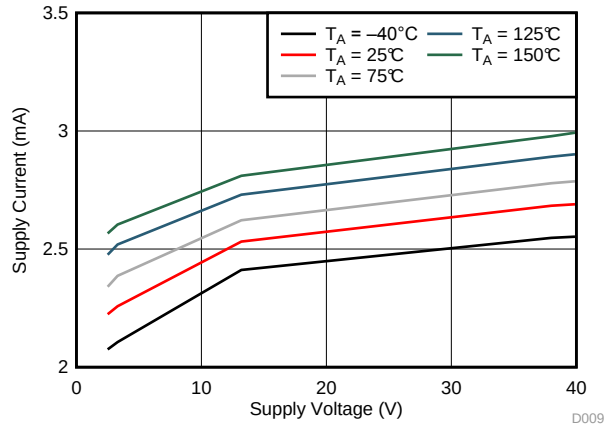


Figure 1. I_{CC} vs V_{CC}

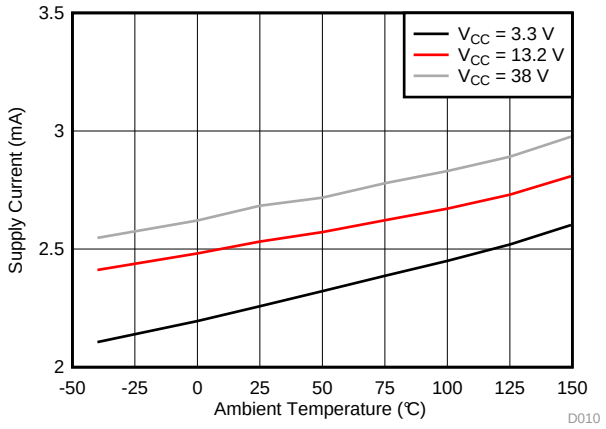
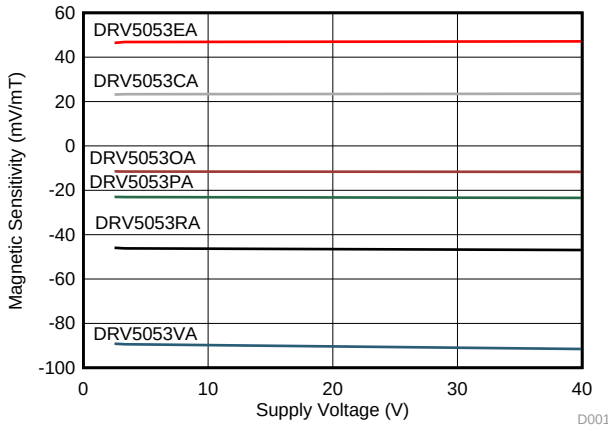
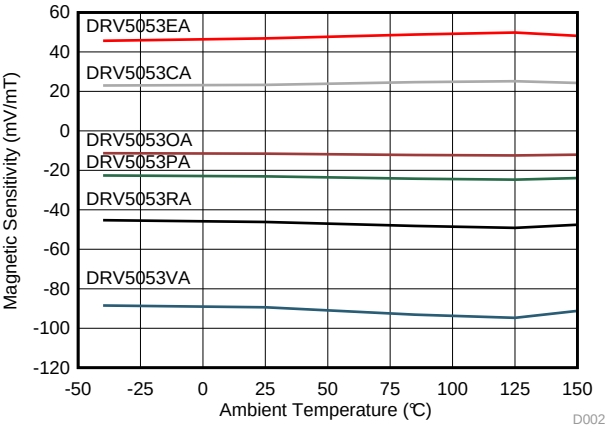


Figure 2. I_{CC} vs Temperature



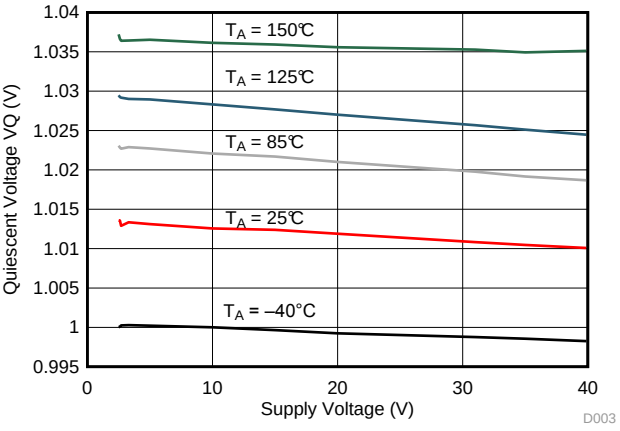
T_A = 25°C

Figure 3. Sensitivity vs V_{CC}



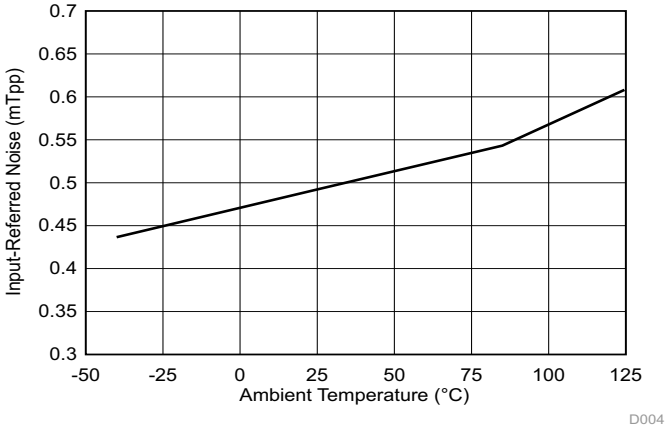
V_{CC} = 3.3 V

Figure 4. Sensitivity vs Temperature



T_A = 25°C

Figure 5. V_Q vs V_{CC}



V_{CC} = 3.3 V

Figure 6. B_N vs Temperature

7 Detailed Description

7.1 Overview

The DRV5053-Q1 device is a chopper-stabilized Hall sensor with an analog output for magnetic sensing applications. The DRV5053-Q1 device can be powered with a supply voltage between 2.7 and 38 V, and will survive –22 V reverse battery conditions continuously. Note that the DRV5053-Q1 device will not be operating when approximately –22 to 2.4 V is applied to V_{CC} (with respect to GND). In addition, the device can withstand supply voltages up to 40 V for transient durations.

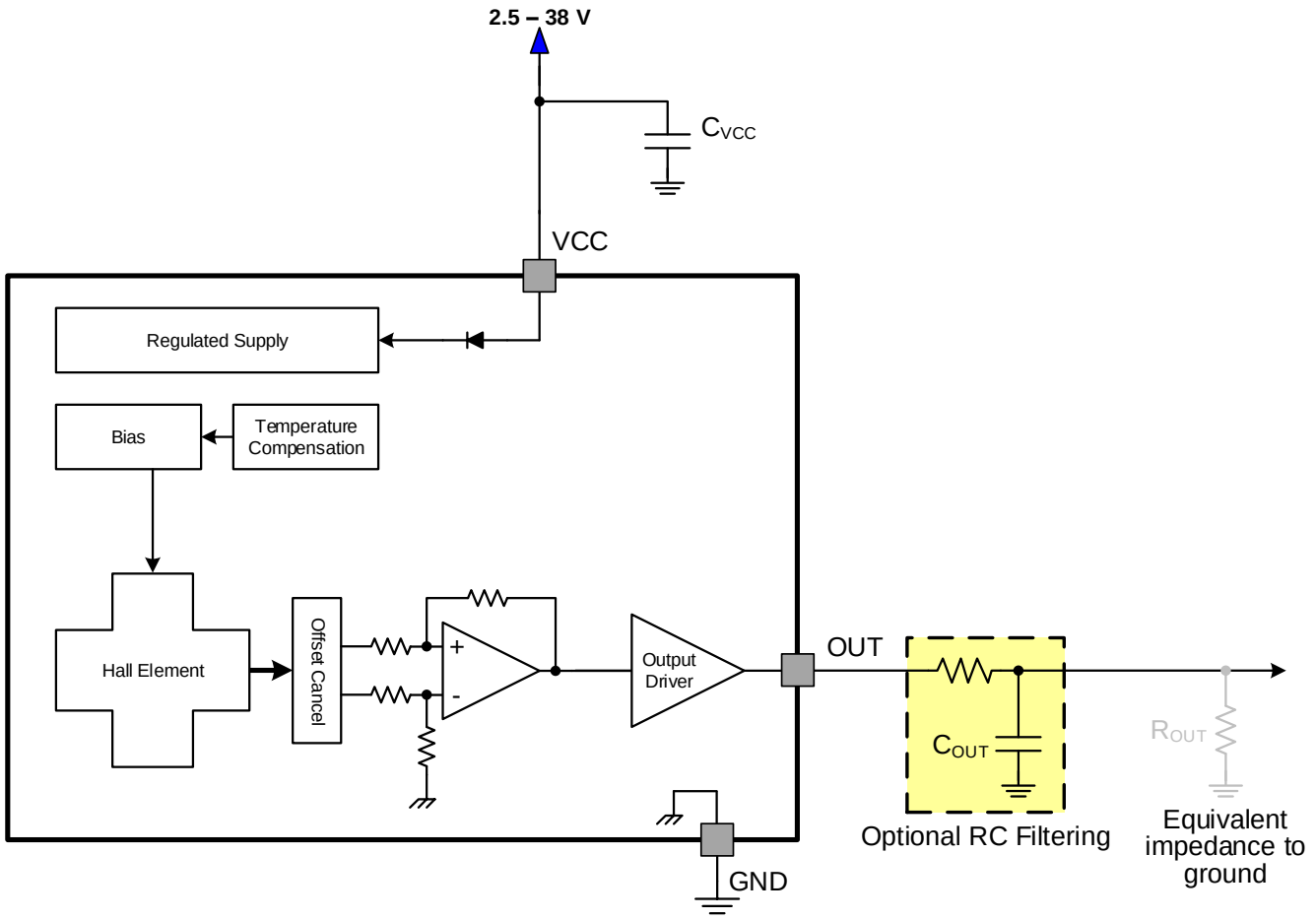
The output voltage is dependent on the magnetic field perpendicular to the package. The absence of a magnetic field will result in OUT = 1 V. A magnetic field will cause the output voltage to change linearly with the magnetic field.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

For devices with a negative sensitivity (that is, DRV5053RA: –40 mV/mT), a south pole will cause the output voltage to drop below 1 V, and a north pole will cause the output to rise above 1 V.

For devices with a positive sensitivity (that is, DRV5053EA: +40 mV/mT), a south pole will cause the output voltage to rise above 1 V, and a north pole will cause the output to drop below 1 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 7.

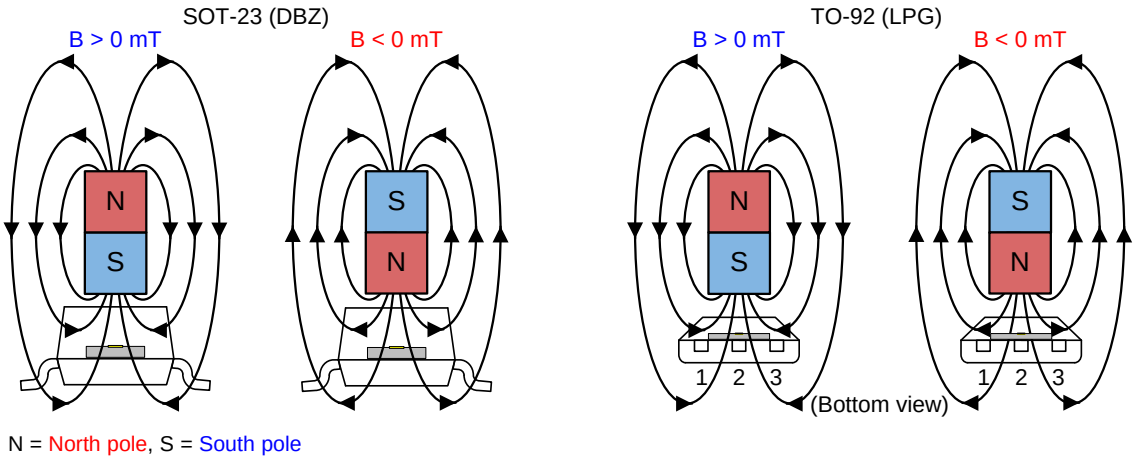


Figure 7. Field Direction Definition

7.3.2 Device Output

The DRV5053-Q1 device output is defined below for negative sensitivity (that is, –45 mV/mT, RA) and positive sensitivity (that is, +45 mV/mT, EA):

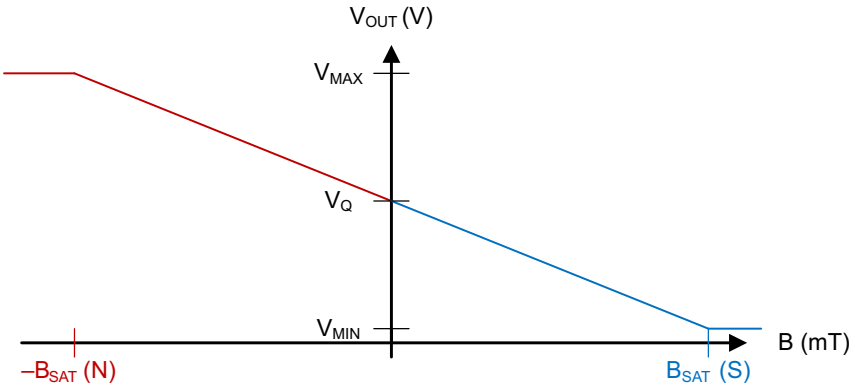


Figure 8. DRV5053-Q1 – Negative Sensitivity

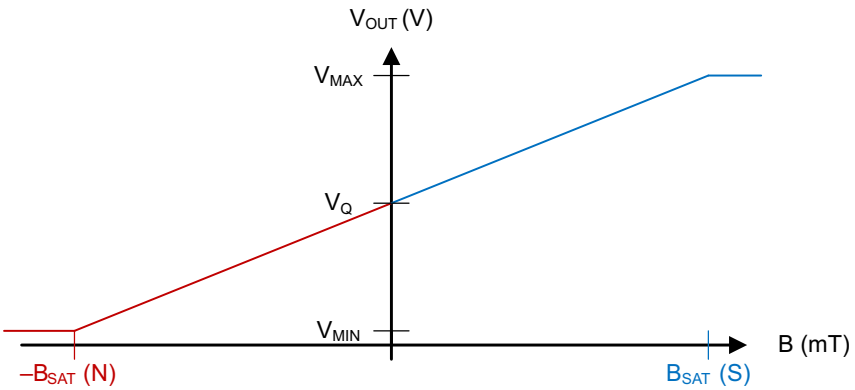


Figure 9. DRV5053-Q1 – Positive Sensitivity

Feature Description (continued)

7.3.3 Power-On Time

After applying V_{CC} to the DRV5053-Q1 device, t_{on} must elapse before OUT is valid. Figure 10 shows Case 1 and Figure 11 shows case 2; the output is defined assuming a negative sensitivity device and a constant magnetic field $-B_{SAT} < B < B_{SAT}$.

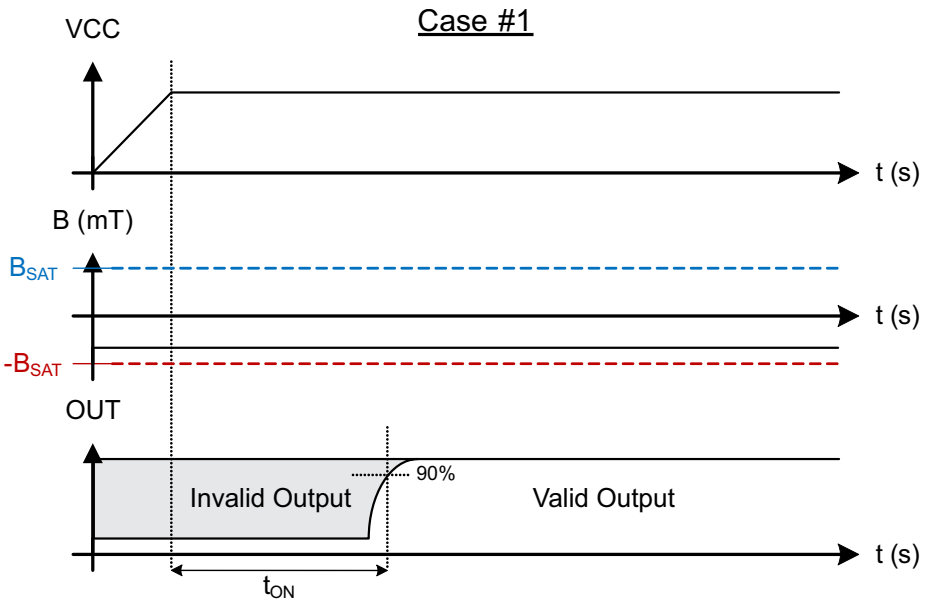


Figure 10. Case 1: Power On When B < 0, North

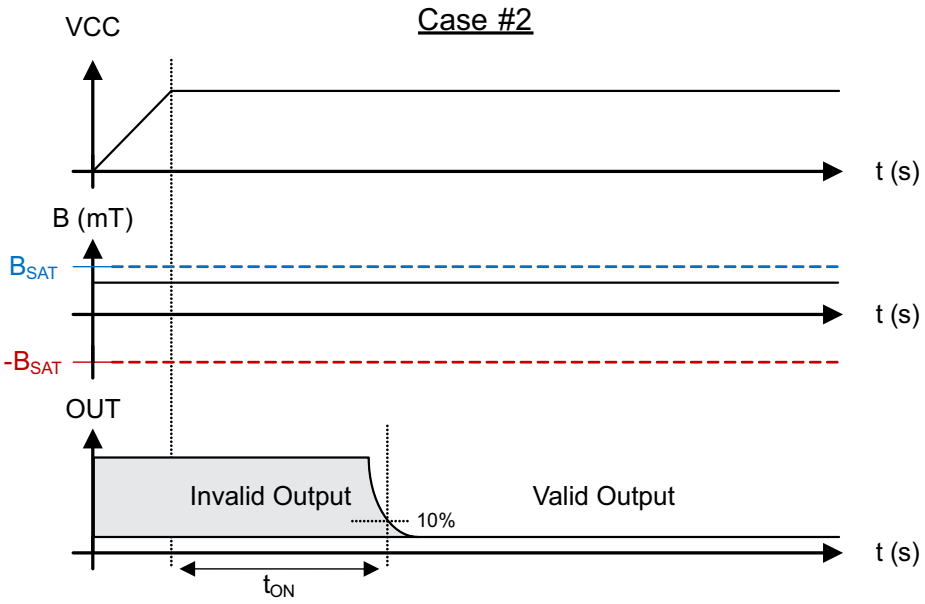


Figure 11. Case 2: Power On When B > 0, South

Feature Description (continued)

7.3.4 Output Stage

The DRV5053-Q1 output stage is capable of up to 300-µA of current source or 2.3-mA sink. For proper operation, ensure that equivalent output load R_{OUT} > 10 kΩ.

The capacitive load directly present on the OUT pin should be less than 10 nF to ensure the internal operational amplifier is stable. If an external RC filter is added to reduce noise, it is acceptable to use a resistor ≥ 200 Ω with a capacitor ≤0.1 µF. For an application example, see *Filtered Typical Application*.

7.3.5 Protection Circuits

An analog current limit circuit limits the current through the output driver. The driver current will be clamped to I_{OCP}

7.3.5.1 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

7.3.5.2 Load Dump Protection

The DRV5053-Q1 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

7.3.5.3 Reverse Supply Protection

The DRV5053-Q1 device is protected in the event that the V_{CC} pin and the GND pin are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT pin reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings*.

Table 1.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load Dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse Supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.7 V

7.4 Device Functional Modes

The DRV5053-Q1 device is active only when V_{CC} is between 2.7 and 38 V.

When a reverse supply condition exists, the device is inactive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV5053-Q1 device is used in magnetic-field sensing applications.

8.2 Typical Applications

8.2.1 Typical Application With No Filter

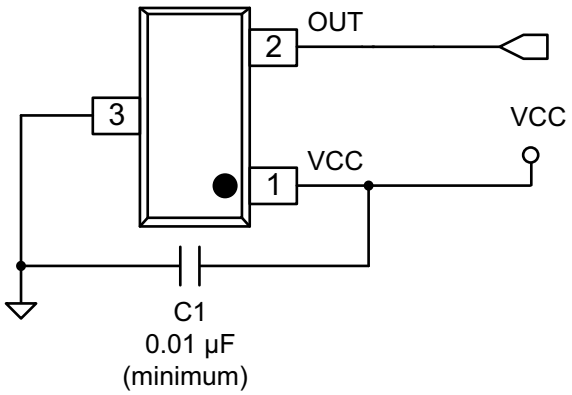


Figure 12. Typical Application Schematic – No Filter

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
System bandwidth	f_{BW}	15 kHz

8.2.1.2 Detailed Design Procedure

The DRV5053-Q1 has internal filtering that limits the bandwidth to at least 20 kHz. For this application no external components are required other than the C1 bypass capacitor, which is 0.01 µF minimum. If the analog output OUT is tied to a microcontroller ADC input, the equivalent load must be R > 10 kΩ and C < 10 nF.

Table 3. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}

8.2.1.3 Application Curve

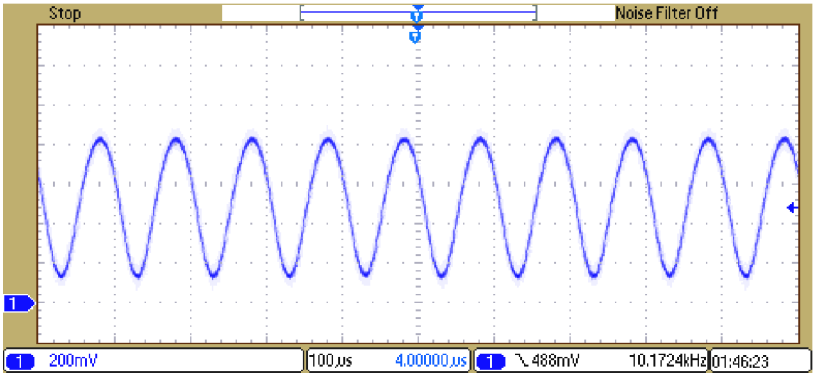


Figure 13. 10-kHz Switching Magnetic Field

8.2.2 Filtered Typical Application

For lower noise on the analog output OUT, additional RC filtering can be added to further reduce the bandwidth.

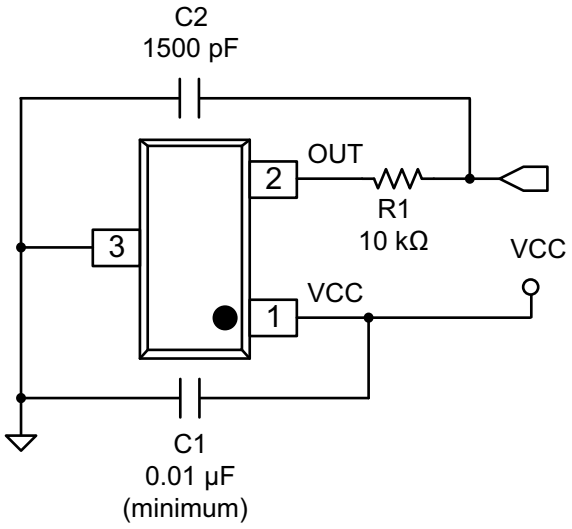


Figure 14. Filtered Typical Application Schematic

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
System bandwidth	f_{BW}	5 kHz

8.2.2.2 Detailed Design Procedure

In this example we will add an external RC filter in order to reduce the output bandwidth.

In order to preserve the signal at the frequencies of interest, we will conservatively select a low-pass filter bandwidth (–3-dB point) at twice the system bandwidth (10 kHz).

$$10\ \text{kHz} < \frac{1}{2\pi \times R_1 \times C_2} \tag{1}$$

If we guess R1 = 10 kΩ, then C2 < 1590 pF. So we select C2 = 1500 pF.

8.2.2.2.1 Typical Noise Versus Cutoff Frequency

RC filters are an effective way to reduce the noise present on OUT. The following shows typical noise measurements for different cutoff frequencies using the DRV5053VA.

Table 5. DRV5053VA Typical Noise Data

R (Ω)	C (µF)	f_{CUTOFF} (kHz)	NOISE (mVpp)
163	0.1	9.8	30.4
349	0.1	4.6	22.8
750	0.1	2.1	15.2
1505	0.1	1.1	9.7
3322	0.1	0.5	5.3
7510	0.1	0.2	2.5

8.2.2.3 Application Curves

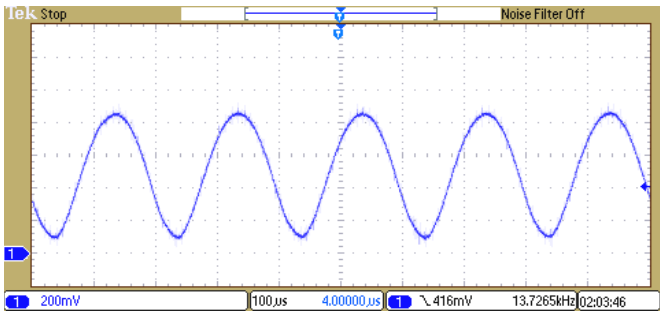


Figure 15. 5-kHz Switching Magnetic Field

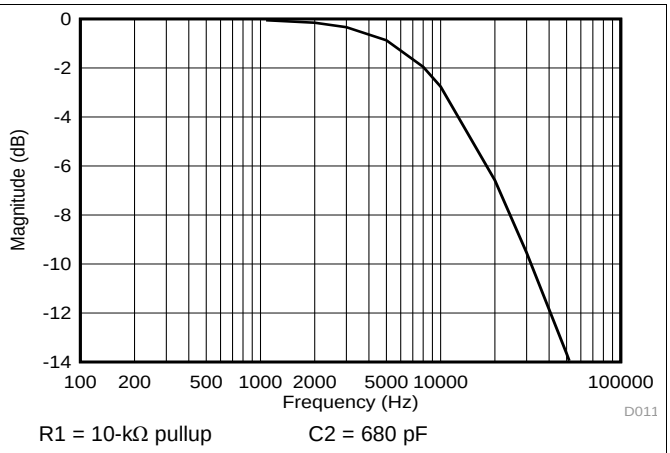


Figure 16. Low-Pass Filtering

9 Power Supply Recommendations

The DRV5053-Q1 device is designed to operate from an input voltage supply (VM) range between 2.7 and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5053-Q1 device as possible.

10 デバイスおよびドキュメントのサポート

10.1 デバイス・サポート

10.1.1 デバイスの項目表記

DRV5053-Q1デバイスの完全なデバイス名を読むための凡例を、図 17に示します。

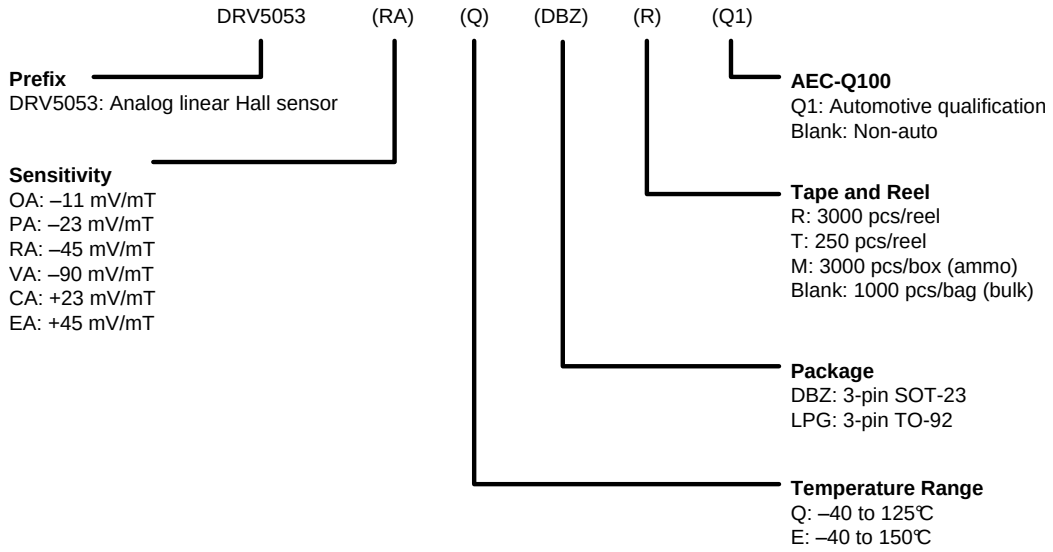


図 17. デバイス名の見方

10.1.2 デバイスのマーキング

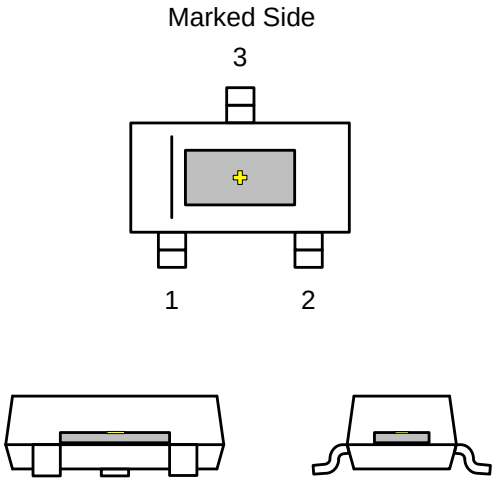


図 18. SOT-23 (DBZ)パッケージ

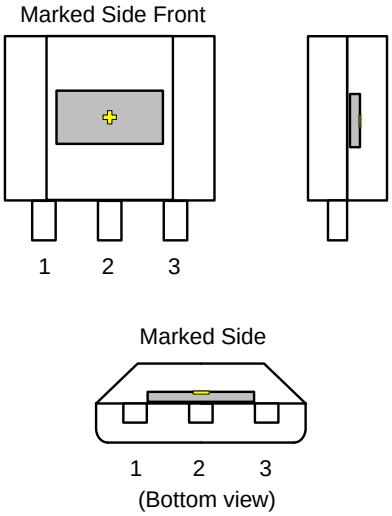


図 19. TO-92 (LPG)パッケージ

✚はホール効果センサを示します(実際の大きさに比例してはいません)。ホール素子はパッケージの中心に、許容誤差±100µmで配置されています。ホール素子の高さは、パッケージの底面から計測して、DBZパッケージでは0.7mm±50µm、LPGパッケージでは0.987mm±50µmです。

10.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

10.3 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

10.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

10.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5053CAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJCA	Samples
DRV5053CAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJCA	Samples
DRV5053CAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJCA	Samples
DRV5053CAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+AKCA	Samples
DRV5053CAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKCA	Samples
DRV5053CAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKCA	Samples
DRV5053EAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJEA	Samples
DRV5053EAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJEA	Samples
DRV5053EAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJEA	Samples
DRV5053EAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AKEA	Samples
DRV5053EAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AKEA	Samples
DRV5053EAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKEA	Samples
DRV5053OAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJOA	Samples
DRV5053OAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJOA	Samples
DRV5053OAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJOA	Samples
DRV5053OAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+AKOA	Samples
DRV5053OAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKOA	Samples
DRV5053OAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKOA	Samples
DRV5053PAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJPA	Samples
DRV5053PAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJPA	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5053PAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJPA	Samples
DRV5053PAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+AKPA	Samples
DRV5053PAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKPA	Samples
DRV5053PAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKPA	Samples
DRV5053RAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJRA	Samples
DRV5053RAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJRA	Samples
DRV5053RAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJRA	Samples
DRV5053RAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+AKRA	Samples
DRV5053RAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKRA	Samples
DRV5053RAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type		+AKRA	Samples
DRV5053VAEDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 150	+AJVA	Samples
DRV5053VAELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJVA	Samples
DRV5053VAELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	+AJVA	Samples
DRV5053VAQDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	+AKVA	Samples
DRV5053VAQLPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKVA	Samples
DRV5053VAQLPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	+AKVA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF DRV5053-Q1 :

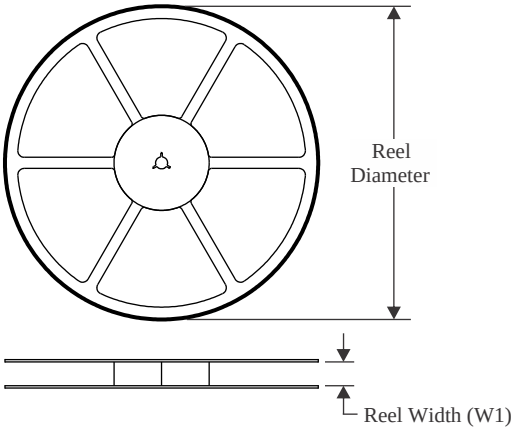
- Catalog : DRV5053

NOTE: Qualified Version Definitions:

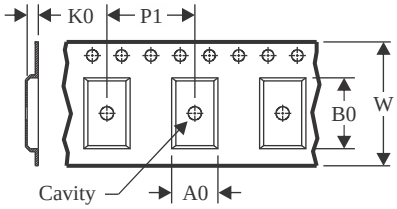
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

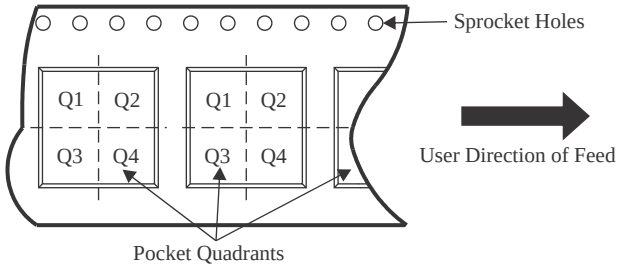


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

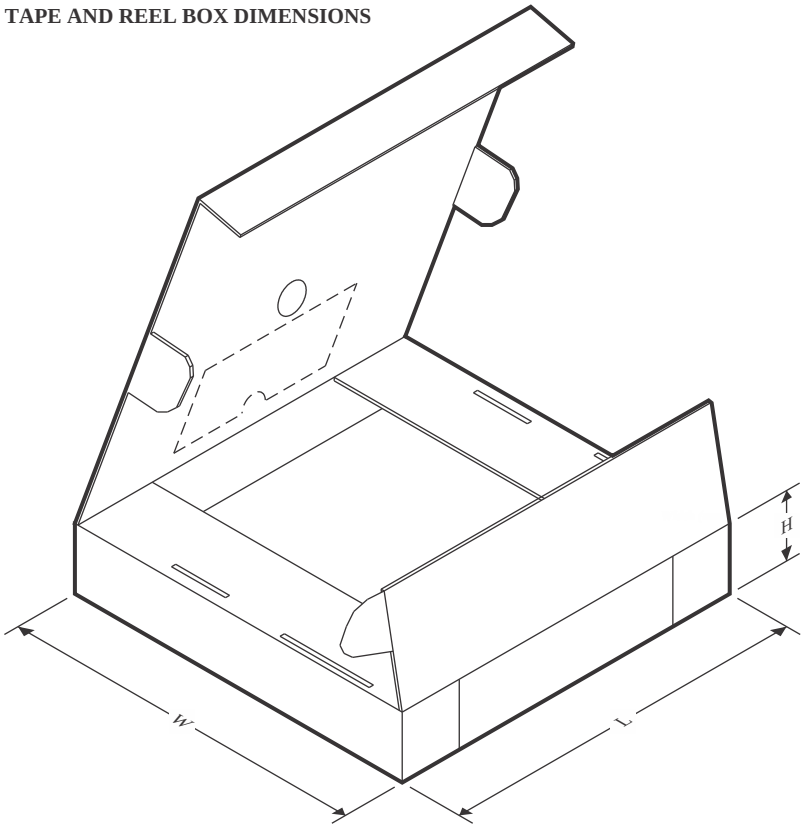
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5053CAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053CAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053EAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053EAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053OAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053OAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053PAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053PAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053RAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053RAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053VAEDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5053VAQDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

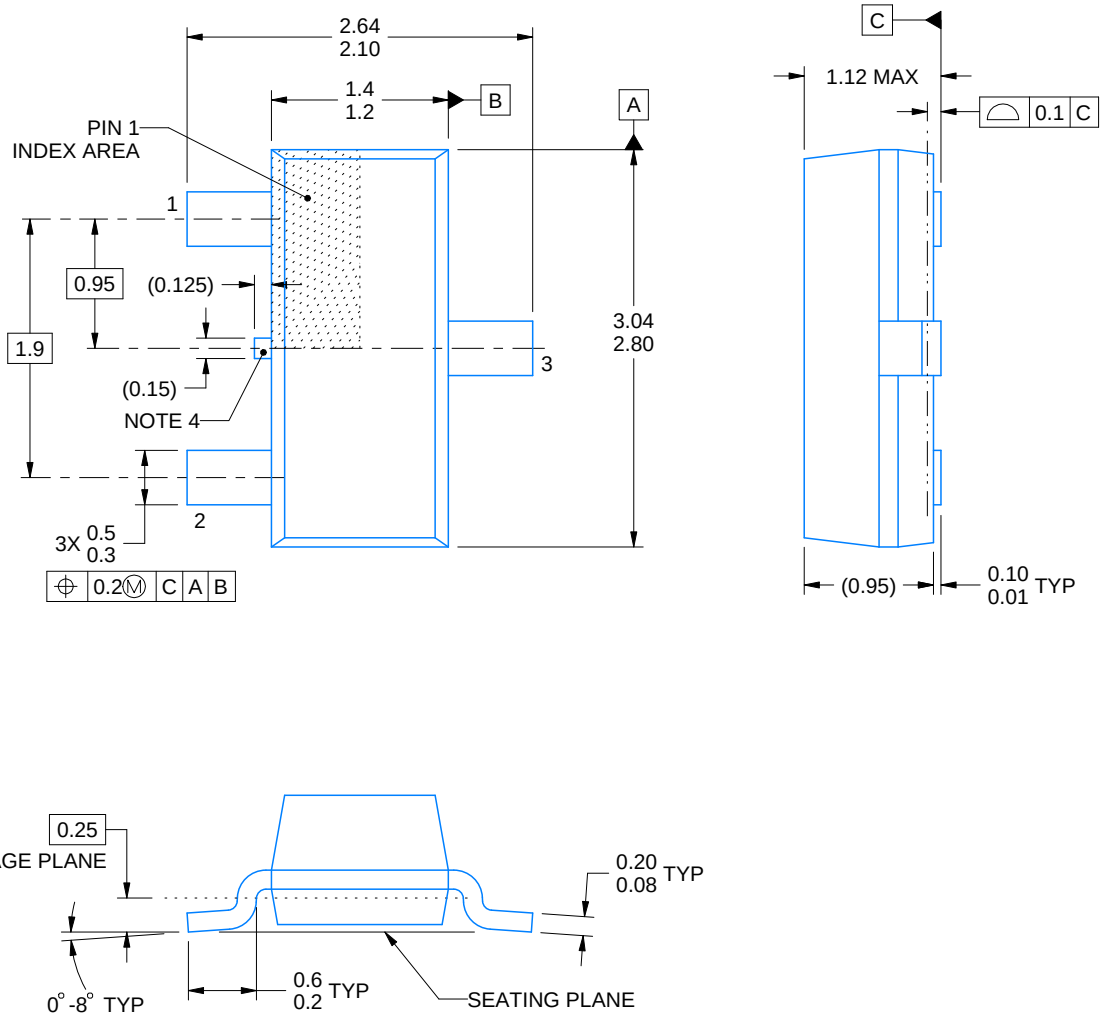
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5053CAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053CAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053EAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053EAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053OAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053OAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053PAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053PAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053RAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053RAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053VAEDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0
DRV5053VAQDBZRQ1	SOT-23	DBZ	3	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

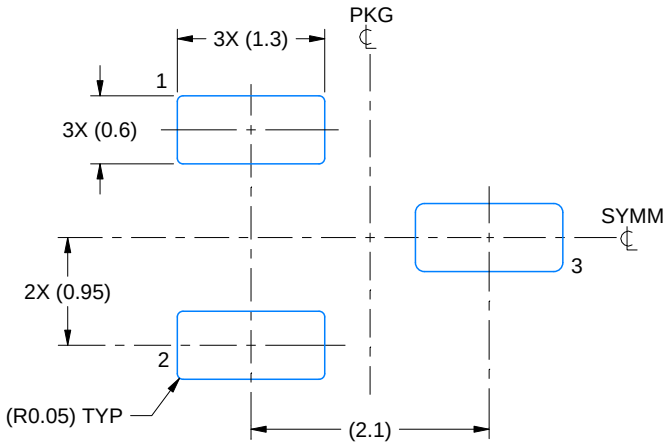
SMALL OUTLINE TRANSISTOR



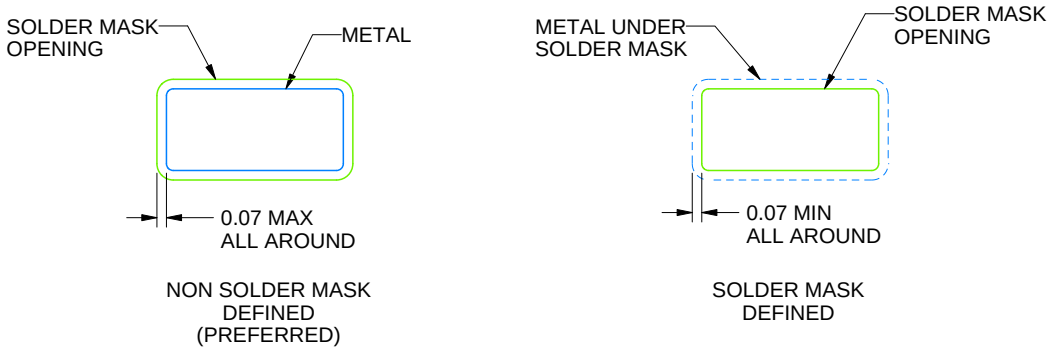
4214838/D 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:15X

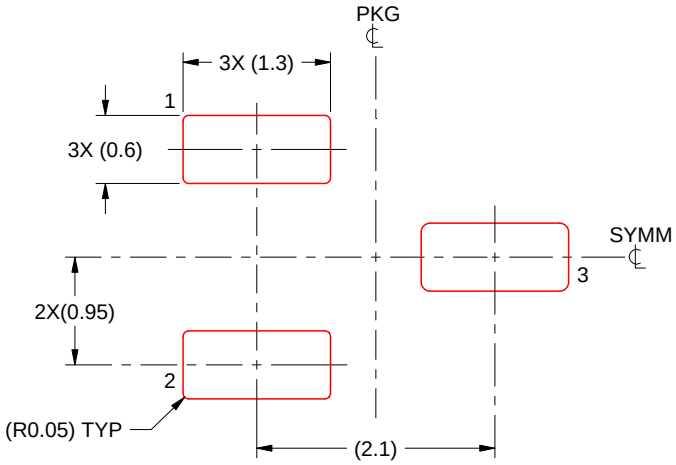


SOLDER MASK DETAILS

4214838/D 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/D 03/2023

NOTES: (continued)

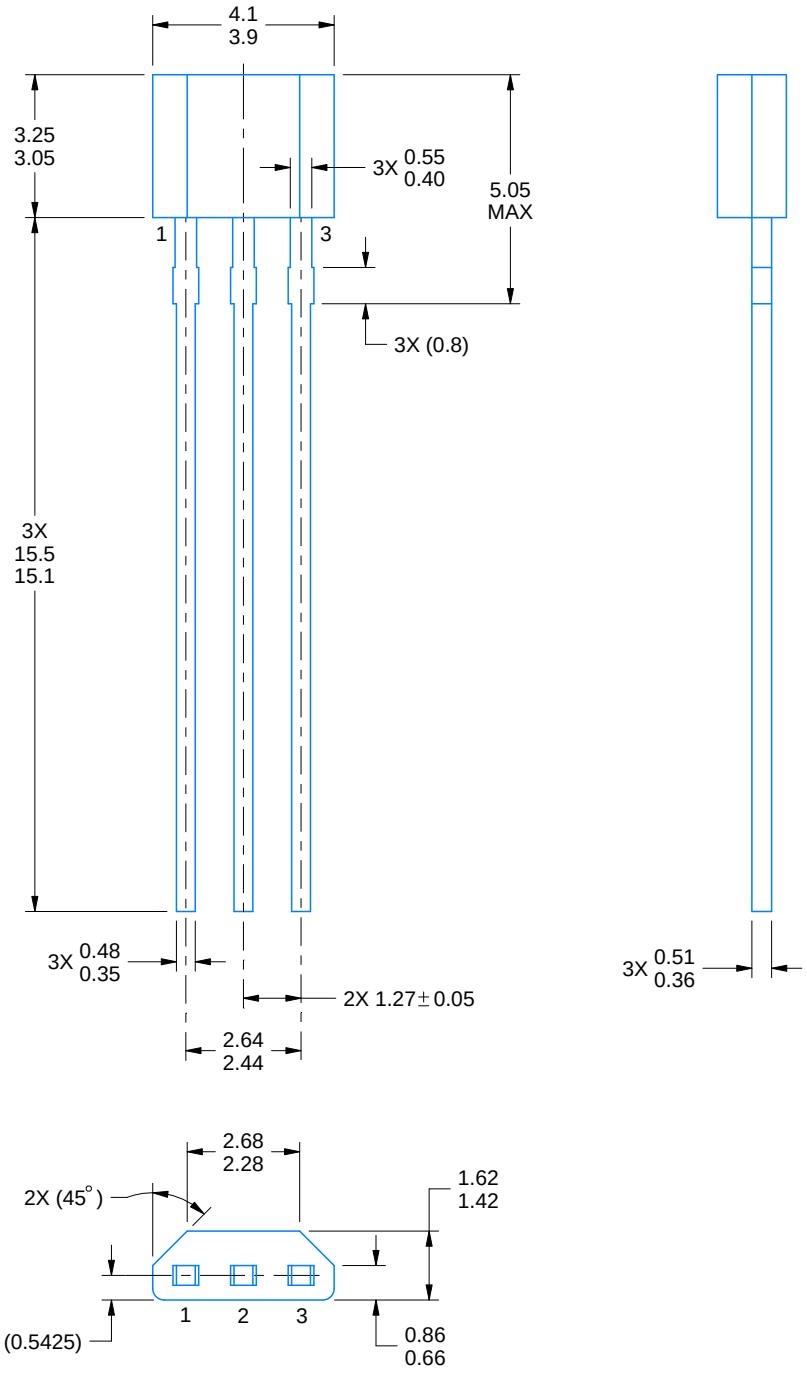
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

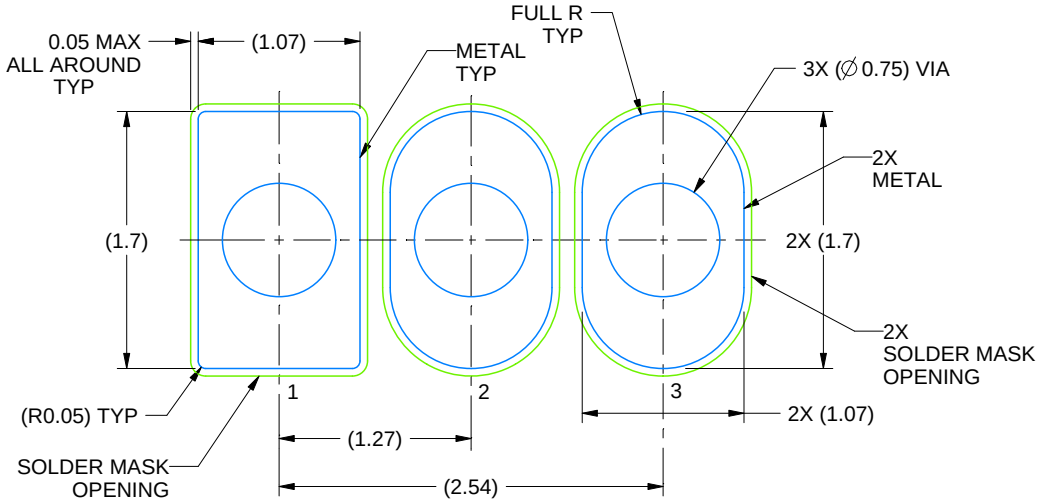
TRANSISTOR OUTLINE



4221343/C 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X

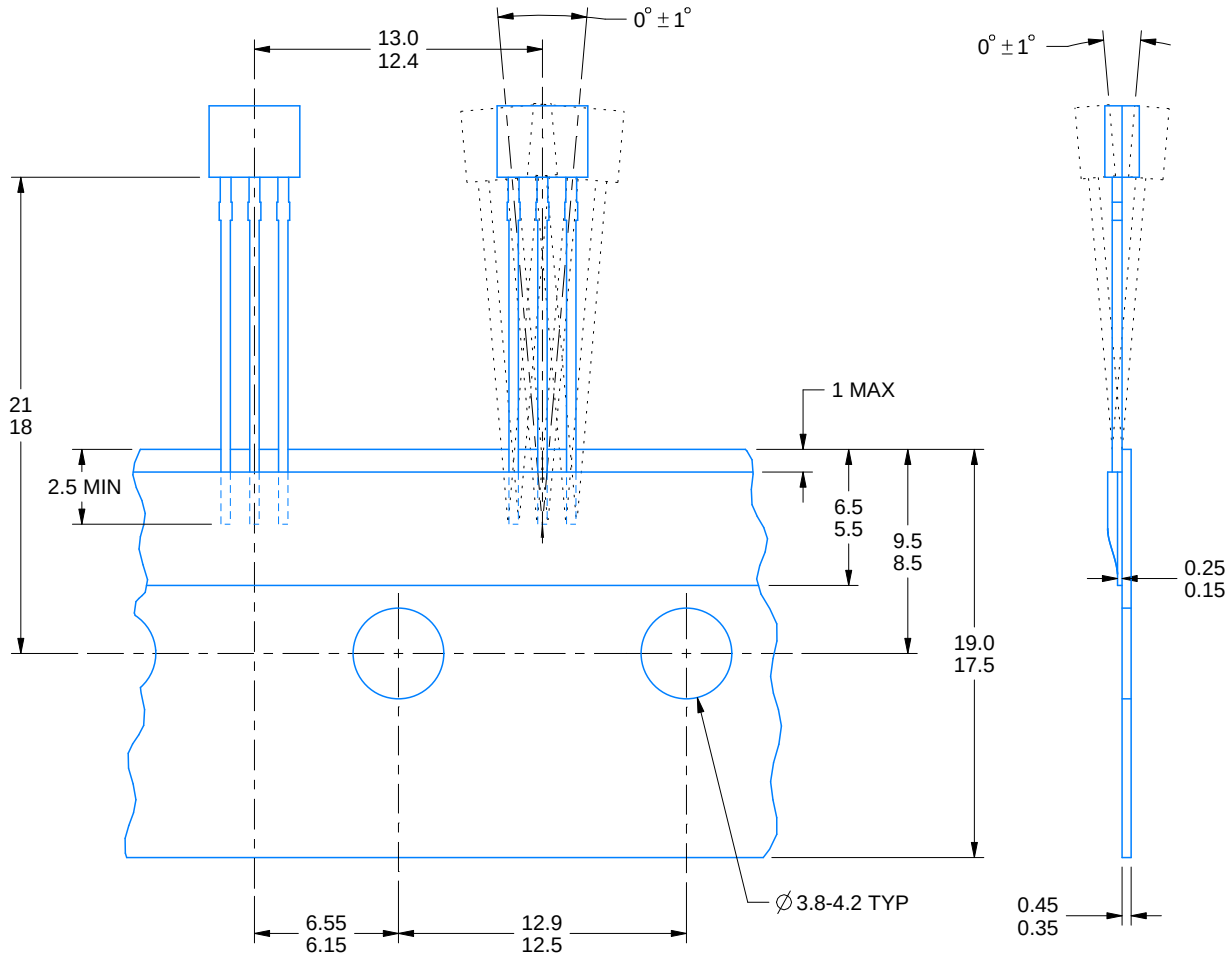
4221343/C 01/2018

TAPE SPECIFICATIONS

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

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