TEXAS INSTRUMENTS
DRV8316-Q1
JAJSN64 – JANUARY 2022

DRV8316-Q1 3 相 FET 内蔵モーター・ドライバ

1 特長

- 車載アプリケーション向けの AEC-Q100 認証取得済み
  - 温度グレード 1:-40℃ ≤ TA ≤ 125℃
- 3 相 BLDC モーター・ドライバ
- 動作電圧:4.5V～35V (絶対最大定格 40V)
- 高い出力電流能力:ピーク 8A
- 低い MOSFET ON 抵抗
  - T_A = 25℃で 95mΩ の $R_{DS(ON)}$ (HS + LS)
- 低消費電力スリープ・モード
  - V_{VM} = 24V、T_A = 25℃で 1.5μA
- 複数の制御インターフェイス・オプション
  - 6x PWM 制御インターフェイス
  - 3x PWM 制御インターフェイス
- 低インダクタンスのモーターをサポートするため、最大 200kHz の PWM 周波数に対応
- サイクル単位の電流制限
- 統合型の電流センス機能を内蔵
  - 外付け電流センス抵抗不要
- ハードウェアまたは 5MHz の 16 ビット SPI インターフェイス
- 1.8V、3.3V、5V のロジック入力電圧に対応
- 3.3V (5%)、30mA の LDO レギュレータを内蔵
- 3.3V/5V、200mA の降圧レギュレータを内蔵
- 遅延補償によりデューティ・サイクルの歪みを低減
- 一連の内蔵保護機能
  - 電源低電圧誤動作防止 (UVLO)
  - チャージ・ポンプ低電圧 (CPUV)
  - 過電流保護 (OCP)
  - 熱警告およびシャットダウン (OTW/OTSD)
  - フォルト状況表示ピン (nFAULT)
  - SPI インターフェイスによるフォルト診断 (任意)

2 アプリケーション

- ブラシレス DC (BLDC) モーター・モジュール
- 車載用 LIDAR
- 小型の車載用ファンおよびポンプ
- 車載用アクチュエータ

3 概要

DRV8316-Q1 は、12V ブラシレス DC モーターを最大 40W で駆動するシングル・チップ出力段ソリューションです。DRV8316-Q1 は、40V の絶対最大定格能力および 95mΩ (下限側と上限側) の非常に小さい RDS (ON) を備えた 3 つの 1/2-H ブリッジを内蔵し、大電力の駆動能力を実現しています。電流は、外付けセンス抵抗を使わない内蔵電流検出機能を使って測定します。可変降圧レギュレータおよび LDO の電源管理機能は、デバイスに必要な電圧レールを生成します。また、外部回路に電力を供給するためにも使用できます。

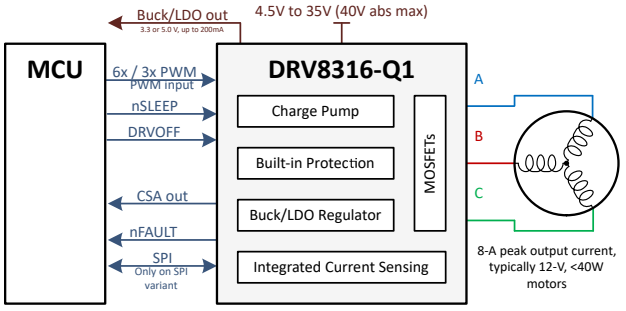
DRV8316-Q1 には 6x または 3x の PWM 制御方式が実装されており、センサ付きまたはセンサレスのフィールド・オリエンテッド制御 (FOC)、正弦波制御、または外付けマイコンを使用した台形制御を実現できます。DRV8316-Q1 は最大 200kHz の PWM 周波数を駆動できます。制御方式は、モーター電流制限動作からフォルト応答まで、ハードウェア・ピンまたはレジスタ設定を使って詳細に設定できます。

DRV8316-Q1 は、本デバイス自身、モーター、システムをフォルト・イベントから保護するための多くの保護機能を内蔵しています。

デバイス情報(1)

部品番号	パッケージ	本体サイズ (公称)
DRV8316R-Q1	VQFN (40)	7.00mm × 5.00mm
DRV8316T-Q1(2)	VQFN (40)	7.00mm × 5.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) このデバイスはプレビュー版としてのみ供給されます。



概略回路図

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
January 2022	*	Initial Release

5 Device Comparison Table

DEVICE	PACKAGES	INTERFACE	BUCK REGULATOR
DRV8316R-Q1	40-pin VQFN (7x5 mm)	SPI	Yes
DRV8316T-Q1[(1)]		Hardware	

(1) Device available for preview only.

6 Pin Configuration and Functions

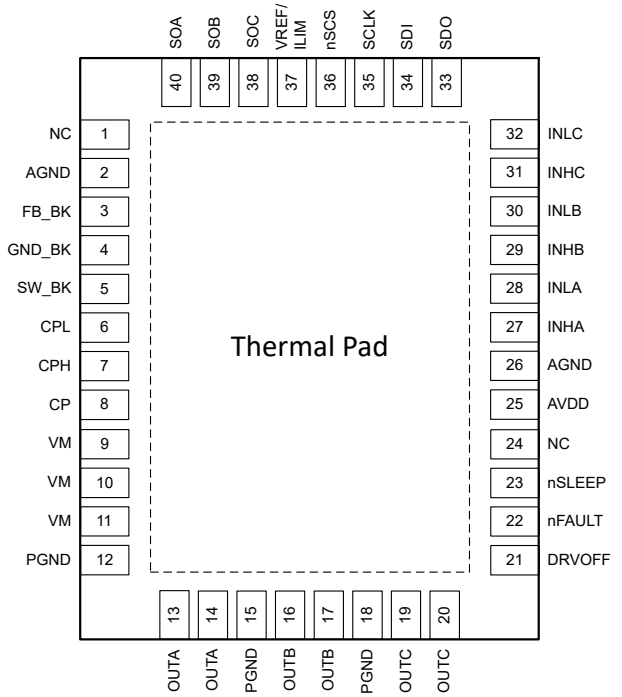


図 6-1. DRV8316R-Q1 40-Pin VQFN With Exposed Thermal Pad Top View

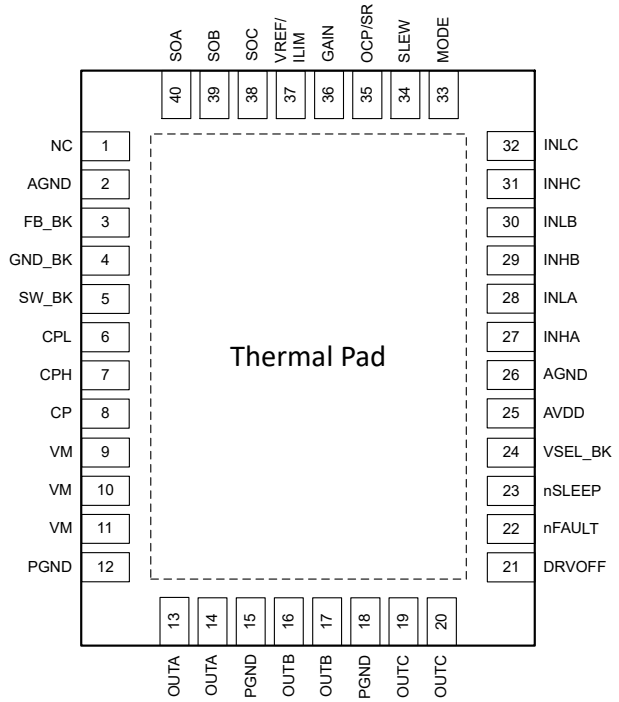


図 6-2. DRV8316T-Q1 40-Pin VQFN With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN	40-pin Package		TYPE[1]	DESCRIPTION
NAME	DRV8316R-Q1	DRV8316T-Q1		
AGND	2, 26	2, 26	GND	Device analog ground. Refer Layout Guidelines for connections recommendation.
AVDD	25	25	PWR O	3.3-V internal regulator output. Connect an X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30 mA externally.
CP	8	8	PWR O	Charge pump output. Connect a X5R or X7R, 1-µF, 16-V ceramic capacitor between the CP and VM pins.
CPH	7	7	PWR	Charge pump switching node. Connect a X5R or X7R, 47-nF, ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
CPL	6	6	PWR	
DRVOFF	21	21	I	When this pin is pulled high the six MOSFETs in the power stage are turned OFF making all outputs Hi-Z.
FB_BK	3	3	PWR I	Feedback for buck regulator. Connect to buck regulator output after the inductor/resistor.
GAIN	—	36	I	Amplifier gain setting. The pin is a 4 level input pin set by an external resistor.
GND_BK	4	4	GND	Buck regulator ground. Refer Layout Guidelines for connections recommendation.
INHA	27	27	I	High-side driver control input for OUTA. This pin controls the output of the high-side MOSFET.
INHB	29	29	I	High-side driver control input for OUTB. This pin controls the output of the high-side MOSFET.
INHC	31	31	I	High-side driver control input for OUTC. This pin controls the output of the high-side MOSFET.
INLA	28	28	I	Low-side driver control input for OUTA. This pin controls the output of the low-side MOSFET.

表 6-1. Pin Functions (continued)

PIN	40-pin Package		TYPE[1]	DESCRIPTION
NAME	DRV8316R-Q1	DRV8316T-Q1		
INLB	30	30	I	Low-side driver control input for OUTB. This pin controls the output of the low-side MOSFET.
INLC	32	32	I	Low-side driver control input for OUTC. This pin controls the output of the low-side MOSFET.
MODE	—	33	I	PWM input mode setting. This pin is a 2-level input pin set by an external resistor.
NC	1, 24	1	—	No connection, open
nFAULT	22	22	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0 V. If external supply is used to pull up nFAULT, ensure that it is pulled to >2.2 V on power up or the device will enter test mode
nSCS	36	—	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	23	23	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 20 to 40-µs low pulse can be used to reset fault conditions without entering sleep mode.
OCP	—	35	I	OCP level setting. This pin is a 2 level input pin set by an external resistor (Hardware devices).
OUTA	13, 14	13, 14	PWR O	Half bridge output A
OUTB	16, 17	16, 17	PWR O	Half bridge output B
OUTC	19, 20	19, 20	PWR O	Half bridge output C
PGND	12, 15, 18	12, 15, 18	GND	Device power ground. Refer Layout Guidelines for connections recommendation.
SCLK	35	—	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	34	—	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	33	—	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
SLEW	—	34	I	Slew rate control setting. This pin is a 4-level input pin set by an external resistor.
SOA	40	40	O	Current sense amplifier output.
SOB	39	39	O	Current sense amplifier output.
SOC	38	38	O	Current sense amplifier output.
SW_BK	5	5	PWR O	Buck switch node. Connect this pin to an inductor or resistor.
VM	9, 10, 11	9, 10, 11	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with two 0.1-µF capacitors (for each pin) plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
VSEL_BK	—	24	I	Buck output voltage setting. This pin is a 4-level input pin set by an external resistor.
VREF/ILIM	37	37	PWR/I	VREF in PWM Mode 1 and Mode 3: Current sense amplifier power supply input and reference. Connect a X5R or X7R, 0.1-µF, 6.3-V ceramic capacitor between the VREF and AGND pins. ILIM in PWM Mode 2 and Mode4: Sets the threshold for phase current used in cycle by cycle current limit.
Thermal pad			GND	Must be connected to analog ground.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM)		4	V/µs
Voltage difference between ground pins (GND_BK, PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CPH, CP)	–0.3	V_M + 6	V
Charge pump negative switching pin voltage (CPL)	–0.3	V_M + 0.3	V
Switching regulator pin voltage (FB_BK)	–0.3	5.75	V
Switching node pin voltage (SW_BK)	–0.3	V_M + 0.3	V
Analog regulators pin voltage (AVDD)	–0.3	4	V
Logic pin input voltage (DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO)	–0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_M + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings AUTO

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	Corner pins	±750	
			Other pins	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	4.5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			200	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			8	A
V_{IN}	Logic input voltage	DRVOFF, INHx, INLx, nSCS, nSLEEP, SCLK, SDI	–0.1		5.5	V
V_{OD}	Open drain pullup voltage	nFAULT, SDO	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		5.5	V
I_{OD}	Open drain output current	nFAULT, SDO			5	mA
V_{VREF}	Voltage reference pin voltage	VREF	2.8		AVDD	V
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DRV8316T-Q1, DRV8316R-Q1 VQFN (RGF) 40 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, nSLEEP = 0, T_A = 25 °C		1.5	2.5	µA
		nSLEEP = 0		2.5	5	µA
I_{VMS}	VM standby mode current (Buck regulator disabled)	nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', BUCK_DIS = 1;		4	10	mA
		V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', T_A = 25 °C, BUCK_DIS = 1;		4	5	mA
I_{VMS}	VM standby mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', I_{BK} = 0, T_A = 25 °C, BUCK_DIS = 0;		5	6	mA
		nSLEEP = 1, INHx = INLx = 0, SPI = 'OFF', I_{BK} = 0, BUCK_DIS = 0;		6	10	mA
I_{VM}	VM operating mode current (Buck regulator disabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 1		10	13	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 1		18	21	mA
		nSLEEP =1, f_{PWM} = 25 kHz, BUCK_DIS = 1		11	16	mA
		nSLEEP =1, f_{PWM} = 200 kHz, BUCK_DIS = 1		17	25	mA
I_{VM}	VM operating mode current (Buck regulator enabled)	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		11	13	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 200 kHz, T_A = 25 °C, BUCK_DIS = 0; BUCK_PS_DIS = 0		19	22	mA
		nSLEEP =1, f_{PWM} = 25 kHz, BUCK_DIS = 0; BUCK_PS_DIS = 0		12	17	mA
		nSLEEP =1, f_{PWM} = 200 kHz, BUCK_DIS = 0; BUCK_PS_DIS = 0		18	27	mA
V_{AVDD}	Analog regulator voltage	0 mA ≤ I_{AVDD} ≤ 30 mA; BUCK_PS_DIS = 0	3.1	3.3	3.465	V
I_{AVDD}	External analog regulator load				30	mA
V_{VCP}	Charge pump regulator voltage	VCP with respect to VM	3.6	4.7	5.25	V
f_{CP}	Charge pump switching frequency			400		kHz

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released			1	ms
t_{SLEEP}	Sleep Pulse time	nSLEEP = 0 period to enter sleep mode	120			µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
BUCK REGULATOR						
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 200 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2)(1)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 50 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2) (1)		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (SPI Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 00b	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 01b	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 10b	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, BUCK_SEL = 11b	5.2	5.7	6.2	V
		V_{VM} < 6.0 V (BUCK_SEL = 00b, 01b, 10b) or V_{VM} < 6.0 V (BUCK_SEL = 11b), 0 mA ≤ I_{BK} ≤ 40 mA		V_{VM}– I_{BK}*(R_{BK}+2)		V
V_{BK}	Buck regulator average voltage (L_{BK} = 47 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 200 mA, VSEL_BK pin tied to AVDD	5.2	5.7	6.2	
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 200 mA		V_{VM}– I_{BK}*(R_{LBK}+ 2)(1)		V

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK}	Buck regulator average voltage (L_{BK} = 22 µH, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 50 mA, VSEL_BK pin tied to AVDD	5.2	5.7	6.2	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 50 mA		V_{VM} – I_{BK}*(R_{LBK}+ 2)[(1)]		V
V_{BK}	Buck regulator average voltage (R_{BK} = 22 Ω, C_{BK} = 22 µF) (HW Device)	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin tied to AGND	3.1	3.3	3.5	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to Hi-Z	4.6	5.0	5.4	V
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	3.7	4.0	4.3	V
		V_{VM} > 6.7 V, 0 mA ≤ I_{BK} ≤ 40 mA, VSEL_BK pin tied to AVDD	5.2	5.7	6.2	V
		V_{VM} < 6.0 V, 0 mA ≤ I_{BK} ≤ 40 mA		V_{VM} – I_{BK}*(R_{BK}+2)		V
V_{BK_RIP}	Buck regulator ripple voltage	V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 200 mA, Buck regulator with inductor, L_{BK} = 47 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with inductor, L_{BK} = 22 uH, C_{BK} = 22 µF	–100		100	mV
		V_{VM} > 6 V, 0 mA ≤ I_{BK} ≤ 50 mA, Buck regulator with resistor; R_{BK} = 22 Ω, C_{BK} = 22 µF	–100		100	mV
I_{BK}	External buck regulator load	L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			200	mA
		L_{BK} = 47 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			200 – I_{AVDD}	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			50	mA
		L_{BK} = 22 uH, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			50 – I_{AVDD}	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 1b			40	mA
		R_{BK} = 22 Ω, C_{BK} = 22 µF, BUCK_PS_DIS = 0b			40 – I_{AVDD}	mA
f_{SW_BK}	Buck regulator switching frequency	Regulation Mode	20		535	kHz
		Linear Mode	20		535	kHz

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BK_UV}	Buck regulator undervoltage lockout (SPI Device)	V_{BK} rising, BUCK_SEL = 00b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 00b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 01b	4.2	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 01b	4.0	4.2	4.35	V
		V_{BK} rising, BUCK_SEL = 10b	2.7	2.8	2.9	V
		V_{BK} falling, BUCK_SEL = 10b	2.5	2.6	2.7	V
		V_{BK} rising, BUCK_SEL = 11b	4.2	4.4	4.55	V
		V_{BK} falling, BUCK_SEL = 11b	4	4.2	4.35	V
V_{BK_UV}	Buck regulator undervoltage lockout (HW Device)	V_{BK} rising, VSEL_BK pin tied to AGND	2.7	2.8	2.9	V
		V_{BK} falling, VSEL_BK pin tied to AGND	2.5	2.6	2.7	V
		V_{BK} rising, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	4.3	4.4	4.5	V
		V_{BK} falling, VSEL_BK pin to 47 kΩ +/- 5% tied to AVDD	4.1	4.2	4.3	V
		V_{BK} rising, VSEL_BK pin to Hi-Z	2.7	2.8	2.9	V
		V_{BK} falling, VSEL_BK pin to Hi-Z	2.5	2.6	2.7	V
		V_{BK} rising, VSEL_BK pin tied to AVDD	4.2	4.4	4.55	V
		V_{BK} falling, VSEL_BK pin tied to AVDD	4.0	4.2	4.35	V
$V_{BK\_UV\_HYS}$	Buck regulator undervoltage lockout hysteresis	Rising to falling threshold	90	200	320	mV
I_{BK_CL}	Buck regulator Current limit threshold (SPI Device)	BUCK_CL = 0b	360	600	900	mA
		BUCK_CL = 1b	80	150	250	mA
I_{BK_CL}	Buck regulator Current limit threshold (HW Device)		360	600	900	mA
I_{BK_OCP}	Buck regulator Overcurrent protection trip point		2	3	4	A
t_{BK_RETRY}	Overcurrent protection retry time		0.7	1	1.3	ms
LOGIC-LEVEL INPUTS (DRVOFF, INHx, INLx, nSLEEP, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	Other Pins	1.5		5.5	V
		nSLEEP	1.6		5.5	V
V_{HYS}	Input logic hysteresis	Other PIns	180	300	420	mV
		nSLEEP	95	250	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA
I_{IH}	Input logic high current	nSLEEP, V_{PIN} (Pin Voltage) = 5 V	10		30	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V	30		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	200	300	kΩ
		Other pins	70	100	130	kΩ
C_{ID}	Input capacitance			30		pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		180	300	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V			75	µA
I_{IH}	Input logic high current	V_{PIN} (Pin Voltage) = 5 V	–1		25	µA
R_{PU}	Input pullup resistance		80	100	130	kΩ
C_{ID}	Input capacitance			30		pF

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FOUR-LEVEL INPUTS (GAIN, MODE, SLEW, VSEL_BK)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.2*AVDD	V
V_{L2}	Input mode 2 voltage	Hi-Z	0.27*AVDD	0.5*AVDD	0.545*AVDD	V
V_{L3}	Input mode 3 voltage	47 kΩ +/- 5% tied to AVDD	0.606*AVDD	0.757*AVDD	0.909*AVDD	V
V_{L4}	Input mode 4 voltage	Tied to AVDD	0.945*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	70	100	130	kΩ
R_{PD}	Input pulldown resistance	To AGND	70	100	130	kΩ
FOUR-LEVEL INPUTS (OCP/SR)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		0.09*AVDD	V
V_{L2}	Input mode 2 voltage	22 kΩ ± 5% to AGND	0.12*AVDD	0.15*AVDD	0.2*AVDD	V
V_{L3}	Input mode 3 voltage	Hi-Z	0.45*AVDD	0.5*AVDD	0.55*AVDD	V
V_{L4}	Input mode 4 voltage	Tied to AVDD	0.94*AVDD		AVDD	V
R_{PU}	Input pullup resistance	To AVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA	2.2		5.5	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		95	120	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		105	130	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		140	185	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		145	190	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND	14	25	45	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z	30	50	80	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	185	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD	130	200	280	V/us

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Phase pin slew rate switching high to low (Falling from 80 % to 20 %	V_{VM} = 24 V, SLEW = 00b or SLEW pin tied to AGND	14	25	45	V/us
		V_{VM} = 24 V, SLEW = 01b or SLEW pin to Hi-Z	30	50	80	V/us
		V_{VM} = 24 V, SLEW = 10b or SLEW pin to 47 kΩ +/- 5% to AVDD	80	125	185	V/us
		V_{VM} = 24 V, SLEW = 11b or SLEW pin tied to AVDD	110	200	280	V/us
I_{LEAK}	Leakage current on OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1			5	mA
	Leakage current on OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, SR = 25 V/µs, HS driver ON to LS driver OFF		1800	3400	ns
		V_{VM} = 24 V, SR = 50 V/µs, HS driver ON to LS driver OFF		1100	1550	ns
		V_{VM} = 24 V, SR = 125 V/µs, HS driver ON to LS driver OFF		650	1000	ns
		V_{VM} = 24 V, SR = 200 V/µs, HS driver ON to LS driver OFF		500	750	ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 25 V/µs		2000	4550	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 50V/µs		1200	2150	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 125 V/µs		800	1350	ns
		V_{VM} = 24 V, INHx = 1 to OUTx transisition, SR = 200 V/µs		650	1050	ns
t_{MIN_PULSE}	Minimum output pulse width	SR = 200 V/µs	600			ns
CURRENT SENSE AMPLIFIER						
G_{CSA}	Current sense gain (SPI Device)	CSA_GAIN = 00		0.15		V/A
		CSA_GAIN = 01		0.3		V/A
		CSA_GAIN = 10		0.6		V/A
		CSA_GAIN = 11		1.2		V/A
G_{CSA}	Current sense gain (HW Device)	GAIN pin tied to AGND		0.15		V/A
		GAIN pin to Hi-Z		0.3		V/A
		GAIN pin to 47 kΩ ± 5% to AVDD		0.6		V/A
		GAIN pin tied to AVDD		1.2		V/A
G_{CSA_ERR}	Current sense gain error	T_A = 25°C, I_{PHASE} < 4A	–9.5		9.5	%
		T_A = 25°C, I_{PHASE} > 4A	–10.5		10.5	%
		I_{PHASE} < 4 A	–10.5		10.5	%
		I_{PHASE} > 4 A	–12.5		12.5	%
I_{MATCH}	Current sense gain error matching between phases A, B and C	T_A = 25°C	–4.5		4.5	%
			–7		7	%
FS_{POS}	Full scale positive current measurement		8			A
FS_{NEG}	Full scale negative current measurement				–8	A
V_{LINEAR}	SOX output voltage linear range		0.25		V_{VREF} – 0.25	V
I_{OFFSET}	Current sense offset low side current in	Phase current = 0 A, G_{CSA} = 0.15 V/A	–50		50	mA
		Phase current = 0 A, G_{CSA} = 0.3 V/A	–50		50	mA
		Phase current = 0 A, G_{CSA} = 0.6 V/A	–50		50	mA
		Phase current = 0 A, G_{CSA} = 1.2 V/A	–50		50	mA

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SET}	Settling time to ±1%, 30 pF	Step on SOX = 1.2 V, G_{CSA} = 0.15 V/A			1	µs
		Step on SOX = 1.2 V, G_{CSA} = 0.3 V/A			1	µs
		Step on SOX = 1.2 V, G_{CSA} = 0.6 V/A			1	µs
		Step on SOX = 1.2 V, G_{CSA} = 1.2 V/A			1	µs
V_{DRIFT}	Drift offset	Phase current = 0 A	–160		160	µA/°C
I_{VREF}	VREF input current	VREF = 3.0 V			50	µA
PSRR	Power Supply Rejection Ratio	AVDD to SOx, DC	55		80	dB
		AVDD to SOx, 10 kHz	39		56	dB
		AVDD to SOx, 500 kHz	5		22	dB
PULSE-BY-PULSE CURRENT LIMIT						
V_{LIM}	Voltage on VLIM pin for cycle by cycle current limit		AVDD/2		AVDD/2–0.4	V
I_{LIMIT}	Current limit corresponding to VLIM pin voltage range		0		8	A
I_{LIM_AC}	Current limit accuracy		–10		10	%
t_{BLANK}	Cycle by cycle current limit blank time			5		µs
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	VM rising	4.3	4.4	4.5	V
		VM falling	4.1	4.2	4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling threshold	140	200	350	mV
t_{UVLO}	Supply undervoltage deglitch time		3	5	7	µs
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection (OVP) (SPI Device)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.7	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.3	2.5	2.7	V
		Supply falling	2.2	2.4	2.6	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	75	100	140	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply rising	2.7	2.85	3	V
		Supply falling	2.5	2.65	2.8	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	180	200	240	mV
I_{OCP}	Overcurrent protection trip point (SPI Device)	OCP_LVL = 0b	10	16	20	A
		OCP_LVL = 1b	15	24	28	A
	Overcurrent protection trip point (HW Device)	OCP pin tied to AGND	10	16	21.5	A
		OCP pin tied to AVDD	15	24	31	A

T_J = –40°C to +150°C, V_{VM} = 4.5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.06	0.3	0.7	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.6	1.25	1.8	µs
		OCP_DEG = 11b	1	1.6	2.5	µs
	Overcurrent protection deglitch time (HW Device)		0.06	0.3	0.6	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
t_{RETRY}	Overcurrent protection retry time (HW Device)		4	5	6	ms
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	160	170	180	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD}	Thermal shutdown temperature	Die temperature (T_J)	175	185	195	°C
T_{TSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_J)	25	30	35	°C
T_{TSD_FET}	Thermal shutdown temperature (FET)	Die temperature (T_J)	170	180	190	°C
$T_{TSD\_FET\_HYS}$	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	25	30	35	°C

(1) R_{LBK} is resistance of inductor L_{BK}

7.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			25	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

7.7 SPI Slave Mode Timings

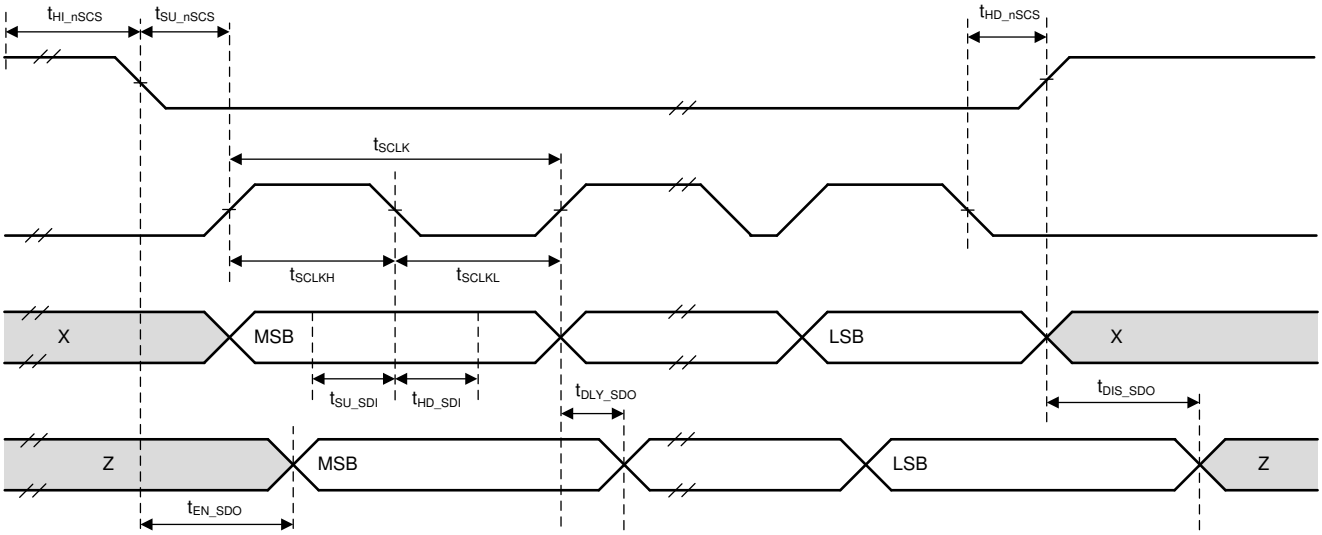


図 7-1. SPI Slave Mode Timings

7.8 Typical Characteristics

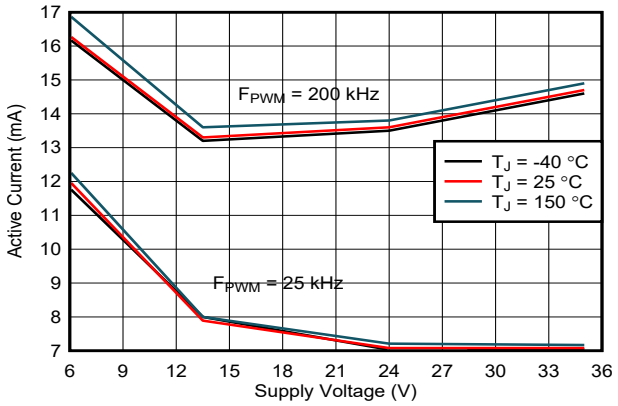


図 7-2. Supply current over supply voltage

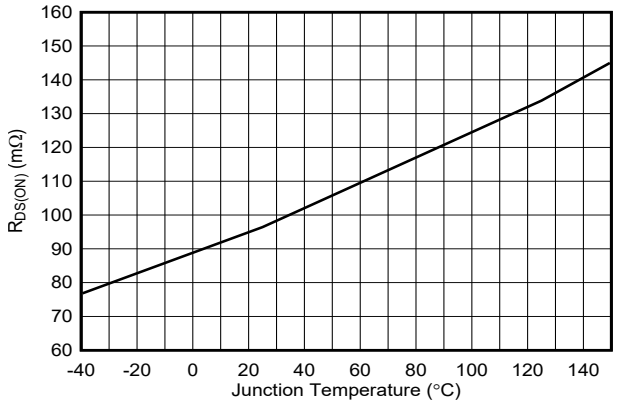


図 7-3. $R_{DS(ON)}$ (high and low side combined) for MOSFETs over temperature

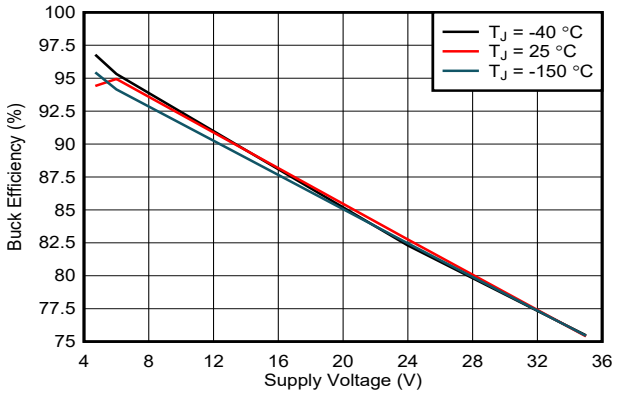


図 7-4. Buck regulator efficiency over supply voltage

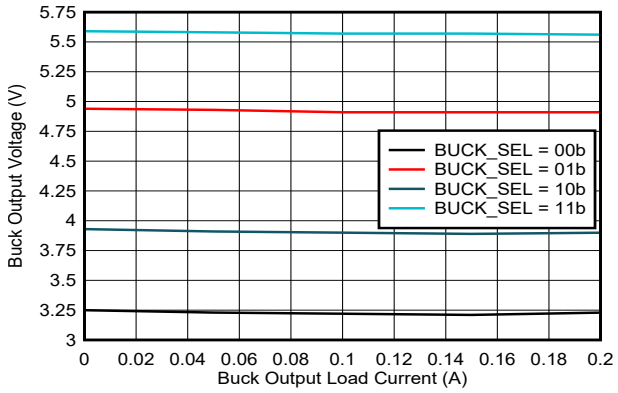


図 7-5. Buck regulator output voltage over load current

8 Detailed Description

8.1 Overview

The DRV8316-Q1 device is an integrated95-mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, charge pump, current sense amplifiers, linear regulator for the external load and buck regulator. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET.

The DRV8316-Q1 device integrates three, bidirectional current-sense amplifiers for monitoring the current level through each of the half-bridges using a built-in current sense. The gain setting of the amplifier can be adjusted through the SPI or hardware interface.

In addition to the high level of device integration, the DRV8316-Q1 device provides a wide range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD undervoltage lockout (AVDD_UV), buck regulator ULVO for DRV8316-Q1 and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The DRV8316R-Q1 and DRV8316T-Q1 device are available in 0.5-mm pin pitch, VQFN surface-mount packages. The VQFN package size is 7 mm × 5 mm.

8.2 Functional Block Diagram

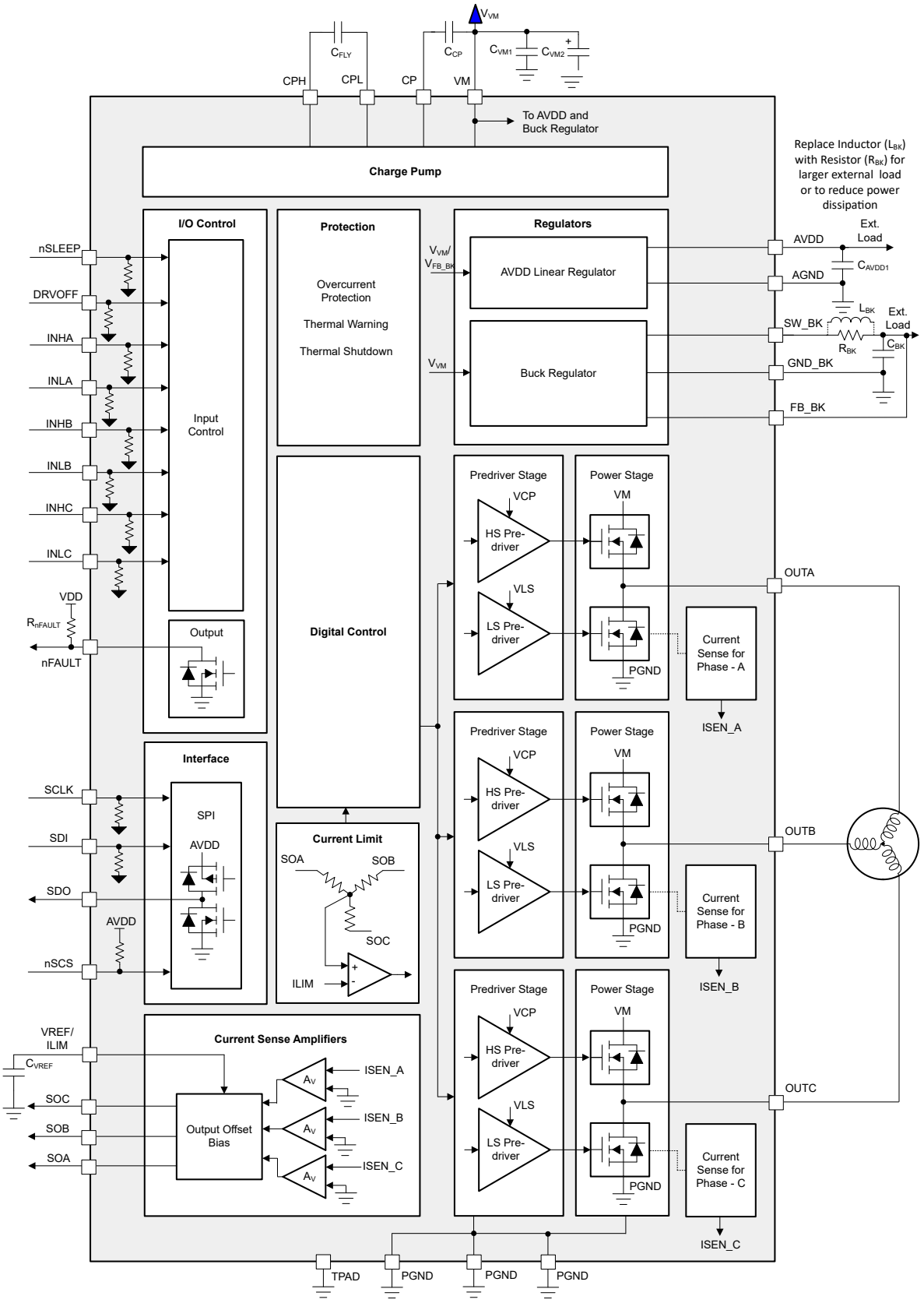


図 8-1. DRV8316R-Q1 Block Diagram

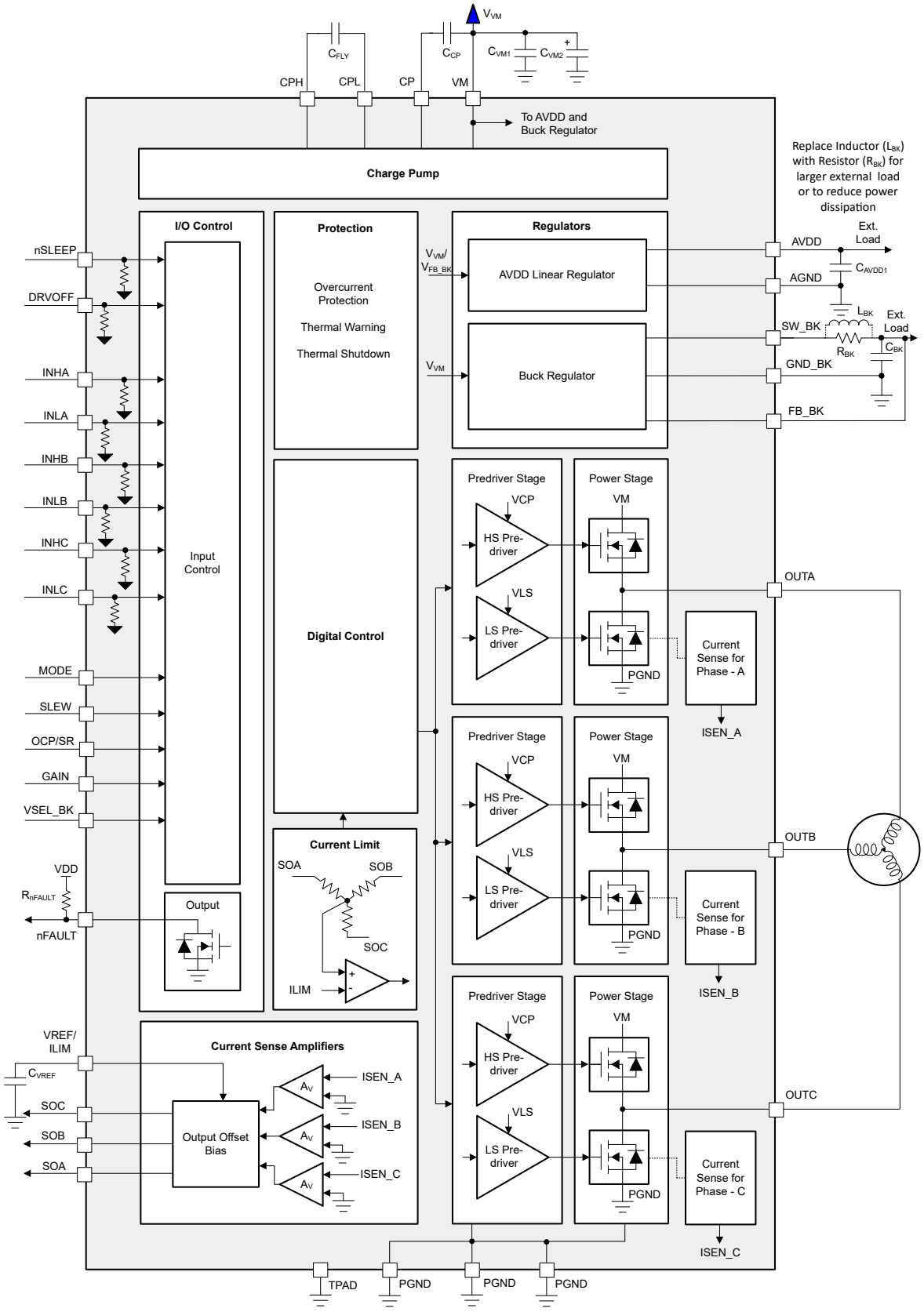


図 8-2. DRV8316T-Q1 Block Diagram

8.3 Feature Description

表 8-1 lists the recommended values of the external components for the driver.

Note

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode. If external supply is used to pull up nFAULT, ensure that it is pulled to >2.2V on power up or the device will enter internal test mode.

表 8-1. DRV8316-Q1 External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, 16-V, 1-µF capacitor
C_{FLY}	CPH	CPL	X5R or X7R, 47-nF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin
C_{AVDD}	AVDD	AGND	X5R or X7R, 1-µF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 1.3-µF at 3.3-V across operating temperature.
C_{BK}	SW_BK	GND_BK	X5R or X7R, 1-µF, ≥ 6.3-V. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 1.3-µF at 3.3-V across operating temperature.
L_{BK}	SW_BK	FB_BK	Output inductor
R_{nFAULT}	VCC	nFAULT	5.1-kΩ, Pullup resistor
R_{MODE}	MODE	AGND or AVDD	DRV8316T-Q1 hardware interface
R_{SLEW}	SLEW	AGND or AVDD	DRV8316T-Q1 hardware interface
R_{OCP}	OCP	AGND or AVDD	DRV8316T-Q1 hardware interface
R_{GAIN}	GAIN	AGND or AVDD	DRV8316T-Q1 hardware interface
R_{VSEL_BK}	VSEL_BK	AGND or AVDD	DRV8316-Q1 hardware interface
C_{VREF}	VREF/ILIM	AGND	X5R or X7R, 0.1-µF, VREF-rated capacitor (Optional)

Note

TI recommends to connect pull up on nFAULT even if it is not used to avoid undesirable entry into internal test mode.

8.3.1 Output Stage

The DRV8316-Q1 device consists of an integrated 95-mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FET's across a wide operating-voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The device has three VM motor power-supply pins which are to be connected together to the motor-supply voltage.

8.3.2 Control Modes

The DRV8316-Q1 family of devices provides four different control modes to support various commutation and control methods. 表 8-2 shows the various modes of the DRV8316-Q1 device.

表 8-2. PWM Control Modes

MODE Type	MODE Pin (Hardware Variant)	PWM_MODE Bits (SPI Variant)	MODE
Mode 1	Connected to AGND	PWM_MODE = 00b	6x Mode
Mode 2	Hi-Z	PWM_MODE = 01b	6x Mode with Current Limit
Mode 3	Connected to AVDD with R_{MODE}	PWM_MODE = 10b	3x Mode
Mode 4	Connected to AVDD	PWM_MODE = 11b	3x Mode with Current Limit

Note

Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set all INHx and INLx pins to logic low before changing the MODE pin or PWM_MODE register.

8.3.2.1 6x PWM Mode (MODE = 00b or MODE Pin Tied to AGND)

In 6x PWM mode, each half-bridge supports three output states: low, high, or high-impedance (Hi-Z). The corresponding INHx and INLx signals control the output state as listed in 表 8-3.

表 8-3. 6x PWM Mode Truth Table

INLx	INHx	PHASEx
0	0	Hi-Z
0	1	H
1	0	L
1	1	Hi-Z

図 8-3 shows the application diagram of DRV8316-Q1 configured in 6x PWM mode.

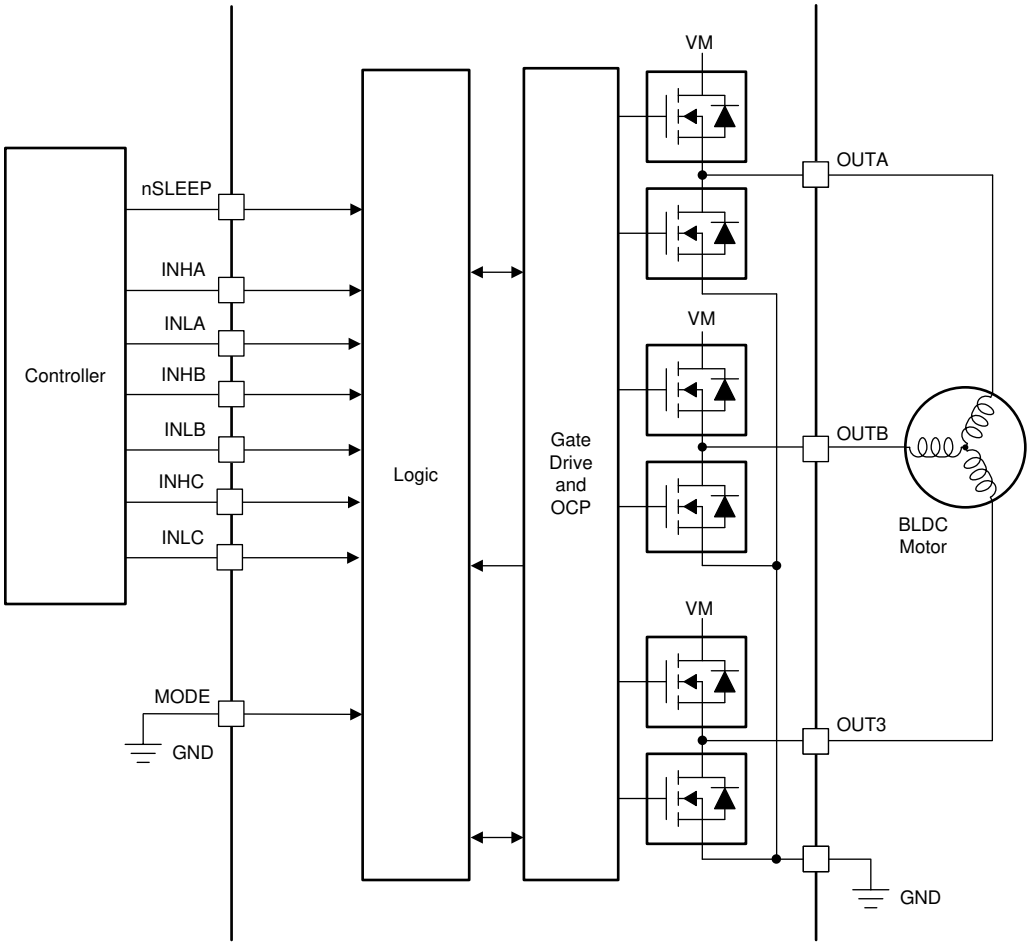


図 8-3. 6x PWM Mode

8.3.2.2 3x PWM Mode (MODE = 10b or MODE Pin is Connected to AGND with R_{MODE})

In 3x PWM mode, the INHx pin controls each half-bridge and supports two output states: low or high. The INLx pin is used to put the half bridge in the Hi-Z state. If the Hi-Z state is not required, tie all INLx pins to logic high. The corresponding INHx and INLx signals control the output state as listed in 表 8-4.

表 8-4. 3x PWM Mode Truth Table

INLx	INHx	PHASEx
0	X	Hi-Z
1	0	L
1	1	H

図 8-4 shows the application diagram of DRV8316-Q1 configured in 3x PWM mode.

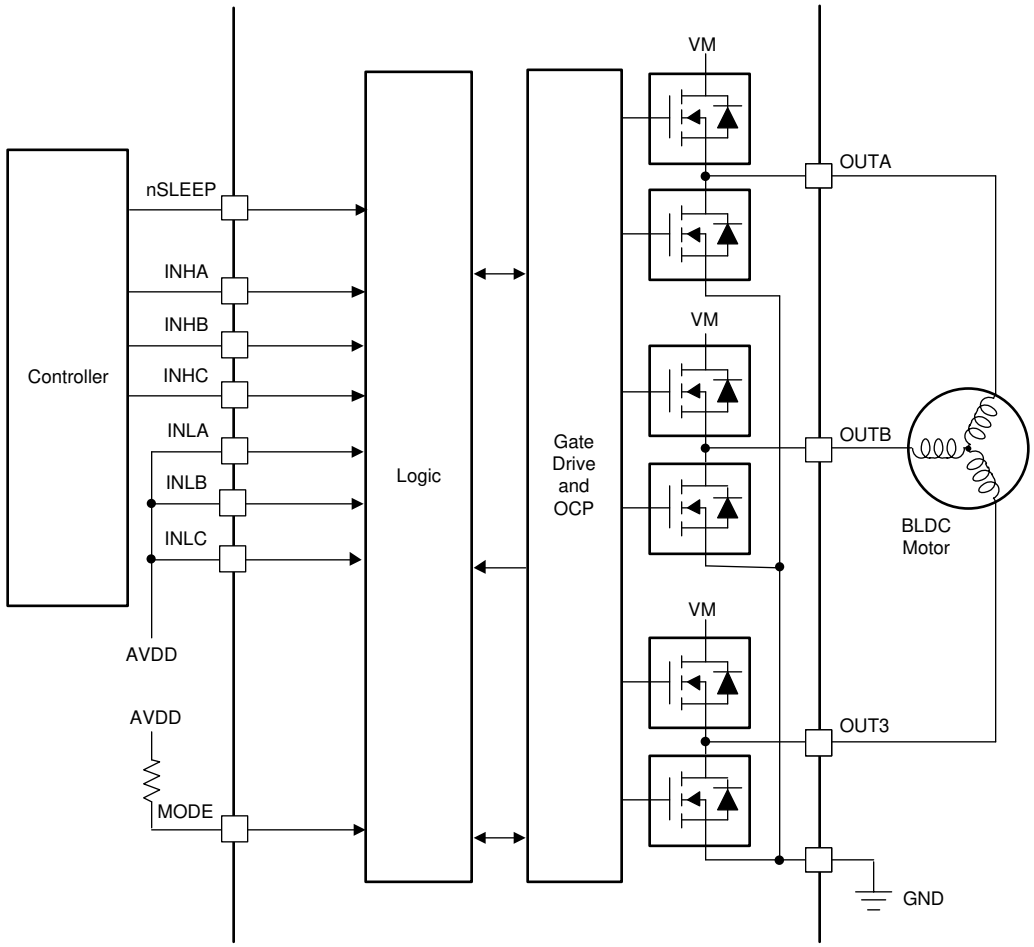


図 8-4. 3x PWM Mode

8.3.2.3 Current Limit Mode (MODE = 01b / 11b or MODE Pin is Hi-Z or Connected to AVDD)

図 8-5 shows the application diagram of DRV8316-Q1 configured in current limit mode. A current limit comparator is used for the current limiting which input is generated with the three current sense amplifier's outputs.

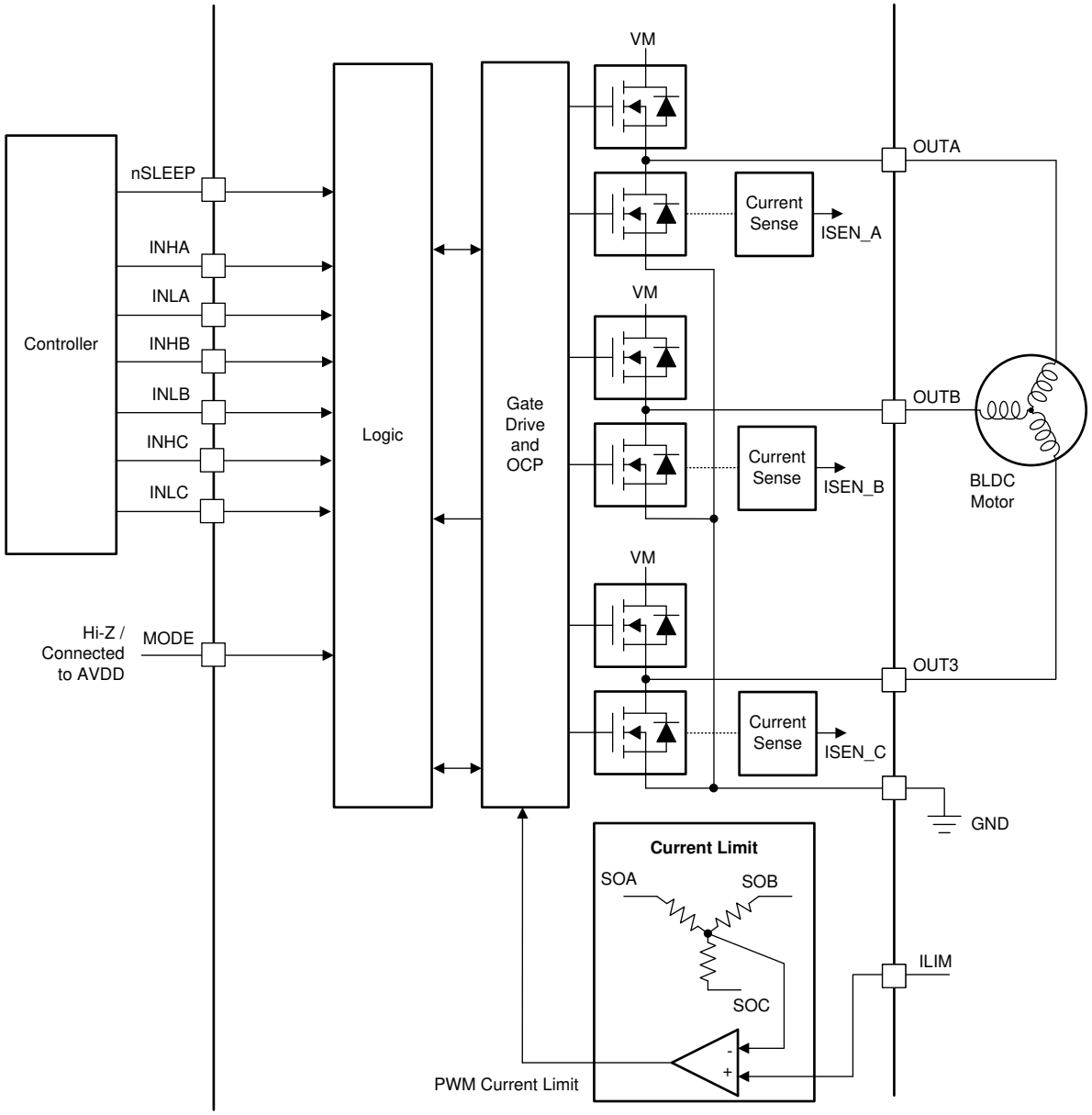


図 8-5. Current Limit Mode

8.3.3 Device Interface Modes

The DRV8316-Q1 family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity. The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design.

8.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the DRV8316-Q1. This support lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin uses an open-drain structure and requires an external pullup resistor.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the DRV8316-Q1.

For more information on the SPI, see the *セクション 8.5* section.

8.3.3.2 Hardware Interface

Hardware interface devices convert the four SPI pins into four resistor-configurable inputs which are GAIN, SLEW, MODE, and OCP.

This conversion lets the application designer configure the most common device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The GAIN pin configures the gain of the current sense amplifier.
- The SLEW pin configures the slew rate of the output voltage.
- The MODE pin configures the PWM control mode.
- The OCP/SR pin is used to configures the OCP level and active demagnetization modes.

For more information on the hardware interface, see the *セクション 8.3.10* section.

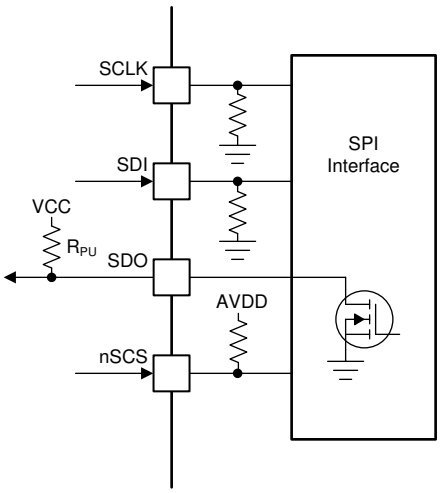


図 8-6. DRV8316R-Q1 SPI Interface

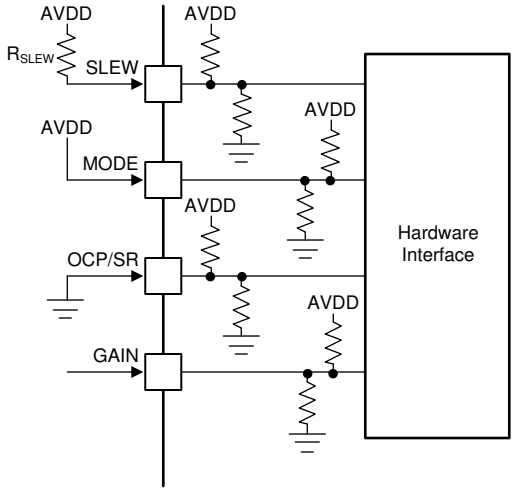


図 8-7. DRV8316T-Q1 Hardware Interface

8.3.4 Step-Down Mixed-Mode Buck Regulator

The DRV8316R-Q1 and DRV8316T-Q1 has an integrated mixed-mode buck regulator in conjunction with AVDD to supply regulated 3.3 V or 5.0 V power for an external controller or system voltage rail. Additionally, the buck output can also be configured to 4.0 V or 5.7 V for supporting the extra headroom for external LDO for generating a 3.3 V or 5.0 V supplies. The output voltage of the buck is set by the VSEL_BK pin in the DRV8316T-Q1 device (hardware variant) and BUCK_SEL bits in the DRV8316R-Q1 device (SPI variant).

The buck regulator has a low quiescent current of ~1-2 mA during light loads to prolong battery life. The device improves performance during line and load transients by implementing a pulse-frequency current-mode control scheme which requires less output capacitance and simplifies frequency compensation design.

To disable the buck regulator, set the BUCK_DIS bit in the DRV8316R-Q1 (SPI variant). The buck regulator cannot be disabled in the DRV8316T-Q1 (hardware variant).

Note

If the buck regulator is unused, the buck pins SW_BK, GND_BK, and FB_BK cannot be left floating or connected to ground. The buck regulator components L_{BK}/R_{BK} and C_{BK} must be connected in hardware.

表 8-5. Recommended settings for Buck Regulator

Buck Mode	Buck output voltage	Max output current from AVDD (I_{AVDD})	Max output current from Buck (I_{BK})	Buck current limit	AVDD power sequencing
Inductor - 47 µH	3.3 V or 4.0 V	30 mA	200 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 47 µH	5.0 V or 5.7 V	30 mA	200 mA - I_{AVDD}	600 mA (BUCK_CL = 0b)	Supported (BUCK_PS_DIS = 0)
Inductor - 22 µH	5.0 V or 5.7 V	30 mA	50 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Inductor - 22 µH	3.3 V or 4.0 V	30 mA	50 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)
Resistor - 22 µH	5.0 V or 5.7 V	30 mA	40 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Not supported (BUCK_PS_DIS = 1)
Resistor - 22 µH	3.3 V or 4.0 V	30 mA	40 mA - I_{AVDD}	150 mA (BUCK_CL = 1b)	Supported (BUCK_PS_DIS = 0)

8.3.4.1 Buck in Inductor Mode

The buck regulator in DRV8316-Q1 device is primarily designed to support low inductance of 47µH and 22µH inductors. The 47µH inductor allows the buck regulator to operate up to 200 mA load current support, whereas the 22µH inductor limits the load current to 50 mA.

図 8-8 shows the connection of buck regulator in inductor mode.

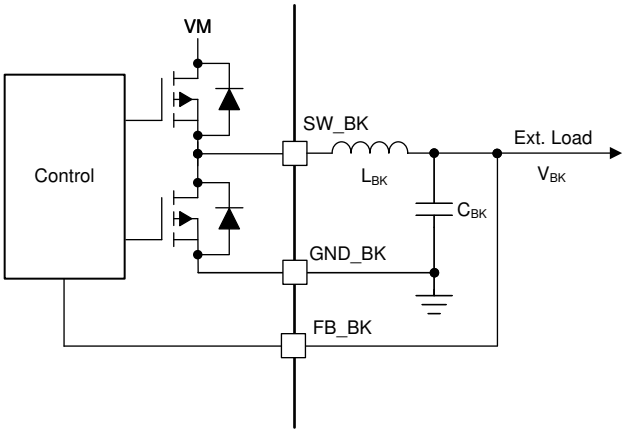


図 8-8. Buck (Inductor Mode)

8.3.4.2 Buck in Resistor mode

If the external load requirements is less than 40mA, the inductor can be replaced with a resistor. In resistor mode the power is dissipated across the external resistor and the efficiency is lower than buck in inductor mode.

図 8-9 shows the connection of buck regulator in resistor mode.

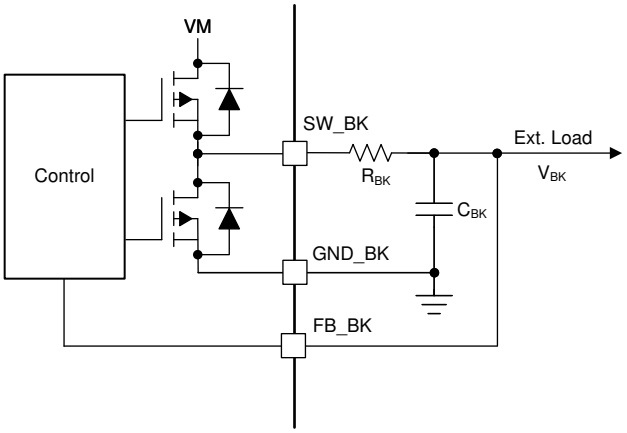


図 8-9. Buck (Resistor Mode)

8.3.4.3 Buck Regulator with External LDO

The buck regulator also supports the voltage requirement to fed to external LDO to generate standard 3.3 V or 5.0 V output rail with higher accuracies. The buck output voltage should be configured to 4 V or 5.5 V to provide for a extra headroom to support the external LDO for generating 3.3 V or 5 V rail as shown in 図 8-10.

This allows for a lower-voltage LDO design to save cost and better thermal management due to low drop-out voltage.

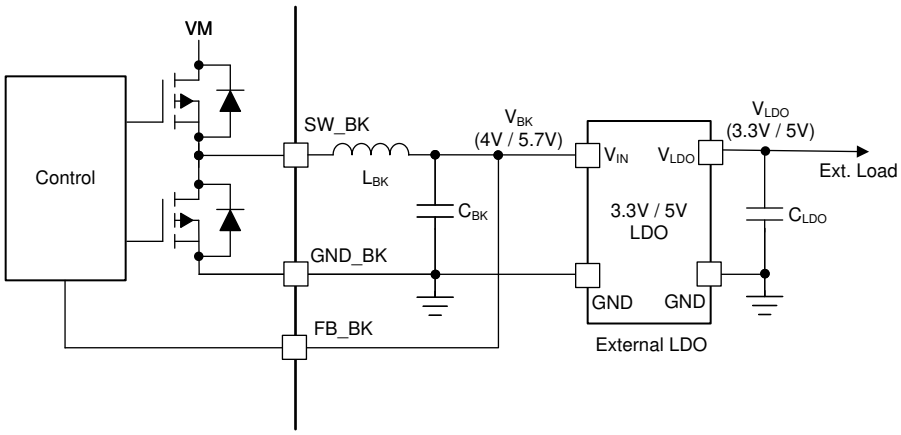


図 8-10. Buck Regulator with External LDO

8.3.4.4 AVDD Power Sequencing on Buck Regulator

The AVDD LDO has an option of using the power supply from mixed mode buck regulator to reduce power dissipation internally. The power sequencing mode allows on-the-fly changeover of LDO power supply from DC mains (VM) to buck output (VBK) as shown in 図 8-11. This sequencing can be configured through the BUCK_PS_DIS bit . Power sequencing is supported only when buck output voltage is set to 5.0 V or 5.7 V.

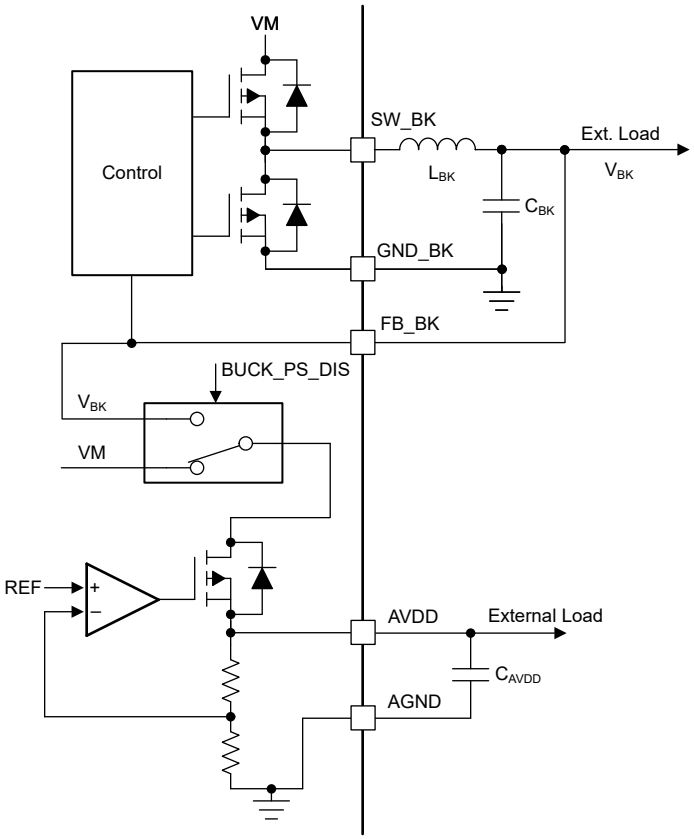


図 8-11. AVDD Power Sequencing on mixed mode Buck Regulator

8.3.4.5 Mixed mode Buck Operation and Control

The buck regulator implements a pulse frequency modulation (PFM) architecture with peak current mode control. The output voltage of the buck regulator is compared with the internal reference voltage (V_{BK_REF}) which is internally generated depending on the buck-output voltage setting (BUCK_SEL) which constitutes an outer voltage control loop. Depending on the comparator output going high ($V_{BK} < V_{BK\_REF}$) or low ($V_{BK} > V_{BK\_REF}$), the high-side power FET of the buck turns on and turn off respectively. An independent current control loop monitors the current in high-side power FET (I_{BK}) and turns off the high-side FET when the current becomes higher than the buck current limit (I_{BK_CL}). This implements a current limit control for the buck regulator. 図 8-12 shows the architecture of the buck and various control/protection loops.

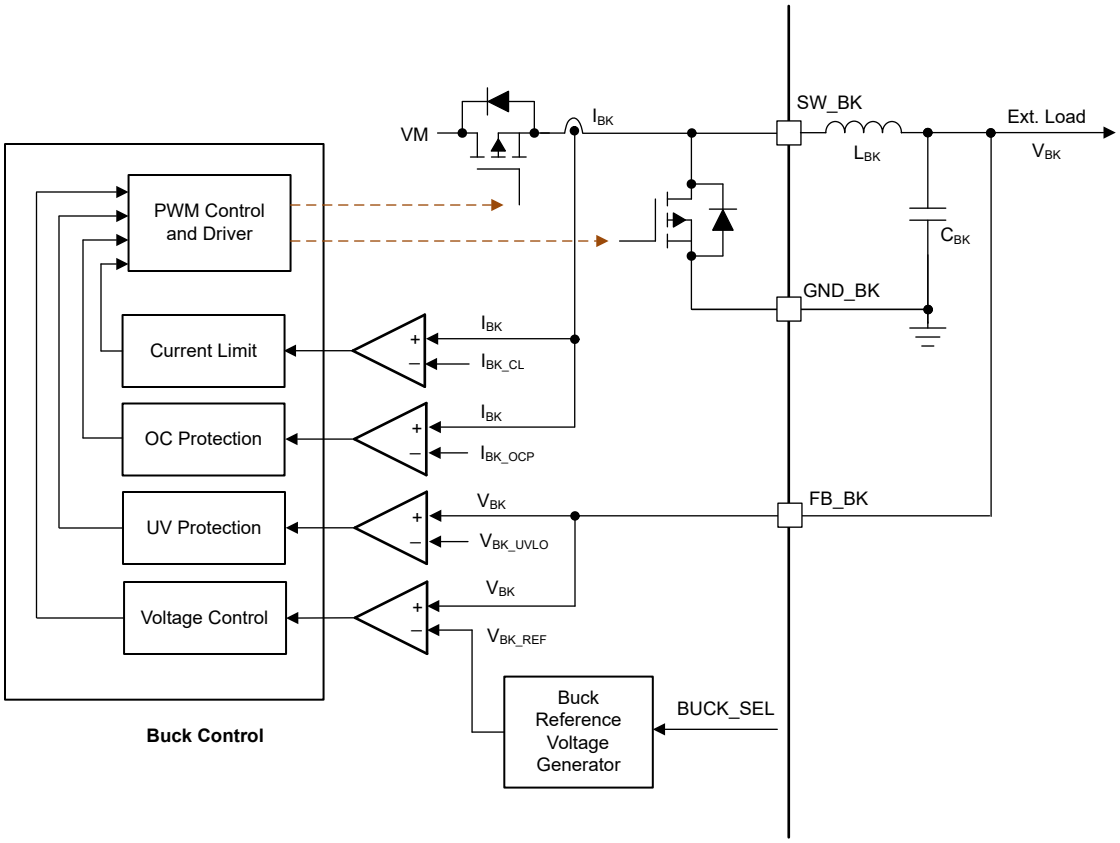


図 8-12. Buck Operation and Control Loops

8.3.4.6 Buck Undervoltage Protection

If at any time the input supply voltage on the FB_BK pin falls lower than the V_{BK_UVLO} threshold, all of the both high-side and low-side MOSFETs of the buck regulator are disabled and the nFAULT pin is driven low. The FAULT, BK_FLT and BUCK_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (buck operation and the nFAULT pin is released) when the VBK undervoltage condition clears. The BUCK_UV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.4.7 Buck Overcurrent Protection

The overcurrent event is sensed by monitoring the current flowing through high-side MOSFET of the buck regulator. If the current across high-side MOSFET exceeds the I_{BK_OCP} threshold for longer than the t_{OCP_DEG} deglitch time, a buck OCP event is recognized and nFAULT pin is driven low. The FAULT, BK_FLT and BK_OCP bits are latched high in the SPI registers. Normal operation starts again automatically (buck operation and the nFAULT pin is released) after the t_{RETRY} time elapses. The FAULT, BK_FLT and BK_OCP bits stay latched until the t_{RETRY} period expires.

On hardware interface devices, the I_{BK_OCP} threshold is set to 600-mA, whereas on SPI devices, the I_{BK_OCP} threshold is set through the BUCK_CL bit to either to 600-mA or 150-mA.

8.3.5 AVDD Linear Voltage Regulator

A 3.3-V, linear regulator is integrated into the DRV8316-Q1 family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30 mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed directly back to the adjacent AGND ground pin.

The AVDD nominal, no-load output voltage is 3.3V.

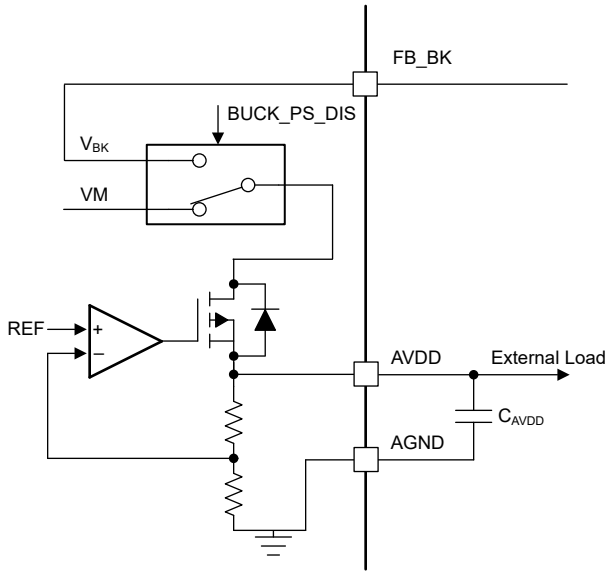


図 8-13. AVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply (BUCK_PD_DIS = 1)

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in a power dissipation as shown in 式 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

Use 式 3 to calculate the power dissipated in the device by the AVDD linear regulator with buck output as supply (BUCK_PD_DIS = 0)

$$P = (V_{FB\_BK} - V_{AVDD}) \times I_{AVDD} \quad (3)$$

8.3.6 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The DRV8316-Q1 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram, pin descriptions and see section (セクション 8.3) for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low.

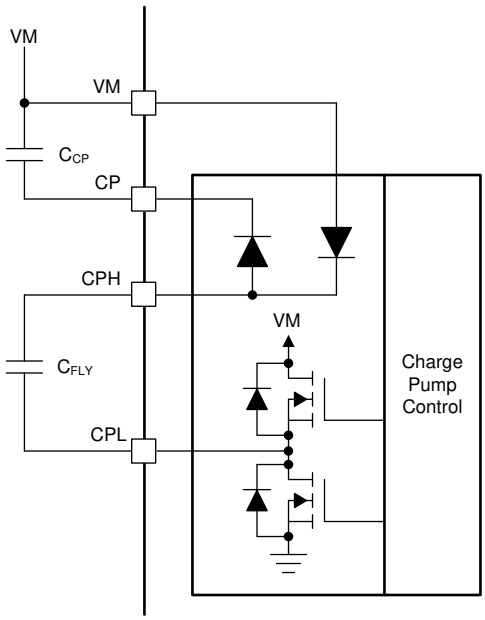


図 8-14. DRV8316-Q1 Charge Pump

8.3.7 Slew Rate Control

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes, and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in 図 8-15.

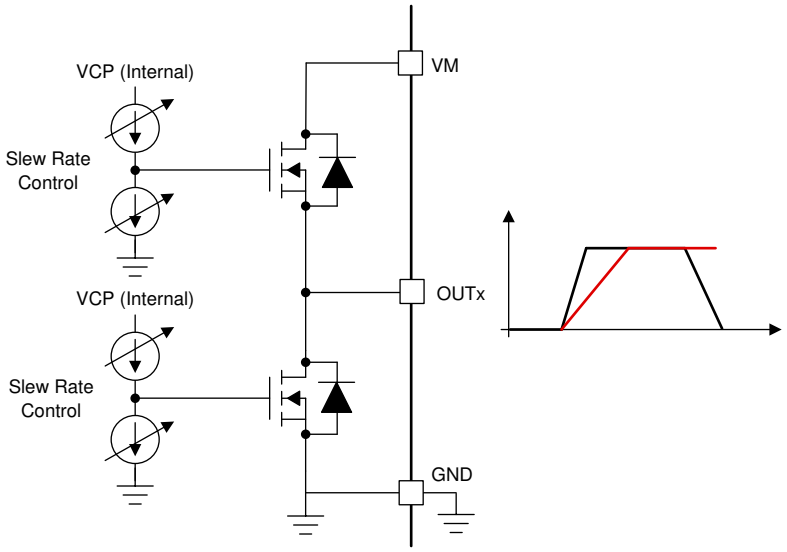


図 8-15. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted by the SLEW pin in hardware device variant or by using the SLEW bits in SPI device variant. Each half-bridge can be selected to either of a slew rate setting of 25-V/µs, 50-V/µs, 125-V/µs or 200-V/µs. The slew rate is calculated by the rise time and fall time of the voltage on OUTx pin as shown in 図 8-16.

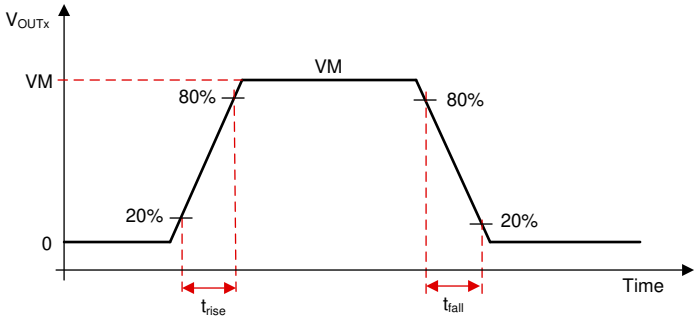


図 8-16. Slew Rate Timings

8.3.8 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (VGS) of the high-side and low-side MOSFETs and ensuring that VGS of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in 図 8-17 and 図 8-18.

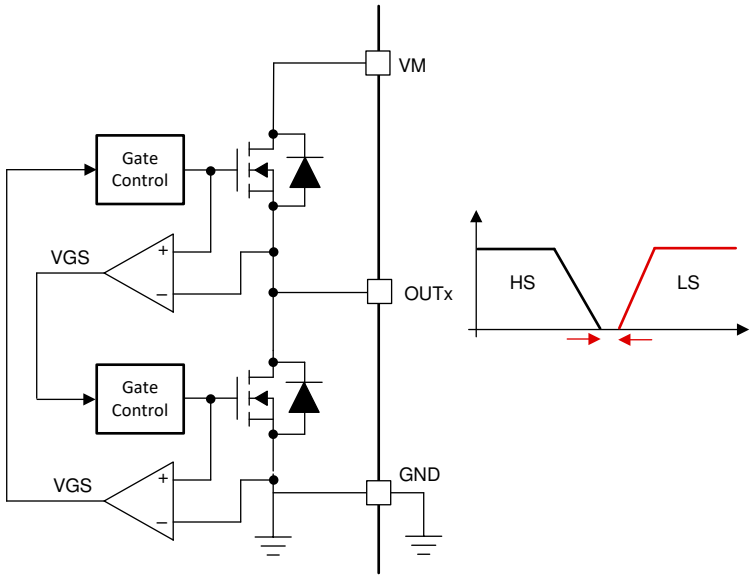


図 8-17. Cross Conduction Protection

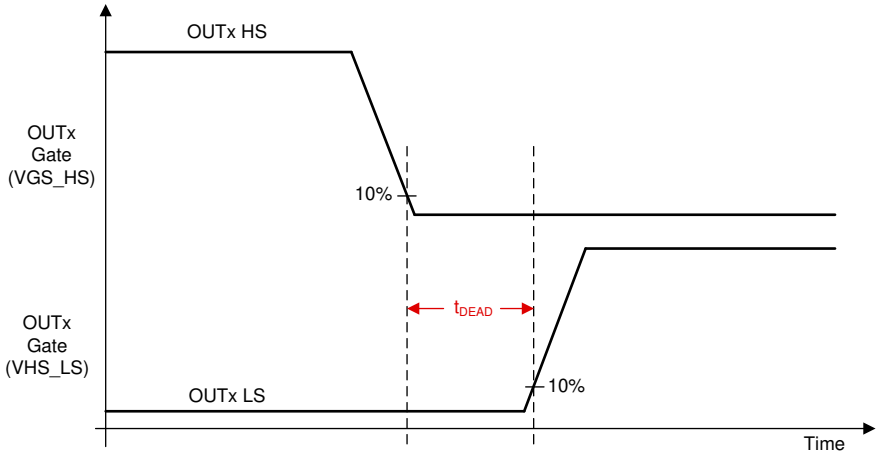


図 8-18. Dead Time

8.3.9 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage. This time has three parts consisting of the digital input deglitcher delay, analog driver, and comparator delay.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

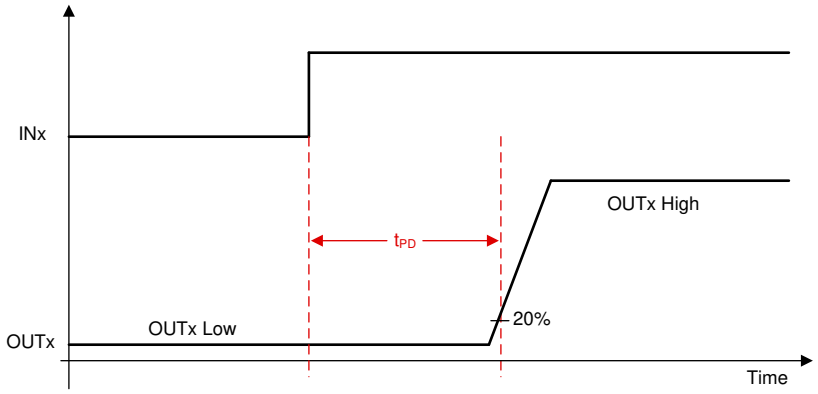


図 8-19. Propagation Delay Timing

8.3.9.1 Driver Delay Compensation

DRV8316-Q1 monitors the prorogation delay internally and adds a variable delay on top of it to provide fixed delay as shown in 図 8-20 and 図 8-21. Delay compensation feature reduces uncertainty caused in timing of current measurement and also reduces duty cycle distortion caused due to propagation delay.

The fixed delay is summation of propagation delay (t_{PD}) caused to internal driver delay and variable delay (t_{VAR}) added to compensate for uncertainty. The fixed delay can be configured through DLY_TARGET register. Refer 表 8-6 for recommendation on configuration for DLY_TARGET for different slew rate settings.

Delay compensation is only available in SPI variant DRV8316R-Q1 and can be enabled by configuring DLYCMP_EN and DLY_TARGET. It is disabled in hardware variant DRV8316T-Q1

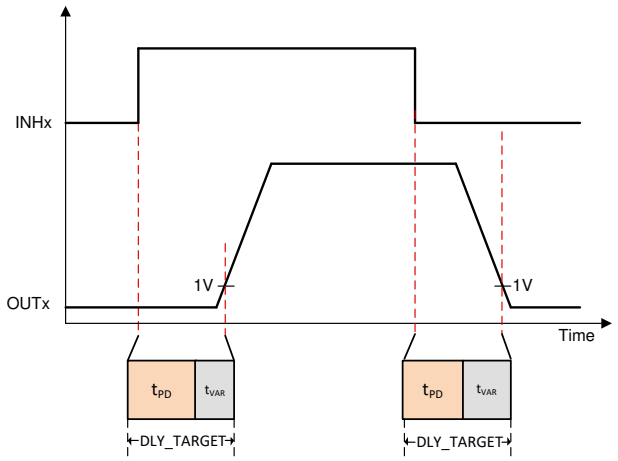


図 8-20. Delay Compensation with current flowing out of phase

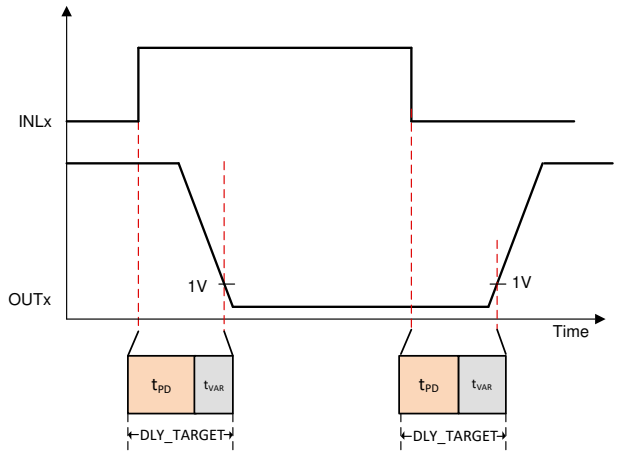


図 8-21. Delay Compensation with current flowing into the phase

表 8-6. Delay Target Recommendation

SLEW RATE	DLY_TARGET
200 V/µs	DLY_TARGET = 0x5 (1.2 µs)
125 V/µs	DLY_TARGET = 0x8 (1.8 µs)
50 V/µs	DLY_TARGET = 0xB (2.4 µs)
25 V/µs	DLY_TARGET = 0xF (3.2 µs)

8.3.10 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

8.3.10.1 Logic Level Input Pin (Internal Pulldown)

図 8-22 shows the input structure for the logic level pins, DRVOFF, INHx, INLx, nSLEEP, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

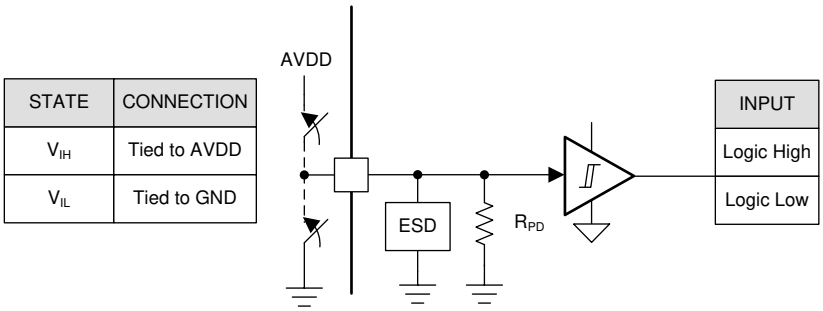


図 8-22. Logic-Level Input Pin Structure

8.3.10.2 Logic Level Input Pin (Internal Pullup)

図 8-23 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

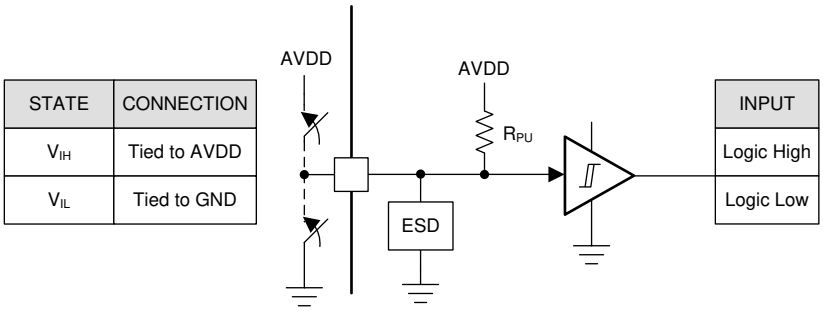


図 8-23. Logic nSCC

8.3.10.3 Open Drain Pin

図 8-24 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function properly.

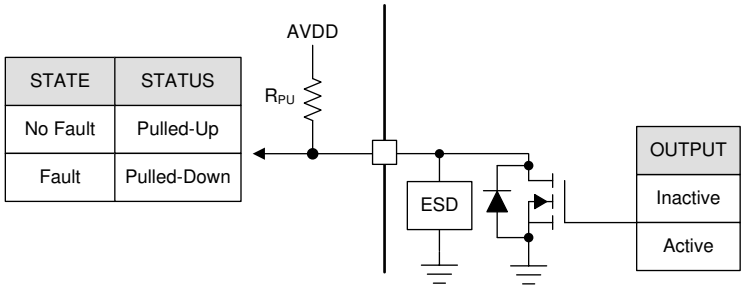


図 8-24. Open Drain

8.3.10.4 Push Pull Pin

図 8-25 shows the structure of push-pull pin, SDO.

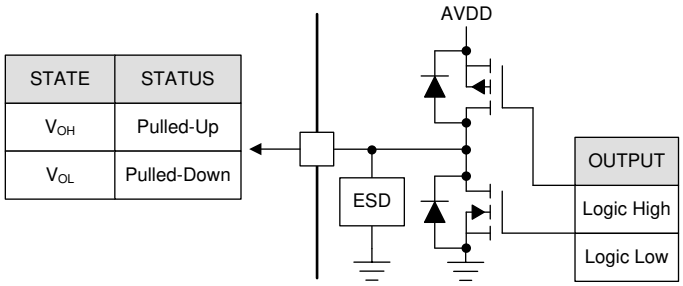


図 8-25. Push Pull

8.3.10.5 Four Level Input Pin

図 8-26 shows the structure of the four level input pins, GAIN, MODE, SLEW, OCP/SR and VSEL_BK on hardware interface devices. The input can be set with an external resistor.

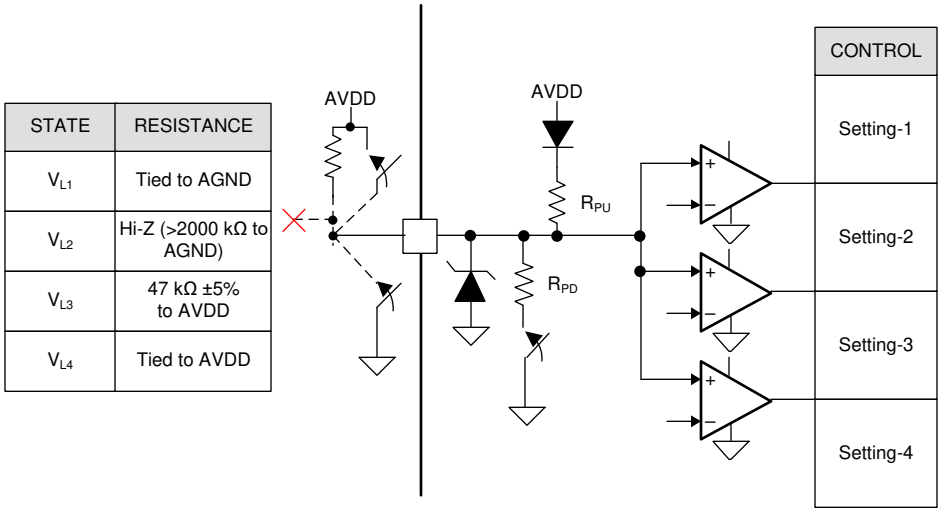


図 8-26. Four Level Input Pin Structure

8.3.11 Current Sense Amplifiers

The DRV8316-Q1 integrates three, high-performance low-side current sense amplifiers for current measurements using built-in current sensing. Low-side current measurements are commonly used to implement overcurrent protection, external torque control, or brushless-DC commutation with an external controller. All three amplifiers can be used to sense the current in each of the half-bridge legs (low-side FETs). The current sense amplifiers include features such as programmable gain and external reference is provided on a voltage reference pin (VREF).

8.3.11.1 Current Sense Amplifier Operation

The SOx pin on the DRV8316-Q1 outputs an analog voltage proportional to current flowing in the low side FETs multiplied by the gain setting (G_{CSA}). The gain setting is adjustable between four different levels which can be set by the GAIN pin (in hardware device variant) or the GAIN bits (in SPI device variant).

図 8-27 shows the internal architecture of the current sense amplifiers. The current sense is implemented with the sense FET on each low-side FET of the DRV8316-Q1 device. This current information is fed to the interal I/V converter, which generates the CSA output voltage on the SOX pin based on the voltage on VREF pin and the Gain setting. The CSA output voltage can be calculated as :

$$SOX = \left({}^{V_{REF}}/_{2}\right) \pm GAIN \times I_{OUTX} \quad (4)$$

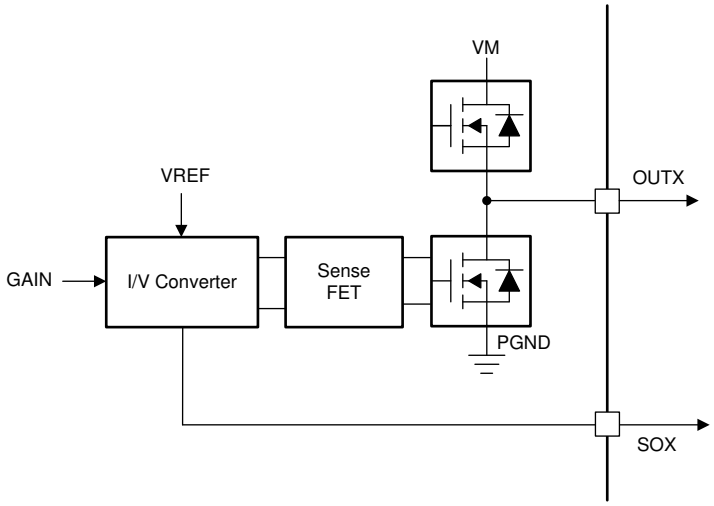


図 8-27. Integrated Current Sense Amplifier

図 8-28 and 図 8-29 show the detail of the amplifier operational range. In bi-directional operation, the amplifier output for 0-V input is set at VREF / 2. Any change in the differential input results in a corresponding change in the output times the CSA_GAIN factor. The amplifier has a defined linear region in which it can maintain operation.

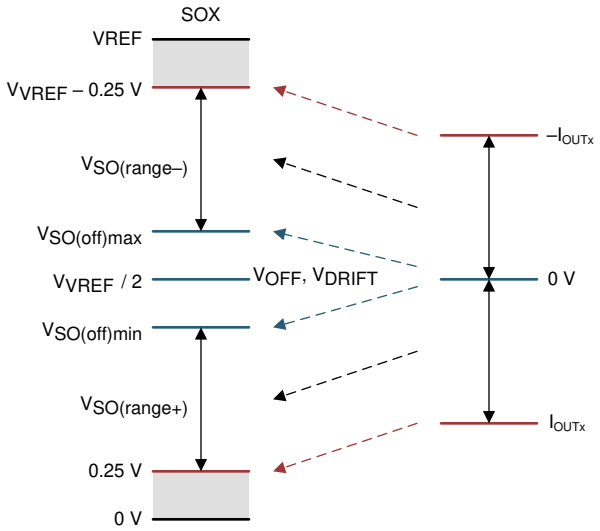


図 8-28. Bidirectional Current Sense Output

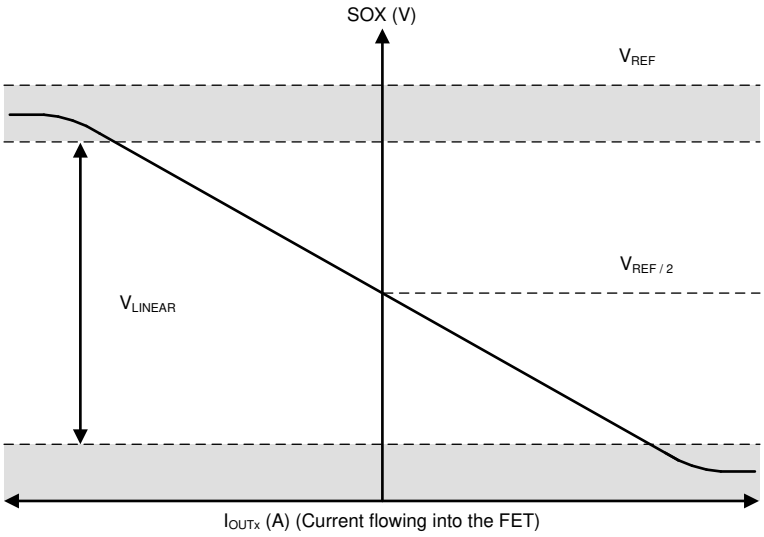


図 8-29. Bidirectional Current Sense Regions

8.3.12 Current Sense Amplifier Offset Correction

CSA output has an offset induced due to ground differences between the sense FET and output FET. When running trapezoidal control or another single-shunt based control (sensored sine, for example) this CSA offset has no impact to operation. When running sensorless sinusoidal or FOC control where two or three current sense are required, some current distortion and noise may occur unless the user implements the corrective action below.

Corrective Action: Implement the below equations in firmware to correct for any current induced offset:

1. When all three current sense amplifiers are used:

$$i_a = 0.995832*i_{a\_sensed} - 0.028199*i_{b\_sensed} - 0.014988*i_{c\_sensed} \quad (5)$$

$$i_b = 0.037737*i_{a_{sensed}} + 1.007723*i_{b\_sensed} - 0.033757*i_{c\_sensed} \quad (6)$$

$$i_c = 0.009226*i_{a_{sensed}} + 0.029805*i_{b_{sensed}} + 1.003268*i_{c\_sensed} \quad (7)$$

2. When only two of the three current sense amplifiers are used:
   a. Current sensed in phases A & B:

$$i_a = 1.013075*i_{a\_sensed} - 0.01236*i_{b\_sensed} \quad (8)$$

$$i_a = 1.013075*i_{a\_sensed} - 0.01236*i_{b\_sensed} \quad (9)$$

$$i_c = -(i_a + i_b) \quad (10)$$

   b. Current sensed in phases B & C:

$$i_b = 0.971197*i_{b\_sensed} - 0.0683*i_{c\_sensed} \quad (11)$$

$$i_c = 0.020876*i_{b_{sensed}} + 0.994823*i_{c\_sensed} \quad (12)$$

$$i_a = -(i_b + i_c) \quad (13)$$

   c. Current sensed in phases C & A:

$$i_a = 1.025489*i_{a_{sensed}} + 0.011936*i_{c\_sensed} \quad (14)$$

$$i_c = 0.022043*i_{a_{sensed}} + 0.996548*i_{c\_sensed} \quad (15)$$

$$i_b = -(i_a + i_c) \quad (16)$$

8.3.13 Active Demagnetization

DRV8316-Q1 family of devices has smart rectification features (active demagnetization) which reduces power losses in device by reducing diode conduction losses. When this feature is enabled device automatically turns ON FET whenever it detects diode conduction. This feature can be configured with the OCP/SR pins in hardware variants. In SPI device variants this can be configured through EN_ASR and EN_AAR bits. The smart rectification is classified into two categories of automatic synchronous rectification (ASR) mode and automatic asynchronous rectification (AAR) mode which are described in sections below.

Note

In SPI device variants both bits, EN_ASR and EN_AAR needs to set to 1 to enable active demagnetization.

The DRV8316-Q1 device includes a high-side (AD_HS) and low-side (AD_LS) comparator which detects the negative flow of current in the device on each half-bridge. The AD_HS comparator compares the sense-FET output with the supply voltage (VM) threshold, whereas the AD_LS compatator compares with the ground (0-V) threshold. Depending upon the flow of current from OUTx to VM or PGND to OUTx, the AD_HS or the AD_LS comparator trips. This comparator provides a reference point for the operation of active demagnetization feature.

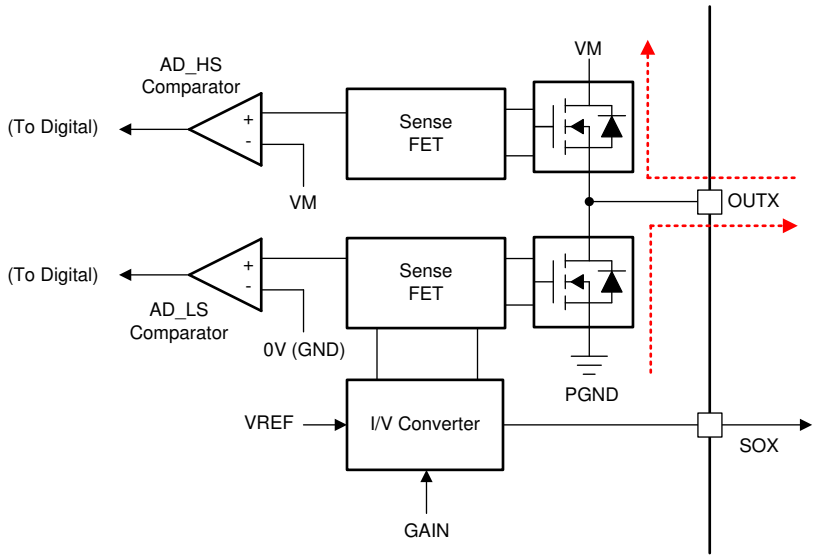


図 8-30. Active Demagnetization Operation

表 8-7 shows the configuration of ASR and AAR mode in the DRV8316-Q1 device.

表 8-7. PWM_MODE Configuration

MODE Type	OCP/SR Pin (Hardware Variant)	SR Bits (SPI Variant)	OCP Setting	ASR and AAR Mode
Mode 1	Connected to AGND	EN_ASR = 0, EN_AAR = 0	16 A	ASR and AAR Disabled
Mode 2	Connected to AGND with R_{MODE1}	EN_ASR = 0, EN_AAR = 0	24 A	ASR and AAR Disabled
Mode 3	Hi-Z	EN_ASR = 1, EN_AAR = 1	16 A	ASR and AAR Enabled
Mode 4	Connected to AVDD	EN_ASR = 1, EN_AAR = 1	24 A	ASR and AAR Enabled

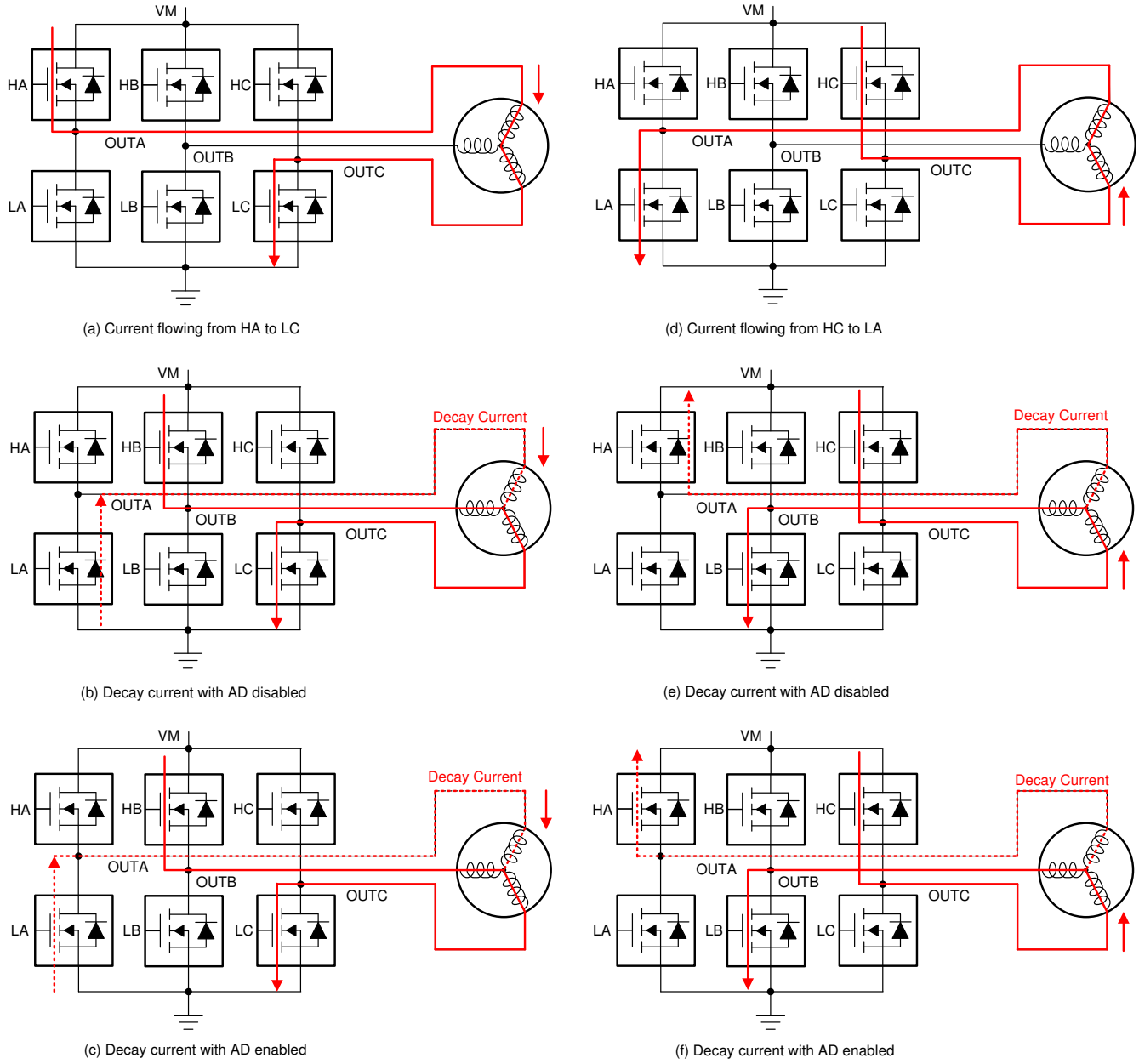
8.3.13.1 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode is divided into two categories of ASR during commutation and ASR during PWM mode.

8.3.13.1.1 Automatic Synchronous Rectification in Commutation

図 8-31 shows the operation of active demagnetization during the BLDC motor commutation. As shown in 図 8-31 (a), the current is flowing from HA to LC in one commutation state. During the commutation changeover as shown in 図 8-31 (b), the HC switch is turned on, whereas the commutation current (due to motor inductance) in OUTA flows through the body diode of LA. This incorporates a higher diode loss depending on the commutation current. This commutation loss is reduced by turning on the LA for the commutation time as shown in 図 8-31 (c).

Similarly the operation of high-side FET is realized in 図 8-31 (d), (e) and (f).



(a) Current flowing from HA to LC

(d) Current flowing from HC to LA

(b) Decay current with AD disabled

(e) Decay current with AD disabled

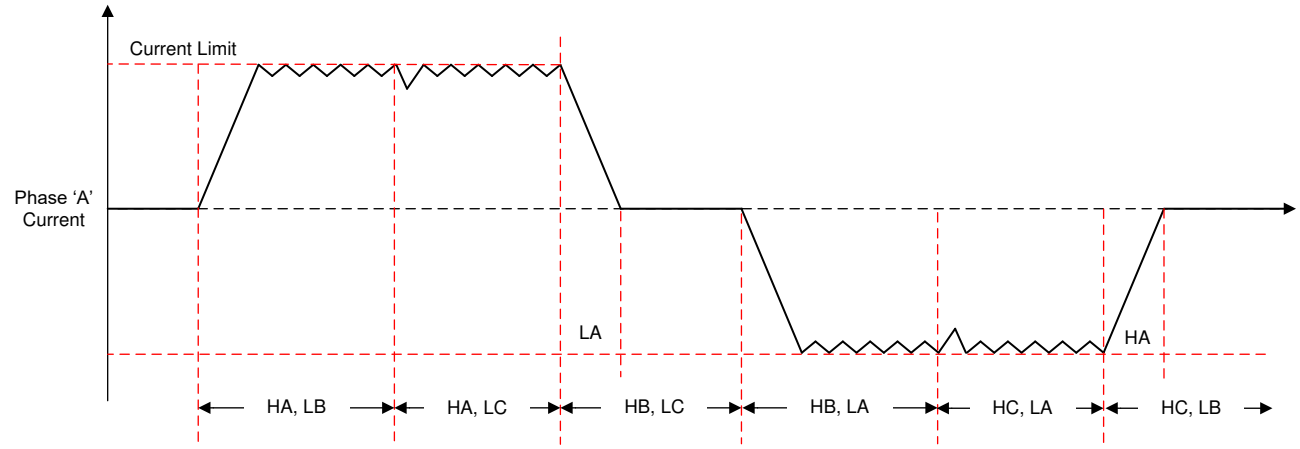
(c) Decay current with AD enabled

(f) Decay current with AD enabled

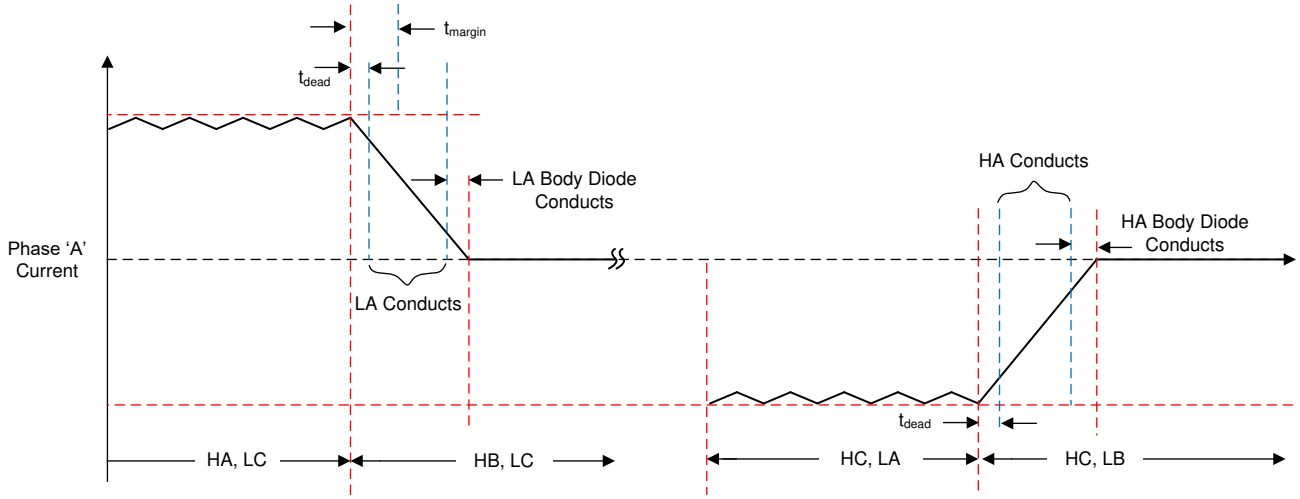
図 8-31. ASR in BLDC Motor Commutation

図 8-32 (a) shows the BLDC motor phase current waveforms for automatic synchronous rectification mode in BLDC motor operating with trapezoidal commutation. This figure shows the operation of various switches in a single commutation cycle.

図 8-32 (b) shows the zoomed waveform of commutation cycle with details on the ASR mode start with margin time (t_{margin}) and ASR mode early stop due to active demag. comparator threshold and delays.



(a) Commutation current of Phase "A"



(b) Zoomed waveform of Active Demagnetization

図 8-32. Current Waveforms for ASR in BLDC Motor Commutation

8.3.13.1.2 Automatic Synchronous Rectification in PWM Mode

図 8-33 shows the operation of ASR in PWM mode. As shown in this figure, a PWM is applied only on the high-side FET, whereas the low-side FET is always off. During the PWM off time, current decays from the low-side FET which results in higher power losses. Therefore, this mode supports turning on the low-side FET during the low-side diode conduction.

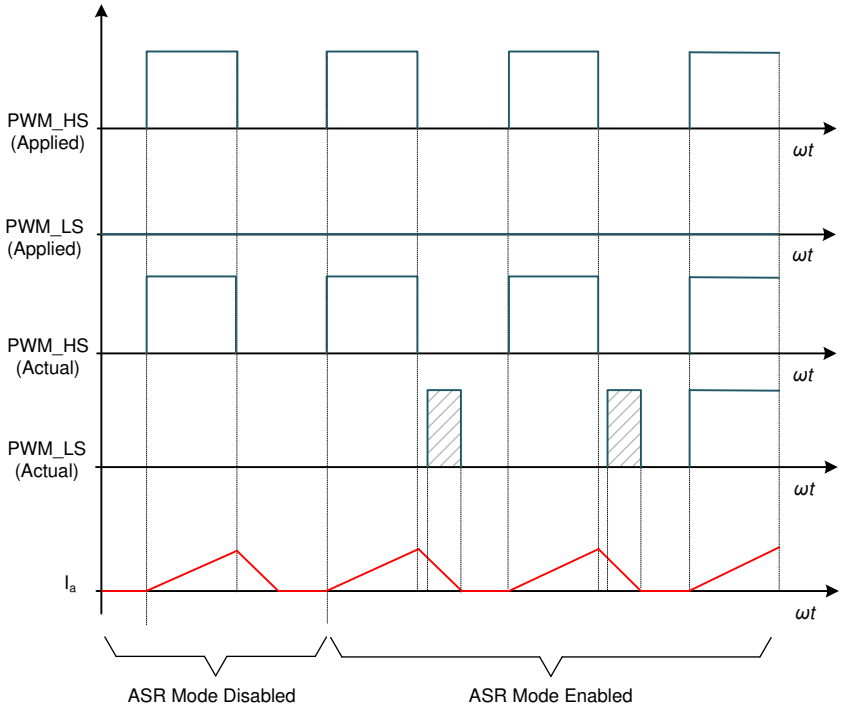


図 8-33. ASR in PWM Mode

8.3.13.2 Automatic Asynchronous Rectification Mode (AAR Mode)

図 8-34 shows the operation of AAR in PWM mode. As shown in this figure, a PWM is applied in a synchronous rectification to the high-side and low-side FETs. During the low-side FET conduction, for lower inductance motors, the current can decay to zero and becomes negative since low side FET is in on-state. This creates a negative torque on the BLDC motor operation. When AAR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management.

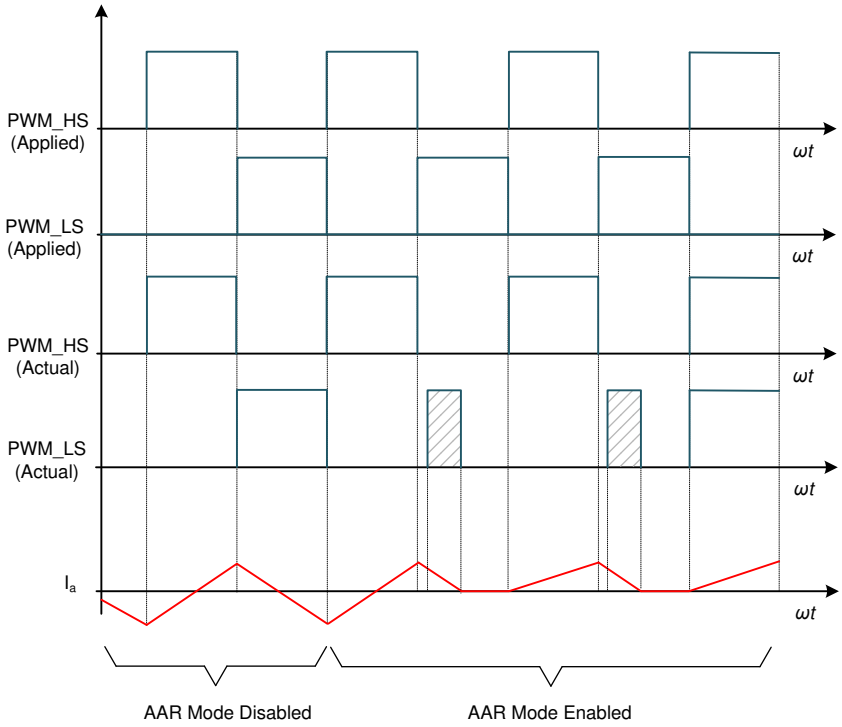


図 8-34. AAR in PWM Mode

8.3.14 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFET exceeds the I_{LIMIT} current. This feature restricts motor current to less than the I_{LIMIT}.

The current-limit circuitry utilizes the current sense amplifier output of the three phases compared with the voltage at ILIM pin. 図 8-35 shows the implementation of current limit circuitry. As shown in this figure, the output of current sense amplifiers is combined with star connected resistive network. This measured voltage V_{MEAS} is compared with the external reference voltage e V_{ILIM} pin to realize the current limit implementation. The relation between current sensed on OUTX pin and V_{MEAS} threshold is given as:

$$V_{MEAS} = \left({}^{V_{AVDD}}/_{2}\right) - \left((I_{OUTA} + I_{OUTB} + I_{OUTC}) \times GAIN/3\right) \quad (17)$$

where

- AVDD is 3.3-V LDO output
- OUTX is current flowing into the low-side MOSFET
- GAIN is the CSA_GAIN setting

The I_{LIMIT} threshold can be adjusted by configuring ILIM pin between AVDD/2 to (AVDD/2 - 0.4) V. AVDD/2 is minimum value and when it is applied on ILIM pin cycle by cycle current limit is disabled, whereas maximum threshold of 8A can be configured by applying (AVDD/2 - 0.4) V on ILIM pin.

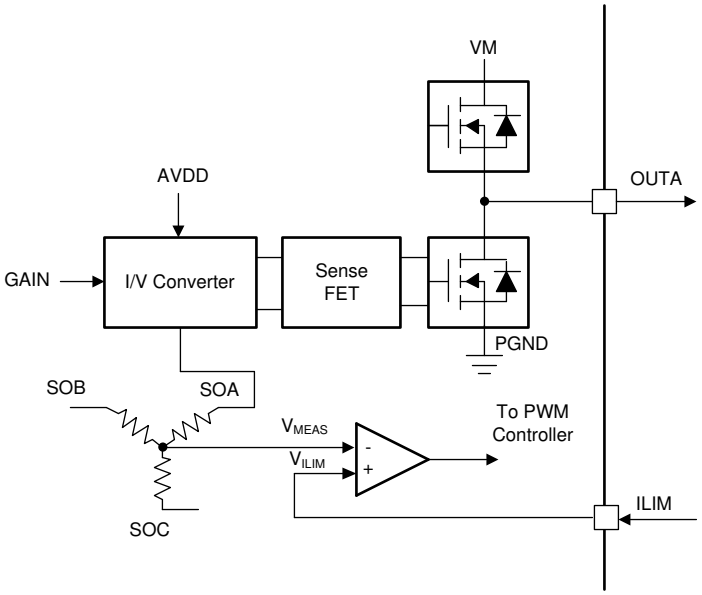


図 8-35. Current Limit Implementation

When then the current limit activates, the high-side FET is disabled until the beginning of the next PWM cycle as shown in 図 8-36. The low-side FETs can operate in brake mode or high-Z mode by configuring the ILIM_RECIR bit in the SPI device variant.

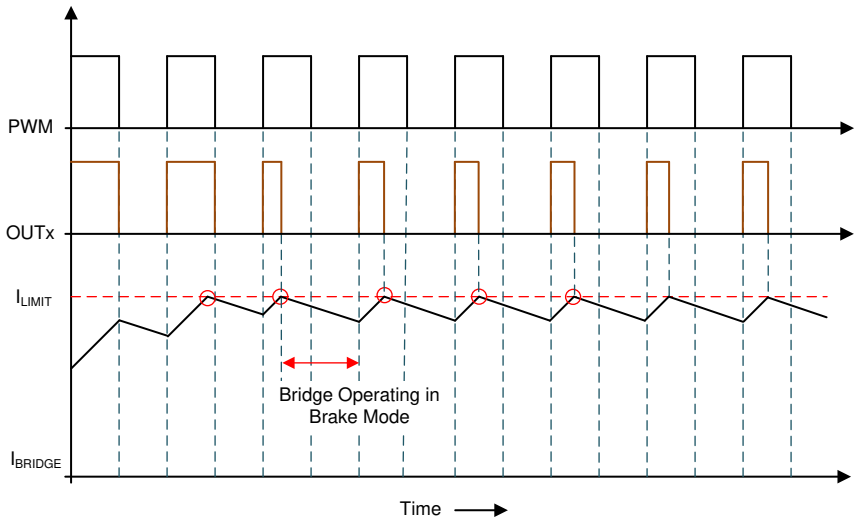


図 8-36. Cycle-by-Cycle Current-Limit Operation

図 8-37 shows the operation of driver in brake mode, where the current recirculates through low-side FETs while the high-side FETs are disabled.

図 8-38 shows the operation of driver in hi-Z mode, where the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled.

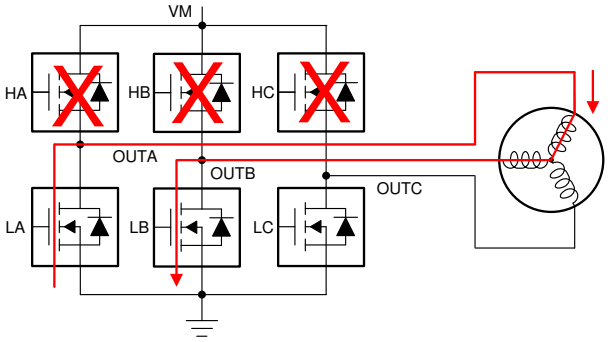


図 8-37. Brake State

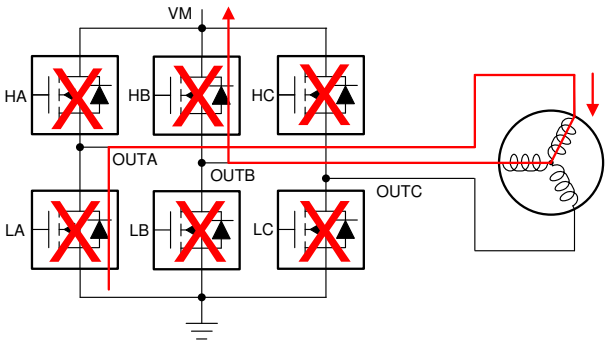


図 8-38. Coast State

Note

The current-limit circuit is ignored immediately after the PWM signal goes active for a short blanking time to prevent false trips of the current-limit circuit.

Note

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

8.3.14.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, DRV8316-Q1 has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant DRV8316R-Q1, this internal PWM clock can

be configured to either 20 kHz or 40 kHz through PWM_100_DUTY_SEL. In H/W variant DRV8316T-Q1 PWM internal clock is set to 20 kHz. 図 8-39 shows operation with 100 % duty cycle.

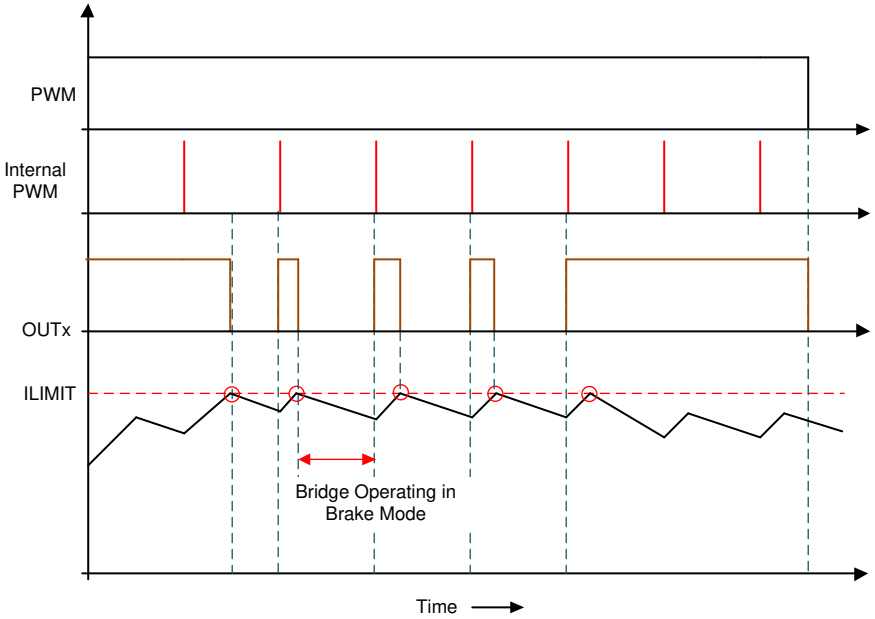


図 8-39. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

8.3.15 Protections

The DRV8316-Q1 family of devices is protected against VM undervoltage, charge pump undervoltage, and overcurrent events. 表 8-8 summarizes various faults details.

表 8-8. Fault Action and Response (SPI Devices)

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (NPOR)	$V_{VM} < V_{UVLO}$	—	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
AVDD undervoltage (NPOR)	$V_{AVDD} < V_{AVDD\_UV}$	—	nFAULT	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
Buck undervoltage (BUCK_UV)	$V_{FB\_BK} < V_{BK\_UV}$	—	nFAULT	Active	Active	Automatic: $V_{FB\_BK} > V_{BUCK\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (BUCK_UV bit)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	—	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
OverVoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
Buck Overcurrent Protection (BUCK_OCP)	$I_{BK} > I_{BK\_OC}$	—	nFAULT	Active	Active	Retry: t_{RETRY}
SPI Error (SPI_FLT)	SCLK fault and ADDR fault	SPI_FLT_REP = 0b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
		SPI_FLT_REP = 1b	None	Active	Active	No action
OTP Error (OTP_ERR)	OTP reading is erroneous	—	nFAULT	Hi-Z	Active	Latched: Power Cycle, nSLEEP Reset Pulse
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD)	$T_J > T_{TSD}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD} - T_{TSD\_HYS}$ CLR_FLT, nSLEEP Pulse (OTS bit)
Thermal shutdown (OTSD_FET)	$T_J > T_{TSD\_FET}$	—	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD\_FET} - T_{TSD\_FET\_HYS}$ CLR_FLT, nSLEEP Pulse (OTS bit)

8.3.15.1 VM Supply Undervoltage Lockout (NPOR)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in 図 8-40. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

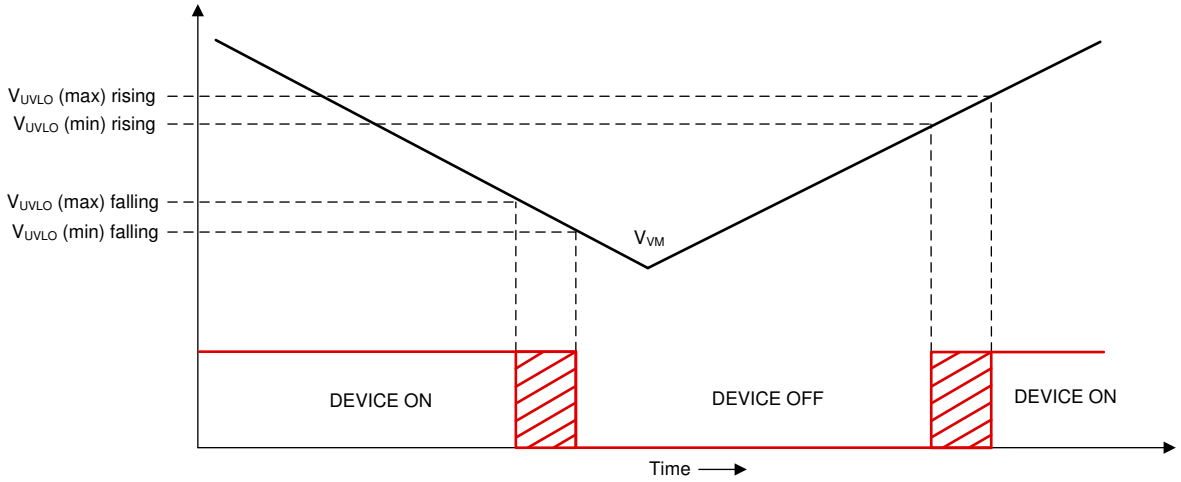


図 8-40. VM Supply Undervoltage Lockout

8.3.15.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.15.3 BUCK Undervoltage Lockout (BUCK_UV)

If at any time the voltage on VFB_BK pin falls lower than the V_{BK_UV} threshold, the integrated FETs of the buck regulator are disabled while the driver FETs, charge pump, and digital logic control continue to operate normally. The nFAULT pin is driven low in the event of a buck undervoltage fault, and the BK_FLT bit in IC_STAT register is set in SPI devices. The FAULT and BUCK_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (buck regulator operation and the nFAULT pin is released) when the BUCK undervoltage condition clears. The BK_FLT and BUCK_UV bits stay set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

8.3.15.4 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and VCP_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

8.3.15.5 Overvoltage Protections (OV)

If at any time input supply voltage on the VM pins rises higher lower than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and OVP bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin

reset pulse (t_{RST}). Setting the OVP_EN bit high on the SPI devices enables this protection feature. On hardware interface devices, the OVP protection is always enabled and set to a 34-V threshold.

The OVP threshold is also programmable on the SPI device variant. The OVP threshold can be set to 20-V or 32-V based on the OVP_SEL bit.

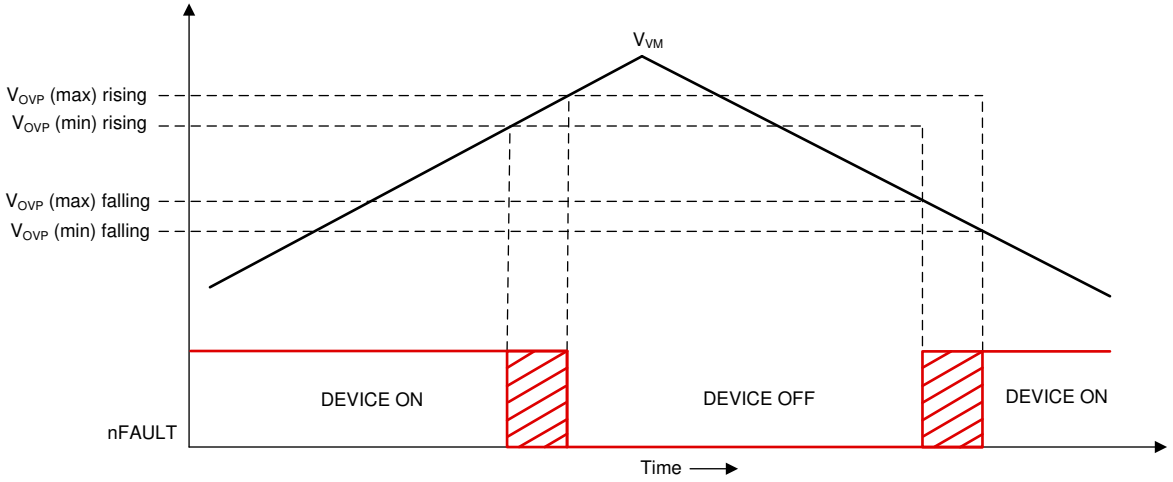


図 8-41. Over Voltage Protection

8.3.15.6 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. On hardware interface devices, the I_{OCP} threshold is set via OCP/SR pin, the t_{OCP_DEG} is fixed at 0.6-µs, and the OCP_MODE bit is configured for latched shutdown. On SPI devices, the I_{OCP} threshold is set through the OCP_LVL SPI register, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

8.3.15.6.1 OCP Latched Shutdown (OCP_MODE = 00b)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

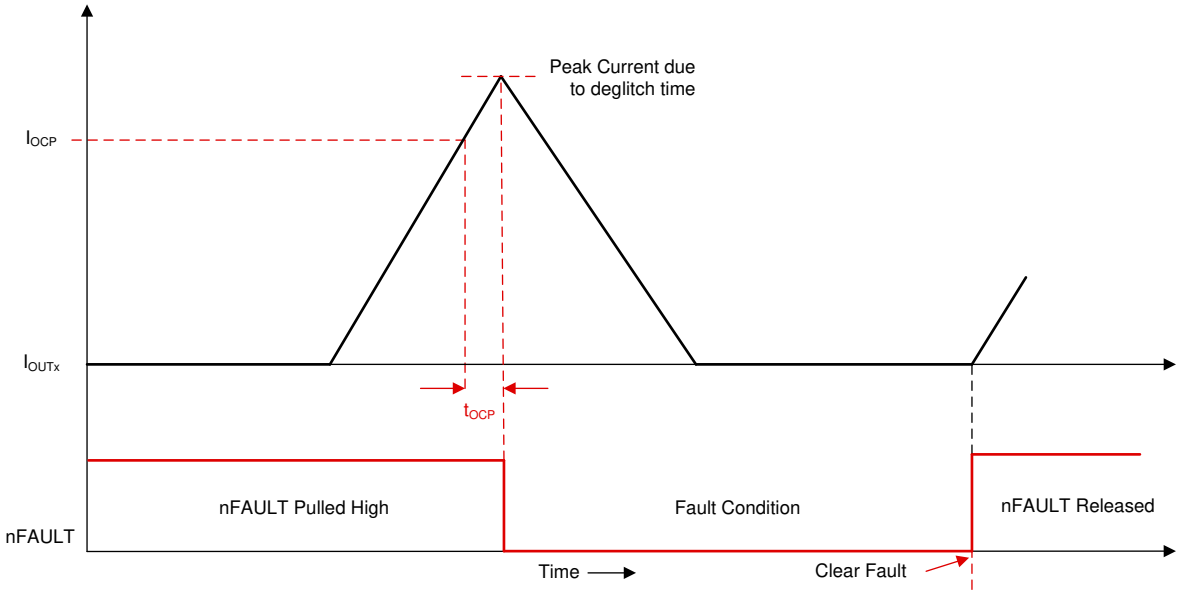


図 8-42. Overcurrent Protection - Latched Shutdown Mode

8.3.15.6.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

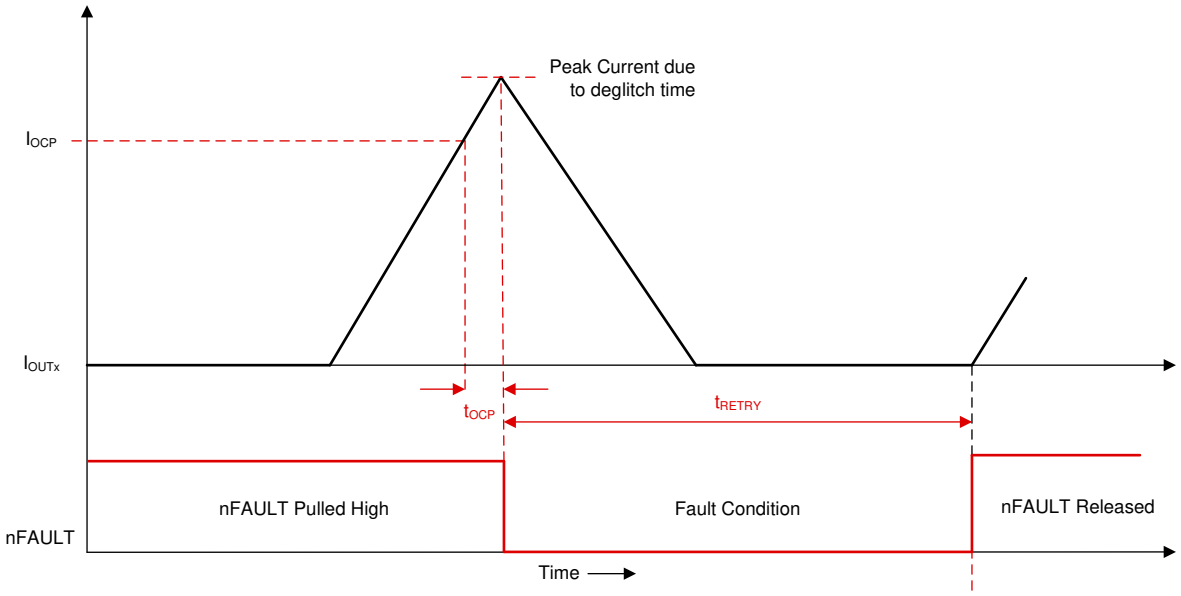


図 8-43. Overcurrent Protection - Automatic Retry Mode

8.3.15.6.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The DRV8316-Q1 continues to operate as usual. The external controller manages the overcurrent condition by acting

appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

8.3.15.6.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

8.3.15.7 Buck Overcurrent Protection

A buck overcurrent event is sensed by monitoring the current flowing through buck regulator's FETs. If the current across the buck regulator FET exceeds the I_{BK_OCP} threshold for longer than the t_{BK_OCP} deglitch time, an OCP event is recognized. The buck OCP mode is configured in automatic retry setting. In this setting, after a buck OCP event is detected, all the buck regulator's FETs are disabled and the nFAULT pin is driven low. The FAULT, BK_FLT, and BUCK_OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{BK_RETRY} time elapses. The FAULT, BK_FLT, and BUCK_OCP bits stay latched until the t_{RETRY} period expires.

8.3.15.8 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the IC status (IC_STAT) register and OTW bit in the status register is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}).

Note

Over temperature warning is not reported on nFAULT pin by default.

8.3.15.9 Thermal Shutdown (OTS)

DRV8316-Q1 has 2 die temperature sensor for thermal shutdown, one of them near FETs and other one in other part of die.

8.3.15.9.1 OTS FET

If the die temperature near FET exceeds the trip point of the thermal shutdown limit (T_{TSD_FET}), all the FETs are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

8.3.15.9.2 OTS (Non FET)

If the die temperature in the device exceeds the trip point of the thermal shutdown limit (T_{TSD}), all the FETs are disabled, the buck regulator disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

8.4 Device Functional Modes

8.4.1 Functional Modes

8.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the DRV8316-Q1 family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, buck regulator (if present) is disabled, the charge pump is disabled, the AVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

Note

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

8.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, AVDD regulator, buck regulator, and SPI bus are active.

8.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the DRV8316-Q1 family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

8.4.2 DRVOFF functionality

DRV8316-Q1 has capability to disable predriver and MOSFETs bypassing the digital through DRVOFF pin. When DRVOFF pin is pulled high, all six MOSFETs are disabled. If nSLEEP is high when the DRVOFF pin is high, the charge pump, AVDD regulator, buck regulator, and SPI bus are active and any driver-related faults such as OCP will be inactive. DRVOFF pin independently disables MOSFETs which will stop motor commutation irrespective of status of INHx and INLx input pins.

Note

DRVOFF pin independently disables MOSFET, it may trigger fault condition resulting in nFAULT getting pulled low.

8.5 SPI Communication

8.5.1 Programming

On DRV8316-Q1 SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16-bit word, with a 6-bit address and 8 bits of data. The SPI output consists of 16 bit word, with a 8 bits of status information (STAT register) and 8-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

8.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 6 address bits, A (bits B14 through B9)
- Parity bit, P (bit B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits are status bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

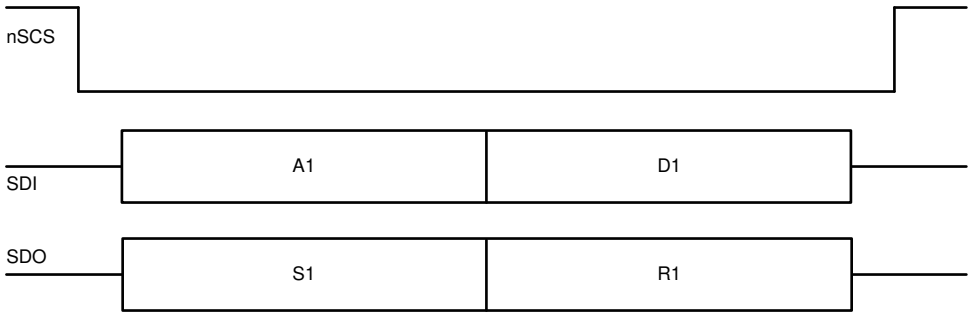


図 8-44.

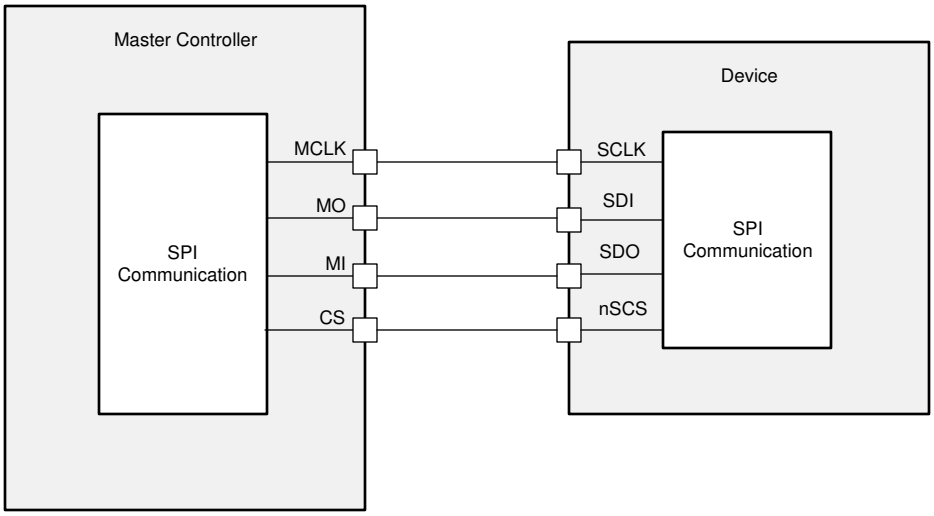


図 8-45.

表 8-9. SDI Input Data Word Format

R/W	ADDRESS						Parity	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A5	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0

表 8-10. SDO Output Data Word Format

STATUS								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0

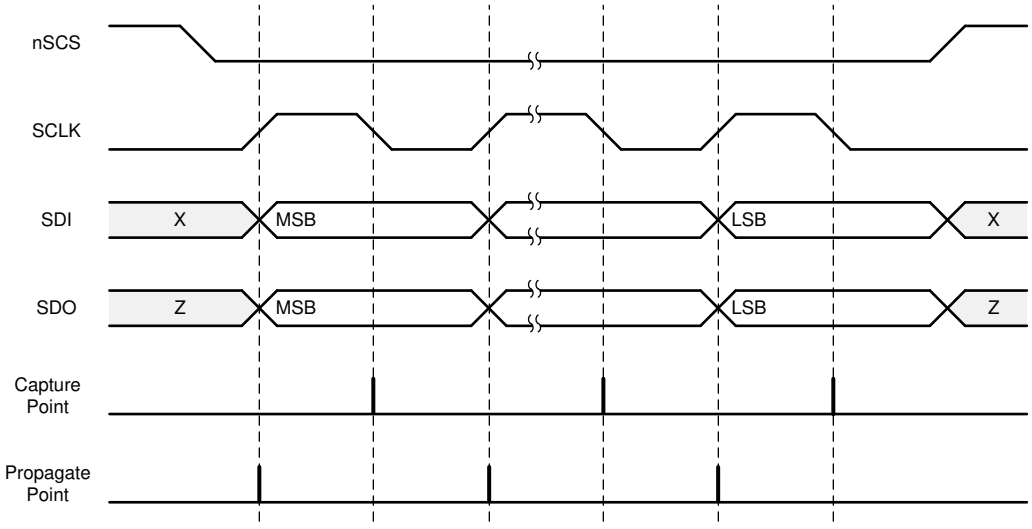


図 8-46. SPI Slave Timing Diagram

8.6 Register Map

8.6.1 STATUS Registers

STATUS Registers lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in STATUS Registers should be considered as reserved locations and the register contents should not be modified.

表 8-11. STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC_Status_Register	IC Status Register	セクション 8.6.1.1
1h	Status_Register_1	Status Register 1	セクション 8.6.1.2
2h	Status_Register_2	Status Register 2	セクション 8.6.1.3

Complex bit access types are encoded to fit into small table cells. STATUS Access Type Codes shows the codes that are used for access types in this section.

表 8-12. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

8.6.1.1 IC_Status_Register Register (Offset = 0h) [Reset = 00h]

IC_Status_Register is shown in IC_Status_Register Register and described in IC_Status_Register Register Field Descriptions.

Return to the STATUS Registers.

図 8-47. IC_Status_Register Register

7	6	5	4	3	2	1	0
	BK_FLT	SPI_FLT	OCP	NPOR	OVP	OT	FAULT
	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-13. IC_Status_Register Register Field Descriptions

Bit	Field	Type	Reset	Description
6	BK_FLT	R	0h	Buck Fault Bit 0h = No buck regulator fault condition is detected 1h = Buck regulator fault condition is detected
5	SPI_FLT	R	0h	SPI Fault Bit 0h = No SPI fault condition is detected 1h = SPI Fault condition is detected
4	OCP	R	0h	Over Current Protection Status Bit 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
3	NPOR	R	0h	Supply Power On Reset Bit 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
2	OVP	R	0h	Supply Overvoltage Protection Status Bit 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
1	OT	R	0h	Overtemperature Fault Status Bit 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device Fault Bit 0h = No fault condition is detected 1h = Fault condition is detected

8.6.1.2 Status_Register_1 Register (Offset = 1h) [Reset = 00h]

Status_Register_1 is shown in Status_Register_1 Register and described in Status_Register_1 Register Field Descriptions.

Return to the STATUS Registers.

図 8-48. Status_Register_1 Register

7	6	5	4	3	2	1	0
OTW	OTS	OCP_HC	OCL_LC	OCP_HB	OCP_LB	OCP_HA	OCP_LA
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

表 8-14. Status_Register_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OTW	R	0h	Overtemperature Warning Status Bit 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
6	OTS	R	0h	Overtemperature Shutdown Status Bit 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
5	OCP_HC	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
4	OCL_LC	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
3	OCP_HB	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
2	OCP_LB	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
1	OCP_HA	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
0	OCP_LA	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA

8.6.1.3 Status_Register_2 Register (Offset = 2h) [Reset = 00h]

Status_Register_2 is shown in Status_Register_2 Register and described in Status_Register_2 Register Field Descriptions.

Return to the STATUS Registers.

図 8-49. Status_Register_2 Register

7	6	5	4	3	2	1	0
RESERVED	OTP_ERR	BUCK_OCP	BUCK_UV	VCP_UV	SPI_PARITY	SPI_SCLK_FLT	SPI_ADDR_FLT
R-0-0h	R-0h	R-0h	R-0h	R-0h	R-0-0h	R-0h	R-0h

表 8-15. Status_Register_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	OTP_ERR	R	0h	One Time Programmabilty Error 0h = No OTP error is detected 1h = OTP Error is detected
5	BUCK_OCP	R	0h	Buck Regulator Overcurrent Staus Bit 0h = No buck regulator overcurrent is detected 1h = Buck regulator overcurrent is detected
4	BUCK_UV	R	0h	Buck Regulator Undervoltage Staus Bit 0h = No buck regulator undervoltage is detected 1h = Buck regulator undervoltage is detected
3	VCP_UV	R	0h	Charge Pump Undervoltage Status Bit 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
2	SPI_PARITY	R-0	0h	SPI Parity Error Bit 0h = No SPI parity error is detected 1h = SPI parity error is detected
1	SPI_SCLK_FLT	R	0h	SPI Clock Framing Error Bit 0h = No SPI clock framing error is detected 1h = SPI clock framing error is detected
0	SPI_ADDR_FLT	R	0h	SPI Address Error Bit 0h = No SPI address fault is detected (due to accessing non-user register) 1h = SPI address fault is detected

8.6.2 CONTROL Registers

CONTROL Registers lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in CONTROL Registers should be considered as reserved locations and the register contents should not be modified.

表 8-16. CONTROL Registers

Offset	Acronym	Register Name	Section
3h	Control_Register_1	Control Register 1	セクション 8.6.2.1
4h	Control_Register_2	Control Register 2	セクション 8.6.2.2
5h	Control_Register_3	Control Register 3	セクション 8.6.2.3
6h	Control_Register_4	Control Register 4	セクション 8.6.2.4
7h	Control_Register_5	Control Register 5	セクション 8.6.2.5
8h	Control_Register_6	Control Register 6	セクション 8.6.2.6
Ch	Control_Register_10	Control Register 10	セクション 8.6.2.7

Complex bit access types are encoded to fit into small table cells. CONTROL Access Type Codes shows the codes that are used for access types in this section.

表 8-17. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WAPU	W APU	Write Atomic write with password unlock
Reset or Default Value		
-n		Value after reset or the default value

8.6.2.1 Control_Register_1 Register (Offset = 3h) [Reset = 00h]

Control_Register_1 is shown in Control_Register_1 Register and described in Control_Register_1 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-50. Control_Register_1 Register

7	6	5	4	3	2	1	0
RESERVED					REG_LOCK		
R-0-0h					R/WAPU-0h		

表 8-18. Control_Register_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	REG_LOCK	R/WAPU	0h	Register Lock Bits 0h = No effect unless locked or unlocked 1h = No effect unless locked or unlocked 2h = No effect unless locked or unlocked 3h = Write 011b to this register to unlock all registers 4h = No effect unless locked or unlocked 5h = No effect unless locked or unlocked 6h = Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x03h bits 2-0. 7h = No effect unless locked or unlocked

8.6.2.2 Control_Register_2 Register (Offset = 4h) [Reset = 60h]

Control_Register_2 is shown in Control_Register_2 Register and described in Control_Register_2 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-51. Control_Register_2 Register

7	6	5	4	3	2	1	0
RESERVED		SDO_MODE	SLEW		PWM_MODE		CLR_FLT
R/W-1h		R/W-1h	R/W-0h		R/W-0h		W1C-0h

表 8-19. Control_Register_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	1h	Reserved
5	SDO_MODE	R/W	1h	SDO Mode Setting 0h = SDO IO in Open Drain Mode 1h = SDO IO in Push Pull Mode
4-3	SLEW	R/W	0h	Slew Rate Settings 0h = Slew rate is 25 V/µs 1h = Slew rate is 50 V/µs 2h = Slew rate is 125 V/µs 3h = Slew rate is 200 V/µs
2-1	PWM_MODE	R/W	0h	Device Mode Selection 0h = 6x mode 1h = 6x mode with current limit 2h = 3x mode 3h = 3x mode with current limit
0	CLR_FLT	W1C	0h	Clear Fault 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

8.6.2.3 Control_Register_3 Register (Offset = 5h) [Reset = 46h]

Control_Register_3 is shown in Control_Register_3 Register and described in Control_Register_3 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-52. Control_Register_3 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	PWM_100_DUTY_SEL	OVP_SEL	OVP_EN	RESERVED	OTW_REP
R-0-0h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-1h	R/W-1h	R/W-0h

表 8-20. Control_Register_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	RESERVED	R/W	1h	Reserved
5	RESERVED	R/W	0h	Reserved
4	PWM_100_DUTY_SEL	R/W	0h	Freqency of PWM at 100% Duty Cycle 0h = 20KHz 1h = 40KHz
3	OVP_SEL	R/W	0h	Overvoltage Level Setting 0h = VM overvoltage level is 34-V 1h = VM overvoltage level is 22-V
2	OVP_EN	R/W	1h	Overvoltage Enable Bit 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
1	RESERVED	R/W	1h	Reserved
0	OTW_REP	R/W	0h	Overtemperature Warning Reporting Bit 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

8.6.2.4 Control_Register_4 Register (Offset = 6h) [Reset = 10h]

Control_Register_4 is shown in Control_Register_4 Register and described in Control_Register_4 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-53. Control_Register_4 Register

7	6	5	4	3	2	1	0
DRV_OFF	OCP_CBC	OCP_DEG		OCP_RETRY	OCP_LVL	OCP_MODE	
R/W-0h	R/W-0h	R/W-1h		R/W-0h	R/W-0h	R/W-0h	

表 8-21. Control_Register_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRV_OFF	R/W	0h	Driver OFF Bit 0h = No Action 1h = Enter Low Power Standby Mode
6	OCP_CBC	R/W	0h	OCP PWM Cycle Operation Bit 0h = OCP clearing in PWM input cycle change is disabled 1h = OCP clearing in PWM input cycle change is enabled
5-4	OCP_DEG	R/W	1h	OCP Deglitch Time Settings 0h = OCP deglitch time is 0.2 µs 1h = OCP deglitch time is 0.6 µs 2h = OCP deglitch time is 1.25 µs 3h = OCP deglitch time is 1.6 µs
3	OCP_RETRY	R/W	0h	OCP Retry Time Settings 0h = OCP retry time is 5 ms 1h = OCP retry time is 500 ms
2	OCP_LVL	R/W	0h	Overcurrent Level Setting 0h = OCP level is 16 A 1h = OCP level is 24 A
1-0	OCP_MODE	R/W	0h	OCP Fault Options 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Overcurrent is report only but no action is taken 3h = Overcurrent is not reported and no action is taken

8.6.2.5 Control_Register_5 Register (Offset = 7h) [Reset = 00h]

Control_Register_5 is shown in Control_Register_5 Register and described in Control_Register_5 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-54. Control_Register_5 Register

7	6	5	4	3	2	1	0
RESERVED	ILIM_RECIR	RESERVED	RESERVED	EN_AAR	EN_ASR	CSA_GAIN	
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	

表 8-22. Control_Register_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	ILIM_RECIR	R/W	0h	Current Limit Recirculation Settings 0h = Current recirculation through FETs (Brake Mode) 1h = Current recirculation through diodes (Coast Mode)
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	EN_AAR	R/W	0h	Active Asynshronous Rectification Enable Bit 0h = AAR mode is disabled 1h = AAR mode is enabled
2	EN_ASR	R/W	0h	Active Synchronous Rectification Enable Bit 0h = ASR mode is disabled 1h = ASR mode is enabled
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier's Gain Settings 0h = CSA gain is 0.15 V/A 1h = CSA gain is 0.3 V/A 2h = CSA gain is 0.6 V/A 3h = CSA gain is 1.2 V/A

8.6.2.6 Control_Register_6 Register (Offset = 8h) [Reset = 00h]

Control_Register_6 is shown in Control_Register_6 Register and described in Control_Register_6 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-55. Control_Register_6 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED	BUCK_PS_DIS	BUCK_CL	BUCK_SEL		BUCK_DIS
R-0-0h		R/W-0h	R/W-0h	R/W-0h	R/W-0h		R/W-0h

表 8-23. Control_Register_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R-0	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	BUCK_PS_DIS	R/W	0h	Buck Power Sequencing Disable Bit 0h = Buck power sequencing is enabled 1h = Buck power sequencing is disabled
3	BUCK_CL	R/W	0h	Buck Current Limit Setting 0h = Buck regulator current limit is set to 600 mA 1h = Buck regulator current limit is set to 150 mA
2-1	BUCK_SEL	R/W	0h	Buck Voltage Selection 0h = Buck voltage is 3.3 V 1h = Buck voltage is 5.0 V 2h = Buck voltage is 4.0 V 3h = Buck voltage is 5.7 V
0	BUCK_DIS	R/W	0h	Buck Disable Bit 0h = Buck regulator is enabled 1h = Buck regulator is disabled

8.6.2.7 Control_Register_10 Register (Offset = Ch) [Reset = 00h]

Control_Register_10 is shown in Control_Register_10 Register and described in Control_Register_10 Register Field Descriptions.

Return to the CONTROL Registers.

図 8-56. Control_Register_10 Register

7	6	5	4	3	2	1	0
RESERVED			DLYCMP_EN	DLY_TARGET			
R-0-0h			R/W-0h	R/W-0h			

表 8-24. Control_Register_10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R-0	0h	Reserved
4	DLYCMP_EN	R/W	0h	Driver Delay Compensation enable 0h = Disable 1h = Enable
3-0	DLY_TARGET	R/W	0h	Delay Target for Driver Delay Compensation 0h = 0 us 1h = 0.4 us 2h = 0.6 us 3h = 0.8 us 4h = 1 us 5h = 1.2 us 6h = 1.4 us 7h = 1.6 us 8h = 1.8 us 9h = 2 us Ah = 2.2 us Bh = 2.4 us Ch = 2.6 us Dh = 2.8 us Eh = 3 us Fh = 3.2 us

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The DRV8316-Q1 can be used to drive Brushless-DC motors. The following design procedure can be used to configure the DRV8316-Q1.

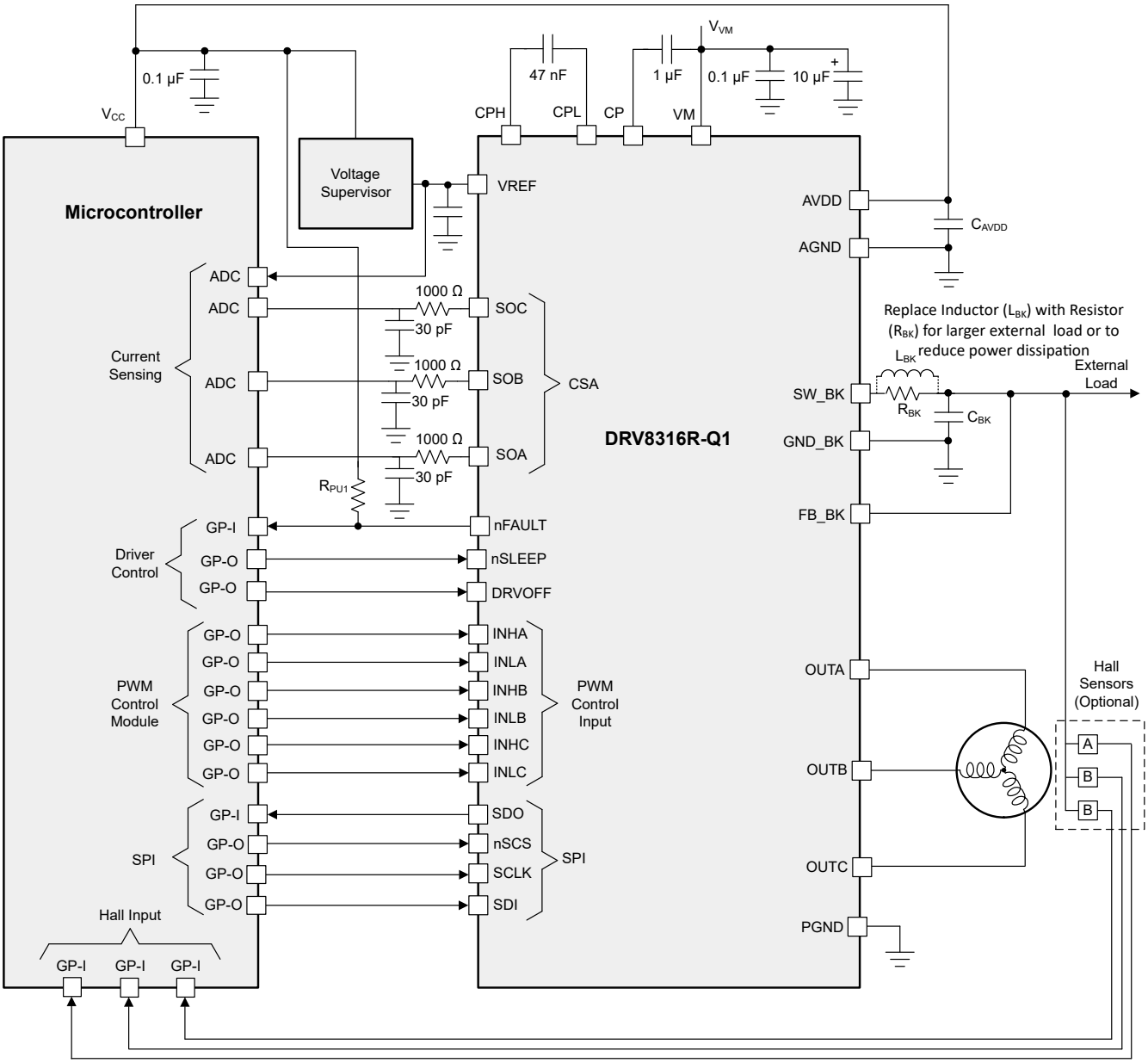


図 9-1. Primary Application Schematics

9.2 Typical Applications

9.2.1 Three-Phase Brushless-DC Motor Control

In this application, the DRV8316-Q1 is used to drive a Brushless-DC motor.

9.2.1.1 Detailed Design Procedure

表 9-1 lists the example input parameters for the system design.

表 9-1. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	24 V
Motor RMS current	I_{RMS}	3 A
Motor peak current	I_{PEAK}	8 A
PWM Frequency	f_{PWM}	50 kHz
Slew Rate Setting	SR	200 V/µs
Buck regulator output voltage	V_{BK}	3.3 V
ADC reference voltage	V_{VREF}	3.0 V
System ambient temperature	T_A	–20°C to +105°C

9.2.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. Operating at lower voltages generally allows for more accurate control of phase currents. The DRV8316-Q1 functions down to a supply of 4.5V. A higher operating voltage also corresponds to a higher obtainable rpm. The DRV8316-Q1 allows for a range of possible operating voltages because of a maximum VM rating of 40 V.

9.2.1.1.2 Using Active Demagnetization

Active demagnetization reduces power losses in the device by turning on the MOSFETs automatically when the body diode starts conducting to reduce diode conduction losses. It is used in trapezoidal commutation when switching commutation states (turning a high-side MOSFET off and another high-side MOSFET on while keeping a low-side MOSFET on). Active demagnetization is enabled when EN_ASR and EN_AAR bits are set in the SPI variant or OCP/SR pin is set to Mode 3 or Mode 4 in the H/W variant.

When switching commutation states with active demagnetization disabled, dead time is inserted and the low-side MOSFET's body diode conducts while turning another high-side MOSFET on to continue sourcing current through the motor. This conduction period causes higher power losses due to the forward-bias voltage of the diode and slower dissipation of current. 図 9-2 shows the body diode conducting when switching commutation states.

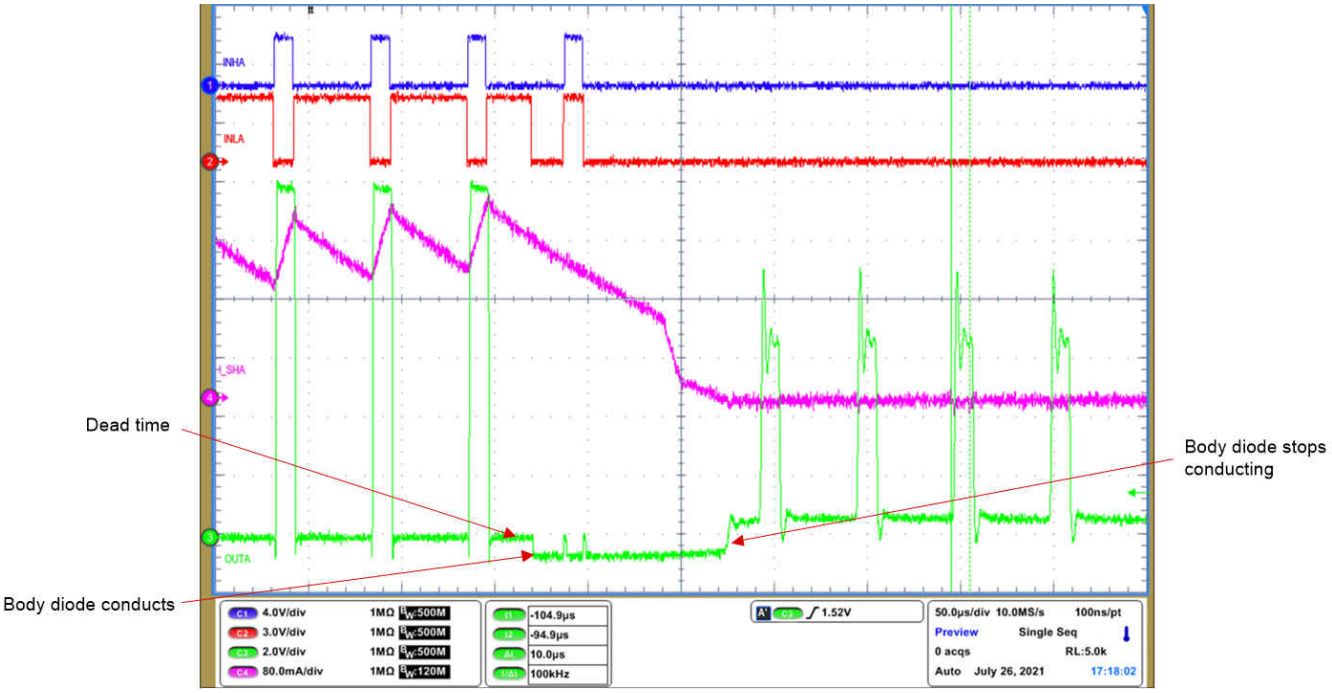


図 9-2. Active demagnetization disabled in DRV8316-Q1

When active demagnetization is enabled, the AD_HS and AD_LS comparators detect when the sense FET voltage is higher or lower than the programmed threshold. After the dead time period, if the threshold is exceeded for a fixed amount of time, the body diode is conducting and the logic core turns the low-side FET on to provide a conduction path with smaller power losses. Once the V_{DS} voltage is below the comparator threshold, the MOSFET turns off and current briefly conducts through the body diode until the current completely decays to zero. This is shown in 図 9-3.

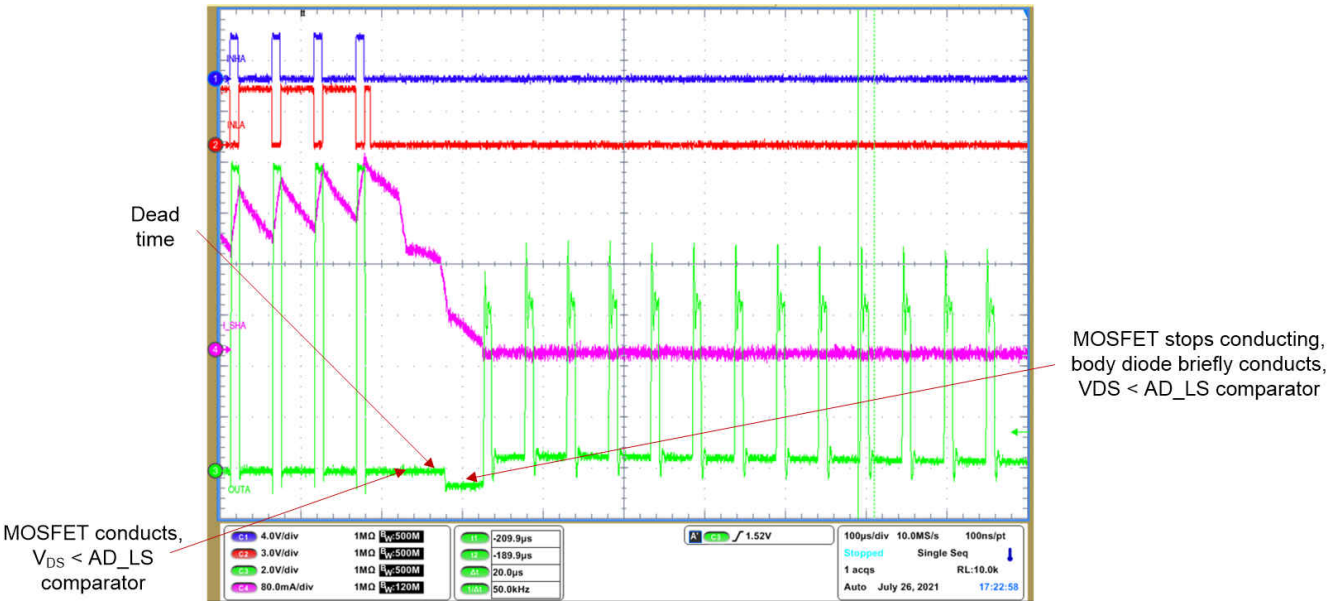


図 9-3. Active demagnetization enabled in DRV8316-Q1

9.2.1.1.3 Driver Propagation Delay and Dead Time

Driver propagation delay (t_{PD}) and dead time (t_{dead}) is specified with a typical and maximum value, but not with a minimum value. This is due to the direction of current at the OUTx pin when synchronous inputs are switching.

Driver propagation delay and dead time can be shorter than typical values due to slower internal turn-ons of the high-side or low-side internal MOSFETs to avoid internal dV/dt coupling.

For more information and examples of how propagation delay and dead time differs for input PWM and output configurations, please visit the Delay and Dead Time in Integrated MOSFET Drivers application note.

The dead time from the microcontroller's PWM outputs can be used as an extra precaution in addition to the DRV8316-Q1 internal shoot-through protection. This creates a condition where internal logic prioritizes the MCU dead time or driver dead time based on their durations.

If the MCU dead time is less than the driver dead time, the driver will compensate and make the true output dead time the value specified by the DRV8316-Q1. If the MCU inserted dead time is larger than the driver dead time, then the DRV8316-Q1 will adjust accordingly to the MCU dead time as shown in the table below.

A summary of the device delay times with respect to synchronous inputs INHx and INLx, OUTx current direction, and inserted MCU dead time are shown in 表 9-2.

表 9-2. Summary of delay times in integrated FET devices depending on inputs and output current direction

OUTx current direction	INHx	INLx	Propagation Delay (t_{PD})	Dead Time (t_{dead})	Inserted MCU dead time ($t_{dead(MCU)}$)	
					$t_{dead(MCU)} < t_{dead}$	$t_{dead(MCU)} > t_{dead}$
Out of OUTx	Rising	Falling	Typical	Typical	Output dead time = t_{dead}	Output dead time = $t_{dead(MCU)}$
	Falling	Rising	Smaller than typical	Smaller than typical	Output dead time < t_{dead}	Output dead time < $t_{dead(MCU)}$
Into OUTx	Rising	Falling	Smaller than typical	Smaller than typical	Output dead time < t_{dead}	Output dead time < $t_{dead(MCU)}$
	Falling	Rising	Typical	Typical	Output dead time = t_{dead}	Output dead time = $t_{dead(MCU)}$

9.2.1.1.4 Using Delay Compensation

Differences in delays of dead time and propagation delay can cause mismatch in the output timings of PWMs, which can lead to duty cycle distortion. In order to accommodate differences in propagation delay between various input conditions, the DRV8316R-Q1 integrates a Delay Compensation feature.

Delay Compensation is used to match delay times for currents going into and out of phase by adding a variable delay time (t_{var}) to match a preset target delay time. This delay time is configurable in SPI devices, and it is recommended in the datasheets to choose a target delay time that is equal to the propagation delay time plus the driver dead time (t_{pd} + t_{dead}).

For an example of Delay Compensation implementation, please visit the Delay and Dead Time in Integrated MOSFET Drivers application note.

9.2.1.1.5 Using the Buck Regulator

In the DRV8316-Q1, the buck regulator components must be populated whether the buck is used or unused.

If unused, Resistor Mode should be configured by placing a small value resistor of 22-ohm for R_{BK} and a 6.3-V rated, 22-uF capacitor for C_{BK} to minimize board space and reduce component cost. To disable the buck regulator, set the BUCK_DIS in the SPI variant. The buck cannot be disabled in the Hardware variant.

If the buck regulator is used, either the Inductor or Resistor Mode can be selected. Inductor Mode allows a 22-uH or 47-uH inductor be used for L_{BK}. C_{BK} is recommended to be 22-uF. Ensure an appropriate inductor is chosen to allow for maximum peak saturation current at a 20% inductance drop since the buck can supply up to 600-mA external current.

Resistor Mode allows for power to be dissipated in an external resistor if the load requirement is less than 40-mA. Ensure the resistor is rated for the power dissipation required at worst case VM voltage dropout. See 式 18,

式 19, and 式 20 to calculate the resistor power rating required for a 24-V rated system, 3.3V buck output voltage, and 20-mA load current.

$$P_{R_{BK}} > (V_M - V_{BK}) \times I_{BK} \quad (18)$$

$$P_{R_{BK}} > (24V - 3.3V) \times 20mA \quad (19)$$

$$P_{R\_BK} > 0.434W \quad (20)$$

9.2.1.1.6 Current Sensing and Output Filtering

The SOx pins are typically sampled by an analog-to-digital converter in the MCU to calculate the phase current. Phase current calculations are used for closed-loop feedback such as Field-oriented control.

An example calculation for phase current is shown in 式 21, 式 22, and 式 23 for a system using VREF = 3.0V, GAIN = 0.15 V/A, and a SOx voltage of 1.2V.

$$SOx = \left(\frac{VREF}{2}\right) \pm GAIN \times I_{OUTx} \quad (21)$$

$$1.2V = \left(\frac{3.0V}{2}\right) \pm 0.15\,V/A \times I_{OUTx} \quad (22)$$

$$I_{OUTx} = -2.0\,A \quad (23)$$

Sometimes high frequency noise can appear at the SOx signals based on voltage ripple at VREF, added inductance at the SOx traces, or routing of SOx traces near high frequency components. It is recommended to add a low-pass RC filter close to the MCU with cutoff frequency at least 10 times the PWM switching frequency for trapezoidal commutation and 100 times the PWM switching frequency for sinusoidal commutation to filter high frequency noise. A recommended RC filter is 1000-ohms, 30-pF to add minimal parallel capacitance to the ADC and current mirroring circuitry. The cutoff frequency for the low-pass RC filter is in 式 24.

$$f_c = \frac{1}{2\pi RC} \quad (24)$$

Note

There is a small dynamic offset and gain error that appears at the SOB output when sinking larger currents into OUTB in applications such as 3-shunt Field-oriented control. Check Current Sense Amplifier Offset Correction for equations to manually implement in software to compensate for dynamic gain and offset errors at larger currents.

9.2.1.1.7 Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the DRV8316-Q1 from power losses, use 式 25. Note that the thermal resistance θ_{JA} depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[℃] = P_{loss}[W] \times \theta_{JA}\left[\frac{℃}{W}\right] + T_A[℃] \quad (25)$$

9.2.1.2 Application Curves

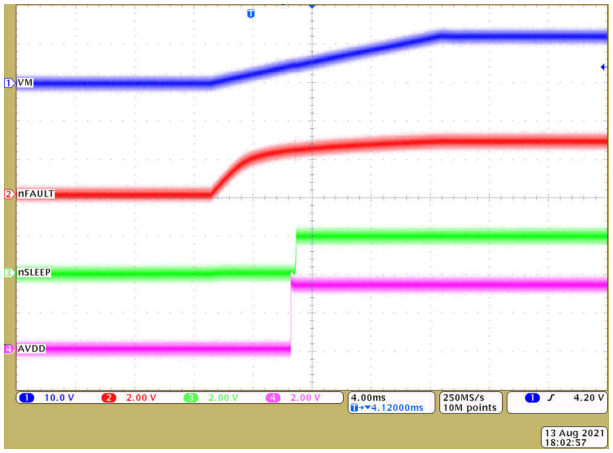


図 9-4. Device powerup with VM

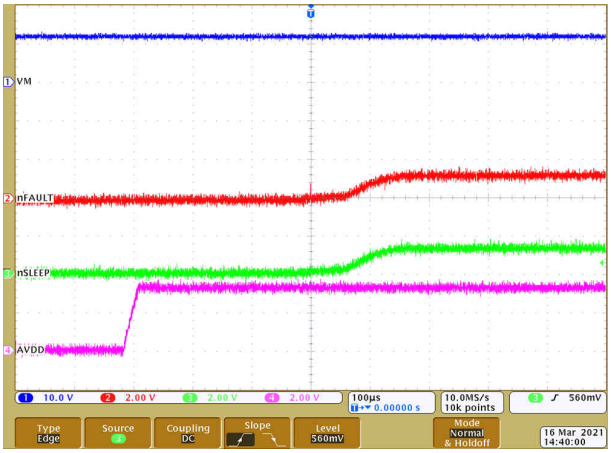


図 9-5. Device powerup with nSLEEP

図 9-6. Driver PWM operation with feedback

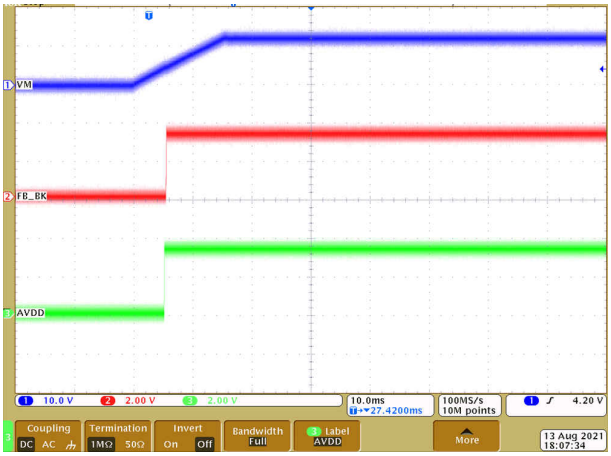


図 9-7. Power management

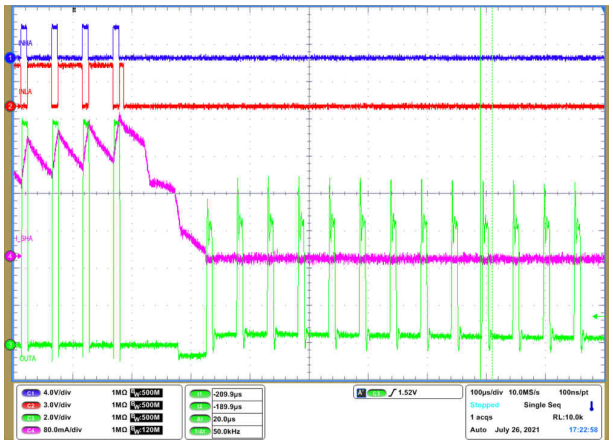


図 9-8. Driver PWM with active demagnetization (ASR and AAR)

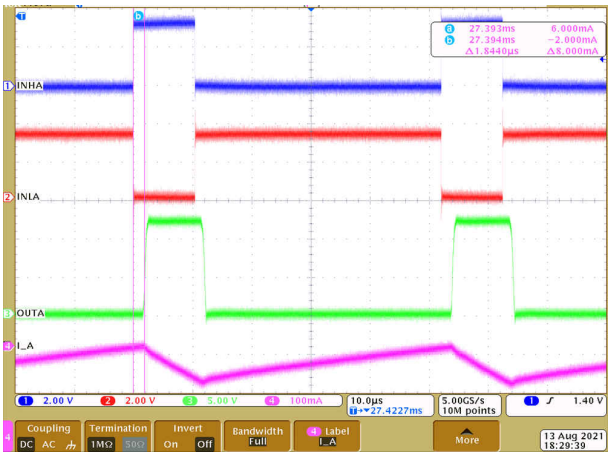


図 9-9. Driver delay compensation (1.8 µs)

9.2.2 Three-Phase Brushless-DC Motor Control With Current Limit

In this application, the DRV8316-Q1 is used to drive a brushless-DC motor with current limit up to 100% duty cycle. The following design procedure can be used to configure the DRV8316-Q1in current limit mode.

9.2.2.1 Block Diagram

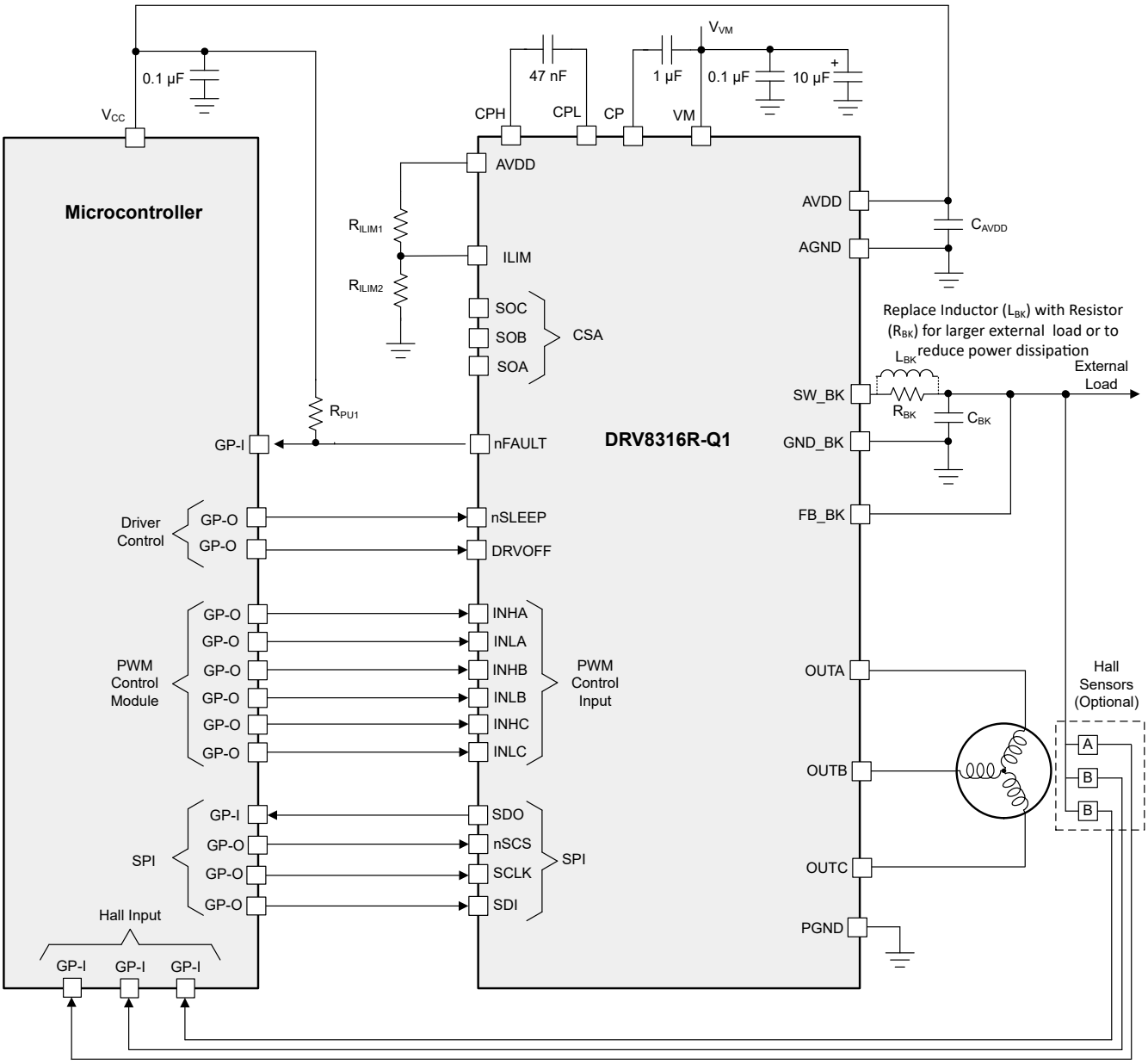


図 9-10. Alternate Application - BLDC Motor Control with Current Limit

9.2.2.2 Detailed Design Procedure

表 9-3 lists the example input parameters for the system design.

表 9-3. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	24 V
Motor peak current	I_{PEAK}	2 A

表 9-3. Design Parameters (continued)

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
PWM Frequency	f_{PWM}	50 kHz
Slew Rate Setting	SR	200 V/µs
Buck regulator output voltage	V_{BK}	3.3 V

9.2.2.2.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V and 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. A higher operating voltage also corresponds to a higher obtainable rpm. DRV8316-Q1 device allows for the use of higher operating voltage because of a maximum VM rating of 40 V.

Operating at lower voltages generally allows for more accurate control of phase currents. The DRV8316-Q1 functions down to a supply of 4.5V.

9.2.2.2.2 ILIM Implementation

The ILIM pin on the DRV8316-Q1 device is used to set a cycle-by-cycle current limit proportional to the voltage on the ILIM pin. The analog voltage ILIM can be set using a digital-to-analog converter from an external microcontroller or a resistor divider. Applying AVDD/2 on the ILIM pin disables the cycle-by-cycle current limit, and applying (AVDD/2 - 0.4) V on ILIM pin sets the current limit at the maximum threshold of 8-A.

式 26, 式 27, and 式 28 shows how to set the ILIM voltage with respect to AVDD = 3.3V to set cycle-by-cycle current limit to 2-A.

$$1.55V = 3.3\left(\frac{10\ \text{k}\Omega}{R_{ILIM1} + 10\ \text{k}\Omega}\right) \tag{26}$$

$$ILIM[V] = \frac{\left(1.25 - \frac{3.3}{2}\right)[V]}{8\ A} \times 2\ A + 1.65\ V \tag{27}$$

$$ILIM[V] = 1.55V \tag{28}$$

Use 式 29 to calculate values for an AVDD-sourced resistor divider with resistors RILIM1 and RILIM2 to set ILIM equal to the 2-A calculated current limit.

$$ILIM[V] = AVDD\left(\frac{R_{ILIM2}}{R_{ILIM1} + R_{ILIM2}}\right) \tag{29}$$

To reduce current load on AVDD, R_{ILIM2} is configured to be 10 kΩ as shown in 式 30 and 式 31.

$$1.55V = 3.3\left(\frac{10\ \text{k}\Omega}{R_{ILIM1} + 10\ \text{k}\Omega}\right) \tag{30}$$

$$R_{ILIM1} = 11.29\ \text{k}\Omega \tag{31}$$

Cycle-by-cycle limit can also occur with 100% PWM duty cycle inputs using an internal PWM pulse to monitor the current with ILIM. Setting the PWM_100_DUTY_SEL configures the frequency of the internal PWM pulse to 20kHz or 40kHz.

9.2.2.3 Application Curves

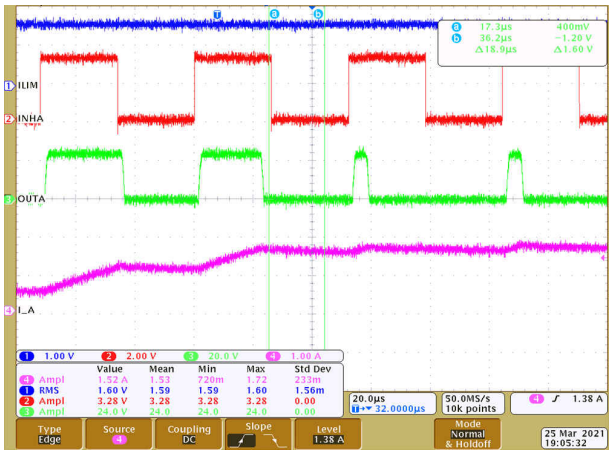


図 9-11. Driver PWM with Current Limit

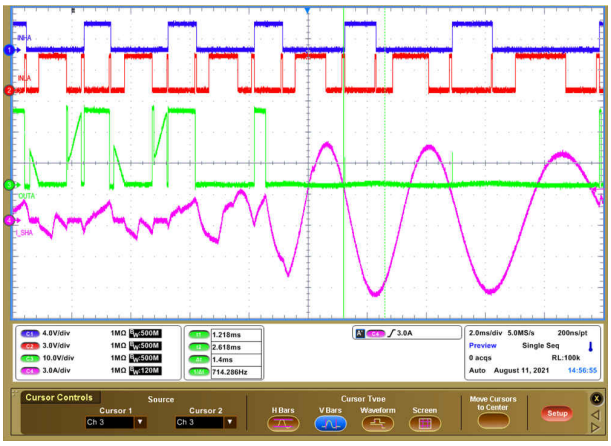


図 9-12. Device 100% Operation with Current Chopping (Latched shutdown mode)

9.2.3 Brushed-DC and Solenoid Load

In this application, the DRV8316-Q1 can be configured to drive a Brushed-DC motor and a solenoid load.

9.2.3.1 Block Diagram

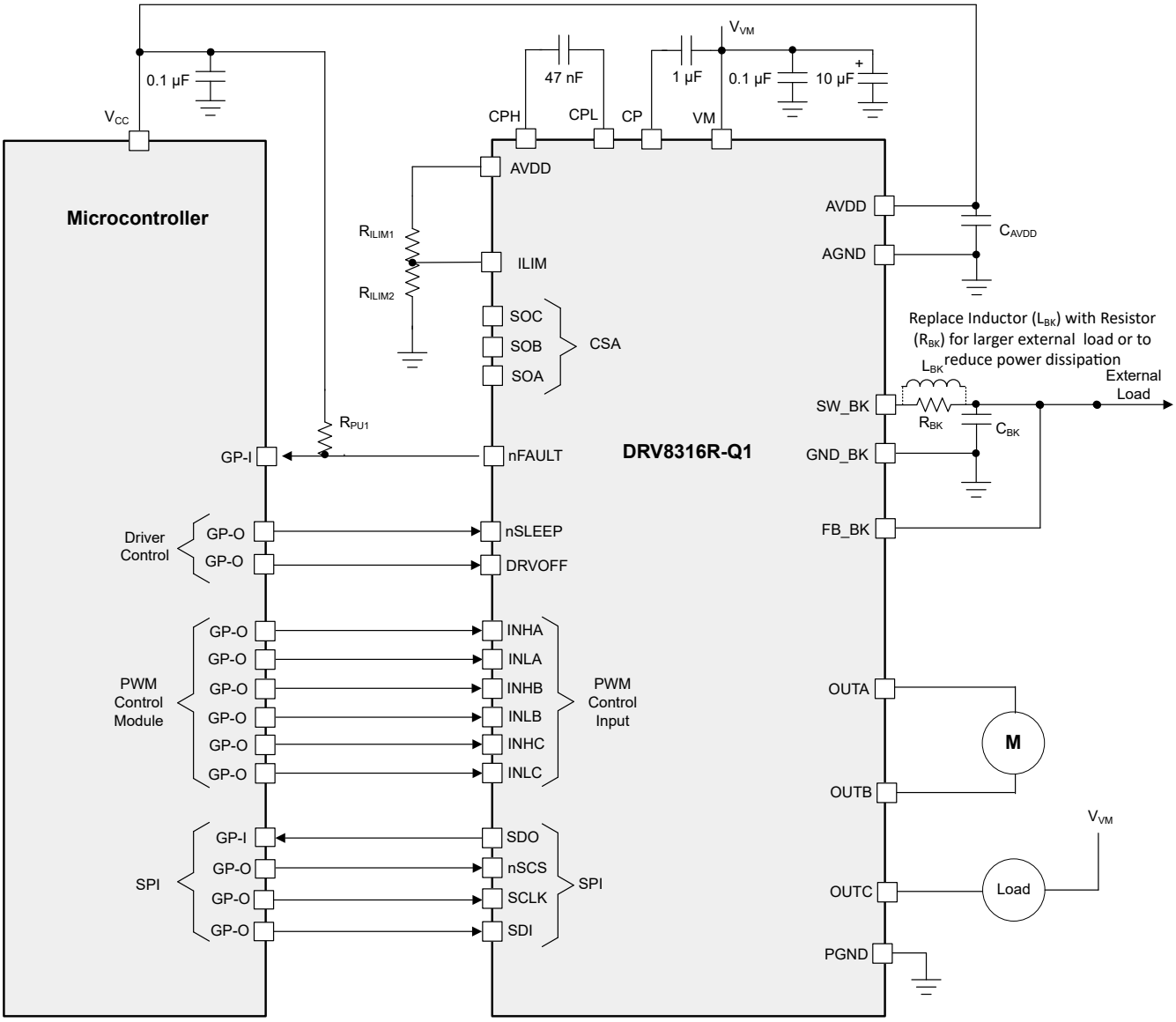


図 9-13. Alternate Application - Brushed DC Motor and Solenoid with Current Limit

9.2.3.2 Design Requirements

表 9-4 gives design input parameters for system design.

表 9-4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Brushed motor rms current	$I_{RMS, BDC}$	1.0 A
Brushed motor peak current	$I_{PEAK, BDC}$	2.0 A
Solenoid rms current	$I_{RMS, SOL}$	0.5 A
Solenoid peak current	$I_{PEAK, SOL}$	1.0 A

9.2.3.2.1 Detailed Design Procedure

表 9-5. Brushed-DC Control

Function	IN1	EN1	IN2	EN2	OUT1	OUT2
Forward	1	1	0	1	H	L
Reverse	0	1	1	1	L	H
Brake (low-side slow decay)	0	1	0	1	L	L
High-side slow decay	1	1	1	1	H	H
Coast	X	0	X	0	Z	Z

表 9-6. Solenoid Control (High-Side Load)

Function	IN3	EN3	OUT3
Coast / Off	X	0	Z
On	0	1	L
Brake	1	1	H

6x PWM mode or 3x PWM mode (with or without current limit) can be used to drive three solenoid loads depending on the application.

A Brushed-DC motor can be connected to two OUTx phases to create an integrated full H-bridge configuration to drive the motor. In 6x PWM mode or 3x PWM mode, current feedback can be monitored through the SOx pins of the H-bridge when current is dissipated through that phase's low-side FET during motor control. In 6x PWM with Current Limit or 3x PWM with Current Limit mode, cycle-by-cycle current can be implemented by setting the ILIM analog voltage to the proportional threshold.

Solenoid loads can be connected from OUTx to VM or GND to use the DRV8316-Q1 as a push-pull driver in 6x PWM or 3x PWM mode. When the load is connected from OUTx to GND, current is sourced from the high-side MOSFET and therefore current feedback or cycle-by-cycle current limit is not available. When the load is connected from OUTx to VM, current feedback or cycle-by-cycle current limit can be used depending on the mode configuration.

9.2.4 Three Solenoid Loads

The DRV8316-Q1 can be used to drive three solenoid loads. The following design procedure can be used to configure the DRV8316-Q1 for three solenoid loads.

9.2.4.1 Block Diagram

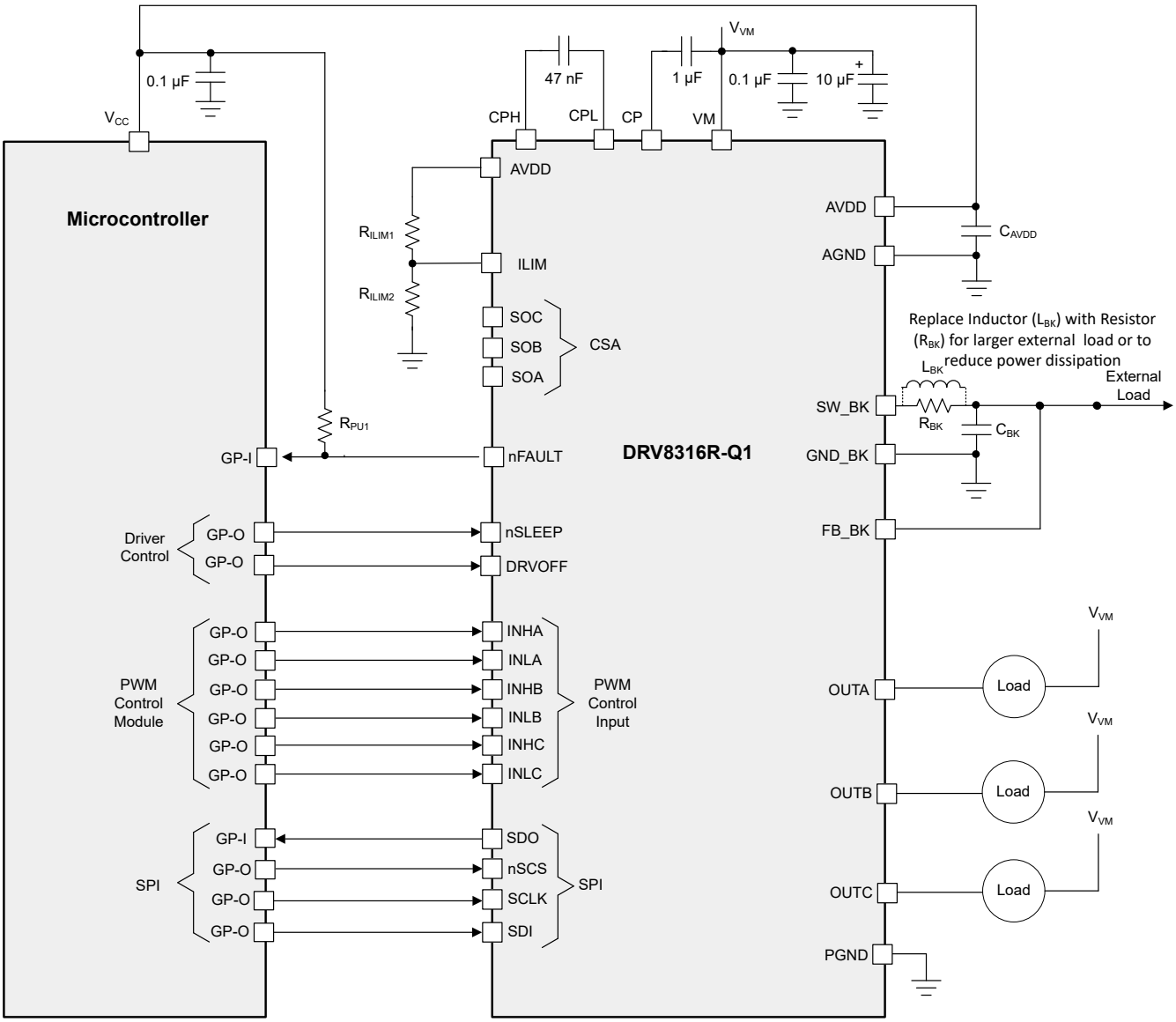


図 9-14. Alternate Application - Three Solenoid Loads with Current Limit

9.2.4.2 Design Requirements

表 9-7 gives design input parameters for system design.

表 9-7. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Solenoid rms current	$I_{RMS, SOL}$	1.0 A
Solenoid peak current	$I_{PEAK, SOL}$	1.5 A

9.2.4.2.1 Detailed Design Procedure

表 9-8. Solenoid Control (high-side load)

Function	IN2	EN2	OUT2
Coast / Off	X	0	Z
On	0	1	L
Brake	1	1	H

表 9-9. Solenoid Control (low-side load)

Function	IN1	EN1	OUT1
Coast / Off	X	0	Z
On	1	1	H
Brake	0	1	L

6x PWM mode or 3x PWM mode (with or without current limit) can be used to drive three solenoid loads depending on the application.

Solenoid loads can be connected from OUTx to VM or GND to use the DRV8316-Q1 as a push-pull driver in 6x PWM or 3x PWM mode. When the load is connected from OUTx to GND, current is sourced from the high-side MOSFET and therefore current feedback or cycle-by-cycle current limit is not available. When the load is connected from OUTx to VM, current feedback or cycle-by-cycle current limit can be used depending on the mode configuration.

10 Power Supply Recommendations

10.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

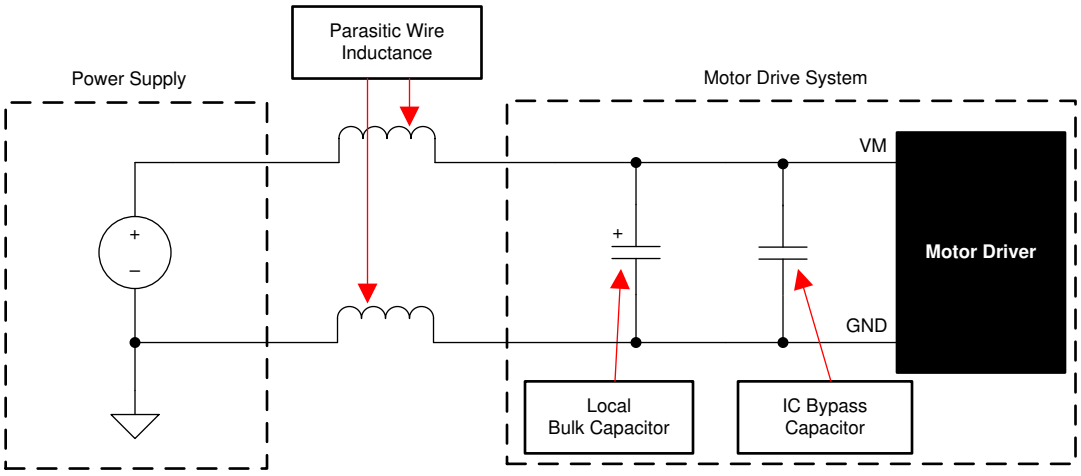


図 10-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11 Layout

11.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump, AVDD, and VREF capacitors should be ceramic and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Optionally, GND_BK can be split. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

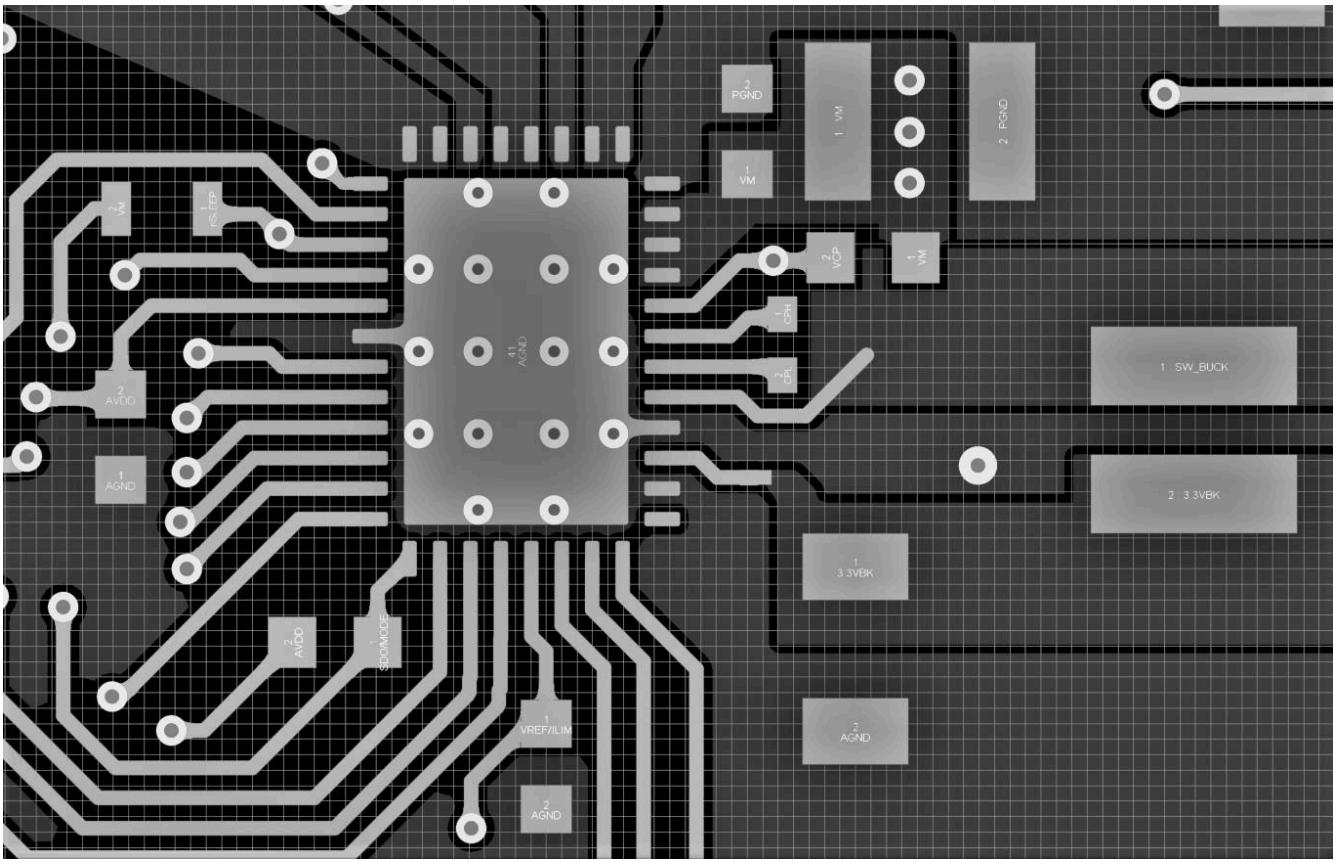
To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Separate the SW_BUCK and FB_BUCK traces with ground separation to reduce buck switching from coupling as noise into the buck outer feedback loop. Widen the FB_BUCK trace as much as possible to allow for faster load switching.

Recommended Layout Example for VQFN Package shows a layout example for the DRV8316-Q1.

11.2 Layout Example

Recommended Layout Example for VQFN Package



11.3 Thermal Considerations

The DRV8316-Q1 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11.3.1 Power Dissipation

The power dissipated in the output FET resistance, or $R_{DS(on)}$ dominates power dissipation in the DRV8316-Q1.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

A summary of equations for calculating each loss is shown below for trapezoidal controland field-oriented control.

表 11-1. DRV8316-Q1 Power Losses for Trapezoidal and Field-oriented Control

Loss type	Trapezoidal	Field-oriented control
Standby power	$P_{standby} = VM \times I_{VM\_TA}$	
LDO (from VM)	$P_{LDO} = (VM - V_{AVDD}) \times I_{AVDD}$, if BUCK_PS_DIS = 1b $P_{LDO} = (V_{BK} - V_{AVDD}) \times I_{AVDD}$, if BUCK_PS_DIS = 0b	
FET conduction	$P_{CON} = 2 \times (I_{RMS(trap)})^2 \times R_{ds,on(TA)}$	$P_{CON} = 3 \times (I_{RMS(FOC)})^2 \times R_{ds,on(TA)}$
FET switching	$P_{SW} = I_{PK(trap)} \times V_{PK(trap)} \times t_{rise/fall} \times f_{PWM}$	$P_{SW} = 3 \times I_{PK(FOC)} \times V_{PK(FOC)} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = I_{PK(trap)} \times V_{diode} \times t_{dead} \times f_{PWM}$	$P_{diode} = 3 \times I_{PK(FOC)} \times V_{diode} \times t_{dead} \times f_{PWM}$
Demagnetization	Without Active Demag: $3 \times I_{PK(trap)} \times V_{diode} \times t_{commutation} \times f_{motor\_elec}$ With Active Demag: $3 \times (I_{RMS(trap)})^2 \times R_{ds,on(TA)} \times t_{commutation} \times f_{motor\_elec}$	Not Applicable
Buck	$P_{BK} = 0.11 \times V_{BK} \times I_{BK}$ (η_{BK} = 90%)	

12 Device and Documentation Support

12.1 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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12.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

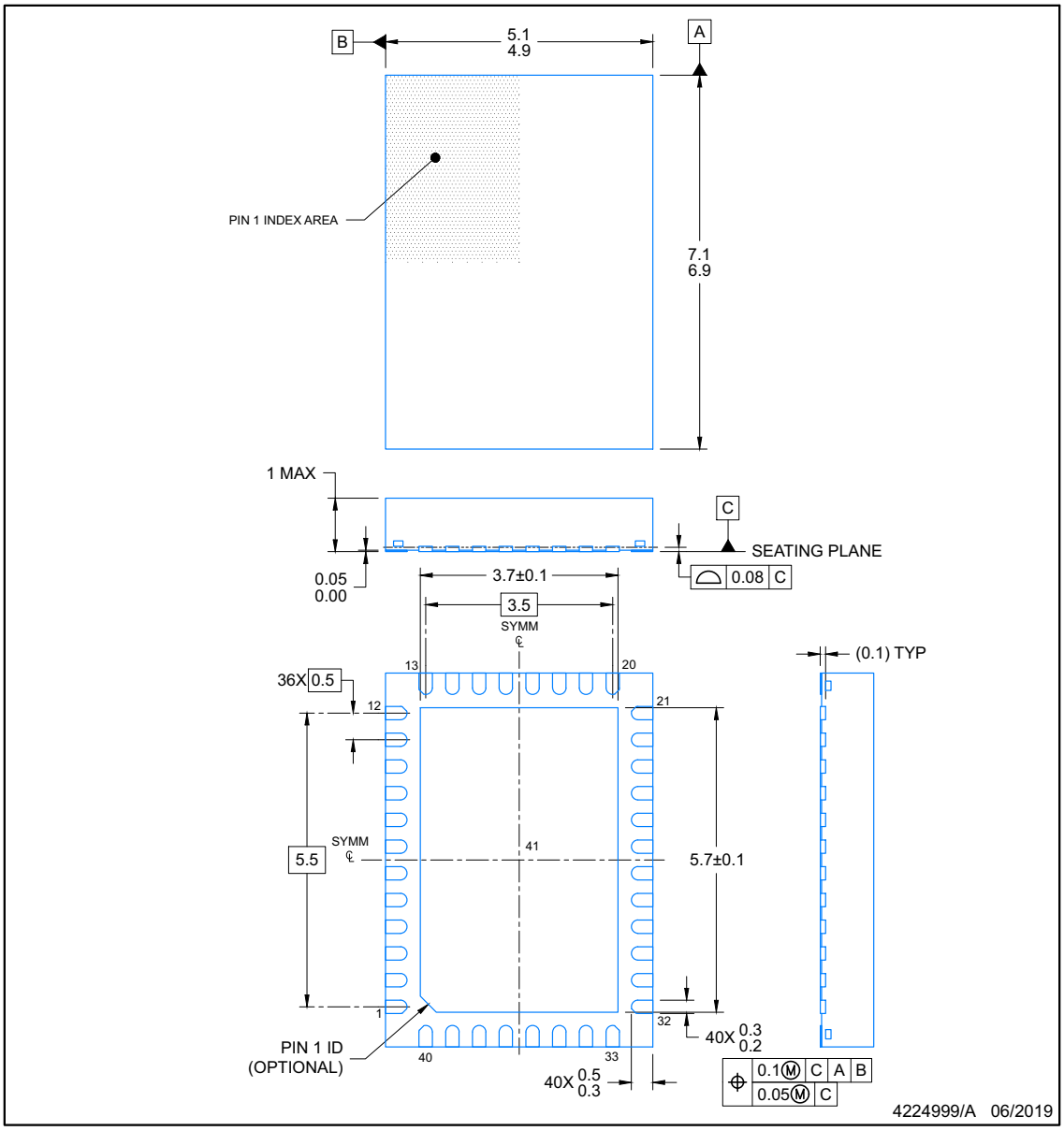
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGE OUTLINE

RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

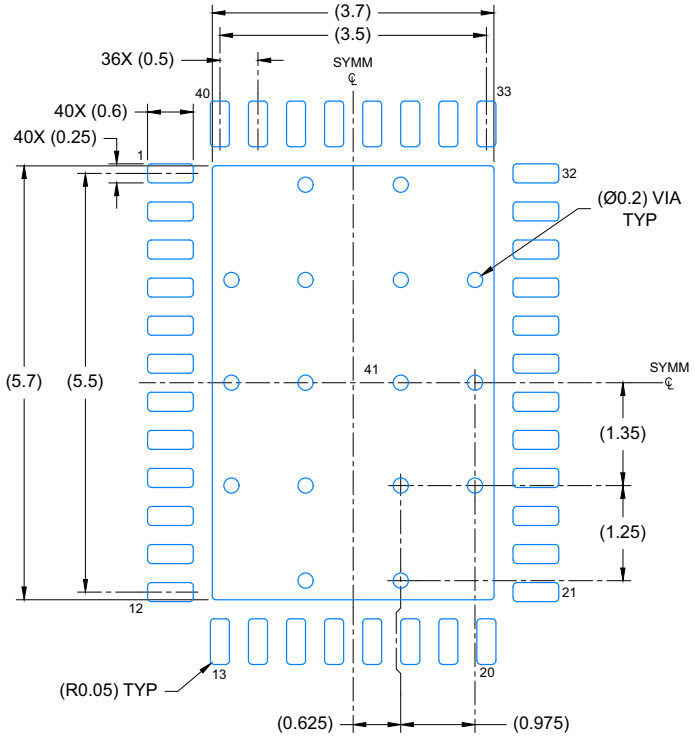
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

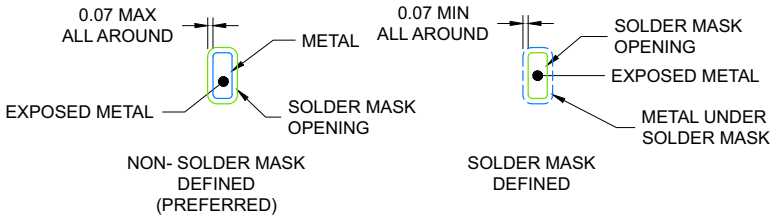
RGF0040E

VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4224999/A 06/2019

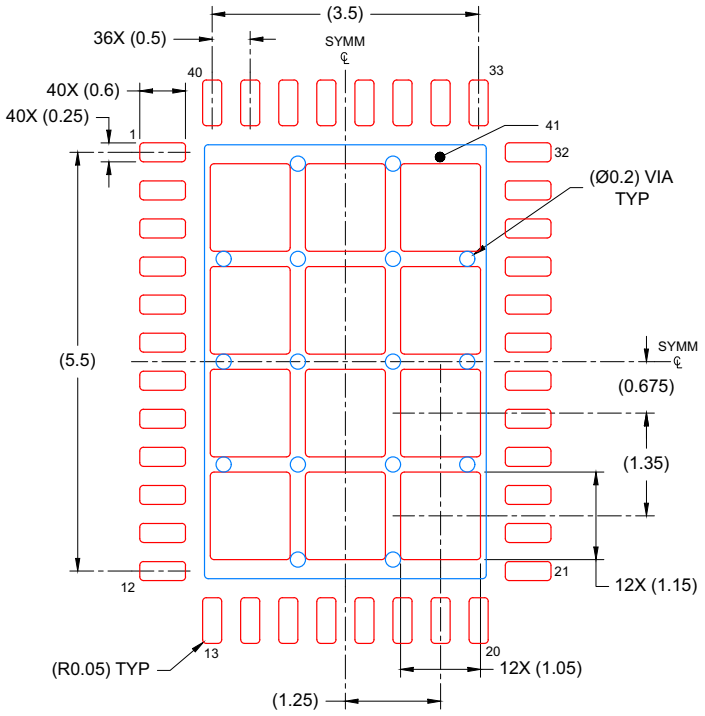
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGF0040E — **VQFN - 1 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4224999/A 06/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8316RQRGFRQ1	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8316RQ
DRV8316RQRGFRQ1.A	Active	Production	VQFN (RGF) | 40	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8316RQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DRV8316-Q1 :

- Catalog : DRV8316

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

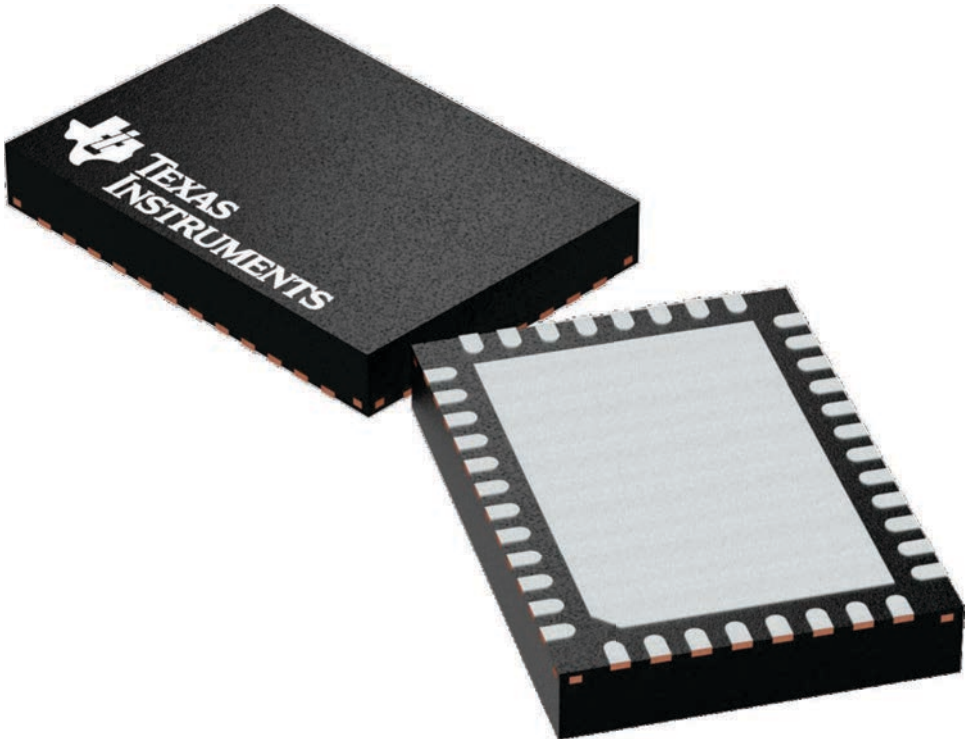
RGF 40

VQFN - 1 mm max height

5 x 7, 0.5 mm pitch

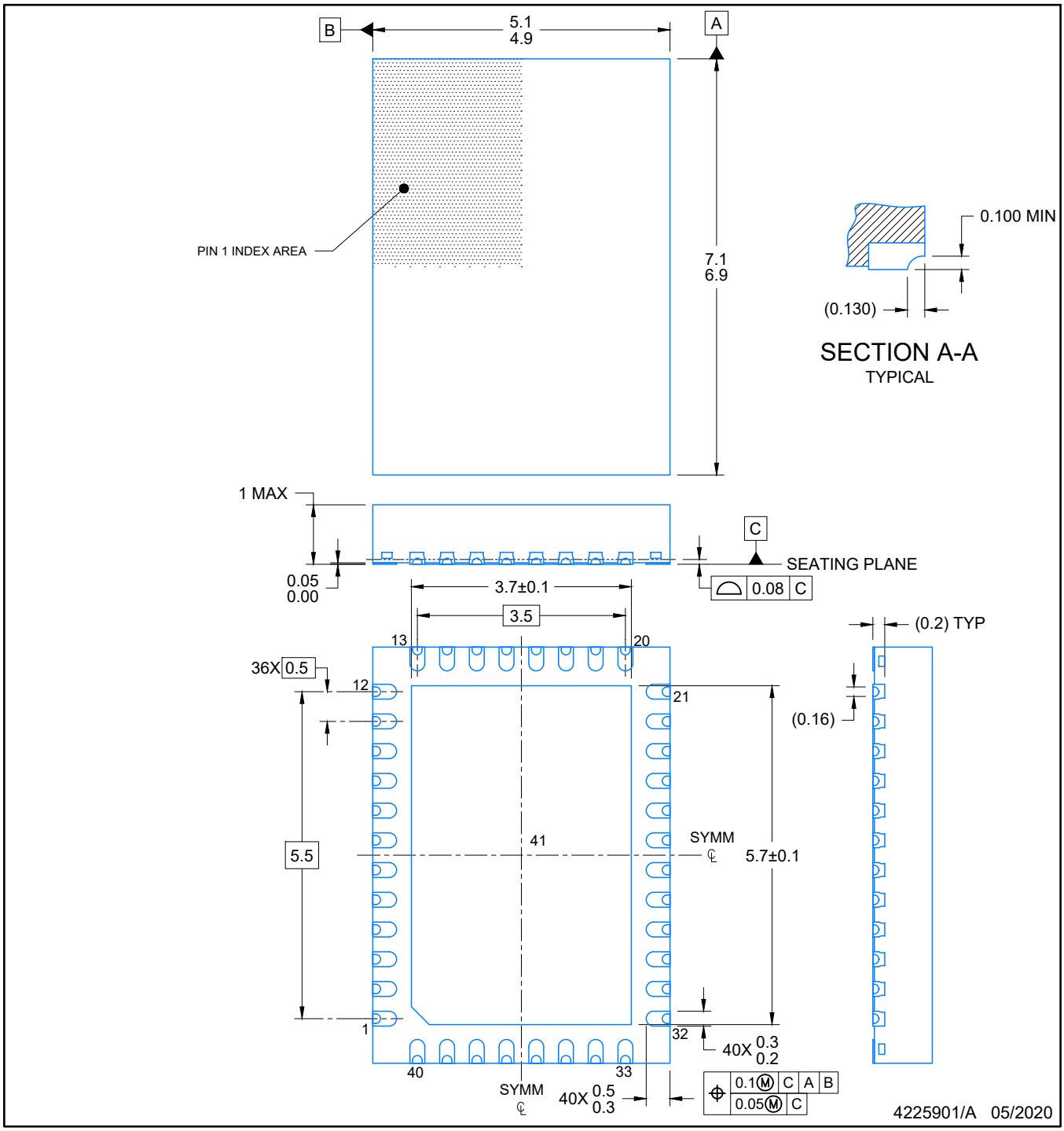
PLASTIC QUAD FLAT PACK- NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



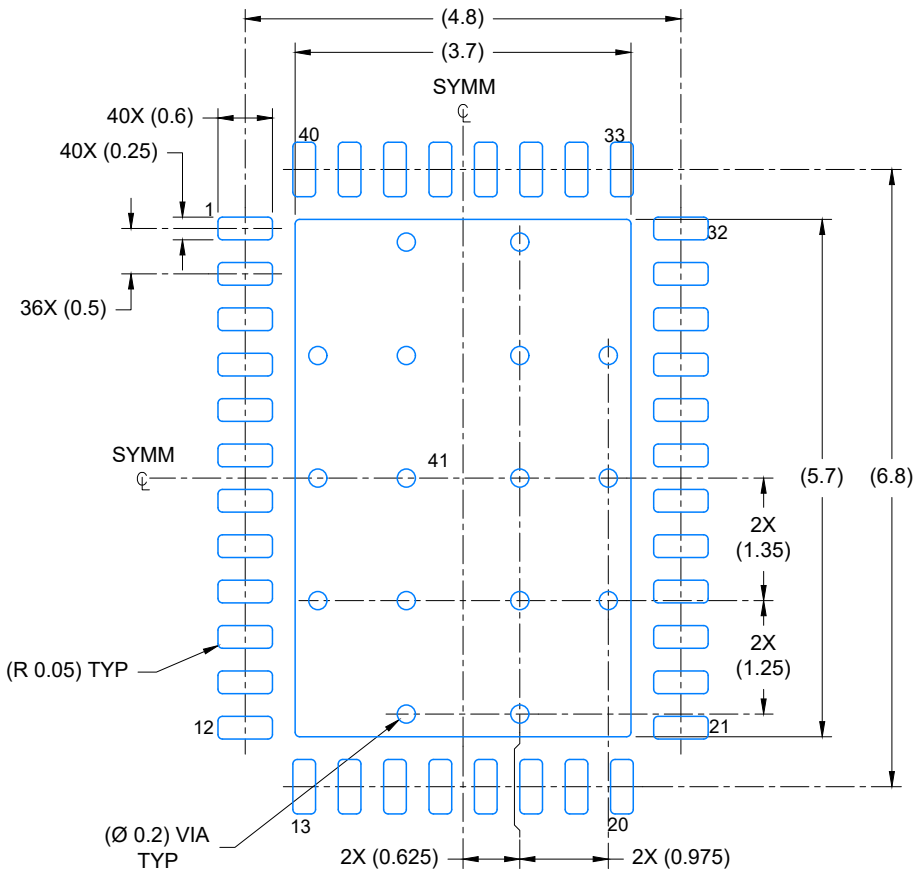
4225115/A

PLASTIC QUAD FLATPACK- NO LEAD

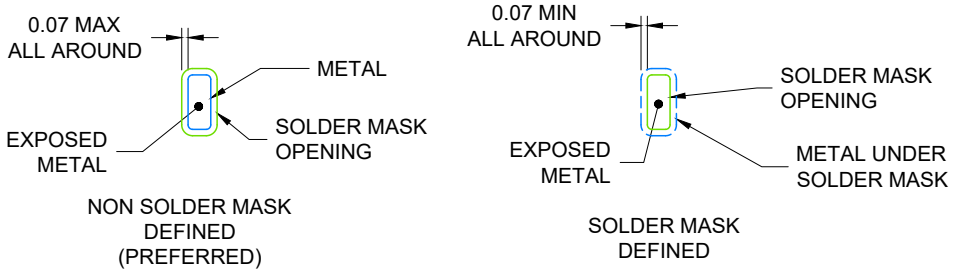


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

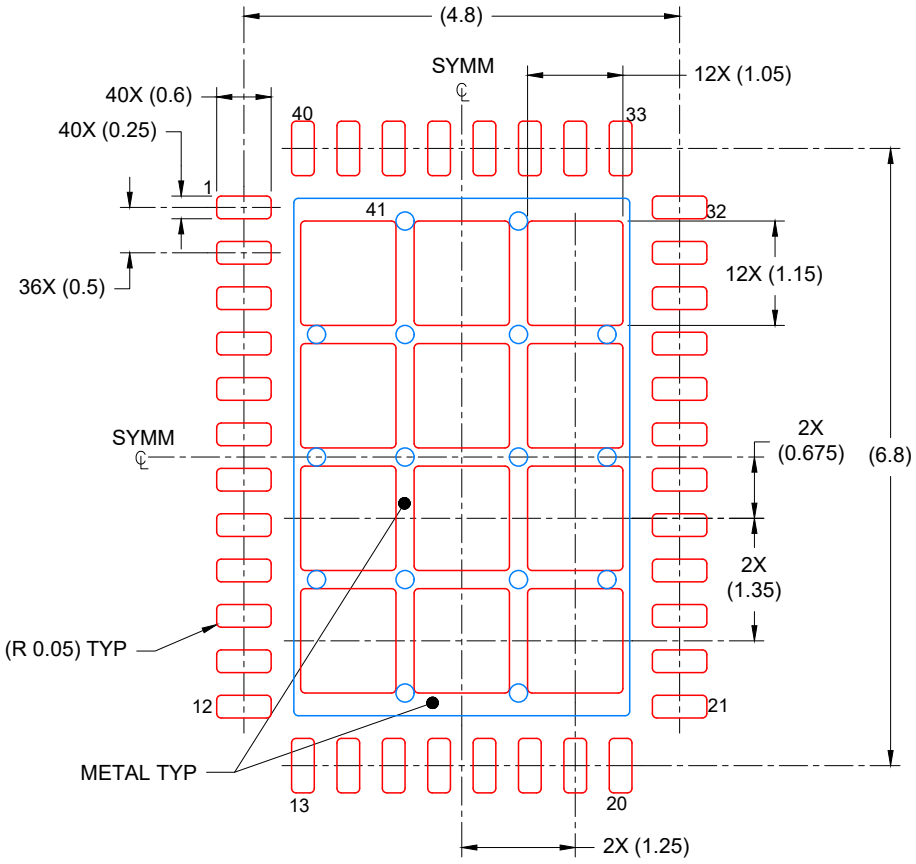


SOLDER MASK DETAILS

4225901/A 05/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
69% PRINTED COVERAGE BY AREA
SCALE: 12X

4225901/A 05/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最終更新日：2025 年 10 月