DRV8873-Q1 車載 H ブリッジ・モータ・ドライバ

1 特長

- 車載アプリケーション向けに AEC-Q100 認証を取得
  - デバイス温度グレード 1：-40℃～+125℃、T_A
- N チャネルの H ブリッジ・モータ・ドライバ
  - 1 つの双方向ブラシ付き DC モータを駆動
  - 2 つの単方向ブラシ付き DC モータ
  - ソレノイドまたはその他の抵抗性および誘導性負荷
- 4.5V～38V の動作電圧範囲
- 10A のピーク駆動電流
- 小さい $R_{DS(ON)}$ (HS + LS)
  - T_J = 25℃、13.5V 時 150mΩ
  - T_J = 150℃、13.5V 時 250mΩ
- 電流センス機能内蔵
- 比例電流出力 (IPROPI)
- 構成可能な制御インターフェイス
  - PH/EN
  - PWM (IN1/IN2)
  - 独立したハーフブリッジ制御
- 1.8V、3.3V、5V のロジック入力をサポート
- SPI またはハードウェア・インターフェイスを利用可能
- 小さなパッケージと占有面積
  - 24 ピン HTSSOP PowerPAD™ IC パッケージ
- 保護機能
  - VM 低電圧誤動作防止 (UVLO)
  - チャージ・ポンプ低電圧検出 (CPUV)
  - 過電流保護 (OCP)
  - 出力バッテリ短絡 / GND 短絡保護
  - 開放負荷検出
  - サーマル・シャットダウン (TSD)
  - フォルト状態出力 (nFAULT/SPI)
- 拡散スペクトラム・クロックによる低い電磁気妨害 (EMI)
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能

2 アプリケーション

- 電子スロットル制御
- 排気再循環
- サイドミラー・チルト
- e シフタ
- エアフロー誘導弁制御

3 概要

DRV8873-Q1 は車載用ブラシ付き DC モータを駆動する統合型ドライバ IC です。2 つのロジック入力が H ブリッジ・ドライバを制御し、ドライバを構成する 4 つの N チャネル MOSFET により、最大 10A のピーク電流でモータを双方向制御できます。また単一電源で動作し、4.5V～38V の広い入力電源電圧範囲に対応します。

PH/EN または PWM インターフェイスにより、制御回路に容易に接続できる一方、独立したハーフブリッジ制御を利用して 2 つのソレノイド負荷を駆動することも可能です。

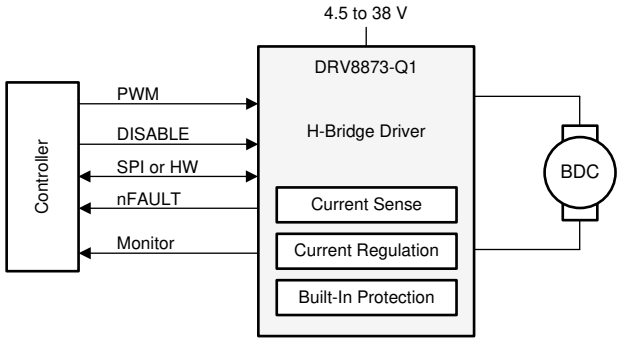
内蔵の電流センス機能により、電力定格が大きいセンス抵抗を使わなくても、両方のハイサイド FET のモータ負荷電流に比例する出力電流を供給できます。この機能を使用して、モータのストールまたは負荷条件の変化を検出できます。

低消費電力のスリープ・モードにより、内部回路の多くをシャットダウンして、静止電流を極めて小さく抑制できます。内蔵する保護機能には、低電圧誤動作防止、チャージ・ポンプ異常検出、過電流保護、短絡保護、開放負荷検出、過熱保護があります。フォルト状態は nFAULT ピンおよび SPI レジスタにより通知されます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
DRV8873-Q1	HTSSOP (24)	7.70mm × 4.40mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2018) to Revision B (January 2021)	Page
• 機能安全の箇条書き項目を追加	1

Changes from Revision * (October 2017) to Revision A (August 2018)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

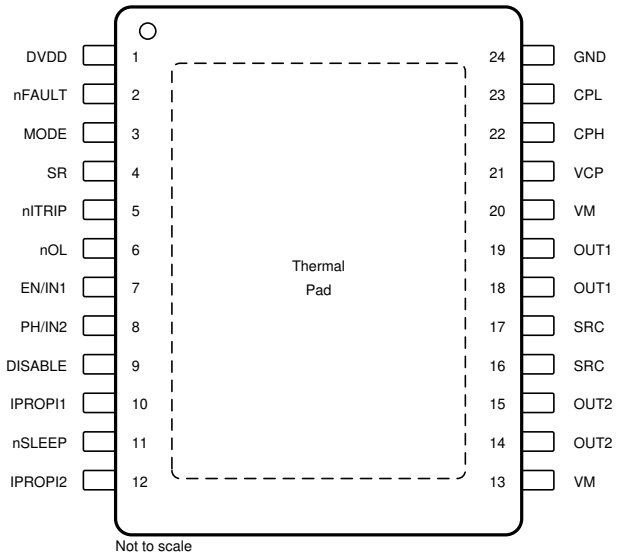


図 5-1. DRV8873H-Q1 PWP PowerPAD Package 24-Pin HTSSOP Top View

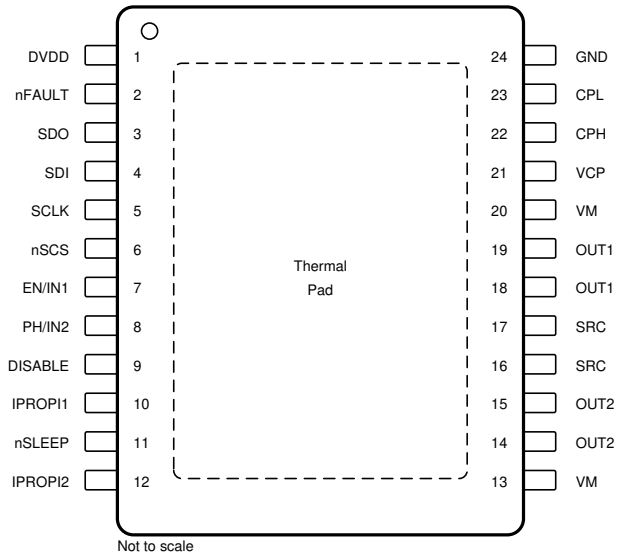


図 5-2. DRV8873S-Q1 PWP PowerPAD Package 24-Pin HTSSOP Top View

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	DRV8873H-Q1	DRV8873S-Q1		
CPH	22	22	PWR	Charge pump switching node. Connect a X7R capacitor with a value of 47 nF between the CPH and CPL pins.
CPL	23	23	PWR	Charge pump switching node. Connect a X7R capacitor with a value of 47 nF between the CPH and CPL pins.
DVDD	1	1	PWR	Digital regulator. This pin is the 5-V internal digital-supply regulator. Bypass this pin to GND with a 6.3-V, 1-µF ceramic capacitor.
EN/IN1	7	7	I	Control Inputs. For details, see the *セクション 7.3.1.1* section. This pin has an internal pulldown resistor to GND.
DISABLE	9	9	I	Bridge disable input. A logic high on this pin disables the H-bridge Hi-Z. Internal pullup to DVDD.
GND	24	24	PWR	Ground pin
IPROPI1	10	10	O	High-side FET current. The analog current proportional to the current flowing in the half bridge.
IPROPI2	12	12	O	High-side FET current. The analog current proportional to the current flowing in the half bridge.
nITRIP	5	—	I	Internal current-regulation control pin (ITRIP). To enable the ITRIP feature, do not connect this pin (or tie it to GND). To disable the ITRIP feature, connect this pin to the DVDD pin.
nOL	6	—	I	Open-load diagnostic control pin. To run the open-load diagnostic at power up, tie it to ground. Connect it to DVDD, open-load diagnostic will be disabled.
MODE	3	—	I	Input mode pin. Sets the PH/EN, PWM, or independent-PWM mode.
OUT1	18	18	O	Half-bridge output 1. Connect this pin to the motor or load.
OUT1	19	19	O	Half-bridge output 1. Connect this pin to the motor or load.
OUT2	14	14	O	Half-bridge output 2. Connect this pin to the motor or load.
OUT2	15	15	O	Half-bridge output 2. Connect this pin to the motor or load.

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PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	DRV8873H-Q1	DRV8873S-Q1		
PH/IN2	8	8	I	Control inputs. For details, see the セクション 7.3.1.1 section. This pin has an internal pulldown resistor to GND.
SCLK	—	5	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin.
SDI	—	4	I	Serial data input. Data is captured on the falling edge of the SCLK pin.
SDO	—	3	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This is a push-pull output.
SR	4	—	I	Slew rate adjust. This pin sets the slew rate of the H-bridge outputs.
SRC	16	16	O	Power FET source. Tie this pin to GND through a low-impedance path.
SRC	17	17	O	Power FET source. Tie this pin to GND through a low-impedance path.
VCP	21	21	PWR	Charge pump output. Connect a 16-V, 1-µF ceramic capacitor from this pin to the VM supply.
VM	13	13	PWR	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
VM	20	20	PWR	Power supply. This pin is the motor supply voltage. Bypass this pin to GND with a 0.1-µF ceramic capacitor and a bulk capacitor.
nFAULT	2	2	OD	Fault indication pin. This pin is pulled logic low with a fault condition. This open-drain output requires an external pullup resistor.
nSCS	—	6	I	Serial chip select. An active low on this pin enables the serial interface communications. Internal pullup to nSLEEP.
nSLEEP	11	11	I	Sleep input. To enter a low-power sleep mode, set this pin logic low.

(1) I = input, O = output, PWR = power, NC = no connect, OD = open-drain output, PP = push-pull output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Power supply voltage	VM	–0.3	40	V
	Charge pump voltage	VCP, CPH	–0.3	V_{VM} + 5.7	V
	Charge pump switching pin	CPL	–0.3	V_{VM}	V
	Internal logic regulator voltage	DVDD	–0.3	5.7	V
	Digital pin voltage	EN/IN1, PH/IN2, nSLEEP, DISABLE, nFAULT, MODE, SR, SCLK, SDI, SDO, nSCS	–0.3	5.7	V
V_{TRIP}	Analog pin voltage	IPROPI1, IPROPI2	0	5.5	V
V_{SRC}	H-Bridge source pin voltage		–0.3	0.3	V
	Phase node pin voltage	OUTx	V_{SRC} – 1	V_{VM} + 1	V
	Open drain output current	nFAULT	0	10	mA
	Push-pull output current	SDO	0	10	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100–002 HBM ESD Classification Level 2(1)		±2000	V
		Charged device model (CDM), per AEC Q100–011 CDM ESD Classification Level C4B	Corner pins (1, 12, 13, and 24)	±750	
			Other pins	±500	

(1) AEC Q100–002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS–001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{VM}	Power supply voltage	4.5	38	V
V_I	Logic level input voltage	0	5.5	V
f_{PWM}	Applied PWM signal (EN/IN1, PH/IN2)		100	kHz
T_A	Operating ambient temperature	–40	125	°C
T_J	Operating junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DRV8873-Q1 PWP (HTSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

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THERMAL METRIC(1)		DRV8873-Q1 PWP (HTSSOP) 24 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, DVDD)						
V_{VM}	VM operating voltage		4.5		38	V
I_{VM}	VM operating supply current	V_{VM} = 13.5 V; nSLEEP = 1; DISABLE =0		5	10	mA
$I_{VM(Q)}$	VM sleep mode supply current	V_{VM} = 13.5 V; nSLEEP = 0		15	30	µA
V_{DVDD}	Internal logic regulator voltage	2-mA load, V_{VM} > 5.5 V	4.7	5	5.3	V
$t_{(SLEEP)}$	Sleep time	nSLEEP low to start device shutdown	50			µs
$t_{(RESET)}$	nSLEEP reset pulse	nSLEEP low to only clear fault registers	5		20	µs
$t_{(WAKE)}$	Wake-up time	nSLEEP high to device ready for input signals			1.5	ms
t_{on}	Turn-on time	VM > $V_{(UVLO)}$; nSLEEP = 1, to output transition			1.5	ms
$t_{(DISABLE)}$	DISABLE deglitch time	DISABLE signal transition		2.5		µs
CHARGE PUMP (VCP, CPH, CPL)						
V_{VCP}	VCP operating voltage	with respect to VM		V_{VM}+5		V
I_{VCP}	VCP current	V_{VM} = 13.5 V		7	10	mA
$f_{(VCP)}$	Charge pump switching frequency	V_{VM} > $V_{(UVLO)}$; nSLEEP = 1		400		kHz
LOGIC-LEVEL INPUTS (EN/IN1, PH/IN2, nSLEEP, SCLK, SDI)						
V_{IL}	Input logic-low voltage		0		0.8	V
V_{IH}	Input logic-high voltage		1.6		5.3	V
V_{HYS}	Input logic hysteresis			150		mV
I_{IL}	Input logic-low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input logic-high current	V_{IN} = 5 V		50		µA
R_{PD}	Internal pulldown resistance	to GND		100		kΩ
t_{pd}	Propagation delay (EN/IN1, PH/IN2 to OUTx = 50%)	SR = 000b; I_O = 1 A		1.2		µs
		SR = 001b; I_O = 1 A		1.6		
		SR = 010b; I_O = 1 A		2.6		
		SR = 011b; I_O = 1 A		3.4		
		SR = 100b; I_O = 1 A		4.1		
		SR = 101b; I_O = 1 A		5.2		
		SR = 110b; I_O = 1 A		7.8		
		SR = 111b; I_O = 1 A		13.3		
LOGIC-LEVEL INPUT (DISABLE)						
$R_{PU,DIS}$	Internal pull-up resistance	DISABLE to DVDD		100		kΩ
$V_{IL,DIS}$	Input logic-low voltage		0		0.8	V
$V_{IH,DIS}$	Input logic-high voltage		1.6		5.3	V
LOGIC-LEVEL INPUT (nSCS)						

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Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL,nSCS}$	Input logic-low voltage		0		0.8	V
$V_{IH,nSCS}$	Input logic-high voltage		1.6		5.3	V
$R_{PU,nSCS}$	Internal pull-up resistance	nSCS to nSLEEP		450		kΩ
LOGIC-LEVEL INPUT (nSLEEP)						
$V_{IL,SLEEP}$	Input logic-low voltage		0		0.8	V
$V_{IH,SLEEP}$	Input logic-high voltage		2.7		5.3	V
$I_{IH,SLEEP}$	Input logic-high current	V_{IN} = 5 V; nSCS is High			80+I_{SDO} (1)	µA
THREE-LEVEL INPUT (MODE)						
R_{IN-1}	Input mode 1	Tied to GND			105	Ω
R_{IN-2}	Input mode 2	Tied to GND	190			kΩ
R_{IN-3}	Input mode 3	Tied to DVDD			105	Ω
PUSH-PULL OUTPUT (SDO)						
$R_{PD,SDO}$	Internal pull-down resistance	With respect to GND		30	50	Ω
$R_{PU,SDO}$	Internal pull-up resistance	With respect to nSLEEP		120	240	Ω
OPEN DRAIN OUTPUT (nFAULT)						
V_{OL}	Output logic-low voltage	I_O = 2 mA			0.1	V
I_{OZ}	Output high-impedance leakage	V_O = 5 V	–2		2	µA
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
$R_{DS(ON)}$	High-side FET on-resistance	V_{VM} = 13.5 V; T_A = 25°C; T_J = 25°C		75		mΩ
		V_{VM} = 13.5 V; T_A = 25°C; T_J = 150°C		125	155	
$R_{DS(ON)}$	Low-side FET on-resistance	V_{VM} = 13.5 V; T_A = 25°C; T_J = 25°C		75		mΩ
		V_{VM} = 13.5 V; T_A = 25°C; T_J = 150°C		125	155	
$t_{(DEAD)}$	Output dead time	SR = 100b		500		ns
$V_{F(DIODE)}$	Body diode forward voltage	I_O = 1 A		0.8		V
I_{SINK}	Sink current when OUTx = Hi-Z	nSLEEP = 0		62		µA
		nSLEEP = 1, DISABLE = 1		340		
SR	Slew rate (H/W Device) OUTx 10% to 90% changing	I_O = 1 A; Connect to GND		53.2		V/µs
		I_O = 1 A; $R_{(SR)}$ = 22 kΩ ± 5% to GND		34		
		I_O = 1 A; $R_{(SR)}$ = 68 kΩ ± 5% to GND		18.3		
		I_O = 1 A; No connect (Hi-Z)		13		
		I_O = 1 A; $R_{(SR)}$ = 51 kΩ ± 5% to DVDD		7.9		
		I_O = 1 A; Connect to DVDD		2.6		
SR	Slew rate (SPI Device) OUTx 10% to 90% changing	I_O = 1 A; SR = 000b		53.2		V/µs
		I_O = 1 A; SR = 001b		34		
		I_O = 1 A; SR = 010b		18.3		
		I_O = 1 A; SR = 011b		13		
		I_O = 1 A; SR = 100b		10.8		
		I_O = 1 A; SR = 101b		7.9		
		I_O = 1 A; SR = 110b		5.3		
		I_O = 1 A; SR = 111b		2.6		
CURRENT SENSE OUTPUTS (IPROPI1, IPROPI2)						
k	Current mirror scaling			1100		A/A
k_{ERR}	Current mirror scaling	I_O < 1 A	–50		50	mA
		I_O ≥ 1 A	–5		5	%

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Over recommended operating conditions unless otherwise noted. Typical limits apply for T_A = 25°C and V_{VM} = 13.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(IPROPI)}$	OUTx to IPROPI	V_O = 2 V; SR = 000b		2.2		µs
		V_O = 2 V; SR = 111b		10.5		
CURRENT REGULATION						
I_{TRIP}	Current limit threshold	ITRIP_LVL = 00b; V_{VM} = 13.5 V	3.27	3.85	4.43	A
		ITRIP_LVL = 01b; V_{VM} = 13.5 V	4.6	5.4	6.2	
		ITRIP_LVL = 10b; V_{VM} = 13.5 V	5.5	6.5	7.5	
		ITRIP_LVL = 11b; V_{VM} = 13.5 V	5.95	7	8.1	
t_{OFF}	PWM off-time	TOFF = 00b		20		µs
		TOFF = 01b		40		
		TOFF = 10b		60		
		TOFF = 11b		80		
t_{BLANK}	PWM blanking time			5		µs
PROTECTION CIRCUITS						
$V_{(UVLO)}$	VM undervoltage lockout	VM falling; UVLO report		4.35	4.45	V
		VM rising; UVLO recovery		4.5	4.7	
$t_{(UVLO)}$	VM UVLO falling deglitch time	VM falling; UVLO report		10		µs
$V_{(RST)}$	VM UVLO reset	VM falling; UVLO report; device reset			4.1	V
$V_{VCP(UV)}$	Charge pump undervoltage	V_{VM} = 12 V; T_A = 25°C; CPUV report		V_{VM} + 2.25		V
$I_{(OCP)}$	Overcurrent protection trip level		10			A
$t_{(OCP)}$	Overcurrent deglitch time			3	5	µs
$t_{(RETRY)}$	Overcurrent retry time (H/W Device)			4		ms
$t_{(RETRY)}$	Overcurrent retry time (SPI Device)	OCP_TRETRY = 00b		0.5		ms
		OCP_TRETRY = 01b		1		
		OCP_TRETRY = 10b		2		
		OCP_TRETRY = 11b		4		
V_{OLA}	Open load active mode		150	300	450	mV
$t_{d(OL)}$	Open load diagnostic delay time	OL_DLY = 0b		0.3		ms
		OL_DLY = 1b		1.2		
I_{OL}	Open load current			3		mA
T_{OTW}	Thermal warning temperature	Die temperature (T_J)	140	150	160	°C
T_{TSD}	Thermal shutdown temperature	Die Temperature (T_J)	165	175	185	°C
T_{hys}	Thermal shutdown hysteresis	Die temperature (T_J)		20		°C

(1) SDO output current external to the device

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{(READY)}$	SPI ready, VM > $V_{(UVLO)}$		1		ms
$t_{(CLK)}$	SCLK minimum period	100			ns
$t_{(CLKH)}$	SCLK minimum high time	50			ns
$t_{(CLKL)}$	SCLK minimum low time	50			ns
$t_{su(SDI)}$	SDI input setup time	20			ns
$t_{h(SDI)}$	SDI input hold time	30			ns
$t_{d(SDO)}$	SDO output delay time, SCLK high to SDO valid, C_L = 20 pF			30	ns
$t_{su(nSCS)}$	nSCS input setup time	50			ns
$t_{h(nSCS)}$	nSCS input hold time	50			ns

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		MIN	NOM	MAX	UNIT
$t_{(HI_nSCS)}$	nSCS minimum high time before active low	500			ns
$t_{dis(nSCS)}$	nSCS disable time, nSCS high to SDO high impedance		10		ns

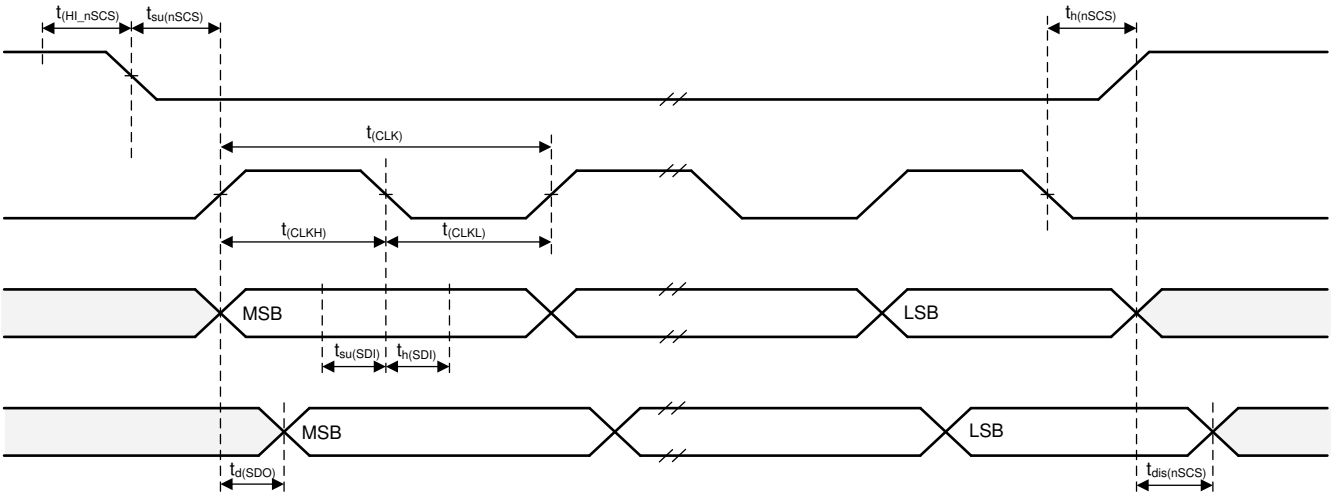


図 6-1. SPI Slave-Mode Timing Definition

6.7 Typical Characteristics

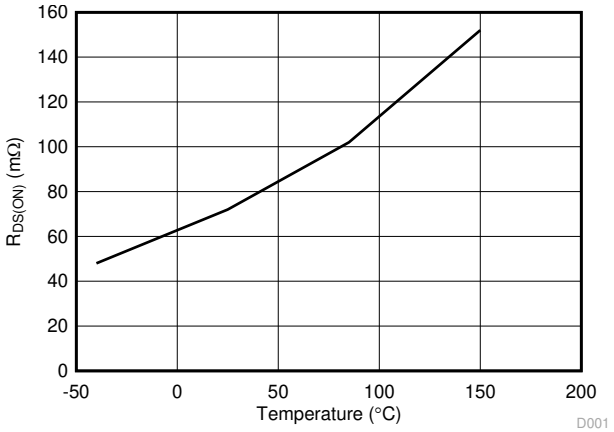


図 6-2. $R_{DS(on)}$ vs Temperature

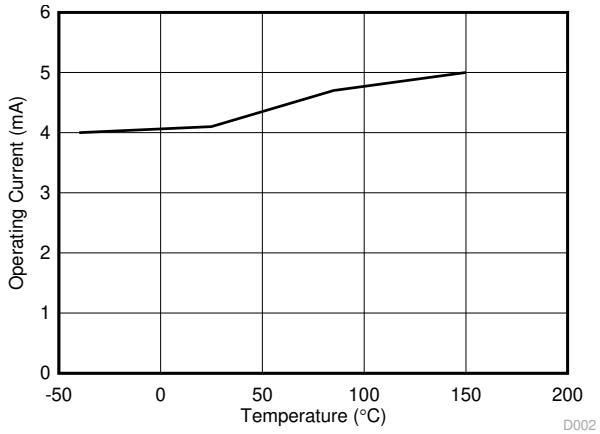


図 6-3. Operating Current (I_{VM}) vs Temperature

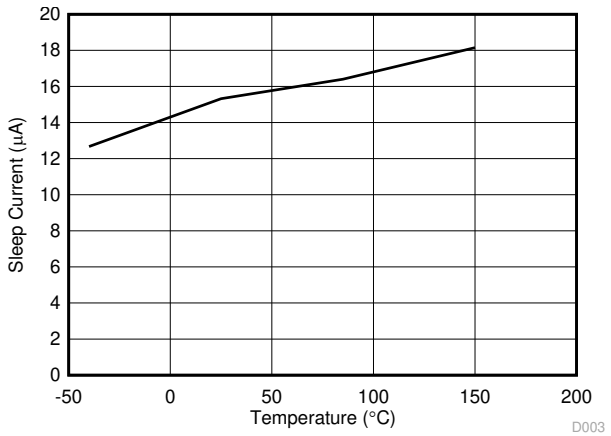
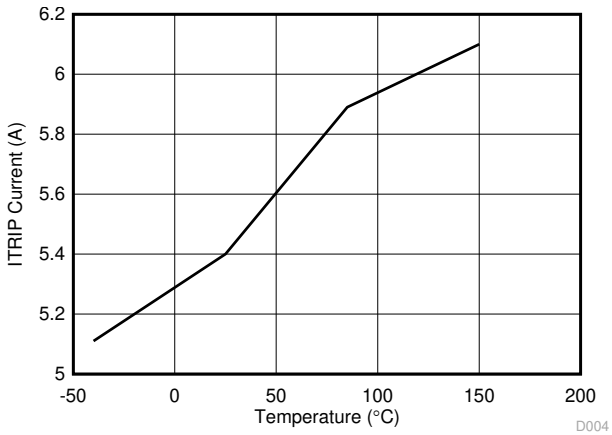
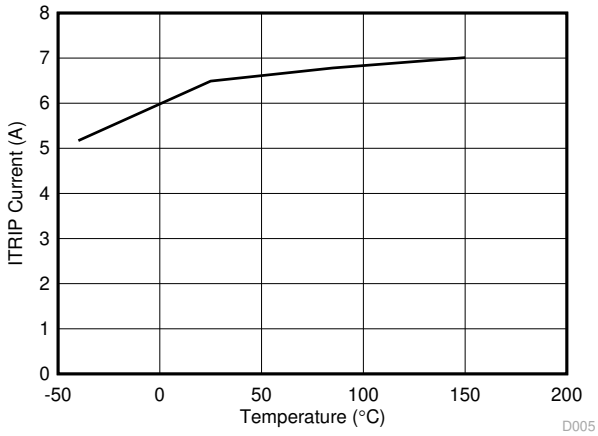


図 6-4. Sleep Current ($I_{VM(Q)}$) vs Temperature



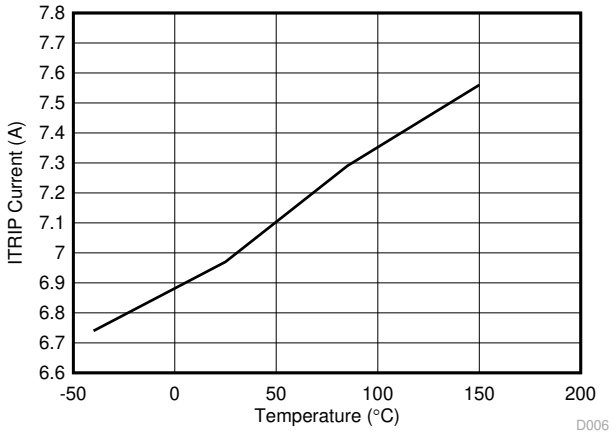
ITRIP = 01b

図 6-5. ITRIP Current vs Temperature



ITRIP = 10b

図 6-6. ITRIP Current vs Temperature



ITRIP = 11b

図 6-7. ITRIP Current vs Temperature

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7 Detailed Description

7.1 Overview

The device is an integrated, 4.5-V to 38-V motor driver for automotive brushed-motor applications. The device is capable of high output-current drive using low-$R_{DS(ON)}$ integrated MOSFETs.

A standard 4-wire serial peripheral interface (SPI) decreases the device pin count by allowing the various device settings and fault reporting to be managed through an external controller. Alternatively a hardware interface option device is available for easy configuration with less detailed control of all device functions.

The device integrates a current mirror which provides an output current proportional to the current through the high-side FETs. This feature allows the system to monitor the motor current without the need for a large high-power resistor for current sensing. The device has a built-in current regulation feature with a fixed off-time current-chopping scheme. The current-chopping level is selected through SPI in the SPI version of the device and in the hardware version of the device is it a fixed value.

In addition to the high level of driver integration, the device provides a broad range of integrated protection features. These features include power-supply undervoltage lockout (UVLO), charge-pump undervoltage lockout, overcurrent faults, open-load detection, output short to battery and short to ground protection, and thermal shutdown. Device faults are indicated by the nFAULT pin with detailed information available in the device registers.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with output slew rate control minimizes the radiated emissions from the device.

The device is available in a 24-pin HTSSOP package with a thermal pad.

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7.2 Functional Block Diagram

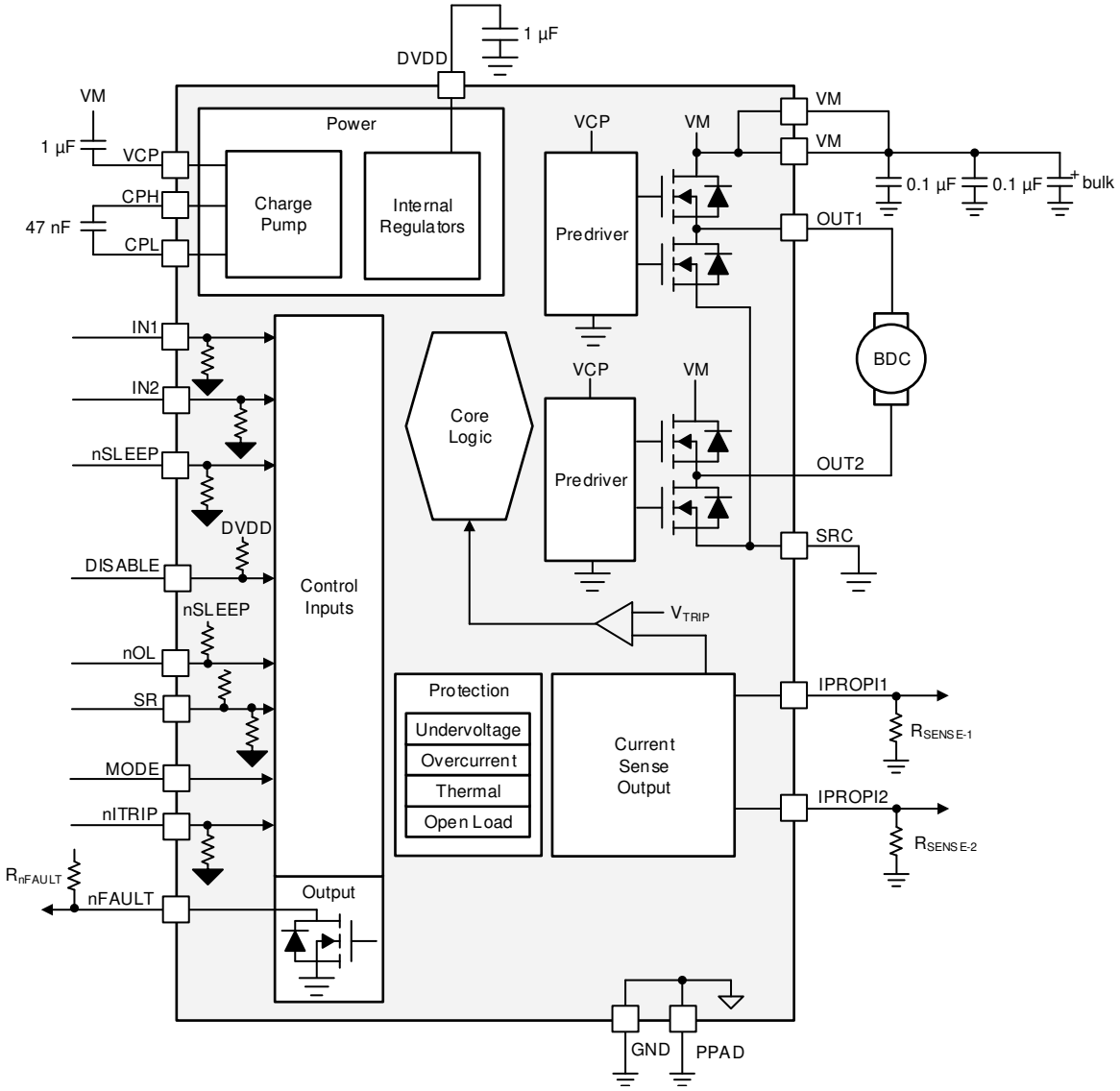


図 7-1. Hardware Device Block Diagram

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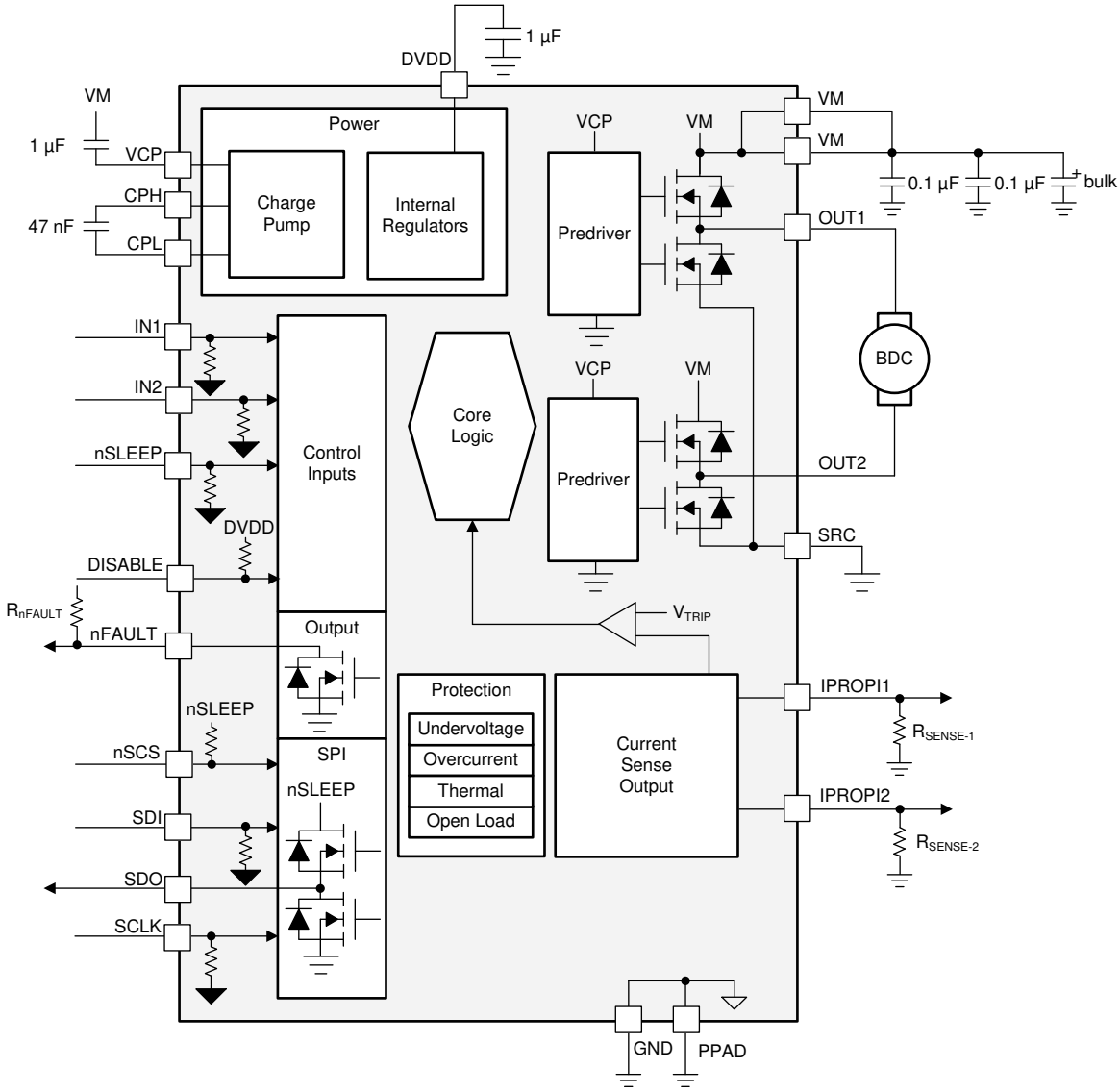


図 7-2. SPI Device Block Diagram

7.3 Feature Description

表 7-1 lists the recommended external components for the device.

表 7-1. External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	0.1-µF ceramic capacitor rated for VM
C_{VM2}	VM	GND	Bulk capacitor rated for VM
C_{VCP}	VCP	VM	16-V, 1-µF ceramic capacitor
C_{FLY}	CPH	CPL	47-nF capacitor rated for VM
C_{DVDD}	DVDD	GND	6.3-V, 1-µF ceramic capacitor
R_{nFAULT}	VCC(1)	nFAULT	≥ 10-kΩ pullup resistor
R_{MODE}	MODE	GND or DVDD	Device hardware interface
$R_{SENSE-1}$	IPROPI1	GND	Resistors to convert mirrored current into a voltage
$R_{SENSE-2}$	IPROPI2	GND	Resistors to convert mirrored current into a voltage

(1) VCC is not a pin on the device, but a VCC supply-voltage pullup is required for the open-drain output nFAULT.

7.3.1 Bridge Control

The device output has four N-channel MOSFETs configured in a H-bridge. The driver can be controlled using a PH/EN, PWM, or independent half-bridge input mode. 表 7-2 lists the control mode configurations.

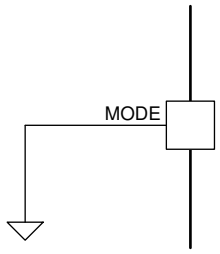
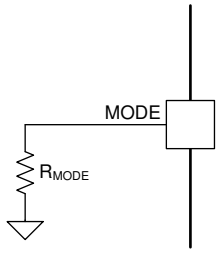
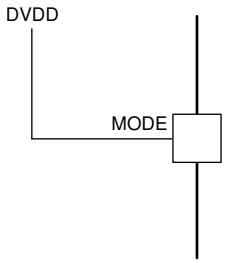
表 7-2. Control Mode Configuration

HARDWARE DEVICE MODE PIN	SPI DEVICE MODE REGISTER	CONTROL MODE
L	00b	PH/EN
H	01b (default)	PWM
200 kΩ ± 5% to GND	10b	Independent half bridge
Not applicable	11b	Input disabled, bridge Hi-Z

In the hardware version of the device, the MODE pin determines the control interface and latches on power-up or when exiting sleep mode. During the device power-up sequence, the DVDD pin is enabled first, and then the MODE pin latches. Tying the MODE pin directly to ground sets the mode to phase and enable. Tying the MODE pin to the DVDD pin, or an external 5 V rail, sets the mode to PWM. Connecting the MODE pin to ground with a 200 kΩ ± 5% resistor sets the mode to independent half-bridge where the two half-bridges can be independently controlled by their respective input (INx) pins. 表 7-3 lists the different MODE pin settings.

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表 7-3. DRV8873H-Q1 MODE Pin Settings

CONNECTION	MODE	CIRCUIT
Connect to GND	Phase and Enable	
200 kΩ ± 5% to GND	Independent half-bridge	
Connect to DVDD	PWM	

In the SPI version of the device, the mode setting can be changed by writing to the MODE register in the IC1 control register because this device version has no dedicated MODE pin. The device mode gets latched when the DISABLE signal transitions from high to low.

7.3.1.1 Control Modes

The device output consists of four N-channel MOSFETs that are designed to drive high current. The MOSFETs are controlled by two logic inputs, EN/IN1 and PH/IN2, in three different input modes to support various commutation and control methods, as shown in the logic tables (表 7-4, 表 7-5, and 表 7-6). In the Independent PWM mode, the fault handling is performed independently for each half bridge. For example, if an overcurrent condition (OCP) is detected in half-bridge 1, only the half-bridge 1 output (OUT1) is disabled and half-bridge 2 continues to operate based on the IN2 input.

表 7-4. PH/EN Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2
0	X	X	X	Hi-Z	Hi-Z
1	1	X	X	Hi-Z	Hi-Z
1	0	0	X	H	H
1	0	1	0	L	H
1	0	1	1	H	L

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表 7-5. PWM Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2
0	X	X	X	Hi-Z	Hi-Z
1	1	X	X	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z
1	0	0	1	L	H
1	0	1	0	H	L
1	0	1	1	H	H

表 7-6. Independent Mode Truth Table

nSLEEP	DISABLE	EN/IN1	PH/IN2	OUT1	OUT2
0	X	X	X	Hi-Z	Hi-Z
1	1	X	X	Hi-Z	Hi-Z
1	0	0	0	L	L
1	0	0	1	L	H
1	0	1	0	H	L
1	0	1	1	H	H

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM mode (MODE = 1), switching between driving and braking typically is best. For example, to drive a motor forward with 50% of its maximum revolutions per minute (RPM), the IN1 pin is high and the IN2 pin is low during the driving period. During the other period in this example, the IN1 pin is high and the IN2 pin is high.

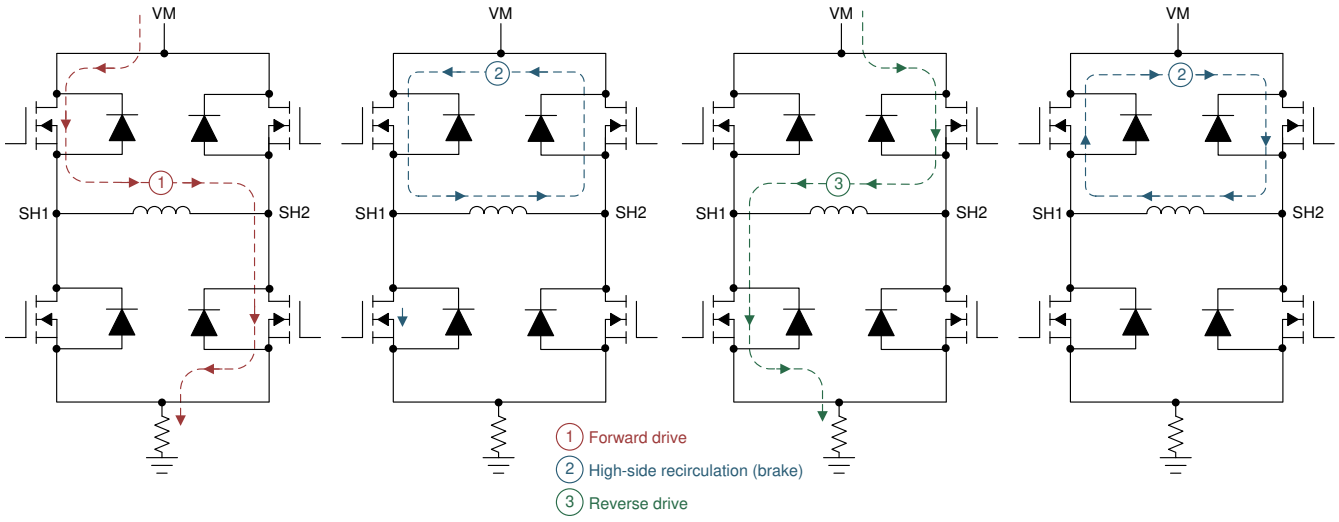


図 7-3. Half-Bridge Current Paths

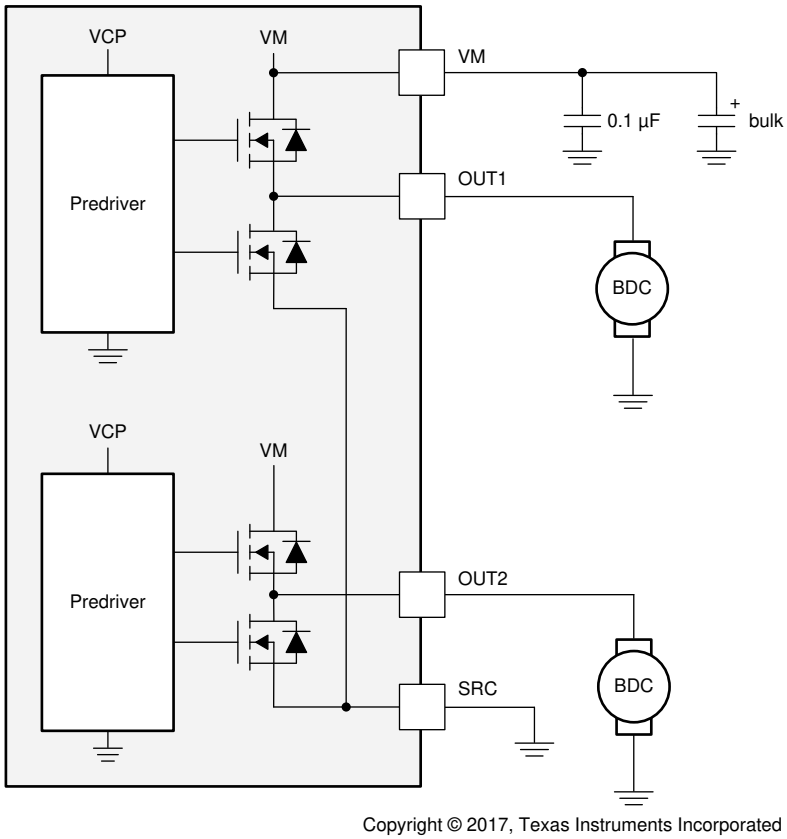
In the Independent PWM mode, to independently put the outputs of the half bridge in the high-impedance (Hi-Z) state, the OUT1_DIS or OUT2_DIS bit in the IC3 register must be set to 1b. Writing a logic 1 to the OUT1_DIS bit disables the OUT1 output. Writing a logic 1 to the OUT2_DIS bit disables the OUT2 output. The default value in these registers is 0b. The option to independently set the outputs of the half bridge in the Hi-Z state is not available for the hardware version of the device.

7.3.1.2 Half-Bridge Operation

The device can be used to drive two solenoids or unidirectional brushed DC-motor loads instead of a brushed-DC motor in full H-bridge configuration. Independent half-bridge control is preferred for operation in this mode;

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however, using the PH/EN or PWM modes is not restricted if the correct driving and braking states can be achieved.



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図 7-4. Independent Half bridge Mode Driving Two Low-Side Loads

7.3.1.3

TI does not recommend tying the OUT1 and OUT2 pins together and drive a load. The half bridges may be out of synchronization in this configuration and any mismatch in the input commands can momentarily result in shoot through condition. This mismatch can be mitigated by adding an inductor in-line with the outputs.

If loads are connected between the OUTx and VM pins, the device can draw more current than specified in the *セクション 6.5* table. To avoid this condition, TI recommends connecting loads in the configuration shown in 図 7-4.

Depending on how the loads are connected on the outputs pin, some of the features offered by the device could have reduced functionality. For example, having a load between the OUTx and GND pins, as shown in 図 7-4, results in false trips of the open-load diagnosis in active-mode (OLA). Having a load tied between the OUTx and VM pins restricts the use of internal current regulation because no means of measuring current flowing through the load with the current mirror block is available. 表 7-7 lists these use cases.

表 7-7. Control Mode Configuration

LOAD CONNECTIONS		FUNCTIONALITY	
NODE 1	NODE 2	OLA	CURRENT REGULATION (I_{TRIP})
OUTx	GND	Not Available	Operational
OUTx	VM	Operational	Not Available

7.3.1.4 Internal Current Sense and Current Regulation

The IPROPI pin outputs an analog current that is proportional to the current flowing in the H-bridge. The output current is typically 1/1100 of the current in both high-side FETs. The IPROPI pin is derived from the current through either of the high-side FETs. Because of this, the IPROPI pin does not represent the half bridge current when operating in a fast decay mode or low-side slow decay mode. The IPROPI pin represents the H-bridge current under forward drive, reverse drive, and high-side slow decay. The IPROPI output is delayed by approximately 2 µs for the fastest slew-rate setting (43.2 V/µs) after the high-side FET is switched on.

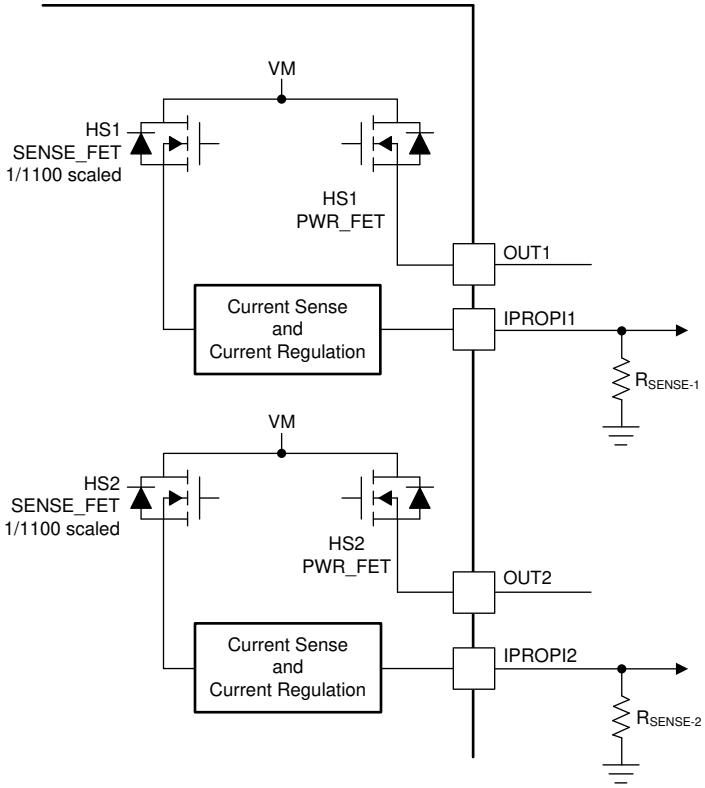


図 7-5. Current-Sense Block Diagram

The selection of the external resistor should be such that the voltage on the IPROPI pin is less than 5 V. Therefore the resistor must be sized less than this value based on 式 1. The range of current that can be monitored is from 100 mA to 10 A assuming the selected external resistor meets the calculated value from 式 1. If the current exceeds 10 A, the device could reach overcurrent protection (OCP) or overtemperature shutdown (TSD). If OCP occurs, the device disables the internal MOSFETs and protects itself (for the hardware version of the device) or based on the OCP_MODE setting (for the SPI version of the device). For guidelines on selecting a sense resistor, see the *セクション 8.2.1.3* section.

$$R_{(SENSE)} = k \times 5\ V / I_O \quad (1)$$

where

- k is the current mirror scaling factor, which is typically 1100.
- I_O is the maximum drive current to be monitored.

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注

Texas Instruments recommends the load current not exceed 8 A during normal operation. If slew rate setting of 2.6 V/µs (SR = 111b) is used when the load current is about 8 A, choose TOFF to be either 40 µs or 60 µs.

The SPI version of the device limits the output current based on the trip level set in the SPI registers. In the hardware version of the device, the current trip limit is set to 6.5 A. The current regulation feature is enabled by default on both the outputs (OUT1 and OUT2). To disable current regulation in the hardware version of the device, the nITRIP pin must be connected to DVDD. To disable current regulation in the SPI version of the device, the DIS_ITRIP bits in the IC4 Control register must be written to. The bit settings are:

- 01b to disable current regulation only on the OUT1 pin
- 10b to disable current regulation only on the OUT2 pin
- 11b to disable current regulation on both the OUT1 and OUT2 pins

表 7-8. Control Regulation Threshold

PARAMETER		ITRIP_LVL BIT	MIN	TYP	MAX	UNIT
I_{TRIP}	Current limit threshold	ITRIP_LVL = 00b	3.4	4	4.6	A
		ITRIP_LVL = 01b	4.6	5.4	6.2	A
		ITRIP_LVL = 10b	5.5	6.5	7.5	A
		ITRIP_LVL = 11b	6	7	8	A

When the I_{TRIP} current has been reached, the device enforces slow current decay by enabling both the high-side FETs for a time of t_{OFF} . In the hardware version of the device, the t_{OFF} time is 40 µs. The t_{OFF} time is selectable through SPI in the SPI version of the device, as shown in 表 7-9. The default setting is 01b (t_{OFF} = 40 µs).

表 7-9. PWM Off Time Settings

PARAMETER		TOFF BIT	t_{OFF} DURATION	UNIT
t_{OFF}	PWM off time	TOFF = 00b	20	µs
		TOFF = 01b	40	µs
		TOFF = 10b	60	µs
		TOFF = 11b	80	µs

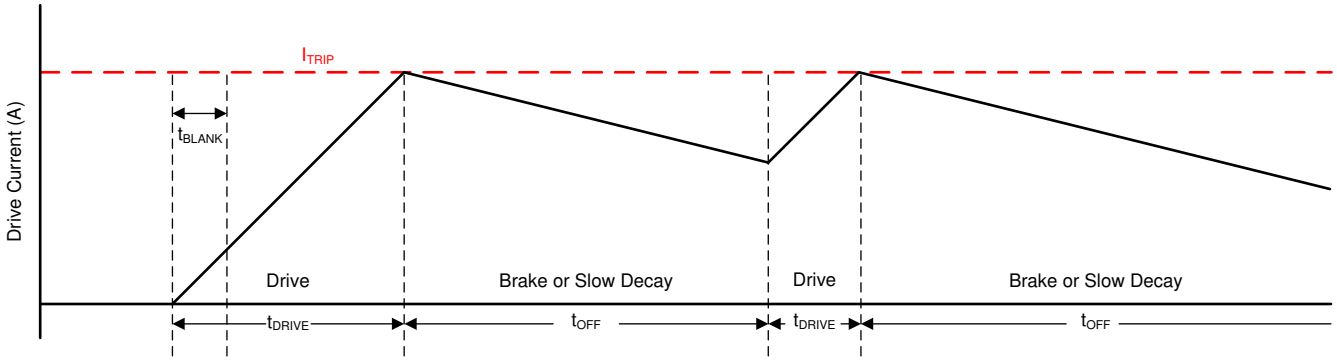


図 7-6. Current Regulation Time Periods

When the t_{OFF} time has elapsed and the current level falls below the current regulation (I_{TRIP}) level, the output is re-enabled according to the inputs. If, after the t_{OFF} time has elapsed the current is still higher than the I_{TRIP} level, the device enforces another t_{OFF} time period of the same duration.

The drive time (t_{DRIVE}) occurs until another ITRIP event is reached and depends heavily on the VM voltage, the back-EMF of the motor, and the inductance of the motor. During the t_{DRIVE} time, the current-sense regulator does not enforce the ITRIP limit until the t_{BLANK} time has elapsed. While in current regulation, the inputs can be

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toggled to drive the load in the opposite direction to decay the current faster. For example, if the load was in forward drive prior to entering current regulation it can only go into reverse drive when the driver enforces current regulation.

The IPROPI1 pin represents the current flowing through the HS1 MOSFET of half-bridge 1. The IPROPI2 pin represents the current flowing through the HS2 MOSFET of half-bridge 2. To measure current with one sense resistor, the IPROPI1 and IPROPI2 pins must be connected together with the R_{SENSE} resistor as shown in 図 7-7. In this configuration, the current-sense output is proportional to the sum of the currents flowing through the both high-side FETs.

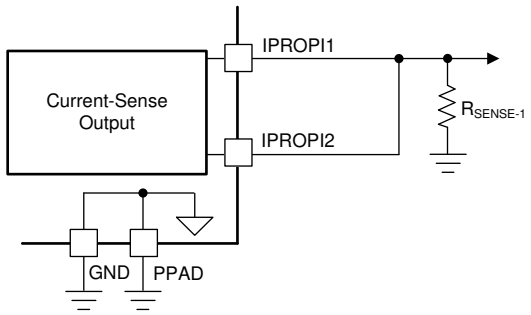
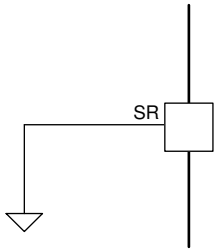
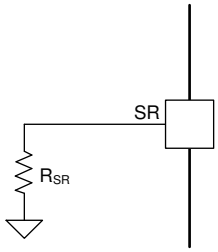


図 7-7. Current Sense Output

7.3.1.5 Slew-Rate Control

The rise and fall times (t_r and t_f) of the outputs can be adjusted on the hardware version of the device by changing the value of an external resistor connected from the SR pin to ground. On the SPI version of the device, the slew rate can be adjusted through the SPI. The output slew rate is adjusted internally to the device by controlling the ramp rate of the driven FET gate. The voltage or resistance on the SR pin sets the output rise and fall times in the hardware version of the device.

表 7-10. DRV8873H-Q1 Slew Rate (SR) Pin Connections

CONNECTION	SR	CIRCUIT
Connect to GND	53.2 V/µs	
22 kΩ ± 5% to GND	34 V/µs	

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表 7-10. DRV8873H-Q1 Slew Rate (SR) Pin Connections (continued)

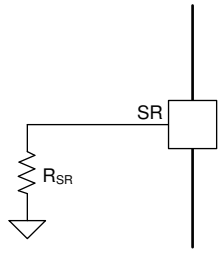
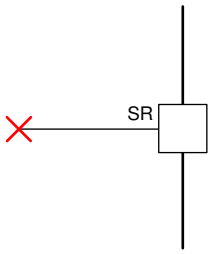
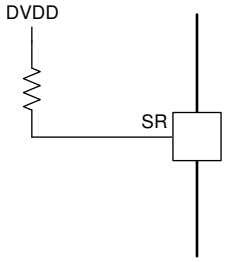
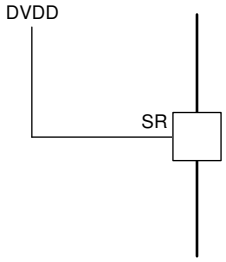
CONNECTION	SR	CIRCUIT
68 kΩ ± 5% to GND	18.3 V/µs	
> 2 MΩ to GND (Hi-Z)	13 V/µs	
51 kΩ ± 5% to DVDD	7.9 V/µs	
Connect to DVDD	2.6 V/µs	

図 7-8 shows the internal circuit block for the SR pin.

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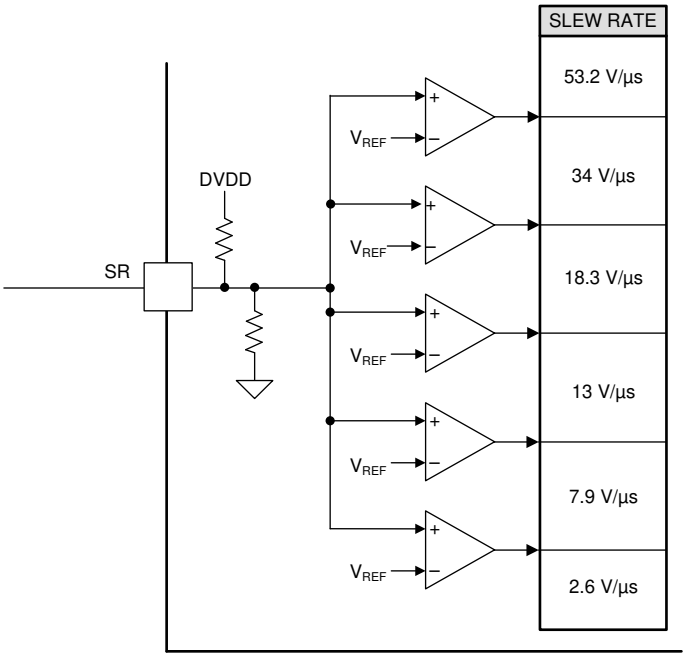


図 7-8. SR Block Diagram

表 7-11 lists the settings in the SPI register that set the output rise and fall times in the SPI version of the device.

表 7-11. DRV8873S-Q1 Slew Rate Settings

SR	RISE TIME (V/µs)	FALL TIME (V/µs)
000b	53.2	53.2
001b	34	34
010b	18.3	18.3
011b	13	13
100b	10.8	10.8
101b	7.9	7.9
110b	5.3	5.3
111b	2.6	2.6

The typical voltage on the SR pin is 3 V and is driven internally. Changing the resistor value on the SR pin changes the slew-rate setting from approximately 2.6 V/µs to 53.2 V/µs. The recommended values for the external resistor are shown in the *セクション 7.3.3.2* section. If the SR pin is grounded then the slew rate is 53.2 V/µs. Leaving the SR pin as a no-connect pin sets the slew rate to 13 V/µs. Tying it to the DVDD pin sets the slew rate to 2.6 V/µs.

7.3.1.6 Dead Time

The dead time ($t_{(DEAD)}$) is measured as the time when the OUTx pin is in the Hi-Z state between turning off one of the half bridge MOSFETs and turning on the other. For example, the output is in the Hi-Z state between turning off the high-side MOSFET and turning on the low-side MOSFET, or turning on the high-side MOSFET and turning off the low-side MOSFET.

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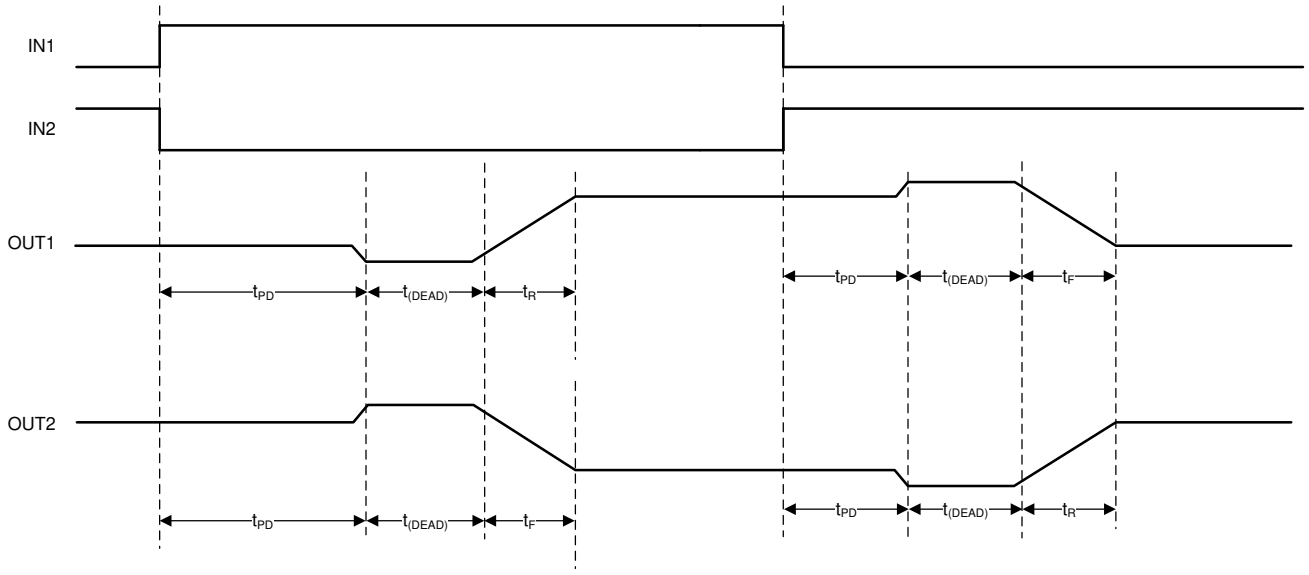


図 7-9. Propagation Delay Time

If the output pin is measured during the t_{DEAD} time the voltage depends on the direction of the current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. The diode drop is associated with the body diode of the high-side or the low-side FET. The dead time is dependent on the slew-rate setting because a portion of the FET gate ramp includes the observable dead time.

7.3.1.7 Propagation Delay

The propagation delay time (t_{PD}) is measured as the time between an input edge to an output change. This time comprises two parts: an input deglitcher and output slewing delay. The input deglitcher prevents noise on the input pins from affecting the output state. The adjustable slew rate also contributes to the propagation delay time. For the fastest slew-rate setting, the t_{PD} time is typically 1.5 µs, and for the slowest slew-rate setting, the t_{PD} time is typically 4.5 µs. For the output to change state during normal operation, one FET must first be turned off.

7.3.1.8 nFAULT Pin

The nFAULT pin has an open-drain output and should be pulled up to a 5-V or 3.3-V supply. When a fault is detected, the nFAULT line is logic low. For a 5-V pullup the nFAULT pin can be tied to the DVDD pin with a resistor (see the *セクション 8* section). For a 3.3-V pullup, an external 3.3-V supply must be used.

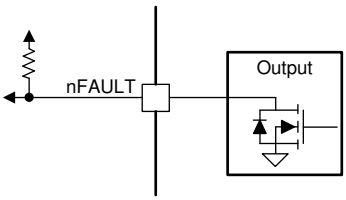


図 7-10. nFAULT Pin

During the device power-up sequence, or when exiting sleep mode, the nFAULT pin is held low until the digital core is alive and functional. This low level signal on the nFAULT line does not represent a fault condition. The signal can be used by the external MCU to determine when the digital core of the device is ready; however, this does not mean that the device is ready to accept input commands via the INx pins.

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7.3.1.9 nSLEEP as SDO Reference

The nSLEEP pin manages the state of the device. The device goes into sleep mode with a logic-low signal, and comes out of sleep mode when the nSLEEP pin goes high. The signal level when the nSLEEP pin goes high determines the logic level on the SDO output in the SPI version of the device. A 3.3-V signal on the nSLEEP pin provides a 3.3-V output on the SDO output. A 5-V signal on the nSLEEP pin provides a 5-V output on the SDO pin. If the sleep feature is not required, the nSLEEP pin can be connected to the MCU power supply. In that case, when the MCU is powered-up, the motor driver device is also be powered-up.

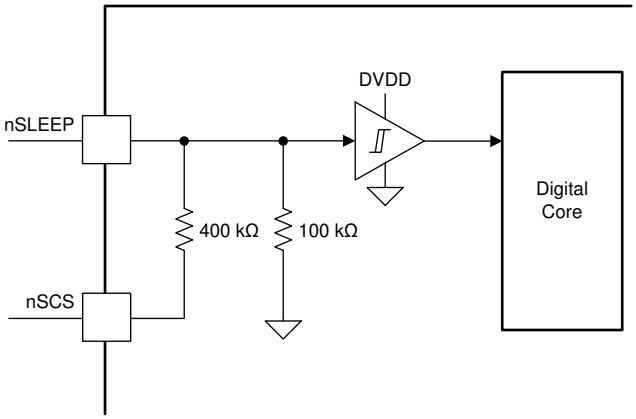


図 7-11. nSCS and nSLEEP Circuit

In the SPI version of the device, if the nSLEEP reset pulse is used to clear faults, the SDO voltage reference is not available for the duration of the nSLEEP reset pulse. No data can be transmitted on the SDO line for the duration when the nSLEEP pin is held low. Therefore, TI recommends using the CLR_FLT bit in the IC3 control register to clear the faults.

7.3.2 Motor Driver Protection Circuits

The device is protected against VM undervoltage conditions, charge-pump undervoltage conditions, overcurrent events, and overtemperature events.

7.3.2.1 VM Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the UVLO-threshold voltage, $V_{(UVLO)}$, for the voltage supply, all the outputs (OUTx) are disabled, and the nFAULT pin is driven low. The charge pump is disabled in this condition. The FAULT and UVLO bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VM undervoltage condition is removed. The UVLO bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse.

注

During the power-up sequence VM must exceed $V_{(UVLO)}$ recovery max limit in order to power-up and function properly. After a successful power-up sequence, the device can operate down to the $V_{(UVLO)}$ report limit before going into the undervoltage lockout condition.

7.3.2.2 VCP Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin falls below the $V_{VCP(UV)}$ voltage for the charge pump, all the outputs (OUTx) are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. The FAULT and CPUV bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the VCP undervoltage condition is removed. The CPUV bit remains set until it is cleared through the CLR_FLT bit or an nSLEEP reset pulse. This protection feature can be disabled by setting the DIS_CPUV bit high.

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7.3.2.3 Overcurrent Protection (OCP)

If the current in any FET exceeds the $I_{(ocp)}$ limits for longer than the $t_{(OCP)}$ time, all FETs in the half bridge are disabled and the nFAULT pin is driven low. The charge pump remains active during this condition. The overcurrent protection can operate in four different modes: latched shutdown, automatic retry, report only, and disabled. In the independent PWM mode (MODE = 10b or MODE pin to ground with a 200-kΩ ± 5% resistor) the fault handling is performed independently for each half-bridge based on the OCP mode selected. This protection scheme protects the outputs from shorts to battery and shorts to ground.

7.3.2.3.1 Latched Shutdown (OCP_MODE = 00b)

In this mode, after an OCP event, all the outputs (OUTx) are disabled and the nFAULT pin are driven low. The FAULT, OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes (motor-driver operation and nFAULT released) when the OCP condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for an OCP event for both the hardware version and SPI version of the device.

7.3.2.3.2 Automatic Retry (OCP_MODE = 01b)

In this mode, after an OCP event all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding MOSFET OCP bits are latched high in the SPI registers. Normal operation resumes automatically (motor-driver operation and nFAULT released) after the $t_{(RETRY)}$ time has elapsed and the fault condition is removed.

7.3.2.3.3 Report Only (OCP_MODE = 10b)

In this mode, no protective action is performed when an overcurrent event occurs. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding MOSFET OCP bits high in the SPI registers. The motor driver continues to operate. The external controller acts appropriately to manage the overcurrent condition. The reporting is cleared (nFAULT released) when the OCP condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse.

7.3.2.3.4 Disabled (OCP_MODE = 11b)

In this mode, no protective or reporting action is performed when an overcurrent event occurs. The device continues to drive the load based on the input signals.

7.3.2.4 Open-Load Detection (OLD)

If the motor is disconnected from the device, an open-load condition is detected and the nFAULT pin is latched low until a clear faults command is issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse. The fault also clears when the device is power cycled or comes out of sleep mode. The OLD test is designed for applications that have capacitance less than 15 nF when the OLP_DLY bit set to 0b and for less than 60 nF when the OLP_DLY bit is set to 1b on the OUTx pins. This setting is equivalent to measuring the resistance values listed in 表 7-12.

表 7-12. Resistance for Open Load Detection

NODE 1	NODE 2	RESISTANCE	COMMENTS
OUT1	OUT2	2 kΩ	
OUTx	VM	12 kΩ	V_{VM} = 13.5 V
OUTx	GND	3 kΩ	

Open load detection works in both standby mode (OLP) and active mode (OLA). OLP detects the presence of the motor prior to commutating the motor. OLA detects the motor disconnection from the driver during commutation.

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7.3.2.4.1 Open-Load Detection in Passive Mode (OLP)

The open-load passive diagnostic (OLP) is different for the hardware and SPI version of the device. The OLP test is available in all three modes of operation (PN/EN, PWM, and independent half-bridge). When the open-load test is running, the internal power MOSFETs are disabled.

For the hardware version of the device, the OLP test is performed at power-up or after exiting sleep mode if the nOL pin is left as a no connect pin (or tied to GND). If the nOL pin is tied to the DVDD pin (or an external 5-V rail), the OLP test is not performed by the device.

For the SPI version of the device, the OLP test is performed when commanded. The following sequence shows how to perform the OLP test directly after the device powers up:

1. Power up the device (DISABLE pin high).
2. Select the mode through SPI.
3. Wait for the $t_{(DISABLE)}$ time to expire.
4. Write 1b to the EN_OL bit in the IC1 register.
5. Perform the OLP test.
   - If an open load (OL) is detected, the nFAULT pin is driven low, the FAULT and OLx bits are latched high. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse which resets the OLx register bit.
   - If an OL condition is not detected, the EN_OL bits return to the default setting (0b) after the $t_{d(OL)}$ time expires.
6. Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

If an open-load diagnostic is performed at any other time, the following sequence must be followed:

1. Set the pin DISABLE high (to disable the half bridge outputs).
2. Wait for the $t_{(DISABLE)}$ time to expire.
3. Write 1b to the EN_OL bit in the IC1 register.
4. Perform the OLP test.
   - If an OL condition is detected, the nFAULT pin is driven low, and the FAULT and OLx bits are latched high. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse which resets the OLx register bits.
   - If an OL condition is not detected, the EN_OL bits return to the default setting (0b) after the $t_{d(OL)}$ time expires.
5. Set the DISABLE pin low so that the device drives the motor or load based on the input signals.

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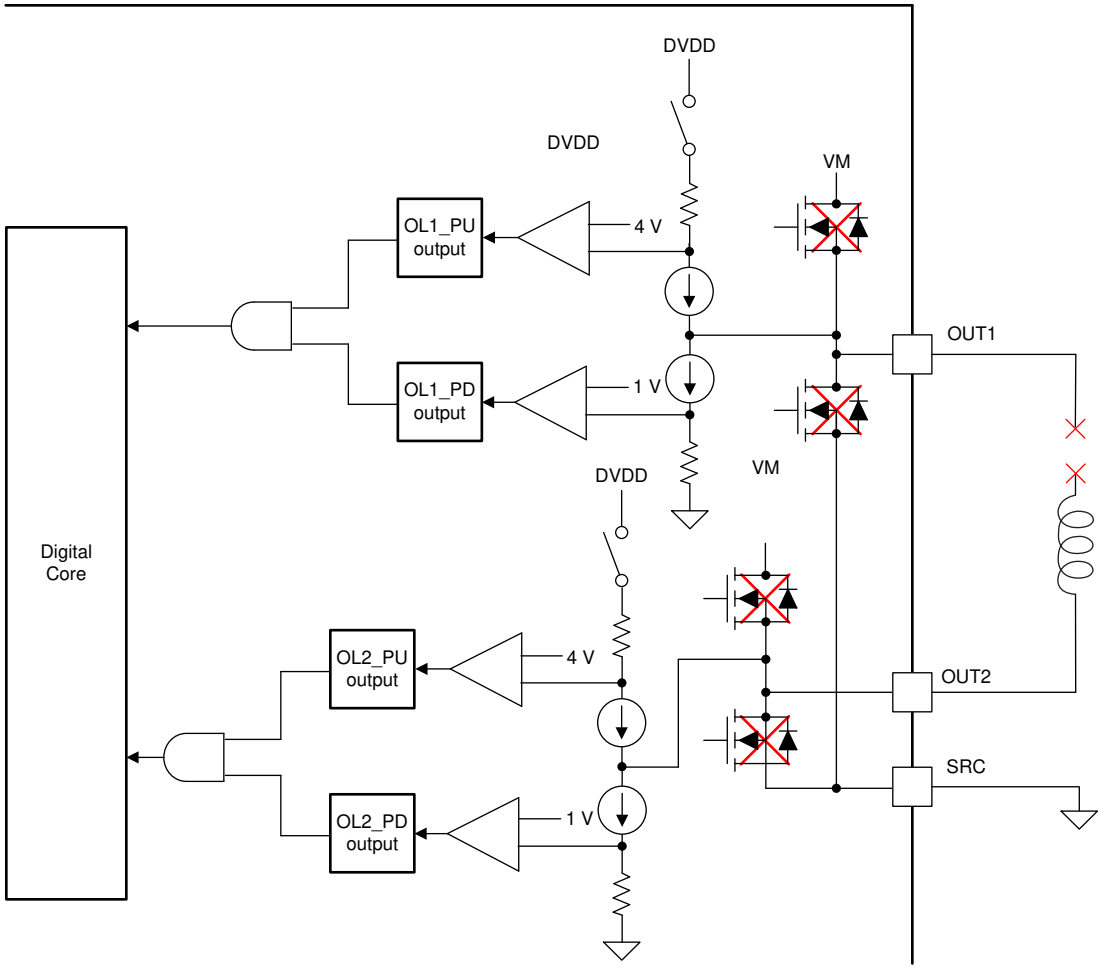


図 7-12. Open-Load Detection Circuit

The EN_OL register maintains the written command until the diagnostic is complete. The signal on the DISABLE pin must remain high for the entire duration of the test. While the OLP test is running, if the DISABLE pin goes low, the OLP test is aborted to resume normal operation and no fault is reported. The OLP test is not performed if the motor is energized.

The OLD test checks for a high-impedance connection on the OUTx pins. The diagnostic runs in two steps. First the pullup current source is enabled. If a load is connected, the current passes through the pullup resistor and the OLx_PU comparator output remains low. If an OL condition exists, the current through the pullup resistor goes to 0 A and the OLx_PU comparator trips high. Second the pulldown current source is enabled. In the same way, the OLx_PD comparator output either remains low to indicate that a load is connected, or trips high to indicate an OL condition.

If both the OLx_PU and OLx_PD comparators report an OL condition, the OLx bit in the SPI register latches high and the nFAULT line goes low to indicate an OL fault. When the OL condition is removed, a clear faults command must be issued by the MCU either through the CLR_FLT bit or an nSLEEP reset pulse which resets the OL1 and OL2 register bits. The charge pump remains active during this fault condition.

7.3.2.4.2 Open-Load Detection in Active Mode (OLA)

Open load in active mode is detected when the OUT1 and OUT2 voltages do not exhibit overshoot greater than the V_{OLA} over VM between the time the low-side FET is switched off and the high-side FET is switched on during an output PWM cycle, as shown in 図 7-13. An open load is not detected if the energy stored in the inductor is high enough to cause an overshoot greater than the V_{OLA} over VM caused by the flyback current flowing through

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the body diode of the high-side FET. The OLA diagnostic is disabled by default and can be enabled by writing a 1b to the EN_OLA bit in IC4 control register.

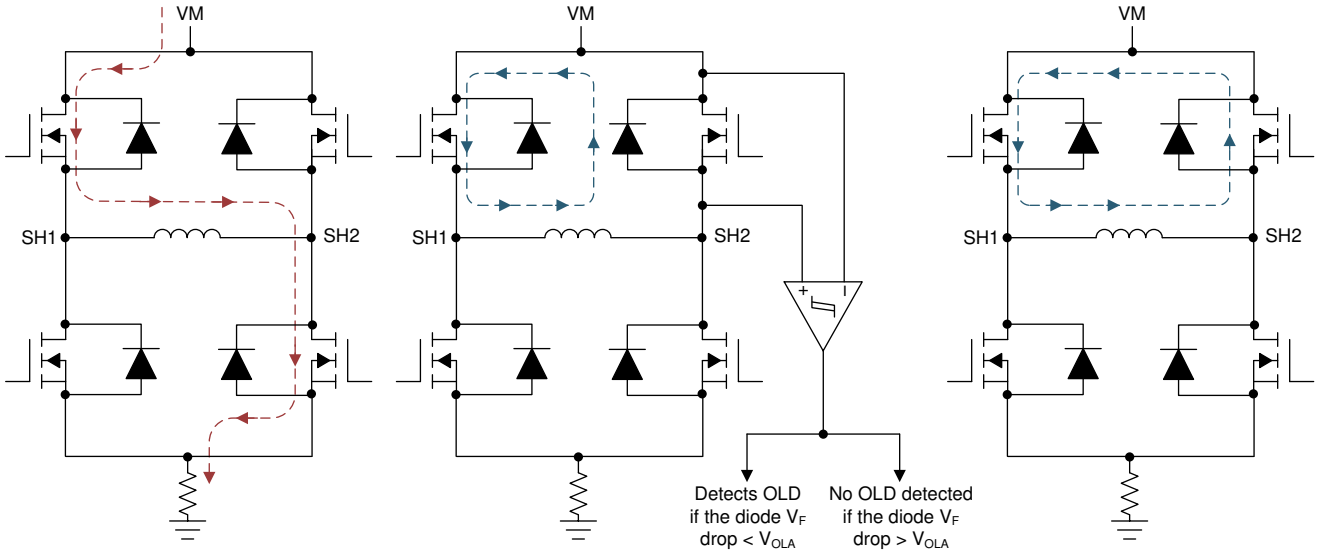


図 7-13. Open-Load Active Mode Circuit

In PH/EN and PWM mode, the motor current decays by high-side recirculation. In independent PWM mode, the motor can enter the brake state either by high-side or low-side recirculation. If the motor enters the brake state using low-side recirculation, the diode V_F voltage of high-side FET is less than the V_{OLA} voltage which flags an open load fault even though the load is connected across the OUT1 and OUT2 pins. In this case, the OLA mode should not be used. If high-side current recirculation is done with independent PWM mode, the OLA mode functions properly.

注

The OLA mode is functional only when high-side recirculation of the motor current occurs. Depending on the operation conditions and external circuitry, such as the output capacitors, an open load condition could be indicated even though the load is present. This case might occur, for example, during a direction change or for small load currents with respectively small PWM duty cycles. Therefore, TI recommends evaluating the open load diagnosis only in known, suitable operating conditions and to ignore it otherwise.

To avoid inadvertently triggering the open load diagnosis, a failure counter is implemented. Three consecutive occurrences of the internal open-load signal must occur, essentially three consecutive PWM pulses without freewheeling detected, before an open load condition is reported by the nFAULT pin and in the SPI register.

In the hardware version of the device, OLA mode is active when the nOL pin is left as a no-connect pin or tied to ground. If low-side current recirculation is done with independent PWM control, an open load condition is detected even though the load is connected. To avoid this false trip, the OLD must be disabled by taking the nOL pin high; however, both OLA and OLP diagnostics will be disabled.

7.3.2.5 Thermal Shutdown (TSD)

If the die temperature exceeds the thermal shutdown limit, the half bridge are disabled, and the nFAULT pin is driven low. The charge pump remains active during this condition. In addition, the FAULT bit and TSD bit are latched high. This protection feature cannot be disabled. The overtemperature protection can operate in two different modes: latched shutdown and automatic recovery.

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7.3.2.5.1 Latched Shutdown (TSD_MODE = 0b)

In this mode, after a TSD event all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT and TSD bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the TSD condition is removed and a clear faults command has been issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for a TSD event in the SPI version of the device.

7.3.2.5.2 Automatic Recovery (TSD_MODE = 1b)

In this mode, after a TSD event all the outputs (OUTx) are disabled and the nFAULT pin is driven low. The FAULT and TSD bits are latched high in the SPI register. Normal operation resumes (motor-driver operation and the nFAULT line released) when the junction temperature falls below the overtemperature threshold limit minus the hysteresis (T_{TSD} – T_{HYS}). The TSD bit remains latched high indicating that a thermal event occurred until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse. This mode is the default mode for a TSD event in the hardware version of the device.

7.3.2.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}) the OTW bit is set in the registers of SPI devices. The device performs no additional action and continues to function. When the die temperature falls below the hysteresis point of the thermal warning, the OTW bit clears automatically. The OTW bit can also be configured to report on the nFAULT pin, and set the FAULT bit in the SPI version of the device, by setting the OTW_REP bit to 1b through the SPI registers. The charge pump remains active during this condition.

表 7-13. Fault Response

FAULT	CONDITION	CONFIGURATION	REPORT	HALF BRIDGE	LOGIC	RECOVERY
VM undervoltage (UVLO)	V_{VM} < $V_{(UVLO)}$ (maximum 4.45 V)	—	nFAULT	Hi-Z	Reset	Automatic: V_{VM} > $V_{(UVLO)}$ (maximum 4.55 V)
Charge pump undervoltage (CPUV)	V_{VCP} < $V_{VCP(UV)}$ (typical V_{VM} + 2.25 V)	DIS_CPUV = 0b	nFAULT	Hi-Z	Active	Automatic: V_{VCP} > $V_{VCP(UV)}$ (typical V_{VM} + 2.25 V)
		DIS_CPUV = 1b	none	Active	Active	No action
Overcurrent (OCP)	I_O > $I_{(OCP)}$ (minimum 10 A)	OCP_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: $t_{(RETRY)}$
		OCP_MODE = 10b	nFAULT	Active	Active	No action
		OCP_MODE = 11b	none	Active	Active	No action
Open load (OLD)	No load detected	EN_OLP = 1b	nFAULT	Active	Active	Latched: CLR_FLT/ nSLEEP
		EN_OLA = 1b	nFAULT	Active	Active	Latched: CLR_FLT/ nSLEEP
Current regulation (ITRIPx)	I_O > ITRIP_LVL	ITRIP_REP = 0b	none	Active	Active	No action
		ITRIP_REP = 1b	nFAULT	Active	Active	No action
Thermal shutdown (TSD)	T_J > T_{TSD} (minimum 165°C)	TSD_MODE = 0b	nFAULT	Hi-Z	Active	Latched: CLR_FLT/ nSLEEP
		TSD_MODE = 1b	nFAULT	Hi-Z	Active	Automatic: T_J > T_{TSD} – T_{HYS} (T_{HYS} typical 20°C)

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表 7-13. Fault Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	HALF BRIDGE	LOGIC	RECOVERY
Thermal Warning (OTW)	$T_J > T_{OTW}$ (minimum 140°C)	OTW_REP = 0b	none	Active	Active	No action
		OTW_REP = 1b	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{HYS}$

7.3.3 Hardware Interface

The hardware-interface device option lets the device be configured without a SPI, however not all of the functionality is configurable. The following configuration settings are fixed for the hardware interface device option:

- CPUV is enabled
- OCP_MODE is latched shutdown
- TSD_MODE is automatic recovery
- OLP_DLY is 300 µs
- ITRIP level is 6.5-A if current regulation is enabled by the nITRIP pin
- OLA is activated when the open load diagnostic is enabled by the nOL pin
- No option to independently set the outputs (OUTx) to the Hi-Z state

7.3.3.1 MODE (Tri-Level Input)

The MODE pin of the hardware version of the device determines the control interface and latches on power-up or when exiting sleep mode. 表 7-14 lists the different control interfaces that can be set with the MODE pin.

表 7-14. DRV8873H-Q1 MODE Settings

MODE	CONTROL MODE
L	PH/EN
H	PWM
Hi-Z (200 kΩ ± 5% to GND)	Independent half bridge

When the MODE pin is latched on power-up or when exiting sleep mode; any additional changes to the signal at the MODE pin are ignored by the device. To change the mode settings, a power cycle or sleep reset must be performed on the device. To use the device in PWM mode, tie the MODE pin to either the DVDD pin or an external 5-V rail. To use the device in independent half-bridge mode, the MODE pin must be connected to with a 200-kΩ ± 5% resistor (or left as a no connect). Tying the MODE pin to the GND pin puts the device in phase and enable (PH/EN) mode.

7.3.3.2 Slew Rate

The rise and fall times of the outputs can be selected based on the configuration listed in 表 7-15 for the hardware version of the device.

表 7-15. Slew Rate Settings in H/W Device

SR PIN CONNECTION	RISE TIME (V/µs)	FALL TIME (V/µs)
Connect to GND	53.2	53.2
22 kΩ ± 5% to GND	34	34
68 kΩ ± 5% to GND	18.3	18.3
> 2MΩ to GND (Hi-Z)	13	13
51 kΩ ± 5% to DVDD	7.9	7.9
Connect to DVDD	2.6	2.6

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7.4 Device Functional Modes

7.4.1 Motor Driver Functional Modes

7.4.1.1 Sleep Mode (nSLEEP = 0)

The nSLEEP pin sets the state of the device. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all the internal MOSFETs are disabled, DVDD output is disabled; the charge pump is disabled, and the SPI is disabled. The $t_{(SLEEP)}$ time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device goes from sleep mode automatically if the nSLEEP pin is brought high. The $t_{(WAKE)}$ time must elapse before the device is ready for inputs.

7.4.1.2 Disable Mode (nSLEEP = 1, DISABLE = 1)

The DISABLE pin is used to enable or disable the half bridge in the device. When the DISABLE pin is high, the output drivers are disabled in the Hi-Z state. In this mode, the open-load diagnostic can be performed for the SPI version of the device because the SPI remains active.

7.4.1.3 Operating Mode (nSLEEP = 1, DISABLE = 0)

When the nSLEEP pin is high, the DISABLE pin is low, and VM > $V_{(UVLO)}$, the device enters the active mode. The $t_{(WAKE)}$ time must elapse before the device is ready for inputs. In this mode, the charge pump and low-side gate regulator are enabled.

7.4.1.4 nSLEEP Reset Pulse

In addition to the CLR_FLT bit in the SPI register, a latched fault can be cleared through a quick nSLEEP pulse. This pulse must be greater than the nSLEEP deglitch time of 5 µs and shorter than 20 µs. If nSLEEP is low for longer than 20 µs, the faults are cleared and the device may or may not shutdown, as shown in the timing diagram (see 図 7-14). This reset pulse resets any SPI faults and does not affect the status of the charge pump or other functional blocks.

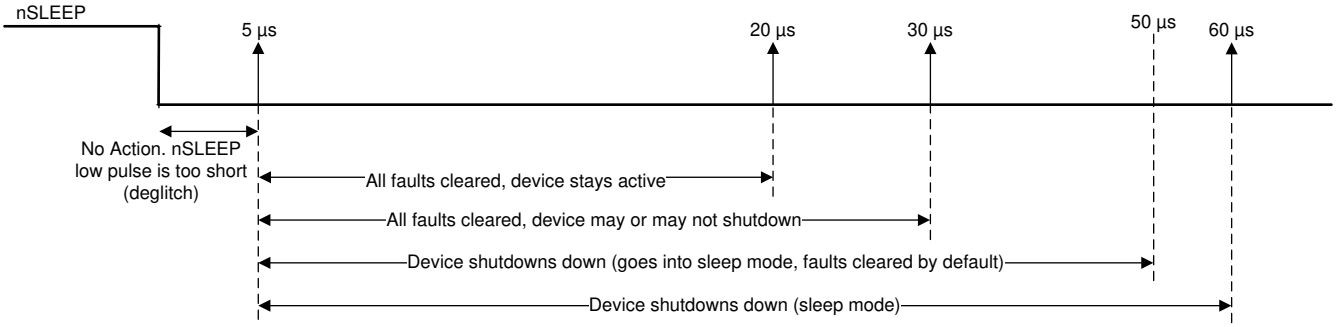


図 7-14. nSLEEP Reset Pulse

7.5 Programming

7.5.1 Serial Peripheral Interface (SPI) Communication

The SPI version of the device has full duplex, 4-wire synchronous communication. This section describes the SPI protocol, the command structure, and the control and status registers. The device can be connected with the MCU in the following configurations:

- One slave device
- Multiple slave devices in parallel connection
- Multiple slave devices in series (daisy chain) connection

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit 14)
- 5 address bits, A (bits 13 through 9)
- 8 data bits, D (bits 7 through 0)

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The SDO output-data word is 16 bits long and the first 8 bits make up the Status Register (S1). The Report word (R1) is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read

表 7-16. SDI Input Data Word Format

	R/W	ADDRESS						DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	W0	A4	A3	A2	A1	A0	X	D7	D6	D5	D4	D3	D2	D1	D0

表 7-17. SDO Output Data Word Format

STATUS								REPORT							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	OTW	UVLO	CPUV	OCP	TSD	OLD	D7	D6	D5	D4	D3	D2	D1	D0

7.5.1.2 SPI for a Single Slave Device

The SPI is used to set device configurations, operating parameters, and read out diagnostic information. The device SPI operates in slave mode. The SPI input-data (SDI) word consists of a 16-bit word, with 8 bits command and 8 bits of data. The SPI output data (SDO) word consists of 8 bits of status register with fault status indication and 8 bits of register data. 図 7-15 shows the data sequence between the MCU and the SPI slave driver.

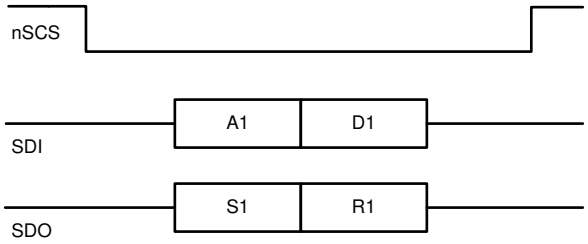


図 7-15. SPI Transaction Between MCU and SPI version of the device

A valid frame must meet the following conditions:

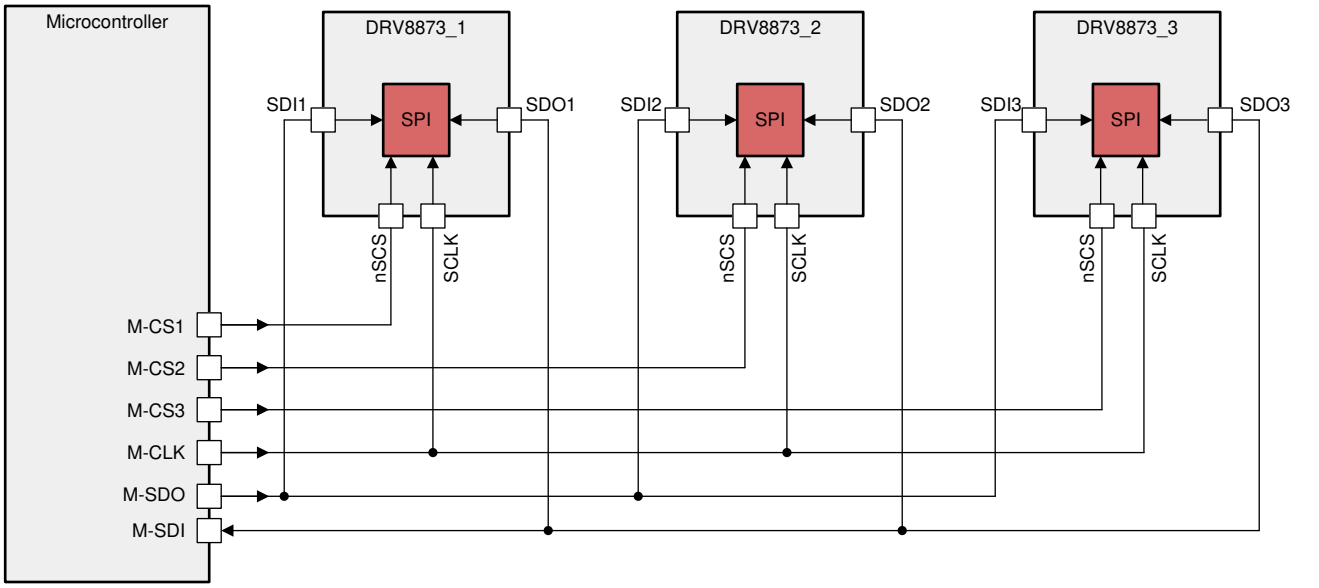
- The SCLK pin must be low when the nSCS pin goes low and when the nSCS pin goes high.
- The nSCS pin should be taken high for at least 500 ns between frames.
- When the nSCS pin is asserted high, any signals at the SCLK and SDI pins are ignored, and the SDO pin is in the high-impedance state (Hi-Z).
- Full 16 SCLK cycles must occur.
- Data is captured on the falling edge of the clock and data is driven on the rising edge of the clock.
- The most-significant bit (MSB) is shifted in and out first.
- If the data word sent to SDI pin is less than 16 bits or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

7.5.1.3 SPI for Multiple Slave Devices in Parallel Configuration

Multiple devices can be connected in parallel as shown in 図 7-16. In this configuration, all the slave devices can share the same SDI, SDO, and CLK lines from the micro-controller, but has dedicated chip-select pin (CSx) for each device from the micro-controller.

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The micro-controller activates the SPI of a given device via that device's chip-select input, the other devices remain inactive for SPI transactions. This configuration helps reduce micro-controller resources for SPI transactions if multiple slave devices are connected to the same micro-controller.



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図 7-16. Three DRV8873S-Q1 Devices Connected in Parallel Configuration

7.5.1.4 SPI for Multiple Slave Devices in Daisy Chain Configuration

The device can be connected in a daisy chain configuration to keep GPIO ports available when multiple devices are communicating to the same MCU. 図 7-17 shows the topology when three devices are connected in series.

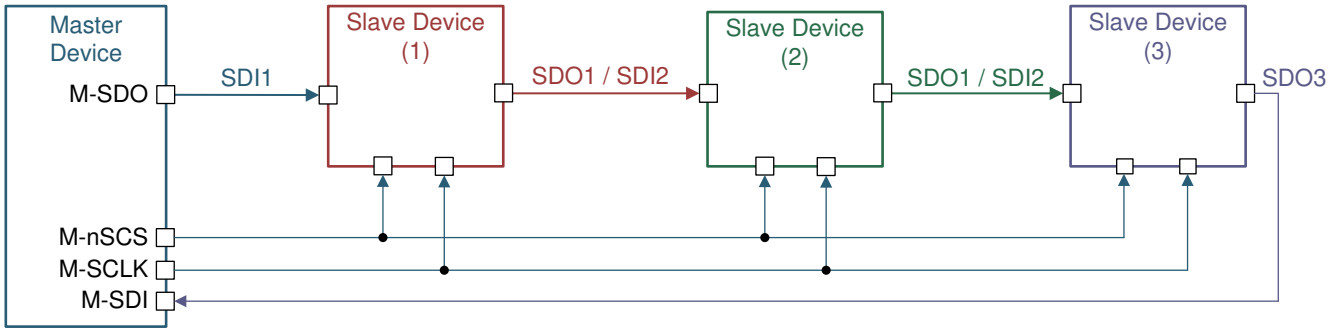


図 7-17. Three DRV8873S-Q1 Devices Connected in Daisy Chain

The first device in the chain receives data from the MCU in the following format for 3-device configuration: 2 bytes of header (HDRx) followed by 3 bytes of address (Ax) followed by 3 bytes of data (Dx).

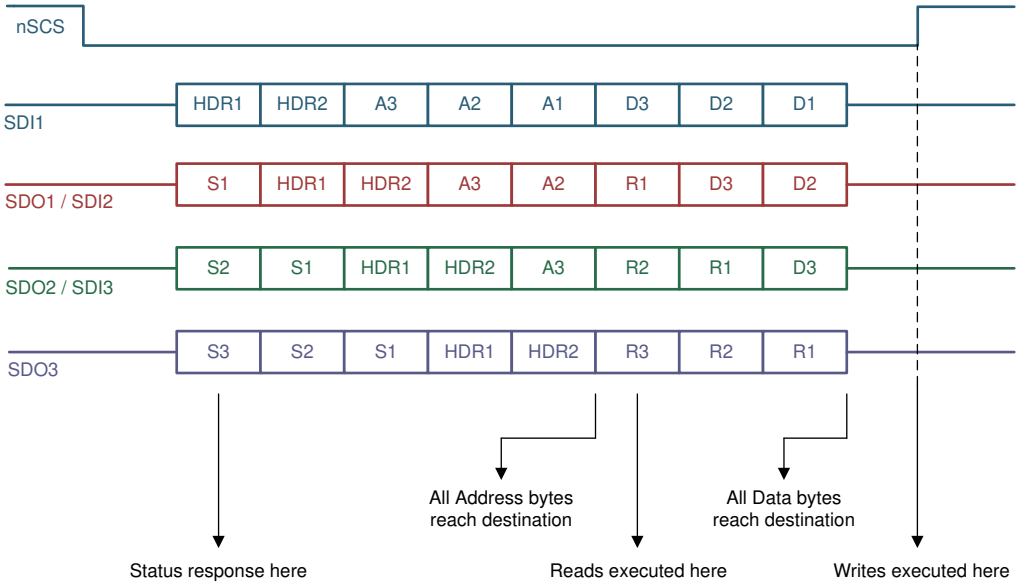


図 7-18. SPI Frame With Three DRV8873S-Q1 Devices

After the data has been transmitted through the chain, the MCU receives the data string in the following format for 3-device configuration: 3 bytes of status (Sx) followed by 2 bytes of header followed by 3 bytes of report (Rx).

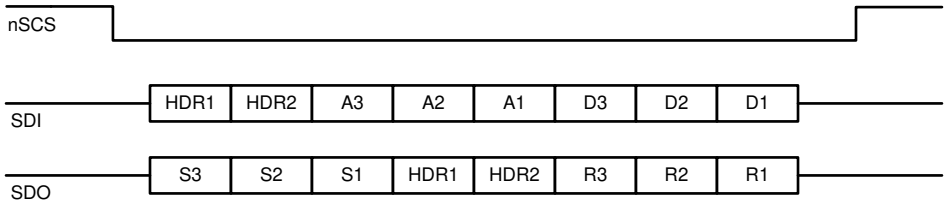


図 7-19. SPI Data Sequence for Three DRV8873S-Q1 Devices

The header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. Header values N5 through N0 are 6 bits dedicated to show the number of devices in the chain. Up to 63 devices can be connected in series for each daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

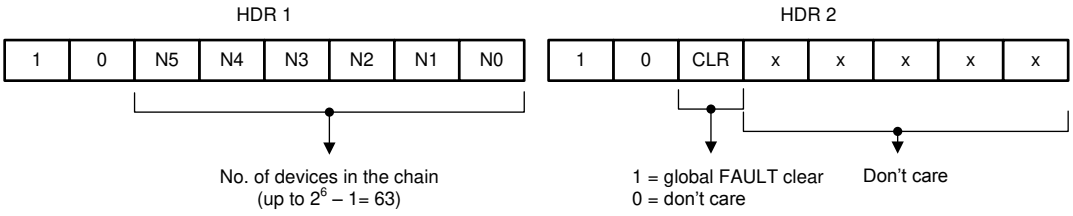


図 7-20. Header Bytes

The status byte provides information about the fault status register for each device in the daisy chain so that the MCU does not have to initiate a read command to read the fault status from any particular device. This keeps additional read commands for the MCU and makes the system more efficient to determine fault conditions flagged in a device. Status bytes must start with 1 and 1 for the two MSBs.

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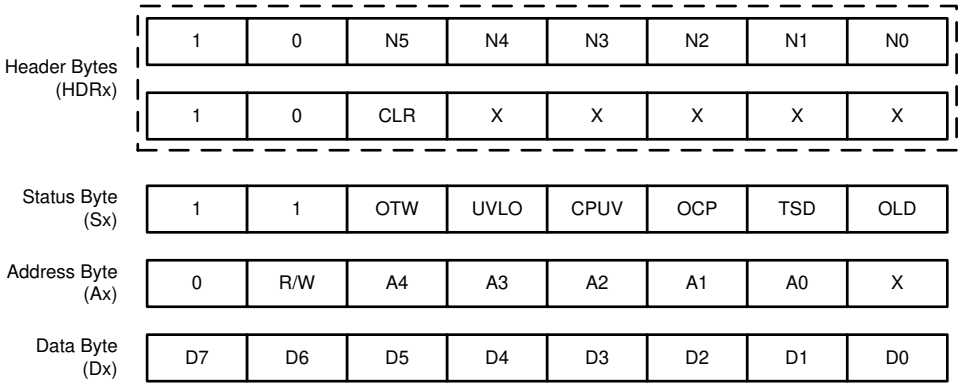


図 7-21. Contents of Header, Status, Address, and Data Bytes

When data passes through a device, it determines the position of itself in the chain by counting the number of status bytes it receives followed by the first header byte. For example, in this 3-device configuration, device 2 in the chain receives two status bytes before receiving the HDR1 byte which is then followed by the HDR2 byte.

From the two status bytes, the data can determine that its position is second in the chain. From the HDR2 byte, the data can determine how many devices are connected in the chain. In this way, the data only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a 1-device connection. The report bytes (R1 through R3), as shown in 図 7-19, are the content of the register being accessed.

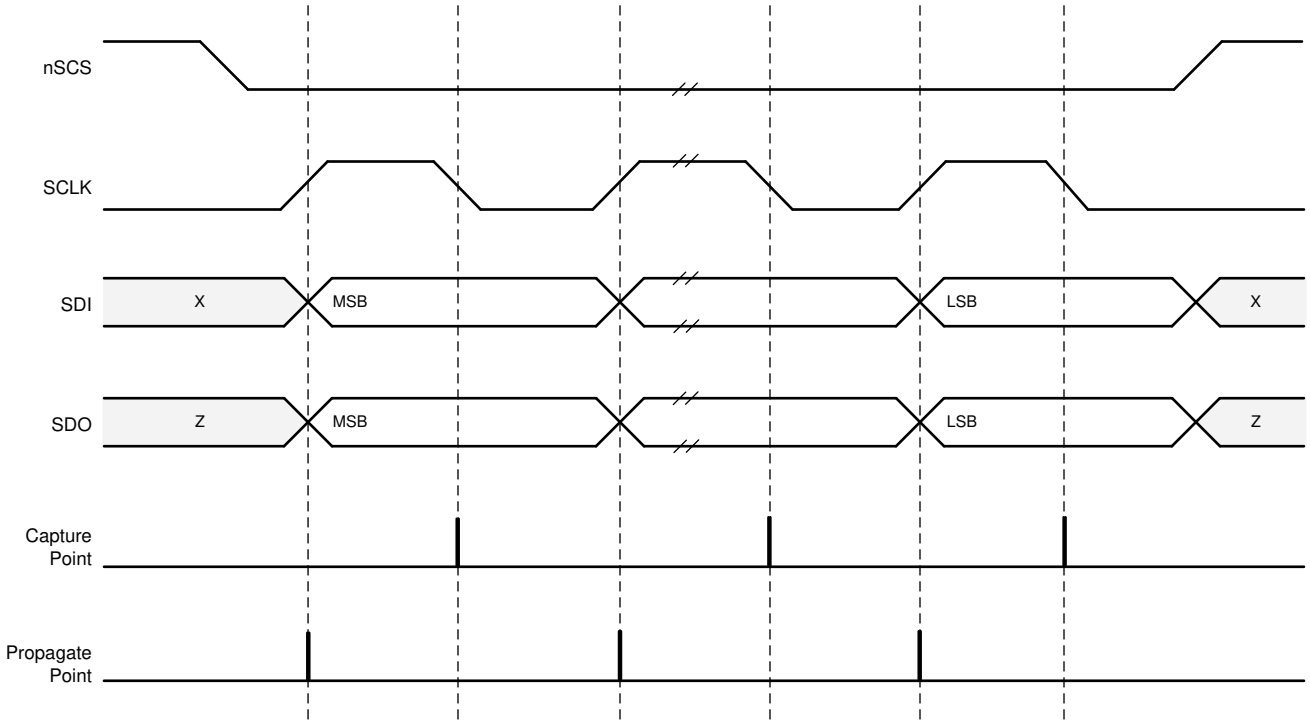


図 7-22. SPI Transaction

7.6 Register Maps

表 7-18 lists the memory-mapped registers for the device. All register addresses not listed in 表 7-18 should be considered as reserved locations and the register contents should not be modified.

表 7-18. Memory Map

Register Name	7	6	5	4	3	2	1	0	Access Type	Address
FAULT Status	RSVD	FAULT	OTW	UVLO	CPUV	OCP	TSD	OLD	R	0x00
DIAG Status	OL1	OL2	ITRIP1	ITRIP2	OCP_H1	OCP_L1	OCP_H2	OCP_L2	R	0x01
IC1 Control	TOFF		SPI_IN	SR			MODE		RW	0x02
IC2 Control	ITRIP_REP	TSD_MODE	OTW_REP	DIS_CPUV	OCP_TRETRY		OCP_MODE		RW	0x03
IC3 Control	CLR_FLT	LOCK			OUT1_DIS	OUT2_DIS	EN_IN1	PH_IN2	RW	0x04
IC4 Control	RSVD	EN_OLP	OLP_DLY	EN_OLA	ITRIP_LVL		DIS_ITRIP		RW	0x05

Complex bit access types are encoded to fit into small table cells. 表 7-19 shows the codes that are used for access types in this section.

表 7-19. Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.6.1 Status Registers

The status registers are used to reporting warning and fault conditions. Status registers are read-only registers

表 7-20 lists the memory-mapped registers for the status registers. All register offset addresses not listed in 表 7-20 should be considered as reserved locations and the register contents should not be modified.

表 7-20. Status Registers Summary Table

Address	Register Name	Section
0x00	FAULT status	Go
0x01	DIAG status	Go

7.6.2 FAULT Status Register Name (address = 0x00)

FAULT status is shown in 図 7-23 and described in 表 7-21.

Read-only

図 7-23. FAULT Status Register

7	6	5	4	3	2	1	0
RSVD	FAULT	OTW	UVLO	CPUV	OCP	TSD	OLD
R-0b		R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-21. FAULT Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R	0b	Reserved
6	FAULT	R	0b	Global FAULT status register. Compliments the nFAULT pin
5	OTW	R	0b	Indicates overtemperature warning
4	UVLO	R	0b	Indicates UVLO fault condition
3	CPUV	R	0b	Indicates charge-pump undervoltage fault condition
2	OCP	R	0b	Indicates an overcurrent condition
1	TSD	R	0b	Indicates an overtemperature shutdown
0	OLD	R	0b	Indicates an open-load detection

7.6.3 DIAG Status Register Name (address = 0x01)

DIAG status is shown in 図 7-24 and described in 表 7-22.

Read-only

図 7-24. DIAG Status Register

7	6	5	4	3	2	1	0
OL1	OL2	ITRIP1	ITRIP2	OCP_H1	OCP_L1	OCP_H2	OCP_L2
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-22. DIAG Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	OL1	R	0b	Indicates open-load detection on half bridge 1
6	OL2	R	0b	Indicates open-load detection on half bridge 2

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表 7-22. DIAG Status Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
5	ITRIP1	R	0b	Indicates the current regulation status of half bridge 1. 0b = Indicates output 1 is not in current regulation 1b = Indicates output 1 is in current regulation
4	ITRIP2	R	0b	Indicates the current regulation status of half bridge 2. 0b = Indicates output 2 is not in current regulation 1b = Indicates output 2 is in current regulation
3	OCP_H1	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 1
2	OCP_L1	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 1
1	OCP_H2	R	0b	Indicates overcurrent fault on the high-side FET of half bridge 2
0	OCP_L2	R	0b	Indicates overcurrent fault on the low-side FET of half bridge 2

7.6.4 Control Registers

The IC control registers are used to configure the device. Status registers are read and write capable.

表 7-23 lists the memory-mapped registers for the control registers. All register offset addresses not listed in 表 7-23 should be considered as reserved locations and the register contents should not be modified.

表 7-23. Control Registers Summary Table

Address	Register Name	Section
0x02	IC1 control	Go
0x03	IC2 control	Go
0x04	IC3 control	Go
0x05	IC4 control	Go

7.6.5 IC1 Control Register (address = 0x02)

IC1 control is shown in 図 7-25 and described in 表 7-24.

Read/Write

図 7-25. IC1 Control Register

7	6	5	4	3	2	1	0
TOFF		SPI_IN	SR			MODE	
R/W-01b		R/W-0b	R/W-100b			R/W-01b	

表 7-24. IC1 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	TOFF	R/W	01b	00b = 20 µs **01b = 40 µs** 10b = 60 µs 11b = 80 µs
5	SPI_IN	R/W	0b	**0b = Outputs follow input pins (INx)** 1b = Outputs follow SPI registers EN_IN1 and PH_IN2

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表 7-24. IC1 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
4-2	SR	R/W	100b	000b = 53.2-V/µs rise time 001b = 34-V/µs rise time 010b = 18.3-V/µs rise time 011b = 13-V/µs rise time **100b = 10.8-V/µs rise time** 101b = 7.9-V/µs rise time 110b = 5.3-V/µs rise time 111b = 2.6-V/µs rise time
1-0	MODE	R/W	01b	00b = PH/EN **01b = PWM** 10b = Independent half bridge 11b = Input disabled; bridge Hi-Z

7.6.6 IC2 Control Register (address = 0x03)

IC2 control is shown in 図 7-26 and described in 表 7-25.

Read/Write

図 7-26. IC2 Control Register

7	6	5	4	3	2	1	0
ITRIP_REP	TSD_MODE	OTW_REP	DIS_CPUV	OCP_TRETRY		OCP_MODE	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-11b		R/W-00b	

表 7-25. IC2 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	ITRIP_REP	R/W	0b	**0b = ITRIP is not reported on nFAULT or the FAULT bit** 1b = ITRIP is reported on nFAULT and the FAULT bit
6	TSD_MODE	R/W	0b	**0b = Overtemperature condition causes a latched fault** 1b = Overtemperature condition causes an automatic recovery fault
5	OTW_REP	R/W	0b	**0b = OTW is not reported on nFAULT or the FAULT bit** 1b = OTW is reported on nFAULT and the FAULT bit
4	DIS_CPUV	R/W	0b	**0b = Charge pump undervoltage fault is enabled** 1b = Charge pump undervoltage fault is disabled
3-2	OCP_TRETRY	R/W	11b	00b = Overcurrent retry time is 0.5 ms 01b = Overcurrent retry time is 1 ms 10b = Overcurrent retry time is 2 ms **11b = Overcurrent retry time is 4 ms**
1-0	OCP_MODE	R/W	00b	**00b = Overcurrent condition causes a latched fault** 01b = Overcurrent condition causes an automatic retrying fault 10b = Overcurrent condition is report only but no action is taken 11b = Overcurrent condition is not reported and no action is taken

7.6.7 IC3 Control Register (address = 0x04)

IC3 control is shown in 図 7-27 and described in 表 7-26.

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Read/Write

図 7-27. IC3 Control Register

7	6	5	4	3	2	1	0
CLR_FLT	LOCK			OUT1_DIS	OUT2_DIS	EN_IN1	PH_IN2
R/W-0b	R/W-100b			R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-26. IC3 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write a 1b to this bit to clear the fault bits. This bit is automatically reset after a write.
6-4	LOCK	R/W	100b	Write 011b to this register to lock all register settings in the IC1 control register except to these bits and address 0x04, bit 7 (CLR_FLT) Write 100b to this register to unlock all register settings in the IC1 control register
3	OUT1_DIS	R/W	0b	Enabled only in the Independent PWM mode **0b = Half bridge 1 enabled** 1b = Half bridge 1 disabled (Hi-Z)
2	OUT2_DIS	R/W	0b	Enabled only in the Independent PWM mode **0b = Half bridge 2 enabled** 1b = Half bridge 2 disabled (Hi-Z)
1	EN_IN1	R/W	0b	EN/IN1 bit to control the outputs through SPI (when SPI_IN = 1b)
0	PH_IN2	R/W	0b	PH/IN2 bit to control the outputs through SPI (when SPI_IN = 1b)

7.6.8 IC4 Control Register (address = 0x05)

IC4 control is shown in 図 7-28 and described in 表 7-27.

Read/Write

図 7-28. IC4 Control Register

7	6	5	4	3	2	1	0
RSVD	EN_OLP	OLP_DLY	EN_OLA	ITRIP_LVL		DIS_ITRIP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-10b		R/W-00b	

表 7-27. IC4 Control Register Field Descriptions

Bit	Field	Type	Default	Description
7	RSVD	R/W	0b	Reserved
6	EN_OLP	R/W	0b	Write 1b to run open load diagnostic in standby mode. When open load test is complete EN_OLP returns to 0b (status check)
5	OLP_DLY	R/W	0b	**0b = Open load diagnostic delay is 300 µs** 1b = Open load diagnostic delay is 1.2 ms
4	EN_OLA	R/W	0b	**0b = Open load diagnostic in active mode is disabled** 1b = Enable open load diagnostics in active mode

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表 7-27. IC4 Control Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
3-2	ITRIP_LVL	R/W	10b	00b = 4 A 01b = 5.4 A **10b = 6.5 A** 11b = 7 A
1-0	DIS_ITRIP	R/W	00b	**00b = Current regulation is enabled** 01b = Current regulation is disabled for OUT1 10b = Current regulation is disabled for OUT2 11b = Current regulation is disabled for both OUT1 and OUT2

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8 Application and Implementation

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8.1 Application Information

The device is used mainly to drive a brushed DC motor. The on-board current regulation allows for limiting the motor current during start-up and stall conditions. The design procedures in the *セクション 8.2* section highlight how to use and configure the SPI version of the device.

8.2 Typical Application

図 8-1 shows the typical application schematic for the SPI version of the device.

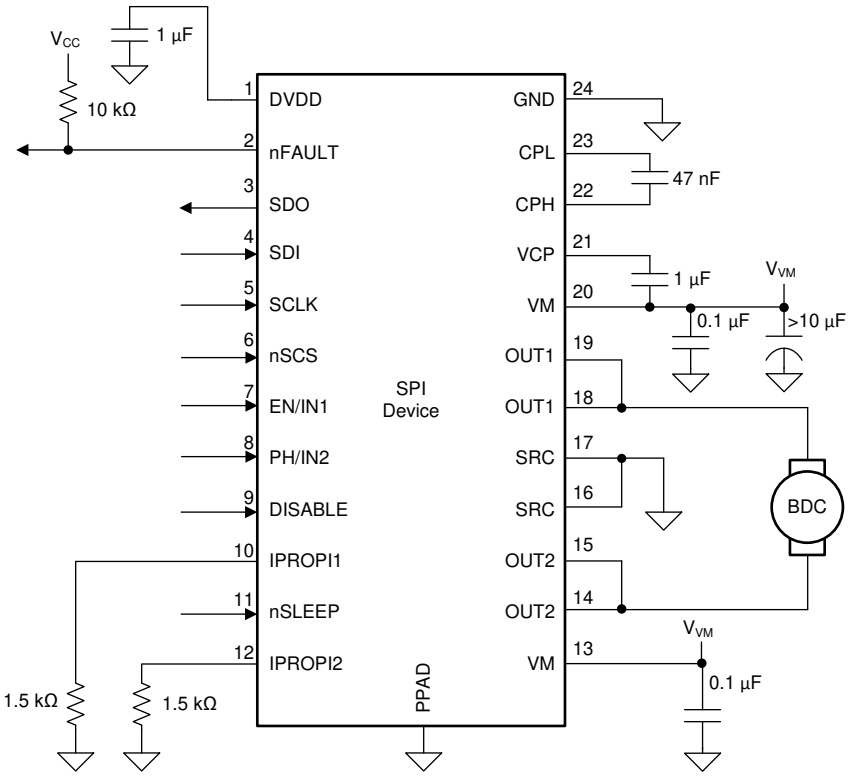


図 8-1. Typical Application Schematic

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8.2.1 Design Requirements

表 8-1 lists the example input parameters for the system design.

表 8-1. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	VM	13.5 V
Motor RMS current	I_{RMS}	2.5 A
Motor winding inductance	LM	2.9 mH
Motor current trip point	I_{TRIP}	6.5 A
PWM frequency	f_{PWM}	10 kHz
Sense resistor	R_{SENSE}	1.5 kΩ
Rise and fall times (slew rate)	t_{SR}	1 µs

8.2.1.1 Motor Voltage

The motor voltage used depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.1.2 Drive Current and Power Dissipation

The current path is through the high-side sourcing power driver, motor winding, and low-side sinking power driver. The amount of current the device can drive depends on the power dissipation without going into thermal shutdown. The amount of current that can be power dissipation losses in one source and sink power driver are calculated in 式 2.

$$P_D = (I_{RMS})^2 \times (R_{DS(on)High\text{-}side} + R_{DS(on)Low\text{-}side}) \quad (2)$$

The I_{OUT} current is equal to the average current drawn by the DC motor. At 25°C ambient temperature, the power dissipation becomes $(2.5\ A)^2 \times (150\ m\Omega) = 0.94\ W$.

The temperature that the device reaches depends on the thermal resistance to the air and PCB. Soldering the device PowerPAD to the PCB ground plane, with vias to the top and bottom board layers, is important to dissipate heat into the PCB and reduce the device temperature. In the example used here, the device had an effective thermal resistance $R_{\theta JA}$ of 27.8°C/W. The junction temperature T_J value becomes as shown in 式 3.

$$T_J = T_A + (P_D \times R_{\theta JA}) = 25°C + (0.94\ W \times 27.8°C/W) = 51°C \quad (3)$$

注

The values of $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This fact must be taken into consideration when sizing the heatsink.

At start-up and fault conditions, the current flowing through the motor is much higher than normal running current; these peak currents and their duration must also be considered. High PWM frequency also results in higher switching losses. Typically, switching the inputs at 100 kHz compared to 10 kHz causes 20% more power loss in heat.

Power dissipation in the device is dominated by the power dissipated of the internal MOSFET resistance. The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Total power dissipation for the device is composed of three main components. These are the quiescent supply current dissipation, the power MOSFET switching losses, and the power MOSFET $R_{DS(ON)}$ (conduction) losses. While other factors may contribute additional power losses, these other items are typically insignificant compared to the three main items.

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$$P_{TOT} = P_{VM} + P_{SW} + P_D \quad (4)$$

P_{VM} can be calculated from the nominal supply voltage (V_M) and the supply current (I_{VM}) in active mode.

$$P_{VM} = V_M \times I_{VM} = 13.5\ V \times 5\ mA = 67.5\ mW \quad (5)$$

P_{SW} can be calculated from the nominal supply voltage (V_M), average output current (I_{RMS}), switching frequency (f_{PWM}) and the device output rise and fall times (t_{SR}) time specifications.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} = 0.17\ W + 0.17\ W = 0.34\ W \quad (6)$$

$$P_{SW_RISE} = 0.5 \times V_M \times I_{RMS} \times t_{SR} \times f_{PWM} = 0.5 \times 13.5\ V \times 2.5\ A \times 1\ \mu s \times 10\ kHz = 0.17\ W \quad (7)$$

$$P_{SW_FALL} = 0.5 \times V_M \times I_{RMS} \times t_{SR} \times f_{PWM} = 0.5 \times 13.5\ V \times 2.5\ A \times 1\ \mu s \times 10\ kHz = 0.17\ W \quad (8)$$

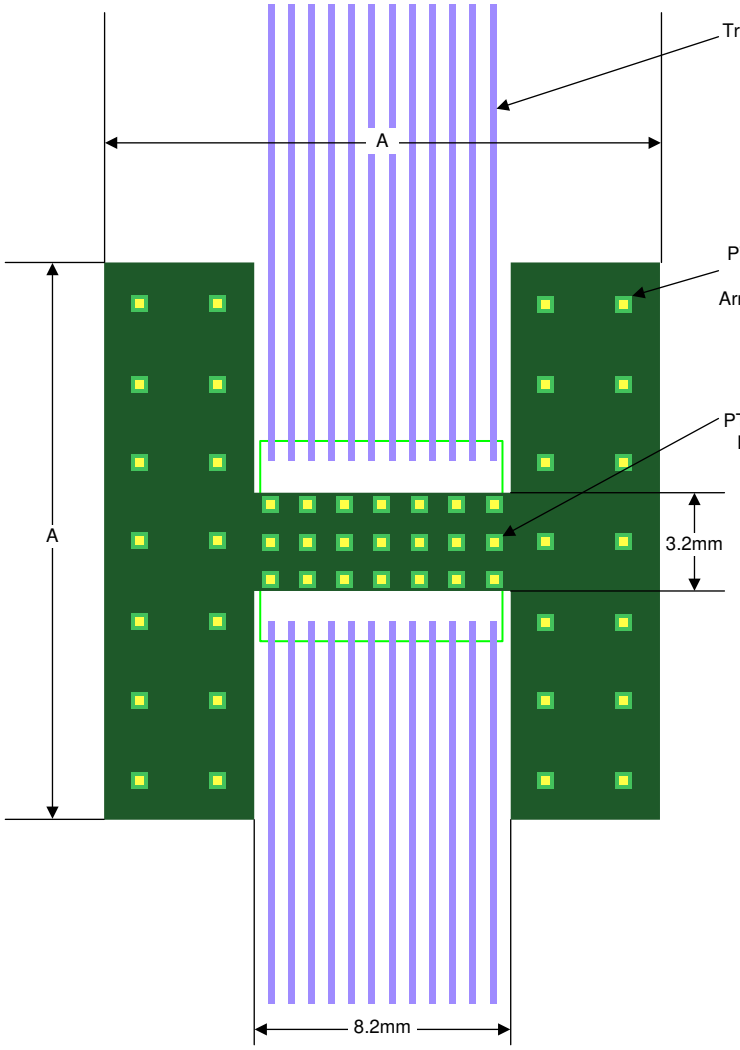
Therefore, total power dissipation (P_{TOT}) at 25°C ambient temperature becomes = $P_{VM} + P_{SW} + P_D$ = 67.5 mW + 0.34 W + 0.94 W = 1.35 W

P_{TOT} makes the junction temperature (T_J) of the device to be

$$T_J = T_A + (P_{TOT} \times R_{\theta JA}) = 25°C + (1.35\ W \times 27.8°C/W) = 63°C \quad (9)$$

The power dissipation from power MOSFET switching losses and quiescent supply current dissipation results is approximately 12°C rise in the junction temperature (different between 式 9 and 式 3). Care must be taken when doing the PCB layout and heatsinking the motor driver device so that the thermal characteristics are properly managed.

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Copper (Cu) Area (cm^2)	Dimension A (mm)
2	17.9
4	23.9
8	32.2
16	44.0
32	60.6
49.23	74.2

図 8-2. PCB Model (4-Layer PCB Shown, 2-Layer PCB Has No Vias)

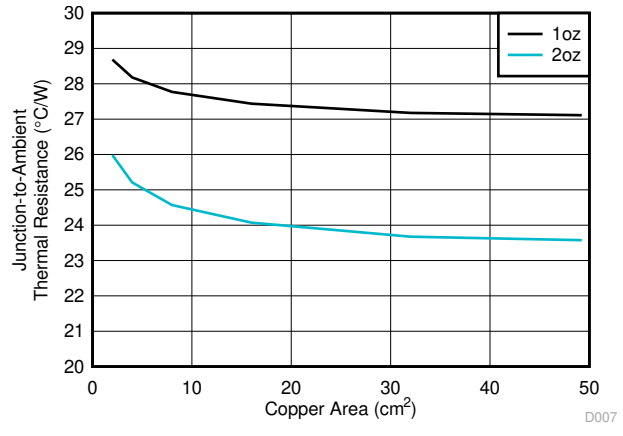


図 8-3. 4-Layer PCB Junction-to-Ambient Thermal Resistance vs Copper Area

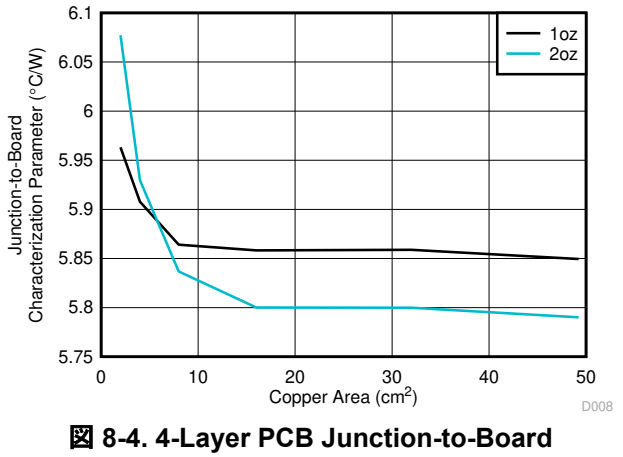


図 8-4. 4-Layer PCB Junction-to-Board Characterization Parameter vs Copper Area

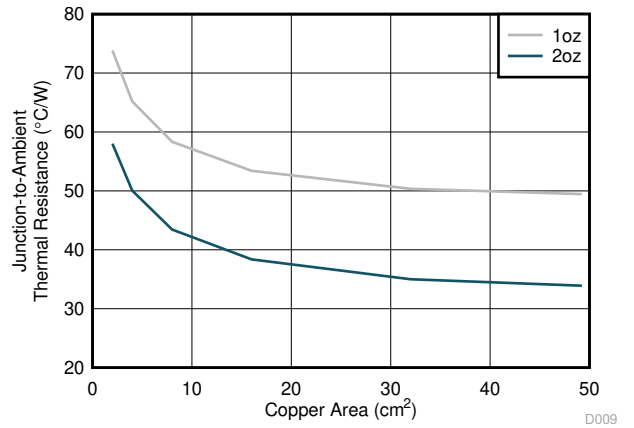


図 8-5. 2-Layer PCB (No Vias) Junction-to-Ambient Thermal Resistance vs Copper Area

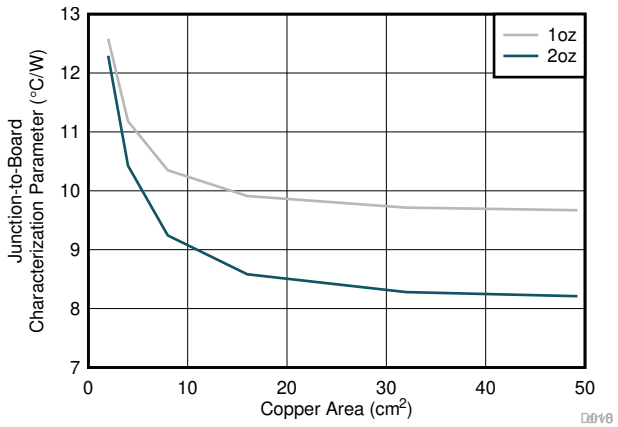


図 8-6. 2-Layer PCB (No Vias) Junction-to-Board Characterization Parameter vs Copper Area

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8.2.1.3 Sense Resistor

For optimal performance, the sense resistor must have the following features:

- Surface-mount device
- Low inductance
- Placed closely to the motor driver device

Use 式 10 to calculate the power dissipation (P_D) of the sense resistor.

$$P_D = (I_{(RMS)} / k)^2 \times R_{(SENSE)} \quad (10)$$

In this example, for the RMS motor current is 2.5 A, the sense resistor of 1.5 kΩ dissipates approximately 7.5 mW of power. The power quickly increases with higher current levels. Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components that generate heat, the system designer should add margin. Measuring the actual sense resistor temperature in a final system is best.

8.2.2 Detailed Design Procedure

8.2.2.1 Thermal Considerations

The device has thermal shutdown (TSD) at 165°C (mininum). If the die temperature exceeds this TSD threshold, the device will be disabled until the temperature drops below the temperature hysteresis level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high of an ambient temperature.

8.2.2.2 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this connection can be accomplished by adding a number of vias to connect the thermal pad to the ground plane.

On PCBs without internal planes, a copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to the *PowerPAD™ Thermally Enhanced Package* application report, and the *PowerPAD™ Made Easy* application report, available at www.ti.com. In general, the more copper area that can be provided, the more power can be dissipated.

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8.2.3 Application Curves

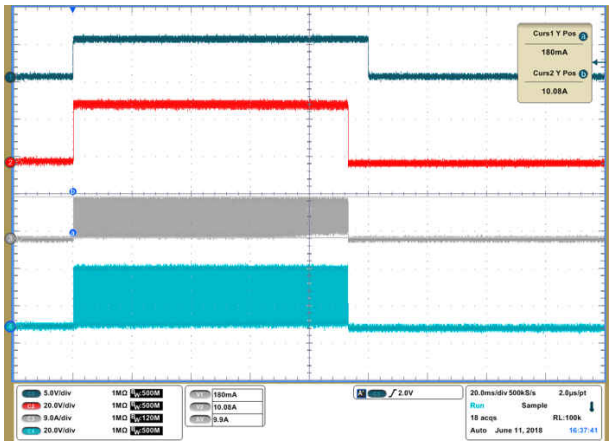


図 8-7. Overcurrent (OCP) Detection

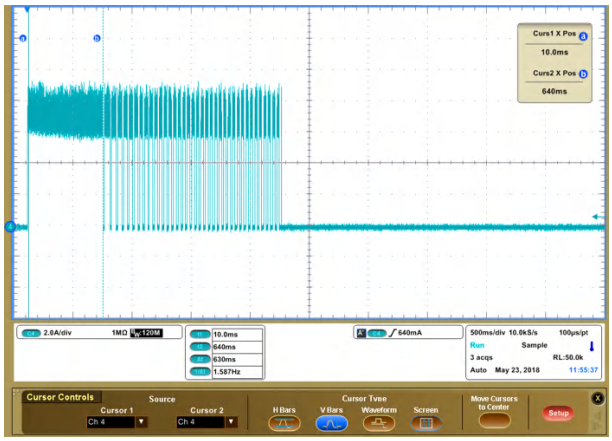


図 8-8. Current Regulation (ITRIP)



図 8-9. ITRIP Across TOFF and Load Current

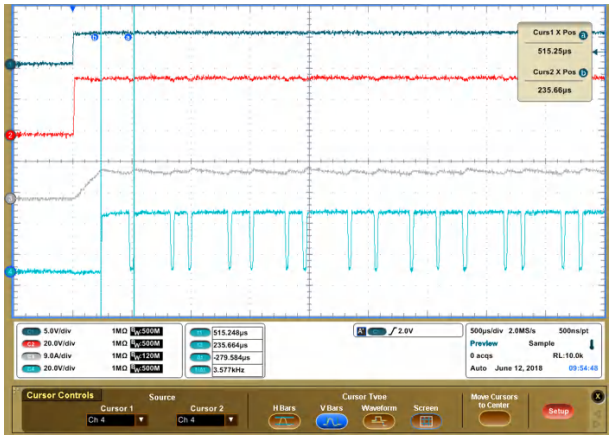


図 8-10. Motor Motion at Different Speeds

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9 Power Supply Recommendations

The device is designed to operate with an input voltage supply (VM) range from 4.5 V to 40 V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. Also, an appropriately sized bulk capacitor must be placed on the VM pin.

9.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It is beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors including:

- The highest current required by the motor system.
- The capacitance of the power supply and the ability of the power supply to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (brushed DC, brushless DC, and stepper).
- The motor braking method.

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When sufficient bulk capacitance is used, the motor voltage remains stable, and high current can be quickly supplied.

The data sheet provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

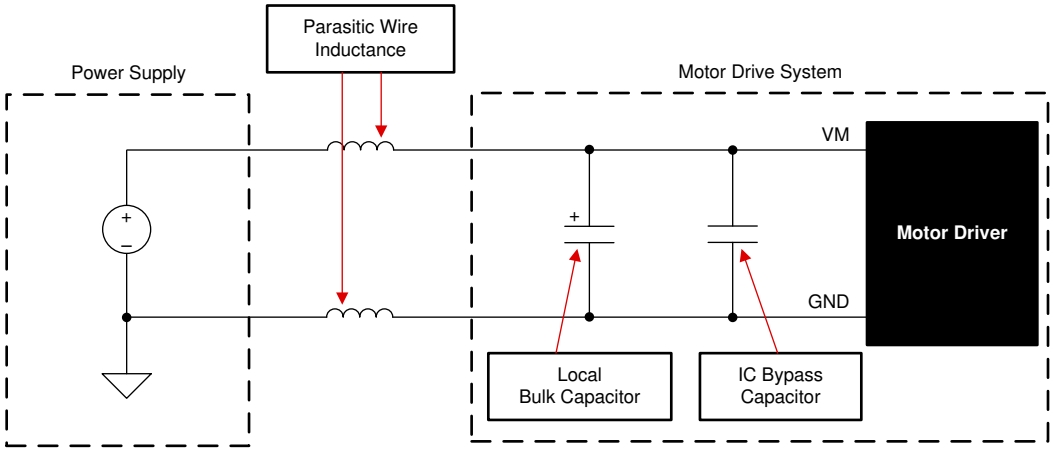


図 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage to provide a margin for cases when the motor transfers energy to the supply.

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10 Layout

10.1 Layout Guidelines

Each VM pin must be bypassed to ground using low-ESR ceramic bypass capacitors with recommended values of 0.1 µF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

Additional bulk capacitance is required to bypass the high current path. This bulk capacitance should be placed such that it minimizes the length of any high current paths. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 47 nF, rated for VM, and be of type X5R or X7R. Additionally, place a low-ESR ceramic capacitor between the VCP and VM pins. This capacitor should be 1 µF, rated for 16 V, and be of type X5R or X7R.

The current sense resistors should be placed as close as possible to the device pins to minimize trace inductance between the device pin and resistors.

10.2 Layout Example

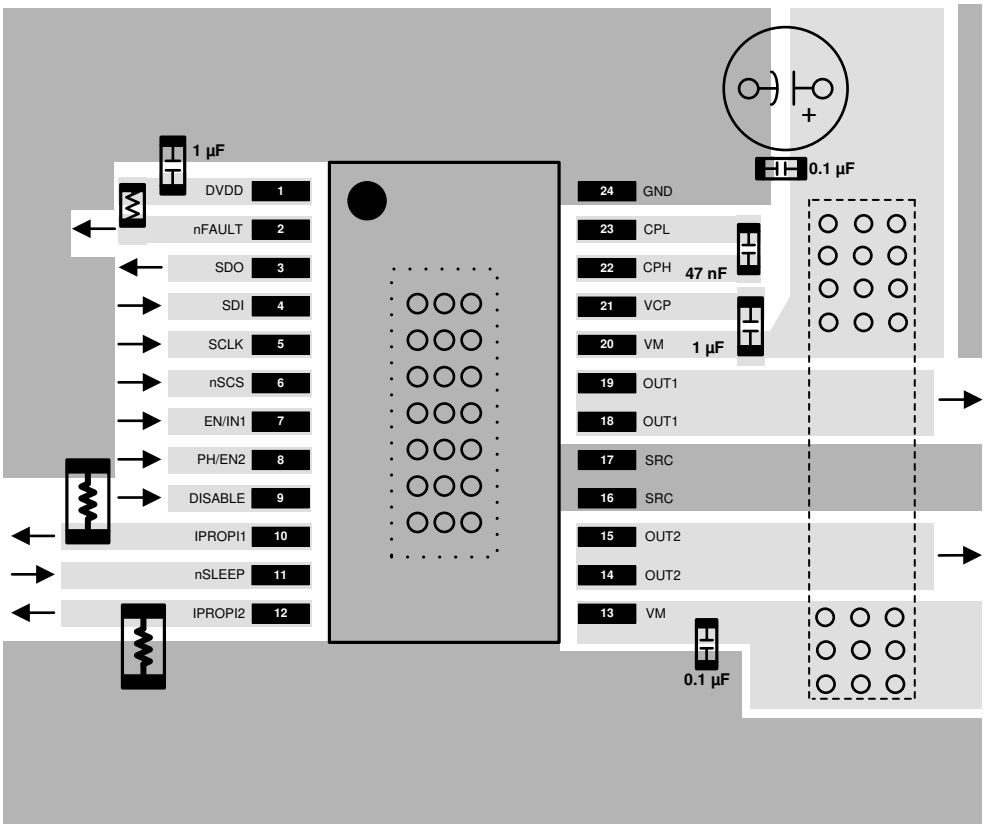


図 10-1. Layout Example

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

-
- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *Daisy Chain Implementation for Serial Peripheral Interface* application report
- Texas Instruments, *DRV8873x-Q1EVM User's Guide*
- Texas Instruments, *DRV8873x-Q1EVM GUI User's Guide*
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8873HPWPRQ1	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8873HQ
DRV8873HPWPRQ1.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8873HQ
DRV8873SPWPRQ1	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8873SQ
DRV8873SPWPRQ1.A	Active	Production	HTSSOP (PWP) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	8873SQ
PDRV8873SPWPRQ1	Obsolete	Preproduction	HTSSOP (PWP) | 24	-	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF DRV8873-Q1 :

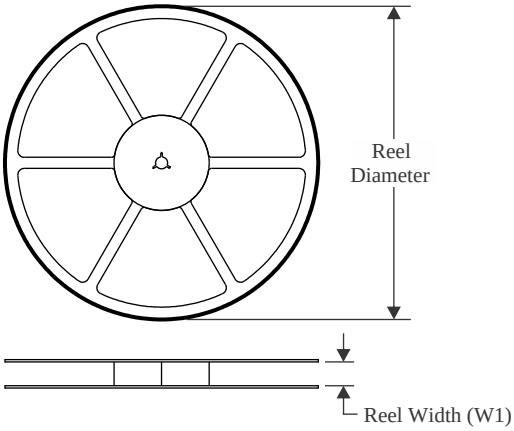
- Catalog : DRV8873

NOTE: Qualified Version Definitions:

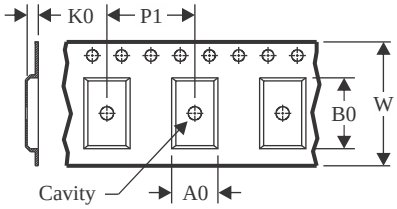
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

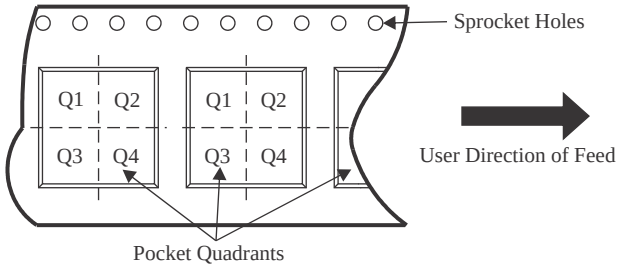


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

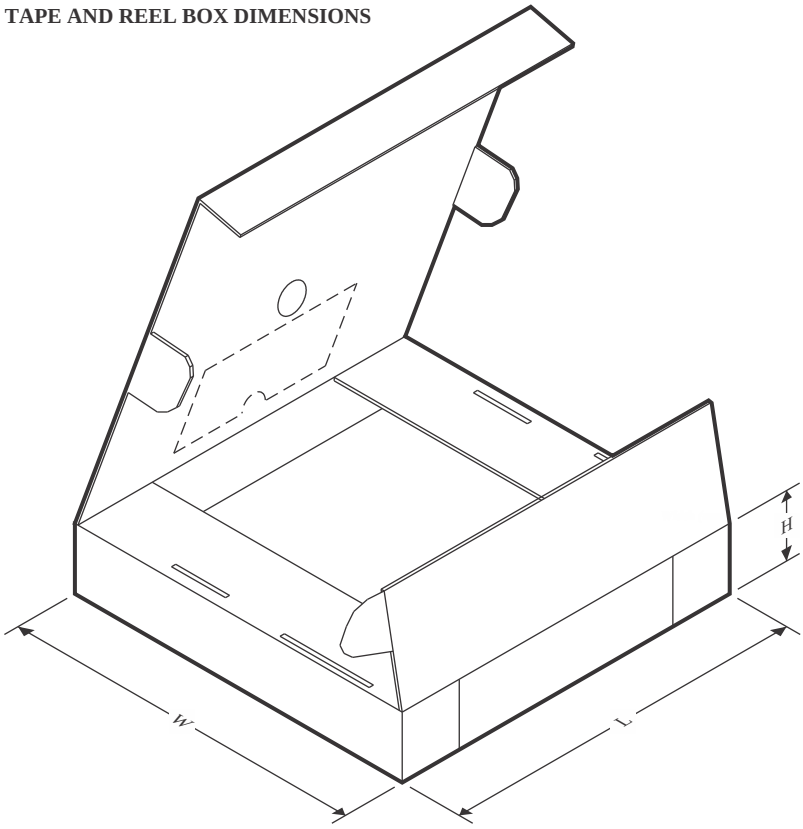
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8873HPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8873SPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8873HPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0
DRV8873SPWPRQ1	HTSSOP	PWP	24	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

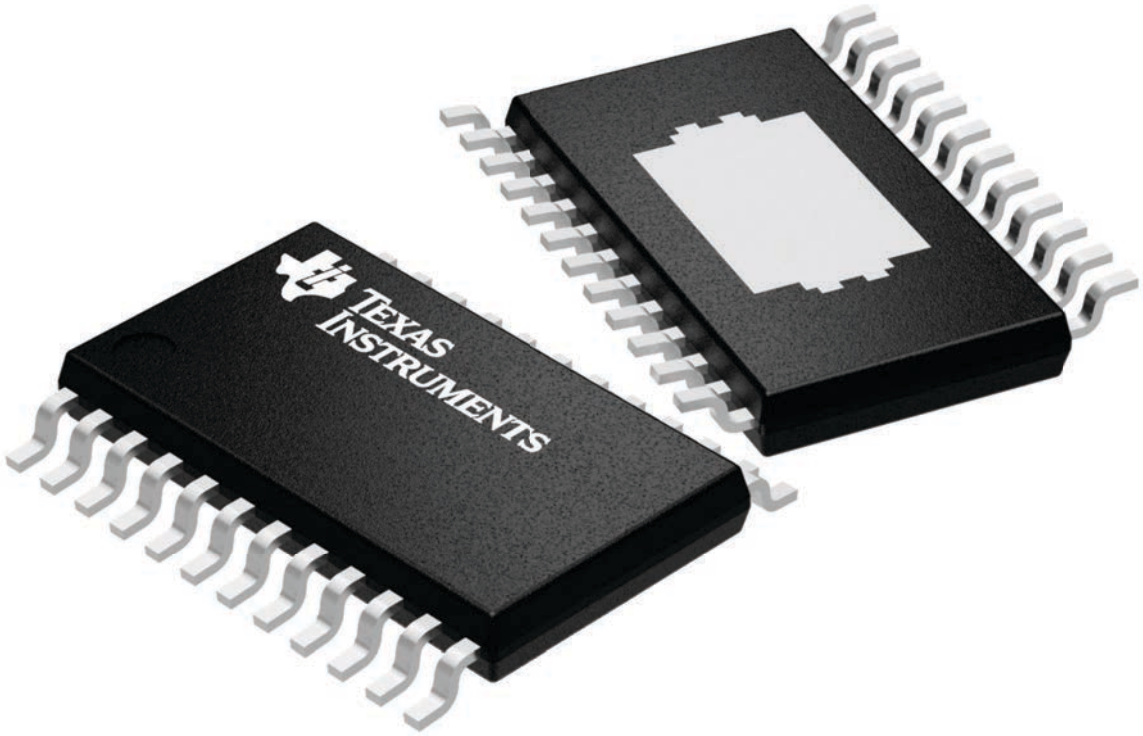
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

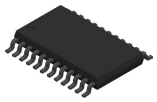
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

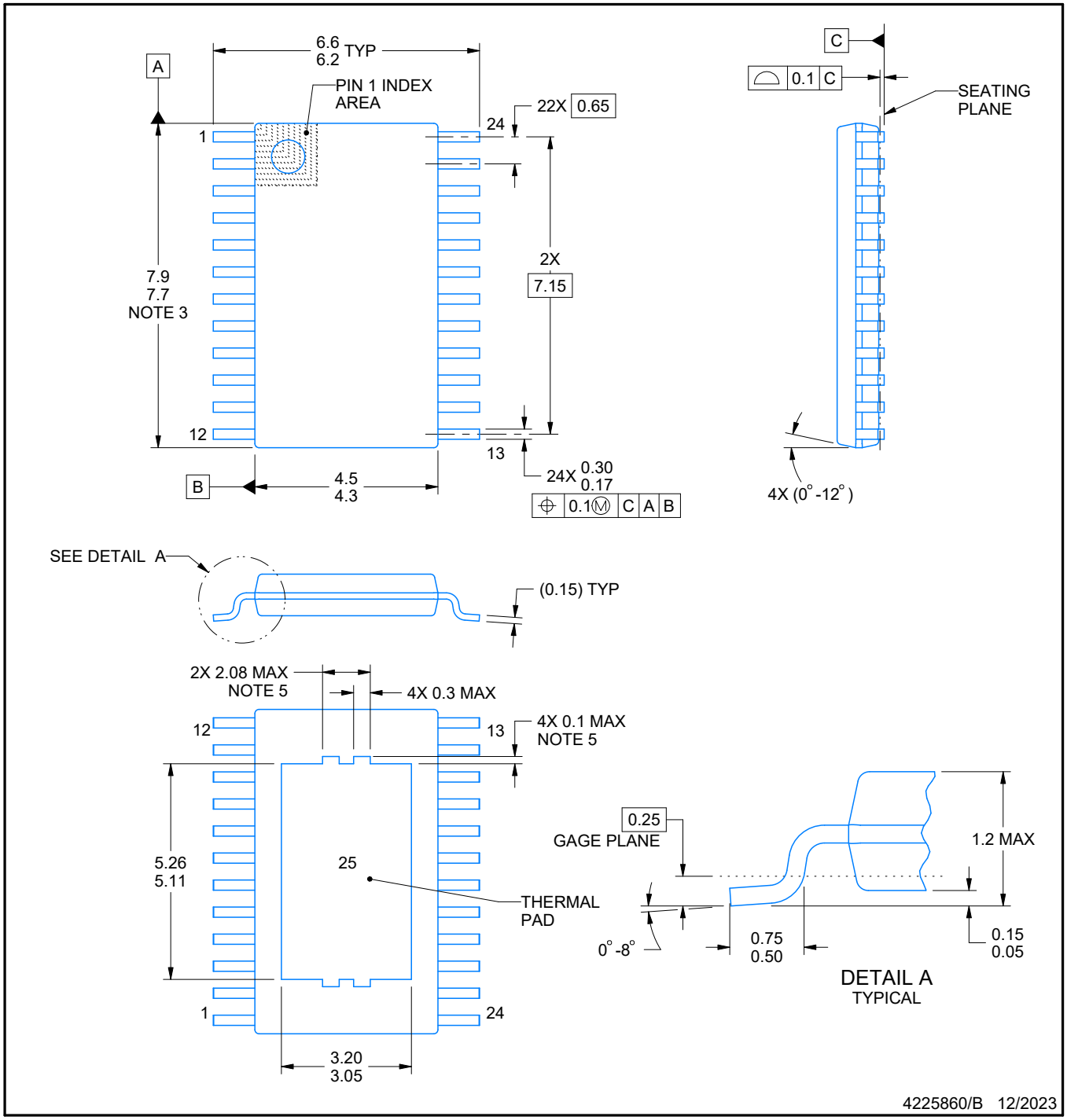
PACKAGE OUTLINE

PWP0024J



PowerPAD™ TSSOP - 1.2 mm max height

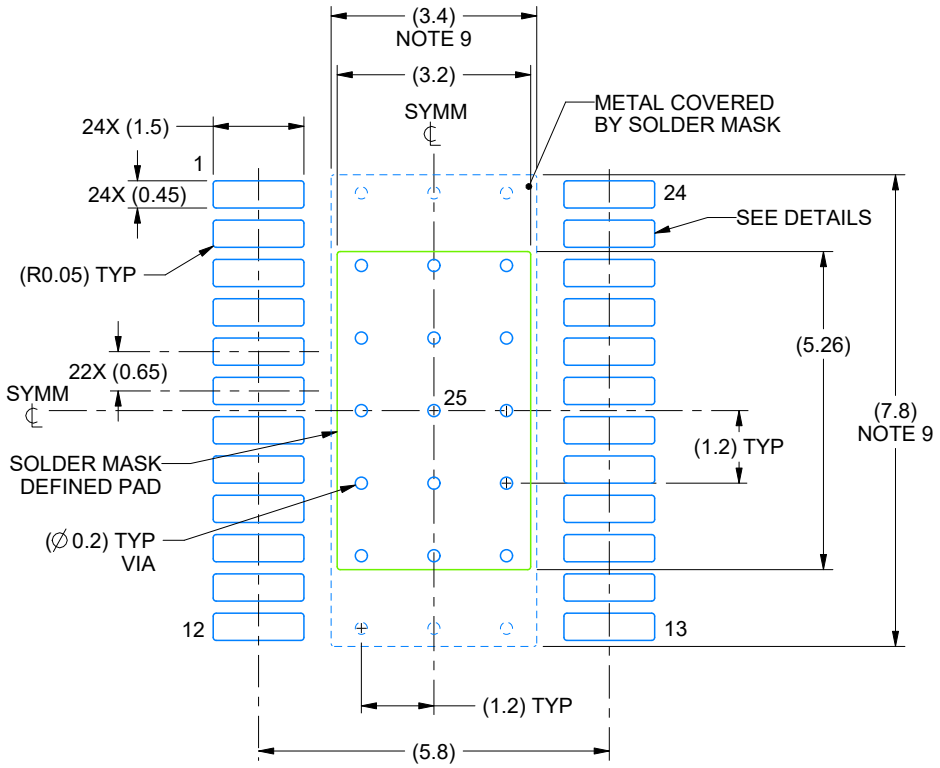
SMALL OUTLINE PACKAGE



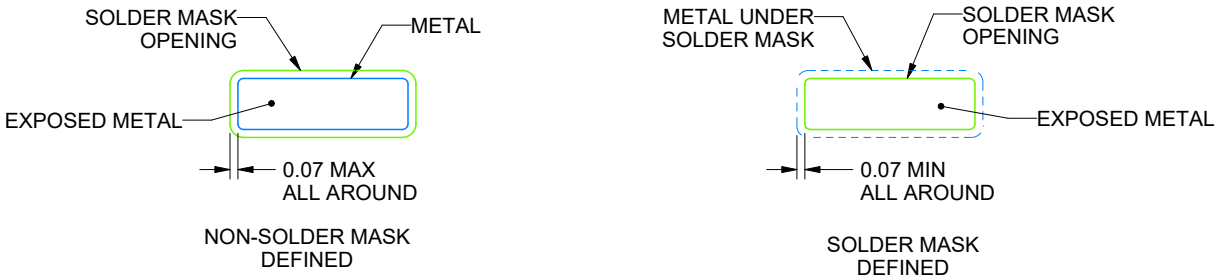
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

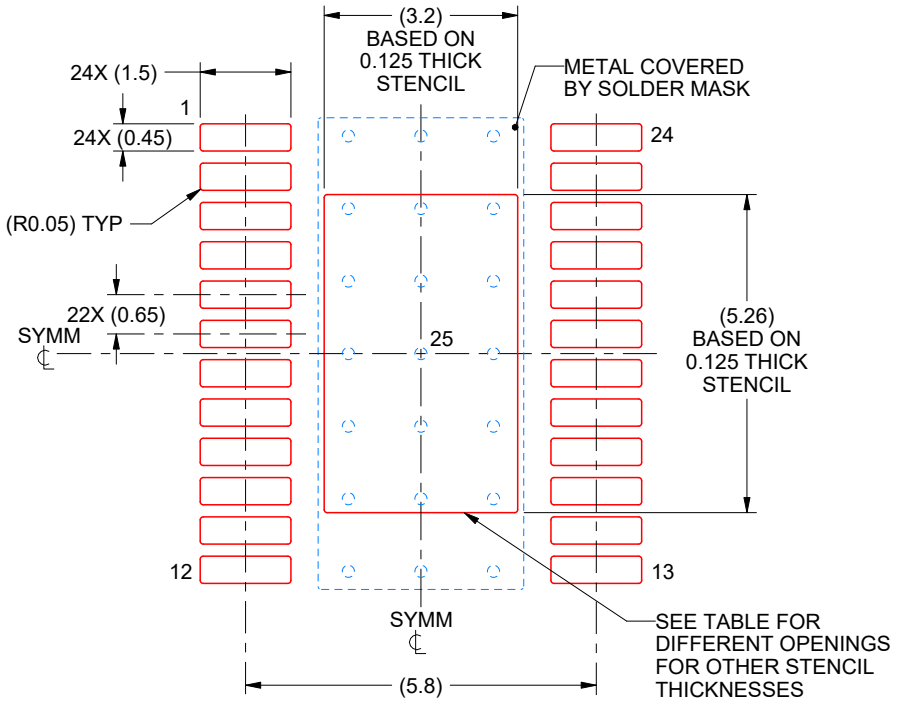


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.58 X 5.88
0.125	3.20 X 5.26 (SHOWN)
0.15	2.92 X 4.80
0.175	2.70 X 4.45

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月