TEXAS INSTRUMENTS
DS90C124, DS90C241
JAJSAG9M – NOVEMBER 2005 – REVISED JANUARY 2017

DS90C241およびDS90C124 5MHz～35MHz DC平衡化24ビット FPD-Link IIシリアライザ/デシリアライザ

1 特長

- 5MHz～35MHzクロック組み込みおよびDC平衡化の24:1および1:24データ転送
- LVDS出力上の外付け抵抗によるユーザー定義のプリエンファシス駆動能力、最大10mのシールド・ツイストペア・ケーブルを駆動可能
- トランスミッタとレシーバの両方で、並列データのクロック・エッジをユーザーが選択可能
- 内部DC平衡化のエンコードおよびデコード(外部コーディングなしでACカップリング・インターフェイスをサポート)
- トランスミッタとレシーバの両方を個別にパワー・ダウン制御
- レシーバにクロックCDR (クロックおよびデータ回復)を内蔵し、外部基準クロック・ソース不要
- すべてのコードRDL (ランダム・データ・ロック)でライブ・プラグ可能アプリケーションをサポート
- LOCK出力フラグにより、レシーバ側でデータ整合性を保証
- レシーバ側のRCLKとRDATAとの間でT_{SETUP}およびT_{HOLD}を平衡化
- PTO (段階的電源オン) LVCMOS出力によりEMIを低減しSSO効果を最小化
- すべてのLVCMOS入力および制御ピンは内部プルダウン付き
- トランスミッタとレシーバのPLL用にオンチップのフィルタを搭載
- 温度範囲: -40℃～+105℃
- 8kVを超えるHBM ESD耐圧
- AEC-Q100準拠
- 電源電圧範囲: 3.3V±10%
- 48ピンTQFPパッケージ

2 アプリケーション

- 車載用集中情報ディスプレイ
- 車載用計器盤表示
- 車載用ヘッドアップ・ディスプレイ
- リモート・カメラ・ベースの運転支援システム

3 概要

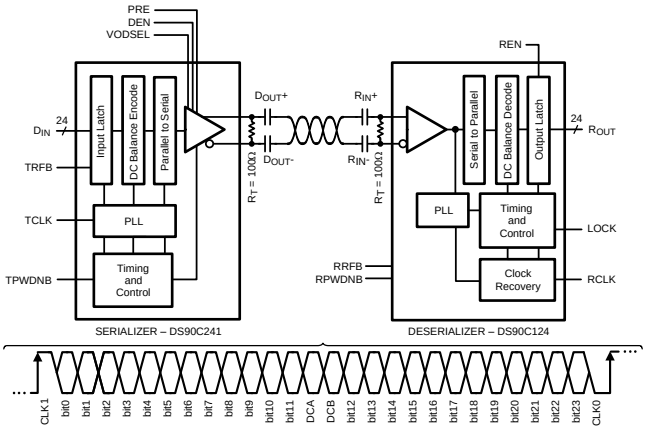
DS90C241およびDS90C124チップセットは、24ビットのパラレル・バスを、完全に透過的な、クロック情報が埋め込まれたデータおよび制御LVDSシリアル・ストリームに変換します。この単一のシリアル・ストリームにより、パラレル・データとクロック・パスの間でスキューの問題が排除されるため、PCB上の配線およびケーブルで24ビットのデータ・バスを簡単に転送できます。これによって、データ・パスを狭くでき、PCBレイヤ、ケーブル幅、コネクタのサイズとピン数のすべてを削減できるため、システム・コストを低減できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DS90C124 DS90C241	TQFP (48)	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision L (April 2013) から **Revision M** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- Deleted Lead temperature, soldering (260°C maximum) from *Absolute Maximum Ratings* ... 8
- Added *Thermal Information* table ... 9
- Added *Typical Characteristics* (PCLK = 5 MHz and PCLK = 25 MHz plus pre-emphasis) ... 12

Revision K (April 2013) から **Revision L** に変更 **Page**

- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

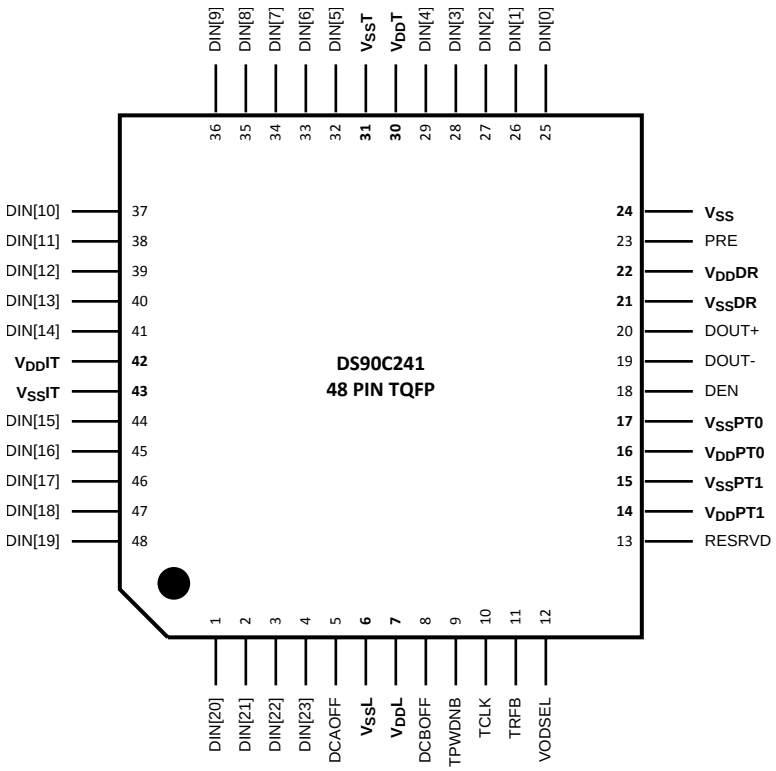
5 概要（続き）

DS90C241およびDS90C124には、高速I/OのLVSD信号通知が組み込まれています。LVDSによって、低消費電力かつ低ノイズの環境により、シリアル転送パス上で確実にデータを転送できます。動作周波数範囲について、シリアライザの出力エッジ・レートを最適化することにより、さらにEMIが低減されます。

さらに、このデバイスにはプリエンファシス機能があり、損失の多いケーブル上で長距離の伝送を行えるよう信号をブーストできます。内部DC平衡化されたエンコードとデコードは、ACカップリングされた相互接続をサポートします。

6 Pin Configuration and Functions

DS90C241 Serializer PFB Package
48-Pin TQFP
Top View



Pin Functions – DS90C241 Serializer

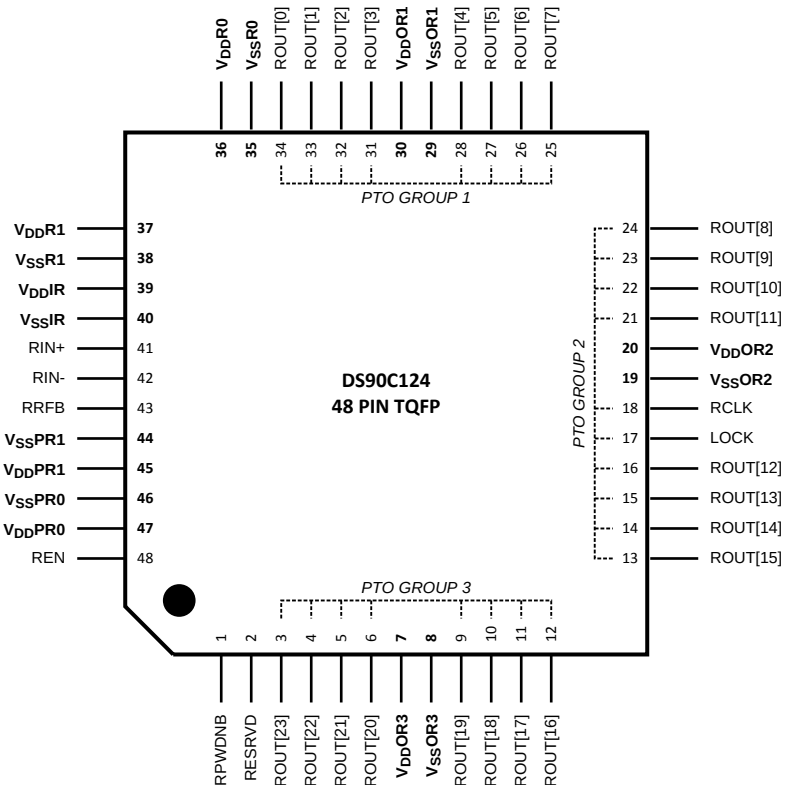
PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE PINS			
DIN[23:0]	4-1, 48-44, 41-32, 29-25	I	LVCMOS, Transmitter parallel interface data input pins. Tie LOW if unused, do not float.
TCLK	10	I	LVCMOS, Transmitter parallel interface clock input pin. Strobe edge set by TRFB configuration pin.
CONTROL AND CONFIGURATION PINS			
DCAOFF	5	I	LVCMOS, Reserved. This pin *must* be tied LOW.
DCBOFF	8	I	LVCMOS, Reserved. This pin *must* be tied LOW.
DEN	18	I	LVCMOS, Transmitter data enable. DEN = H; LVDS driver outputs are enabled (ON). DEN = L; LVDS driver outputs are disabled (OFF), Transmitter LVDS driver D_{OUT} (±) outputs are in TRI-STATE, PLL still operational and locked to TCLK.
PRE	23	I	LVCMOS, Pre-emphasis level select. PRE = NC (No Connect); Pre-emphasis is disabled (OFF). Pre-emphasis is active when input is tied to VSS through external resistor R_{PRE}. Resistor value determines pre-emphasis level. Recommended value $R_{PRE} \geq 3$ kΩ; $I_{max} = [(1.2/R) \times 20]$, $R_{min} = 3$ kΩ
RESRVD	13	I	LVCMOS, Reserved. This pin *must* be tied LOW.
TPWDNB	9	I	LVCMOS, Transmitter power down bar. TPWDNB = H; Transmitter is enabled and ON TPWDNB = L; Transmitter is in power down mode (Sleep), LVDS driver D_{OUT} (±) outputs are in TRI-STATE stand-by mode, PLL is shutdown to minimize power consumption.

(1) G = Ground, I = Input, O = Output, P = Power

Pin Functions – DS90C241 Serializer (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
TRFB	11	I	LVCMOS, Transmitter clock edge select pin. TRFB = H; Parallel interface data is strobed on the rising clock edge. TRFB = L; Parallel interface data is strobed on the falling clock edge.
VODSEL	12	I	LVCMOS, VOD Level select VODSEL = L; LVDS driver output is approximately ± 400 mV (R_L = 100 Ω) VODSEL = H; LVDS driver output is approximately ± 750 mV (R_L = 100 Ω) For normal applications, set this pin LOW. For long cable applications where a larger VOD is required, set this pin HIGH.
LVDS SERIAL INTERFACE PINS			
DOUT−	19	O	LVDS, Transmitter LVDS inverted (-) output This output is intended to be loaded with a 100-Ω load to the D_{OUT-} pin. The interconnect must be AC-coupled to this pin with a 100-nF capacitor.
DOUT+	20	O	LVDS, Transmitter LVDS true (+) output. This output is intended to be loaded with a 100-Ω load to the D_{OUT+} pin. The interconnect must be AC-coupled to this pin with a 100-nF capacitor.
POWER OR GROUND PINS			
VDDDR	22	P	VDD, Analog voltage supply, LVDS output power
VDDIT	42	P	VDD, Digital voltage supply, Tx input power
VDDL	7	P	VDD, Digital voltage supply, Tx logic power
VDDPT0	16	P	VDD, Analog voltage supply, VCO power
VDDPT1	14	P	VDD, Analog voltage supply, PLL power
VDDT	30	P	VDD, Digital voltage supply, Tx serializer power
VSS	24	G	ESD ground
VSSDR	21	G	Analog ground, LVDS output ground
VSSIT	43	G	Digital ground, Tx input ground
VSSL	6	G	Digital ground, Tx logic ground
VSSPT0	17	G	Analog ground, VCO ground
VSSPT1	15	G	Analog ground, PLL ground
VSST	31	G	Digital ground, Tx serializer ground

DS90C124 Deserializer PFB Package
48-Pin TQFP
Top View



Pin Functions – DS90C124 Deserializer

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LVCMOS PARALLEL INTERFACE PINS			
RCLK	18	O	LVCMOS, Parallel interface clock output pin. Strobe edge set by RRFB configuration pin.
ROUT[7:0]	25-28, 31-34	O	LVCMOS, Receiver LVCMOS level outputs – Group 1
ROUT[15:8]	13-16, 21-24	O	LVCMOS, Receiver LVCMOS level outputs – Group 2
ROUT[23:16]	3-6, 9-12	O	LVCMOS, Receiver LVCMOS level outputs – Group 3
CONTROL AND CONFIGURATION PINS			
REN	48	I	LVCMOS, Receiver data enable REN = H; R_{OUT}[23:0] and RCLK are enabled (ON). REN = L; R_{OUT}[23:0] and RCLK are disabled (OFF), receiver R_{OUT}[23:0] and RCLK outputs are in TRI-STATE, PLL still operational and locked to TCLK.
LOCK	17	O	LVCMOS, LOCK indicates the status of the receiver PLL LOCK = H; receiver PLL is locked LOCK = L; receiver PLL is unlocked, R_{OUT}[23:0] and RCLK are TRI-STATED
RESRVD	2	I	LVCMOS, Reserved. This pin *must* be tied LOW.
RPWDNB	1	I	LVCMOS, Receiver power down bar. RPWDNB = H; Receiver is enabled and ON RPWDNB = L; Receiver is in power down mode (Sleep), R_{OUT}[23:0], RCLK, and LOCK are in TRI-STATE standby mode, PLL is shutdown to minimize power consumption.
RRFB	43	I	LVCMOS, Receiver clock edge select pin. RRFB = H; R_{OUT} LVCMOS outputs strobed on the rising clock edge. RRFB = L; R_{OUT} LVCMOS outputs strobed on the falling clock edge.

(1) G = Ground, I = Input, O = Output, P = Power

Pin Functions – DS90C124 Deserializer (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
LVDS SERIAL INTERFACE PINS			
RIN−	42	I	Receiver LVDS Inverted (−) Input This input is intended to be terminated with a 100-Ω load to the R_{IN-} pin. The interconnect must be AC-coupled to this pin with a 100-nF capacitor.
RIN+	41	I	Receiver LVDS True (+) input This input is intended to be terminated with a 100-Ω load to the R_{IN+} pin. The interconnect must be AC-coupled to this pin with a 100-nF capacitor.
POWER OR GROUND PINS			
VDDIR	39	P	VDD, Analog LVDS voltage supply, power
VDDOR1	30	P	VDD, Digital voltage supply, LVCMOS output power
VDDOR2	20	P	VDD, Digital voltage supply, LVCMOS output power
VDDOR3	7	P	VDD, Digital voltage supply, LVCMOS output power
VDDPR0	47	P	VDD, Analog voltage supply, PLL power
VDDPR1	45	P	VDD, Analog voltage supply, PLL VCO power
VDDR0	36	P	VDD, Digital voltage supply, Logic power
VDDR1	37	P	VDD, Digital voltage supply, Logic power
VSSIR	40	G	Analog LVDS ground
VSSOR1	29	G	Digital ground, LVCMOS output ground
VSSOR2	19	G	Digital ground, LVCMOS output ground
VSSOR3	8	G	Digital ground, LVCMOS output ground
VSSPR0	46	G	Analog ground, PLL ground
VSSPR1	44	G	Analog ground, PLL VCO ground
VSSR0	35	G	Digital ground, Logic ground
VSSR1	38	G	Digital ground, Logic ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	4	V
	LVCMOS/LVTTL input voltage	–0.3	V_{CC} + 0.3	V
	LVCMOS/LVTTL output voltage	–0.3	V_{CC} + 0.3	V
	LVDS receiver input voltage	–0.3	3.9	V
	LVDS driver output voltage	–0.3	3.9	V
	LVDS output short circuit duration		10	ms
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±8000	V
		Charged-device model (CDM), per AEC Q100-011		±1250	
		R_D = 330 Ω, C_S = 150 pF	IEC, powered-up only contact discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±8000	
			IEC, powered-up only air-gap discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±15000	
		R_D = 330 Ω, C_S = 150 and 330 pF	ISO10605 contact discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±8000	
			ISO10605 air-gap discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±15000	
		R_D = 2 kΩ, C_S = 150 and 330 pF	ISO10605 contact discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±8000	
			ISO10605 air-gap discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, R_{IN1-})	±15000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Clock rate	5		35	MHz
	Supply noise			±100	mV_{P-P}
T_A	Operating free-air temperature	−40	25	105	°C

7.4 Thermal Information

THERMAL METRIC[1]		DS90C241-Q1 DS90C124-Q1 TFB (TQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	33.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS AND LVTTL DC SPECIFICATIONS							
V_{IH}	High-level voltage	*Tx:* DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, and VODSEL; and *Rx:* RPWDNB, RRFB, and REN		2		V_{CC}	V
V_{IL}	Low-level input voltage	*Tx:* DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, and VODSEL; and *Rx:* RPWDNB, RRFB, and REN		GND		0.8	V
V_{CL}	Input clamp voltage	I_{CL} = −18 mA, *Tx:* DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, and VODSEL; and *Rx:* RPWDNB, RRFB, and REN[1]			−0.8	−1.5	V
I_{IN}	Input current	V_{IN} = 0 V or 3.6 V	*Tx*: DIN[23:0], TCLK, TPWDNB, DEN, TRFB, DCAOFF, DCBOFF, and VODSEL	−10	±5	10	µA
			Rx: RPWDNB, RRFB, and REN	−20	±5	20	
V_{OH}	High-level output voltage	I_{OH} = −4 mA, *Rx:* ROUT[23:0], RCLK, and LOCK		2.3	3	V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, *Rx:* ROUT[23:0], RCLK, and LOCK		GND	0.33	0.5	V
I_{OS}	Output short circuit current	V_{OUT} = 0 V, *Rx:* ROUT[23:0], RCLK, and LOCK[1]		−40	−70	−110	mA
I_{OZ}	TRI-STATE output current	RPWDNB, REN = 0 V, V_{OUT} = 0 V or 2.4 V, *Rx:* ROUT[23:0], RCLK, and LOCK		−30	±0.4	30	µA
LVDS DC SPECIFICATIONS							
V_{TH}	Differential threshold high voltage	V_{CM} = 1.2 V, *Rx*: R_{IN+} and R_{IN-}				50	mV
V_{TL}	Differential threshold low voltage	*Rx*: R_{IN+} and R_{IN-}		−50			mV
I_{IN}	Input current	V_{IN} = 2.4 V, V_{CC} = 3.6 V or 0 V, *Rx*: R_{IN+} and R_{IN-}				±200	µA
		V_{IN} = 0 V, V_{CC} = 3.6 V, *Rx*: R_{IN+} and R_{IN-}				±200	
V_{OD}	Output differential voltage (D_{OUT+}) – (D_{OUT-})	R_L = 100 Ω, without pre-emphasis, *Tx*: D_{OUT+} and D_{OUT-} (see Figure 12)	VODSEL = L	250	400	600	mV
			VODSEL = H	450	750	1200	
ΔV_{OD}	Output differential voltage unbalance	R_L = 100 Ω, without pre-emphasis, *Tx*: D_{OUT+} and D_{OUT-}			10	50	mV
V_{OS}	Offset voltage	R_L = 100 Ω, without pre-emphasis, *Tx*: D_{OUT+} and D_{OUT-}		1	1.25	1.5	V
ΔV_{OS}	Offset voltage unbalance	R_L = 100 Ω, without pre-emphasis, *Tx*: D_{OUT+} and D_{OUT-}			1	50	mV

(1) Specification is ensured by characterization and is not tested in production.

Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OS}	Output short circuit current	DOUT = 0 V, DIN = H, TPWDNB, DEN = 2.4 V, *Tx*: D_{OUT+} and D_{OUT-}	VODSEL = L	−2		−8	mA
		DOUT = 0 V, DIN = H, TPWDNB, DEN = 2.4 V, *Tx*: D_{OUT+} and D_{OUT-}	VODSEL = H	−7		−13	
I_{OZ}	TRI-STATE output current	TPWDNB, DEN = 0 V, DOUT = 0 V or 2.4 V, *Tx*: D_{OUT+} and D_{OUT-}		−15	±1	15	µA
SERIALIZER OR DESERIALIZER SUPPLY CURRENT – DVDDx, PVDDx, AND AVDDx PINS (*Digital, PLL, and Analog VDDs*)							
I_{CCT}	Serializer (Tx) total supply current (includes load current)	R_L = 100 Ω, R_{PRE} = OFF, VODSEL = H/L, f = 35 MHz, and checker-board pattern (see Figure 3)			40	65	mA
		R_L = 100 Ω, R_{PRE} = 6 kΩ, VODSEL = H/L, f = 35 MHz, and checker-board pattern (see Figure 3)			45	70	mA
	Serializer (Tx) total supply current (includes load current)	f = 35 MHz, R_L = 100 Ω, R_{PRE} = OFF, and VODSEL = H/L			40	65	mA
		f = 35 MHz, R_L = 100 Ω, R_{PRE} = 6 kΩ, VODSEL = H/L, and random pattern			45	70	mA
I_{CCTZ}	Serializer (Tx) supply current power-down	TPWDNB = 0 V (all other LVCMOS inputs = 0 V)				800	µA
I_{CCR}	Deserializer (Rx) total supply current (includes load current)	C_L = 8-pF LVCMOS output, f = 35 MHz, and checker-board pattern (see Figure 4)				85	mA
	Deserializer (Rx) total supply current (includes load current)	C_L = 8-pF LVCMOS output, f = 35 MHz, and random pattern				80	mA
I_{CCRZ}	Deserializer (Rx) supply current power-down	RPWDNB = 0 V (all other LVCMOS inputs = 0 V, R_{IN+}/ R_{IN-} = 0 V)				50	µA

7.6 Timing Requirements – Serializer

over recommended operating supply and temperature ranges (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_{TCP}	Transmit clock period (see Figure 7)	28.6	T	200	ns
t_{TCIH}	Transmit clock high time	0.4T	0.5T	0.6T	ns
t_{TCIL}	Transmit clock low time	0.4T	0.5T	0.6T	ns
t_{CLKT}	TCLK input transition time (see Figure 6)		3	6	ns
t_{JIT}	TCLK input jitter (1)			33	ps (RMS)

(1) t_{JIT} (at BER of 10e-9) specifies the allowable jitter on TCLK. t_{JIT} not included in TxOUT_E_O parameter.

7.7 Switching Characteristics – Serializer

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LLHT}	LVDS Low-to-High transition time	R_L = 100 Ω, C_L = 10 pF to GND, and VODSEL = L (see Figure 5)			0.6	ns
t_{LHLT}	LVDS High-to-Low transition time	R_L = 100 Ω, C_L = 10 pF to GND, and VODSEL = L (see Figure 5)			0.6	ns
t_{DIS}	DIN[23:0] setup to TCLK	R_L = 100 Ω and C_L = 10 pF to GND (1)	5			ns
t_{DIH}	DIN[23:0] hold from TCLK	R_L = 100 Ω and C_L = 10 pF to GND (1)	5			ns
t_{HZD}	DOUT± HIGH to TRI-STATE delay	R_L = 100 Ω and C_L = 10 pF to GND (see Figure 8) (2)			15	ns
t_{LZD}	DOUT± LOW to TRI-STATE delay	R_L = 100 Ω and C_L = 10 pF to GND (see Figure 8) (2)			15	ns
t_{ZHD}	DOUT± TRI-STATE to HIGH delay	R_L = 100 Ω and C_L = 10 pF to GND (see Figure 8) (2)			200	ns
t_{ZLD}	DOUT± TRI-STATE to LOW delay	R_L = 100 Ω and C_L = 10 pF to GND (see Figure 8) (2)			200	ns
t_{PLD}	Serializer PLL lock time	R_L = 100 Ω (see Figure 9)			10	ms
t_{SD}	Serializer delay	R_L = 100 Ω, VODSEL = L, and TRFB = H (see Figure 10)		3.5T + 2.85	3.5T + 10	ns
		R_L = 100 Ω, VODSEL = L, and TRFB = L (see Figure 10)		3.5T + 2.85	3.5T + 10	ns
TxOUT_E_O	TxOUT_Eye_Opening (respect to ideal)	5 MHz to 35 MHz (see Figure 11) (1) (3) (4)	0.75			UI (5)

(1) Specification is ensured by characterization and is not tested in production.
(2) When the serializer output is tri-stated, the deserializer loses PLL lock. Resynchronization *must* occur before data transfer.
(3) t_{JIT} (at BER of 10e-9) specifies the allowable jitter on TCLK. t_{JIT} not included in TxOUT_E_O parameter.
(4) TxOUT_E_O is affected by pre-emphasis value.
(5) UI – Unit Interval; equivalent to one ideal serialized data bit width. The UI scales with frequency.

7.8 Switching Characteristics – Deserializer

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{RCP}	Receiver out clock period	t_{RCP} = t_{TCP} and RCLK pin (1)	28.6		200	ns
t_{RDC}	RCLK duty cycle	RCLK pin	45%	50%	55%	
t_{CLH}	LVCMOS low-to-high transition time	C_L = 8 pF (lumped load); ROUT[23:0], LOCK, and RCLK pins (see Figure 13) (1)		2.5	3.5	ns
t_{CHL}	LVCMOS high-to-low transition time	C_L = 8 pF (lumped load); ROUT[23:0], LOCK, and RCLK pins (see Figure 13) (1)		2.5	3.5	ns
t_{ROS}	ROUT[7:0] setup data to RCLK (Group 1)	ROUT[7:0] pins (see Figure 17)	0.4 × t_{RCP}	(29/56) × t_{RCP}		ns
t_{ROH}	ROUT[7:0] hold data to RCLK (Group 1)	ROUT[7:0] pins (see Figure 17)	0.4 × t_{RCP}	(27/56) × t_{RCP}		ns
t_{ROS}	ROUT[15:8] setup data to RCLK (Group 2)	ROUT[15:8] and LOCK pins (see Figure 17)	0.4 × t_{RCP}	0.5 × t_{RCP}		ns
t_{ROH}	ROUT[15:8] hold data to RCLK (Group 2)	ROUT[15:8] and LOCK pins (see Figure 17)	0.4 × t_{RCP}	0.5 × t_{RCP}		ns
t_{ROS}	ROUT[23:16] setup data to RCLK (Group 3)	ROUT[23:16] pins (see Figure 17)	0.4 × t_{RCP}	(27/56) × t_{RCP}		ns
t_{ROH}	ROUT[23:16] hold data to RCLK (Group 3)	ROUT[23:16] pins (see Figure 17)	0.4 × t_{RCP}	(29/56) × t_{RCP}		ns
t_{HZR}	HIGH to TRI-STATE delay	ROUT[23:0], RCLK, and LOCK pins (see Figure 15)		3	10	ns

(1) Specification is ensured by characterization and is not tested in production.

Switching Characteristics – Deserializer (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{LZR}	LOW to TRI-STATE delay	ROUT[23:0], RCLK, and LOCK pins			3	10	ns
t_{ZHR}	TRI-STATE to HIGH delay	ROUT[23:0], RCLK, and LOCK pins			3	10	ns
t_{ZLR}	TRI-STATE to LOW delay	ROUT[23:0], RCLK, and LOCK pins			3	10	ns
t_{DD}	Deserializer delay	RCLK pin (see Figure 14)			[4+(3/56)]T + 5.9	[4+(3/56)]T + 14	ns
t_{DRDL}	Deserializer PLL lock time from power down	See Figure 16 (1)(2)	5 MHz		5	50	ms
			35 MHz		5	50	
RxIN_TOL_L	Receiver input tolerance (left)	5 MHz to 35 MHz (see Figure 18) (1)(3)				0.25	UI (4)
RxIN_TOL_R	Receiver input tolerance (right)	5 MHz to 35 MHz (see Figure 18) (1)(3)				0.25	UI (4)

(2) The deserializer PLL lock time (t_{DRDL}) may vary depending on input data patterns and the number of transitions within the pattern.
(3) RxIN_TOL is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. It is a measurement in reference with the ideal bit position. See *AN-1217 How to Validate BLVDS SER/DES Signal Integrity Using an Eye Mask* (SNLA053) for details.
(4) UI – Unit Interval; equivalent to one ideal serialized data bit width. The UI scales with frequency.

7.9 Typical Characteristics

Figure 1 and Figure 2 are scope shots with PCLK = 5 MHz measured out of the DS90C241 DOUT± with pre-emphasis OFF and pre-emphasis ON using a 1010... pattern on the DIN[23:0] inputs. The scope was triggered on the input PCLK.

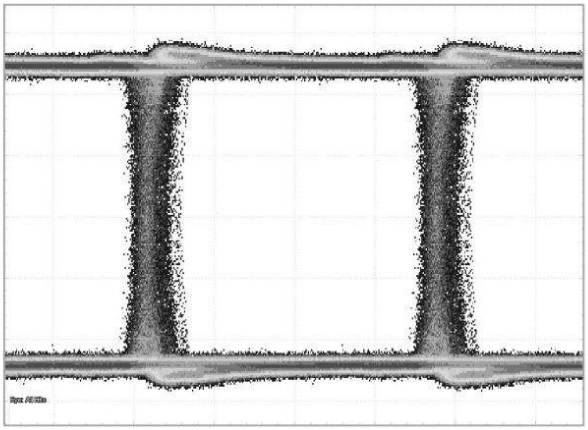


Figure 1. DS90C241 DOUT± Eye Diagram at 5 MHz Without Pre-Emphasis

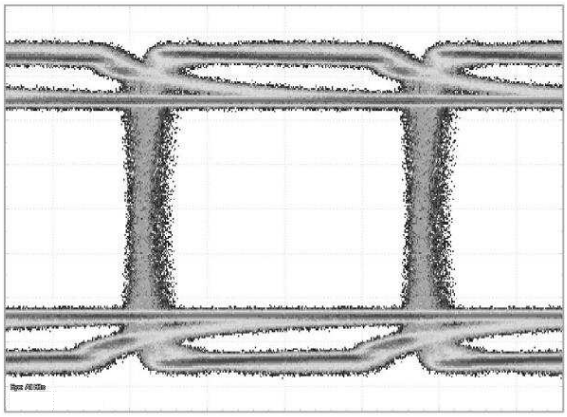


Figure 2. DS90C241 DOUT± Eye Diagram at 5 MHz With Pre-Emphasis ON

8 Parameter Measurement Information

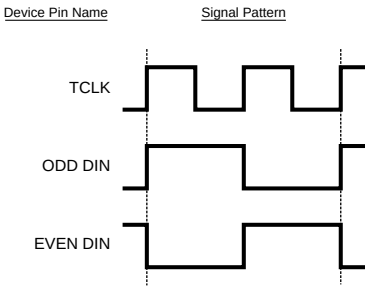


Figure 3. Serializer Input Checkerboard Pattern

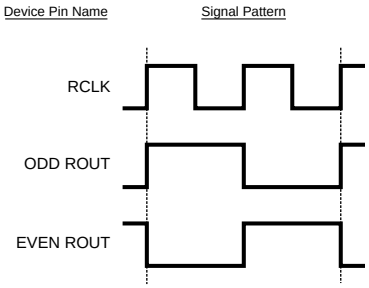


Figure 4. Deserializer Output Checkerboard Pattern

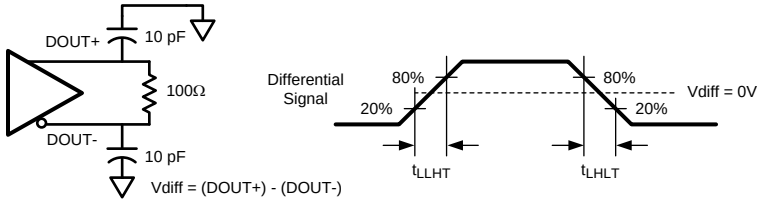


Figure 5. Serializer LVDS Output Load and Transition Times

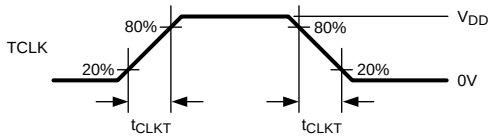


Figure 6. Serializer Input Clock Transition Times

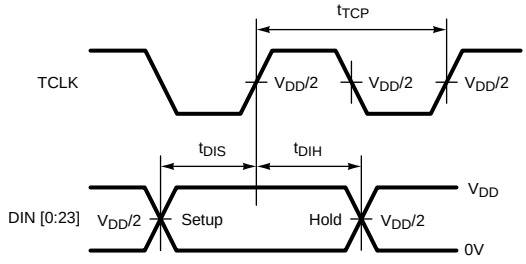


Figure 7. Serializer Setup and Hold Times

Parameter Measurement Information (continued)

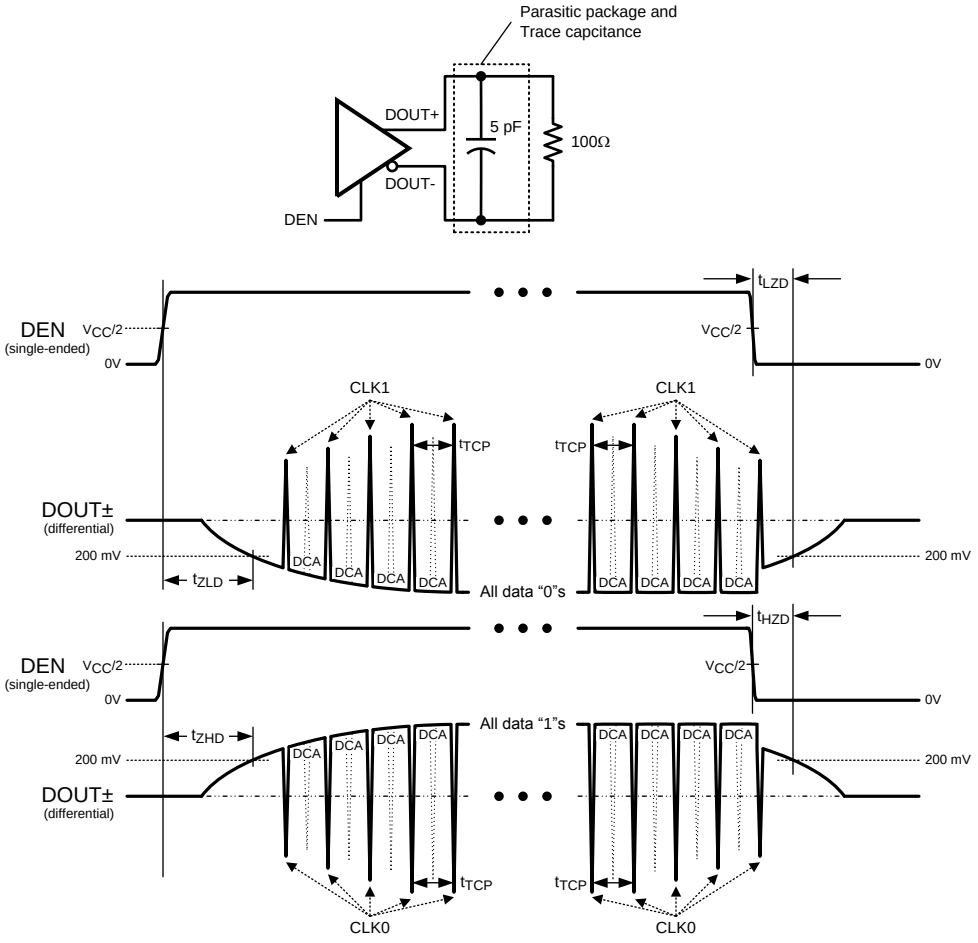


Figure 8. Serializer TRI-STATE Test Circuit and Delay

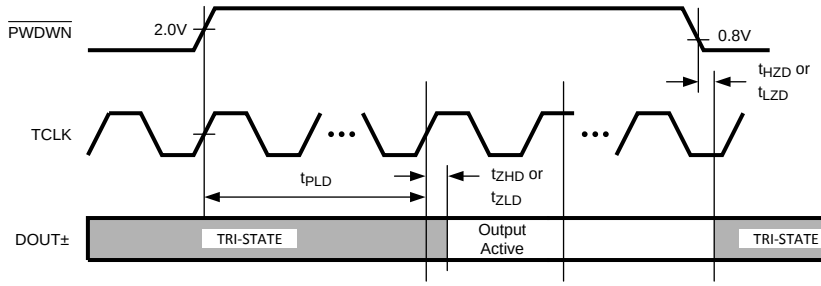


Figure 9. Serializer PLL Lock Time and TPWDNB TRI-STATE Delays

Parameter Measurement Information (continued)

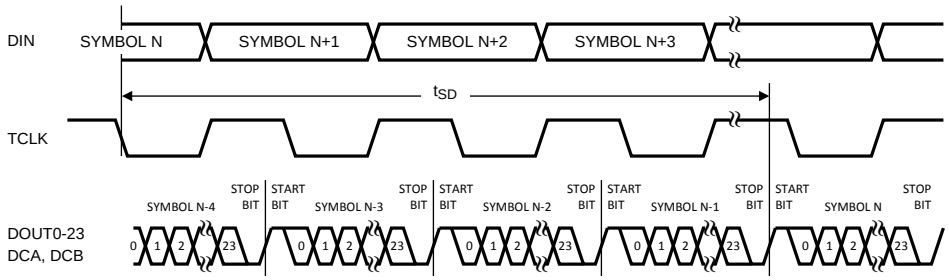


Figure 10. Serializer Delay

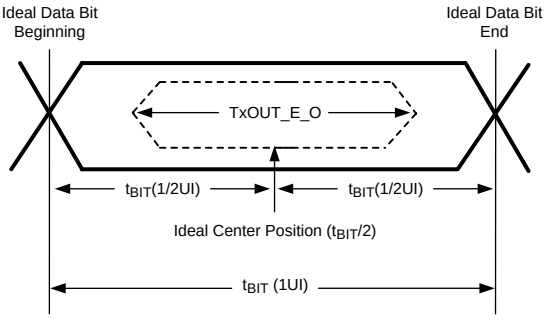
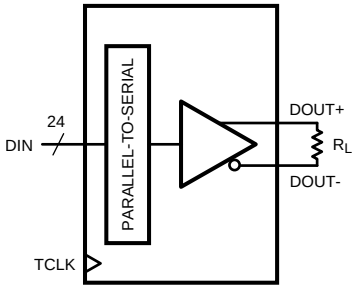


Figure 11. Transmitter Output Eye Opening (TxOUT_E_O)



$VOD = (D_{OUT+}) – (D_{OUT\ -})$
Differential output signal is shown as $(D_{OUT+}) – (D_{OUT\ -})$ with the device in data transfer mode.

Figure 12. Serializer VOD Diagram

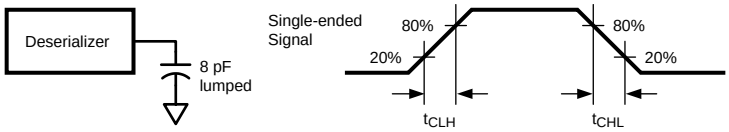


Figure 13. Deserializer LVCMOS/LVTTL Output Load and Transition Times

Parameter Measurement Information (continued)

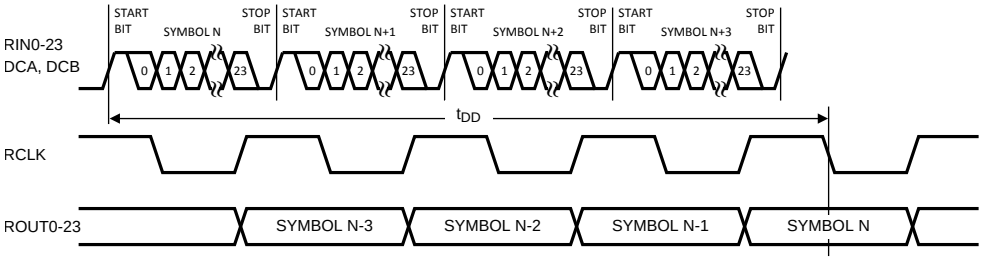
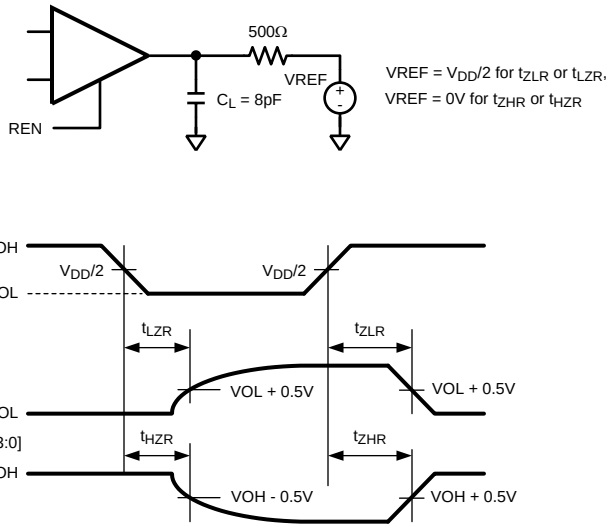


Figure 14. Deserializer Delay



C_L includes instrumentation and fixture capacitance within 6 cm of ROUT[23:0].

Figure 15. Deserializer TRI-STATE Test Circuit and Timing

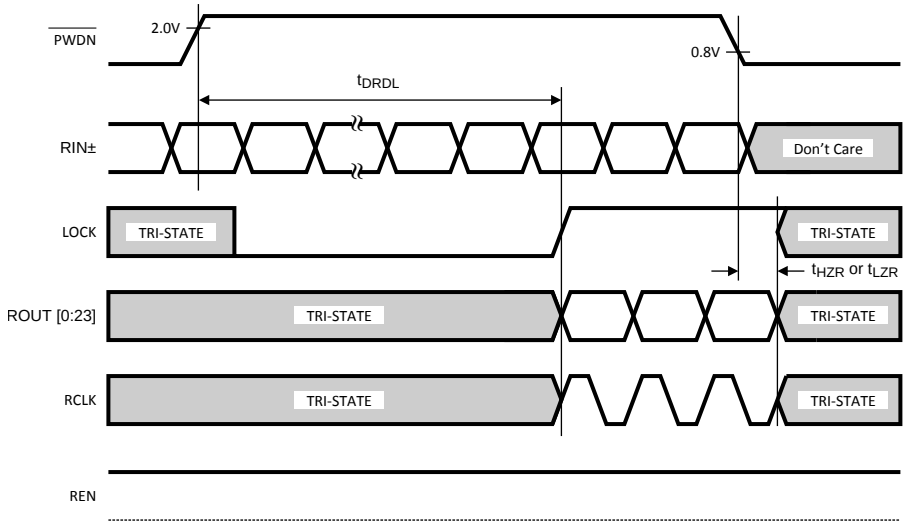


Figure 16. Deserializer PLL Lock Times and RPWDNB TRI-STATE Delay

Parameter Measurement Information (continued)

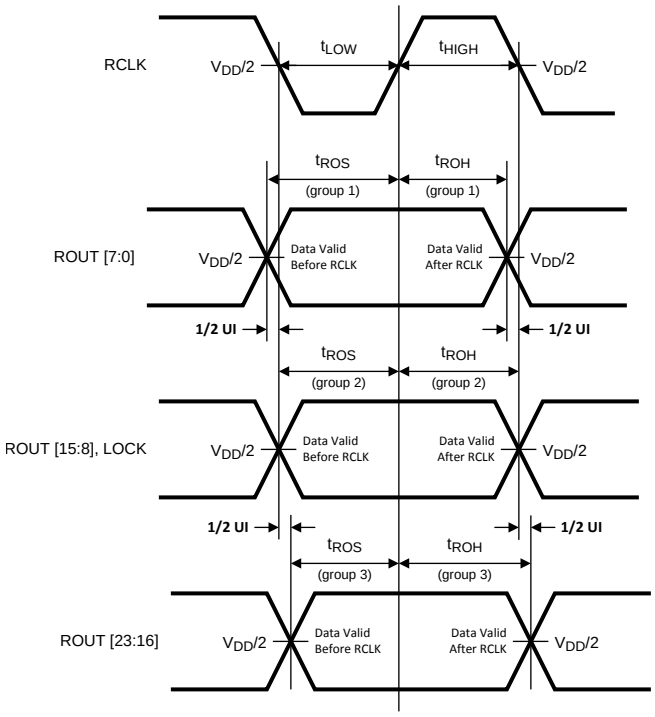
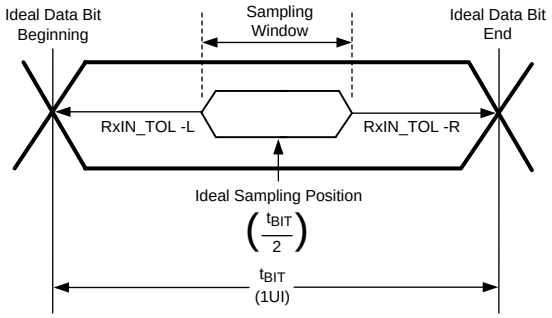


Figure 17. Deserializer Setup and Hold Times



RxIN_TOL_L is the ideal noise margin on the left of the figure with respect to ideal.
RxIN_TOL_R is the ideal noise margin on the right of the figure with respect to ideal.

Figure 18. Receiver Input Tolerance (RxIN_TOL) and Sampling Window

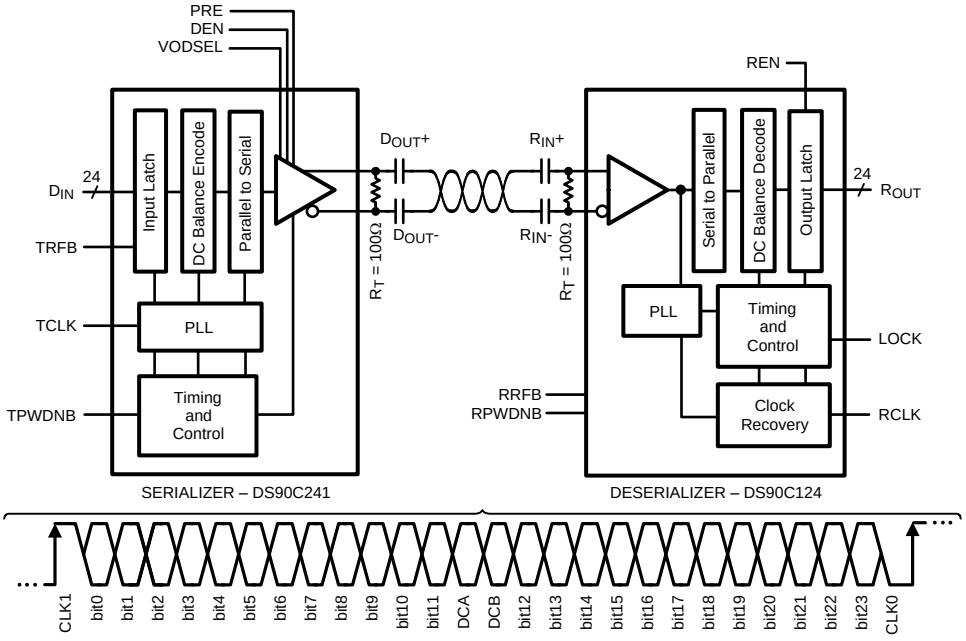
9 Detailed Description

9.1 Overview

The DS90C241 serializer and DS90C124 deserializer chipset is an easy-to-use transmitter and receiver pair that sends 24-bits of parallel LVCMOS data over a single serial LVDS link from 120 Mbps to 840 Mbps throughput. The DS90C241 transforms a 24-bit wide parallel LVCMOS data into a single high speed LVDS serial data stream with embedded clock, and scrambles or DC balances the data to enhance signal quality to support AC coupling. The DS90C124 receives the LVDS serial data stream and converts it back into a 24-bit wide parallel data and recovered clock. The 24-bit serializer or deserializer chipset is designed to transmit data up to 10 meters over shielded twisted pair (STP) at clock speeds from 5 MHz to 35 MHz.

The deserializer can attain lock to a data stream without the use of a separate reference clock source. This greatly simplifies system complexity and overall cost. The deserializer synchronizes to the serializer regardless of data pattern, delivering true automatic *plug and lock* performance. It locks to the incoming serial stream without the requirement of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information and validating data integrity from the incoming data stream and then deserializes the data. The deserializer monitors the incoming clock information, determines lock status, and asserts the LOCK output high when lock occurs. Each has a power down control to enable efficient operation in various applications.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Initialization and Locking Mechanism

Initialization of the DS90C241 and DS90C124 must be established before each device sends or receives data. Initialization refers to synchronizing the PLLS of the serializer and the deserializer together. After the serializers locks to the input clock source, the deserializer synchronizes to the serializers as the second and final initialization step.

1. When V_{CC} is applied to both serializer or deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.2 V) the PLL in serializer begins locking to a clock input. For the serializer, the local clock is the transmit clock, TCLK. The serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the

Feature Description (continued)

serializer block is now ready to send data patterns. The deserializer output remains in TRI-STATE while its PLL locks to the embedded clock information in serial data stream. Also, the deserializer LOCK output remains low until its PLL locks to incoming data and sync-pattern on the RIN± pins.

2. The deserializer PLL acquires lock to a data stream without requiring the serializer to send special patterns. The serializer that is generating the stream to the deserializer automatically sends random (non-repetitive) data patterns during this step of the Initialization State. The deserializer locks onto the embedded clock within the specified amount of time. An embedded clock and data recovery (CDR) circuit locks to the incoming bit stream to recover the high-speed receive bit clock and re-time incoming data. The CDR circuit expects a coded input bit stream. In order for the deserializer to lock to a random data stream from the serializer, it performs a series of operations to identify the rising clock edge and validates data integrity, then locks to it. Because this locking procedure is independent on the data pattern, total random locking duration may vary. At the point when the CDR of the deserializer locks to the embedded clock, the LOCK pin goes high and valid RCLK/data appears on the outputs. Note that the LOCK signal is synchronous to valid data appearing on the outputs. The deserializer's LOCK pin is a convenient way to ensure data integrity is achieved on receiver side.

9.3.2 Data Transfer

After serializer lock is established, the inputs DIN0 to DIN23 may be used to input data to the serializer. Data is clocked into the serializer by the TCLK input. The edge of TCLK used to strobe the data is selectable through the TRFB pin. TRFB high selects the rising edge for clocking data and low selects the falling edge. The serializer outputs (DOUT±) are intended to drive point-to-point connections as shown in Figure 19.

CLK1, CLK0, DCA, DCB are four overhead bits transmitted along the single LVDS serial data stream. The CLK1 bit is always high and the CLK0 bit is always low. The CLK1 and CLK0 bits function as the embedded clock bits in the serial stream. DCB functions as the DC Balance control bit. It does not require any precoding of data on transmit side. The DC Balance bit is used to minimize the short and long-term DC bias on the signal lines. This bit operates by selectively sending the data either unmodified or inverted. The DCA bit is used to validate data integrity in the embedded data stream. Both DCA and DCB coding schemes are integrated and automatically performed within serializer and deserializer.

Serialized data and clock or control bits (24 +4 bits) are transmitted from the serial data output (DOUT±) at 28 times the TCLK frequency. For example, if TCLK is 35 MHz, the serial rate is 35 × 28 = 980 Mega bits per second. Because only 24 bits are from input data, the serial *payload* rate is 24 times the TCLK frequency. For example, if TCLK = 35 MHz, the payload data rate is 35 × 24 = 840 Mbps. TCLK is provided by the data source and must be in the range of 5 MHz to 35 MHz nominal. The serializer outputs (DOUT±) can drive a point-to-point connection. The outputs transmit data when the enable pin (DEN) is high, TPWDNB is high. The DEN pin may be used to TRI-STATE the outputs when driven low.

When the deserializer channel attains lock to the input from a serializer, it drives its LOCK pin high and synchronously delivers valid data and recovered clock on the output. The deserializer locks onto the embedded clock, uses it to generate multiple internal data strobes, and then drives the recovered clock to the RCLK pin. The recovered clock (RCLK output pin) is synchronous to the data on the ROUT[23:0] pins. While LOCK is high, data on ROUT[23:0] is valid. Otherwise, ROUT[23:0] is invalid. The polarity of the RCLK edge is controlled by the RRFB input. ROUT[23:0], LOCK, and RCLK outputs each drive a maximum of 8-pF load with 35-MHz clock. REN controls TRI-STATE for ROUTn and the RCLK pin on the deserializer.

9.3.3 Resynchronization

If the deserializer loses lock, it automatically tries to re-establish lock. For example, if the embedded clock edge is not detected one time in succession, the PLL loses lock and the LOCK pin is driven low. The deserializer then enters the operating mode where it tries to lock to a random data stream. It looks for the embedded clock edge, identifies it and then proceeds through the locking process. The logic state of the LOCK signal indicates whether the data on ROUT is valid; when it is high, the data is valid. The system must monitor the LOCK pin to determine whether data on the ROUT is valid.

Feature Description (continued)

9.3.4 Pre-Emphasis

The DS90C241 features a pre-emphasis function used to compensate for long or lossy transmission media. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. The transmission distance is limited by the loss characteristics and quality of the media. Pre-emphasis adds extra current during LVDS logic transition to reduce the cable loading effects and increase driving distance. In addition, pre-emphasis helps provide faster transitions, increased eye openings, and improved signal integrity. To enable the pre-emphasis function, the *PRE* pin requires one external resistor (Rpre) to Vss to set the additional current level. Pre-emphasis strength is set through an external resistor (Rpre) applied from min to max (floating to 3 kΩ) at the *PRE* pin. A lower input resistor value on the *PRE* pin increases the magnitude of dynamic current during data transition. There is an internal current source based on the following formula: PRE = (Rpre ≥ 3 kΩ); I_{MAX} = [(1.2/Rpre) × 20]. The ability of the DS90C241 to use the pre-emphasis feature extends the transmission distance up to 10 meters in most cases.

The amount of pre-emphasis for a given media depends on the transmission distance of the application. In general, too much pre-emphasis can cause over or undershoot at the receiver input pins. This can result in excessive noise, crosstalk and increased power dissipation. For short cables or distances, pre-emphasis may not be required. Signal quality measurements are recommended to determine the proper amount of pre-emphasis for each application.

9.3.5 AC-Coupling and Termination

The DS90C241 and DS90C124 supports AC-coupled interconnects through integrated DC balanced encoding/decoding scheme. To use AC coupled connection between the serializer and deserializer, insert external AC coupling capacitors in series in the LVDS signal path as illustrated in Figure 19. The deserializer input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal V_{CM} to 1.2 V. With AC signal coupling, capacitors provide the AC-coupling path to the signal input.

For the high-speed LVDS transmissions, the smallest available package must be used for the AC-coupling capacitor. This helps minimize degradation of signal quality due to package parasitics. The most common used capacitor value for the interface is 100-nF (0.1-µF) capacitor. NPO class 1 or X7R class 2 type capacitors are recommended. 50-WVDC must be the minimum used for the best system-level ESD performance.

The DS90C124 input stage is designed for AC-coupling by providing a built-in AC bias network which sets the internal VCM to 1.2 V. Therefore multiple termination options are possible.

9.3.5.1 Receiver Termination Options

9.3.5.1.1 Option 1

A single, 100-Ω termination resistor is placed across the RIN± pins (see Figure 19). This provides the signal termination at the receiver inputs. Other options may be used to increase noise tolerance.

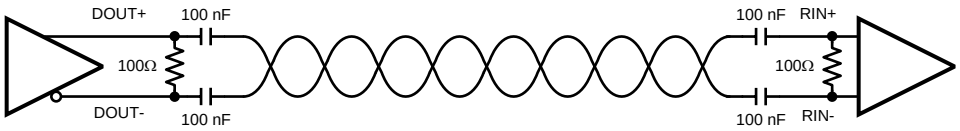


Figure 19. AC Coupled Application

9.3.5.1.1.1 Option 2

For additional EMI tolerance, two 50-Ω resistors may be used in place of the single 100-Ω resistor. A small capacitor is tied from the center point of the 50-Ω resistors to ground (see Figure 20). This provides a high-frequency low impedance path for noise suppression. Value is not critical; 4.7 nF may be used with general applications.

Feature Description (continued)

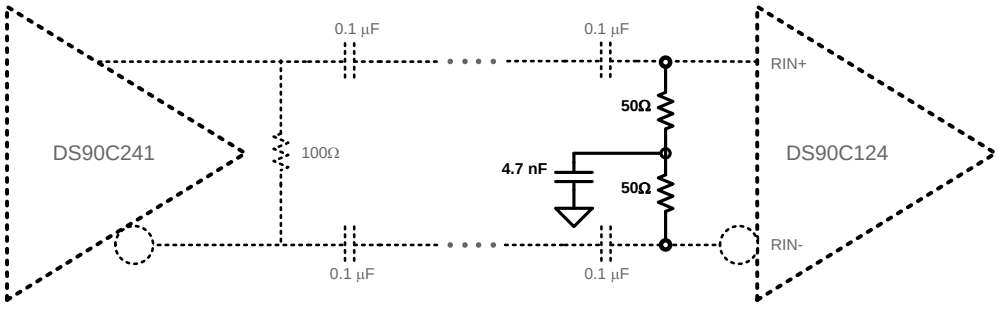


Figure 20. Receiver Termination Option 2

9.3.5.1.1.2 Option 3

For high noise environments an additional voltage divider network may be connected to the center point. This has the advantage of a providing a DC low-impedance path for noise suppression. Use resistor values in the range of 75 Ω to 2 KΩ for the pullup and pulldown. Ratio the resistor values to bias the center point at 1.2 V. For example (see Figure 21), VDD = 3.3 V, Rpullup = 1.3 kΩ, Rpulldown = 750 Ω; or Rpullup = 130 Ω, Rpulldown = 75 Ω (strongest). The smaller values consume more bias current, but provide enhanced noise suppression.

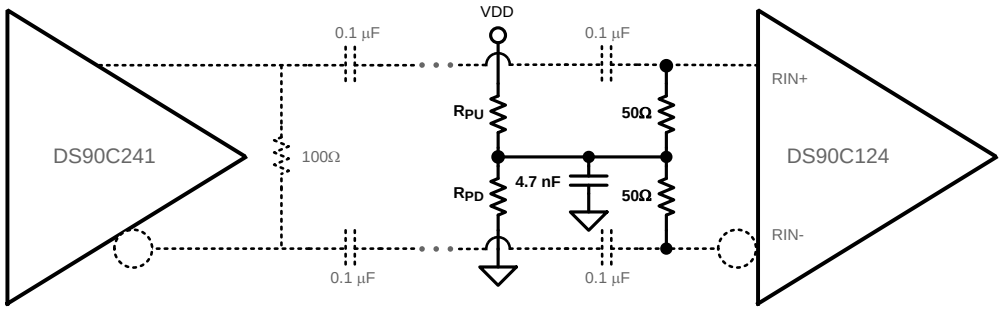


Figure 21. Receiver Termination Option 3

9.4 Device Functional Modes

Table 1 and Table 2 list the truth tables for the serializer and deserializer.

Table 1. DS90C241 Serializer Truth Table

TPWDNB (PIN 9)	DEN (PIN 18)	Tx PLL STATUS (INTERNAL)	LVDS OUTPUTS (PINS 19 AND 20)
L	X	X	Hi Z
H	L	X	Hi Z
H	H	Not locked	Hi Z
H	H	Locked	Serialized data with embedded clock

Table 2. DS90C124 Deserializer Truth Table

RPWDNB (PIN 1)	REN (PIN 48)	Rx PLL STATUS (INTERNAL)	ROUTn AND RCLK (SEE PIN DIAGRAM)	LOCK (PIN 17)
L	X	X	Hi Z	Hi Z
H	L	X	Hi Z	L = PLL unocked H = PLL locked
H	H	Not locked	Hi Z	L

Table 2. DS90C124 Deserializer Truth Table (continued)

RPWDNB (PIN 1)	REN (PIN 48)	Rx PLL STATUS (INTERNAL)	ROUTn AND RCLK (SEE PIN DIAGRAM)	LOCK (PIN 17)
H	H	Locked	Data and RCLK active	H

9.4.1 Power Down

The power-down state is a low power sleep mode that the serializer and deserializer may use to reduce power when no data is being transferred. The TPWDNB and RPWDNB are used to set each device into power down mode, which reduces supply current to the µA range. The serializer enters power down when the TPWDNB pin is driven low. In power down, the PLL stops and the outputs go into TRI-STATE, disabling load current and reducing supply. To exit power down, TPWDNB must be driven high. When the serializer exits power down, its PLL must lock to TCLK before it is ready for the Initialization state. The system must then allow time for Initialization before data transfer can begin. The deserializer enters power down mode when RPWDNB is driven low. In power down mode, the PLL stops and the outputs enter TRI-STATE. To bring the deserializer block out of the power down state, the system drives RPWDNB high.

Both the serializer and deserializer must reinitialize and relock before data can be transferred. The deserializer initializes and asserts LOCK high when it is locked to the input clock.

9.4.2 Tri-State

For the serializer, TRI-STATE is entered when the DEN or TPWDNB pin is driven low. This does TRI-STATE both driver output pins (DOUT+ and DOUT−). When DEN is driven high, the serializer returns to the previous state as long as all other control pins remain static (TPWDNB, TRFB).

When you drive the REN or RPWDNB pin low, the deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0 to ROUT23) and RCLK enters TRI-STATE. The LOCK output remains active, reflecting the state of the PLL. The deserializer input pins are high impedance during receiver power down (RPWDNB low) and power-off (V_{CC} = 0 V).

9.4.3 Progressive Turn–On (PTO)

Deserializer ROUT[23:0] outputs are grouped into three groups of eight, with each group switching about 0.5-UI apart in phase to reduce EMI, simultaneous switching noise, and system ground bounce.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Using the DS90C241 and DS90C124

The DS90C241/DS90C124 serializer or deserializer (SERDES) pair sends 24 bits of parallel LVCMOS data over a serial LVDS link up to 840 Mbps. Serialization of the input data is accomplished using an on-board PLL at the serializer which embeds clock with the data. The deserializer extracts the clock/control information from the incoming data stream and deserializes the data. The deserializer monitors the incoming clockl information to determine lock status and indicates lock by asserting the LOCK output high.

10.1.2 Display Application

The DS90C241/DS90C124 chipset is intended for interface between a host (graphics processor) and a display. It supports an 18-bit color depth (RGB666) and up to 800 × 480 display formats. In a RGB666 configuration 18 color bits (R[5:0], G[5:0], B[5:0]), Pixel Clock (PCLK) and three control bits (VS, HS, and DE) along with three spare bits are supported across the serial link with PCLK rates from 5 MHz to 35 MHz.

10.2 Typical Application

Figure 22 shows a typical application of the DS90C241 serializer (SER). The LVDS outputs use a 100-Ω termination and 100-nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. A system General Purpose Output (GPO) controls the TPWDNB pin. In this application the TRFB pin is tied High to latch data on the rising edge of the TCLK. The DEN signal is not used and is tied High also. In this application, the link is short; therefore, the VODSEL pin is tied Low for the standard LVDS swing. The pre-emphasis input uses a resistor to ground to set the amount of pre-emphasis desired by the application.

Figure 23 shows a typical application of the DS90C124 deserializer (DES). The LVDS inputs use a 100-Ω termination and 100-nF coupling capacitors to the line. Bypass capacitors are placed near the power supply pins. A system GPO controls the RPWDNB pin. In this application, the RRFB pin is tied high to strobe the data on the rising edge of the RCLK. The REN signal is not used and is tied high also.

Typical Application (continued)

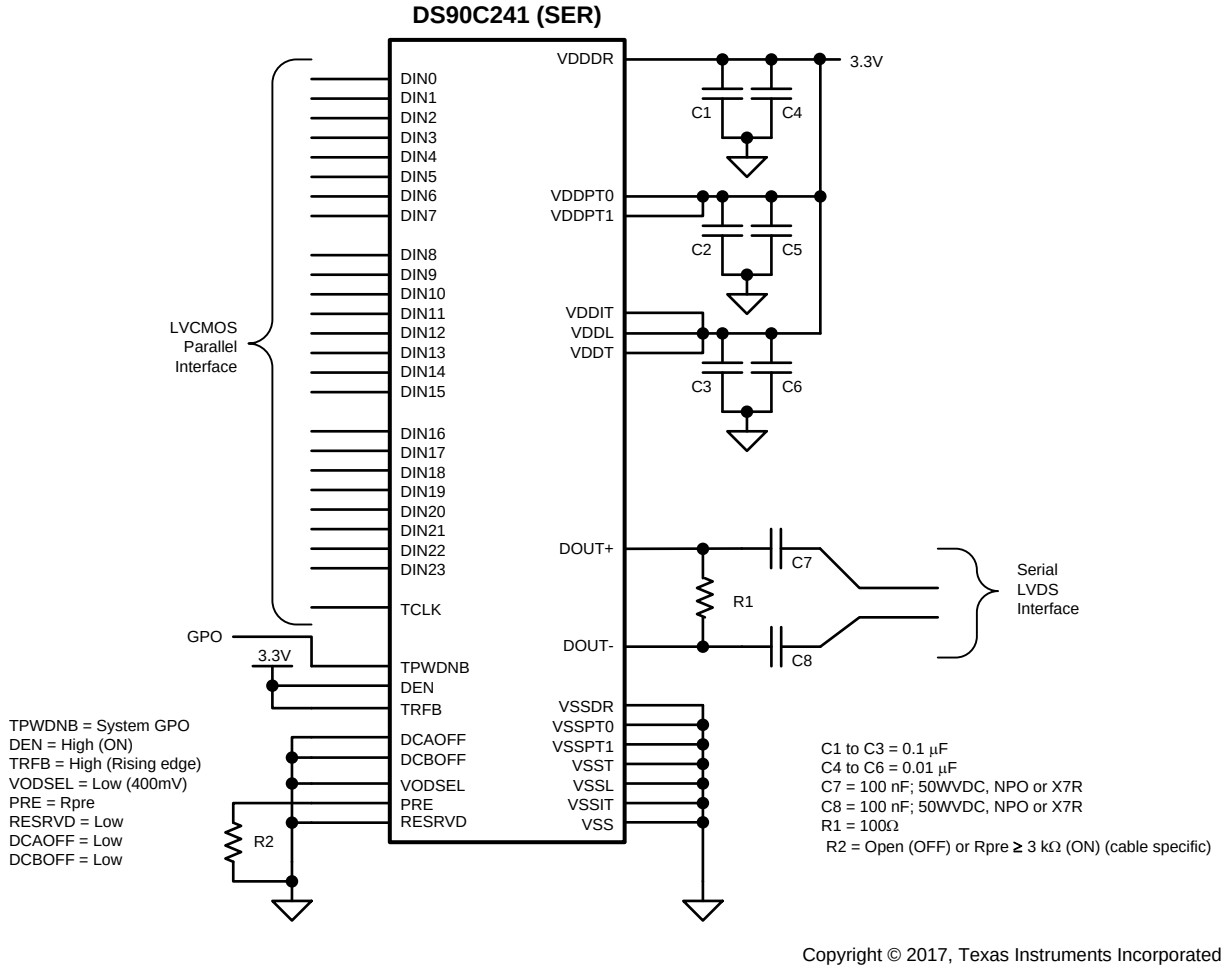


Figure 22. DS90C241 Typical Application Connection

Typical Application (continued)

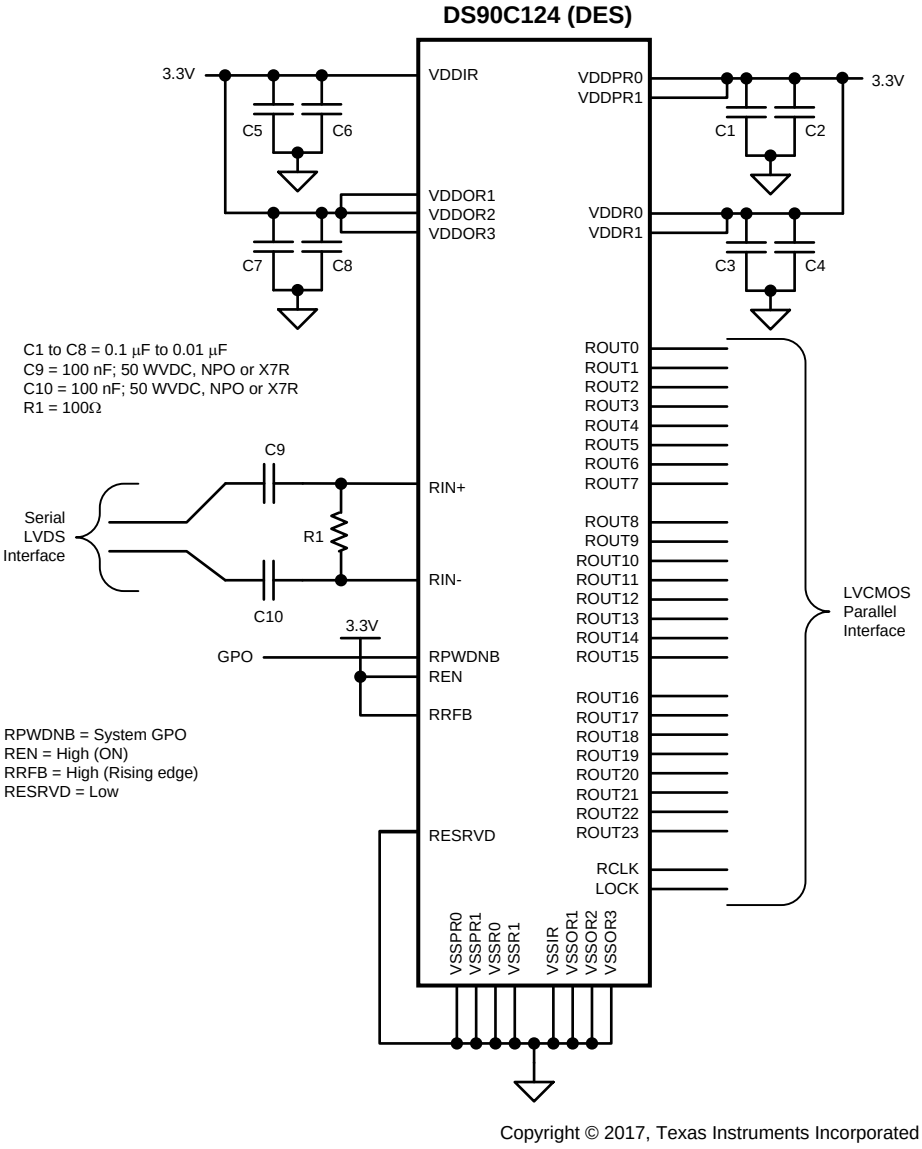


Figure 23. DS90C124 Tyical Application Connection

10.2.1 Design Requirements

For the typical design application, use the following as input parameters:

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 22 and Figure 23.

Typical Application (continued)

10.2.2 Detailed Design Procedure

Circuit board layout and stack-up for the LVDS serializer and deserializer devices must be designed to provide low-noise power to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power and ground sandwiches. This arrangement uses the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors must include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 10 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the tantalum capacitors must be at least 5 times the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 µF to 100 µF range and smooth low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with through on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range from 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Use at least a four layer board with a power and ground plane. Place LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

10.2.2.1 Noise Margin

The deserializer noise margin is the amount of input jitter (phase noise) that the deserializer can tolerate and still reliably recover data. Various environmental and systematic factors include:

- Serializer: TCLK jitter, V_{CC} noise (noise bandwidth and out-of-band noise)
- Media: ISI, V_{CM} noise
- Deserializer: V_{CC} noise

For a graphical representation of noise margin, see Figure 18.

10.2.2.2 Transmission Media

The serializer and deserializer can be used in point-to-point configuration, through a PCB trace, or through twisted pair cable. In a point-to-point configuration, the transmission media requires termination at both ends of the transmitter and receiver pair. Interconnect for LVDS typically has a differential impedance of 100 Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. In most applications that involve cables, the transmission distance is determined on data rates involved, acceptable bit error rate and transmission medium.

The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. The Receiver Input Tolerance in *Switching Characteristics – Deserializer* and the Differential Threshold Voltage specifications in *Electrical Characteristics* define the acceptable data eye opening. A differential probe must be used to measure across the termination resistor at the DS90C124 inputs. Figure 24 illustrates the eye opening and relationship to the receiver input tolerance and differential threshold voltage specifications.

Typical Application (continued)

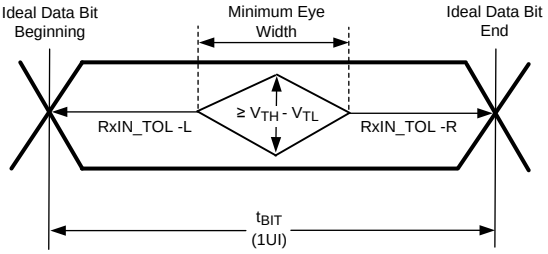


Figure 24. Receiver Input Eye Opening

10.2.2.3 Live Link Insertion

The serializer and deserializer devices support live pluggable applications. The automatic receiver lock to random data *plug and go* hot insertion capability allows the DS90C124 to attain lock to the active data stream during a live insertion event.

10.2.3 Application Curves

Figure 25, Figure 26, and Figure 27 are scope shots with PCLK = 25 MHz into the DS90C241 with a 1010... pattern on the DIN[23:0] inputs. The scope was triggered on the input PCLK.

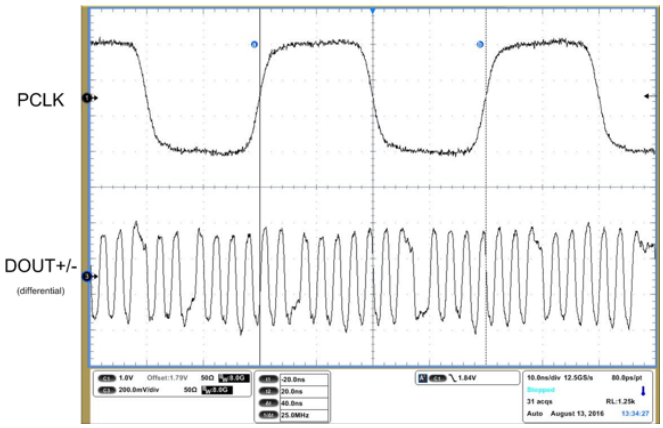


Figure 25. Input PCLK = 25 MHz and Associated DOUT Serial Stream

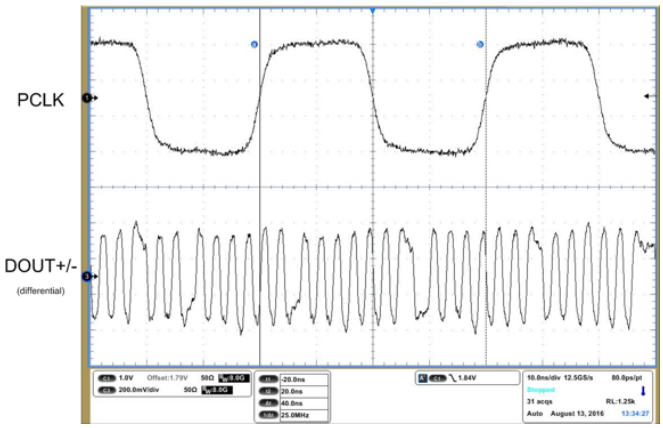


Figure 26. Input PCLK = 25 MHz and Associated DOUT Serial Stream With Pre-Emphasis

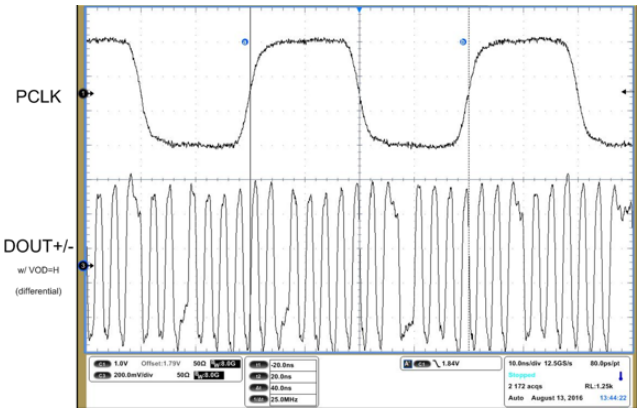


Figure 27. Input PCLK = 25 MHz and Associated DOUT Serial Stream With VODSEL = H

Typical Application (continued)

Figure 28, Figure 29, and Figure 30 are scope shots with PCLK = 33 MHz into the DS90C241 with a 1010... pattern on the DIN[23:0] inputs. The scope was triggered on the input PCLK.

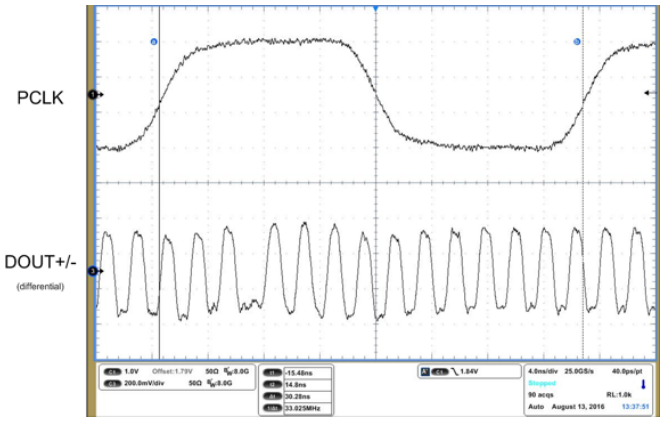


Figure 28. Input PCLK = 33 MHz and Associated DOUT Serial Stream

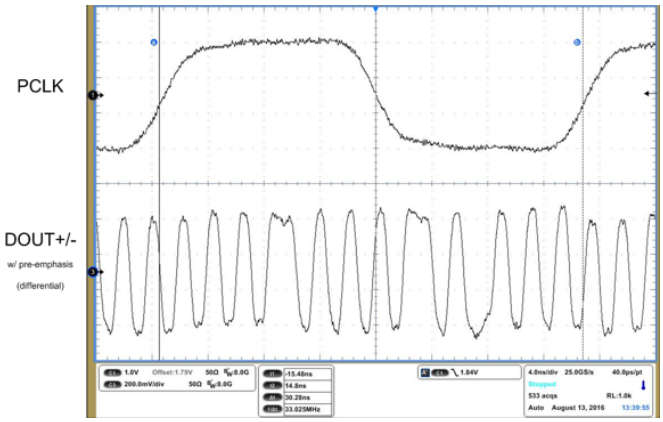


Figure 29. Input PCLK = 33 MHz and Associated DOUT Serial Stream With Pre-Emphasis

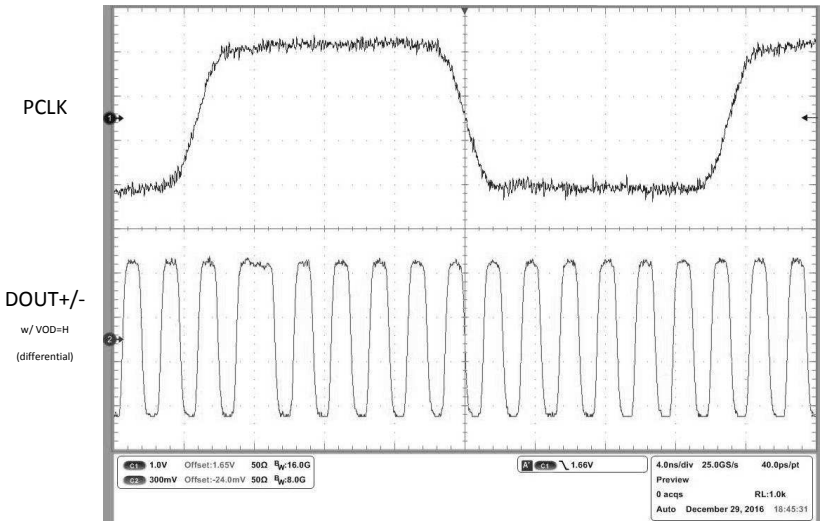


Figure 30. Input PCLK = 33 MHz and Associated DOUT Serial Stream With VODSEL = H

11 Power Supply Recommendations

An all CMOS design of the serializer and deserializer makes them inherently low power devices. Additionally, the constant current source nature of the LVDS outputs minimize the slope of the speed versus I_{CC} curve of CMOS designs.

12 Layout

12.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS SERDES devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power and ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors must include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Tantalum capacitors may be in the 2.2-µF to 10-µF range. Voltage rating of the tantalum capacitors must be at least 5 times the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range and smooth low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz range. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. *Pin Configuration and Functions* typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four layer board with a power and ground plane. Place LVCMOS (LVTTL) signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely-coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Termination of the LVDS interconnect is required. For point-to-point applications, termination must be placed at both ends of the devices. Nominal value is 100 Ω to match the line's differential impedance. Place the resistor as close to the transmitter DOUT± outputs and receiver RIN± inputs as possible to minimize the resulting stub between the termination resistor and device.

12.1.1 LVDS Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER© Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS/LVTTL signal
- Minimize the number of vias
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual available in PDF format from the TI web site at: www.ti.com/lvds.

12.2 Layout Example

Figure 31 shows the input LVCMOS traces and output high-speed, 100-Ω differential traces from the DS90C241 EVM.

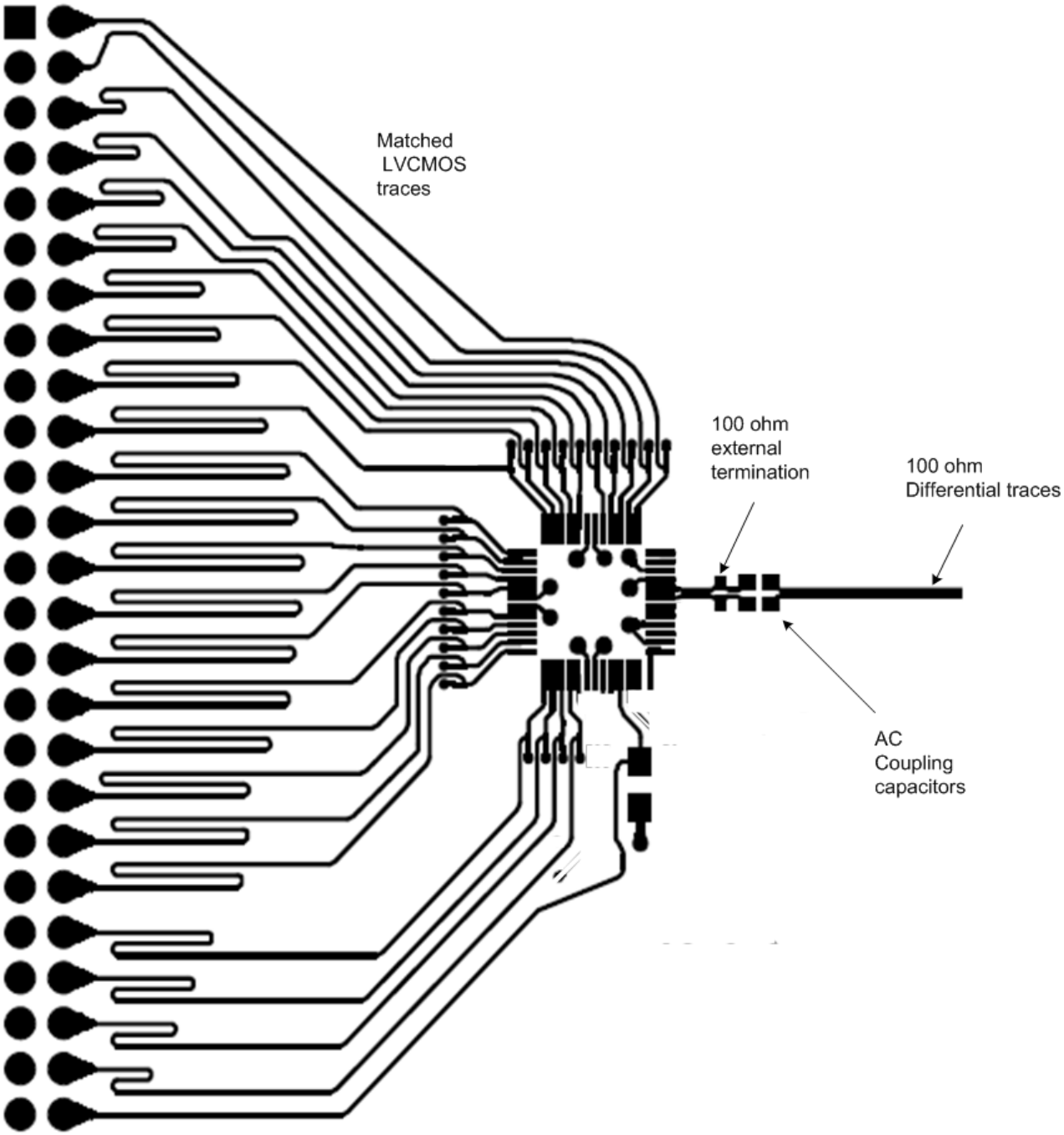


Figure 31. DS90C241 Layout Example from DS90C241 EVM

Layout Example (continued)

Figure 32 shows the input high-speed, 100-Ω differential traces and the output LVCMOS traces and from the DS90C124 EVM.

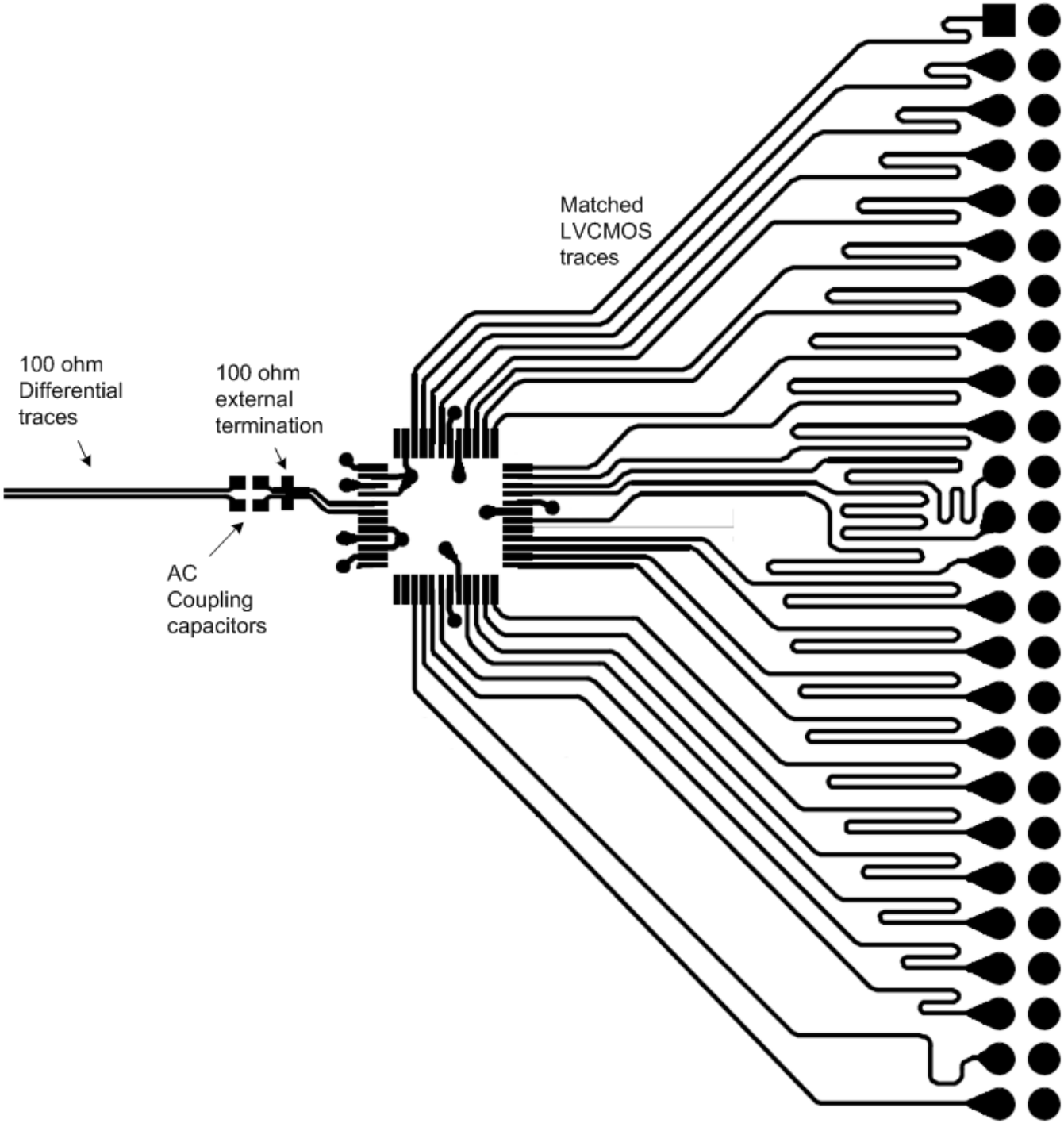


Figure 32. DS90C124 Layout Example from DS90C124 EVM

Layout Example (continued)

Figure 33 shows the power decoupling from the DS90C241 EVM.

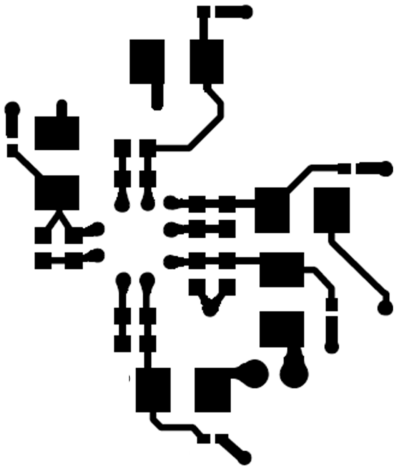


Figure 33. DS90C241 Example Layout of Power Decoupling from EVM

Figure 34 shows the power decoupling from the DS90C124 EVM.

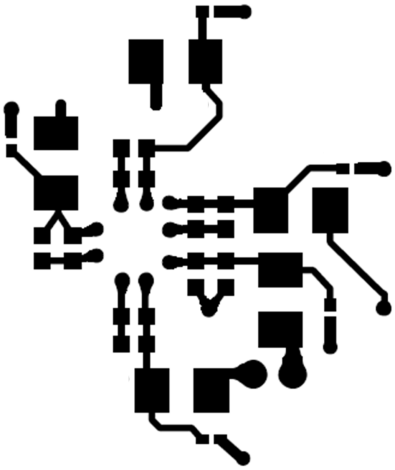


Figure 34. DS90C124 Example Layout of Power Decoupling from EVM

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

関連資料については、以下を参照してください。

- *『AN-1217 アイマスクを使用してBLVDS SER/DES信号の整合性を検証する方法』*(SNLA053)
- *『AN-1108 チャネル・リンクPCBと相互接続デザイン・インのガイドライン』*(SNLA008)
- *『AN-905 転送ラインRAPIDESIGNER©操作およびアプリケーション・ガイド』*(SNLA035)

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 3. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
DS90C124	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DS90C241	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** **エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。**

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.5 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.7 用語集

SLYZ022 — *TI用語集*.

この用語集には、用語や略語の一覧および定義が記載されています。

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C124IVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 IVS
DS90C124IVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 IVS
DS90C124IVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 IVS
DS90C124IVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 IVS
DS90C124IVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DS90C124QVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 QVS
DS90C124QVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 QVS
DS90C124QVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 QVS
DS90C124QVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C124 QVS
DS90C124QVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DS90C241IVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | EIAJ TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 IVS
DS90C241IVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | EIAJ TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 IVS
DS90C241IVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 IVS
DS90C241IVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 IVS
DS90C241IVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	
DS90C241QVS/NOPB	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 QVS
DS90C241QVS/NOPB.A	Active	Production	TQFP (PFB) | 48	250 | JEDEC TRAY (10+1)	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 QVS
DS90C241QVSX/NOPB	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 QVS

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C241QVSX/NOPB.A	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	DS90C241 QVS
DS90C241QVSX/NOPB.B	Active	Production	TQFP (PFB) | 48	1000 | LARGE T&R	-	Call TI	Call TI	-40 to 105	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF DS90C124, DS90C124-Q1, DS90C241, DS90C241-Q1 :

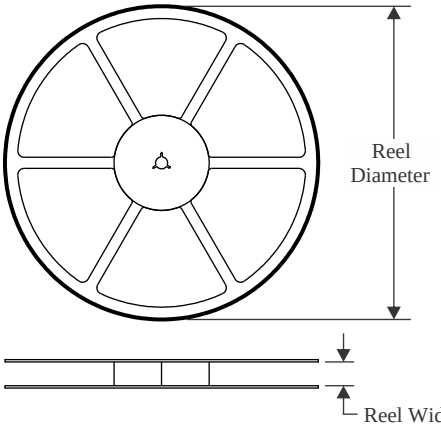
- Catalog : DS90C124, DS90C241
- Automotive : DS90C124-Q1, DS90C241-Q1

NOTE: Qualified Version Definitions:

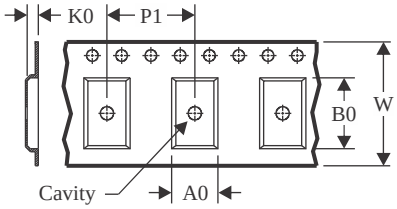
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

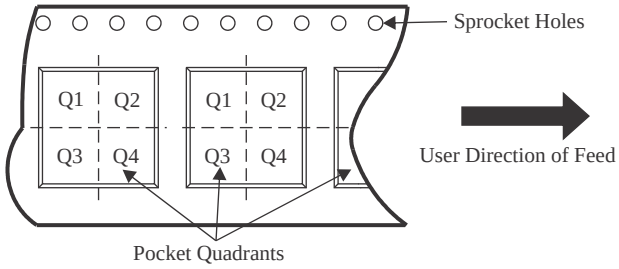


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

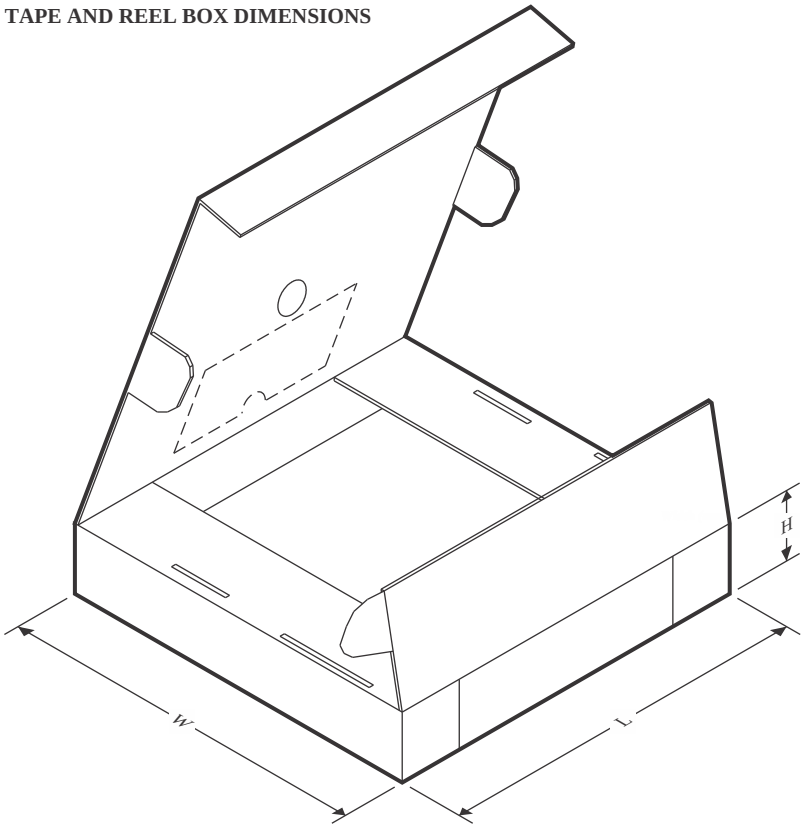
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C124IVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2
DS90C124QVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2
DS90C241IVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2
DS90C241QVSX/NOPB	TQFP	PFB	48	1000	330.0	16.4	9.8	9.8	2.0	12.0	16.0	Q2

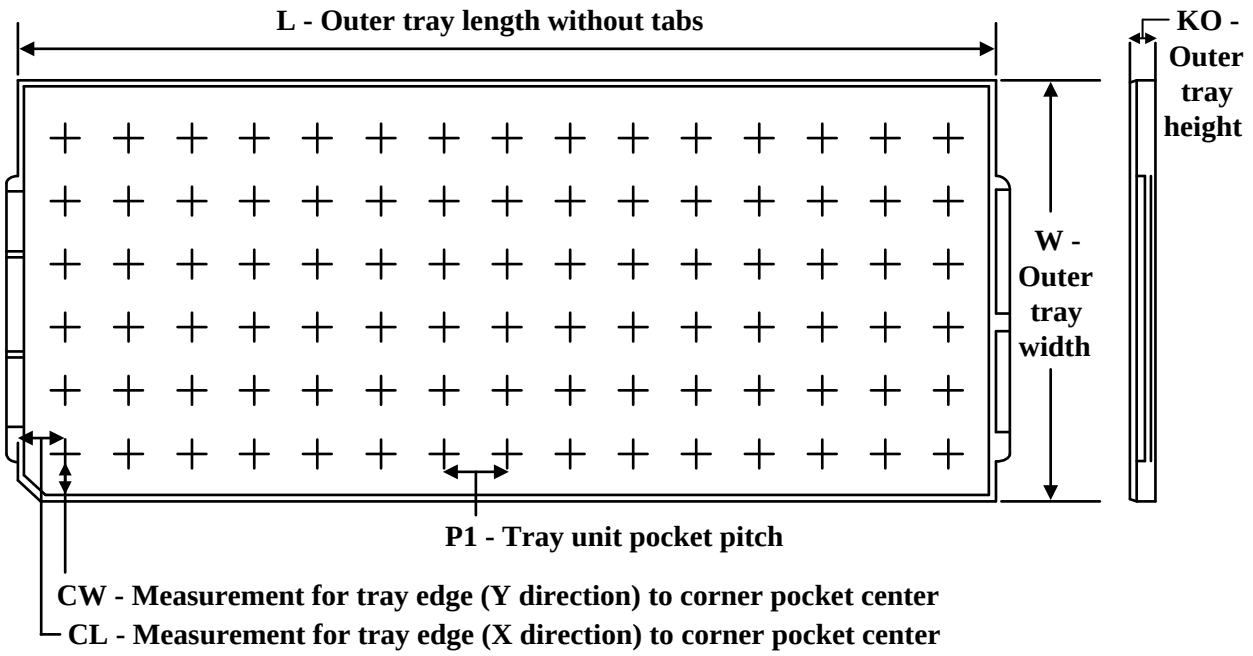
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C124IVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0
DS90C124QVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0
DS90C241IVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0
DS90C241QVSX/NOPB	TQFP	PFB	48	1000	356.0	356.0	36.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

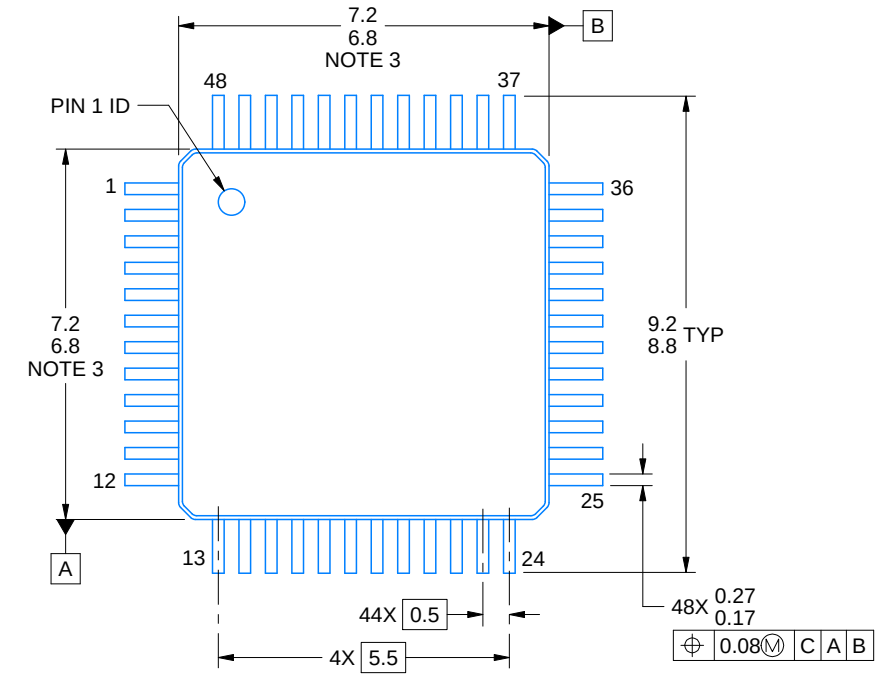
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS90C124IVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90C124IVS/NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90C124QVS/NOPB	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DS90C124QVS/NOPB.A	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

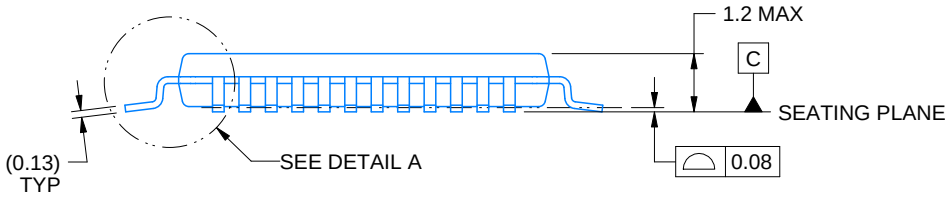
PACKAGE OUTLINE

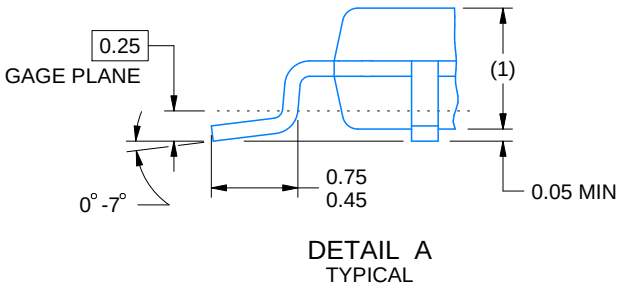
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK







DETAIL A
TYPICAL

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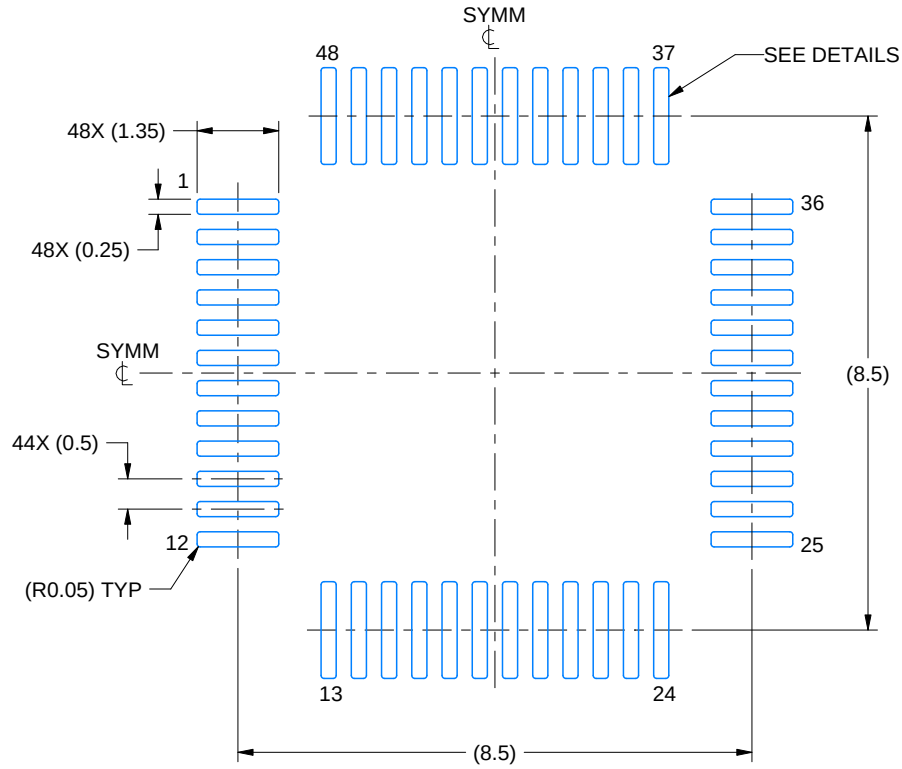
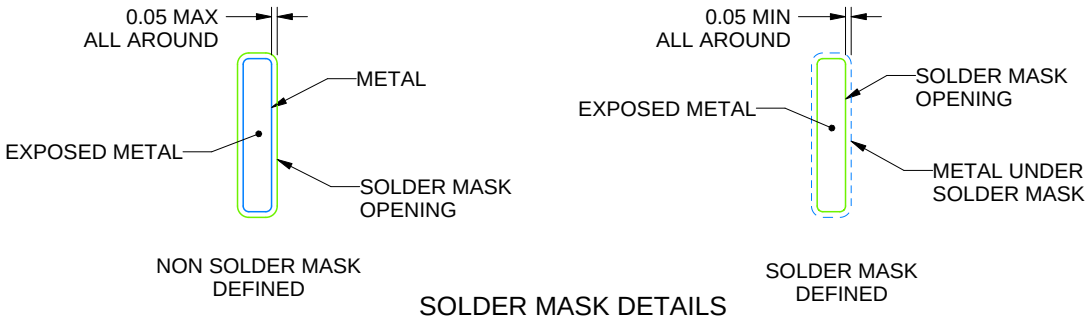
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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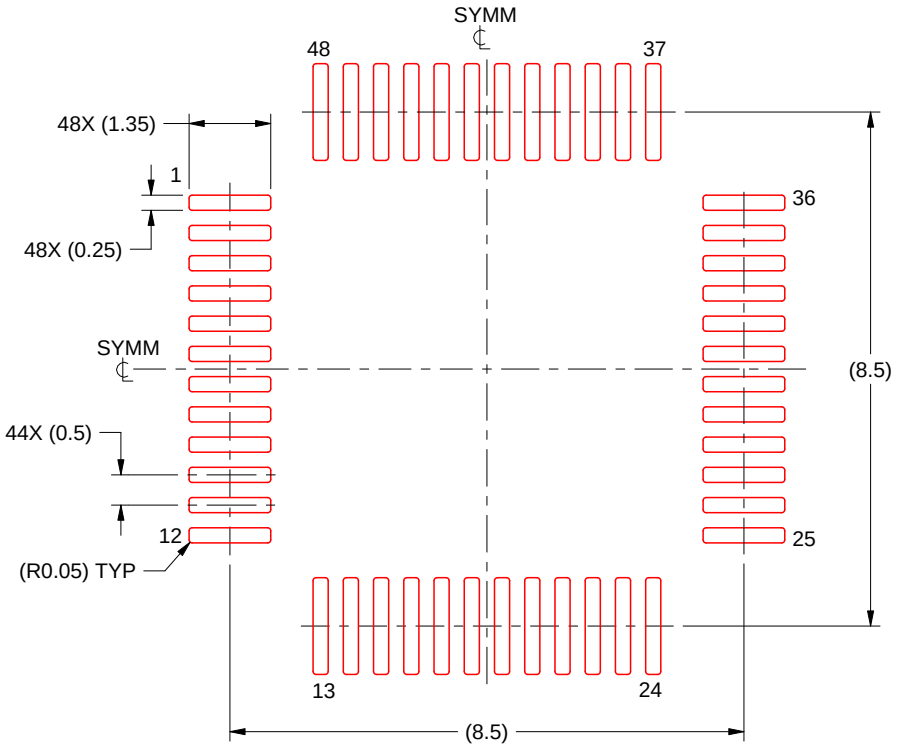
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月