DS90LV032A 3V LVDSクワッドCMOS差動ライン・レシーバ

1 特長

- 400Mbps (200MHz)を超えるスイッチング速度
- チャネル間スキュー: 0.1ns (標準値)
- 差動スキュー: 0.1ns (標準値)
- 最大伝搬遅延: 3.3ns
- 3.3V電源の設計
- パワーダウン時高インピーダンスのLVDS入力
- 低消費電力の設計(3.3V静的で40mW)
- 既存の 5V LVDSネットワークと相互運用可能
- 小スイング(標準値350mV) VIDに対応
- オープン、短絡、終端の入力フェイルセーフに対応
- ANSI/TIA/EIA-644と互換
- 工業用動作温度範囲: -40℃～85℃
- SOICおよびTSSOPパッケージで供給

2 アプリケーション

- ビルディング・オートメーションとファクトリ・オートメーション
- グリッド・インフラストラクチャ

3 概要

DS90LV032Aは、クワッドCMOS差動ライン・レシーバで、非常に低い消費電力と高いデータ速度を必要とするアプリケーション用に設計されています。このデバイスは、低電圧差動信号(LVDS)テクノロジを活用し、400Mbps (200MHz)を超えるデータ転送速度をサポートするよう設計されています。

DS90LV032Aは低電圧(標準値350mV)の差動入力信号を受け付け、3V CMOS出力レベルへ変換します。レシーバはTRI-STATE機能をサポートしており、出力の多重化に使用できます。また、レシーバはオープン、短絡、終端(100Ω)の入力フェイルセーフもサポートします。すべてのフェイルセーフ条件において、レシーバの出力はHIGHになります。

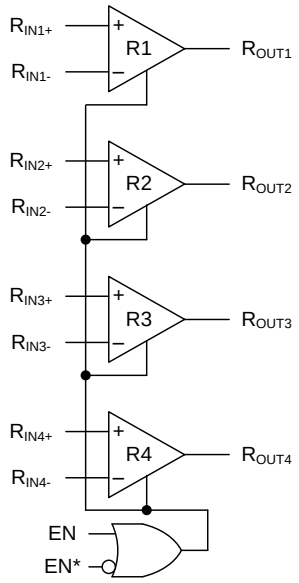
DS90LV032Aおよびコンパニオン LVDSライン・ドライバ(例: DS90LV031A)は、大電力のPECL/ECLデバイスの新しい代替品として、高速のポイント・ツー・ポイント・インターフェイス・アプリケーションに使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DS90LV032A	SOIC (16)	9.90mm×3.91mm
	TSSOP (16)	5.00mm×4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (April 2013) から **Revision D** に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Added *Thermal Information* table. ... 4

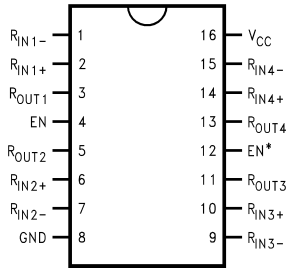
Revision B (April 2013) から **Revision C** に変更 **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 7

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5 Pin Configuration and Functions

D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Active high enable pin, OR-ed with $\overline{EN}$
$\overline{EN}$	12	I	Active low enable pin, OR-ed with EN
GND	8	—	Ground pin
R_{IN-}	1, 7, 9, 15	I	Inverting receiver input pin
R_{IN+}	2, 6, 10, 14	I	Noninverting receiver input pin
R_{OUT}	3, 5, 11, 13	O	Receiver output pin
V_{CC}	16	—	Power supply pin, 3.3 V ± 0.3 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC}	–0.3	4	V
Input voltage	R_{IN+}, R_{IN-}	–0.3	3.9	V
Enable input voltage	EN, EN*	–0.3	V_{CC} + 0.3	V
Output voltage	R_{OUT}	–0.3	V_{CC} + 0.3	V
Lead temperature, soldering (4 s)			260	°C
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge[1]	Human-body model (HBM)[1]	±4500	V
		Machine model (MM), EIAJ	±250	

(1) ESD Ratings: HBM (1.5 kΩ, 100 pF) ≥ 4.5 kV and EIAJ (0 Ω, 200 pF) ≥ 250 V

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
	Receiver input voltage	GND		3	V
T_A	Operating free-air temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC[1]		DS90LV032A		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	75	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47	36	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55	32	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	31.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics

over supply voltage and operating temperature ranges (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{TH}	Differential input high threshold	V_{CM} = 1.2 V, R_{IN+}, R_{IN-} pin(2)			20	100	mV
V_{TL}	Differential input low threshold			–100	–20		mV
VCMR	Common mode voltage range	VID = 200 mV peak to peak, R_{IN+}, R_{IN-} pin(3)		0.1		2.3	V
I_{IN}	Input current	V_{CC} = 3.6 V or 0 V, R_{IN+}, R_{IN-} pin	V_{IN} = 2.8 V	–10	±1	10	µA
			V_{IN} = 0 V	–10	±1	10	µA
		V_{CC} = 0 V, V_{IN} = 3.6 V, R_{IN+}, R_{IN-} pin		–20		20	µA
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{ID} = 200 mV, R_{OUT} pin		2.7	3		V
		I_{OH} = –0.4 mA, input terminated, R_{OUT} pin		2.7	3		V
		I_{OH} = –0.4 mA, input shorted, R_{OUT} pin		2.7	3		V
V_{OL}	Output low voltage	I_{OL} = 2 mA, V_{ID} = –200 mV, R_{OUT} pin			0.1	0.25	V
I_{OS}	Output short-circuit current	Enabled, V_{OUT} = 0 V, R_{OUT} pin(4)		–15	–48	–120	mA
I_{OZ}	Output TRI-STATE current	Disabled, V_{OUT} = 0 V or V_{CC}		–10	±1	10	µA
V_{IH}	Input high voltage	EN, EN* pins		2		V_{CC}	V
V_{IL}	Input low voltage	EN, EN* pins		GND		0.8	V
I_I	Input current	V_{IN} = 0 V or V_{CC}, other input = V_{CC} or GND, EN, EN* pins		–10	±1	10	µA
V_{CL}	Input clamp voltage	I_{CL} = –18 mA, EN, EN* pins		–1.5	–0.8		V
I_{CC}	No load supply current	EN, EN* = V_{CC} or GND, inputs open, V_{CC} pin			10	15	mA
	Receivers enabled	EN, EN* = 2.4 V or 0.5 V, inputs open, V_{CC} pin			10	15	mA
I_{CCZ}	No load supply current	Receivers disabled, EN = GND, EN* = V_{CC}, inputs open, V_{CC} pin			3	5	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) V_{CC} is always higher than R_{IN+} and R_{IN-} voltage. R_{IN-} and R_{IN+} are allowed to have a voltage range –0.2 V to V_{CC} – VID / 2. However, to be compliant with AC specifications, the common voltage range is 0.1 V to 2.3 V
(3) The VCMR range is reduced for larger VID. Example: if VID = 400 mV, the VCMR is 0.2 V to 2.2 V. The fail-safe condition with inputs shorted is valid over a common mode range of 0 V to 2.3 V. A VID up to V_{CC} – 0 V may be applied to the R_{IN+}/ R_{IN-} inputs with the common mode voltage set to V_{CC} / 2. Propagation delay and differential pulse skew decrease when VID is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ VID ≤ 800 mV over the common mode range.
(4) Output short-circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output must be shorted at a time, do not exceed maximum junction temperature specification.

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6.6 Switching Characteristics

over supply voltage and operating temperature ranges (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{PHLD}	Differential propagation delay, high to low	C_L = 10 pF	1.8		3.3	ns
t_{PLHD}	Differential propagation delay, low to high	V_{ID} = 200 mV	1.8		3.3	ns
t_{SKD1}	Differential pulse skew(3) $\lvert t_{PHLD} - t_{PLHD} \rvert$	See Figure 4 and Figure 5	0	0.1	0.35	ns
t_{SKD2}	Differential channel-to-channel skew(4)	Same device	0	0.1	0.5	ns
t_{SKD3}	Differential part-to-part skew(5)				1	ns
t_{SKD4}	Differential part-to-part skew(6)				1.5	ns
t_{TLH}	Rise time			0.35	1.2	ns
t_{THL}	Fall time			0.35	1.2	ns
t_{PHZ}	Disable time high to Z	R_L = 2 kΩ		8	12	ns
t_{PLZ}	Disable time low to Z	C_L = 10 pF		6	12	ns
t_{PZH}	Enable time Z to high	See Figure 6 and Figure 7		11	17	ns
t_{PZL}	Enable time Z to low			11	17	ns
f_{MAX}	Maximum operating frequency(7)	All channels switching	200	250		MHz

(1) All typicals are given for: V_{CC} = 3.3 V, T_A = 25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r and t_f (0% to 100%) ≤ 3 ns for R_{IN}.
(3) t_{SKD1} is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel
(4) t_{SKD2}, channel-to-channel skew, is defined as the difference between the propagation delay of one channel and that of the others on the same chip with any event on the inputs.
(5) t_{SKD3}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same V_{CC}, and within 5°C of each other within the operating temperature range.
(6) t_{SKD4}, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Maximum – Minimum| differential propagation delay.
(7) f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, differential (1.05-V to 1.35-V peak-to-peak). Output criteria: 60% / 40% duty cycle, V_{OL} (maximum: 0.4 V), V_{OH} (minimum: 2.7 V), load = 10 pF (stray plus probes).

6.7 Dissipation Ratings

	MAXIMUM PACKAGE POWER DISSIPATION AT 25°C
D package	1025 mW
PW package	866 mW
Derate D package	8.2 mW/°C above 25°C
Derate PW package	6.9 mW/°C above 25°C

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6.8 Typical Characteristics

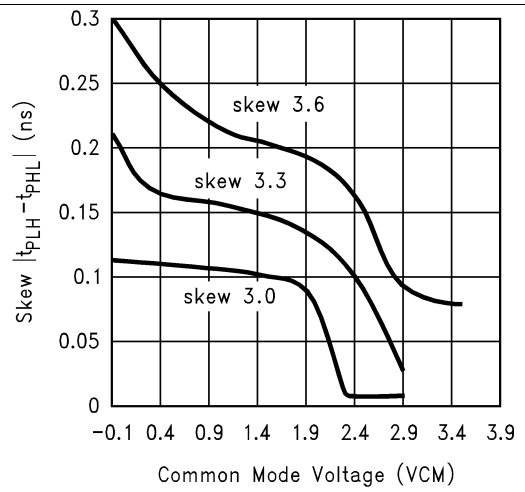


Figure 1. Typical Pulse Skew Variation vs Common Mode Voltage

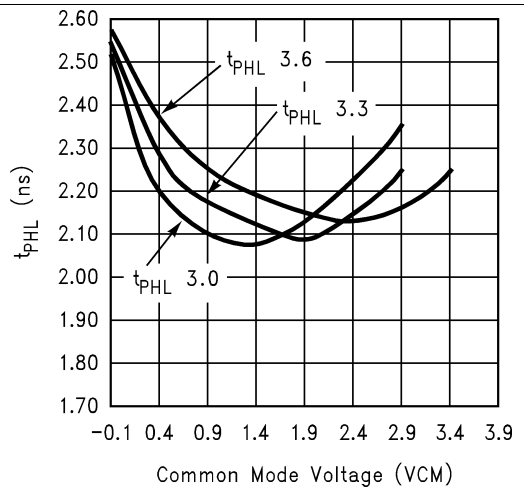


Figure 2. Variation in High-to-Low Propagation Delay vs VCM

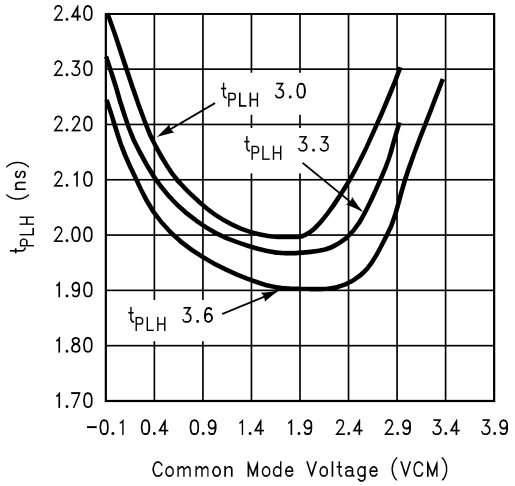


Figure 3. Variation in Low-to-High Propagation Delay vs VCM

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7 Parameter Measurement Information

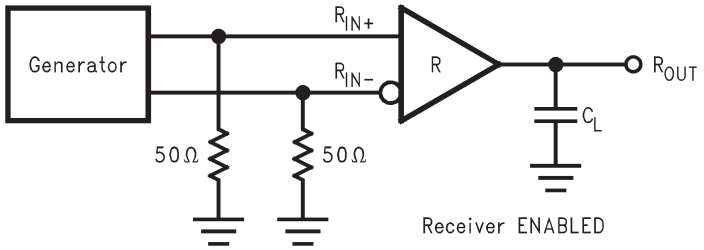


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

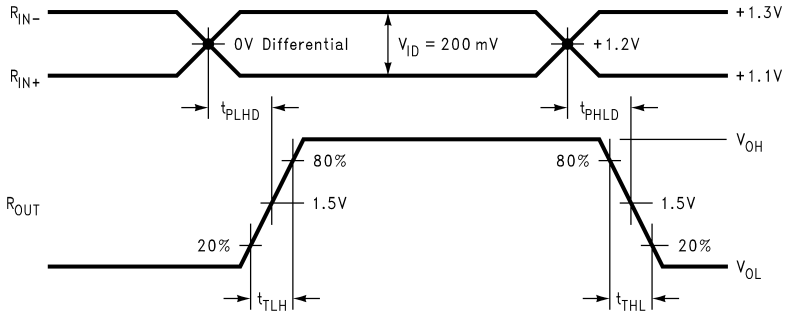
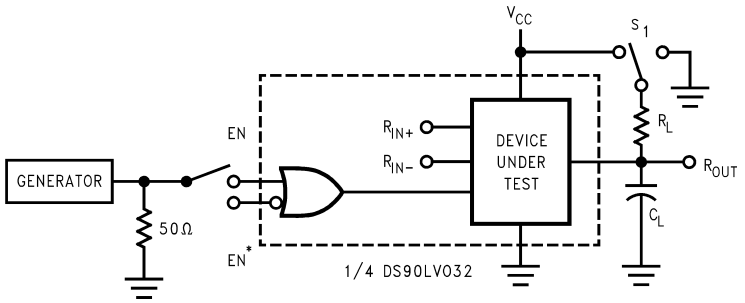


Figure 5. Receiver Propagation Delay and Transition Time Waveforms



C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

Figure 6. Receiver TRI-STATE Delay Test Circuit

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Parameter Measurement Information (continued)

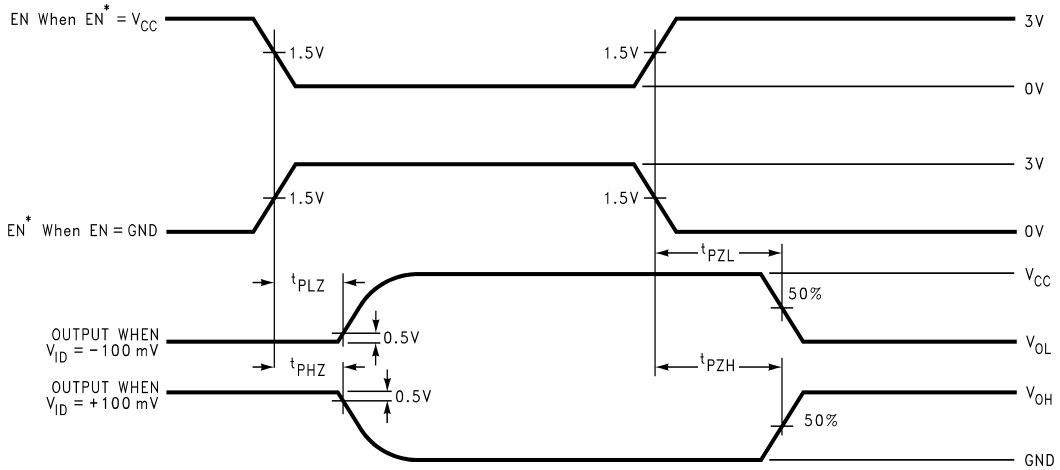


Figure 7. Receiver TRI-STATE Delay Waveforms

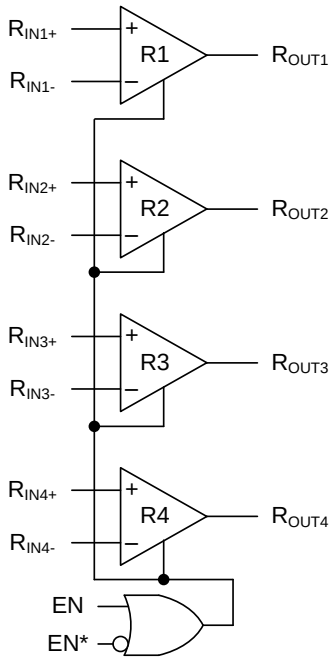
8 Detailed Description

8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 8. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media) is located as close to the receiver input pins as possible. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be considered.

The DS90LV032A differential line receiver is capable of detecting signals as low as 100 mV, over a ±1-V common-mode range centered around 1.2 V. This is related to the driver offset voltage which is typically 1.2 V. The driven signal is centered around this voltage and may shift ±1 V around this center point. The ±1-V shifting may be the result of a ground potential difference between the ground reference of the driver and the ground reference of the receiver, the common-mode effects of coupled noise, or a combination of the two. The AC parameters of both receiver input pins are optimized for a recommended operating input voltage range of 0 V to 2.4 V (measured from each pin to ground). The device operates for receiver input voltages up to VCC, but exceeding VCC turns on the ESD protection circuitry which clamps the bus voltages.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Fail-Safe Feature

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

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Feature Description (continued)

1. *Open input pins*: The DS90LV032A is a quad receiver device, and if an application requires only 1, 2, or 3 receivers, the unused channel(s) inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pullup and pulldown resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
2. *Terminated input*: If the driver is disconnected (cable unplugged), or if the driver is in a TRI-STATE or power-off condition, the receiver output is in a HIGH state, even with the end of cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect must be used. Twisted pair cable offers better balance than flat ribbon cable.
3. *Shorted inputs*: If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors must be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point must be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

The footprint of the DS90LV032A is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

8.4 Device Functional Modes

Table 1 lists the functional modes of the DS90LV032A.

Table 1. Truth Table

ENABLES		INPUTS	OUTPUT
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1$ V	H
		$V_{ID} \leq -0.1$ V	L
		Full Fail-safe OPEN/SHORT or Terminated	H

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90LV032A LVDS receiver and DS90LV031A driver are intended to be primarily used in an uncomplicated point-to-point configuration as shown in Figure 8. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100 Ω.

9.1.1 Probing LVDS Transmission Lines

Always use high impedance (>100 kΩ), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.1.2 Cables and Connectors, General Comments

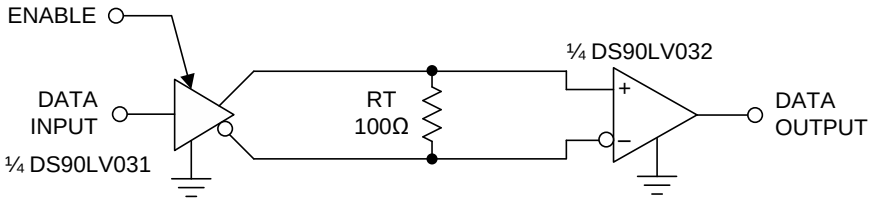
When choosing cable and connectors for LVDS it is important to remember:

- Use controlled impedance media.

  The cables and connectors you use must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities.
- Balanced cables (that is, twisted pair) are usually better than unbalanced cables (such as ribbon cable or simple coax) for noise reduction and signal quality.

  Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the receiver. For cable distances <0.5 m, most cables can be made to work effectively. For distances 0.5 m ≤ d ≤ 10 m, Category 3 (CAT 3) twisted pair cable works well, is readily available, and relatively inexpensive.

9.2 Typical Application



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Figure 8. Balanced System Point-to-Point Application

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media must have a matched differential impedance of about 100 Ω. They must not introduce major impedance discontinuities. Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 m, most cables work effectively. For distances 0.5 m ≤ d ≤ 10 m, Category 5 (CAT5) twisted pair cable works well, is readily available, and relatively inexpensive.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (>100 kΩ), low capacitance (<2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.2.3 Application Curves

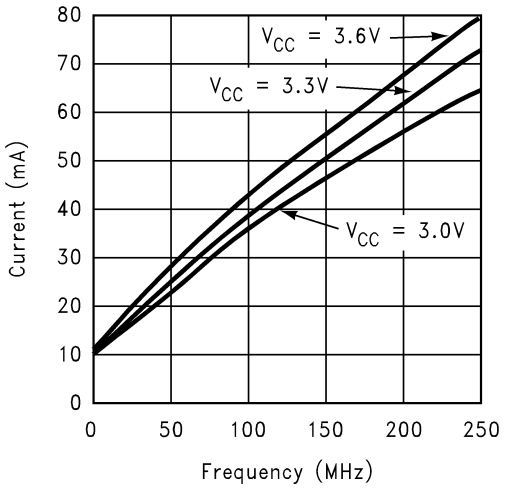


Figure 9. ICC vs Frequency, Four Channels Switching

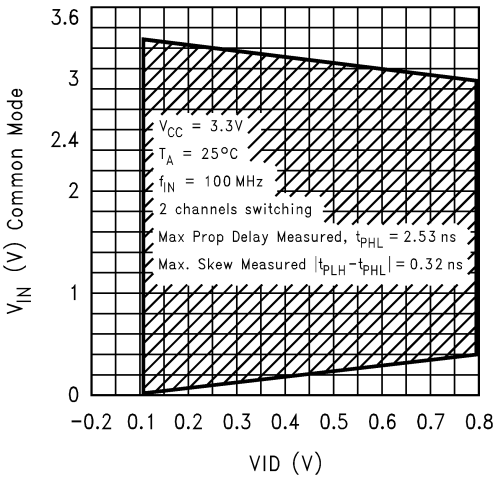


Figure 10. Typical Common Mode Range Variation With Respect to Amplitude of Differential Input

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10 Power Supply Recommendations

Although the DS90LV032A draws very little power, there is a dynamic current component which increases the overall power consumption at higher switching frequencies. The DS90LV032A power supply connection must take this additional current consumption into consideration for maximum power requirements.

11 Layout

11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom): LVDS signals, ground, power, and TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by power or ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. High-frequency ceramic (surface-mount recommended) 0.1-µF in parallel with 0.01-µF, in parallel with 0.001-µF at the power supply pin as well as scattered capacitors over the printed-circuit board. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF, 35-V (or greater) solid tantalum capacitor must be connected at the power entry point on the printed-circuit board.

11.1.2 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be <10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. Lab experiments show that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart because magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and results in EMI. Note the velocity of propagation, v = c/Er where c (the speed of light) = 0.2997 mm/ps or 0.0118 in/ps. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number of vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces must be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.3 Termination

Use a resistor which best matches the differential impedance of your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS does not work without resistor termination. Typically, connect a single resistor across the pair at the receiver end.

Surface-mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver must be <10 mm (12 mm maximum).

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11.2 Layout Example

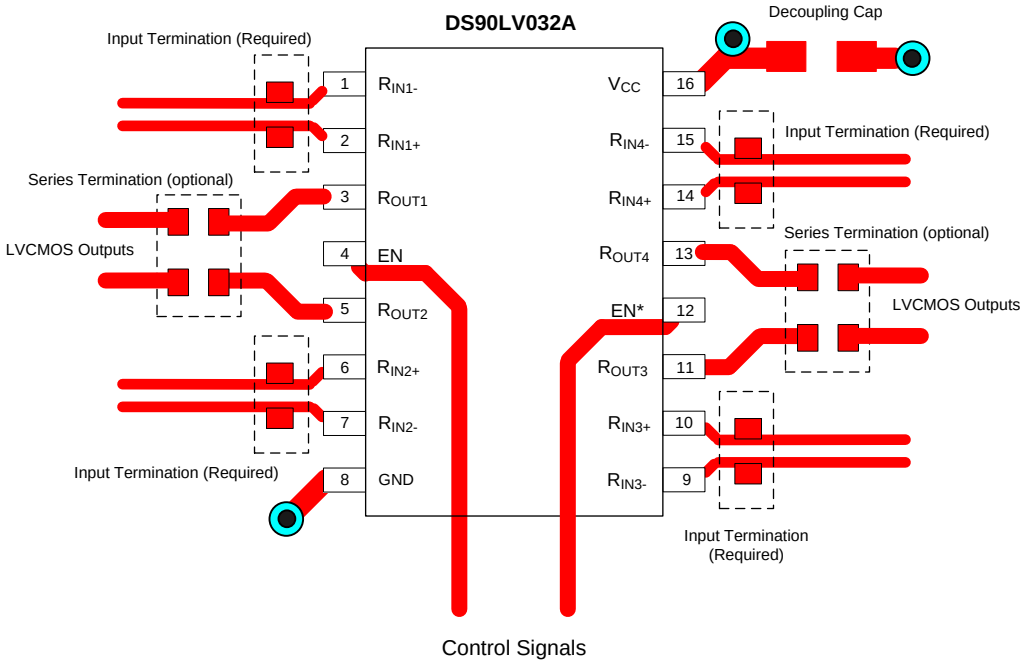


Figure 11. DS90LV032A Layout Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

一般的なアプリケーションのガイドラインと、LVDSドライバおよびレシーバ用のヒントについては、以下のアプリケーション・ノートを参照してください。

- *『LVDSオーナー・マニュアル』*
- *『AN-808、長い伝送ラインとデータ信号の品質』* (SNLA028)
- *『AN-977、LVDS信号の品質: アイ・パターンを使用したジッタ測定のテスト・レポート #1』*(SNLA166)
- *『AN-971、LVDSテクノロジの概要』* (SNLA165)
- *『AN-916、ケーブル選択の実践的ガイド』*(SNLA219)
- *『AN-805、差動ライン・ドライバの消費電力の計算』* (SNOA233)
- *『AN-903、差動終端技法の比較』* (SNLA034)
- *『AN-1035、LVDSテクノロジ用のPCB設計ガイドライン』*(SNOA355)

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90LV032ATM/NOPB	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV032A TM
DS90LV032ATM/NOPB.B	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV032A TM
DS90LV032ATMTC/NOPB	Active	Production	TSSOP (PW) | 16	92 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 032AT
DS90LV032ATMTCX/NOPB	Active	Production	TSSOP (PW) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV 032AT
DS90LV032ATMX/NOPB	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV032A TM
DS90LV032ATMX/NOPB.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90LV032A TM

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

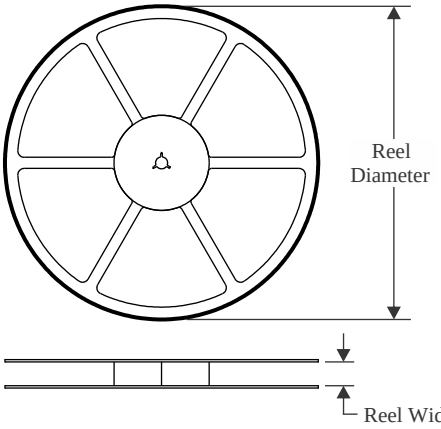
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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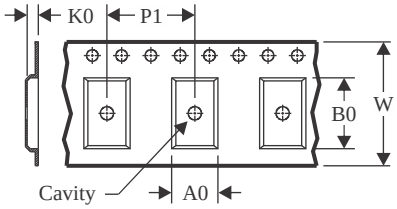
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

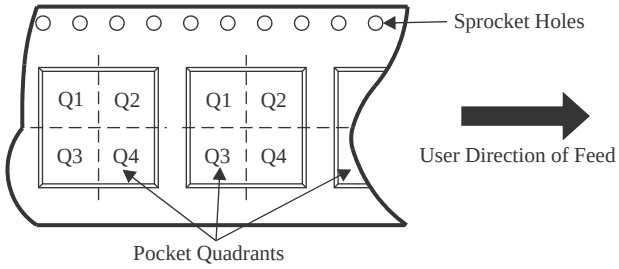


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

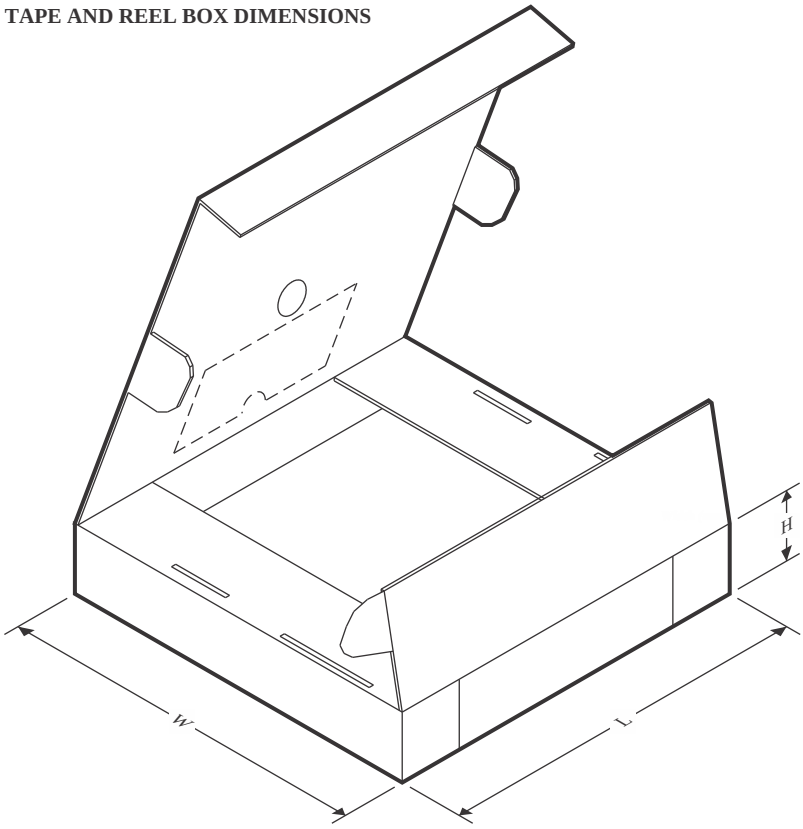
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV032ATMTCX/ NOPB	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DS90LV032ATMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

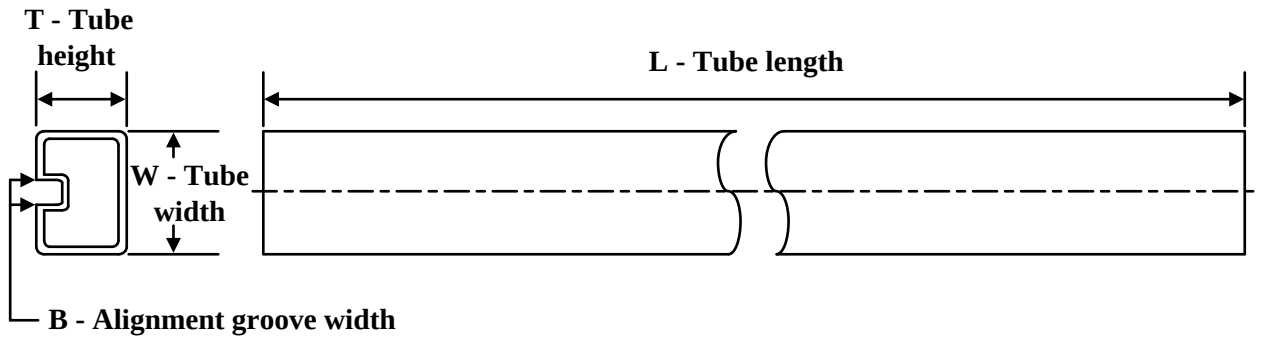
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV032ATMTCX/ NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0
DS90LV032ATMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

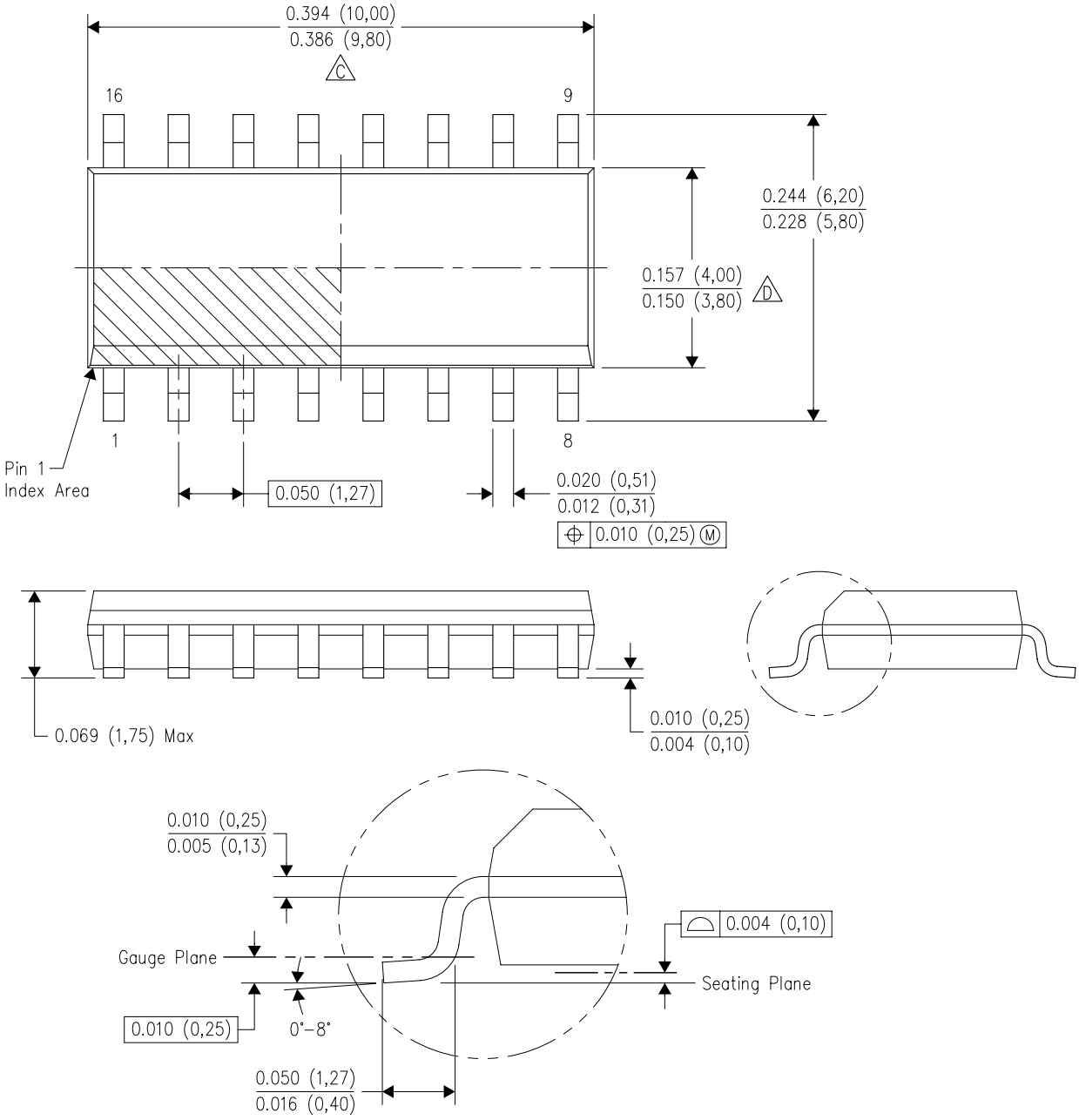
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90LV032ATM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DS90LV032ATM/NOPB.B	D	SOIC	16	48	495	8	4064	3.05
DS90LV032ATMTC/NOPB	PW	TSSOP	16	92	495	8	2514.6	4.06

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



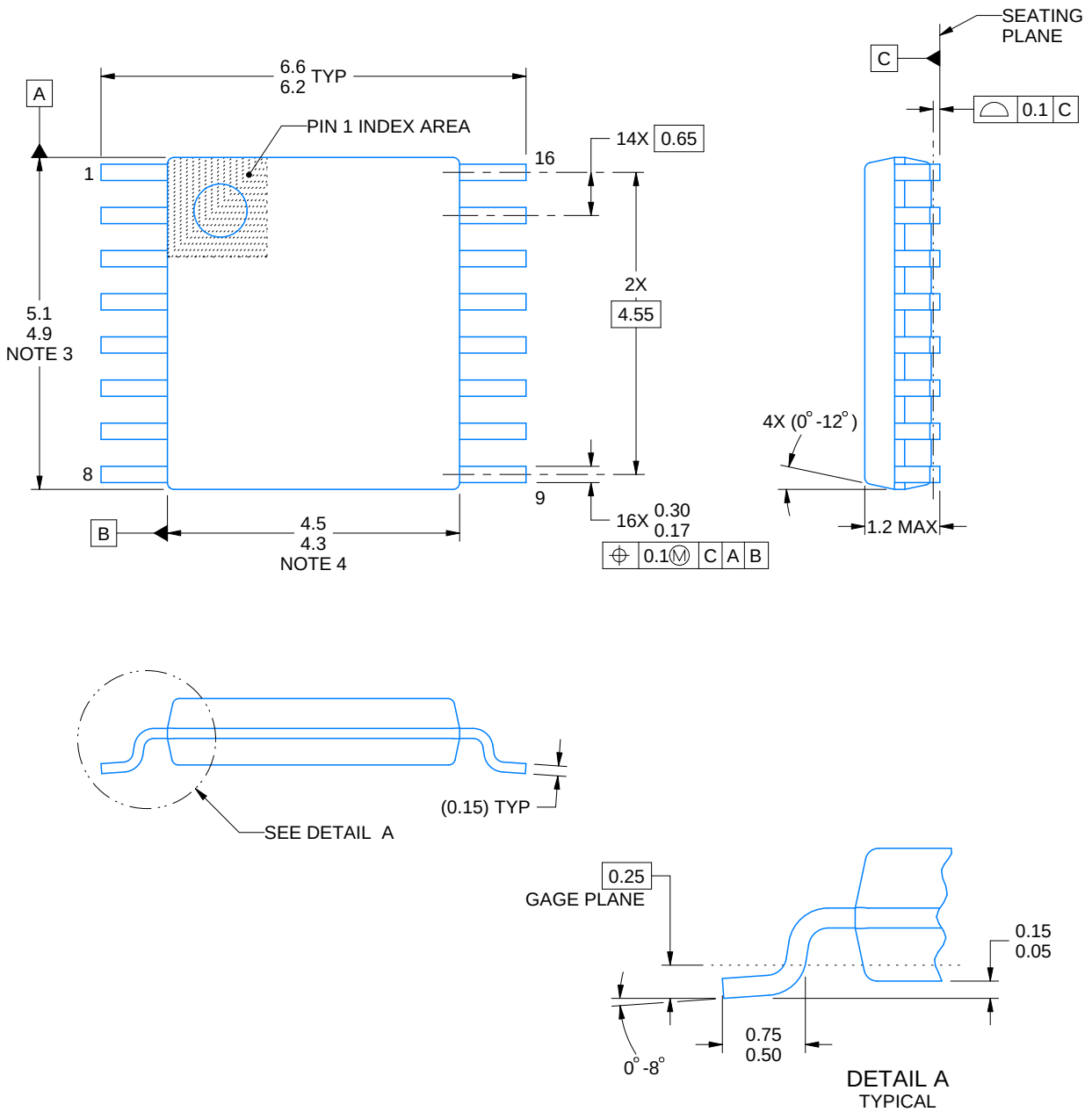
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

PACKAGE OUTLINE

PW0016A

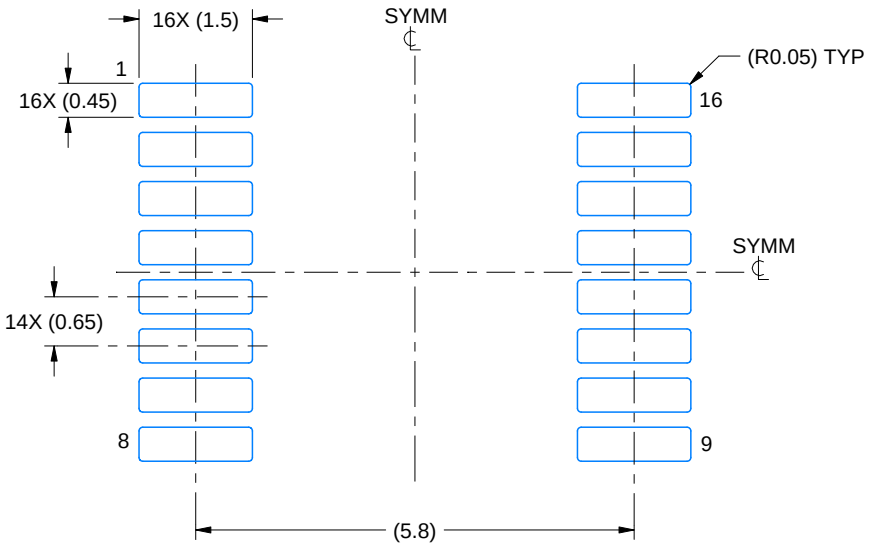
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

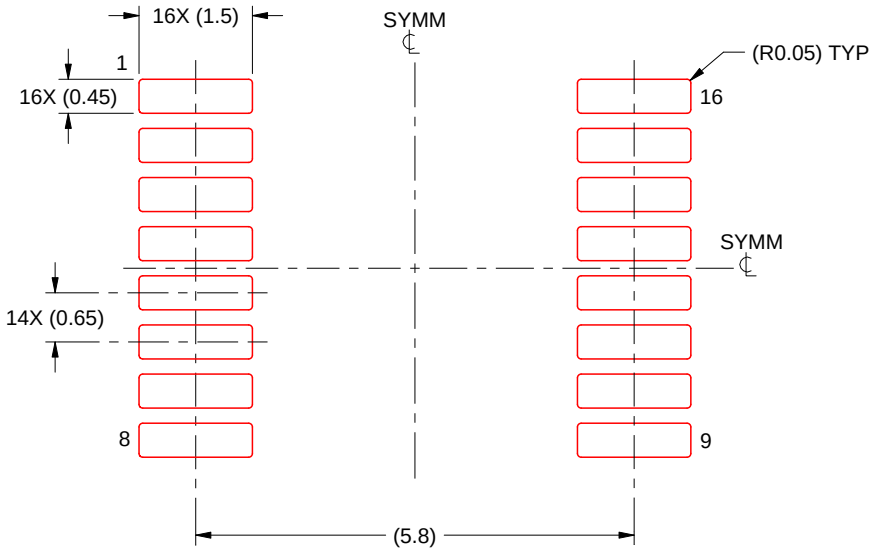


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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