TEXAS INSTRUMENTS
DS90UH940N-Q1
JAJSFP8A – JULY 2018 – REVISED OCTOBER 2018

DS90UH940N-Q1 HDCP搭載、1080p FPD-Link IIIからCSI-2へのデシリアライザ

1 特長

- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード2: 動作時周囲温度–40℃～+105℃
- WUXGA (1920×1200)および1080p60解像度と24ビットの色深度に対応する、最高170MHzのピクセル・クロック周波数をサポート
- 歪み補正機能を搭載した1レーンまたは2レーンのFPD-Link IIIインターフェイス
- MIPI® D-PHY/CSI-2トランスミッタ
  - 2または4レーンでの動作を選択可能で、各レーンが最高1.3GbpsのCSI-2出力ポート
  - ビデオ・フォーマット: RGB888/666/565、YUV422/420、RAW8/10/12
  - 仮想チャネル識別子をプログラム可能
- HDCP暗号エンジンを内蔵し、キーをオンチップに保存
- 4つの高速GPIO (それぞれ最高2Mbps)
- 適応型受信イコライゼーション
  - 1.7GHzにおいて、最高-15.3dBのチャネル挿入損失を補償
  - 温度およびケーブル劣化を自動的に補償
- 最高3.3MbpsのSPI制御インターフェイス
- 1MbpsのFast-Mode Plus対応のI2C (マスタ/スレーブ)
- 7.1のマルチI2S (4データ)チャネルをサポート

2 アプリケーション

- 車載インフォテインメント
  - 集中情報ディスプレイ
  - リアシート・エンターテインメント・システム
  - デジタル計器クラスタ

3 概要

DS90UH940N-Q1はFPD-Link IIIデシリアライザで、DS90UH949/947/929-Q1シリアライザと組み合わせることで、1レーンまたは2レーンのFPD-Link IIIストリームをMIPI® CSI-2フォーマットに変換します。このデシリアライザは、コスト効率の優れた50Ωのシングルエンド同軸、または100Ωの差動シールド付きツイストペア(STP)ケーブル上で動作できます。1つまたは2つのFPD-Link IIIシリアル・ストリームからデータを回復し、カメラ・シリアル・インターフェイス(CSI-2)フォーマットに変換して、最高でWUXGAまたは1080p60で24ビットのカラー深度までのビデオ解像度に対応できます。

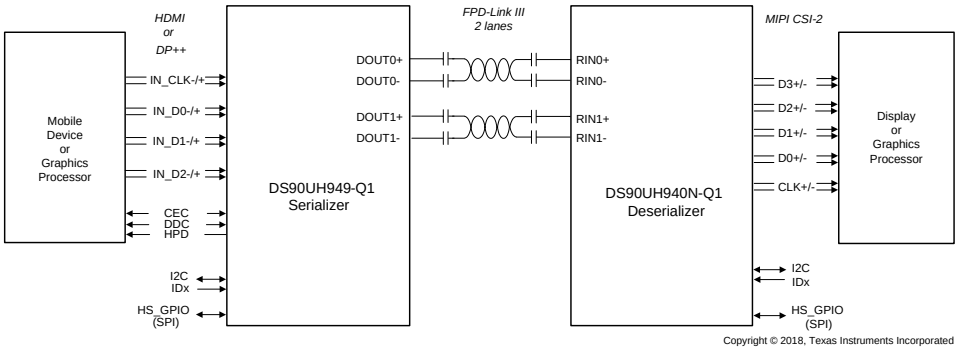
FPD-Link III インターフェイスはビデオおよびオーディオ・データの伝送のほか、I2CやSPI通信などの全二重制御機能を同じ差動リンク上でサポートします。ビデオ・データと制御を2つの差動ペアに統合することで、相互接続のサイズと重量が減少し、システムの設計が簡素化されます。低電圧の差動信号、データのスクランブル処理、およびランダム化を使用することで、EMIが最小限に抑えられます。下位互換モードでは、このデバイスは単一の差動リンク上で、最大WXGAまたは720pの解像度と24ビットのカラー深度に対応できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
DS90UH940N-Q1	WQFN (64)	9.00mm×9.00mm

(1) 提供されているすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



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4 改訂履歴

2018年7月発行のものから更新 **Page**

- デバイスのステータスを「事前情報」から「量産データ」に変更 ... 1

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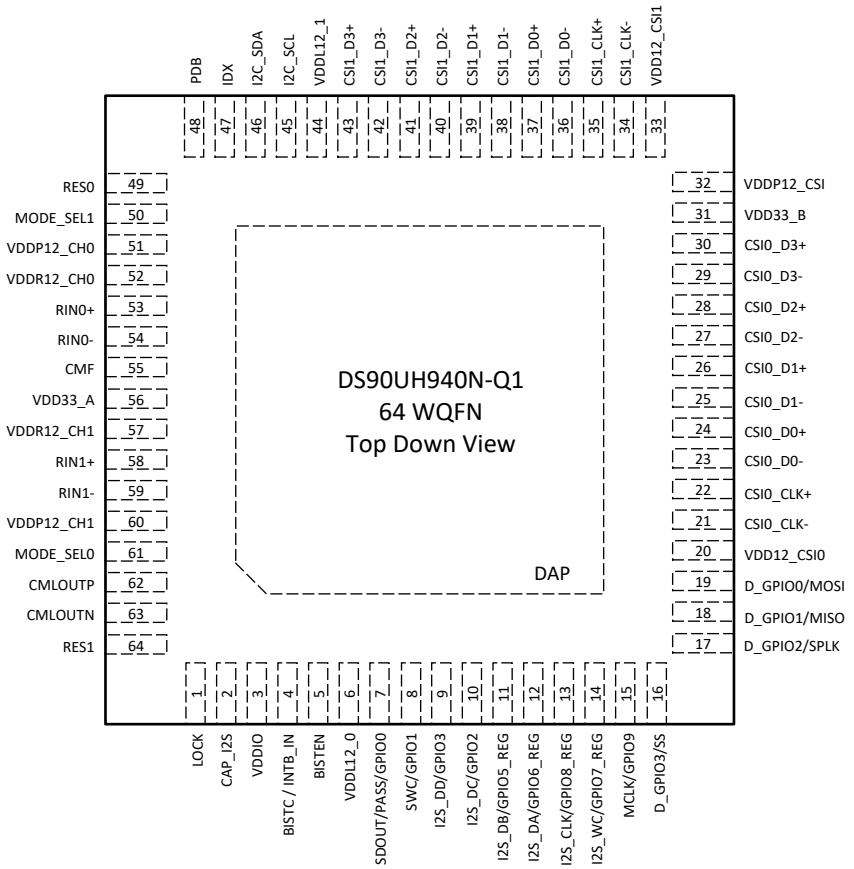
5 概要（続き）

このデバイスはFPD-Link IIIチャネルを自動的に検出し、特別なトレーニング・パターンを必要とせずに、クロック同期および歪み補正機能を提供します。これによって、PCB配線、ケーブルのペア間の長さ相違、コネクタの不均衡など、相互接続配線の不一致に起因する位相歪みに対する許容性が保証されます。

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6 Pin Configuration and Functions

NKD Package
64-Pin WQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
MIPI DPHY / CSI-2 OUTPUT PINS			
CSI0_CLK– CSI0_CLK+	21 22	O	CSI-2 TX Port 0 differential clock output pins. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
CSI0_D0– CSI0_D0+	23 24	O	CSI-2 TX Port 0 differential data output pins. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
CSI0_D1– CSI0_D1+	25 26	O	
CSI0_D2– CSI0_D2+	27 28	O	
CSI0_D3– CSI0_D3+	29 30	O	

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
CSI1_CLK– CSI1_CLK+	34 35	O	CSI-2 TX Port 1 differential clock output pins. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
CSI1_D0– CSI1_D0+	36 37	O	CSI-2 TX Port 1 differential data output pins. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
CSI1_D1– CSI1_D1+	38 39	O	
CSI1_D2– CSI1_D2+	40 41	O	
CSI1_D3– CSI1_D3+	42 43	O	
FPD-LINK III INTERFACE			
RIN0–	54	I/O	FPD-Link III RX Port 0 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see 図 41 and 図 42). It must be AC-coupled per 表 113. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
RIN0+	53	I/O	
RIN1–	59	I/O	FPD-Link III RX Port 1 pins. The port receives FPD-Link III high-speed forward channel video and control data and transmits back channel control data. It can interface with a compatible FPD-Link III serializer TX through a STP or coaxial cable (see 図 41 and 図 42). It must be AC-coupled per 表 113. Leave unused pins as No Connect. Do not connect to an external pullup or pulldown.
RIN1+	58	I/O	
CMF	55	I/O	Common mode filter – connect 0.1-µF capacitor to GND
I2C PINS			
I2C_SDA	46	I/O, OD	I2C Data Input / Output Interface pin. See *Serial Control Bus*. Recommend a 2.2 kΩ to 4.7 kΩ pullup to 1.8 V or 3.3 V. See *I2C Bus Pullup Resistor Calculation* (SLVA689).
I2C_SCL	45	I/O, OD	I2C Cock Input / Output Interface pin. See *Serial Control Bus*. Recommend a 2.2 kΩ to 4.7 kΩ pullup to 1.8 V or 3.3 V. See *I2C Bus Pullup Resistor Calculation* (SLVA689).
IDx	47	I, S	I2C Serial Control Bus Device ID Address Select configuration pin Connect to an external pullup to VDD18 and a pulldown to GND to create a voltage divider. See 表 10.
SPI PINS			
MOSI (D_GPIO0)	19	I/O, PD	SPI Master Output, Slave Input pin (function programmed through register) It is a multifunction pin (shared with D_GPIO0) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *SPI Mode Configuration*. If unused, tie to an external pulldown.
MISO (D_GPIO1)	18	I/O, PD	SPI Master Input, Slave Output pin (function programmed through register) It is a multifunction pin (shared with D_GPIO1) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *SPI Mode Configuration*. If unused, tie to an external pulldown.
SPLK (D_GPIO2)	17	I/O, PD	SPI Clock pin (function programmed through register) It is a multifunction pin (shared with D_GPIO2) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *SPI Mode Configuration*. If unused, tie to an external pulldown.
SS (D_GPIO3)	16	I/O, PD	SPI Slave Select pin (function programmed through register) It is a multifunction pin (shared with D_GPIO0) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *SPI Mode Configuration*. If unused, tie to an external pulldown.
CONTROL PINS			
MODE_SEL0	61	I, S	Mode Select 0 configuration pin Connect to an external pullup to VDD33 and pulldown to GND to create a voltage divider. See 表 7.
MODE_SEL1	50	I, S	Mode Select 1 configuration pin Connect to external pullup to VDD33 and pulldown to GND to create a voltage divider. See 表 8.

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
PDB	48	I, PD	Inverted Power-Down input pin Typically connected to a processor GPIO with a pulldown. When PDB input is brought HIGH, the device is enabled and internal registers and state machines are reset to default values. Asserting PDB signal low will power down the device and consume minimum power. The default function of this pin is PDB = LOW; POWER DOWN with a weak (3 µA) internal pulldown enabled. PDB should remain low until after power supplies are applied and reach minimum required levels. PDB = 1, device is enabled (normal operation) PDB = 0, device is powered down When the device is in the POWER DOWN state, the LVCMOS outputs are in tri-state, the PLL is shut down, and IDD is minimized.
BISTEN	5	I, PD	BIST Enable pin 0: BIST mode is disabled 1: BIST mode is enabled It is a configuration pin with a weak (3 µA) internal pulldown. If unused, tie to an external pulldown. See *Built-In Self Test (BIST)* for more information.
BISTC (INTB_IN)	4	I, PD	BIST Clock Select pin (function set by BISTEN pin) 0: PCLK 1: 33 MHz It is a multifunction pin (shared with INTB_IN) with a weak internal pulldown (3 µA). Pin function is only enabled when in BIST mode. If unused, tie to an external pulldown.
INTB_IN (BISTC)	4	I, PD	Interrupt Input pin (default function) It is a multifunction pin (shared with BISTC) with a weak internal pulldown (3 µA). See *Interrupt Pin — Functional Description and Usage (INTB_IN)*. If unused, tie to an external pulldown.
GPIO PINS			
GPIO0 (SDOUT)	7	I/O, PD	General Purpose Input / Output 0 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with SDOUT) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO1 (SWC)	8	I/O, PD	General Purpose Input / Output 1 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with SWC) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO2 (I2S_DC)	10	I/O, PD	General Purpose Input / Output 2 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with I2S_DC) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO3 (I2S_DD)	9	I/O, PD	General Purpose Input / Output 3 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with I2S_DD) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO9 (MCLK)	15	I/O, PD	General Purpose Input / Output 9 pin (default function) default state: logic *LOW* It is a multifunction pin (shared with MCLK) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
HIGH-SPEED GPIO PINS			
D_GPIO0 (MOSI)	19	I/O, PD	High-Speed General Purpose Input / Output 0 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with MOSI) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
D_GPIO1 (MISO)	18	I/O, PD	High-Speed General Purpose Input / Output 1 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with MISO) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
D_GPIO2 (SPLK)	17	I/O, PD	High-Speed General Purpose Input / Output 2 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with SPLK) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
D_GPIO3 (SS)	16	I/O, PD	High-Speed General Purpose Input / Output 3 pin (default function) default state: *tri-state* Only available in Dual Link Mode. It is a multifunction pin (shared with SS) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
REGISTER ONLY GPIO PINS			
GPIO5_REG (I2S_DB)	11	I/O, PD	High-Speed General Purpose Input / Output 5 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_DB) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO6_REG (I2S_DA)	12	I/O, PD	High-Speed General Purpose Input / Output 6 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_DA) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO7_REG (I2S_WC)	14	I/O, PD	High-Speed General Purpose Input / Output 7 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_WC) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
GPIO8_REG (I2S_CLK)	13	I/O, PD	High-Speed General Purpose Input / Output 8 pin (default function) I2C register control only default state: logic *LOW* It is a multifunction pin (shared with I2S_CLK) with a weak internal pulldown (3 µA). Pin function is programmed through registers. See *General-Purpose I/O (GPIO)*. If unused, tie to an external pulldown.
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_WC (GPIO7_REG)	14	O	Slave Mode I2S Word Clock Output pin (function programmed through register) It is a multifunction pin (shared with GPIO7_REG). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
I2S_CLK (GPIO8_REG)	13	O	Slave Mode I2S Clock Output pin (function programmed through register) **NOTE: Disable I2S data jitter cleaner, when using these pins, through the register bit I2S Control: 0x2B[7]=1** It is a multifunction pin (shared with GPIO8_REG). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
I2S_DA (GPIO6_REG)	12	O	Slave Mode I2S Data Output pin (function programmed through register) It is a multifunction pin (shared with GPIO6_REG). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
I2S_DB (GPIO5_REG)	11	O	Slave Mode I2S Data Output pin (function programmed through register) It is a multifunction pin (shared with GPIO5_REG). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
I2S_DC (GPIO2)	10	O	Slave Mode I2S Data Output (function programmed through register) It is a multifunction pin (shared with GPIO2). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
I2S_DD (GPIO3)	9	O	Slave Mode I2S Data Output (function programmed through register) It is a multifunction pin (shared with GPIO3). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
MASTER MODE LOCAL I2S CHANNEL PINS			
SWC (GPIO1)	8	O	Master Mode I2S Word Clock Output pin (function is programmed through registers) (Pin is shared with GPIO1) It is a multifunction pin (shared with GPIO1). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.

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Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NUMBER		
SDOUT (GPIO0)	7	O	Master Mode I2S Data Output pin (function is programmed through registers) (Pin is shared with GPIO0) It is a multifunction pin (shared with GPIO0). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
MCLK (GPIO9)	15	O	Master Mode I2S System Clock Output pin (function is programmed through registers) (Pin is shared with GPIO9) It is a multifunction pin (shared with GPIO9). Pin function is programmed through registers. See *I2S Audio Interface*. If unused, tie to an external pulldown.
STATUS PINS			
LOCK	1	O	Lock Status Output pin LOCK = 1: PLL acquired lock to the reference clock input; DPHY outputs are active LOCK = 0: PLL is unlocked
PASS	7	O	Normal mode status output pin (BISTEN = 0) PASS = 1: No fault detected on input display timing PASS = 0: Indicates an error condition or corruption in display timing. Fault condition occurs: 1. DE length value mismatch measured once in succession 2. VSync length value mismatch measured twice in succession BIST mode status output pin (BISTEN = 1) PASS = 1: No error detected PASS = 0: Error detected
POWER and GROUND			
VDD33_A, VDD33_B	56 31	P	3.3-V (±10%) supply. Power to on-chip regulator. Recommend to connect with 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND.
VDDIO	3	P	LVCMOS I/O power supply: 1.8 V (±5%) OR 3.3 V (±10%). Recommend to connect with 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND.
VDD12_CSI0 VDDP12_CSI VDD12_CSI1 VDDL12_0 VDDL12_1 VDDP12_CH0 VDDR12_CH0 VDDP12_CH1 VDDR12_CH1	20 32 33 6 44 51 52 60 57	P	1.2-V (±5%) supply. Recommend to connect with 10-µF, 1-µF, 0.1-µF, and 0.01-µF capacitors to GND at each VDD pin.
CAP_I2S	2	D	Decoupling capacitor connection for on-chip regulator. Recommend to connect with a 0.1-µF decoupling capacitor to GND.
VSS	DAP	G	DAP is the large metal contact at the bottom side, located at the center of the WQFN package. Connect to the ground plane (GND) with at least 32 vias.
OTHER PINS			
CMLOUTP CMLOUTN	62 63	O	Channel Monitor Loop-through Driver differential output pins Route to a test point or a pad with 100-Ω termination resistor between pins for channel monitoring (recommended). See 図 38 or 図 39.
RES0 RES1	49 64	-	Reserved pins. May be left as No Connect pins.

The following definitions define the functionality of the I/O cells for each pin.

I/O TYPE:

- P = Power supply
- G = Ground
- D = Decoupling for an internal linear regulator
- S = Configuration/Strap Input (All strap pins have internal pulldowns determined by IOZ specification. If the default strap value is needed to be changed then an external resistor should be used.
- I = Input
- O = Output
- I/O = Input/Output
- PD = Internal pulldown

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7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Supply voltage	VDD33 (VDD33_A, VDD33_B)	–0.3	3.96	V
	VDD12 (VDD12_CSI0, VDD12_CSI1, VDDP12_CSI, VDDL_1, VDDL_2, VDDP12_CH0, VDDP12_CH1, VDDR12_CH0, VDDR12_CH1)	-0.3	1.44	V
	VDDIO	–0.3	3.96	V
Configuration input voltage	IDX, MODE_SEL0, MODE_SEL1	–0.3	3.96	V
LVCMOS I/O voltage	PDB, BIST_EN	-0.3	3.96	V
	GPIO0, GPIO1, GPIO2, GPIO3, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, LOCK, PASS, INTB_IN, MCLK	–0.3	$V_{(VDDIO)}$ + 0.3	V
Open-drain voltage	I2C_SDA, I2C_SCL	–0.3	3.96	V
CML output voltage	CMLOUTP, CMLOUTN	-0.3	2.75	V
FPD-Link III input voltage	RIN0+, RIN0-, RIN1+, RIN1-	–0.3	2.75	V
CSI-2 voltage	CSI0_D0+, CSI0_D0-, CSI0_D1+, CSI0_D1-, CSI0_D2+, CSI0_D2-, CSI0_D3+, CSI0_D3-, CSI0_CLK+, CSI0_CLK-, CSI1_D0+, CSI1_D0-, CSI1_D1+, CSI1_D1-, CSI1_D2+, CSI1_D2-, CSI1_D3+, CSI1_D3-, CSI1_CLK+, CSI1_CLK-,	–0.3	1.44	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office or Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±8000	V
	Charged-device model (CDM), per AEC Q100-011		±1250	
	ESD Ratings (IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, $R_{IN1–}$)	±8000	
		Air-gap Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, $R_{IN1–}$)	±15000	
	ESD Ratings (ISO 10605) R_D = 330 Ω, C_S = 150 and 330 pF R_D = 2 kΩ, C_S = 150 and 330 pF	Contact Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, $R_{IN1–}$)	±8000	
		Air-gap Discharge (R_{IN0+}, R_{IN0-}, R_{IN1+}, $R_{IN1–}$)	±15000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{(VDD33)}$	3	3.3	3.6	V
	$V_{(VDD12)}$	1.14	1.2	1.26	V
LVCMOS I/O supply voltage	$V_{(VDDIO)}$ = 3.3 V	3	3.3	3.6	V
	OR $V_{(VDDIO)}$ = 1.8 V	1.71	1.8	1.89	V
Open-drain voltage	I2C pins = $V_{(I2C)}$	1.71		3.6	V
Operating free air temperature, T_A		−40	25	105	°C

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Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Pixel clock frequency (single link)		25		96	MHz
Pixel clock frequency (dual link)		50		170	MHz
Local I^2C frequency, f_{I2C}				1	MHz
Supply noise (1)	$V_{(VDD33)}$			100	mV_{P-P}
	$V_{(VDDIO)}$ = 3.3 V			100	mV_{P-P}
	$V_{(VDDIO)}$ = 1.8 V			50	mV_{P-P}
	$V_{(VDD12)}$			25	mV_{P-P}

(1) DC to 50 MHz.

7.4 Thermal Information

THERMAL METRIC (1)		DS90UB940N-Q1 NKD (WQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	3.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermalmetrics, see the *Semiconductor and IC Package Thermal Metrics*application report.

7.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
POWER CONSUMPTION							
P_T	Total power consumption, normal operation	Checkerboard pattern, 170 MHz. See 図 1. 2-lane FPD-Link III input, 2 MIPI lanes output	VDD		628	875	mW
P_Z	Total power consumption, power-down mode	PDB = 0 V			10	45	mW
SUPPLY CURRENT							
IDD12	Supply current, normal operation	Checkerboard pattern, 96 MHz. See 図 1. 1-lane FPD-Link III input, 2 MIPI lanes output	VDD12 = 1.2 V		150	250	mA
IDD33	Supply current, normal operation		VDD33 = 3.6 V		90	122	mA
IDDIO	Supply current, normal operation		VDDIO = 1.89 V or 3.6 V		1	6	mA
IDD12	Supply current, normal operation	Checkerboard pattern, 96 MHz. See 図 1. 1-lane FPD-Link III input, 4 MIPI lanes output	VDD12 = 1.2 V		125	225	mA
IDD33	Supply current, normal operation		VDD33 = 3.6 V		90	122	mA
IDDIO	Supply current, normal operation		VDDIO = 1.89 V or 3.6 V		1	6	mA

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DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
IDD12	Supply current, normal operation	Checkerboard pattern, 170 MHz. See 図 1. 2-lane FPD-Link III input, 2 MIPI lanes output	VDD12 = 1.2 V		250	345	mA
IDD33	Supply current, normal operation		VDD33 = 3.6 V		90	122	mA
IDDIO	Supply current, normal operation		VDDIO = 1.89 V or 3.6 V		1	6	mA
IDD12	Supply current, normal operation	Checkerboard pattern, 170 MHz. See 図 1. 2-lane FPD-Link III input, 4 MIPI lanes output	VDD12 = 1.2 V		220	300	mA
IDD33	Supply current, normal operation		VDD33 = 3.6 V		90	122	mA
IDDIO	Supply current, normal operation		VDDIO = 1.89 V or 3.6 V		1	6	mA
IDD12Z	Supply current, power-down mode	PDB = 0 V	VDD12 = 1.2 V		2	30	mA
IDD33Z	Supply current, power-down mode		VDD33 = 3.6 V		2	8	mA
IDDIOZ	Supply current, power-down mode		VDDIO = 1.89 V or 3.6 V		0.1	0.3	mA
3.3-V LVCMOS I/O ($V_{(VDDIO)}$ = 3.3 V ± 10%)							
V_{IH}	High level input voltage		PDB, BISTEN	2		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.8	V
V_{IH}	High level input voltage		BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	2		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.8	V
I_{IN}	Input current	V_{IN} = 0 V or $V_{(VDDIO)}$		–10		10	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA		2.4		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		0		0.4	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			–55		mA
I_{OZ}	Tri-state output current	PDB = 0 V V_{OUT} = 0 V or $V_{(VDDIO)}$		–20		20	µA
C_{IN}	Input capacitance					10	pF
$I_{IN-STRAP}$	Strap pin input current	V_{IN} = 0 V or $V_{(VDDIO)}$	IDX, MODE_SEL0 MODE_SEL1	-1		1	µA
1.8-V LVCMOS I/O ($V_{(VDDIO)}$ = 1.8 V ± 5%)							
V_{IH}	High level input voltage		PDB, BISTEN	1.55		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.35 × $V_{(VDDIO)}$	V

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DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage		BISTC, GPIO[3:0], D_GPIO[3:0], I2S_DA, I2S_DB, I2S_DC, I2S_DD, I2S_CLK, I2S_WC, LOCK, PASS	0.65 × $V_{(VDDIO)}$		$V_{(VDDIO)}$	V
V_{IL}	Low level input voltage			0		0.35 × $V_{(VDDIO)}$	V
I_{IN}	Input current	V_{IN} = 0V or $V_{(VDDIO)}$		–10		10	µA
V_{OH}	High level output voltage	I_{OH} = –4 mA		$V_{(VDDIO)}$ – 0.45		$V_{(VDDIO)}$	V
V_{OL}	Low level output voltage	I_{OL} = 4 mA		0		0.45	V
I_{OS}	Output short-circuit current	V_{OUT} = 0 V			–35		mA
I_{OZ}	Tri-state output current	PDB = 0 V V_{OUT} = 0 V or $V_{(VDDIO)}$		–20		20	µA
C_{IN}	Input capacitance					10	pF
SERIAL CONTROL BUS ($V_{(VDDIO)}$ = 1.8 V ± 5% OR 3.3V ±10%)							
V_{IH}	Input high level	$V_{(VDDIO)}$ = 3.0 V to 3.6 V	I2C_SDA, I2C_SCL	2		$V_{(VDDIO)}$	V
V_{IL}	Input low level	$V_{(VDDIO)}$ = 3.0 V to 3.6 V		0		0.9	V
V_{IH}	Input high level	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		1.575		$V_{(VDDIO)}$	V
V_{IL}	Input low level	$V_{(VDDIO)}$ = 1.71 V to 1.89 V		0		0.9	V
V_{HYS}	Input hysteresis				50		mV
V_{OL}	Output low level	I_{OL} = 4 mA		0		0.4	V
I_{IN}	Input current	V_{IN} = 0 V or $V_{(VDDIO)}$		–10		10	µA

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DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III INPUT							
V_{TH}	Differential threshold high voltage	V_{CM} = 2.1 V	RIN0+, RIN0– RIN1+, RIN1–			50	mV
V_{TL}	Differential threshold low voltage			–50			mV
V_{ID}	Input differential threshold			100			mV
V_{CM}	Differential common-mode voltage				2.1		V
R_T	Internal termination resistor - differential			80	100	120	Ω
HSTX DRIVER							
V_{CMTX}	HS transmit static common-mode voltage		CSI0_D3±, CSI0_D2±, CSI0_D1±, CSI0_D0±, CSI0_CLK±, CSI1_D3±, CSI1_D2±, CSI1_D1±, CSI1_D0±, CSI1_CLK±	150	200	250	mV
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is 1 or 0					5	mV
$\lvert V_{OD}\rvert$	HS transmit differential voltage			140	200	270	mV
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is 1 or 0					14	mV
V_{OHHS}	HS output high voltage					360	mV
Z_{OS}	Single-ended output impedance			40	50	62.5	Ω
ΔZ_{OS}	Mismatch in single-ended output impedance					10	%
LPTX DRIVER							
V_{OH}	High-level output voltage	I_{OH} = –4 mA	CSI0_D3±, CSI0_D2±, CSI0_D1±, CSI0_D0±, CSI0_CLK±, CSI1_D3±, CSI1_D2±, CSI1_D1±, CSI1_D0±, CSI1_CLK±	1.05	1.2	1.3	V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA		–50		50	mV
Z_{OLP}	Output impedance			110			Ω
LOOP-THROUGH MONITOR OUTPUT							
V_{OD}	Differential output voltage	R_L = 100 Ω	CMLOUTP, CMLOUTN		360		mV

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7.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO BIT RATE							
$R_{b,FC}$	Forward channel bit rate	PCLK = 25 MHz - 170 MHz(1)	GPIO[3:0]		0.25 × PCLK		Mbps
$R_{b,BC}$	Back channel bit rate				133		kbps
$R_{b,BC}$	Back channel bit rate	High speed (2-lane mode), 1 D_GPIO active See 表 3	D_GPIO[3:0]		2		Mbps
		High speed (2-lane mode), 2 D_GPIOs active See 表 3.			1.33		Mbps
		High speed (2-lane mode), 4 D_GPIOs active See 表 3			800		kbps
		Normal mode — see 表 3			133		kbps
$t_{GPIO,FC}$	GPIO pulse width, forward channel		GPIO[3:0]	> 2 / PCLK(1)			s
$t_{GPIO,BC}$	GPIO pulse width, back channel		GPIO[3:0]	20			µs
RESET							
t_{LRST}	PDB reset low pulse		PDB	2			ms
LOOP-THROUGH MONITOR OUTPUT							
E_W	Differential output eye opening width	R_L = 100 Ω, jitter frequency > PCLK(1) / 40 See 図 2	CMLOUTP, CMLOUTN		0.4		UI(2)
E_H	Differential output eye height				> 300		mV
FPD-LINK III INPUT							
t_{DDLT}	Lock time	See 図 4	RIN0+, RIN0–, RIN1+, RIN1–		5	10	ms
t_{IJIT}	Input jitter	Single Lane PCLK = 96 MHz f_{JIT} > PCLK/20 BER < 1E-10 10-m DACAR535-2 STQ	RIN0+, RIN0–, RIN1+, RIN1–			0.3	UI(2)
		Dual Lane PCLK = 170 MHz f_{JIT} > PCLK/20 BER < 1E-10 10-m DACAR535-2 STQ					
I2S TRANSMITTER							
$t_{J,I2S}$	Clock output jitter		I2S_CLK		2		ns
t_{I2S}	I2S clock period(3)	See 図 9			>2 / PCLK(1) or >77		ns
$t_{HC,I2S}$	I2S clock high time(3)	See 図 9			0.48		t_{I2S}
$t_{LC,I2S}$	I2S clock low time(3)	See 図 9			0.48		t_{I2S}
$t_{SR,I2S}$	I2S set-up time	See 図 9	I2S_DA, I2S_DB, I2S_DC, I2S_DD		0.4		t_{I2S}
$t_{HR,I2S}$	I2S hold time	See 図 9			0.4		t_{I2S}

(1) PCLK refers to the equivalent pixel clock frequency, which is equal to the FPD-Link III line rate / 35.
(2) UI – Unit Interval is equivalent to one serialized data bit width. For Single Lane mode 1UI = 1 / (35*PCLK). For Dual Lane mode, 1UI = 1 / (35*PCLK/2). The UI scales with PCLK frequency.
(3) I2S specifications for $t_{LC,I2S}$ and $t_{HC,I2S}$ pulses must each be greater than 1 period to ensure sampling and supersedes the 0.35 × t_{I2S} requirement. $t_{LC,I2S}$ and $t_{HC,I2S}$ must be longer than the greater of either 0.35 × t_{I2S} or 2 × PCLK.

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7.7 Timing Requirements for the Serial Control Bus

Over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	Standard mode	> 0	100	kHz
		Fast mode	> 0	400	kHz
		Fast plus mode	> 0	1	MHz
t_{LOW}	SCL low period	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast plus mode	0.5		µs
t_{HIGH}	SCL high period	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition 図 8	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{SU;STA}$	Set-up time for a start or a repeated start condition 図 8	Standard mode	4.7		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
$t_{HD;DAT}$	Data hold time 図 8	Standard mode	0		µs
		Fast mode	0		µs
		Fast plus mode	0		µs
$t_{SU;DAT}$	Data set-up time 図 8	Standard mode	250		ns
		Fast mode	100		ns
		Fast plus mode	50		ns
$t_{SU;STO}$	Set-up time for STOP condition 図 8	Standard mode	4		µs
		Fast mode	0.6		µs
		Fast plus mode	0.26		µs
t_{BUF}	Bus free time between STOP and START 図 8	Standard mode	4.7		µs
		Fast mode	1.3		µs
		Fast plus mode	0.5		µs
t_r	SCL and SDA rise time, 図 8	Standard mode		1000	ns
		Fast mode		300	ns
		Fast plus mode		120	ns
t_f	SCL and SDA fall time, 図 8	Standard mode		300	ns
		Fast mode		300	ns
		Fast plus mode		120	ns
C_b	Capacitive load for each bus line	Standard mode		400	pF
		Fast mode		400	pF
		Fast plus mode		200	pF
t_{SP}	Input filter	Fast mode		50	ns
		Fast plus mode		50	ns

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7.8 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
HSTX DRIVER							
$HSTX_{DBR}$	Data bit rate	MIPI 2 lanes	CSI0_D0± CSI0_D1± CSI0_D2± CSI0_D3± CSI1_D0± CSI1_D1± CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK±	350		1344	Mbps
		MIPI 4 lanes		175		1190	
fCLK	DDR Clock frequency	MIPI 2 lanes		175		672	MHz
		MIPI 4 lanes		87.5		595	
$\Delta V_{CMTX(HF)}$	Common mode voltage variations HF	Above 450 MHz				15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode voltage variations LF	Between 50 and 450 MHz				25	mV_{RMS}
t_{RHS} t_{FHS}	20% to 80% rise and fall HS	HS bit rates ≤ 1 Gbps (UI ≥ 1 ns)				0.3	UI
		HS bit rates > 1 Gbps (UI < 1 ns)				0.35	UI
		Applicable for all HS bit rates. However, to avoid excessive radiation, bit rates ≤ 1 Gbps (UI ≥ 1 ns), must not use values below 150 ps.		100			ps
SDD_{TX}	TX differential return loss	f_{LPMAX}			–18		dB
		f_H			-9		dB
		f_{MAX}			–3		dB
LPTX DRIVER							
t_{RLP}	Rise time LP (1)	15% to 85% rise time	CSI0_D0± CSI0_D1± CSI0_D2± CSI0_D3± CSI1_D0± CSI1_D1± CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK±			25	ns
t_{FLP}	Fall time LP (1)	15% to 85% fall time				25	ns
t_{REOT}	Rise time post-EoT (1)	30% to 85% rise time				35	ns
$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock (1)	First LP exclusive-OR clock pulse after stop state or last pulse before stop state		40			ns
		All other pulses		20			ns
$t_{LP-PER-TX}$	Period of the LP exclusive-OR clock			90			ns
DV/DtSR	Slew rate (1)	C_{LOAD} = 0 pF				500	mV/ns
		C_{LOAD} = 5 pF				300	mV/ns
		C_{LOAD} = 20 pF				250	mV/ns
		C_{LOAD} = 70 pF				150	mV/ns
		C_{LOAD} = 0 to 70 pF (falling edge only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (rising edge only)		30			mV/ns
		C_{LOAD} = 0 to 70 pF (rising edge only)		30 – 0.075 × (VO,INST – 700)			mV/ns
C_{LOAD}	Load capacitance (1)			0		70	pF

(1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2-ns delay.

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Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
DATA-CLOCK TIMING SPECIFICATIONS (図 10)							
UI_{INST}	UI instantaneous	f_{CLK} = CSI-2 DDR clock frequency	CSI0_D0± CSI0_D1± CSI0_D2± CSI0_D3± CSI1_D0± CSI1_D1± CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK±		1/(f_{CLK} × 2)		UI
ΔUI	UI variation	UI ≥ 1 ns		–10%		10%	UI
		UI < 1 ns		–5%		5%	UI
$t_{SKEW(TX)}$	Data to clock skew (measured at transmitter) Skew between clock and data from ideal center	Data rate ≤ 1 Gbps		–0.15		0.15	UI_{INST}
		Data rate > 1 Gbps		–0.2		0.2	UI_{INST}
CSI-2 TIMING SPECIFICATIONS (図 11, 図 12)							
$t_{CLK-MISS}$	Timeout for receiver to detect absence of clock transitions and disable the clock lane HS-RX		CSI0_D0± CSI0_D1± CSI0_D2± CSI0_D3± CSI1_D0± CSI1_D1± CSI1_D2± CSI1_D3± CSI0_CLK± CSI1_CLK±	60			ns
$t_{CLK-POST}$	HS exit			60 + 52 × UI			ns
$t_{CLK-PRE}$	Time HS clock shall be driver prior to any associated data lane beginning the transition from LP to HS mode			8			UI
$t_{CLK-PREPARE}$	Clock lane HS Entry			38		95	ns
$t_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any clock lane HS transitions			95		300	ns
$t_{CLK-TERM-EN}$	Timeout at clock lane display module to enable HS Termination			Time for Dn to reach VTERM-EN		38	ns
$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst			60			ns
$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock			300			ns
$t_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination			Time for Dn to reach V-TERM-EN		35 + 4 × UI	ns
t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ to the start of the LP-11 state following a HS burst	see (2)				105 + 12 × UI	ns
$t_{HS-EXIT}$	Time that the transmitter drives LP=11 following a HS burst			100			ns
$t_{HS-PREPARE}$	Data lane HS entry			40 + 4 × UI		85 + 6 × UI	ns
$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence			145 + 10 × UI			ns
$t_{HS-SETTLE}$	Time interval during which the HS receiver ignores any data lane HS transitions, starting from the beginning of $t_{HS-SETTLE}$			85 + 6 × UI		145 + 10 × UI	ns

(2) a. 1280 × 720p60; PCLK = 74.25 MHz; 4 MIPI lanes Reg0x6C = 0x02; Reg0x6D = 0x84
b. 1280 × 720p60; PCLK = 74.25MHz; 2 MIPI lanes Reg0x6C = 0x02; Reg0x6D = 0x89
c. 640 × 480p60; PCLK = 25 MHz; 4 MIPI lanes Reg0x6C = 0x02; Reg0x6D = 0x82
d. 640 × 480p60; PCLK = 25 MHz; 2 MIPI lanes Reg0x6C = 0x02; Reg0x6D = 0x83
e. Other video formats may require additional register configuration.

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Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
$t_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the data lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.			40		55 + 4 × UI	ns
$t_{HS-TRAIL}$	Data lane HS exit			60 + 4 × UI			ns
t_{LPX}	Transmitted length of LP state			50			ns
t_{WAKEUP}	Recovery time from ultra-low-power state (ULPS)			1			ms

7.9 Timing Diagrams and Test Circuits

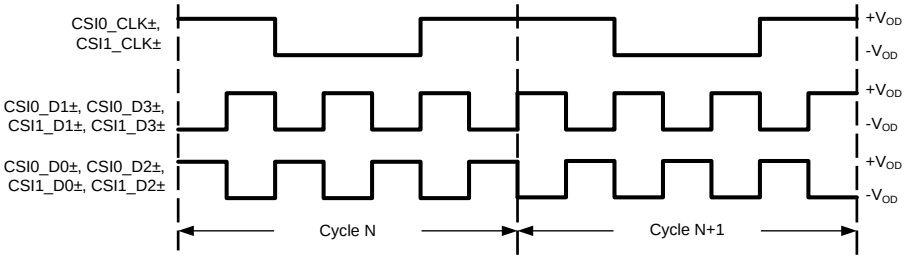


図 1. Checkerboard Data Pattern

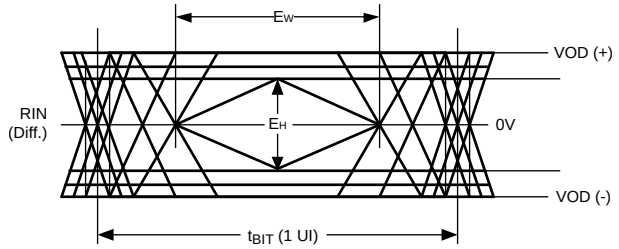


図 2. CML Output Driver

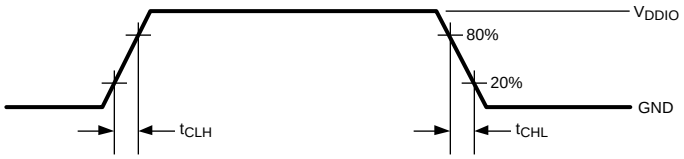


図 3. LVCMOS Transition Times

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Timing Diagrams and Test Circuits (continued)

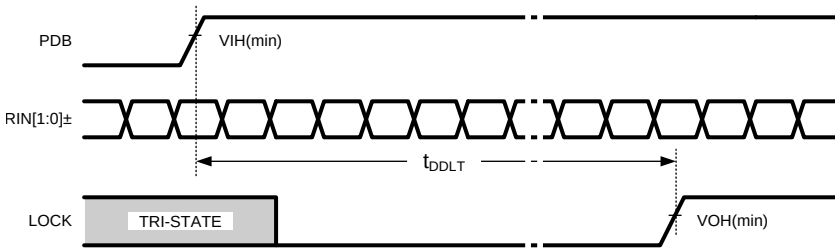


図 4. PLL Lock Time

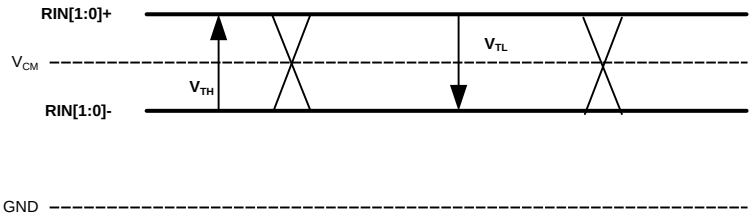


図 5. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

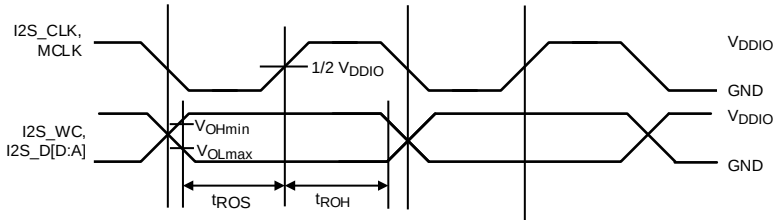


図 6. Output Data Valid (Setup and Hold) Times

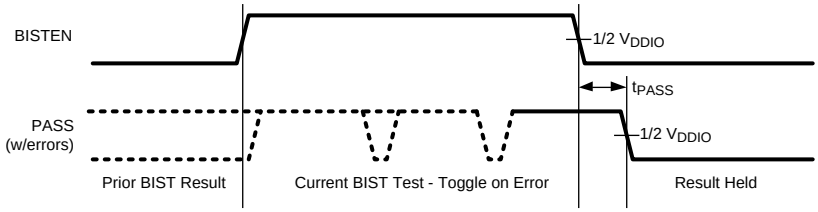


図 7. BIST PASS Waveform

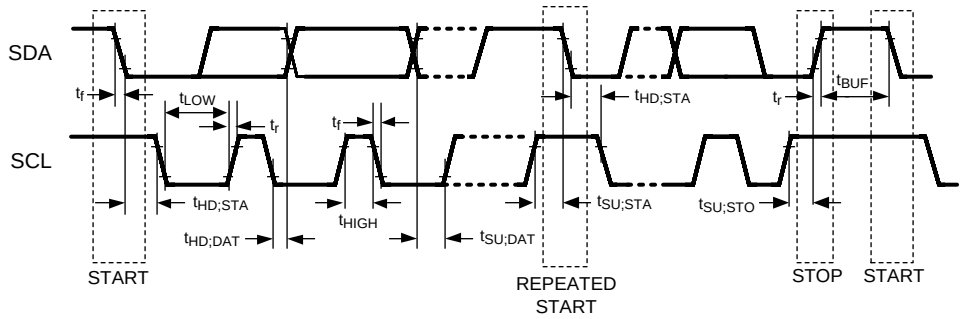


図 8. Serial Control Bus Timing Diagram

Timing Diagrams and Test Circuits (continued)

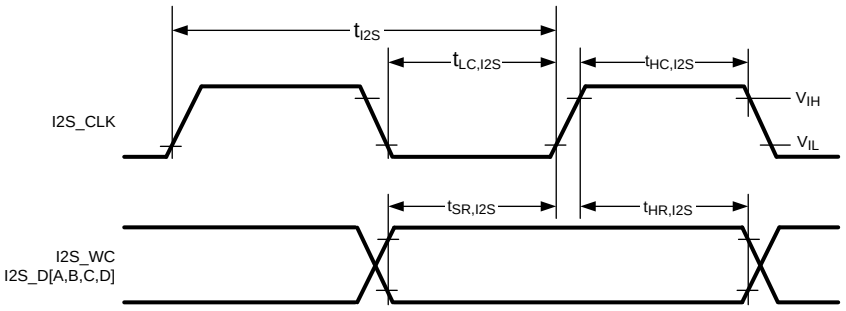


図 9. I2S Timing

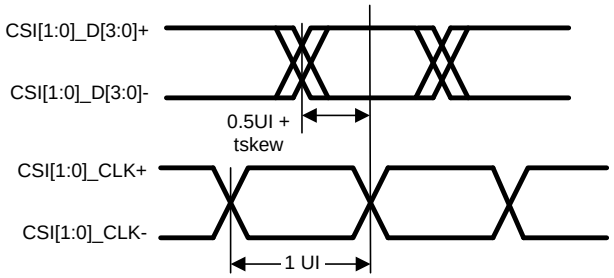


図 10. Clock and Data Timing in HS Transmission

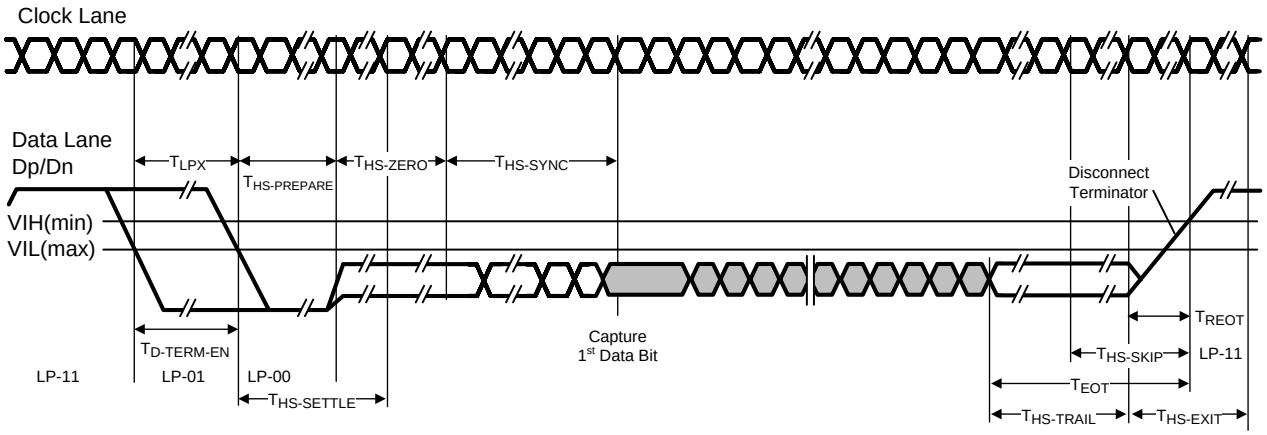


図 11. High-Speed Data Transmission Burst

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Timing Diagrams and Test Circuits (continued)

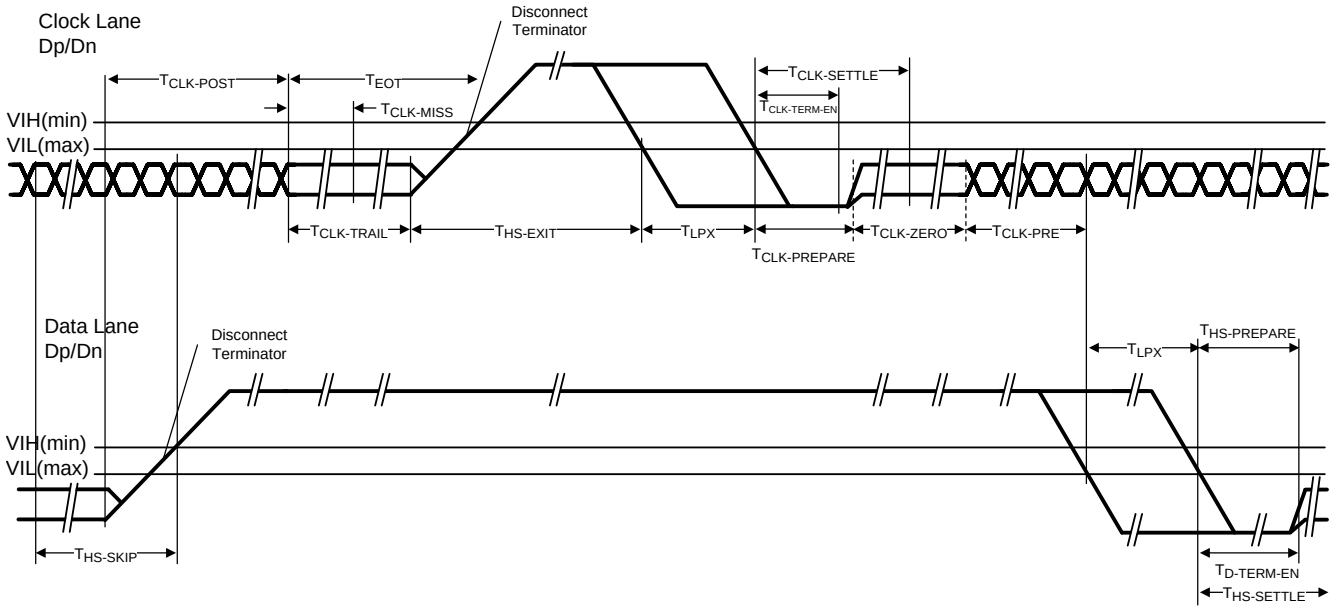


図 12. Switching the Clock Lane Between Clock Transmission and Low-Power Mode

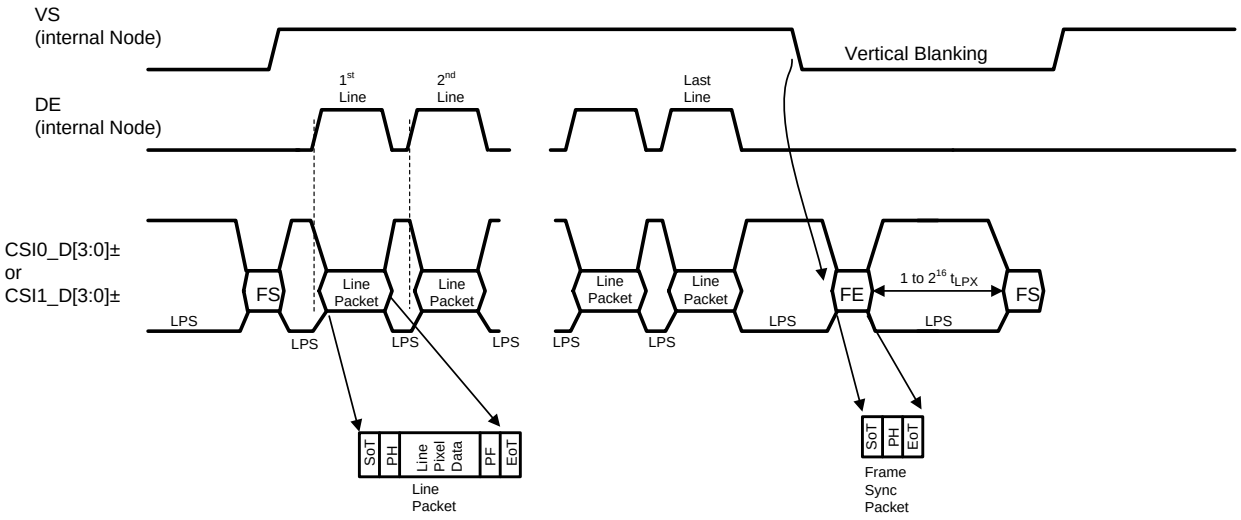


図 13. Long Line Packets and Short Frame Sync Packets

Timing Diagrams and Test Circuits (continued)

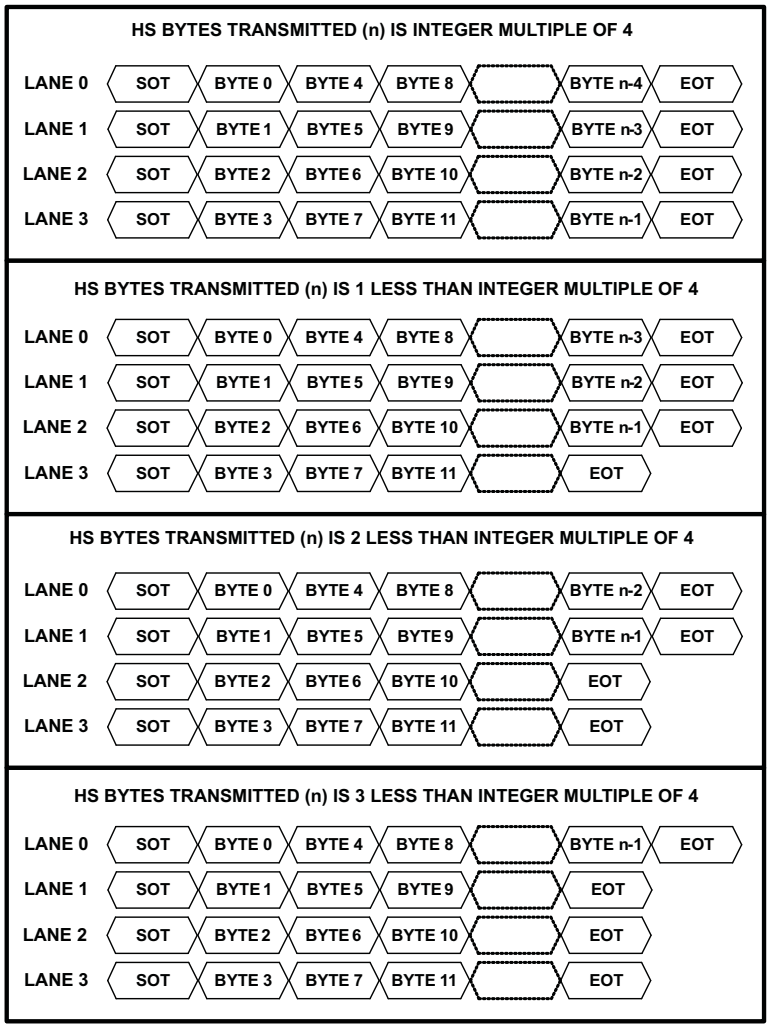


図 14. 4 MIPI® Data Lane Configuration

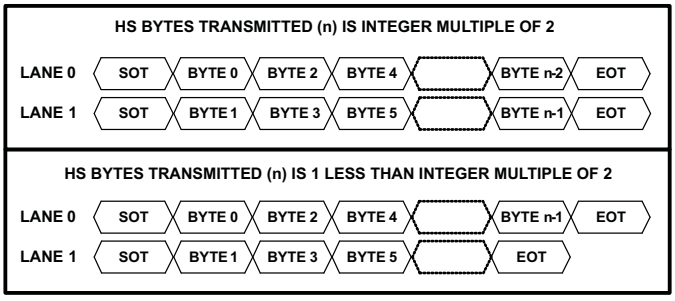


図 15. 2 MIPI® Data Lane Configuration

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7.10 Typical Characteristics

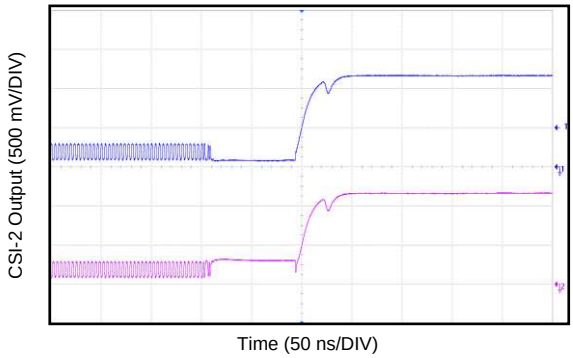


図 16. CSI-2 D0± End of Transmission

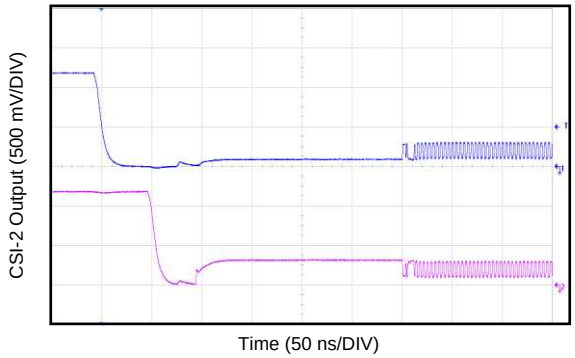


図 17. CSI-2 D0± Start of Transmission

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8 Detailed Description

8.1 Overview

The DS90UH940N-Q1 receives a 35-bit symbol over single or dual serial FPD-Link III pairs operating at up to a 3.36-Gbps line rate in 1-lane FPD-Link III mode and 2.975 Gbps per lane in 2-lane FPD-Link III mode. The DS90UH940N-Q1 converts this stream into a CSI-2 MIPI Interface (4 data channels + 1 clock, or 8 data channels + 2 clocks in replicate mode). The FPD-Link III serial stream contains an embedded clock, video control signals, audio, GPIOs, I2C, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

The DS90UH940N-Q1 is intended for use with the DS90UH949-Q1 or DS90UH947-Q1 serializers, but is also backward compatible to the DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 FPD-Link III serializers.

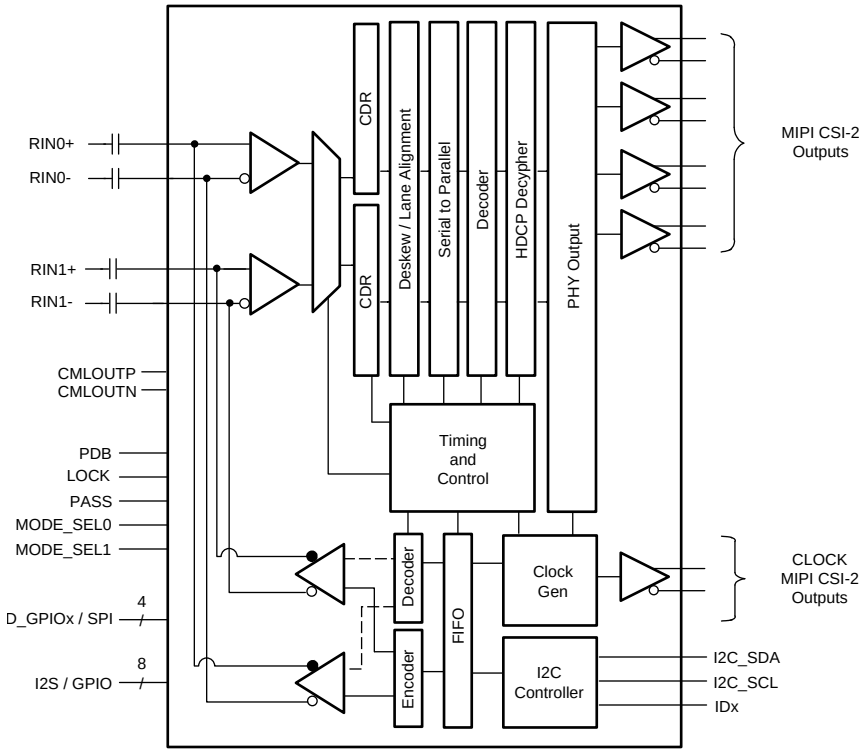
The DS90UH940N-Q1 deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic *plug and lock* performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. It also applies decryption through a high-bandwidth digital content protection (HDCP) Cipher to this video and audio data stream following reception of the data from the FPD-Link III decoder. On-chip non-volatile memory stores the HDCP keys. All key exchange is done through the FPD-Link III bidirectional control interface. The decrypted MIPI CSI-2 interface is provided to the processor.

The DS90UH940N-Q1 deserializer incorporates an I2C-compatible interface. The I2C-compatible interface allows programming of serializer or deserializer devices from a local host controller. The devices also incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C-compatible masters at either side of the serial link.

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8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 High-Speed Forward Channel Data Transfer

The high-speed forward channel is composed of 35 bits of data containing RGB data, sync signals, HDCP, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. 図 18 shows the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC-coupled link. Data is randomized, balanced, and scrambled.



図 18. FPD-Link III Serial Stream

The DS90UH940N-Q1 supports clocks in the range of 25 MHz to 96 MHz over 1 lane, or 50 MHz to 170 MHz over 2 lanes. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum) or 2.975 Gbps maximum per lane (875 Mbps minimum), respectively.

8.3.2 Low-Speed Back Channel Data Transfer

The Low-Speed Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, CRC and 4 bits of standard GPIO information with 5-Mbps or 20-Mbps line rate (configured by MODE_SEL1).

8.3.3 FPD-Link III Port Register Access

Because the DS90UH940N-Q1 contains two ports, some registers must be duplicated to allow control and monitoring of the two ports. To facilitate this, PORT1_SEL and PORT0_SEL bits (0x34[1:0]) register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) are available independent of the settings in the PORT_SEL register.

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Feature Description (continued)

Setting the PORT1_SEL and PORT0_SEL bit allows a read of the register for the selected port. If both bits are set, port1 registers are returned. Writes occur to ports for which the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

8.3.4 Clock and Output Status

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is tri-state or LOW (depending on the value of the OUTPUT ENABLE setting). After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVCMOS and LVDS outputs. The state of the outputs is based on the OUTPUT ENABLE and OUTPUT SLEEP STATE SELECT register settings. See register 0x02 in Table 11.

表 1. Output State Table

INPUTS				OUTPUTS			
SERIAL INPUT	PDB	OUTPUT ENABLE Reg 0x02 [7]	OUTPUT SLEEP STATE SELECT Reg 0x02 [4]	LOCK	PASS	DATA GPIO / D_GPIO I2S	CSI-2 OUTPUT
X	L	X	X	Z	Z	Z	Z
X	H	L	L	L or H	L	L	HS0
X	H	L	H	L or H	Z	Z	Z
Static	H	H	L	L	L	L	HS0
Static	H	H	H	L	Previous status	L	HS0
Active	H	H	L	L	L	L	HS0
Active	H	H	H	H	Valid	Valid	Valid

8.3.5 LVCMOS VDDIO Option

The 1.8-V or 3.3-V inputs and outputs are powered from a separate VDDIO supply to offer compatibility with external system interface signals.

注

When configuring the VDDIO power supplies, all the single-ended data and control input pins for device must scale together with the same operating VDDIO levels.

8.3.6 Power Down (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the VDDIO, where VDDIO = 3 V to 3.6 V or VDD33. To save power, disable the link when the display is not needed (PDB = LOW). When the pin is driven by the host, make sure to release it after VDD33 and VDDIO have reached final levels; no external components are required. When the PDB input pin is driven by the VDDIO = 3 V to 3.6 V or VDD33 directly, a 10-kΩ resistor to the VDDIO = 3 V to 3.6 V or VDD33 and a > 10-µF capacitor to the GND, are required (see 図 38 Typical Connection Diagram).

8.3.7 Interrupt Pin — Functional Description and Usage (INTB_IN)

The INTB_IN pin is an active low interrupt input pin. This interrupt signal, when configured, propagates to the paired serializer. Consult the appropriate serializer data sheet for details of how to configure this interrupt functionality.

1. On the serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN (pin 4) is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read ISR register.
5. A read to ISR clears the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the deserializer INTB_IN. This would be when the downstream device

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releases the INTB_IN (pin 4) on the deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

8.3.8 General-Purpose I/O (GPIO)

The DS90UH940N-Q1 deserializer features standard General-Purpose I/O (GPIO) and High-speed General-Purpose I/O (D_GPIO) pins. The D_GPIO pins are functional only in 2-lane FPD-Link III mode.

8.3.8.1 GPIOx and D_GPIOx Pin Configuration

In normal operation, GPIOx pins may be used as GPIOs in either forward channel (outputs) or back channel (inputs) mode. GPIO and D_GPIO modes may be configured through the registers (Table 11). The same registers configure either GPIOx or D_GPIOx pins, depending on the status of PORT1_SEL and PORT0_SEL bits (0x34[1:0]). D_GPIO mode operation requires 2-lane FPD-Link III mode. Consult the appropriate serializer data sheet for details on D_GPIOx pin configuration. Note: if paired with a DS90UH925Q-Q1 serializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the serializer. To enable 18-bit mode, set serializer register 0x12[2] = 1. 18-bit mode is auto-loaded into the deserializer from the serializer. See 表 2 for GPIOx pins enable and configuration.

表 2. GPIO / D_GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3 / D_GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2 / D_GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1 / D_GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0 / D_GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

The input value present on GPIO[3:0] or D_GPIO[3:0] may also be read from register or configured to local output mode (Table 11).

8.3.8.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. The mode is controlled by register 0x43 (Table 11). The back channel frequency can be controlled several ways:

1. Register 0x23[6] sets the divider that controls the back channel frequency based on the internal oscillator. 0x23[6] = 0 sets the divider to 4 and 0x23[6] = 1 sets the divider to 2. As long as BC_HS_CTL (0x23[4]) is set to 0, the back channel frequency is either 5 Mbps or 10 Mbps, based on this bit.
2. Register 0x23[4] enables the high-speed back channel. This can also be pin-strapped through MODE_SEL1 (see 表 3). This bit overrides 0x23[6] and sets the divider for the back channel frequency to 1. Setting this bit to 1 sets the back channel frequency to 20 Mbps.

The back channel frequency has variation of ±20%. Note: The back channel frequency must be set to 5 Mbps when paired with a DS90UH925Q-Q1, DS90UH925AQ-Q1, or DS90UH927Q-Q1. See 表 3 for details about configuring the D_GPIOs in various modes.

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表 3. Back Channel D_GPIO Effective Frequency

HSCC_MODE (0x43[2:0])	MODE	NUMBER OF D_GPIOs	SAMPLES PER FRAME	D_GPIO EFFECTIVE FREQUENCY(1) (kHz)			D_GPIOs ALLOWED
				5 Mbps BC(2)	10 Mbps BC(3)	20 Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst-case back channel frequency (–20%) and a 4×sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 & BC_HS_CTL = 0.
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 & BC_HS_CTL = 0.
(4) 20 Mbps corresponds to BC FREQ SELECT = X & BC_HS_CTL = 1.

8.3.8.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See 表 4 for GPIO enable and configuration.

注

Local GPIO value may be configured and read either through local register access, or remote register access through the low-speed bidirectional control channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

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表 4. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO9	0x1A[3:0] = 0x1	Output, L
	0x1A[3:0] = 0x9	Output, H
	0x1A[3:0] = 0x3	Input, Read: 0x6F[1]
GPIO_REG8	0x21[7:4] = 0x1	Output, L
	0x21[7:4] = 0x9	Output, H
	0x21[7:4] = 0x3	Input, Read: 0x6F[0]
GPIO_REG7	0x21[3:0] = 0x1	Output, L
	0x21[3:0] = 0x9	Output, H
	0x21[3:0] = 0x3	Input, Read: 0x6E[7]
GPIO_REG6	0x20[7:4] = 0x1	Output, L
	0x20[7:4] = 0x9	Output, H
	0x20[7:4] = 0x3	Input, Read: 0x6E[6]
GPIO_REG5	0x20[3:0] = 0x1	Output, L
	0x20[3:0] = 0x9	Output, H
	0x20[3:0] = 0x3	Input, Read: 0x6E[5]
GPIO3	0x1F[3:0] = 0x1	Output, L
	0x1F[3:0] = 0x9	Output, H
	0x1F[3:0] = 0x3	Input, Read: 0x6E[3]
GPIO2	0x1E[7:4] = 0x1	Output, L
	0x1E[7:4] = 0x9	Output, H
	0x1E[7:4] = 0x3	Input, Read: 0x6E[2]
GPIO1	0x1E[3:0] = 0x1	Output, L
	0x1E[3:0] = 0x9	Output, H
	0x1E[3:0] = 0x3	Input, Read: 0x6E[1]
GPIO0	0x1D[3:0] = 0x1	Output, L
	0x1D[3:0] = 0x9	Output, H
	0x1D[3:0] = 0x3	Input, Read: 0x6E[0]

8.3.9 SPI Communication

The SPI control channel uses the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available: forward channel and reverse channel modes. In forward channel mode, the SPI master is located at the serializer, such that the direction of sending SPI data is in the same direction as the video data. In reverse channel mode, the SPI master is located at the deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI control channel can operate in a high-speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

注

SPI cannot be used to access serializer or deserializer registers.

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8.3.9.1 SPI Mode Configuration

SPI is configured over I2C using the high-speed control channel configuration (HSCC_CONTROL) register, 0x43 (See Table 11). HSCC_MODE (0x43[2:0]) must be configured for either high-speed, forward channel SPI mode (110) or high-speed, reverse channel SPI mode (111).

8.3.9.2 Forward Channel SPI Operation

In forward channel SPI operation, the SPI master located at the serializer generates the SPI clock (SPLK), master out / slave in data (MOSI), and active low slave select (SS). The serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the deserializer, the SPI signals are regenerated using the pixel clock. To preserve setup and hold time, the deserializer holds MOSI data while the SPLK signal is high. The deserializer also delays SPLK by one pixel clock relative to the MOSI data, increasing setup by one pixel clock.

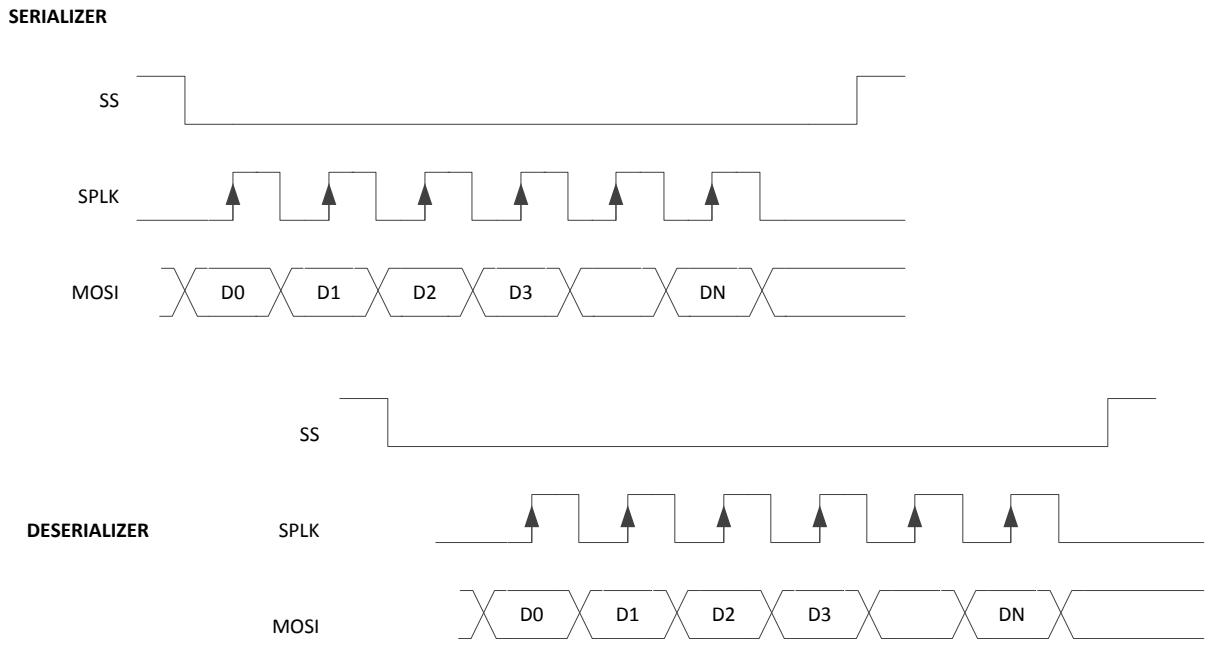


図 19. Forward Channel SPI Write

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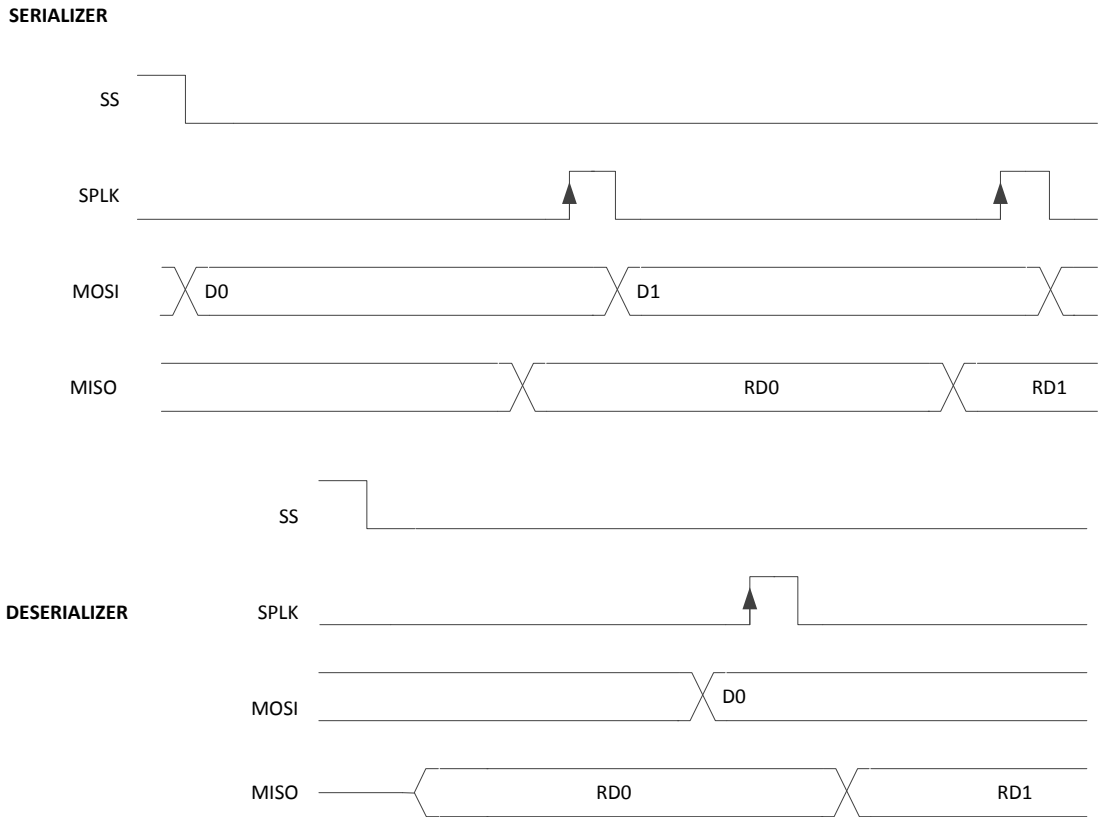


図 20. Forward Channel SPI Read

8.3.9.3 Reverse Channel SPI Operation

In reverse channel SPI operation, the deserializer samples the slave select (SS), SPI clock (SCLK) into the internal oscillator clock domain. Upon detection of the active SPI clock edge, the deserializer also samples the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the serializer over the back channel. The deserializer sends SPI information in a back channel frame to the serializer. In each back channel frame, the deserializer sends an indication of the SS value. The SS must be inactive (high) for at least one back-channel frame period to ensure propagation to the serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. 図 21 shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

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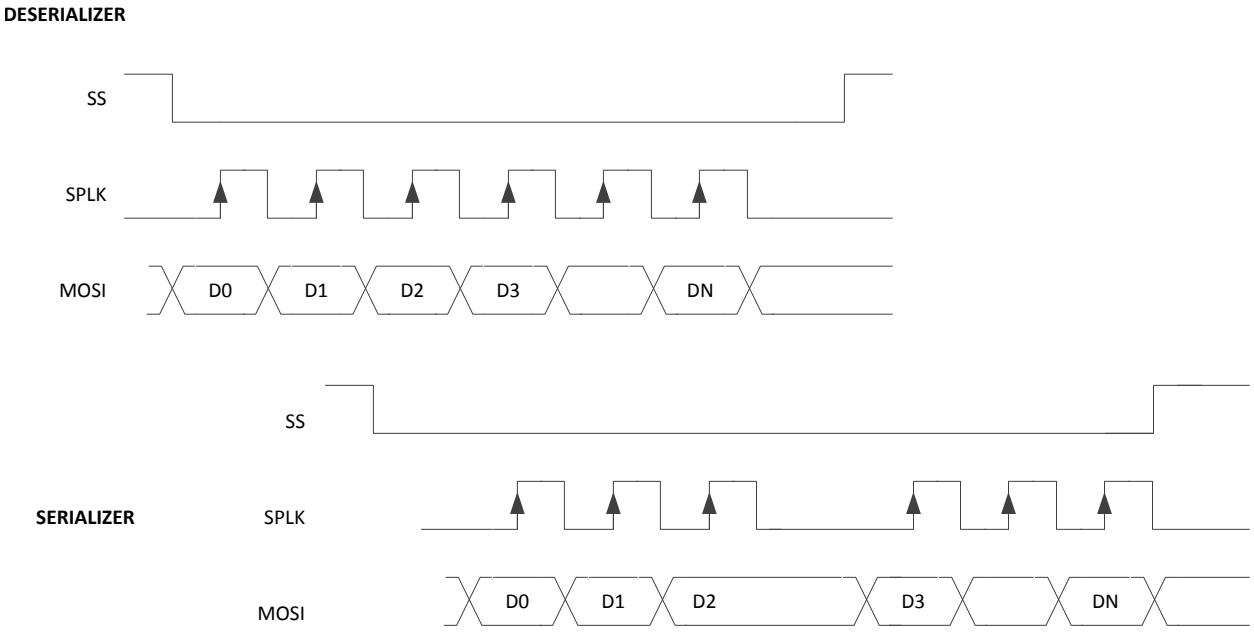


図 21. Reverse Channel SPI Write

For reverse channel SPI reads, the SPI master must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in forward channel mode. Note that at most one data/clock sample is sent per back channel frame.

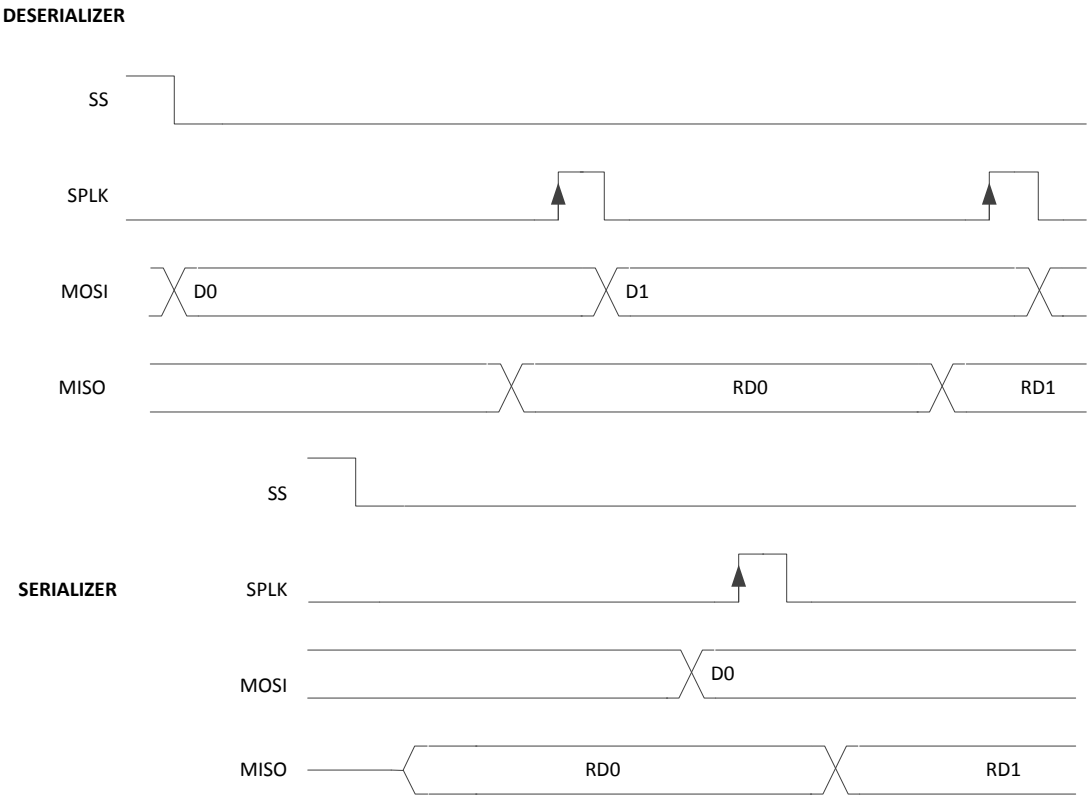


図 22. Reverse Channel SPI Read

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For both reverse-channel SPI writes and reads, the SPI_SS signal must be deasserted for at least one back-channel frame period.

表 5. SPI SS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

8.3.10 Backward Compatibility

The DS90UH940N-Q1 is also backward compatible to the DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 for PCLK frequencies ranging from 25 MHz to 85 MHz. Backward compatibility does not need to be enabled. When paired with a backward-compatible device, the deserializer auto-detects to 1-lane FPD-Link III on the primary channel (RIN0±).

8.3.11 Adaptive Equalizer

The FPD-Link III receiver inputs incorporate an adaptive equalizer (AEQ) to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI), crosstalk, and so forth, must also be considered. The equalization configuration programmed in registers 0x35 (AEQ_CTL1) and 0x45 (AEQ_CTL2). See Table 11.

8.3.11.1 Transmission Distance

The DS90UH940N-Q1 AEQ can compensate for the transmission channel insertion loss of up to –15.3 dB at 1.7 GHz. When designing the transmission channel, consider the total insertion loss of all components in the signal path between a serializer and a deserializer. Typically, the transmission channel would consist of a serializer PCB, two or more connectors, one or more cables, and a deserializer PCB as shown in 図 23.

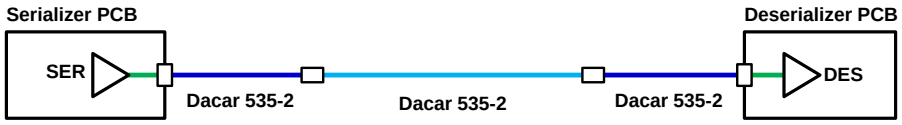


図 23. Typical Transmission Channel Components With STQ Cables

8.3.11.2 Adaptive Equalizer Algorithm

The AEQ process steps through allowed values of the equalizer controls find a value that allows the Clock Data Recovery (CDR) circuit to maintain valid lock condition. For each EQ setting, the circuit waits for a programmed re-lock time period, then checks results for valid lock. If valid lock is detected, the circuit will stop at the current EQ setting and maintain constant value as long as lock state persists. If the deserializer loses LOCK, the adaptive equalizer will resume the LOCK algorithm and the EQ setting is incremented to the next valid state. Once lock is lost, the circuit will continue searching EQ settings to find a valid setting to reacquire the serial data stream sent by the serializer that remains locked.

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8.3.11.3 AEQ Settings

8.3.11.3.1 AEQ Start-Up and Initialization

The AEQ circuit can be restarted at any time by setting the AEQ_RESTART bit in the AEQ_CTL1 register 0x35. Once the deserializer is powered on, the AEQ is continually searching through EQ settings and could be at any setting when signal is supplied from the serializer. If the Rx Port CDR locks to the signal, it may be good enough for low bit errors, but could be not optimized or over-equalized. For a consistent initial EQ setting, TI recommends that the user applies AEQ_RESTART or DIGITAL_RESET0 when the serializer input signal frequency is stable to restart adaption from the minimum EQ gain value.

8.3.11.3.2 AEQ Range

The user can program the AEQ circuit with the minimum AEQ level setting used during the EQ adaption. Using the full AEQ range will provide the most flexible solution, however, if the channel conditions are known and an improved deserializer lock time can be achieved by narrowing the search window for allowable EQ gain settings. For example, in a system use case with a longer cable and multiple interconnects creating a higher channel attenuation, the AEQ would not adapt to the minimum EQ gain settings. In this case, starting the adaptation from a higher AEQ level would improve lock time. The AEQ range is determined by the AEQ_CTL2 register 0x45 where the ADAPTIVE_EQ_FLOOR_VALUE determines the starting value for EQ gain adaption. The maximum AEQ limit is not adjustable. To enable the minimum AEQ limit, OVERRIDE_AEQ_FLOOR and SET_AEQ_FLOOR bits in the AEQ_CTL1 register must also be set. The setting for the AEQ after adaption can be readback from the AEQ_STATUS register 0x3B. See Table 11.

8.3.11.3.3 AEQ Timing

The dwell time for AEQ to wait for either the lock or error-free status is also programmable. When checking each EQ setting, the AEQ will wait for a time interval, controlled by the ADAPTIVE_EQ_RELOCK_TIME field in the AEQ_CTL2 register (see Table 11) before incrementing to the next allowable EQ gain setting. The default wait time is set to 2.62 ms. Once the maximum setting is reached, if there is no lock acquired during the programmed relock time, the AEQ will restart adaption at the minimum setting or AEQ_FLOOR value.

8.3.12 I2S Audio Interface

This deserializer features six I2S output pins that, when paired with a compatible serializer, support surround-sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the smaller of < PCLK/2 or < 13 MHz. Four I2S data outputs carry two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input.

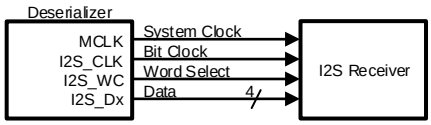


図 24. I2S Connection Diagram

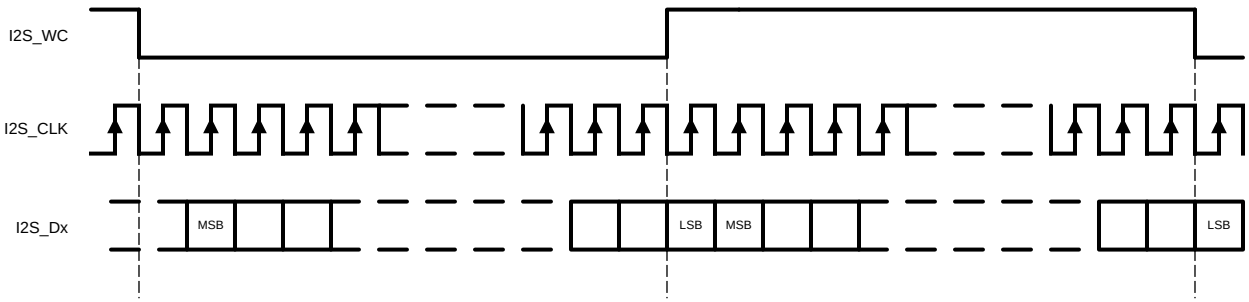


図 25. I2S Frame Timing Diagram

When paired with a DS90UH925Q , the deserializer I2S interface supports a single I2S data output through I2S_DA (24-bit video mode) or two I2S data outputs through I2S_DA and I2S_DB (18-bit video mode).

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8.3.12.1 I2S Transport Modes

By default, packetized audio is received during video blanking periods in dedicated data island transport frames. The transport mode is set in the serializer and auto-loaded into the deserializer by default. The audio configuration may be disabled from control registers if forward channel frame transport of I2S data is desired. In frame transport, only I2S_DA is received to the deserializer. Surround sound mode, which transmits all four I2S data inputs (I2S_D[D:A]), may only be operated in data island transport mode. This mode is only available when connected to a DS90UH927Q, DS90UH949-Q1, DS90UH947-Q1, or DS90UH929-Q1 serializer. If connected to a DS90UH925Q serializer, only I2S_DA and I2S_DB may be received.

8.3.12.2 I2S Jitter Cleaning

This device features a standalone PLL to clean the I2S data jitter, supporting high-end car audio systems. If I2S_CLK frequency is less than 1MHz, this feature must be disabled through register 0x2B[7]. See the *Table 11* section.

8.3.12.3 MCLK

The deserializer has an I2S Master Clock Output (MCLK). It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. 表 6 covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bits 0x3A[6:4] (I2S DIVSEL), shown in Table 11. To select desired MCLK frequency, write 0x3A[7], then write to bit [6:4] accordingly.

表 6. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	16	1.024	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		1.4112	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
48		1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
96		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
192		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100

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表 6. Audio Interface Frequencies (continued)

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	24	1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		2.117	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		2.304	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		4.608	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		9.216	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	101
32	32	2.048	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
44.1		2.8224	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		12.288	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	110

8.3.13 HDCP

The HDCP Cipher function is implemented in the deserializer per HDCP v1.4 specification. The DS90UH940N-Q1 provides HDCP decryption of audiovisual content when connected to an HDCP capable FPD-Link III serializer. HDCP authentication and shared key generation is performed using the HDCP control channel, which is embedded in the forward and backward channels of the serial link. On-chip non-volatile memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

8.3.13.1 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized data island transport audio is also encrypted along with the video data per HDCP v1.4. I2S audio transmitted in forward channel frame transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

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8.3.14 Built-In Self Test (BIST)

An optional at-speed built-in self test (BIST) feature supports testing of the high-speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.3.14.1 BIST Configuration And Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33-MHz internal oscillator clock (OSC) frequency in the serializer. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the back channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or power down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See 図 26 for the BIST mode flow diagram.

8.3.14.1.1 Sample BIST Sequence

Note: Before BIST can be enabled, D_GPIO0 (pin 19) must be strapped HIGH and D_GPIO[3:1] (pins 16, 17, and 18) must be strapped LOW.

1. BIST Mode is enabled through the BISTEN pin of deserializer. The desired clock source is selected through the deserializer BISTC pin.
2. The serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires LOCK, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin switches low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate per 35 bits.
3. To stop BIST mode, set the BISTEN pin LOW. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error-free, the PASS output remains HIGH. If there one or more errors were detected, the PASS output outputs constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. 図 27 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error-free, and Case 2 shows one with multiple errors. In most cases, it is difficult to generate errors due to the robustness of the link (differential data transmission, and so forth). Errors may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx equalization).

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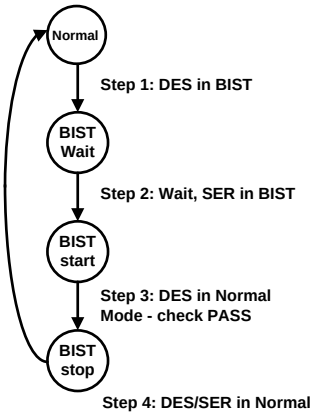


図 26. BIST Mode Flow Diagram

8.3.14.2 Forward Channel and Back Channel Error Checking

The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer. Forward channel errors may also be read from register 0x25 (Table 11).

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 11). CRC errors are recorded in an 8-bit register in the serializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until either the error is cleared or the serializer enters BIST mode again.

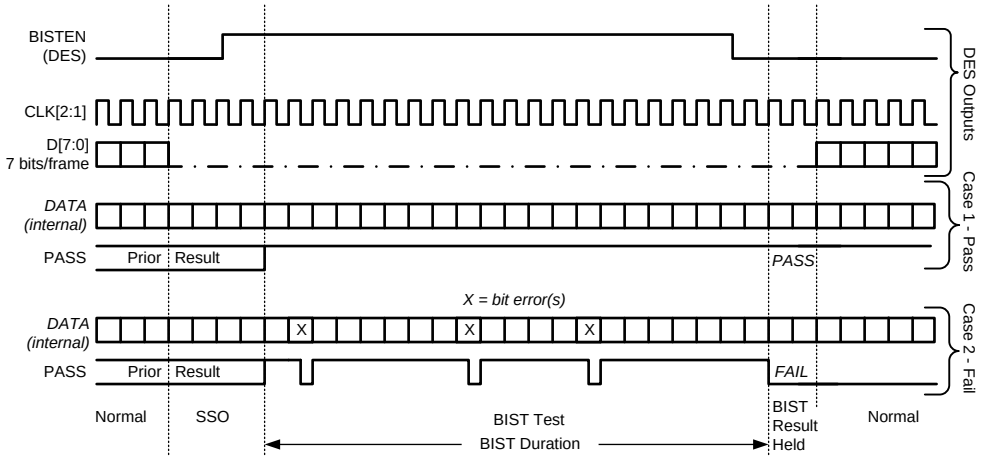


図 27. BIST Waveforms

8.3.15 Internal Pattern Generation

The deserializer supports the internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern is displayed even if no parallel input is applied. If no PCLK is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to *Exploring the Internal Test Pattern Generation Feature of 720p FPD-Link III Devices* (SNLA132).

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8.4 Device Functional Modes

8.4.1 Configuration Select

The DS90UH940N-Q1 can be configured for several different operating modes either through the MODE_SEL[1:0] input pins or through the register bits 0x23 [4:3] (MODE_SEL1) and 0x6A [5:4] (MODE_SEL0). A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] input and VDD33 to select one of the possible selected modes.

The DS90UH940N-Q1 is capable of operating in either in 1-lane or 2-lane modes for FPD-Link III. By default, the FPD-Link III receiver automatically configures the input based on 1- or 2-lane mode operation. Programming register 0x34 [4:3] settings overrides the automatic detection. For each FPD-Link III pair, the serial datastream is composed of a 35-bit symbol.

The DS90UH940N-Q1 recovers the FPD-Link III serial datastream(s) and produces CSI-2 TX data driven to the MIPI DPHY interface. There are two CSI-2 ports (CSI0_Dn and CSI1_Dn) and each consist of one clock lane and four data lanes. The DS90UH940N-Q1 supports two CSI-2 TX ports, and each may be configured to support either two or four CSI-2 data lanes. Unused CSI-2 outputs are driven to LP11 states. The MIPI DPHY transmission operates in both differential (HS) and single-ended (LP) modes. During HS transmission, the pair of outputs operates in differential mode; and in LP mode, the pair operates as two independent single-ended traces. Both the data and clock lanes enter LP mode during the horizontal and vertical blanking periods.

The configurations outlined in 図 28 apply to DS90UH949-Q1, DS90UH947-Q1, DS90UH929-Q1, DS90UH925Q-Q1, DS90UH925AQ-Q1, and DS90UH927Q-Q1 FPD-Link III serializers.

The configurations outlined in 図 29 apply to DS90UH949-Q1 and DS90UH947-Q1 FPD-Link III serializers.

The device can be configured in following modes:

- 1-lane FPD-Link III input, 4 MIPI lanes output
- 1-lane FPD-Link III input, 2 MIPI lanes output
- 2-lane FPD-Link III input, 4 MIPI lanes output
- 2-lane FPD-Link III input, 4 MIPI lanes output
- 1- or 2-lane FPD-Link III input, 2 or 4 MIPI lanes output (replicate)

8.4.1.1 1-Lane FPD-Link III Input, 4 MIPI® Lanes Output

In this configuration the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each MIPI data lane operates at a speed of 7 × PCLK frequency; resulting in a data rate of 175 Mbps to 672 Mbps. The corresponding MIPI transmit clock rate operates between 87.5 MHz to 336 MHz.

8.4.1.2 1-Lane FPD-Link III Input, 2 MIPI® Lanes Output

In this configuration, the PCLK rate embedded within the 1-lane FPD-Link III frame can range from 25 MHz to 96 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 3.36 Gbps (35 bit × 96 MHz). Each MIPI data lane operates at a speed of 14 × PCLK frequency; resulting in a data rate of 350 Mbps to 1344 Mbps. The corresponding MIPI transmit clock rate operates between 175 MHz to 672 MHz.

8.4.1.3 2-Lane FPD-Link III Input, 4 MIPI® Lanes Output

In this configuration, the PCLK rate embedded is split into 2-lane FPD-Link III frame and can range from 50 MHz to 170 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 2.975 Gbps (35 bit × 85 MHz). The embedded datastreams from the received FPD-Link III inputs are merged in HS mode to form packets that carry the video stream. Each MIPI data lane will operate at a speed of 7 × PCLK frequency, resulting in a data rate of 350 Mbps to 1190 Mbps. The corresponding MIPI transmit clock rate operates between 175 MHz to 595 MHz.

8.4.1.4 2-Lane FPD-Link III Input, 2 MIPI® Lanes Output

In this configuration, the PCLK rate embedded is split into 2-lane FPD-Link III frame and can range from 25 MHz to 48 MHz, resulting in a link rate of 875 Mbps (35 bit × 25 MHz) to 1.680 Gbps (35 bit × 48 MHz). The embedded datastreams from the received FPD-Link III inputs are merged in HS mode to form packets that carry the video stream. Each MIPI data lane will operate at a speed of 14 × PCLK frequency, resulting in a data rate of 700 Mbps to 1344 Mbps. The corresponding MIPI transmit clock rate will operate between 350 MHz to 672 MHz.

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Device Functional Modes (continued)

8.4.1.5 1- or 2-Lane FPD-Link III Input, 2 or 4 MIPI® Lanes Output in Replicate

Same as 1- or 2-lane FPD-Link III input(s), this mode can duplicate the MIPI CSI-2 lanes on CSI1_D[3:0] and CSI1_CLK outputs.

8.4.2 MODE_SEL[1:0]

Configuration of the device may be done either through the MODE_SEL[1:0] input pins or through the configuration register bits. A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs (V_{R4}) and VDD33 to select one of the other eight possible selected modes. See 表 7 and 表 8. Possible configurations are shown in 図 28 and 図 29.

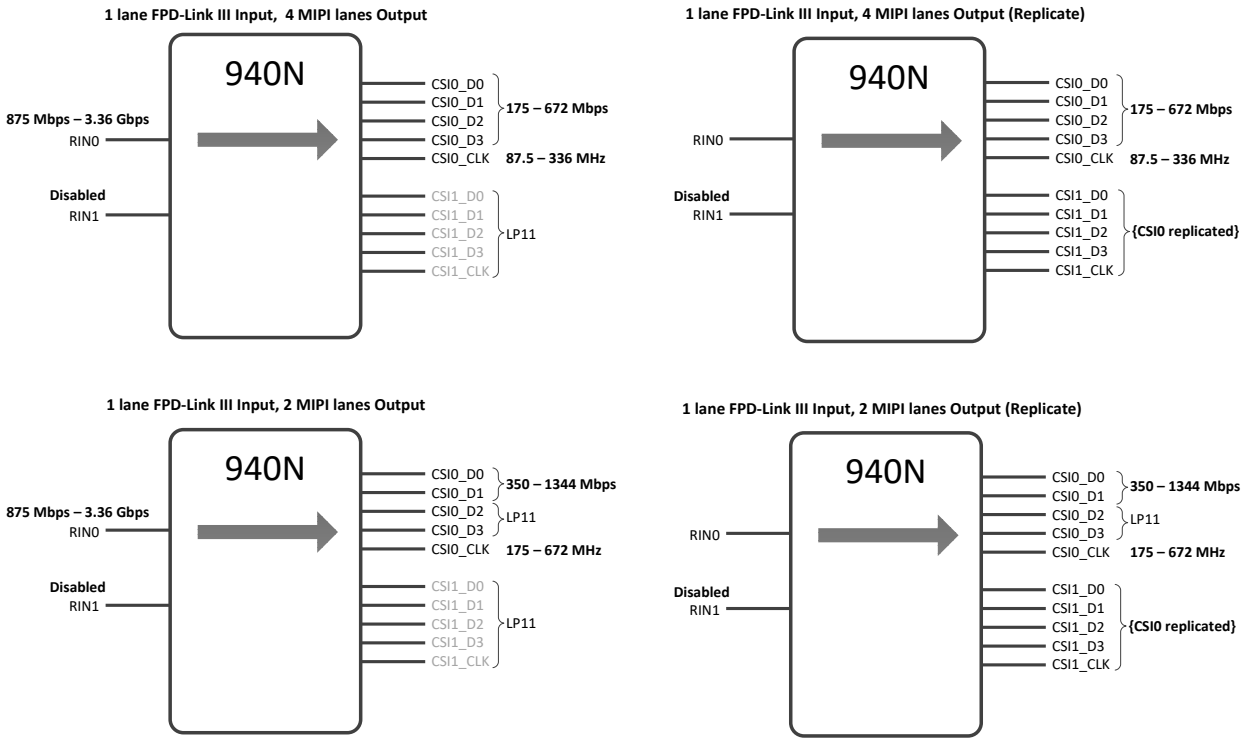


図 28. Data-Path Configurations with 1-Lane FPD-Link III Input

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Device Functional Modes (continued)

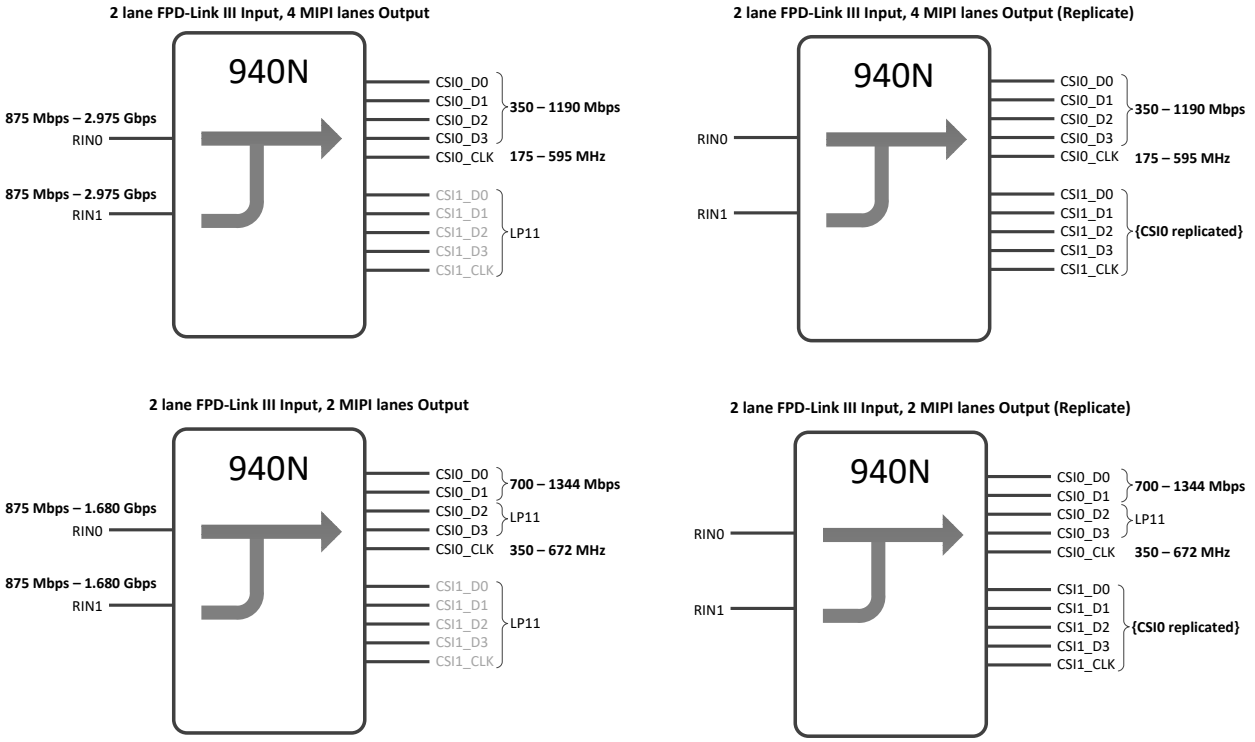


図 29. Data-Path Configurations with 2-Lane FPD-Link III Inputs

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Device Functional Modes (continued)

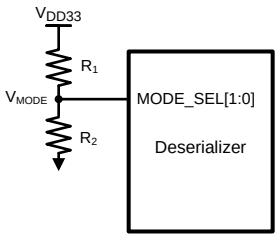


図 30. MODE_SEL[1:0] Connection Diagram

表 7. Configuration Select (MODE_SEL0)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% Tolerance)		OUTPUT MODE
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)	
0	0	0	Open	10	4 data lanes 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit)
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	4 data lanes both CSI ports active (overrides MODE_SEL1)
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	2 data lanes 1 CSI port active (determined by MODE_SEL1 CSI_SEL bit)
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	2 data lanes both CSI port active (overrides MODE_SEL1)
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	RESERVED
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	RESERVED
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	RESERVED
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	RESERVED

表 8. Configuration Select (MODE_SEL1)

NO.	V_{MODE} VOLTAGE	V_{MODE} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% Tolerance)		CSI_SEL (CSI PORT)	HIGH-SPEED BACK CHANNEL	INPUT MODE
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)			
0	0	0	Open	10	CSI0	5 Mbps	STP
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	CSI0	5 Mbps	Coax
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	CSI0	20 Mbps	STP
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	CSI0	20 Mbps	Coax
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	CSI1	5 Mbps	STP
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	CSI1	5 Mbps	Coax
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	CSI1	20 Mbps	STP
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	CSI1	20 Mbps	Coax

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8.4.3 CSI-2 Interface

The DS90UH940N-Q1 (in default mode) takes RGB 24-bpp data bits defined in the serializer and directly maps the bits to the pixel color space in the data frame. The DS90UH940N-Q1 follows the general frame format as described per the CSI-2 standard (図 31). Upon the end of the vertical sync pulse (VS), the DS90UH940N-Q1 generates the frame end and frame start synchronization packets within the vertical blanking period. The timing of the Frame Start will not reflect the timing of the VS signal.

Upon the rising edge of the DE signal, each active line is output in a long data packet with the defined data format (図 13). At the end of each packet, the data lanes Dn± return to the LP-11 state, while the clock lane CLK± continue outputting the high-speed clock.

The DS90UH940N-Q1 CSI-2 transmitter consists of a high-speed clock (CLK±) and data (Dn±) outputs based on a source synchronous interface. The half rate clock at CLK± is derived from the pixel clock sourced by the clock/data recovery circuit of the DS90UH940N-Q1. The CSI-2 clock frequency is 3.5 times (four MIPI lanes) or seven times (two MIPI lanes) the recovered pixel clock frequency. The MIPI DPHY outputs either two or four high-speed data lanes (Dn±) according to the CSI-2 protocol. The data rate of each lane is seven times (four MIPI lanes) or 14 times (two MIPI lanes) the pixel clock. As an example in a 4-MIPI-lane configuration, at a pixel clock of 150 MHz, the CLK± runs at 525 MHz, and each data lane runs at 1050 Mbps.

The half-rate clock maintains a quadrature phase relationship to the data signals and allows receiver to sample data at the rising and falling edges of the clock (DDR). 図 10 shows the timing relationship of the clock and data lines. The DS90UH940N-Q1 supports continuous high-speed clock. High speed data are sent out at data lanes Dn± in bursts. In between data bursts, the data lanes return to low power (LP) states in according to protocol defined in D-PHY standard. The rising edge of the differential clock (CSI_CLK+ – CSI_CLK–) is sent during the first payload bit of a transmission burst in the data lanes.

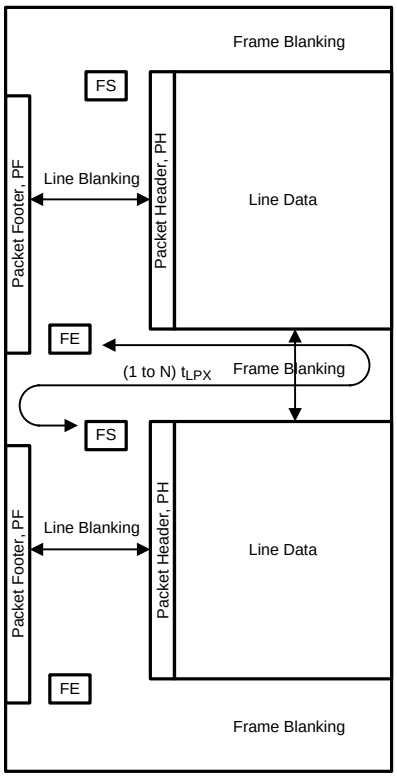


図 31. CSI-2 General Frame Format

8.4.4 Input Display Timing

The DS90UH940N-Q1 has built-in support to detect the incoming video format extracted from the FPD-Link III datastream(s) and automatically generate CSI-2 output timing parameters, accordingly. The input video format detection is derived from progressive display resolutions based on the CEA−861D specification. The video data rate and frame rate is determined by measuring internal VS and DE signals.

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8.4.5 MIPI® CSI-2 Output Data Formats

The DS90UH940N-Q1 CSI-2 Tx supports multiple data types. These can be seen in 表 9.

表 9. CSI-2 Output Data Formats(1)

DATA FORMAT	CSI-2 DATA TYPE [5:0]	Reg0x6B [3:2] IFMT	Reg0x6B [7:4] OFMT	DESCRIPTION
RGB888	0x24	00	0000	RGB888 image data – using 24-bit container for RGB 24-bpp
RGB666	0x23	00	0001	RGB666 image data
RGB565	0x22	00	0010	RGB565 image data
YUV420	0x1A	00	0011	YUV4:2:0 image data, Legacy YUV420 8-bit
YUV420 8-bit	0x18	00	0100	YUV4:2:0 image data
YUV422 8-bit	0x1E	00	0101	YUV4:2:2 image data
RAW8	0x2A	11	0110	RAW Bayer, 8-bit image data D[0:7] of serializer inputs are used as RAW data; alignment is configured with CSIIA_{0x6C}_0x09 [4]
RAW10	0x2B	11	0111	RAW Bayer, 10-bit image data D[0:9] of serializer inputs are used as RAW data; alignment is configured with CSIIA_{0x6C}_0x09 [4]
RAW12	0x2C	11	1000	RAW Bayer, 12-bit image data D[0:11] of serializer inputs are used as RAW data; alignment is configured with CSIIA_{0x6C}_0x09 [4]
YUV420 8-bit (CSPS)	0x1C	00	1001	YUV4:2:0 image data, YUV420 Chroma shifted pixel sampling

(1) Note: Color space conversion is only available from RGB to YUV.

8.4.6 Non-Continuous / Continuous Clock

DS90UH940N-Q1 D-PHY supports Continuous clock mode and Non-Continuous clock mode on the CSI-2 interface. Default mode is Non-Continuous Clock mode, where the Clock Lane enters LP mode between the transmissions of data packets. Non-continuous clock mode will only be non-continuous during the vertical blanking period for lower PCLK rates. For higher PCLK rates, the clock will be non-continuous between line and frame packets. Operating modes are configurable through 0x6A [1].

Clock lane enters LP11 during horizontal blanking if the horizontal blanking period is longer than the overhead time to start/stop the clock lane. There is auto-detection of the length of the horizontal blank period. The fixed threshold is 96 PCLK cycles.

8.4.7 Ultra-Low-Power State (ULPS)

The DS90UH940N-Q1 supports the MIPI defined ultra-low-power state (ULPS). DS90UH940N-Q1 D-PHY lanes enter ULPS mode upon software standby mode through 0x6A [2] generated by the processor. When ULPS is issued, all active CSI-2 lanes including the clock and data lanes of the enabled CSI-2 port are put in ULPS according to the MIPI DPHY protocol. D-PHY can reduce power consumption by entering ULPS mode. ULPS is exited by means of a Mark-1 state with a length TWAKEUP followed by a Stop state.

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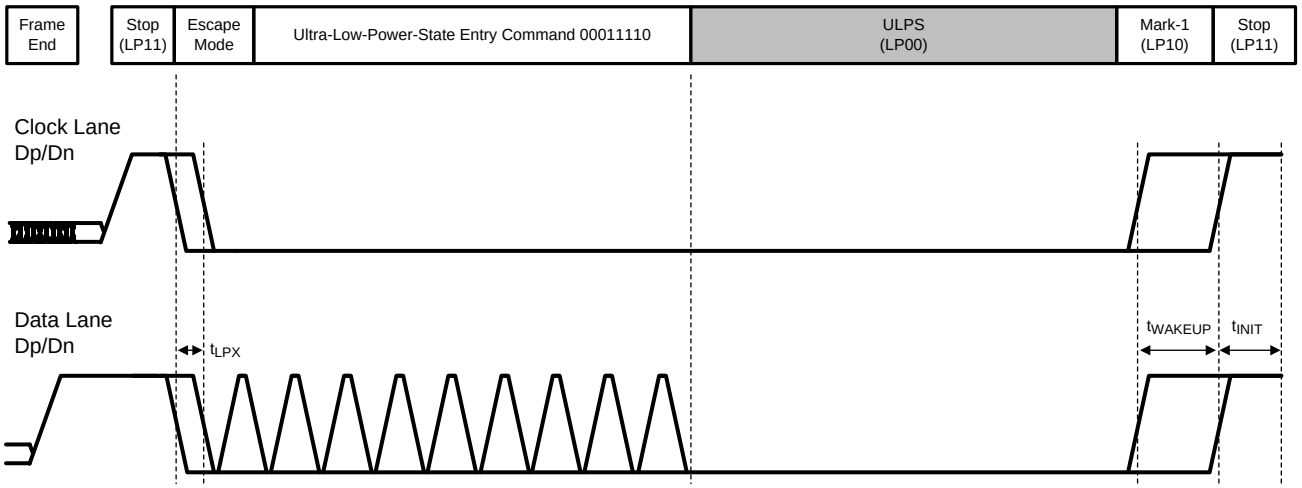


図 32. Ultra-Low-Power State

8.4.8 CSI-2 Data Identifier

The DS90UH940N-Q1 MIPI CSI-2 protocol interface transmits the data identifier byte containing the values for the virtual channel ID (VC) and data type (DT) for the application specific payload data, as shown in 図 33. The virtual channel ID is contained in the two MSBs of the data identifier byte and identify the data as directed to one of four virtual channels. The value of the data type is contained in the 6 LSBs of the data identifier byte.

- CSIIA_{0x6C}_0x2E[7:6] CSI_VC_ID: Configures the virtual ID linked to the current context.
- CSICFG1_0x6B[7:4] OFMT: Configures the data format linked to the current context.

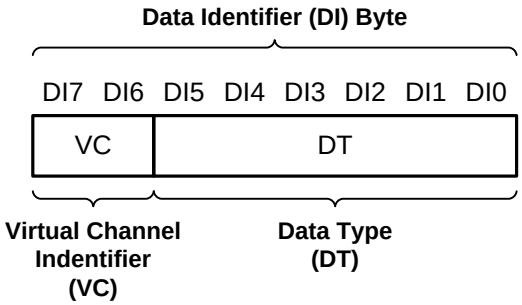


図 33. CSI-2 Data Identifier Structure

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8.5 Programming

8.5.1 Serial Control Bus

The device may also be configured by the use of a I2C-compatible serial control bus. Multiple devices may share the serial control bus (up to eight device addresses supported). The device address is set through a resistor divider (R1 and R2 — see 図 34 below) connected to the IDx pin.

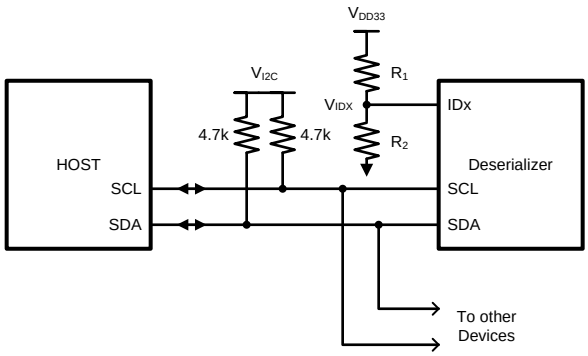


図 34. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a serial bus clock input. SDA is the serial bus data input / output signal. Both SCL and SDA signals require an external pullup resistor to 1.8-V or 3.3-V. For most applications, TI recommends that the user adds a 4.7-kΩ pullup resistor to the 3.3-V rail, however, the pullup resistor value may be adjusted for capacitive loading and data rate requirements. See *I2C Bus Pullup Resistor Calculation* (SLVA689) for more information. The signals are either pulled high or driven low.

The IDx pin configures the control interface to one of eight possible device addresses. A pullup resistor and a pulldown resistor may be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and VDD33, each ratio corresponding to a specific device address. See 表 10 for more information.

表 10. Serial Control Bus Addresses for IDx

NO.	V_{IDX} VOLTAGE	V_{IDX} TARGET VOLTAGE	SUGGESTED STRAP RESISTORS (1% Tolerance)		PRIMARY ASSIGNED I2C ADDRESS	
	V_{TYP}	VDD33 = 3.3 V	R_1 (kΩ)	R_2 (kΩ)	7-BIT	8-BIT
0	0	0	Open	10	0x2C	0x58
1	0.169 x $V_{(VDD33)}$	0.559	73.2	15	0x2E	0x5C
2	0.230 x $V_{(VDD33)}$	0.757	66.5	20	0x30	0x60
3	0.295 x $V_{(VDD33)}$	0.974	59	24.9	0x32	0x64
4	0.376 x $V_{(VDD33)}$	1.241	49.9	30.1	0x34	0x68
5	0.466 x $V_{(VDD33)}$	1.538	46.4	40.2	0x36	0x6C
6	0.556 x $V_{(VDD33)}$	1.835	40.2	49.9	0x38	0x70
7	0.801 x $V_{(VDD33)}$	2.642	18.7	75	0x3C	0x78

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The serial bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SDA transitions low while SCL is high. A STOP occurs when SDA transitions high while SCL is also HIGH. See 図 35.

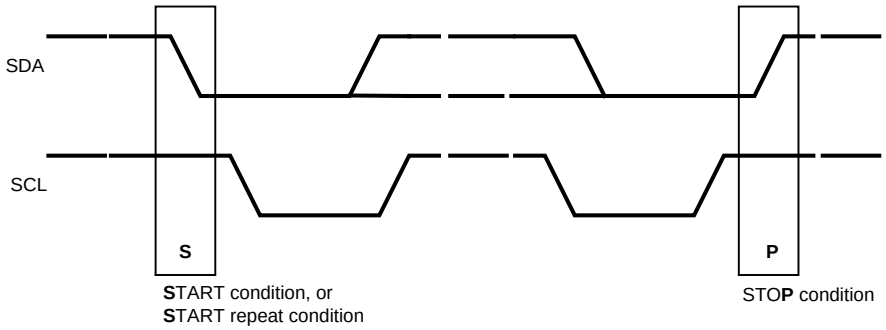


図 35. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it acknowledges (ACKs) the master by driving the SDA bus low. If the address does not match the slave address of a device, the slave not-acknowledges (NACKs) the master by letting the SDA be pulled High. ACKs also occur on the bus when data is transmitted. When the master writes data, the slave sends an ACK after every data byte is successfully received. When the master reads data, the master sends an ACK after every data byte is received to let the slave know that the master is ready to receive another data byte. When the master wants to stop reading, the master sends a NACK after the last data byte to create a stop condition on the bus. All communication on the bus begins with either a start condition or a repeated Start condition. All communication on the bus ends with a stop condition. A READ is shown in 図 36 and a WRITE is shown in 図 37.

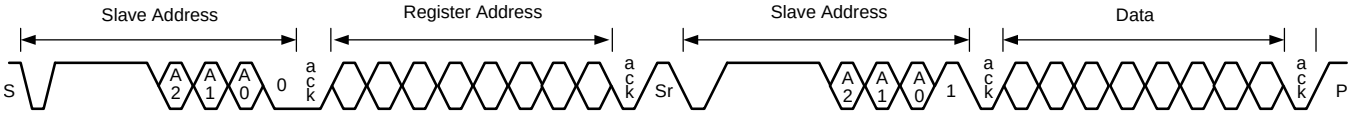


図 36. Serial Control Bus — READ

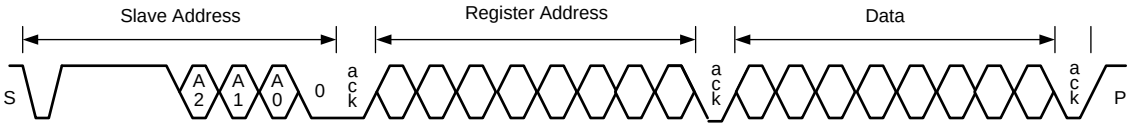


図 37. Serial Control Bus — WRITE

The I2C master located in the deserializer must support I2C clock stretching. For more information on I2C interface requirements and throughput considerations, refer to the *I2C Communication Over FPD-Link III with Bidirectional Control Channel* (SNLA131).

8.5.2 Multi-Master Arbitration Support

The bidirectional control channel in the FPD-Link III devices implements I2C-compatible bus arbitration in the proxy I2C master implementation. When sending a data bit, each I2C master senses the value on the SDA line. If the master sends a logic 1 but senses a logic 0, the master loses arbitration. The master will stop driving SDA and retry the transaction when the bus becomes idle. Thus, multiple I2C masters may be implemented in the system.

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For example, there might also be a local I2C master at each camera. The local I2C master could access the image sensor and EEPROM. The only restriction would be that the remote I2C master at the camera should not attempt to access a remote slave through the BCC that is located at the host controller side of the link. In other words, the control channel should only operate in camera mode for accessing remote slave devices to avoid issues with arbitration across the link. The remote I2C master should also not attempt to access the deserializer registers to avoid a conflict in register access with the Host controller.

If the system does require master-slave operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available R/W registers in the deserializer to allow masters to communicate with each other to pass control between the two masters. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one master to another.

8.5.3 I2C Restrictions on Multi-Master Operation

The I2C specification does not provide for arbitration between masters under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I2C bus:

- One master generates a repeated start while another master is sending a data bit.
- One master generates a stop while another master is sending a data bit.
- One master generates a repeated start while another master sends a stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C slave.

8.5.4 Multi-Master Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices (DS90UH94x-Q1), serializers or deserializer registers may be accessed simultaneously from both local and remote I2C masters. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I2C slaves is still be allowed in only one direction at a time (camera or display mode).

8.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices (in backward compatible mode), simultaneous access to serializer or deserializer registers from both local and remote I2C masters may cause incorrect operation. Thus, restrictions must be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in a read or write error.

TI recommends two basic options:

- Allow device register access only from one controller.

  In a display mode system, this would allow only the host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer (local to the display) would not be allowed to access the deserializer or serializer registers.
- Allow local register access only with no access to remote serializer or deserializer registers.

  The host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I2C slaves would still be allowed in one direction (camera or display mode).

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access is ensured to work correctly if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the bidirectional control channel from one master to another.

8.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only display or camera mode operation should be active at any time across the bidirectional control channel. If both directions are required, some method of transferring control between I2C masters should be implemented.

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8.6 Register Maps

8.6.1 DS90UH940N-Q1 Registers

Table 11 lists the memory-mapped registers for the DS90UH940N-Q1 registers. All register offset addresses not listed in Table 11 should be considered as reserved locations and the register contents should not be modified.

In the register definitions under the *TYPE* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access
- R/RC = Read only access, Read to Clear
- R/W/SC = Read / Write access, Self-Clearing bit
- R/W/S = Read / Write access, Set based on strap pin configuration at start-up
- S = Set based on strap pin configuration at start-up

Table 11. DS90UH940N-Q1 Registers

Address	Acronym	Register Name	Section
0h	I2C_Device_ID		Go
1h	Reset		Go
2h	General_Configuration_0		Go
3h	General_Configuration_1		Go
4h	BCC_Watchdog_Control		Go
5h	I2C_Control_1		Go
6h	I2C_Control_2		Go
7h	REMOTE_ID		Go
8h	SlaveID_0		Go
9h	SlaveID_1		Go
Ah	SlaveID_2		Go
Bh	SlaveID_3		Go
Ch	SlaveID_4		Go
Dh	SlaveID_5		Go
Eh	SlaveID_6		Go
Fh	SlaveID_7		Go
10h	SlaveAlias_0		Go
11h	SlaveAlias_1		Go
12h	SlaveAlias_2		Go
13h	SlaveAlias_3		Go
14h	SlaveAlias_4		Go
15h	SlaveAlias_5		Go
16h	SlaveAlias_6		Go
17h	SlaveAlias_7		Go
18h	MAILBOX_18		Go
19h	MAILBOX_19		Go
1Ah	GPIO_9__Global_GPIO_Config		Go
1Bh	Frequency_Counter		Go
1Ch	General_Status		Go
1Dh	GPIO0_Config		Go
1Eh	GPIO1_2_Config		Go
1Fh	GPIO_3_Config		Go
20h	GPIO_5_6_Config		Go
21h	GPIO_7_8_Config		Go
22h	Datapath_Control		Go

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Table 11. DS90UH940N-Q1 Registers (continued)

Address	Acronym	Register Name	Section
23h	RX_Mode_Status		Go
24h	BIST_Control		Go
25h	BIST_ERROR_COUNT		Go
26h	SCL_High_Time		Go
27h	SCL_Low_Time		Go
28h	Datapath_Control_2		Go
2Bh	I2S_Control		Go
2Eh	PCLK_Test_Mode		Go
34h	DUAL_RX_CTL		Go
35h	AEQ_CTL1		Go
37h	MODE_SEL		Go
3Ah	I2S_DIVSEL		Go
3Bh	Adaptive_EQ_Status		Go
3Dh	General_Status		Go
41h	LINK_ERROR_COUNT		Go
43h	HSCC_CONTROL		Go
44h	ADAPTIVE_EQ_BYPASS		Go
45h	ADAPTIVE_EQ_MIN_MAX		Go
52h	CML_OUTPUT_CTL1		Go
56h	CML_OUTPUT_ENABLE		Go
57h	CML_OUTPUT_CTL2		Go
63h	CML_OUTPUT_CTL3		Go
64h	PGCTL		Go
65h	PGCFG		Go
66h	PGIA		Go
67h	PGID		Go
68h	PGDBG		Go
69h	PGTSTDAT		Go
6Ah	CSICFG0		Go
6Bh	CSICFG1		Go
6Ch	CSIIA		Go
6Dh	CSIID		Go
6Eh	GPIO_Pin_Status_1		Go
6Fh	GPIO_Pin_Status_2		Go
80h	RX_BKSV0		Go
81h	RX_BKSV1		Go
82h	RX_BKSV2		Go
83h	RX_BKSV3		Go
84h	RX_BKSV4		Go
90h	TX_KSV0		Go
91h	TX_KSV1		Go
92h	TX_KSV2		Go
93h	TX_KSV3		Go
94h	TX_KSV4		Go
C0h	HDCP_DBG		Go
C1h	HDCP_DBG2		Go
C4h	HDCP_STS		Go

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Table 11. DS90UH940N-Q1 Registers (continued)

Address	Acronym	Register Name	Section
C9h	KSV_FIFO_DATA		Go
CAh	KSV_FIFO_ADDR0		Go
CBh	KSV_FIFO_ADDR1		Go
E0h	RPTR_TX0		Go
E1h	RPTR_TX1		Go
E2h	RPTR_TX2		Go
E3h	RPTR_TX3		Go
F0h	HDCP_RX_ID0		Go
F1h	HDCP_RX_ID1		Go
F2h	HDCP_RX_ID2		Go
F3h	HDCP_RX_ID3		Go
F4h	HDCP_RX_ID4		Go
F5h	HDCP_RX_ID5		Go

8.6.1.1 I2C_Device_ID Register (Address = 0h) [reset = Strap]

I2C_Device_ID is described in Table 12.

Return to Summary Table.

Table 12. I2C_Device_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	DEVICE_ID	R/W/S	Strap	7-bit address of Deserializer Defaults to address configured by the IDX strap pin. See 表 10.
0	DES_ID	R/W	0h	0: Device ID is from IDX strap 1: Register I2C Device ID overrides IDX strap

8.6.1.2 Reset Register (Address = 1h) [reset = 4h]

Reset is described in Table 13.

Return to Summary Table.

Table 13. Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	1h	Reserved
1	DIGITAL_RESET0	R/W/SC	0h	Digital Reset. Resets the entire digital block including registers. This bit is self-clearing. 1: Reset 0: Normal operation. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show ‘Strap’ as their default value in this table.
0	DIGITAL__RESET1	R/W/SC	0h	Digital Reset. Resets the entire digital block except registers. This bit is self-clearing. 1: Reset 0: Normal operation

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8.6.1.3 General_Configuration_0 Register (Address = 2h) [reset = 0h]

General_Configuration_0 is described in Table 14.

Return to Summary Table.

Table 14. General_Configuration_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUTPUT_ENABLE	R/W	1h	Output Enable Override Value (in conjunction with Output Sleep State Select). If the Override control is not set, the Output Enable will be set to 1. A Digital reset 0x01[0] should be asserted after toggling Output Enable bit *LOW* to *HIGH*
6	OUTPUT_ENABLE_OVERRIDE	R/W	0h	Overrides Output Enable and Output Sleep State default 0: Disable override 1: Enable override
5	OSC_CLOCK_OUTPUT_ENABLE (AUTO_CLOCK_EN)	R/W	0h	OSC Clock Output Enable If there is a loss of lock, OSC clock is output onto PCLK. The frequency is selected in register 0x24. 1: Enable 0: Disable
4	OUTPUT_SLEEP_STATE_SELECT	R/W	0h	OSS Select Override value to control output state when LOCK is low (used in conjunction with Output Enable). If the Override control is not set, the Output Sleep State Select will be set to 1.
3	RESERVED	R/W	0h	Reserved
2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.6.1.4 General_Configuration_1 Register (Address = 3h) [reset = F0h]

General_Configuration_1 is described in Table 15.

Return to Summary Table.

Table 15. General_Configuration_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	1h	Reserved
6	BC_CRC_GENERATOR_ENABLE	R/W	1h	Back Channel CRC Generator Enable 0: Disable 1: Enable
5	FAILSAFE_LOW	R/W	1h	Controls the pull direction for undriven LVCMOS inputs 1: Pull down 0: Pull up
4	FILTER_ENABLE	R/W	1h	HS,VS,DE two clock filter (FPD-Link III 1-Lane Mode) or four clock filter (FPD-Link III 2-Lane Mode) When enabled, pulses less than two full PCLK cycles in 1-Lane mode (or less than four full PCLK cycles in 2-Lane mode) on the DE, HS, and VS inputs will be rejected. 1: Filtering enable 0: Filtering disable
3	I2C_PASS-THROUGH	R/W	0h	I2C Pass-Through to Serializer if decode matches 0: Pass-Through Disabled 1: Pass-Through Enabled
2	AUTO_ACK	R/W	0h	Automatically Acknowledge I2C writes independent of the forward channel lock state 1: Enable 0: Disable

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Table 15. General_Configuration_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	DE_GATE_RGB	R/W	0h	Gate RGB data with DE signal. RGB data is gated with DE in order to allow packetized audio and block unencrypted data when paired with a serializer that supports HDCP. When paired with a serializer that does not support HDCP, RGB data is not gated with DE by default. However, to enable packetized autio this bit must be set. 1: Gate RGB data with DE (has no effect when paired with a serializer that supports HDCP) 0: Pass RGB data independent of DE (has no effect when paired with a serializer that does not support HDCP)
0	RESERVED	R/W	0h	Reserved

8.6.1.5 BCC_Watchdog_Control Register (Address = 4h) [reset = FEh]

BCC_Watchdog_Control is described in Table 16.

Return to Summary Table.

Table 16. BCC_Watchdog_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	BCC_WATCHDOG_TIMER	R/W	7Fh	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
0	BCC_WATCHDOG_TIMER_DISABLE	R/W	0h	Disable Bidirectional Control Channel Watchdog Timer 1: Disables BCC Watchdog Timer operation 0: Enables BCC Watchdog Timer operation

8.6.1.6 I2C_Control_1 Register (Address = 5h) [reset = 1Eh]

I2C_Control_1 is described in Table 17.

Return to Summary Table.

Table 17. I2C_Control_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	I2C_PASS_THROUGH_ALL	R/W	0h	I2C Pass-Through All Transactions 0: Disabled 1: Enabled
6-4	I2C_SDA_HOLD		1h	Internal SDA Hold Time This field configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 50 nanoseconds.
3-0	I2C_FILTER_DEPTH		Eh	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

8.6.1.7 I2C_Control_2 Register (Address = 6h) [reset = 0h]

I2C_Control_2 is described in Table 18.

Return to Summary Table.

Table 18. I2C_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FORWARD_CHANNEL_SEQUENCE_ERROR	R	0h	Control Channel Sequence Error Detected This bit indicates a sequence error has been detected in forward control channel. If this bit is set, an error may have occurred in the control channel operation.

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Table 18. I2C_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	CLEAR_SEQUENCE _ERROR	R/W	0h	Clears the Sequence Error Detect bit
5	RESERVED	R	0h	Reserved
4-3	SDA_Output_Delay	R/W	0h	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00 : 250ns 01: 300ns 10: 350ns 11: 400ns
2	LOCAL_WRITE_DISABLE	R/W	0h	Disable Remote Writes to Local Registers Setting this bit to a 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Deserializer registers from an I2C master attached to the Serializer. Setting this bit does not affect remote access to I2C slaves at the Deserializer.
1	I2C_BUS_TIMER _SPEEDUP	R/W	0h	Speed up I2C Bus Watchdog Timer 1: Watchdog Timer expires after approximately 50 microseconds 0: Watchdog Timer expires after approximately 1 second.
0	I2C_BUS_TIMER _DISABLE	R/W	0h	Disable I2C Bus Watchdog Timer When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signalling occurs for approximately 1 second, the I2C bus will assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL

8.6.1.8 REMOTE_ID Register (Address = 7h) [reset = 0h]

REMOTE_ID is described in Table 19.

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Table 19. REMOTE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	REMOTE_ID	R/W	0h	7-bit Serializer Device ID Configures the I2C Slave ID of the remote Serializer. A value of 0 in this field disables I2C access to the remote Serializer. This field is automatically loaded from the Serializer once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent loading by the Bidirectional Control Channel.
0	FREEZE_DEVICE_ID	R/W	0h	Freeze Serializer Device ID Prevent auto-loading of the Serializer Device ID from the Forward Channel. The ID will be frozen at the value written.

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8.6.1.9 SlaveID_0 Register (Address = 8h) [reset = 0h]

SlaveID_0 is described in Table 20.

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Table 20. SlaveID_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID0	R/W	0h	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.10 SlaveID_1 Register (Address = 9h) [reset = 0h]

SlaveID_1 is described in Table 21.

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Table 21. SlaveID_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID1	R/W	0h	7-bit Remote Slave Device ID 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.11 SlaveID_2 Register (Address = Ah) [reset = 0h]

SlaveID_2 is described in Table 22.

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Table 22. SlaveID_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID2	R/W	0h	7-bit Remote Slave Device ID 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.12 SlaveID_3 Register (Address = Bh) [reset = 0h]

SlaveID_3 is described in Table 23.

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Table 23. SlaveID_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID3	R/W	0h	7-bit Remote Slave Device ID 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.

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Table 23. SlaveID_3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	RESERVED	R/W	0h	Reserved.

8.6.1.13 SlaveID_4 Register (Address = Ch) [reset = 0h]

SlaveID_4 is described in Table 24.

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Table 24. SlaveID_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID4	R/W	0h	7-bit Remote Slave Device ID 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.14 SlaveID_5 Register (Address = Dh) [reset = 0h]

SlaveID_5 is described in Table 25.

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Table 25. SlaveID_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID5	R/W	0h	7-bit Remote Slave Device ID 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.15 SlaveID_6 Register (Address = Eh) [reset = 0h]

SlaveID_6 is described in Table 26.

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Table 26. SlaveID_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID6	R/W	0h	7-bit Remote Slave Device ID 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

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8.6.1.16 SlaveID_7 Register (Address = Fh) [reset = 0h]

SlaveID_7 is described in Table 27.

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Table 27. SlaveID_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ID7	R/W	0h	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
0	RESERVED	R/W	0h	Reserved

8.6.1.17 SlaveAlias_0 Register (Address = 10h) [reset = 0h]

SlaveAlias_0 is described in Table 28.

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Table 28. SlaveAlias_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID0	R/W	0h	7-bit Remote Slave Device Alias ID 0 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID0 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.18 SlaveAlias_1 Register (Address = 11h) [reset = 0h]

SlaveAlias_1 is described in Table 29.

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Table 29. SlaveAlias_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID1	R/W	0h	7-bit Remote Slave Device Alias ID 1 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID1 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.19 SlaveAlias_2 Register (Address = 12h) [reset = 0h]

SlaveAlias_2 is described in Table 30.

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Table 30. SlaveAlias_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID2	R/W	0h	7-bit Remote Slave Device Alias ID 2 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID2 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

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8.6.1.20 SlaveAlias_3 Register (Address = 13h) [reset = 0h]

SlaveAlias_3 is described in Table 31.

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Table 31. SlaveAlias_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID3	R/W	0h	7-bit Remote Slave Device Alias ID 3 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID3 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.21 SlaveAlias_4 Register (Address = 14h) [reset = 0h]

SlaveAlias_4 is described in Table 32.

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Table 32. SlaveAlias_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID4	R/W	0h	7-bit Remote Slave Device Alias ID 4 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID4 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.22 SlaveAlias_5 Register (Address = 15h) [reset = 0h]

SlaveAlias_5 is described in Table 33.

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Table 33. SlaveAlias_5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID5	R/W	0h	7-bit Remote Slave Device Alias ID 5 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID5 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.23 SlaveAlias_6 Register (Address = 16h) [reset = 0h]

SlaveAlias_6 is described in Table 34.

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Table 34. SlaveAlias_6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID6	R/W	0h	7-bit Remote Slave Device Alias ID 6 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID6 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

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8.6.1.24 SlaveAlias_7 Register (Address = 17h) [reset = 0h]

SlaveAlias_7 is described in Table 35.

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Table 35. SlaveAlias_7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	SLAVE_ALIAS_ID7	R/W	0h	7-bit Remote Slave Device Alias ID 7 Configures the decoder for detecting transactions designated for an I2C Slave device attached to the remote Serializer. The transaction will be remapped to the address specified in the Slave ID7 register. A value of 0 in this field disables access to the remote I2C Slave.
0	RESERVED	R	0h	Reserved

8.6.1.25 MAILBOX_18 Register (Address = 18h) [reset = 0h]

MAILBOX_18 is described in Table 36.

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Table 36. MAILBOX_18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_18	R/W	0h	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

8.6.1.26 MAILBOX_19 Register (Address = 19h) [reset = 1h]

MAILBOX_19 is described in Table 37.

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Table 37. MAILBOX_19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAILBOX_19	R/W	1h	Mailbox Register This register is an unused read/write register that can be used for any purpose such as passing messages between I2C masters on opposite ends of the link.

8.6.1.27 GPIO_9__Global_GPIO_Config Register (Address = 1Ah) [reset = 0h]

GPIO_9__Global_GPIO_Config is described in Table 38.

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Table 38. GPIO_9__Global_GPIO_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GLOBAL_GPIO _OUTPUT_VALUE	R/W	0h	Global GPIO Output Value This value is output on each GPIO pin when the individual pin is not otherwise enabled as a GPIO and the global GPIO direction is Output
6	RESERVED	R/W	0h	Reserved
5	GLOBAL_GPIO _FORCE_DIR	R/W	0h	The GLOBAL GPIO DIR and GLOBAL GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. The GLOBAL bits are overridden by the individual GPIO DIR and GPIO EN bits. {GLOBAL GPIO DIR, GLOBAL GPIO EN} 00: Functional mode; output 10: Tri-state 01: Force mode; output 11: Force mode; input

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Table 38. GPIO_9__Global_GPIO_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	GLOBAL_GPIO _FORCE_EN	R/W	0h	
3	GPIO9_OUTPUT_VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	RESERVED	R/W	0h	Reserved
1	GPIO9_DIR	R/W	0h	The GPIO DIR bits configure the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO9_EN	R/W	0h	The GPIO EN bits configure the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

8.6.1.28 Frequency_Counter Register (Address = 1Bh) [reset = 0h]

Frequency_Counter is described in Table 39.

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Table 39. Frequency_Counter Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Frequency_Count	R/W	0h	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 40ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

8.6.1.29 General_Status Register (Address = 1Ch) [reset = 0h]

General_Status is described in Table 40.

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Table 40. General_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	DUAL_RX_STS	R	0h	Receiver Dual Link Status: This bit indicates the current operating mode of the FPD-Link III Receive port 1: Dual-link mode active 0: Single-link mode active
3	I2S_LOCKED	R	0h	I2S LOCK STATUS 0: I2S PLL controller not locked 1: I2S PLL controller locked to input i2s clock
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h or 1h	Reserved

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Table 40. General_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	LOCK	R	0h	De-Serializer CDR, PLL's clock to recovered clock frequency 1: De-Serializer locked to recovered clock 0: De-Serializer not locked In Dual-link mode, this indicates both channels are locked.

8.6.1.30 GPIO0_Config Register (Address = 1Dh) [reset = 0h]

GPIO0_Config is described in Table 41.

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GPIO0 and D_GPIO0 Configuration
If PORT1_SEL is set, this register controls the D_GPIO0 pin.

Table 41. GPIO0_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	Rev-ID	R	0h	Revision ID 0100: DS90UH940-Q1 0110: DS90UH940N-Q1
3	GPIO0_OUTPUT _VALUE _D_GPIO0_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO0_REMOTE _ENABLE _D_GPIO0_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO0_DIR _D_GPIO0_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO0_EN _D_GPIO0_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

8.6.1.31 GPIO1_2_Config Register (Address = 1Eh) [reset = 0h]

GPIO1_2_Config is described in Table 42.

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GPIO1 / GPIO2 and D_GPIO1 / D_GPIO2 Configuration
If PORT1_SEL is set, this register controls the D_GPIO1 / D_GPIO2 pin.

Table 42. GPIO1_2_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO2_OUTPUT _VALUE _D_GPOI2_OUTPUT _VALUE	R/W	0h	GPIO1/GPIO2 and D_GPIO1/D_GPIO2 Configuration If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.

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Table 42. GPIO1_2_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	GPIO2_REMOTE _ENABLE _D_GPIO2_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
5	GPIO2_DIR _D_GPIO2_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO2_EN _D_GPIO2_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
3	GPIO1_OUTPUT _VALUE _D_GPIO1_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO1_REMOTE _ENABLE _D_GPIO1_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO1_DIR _D_GPIO1_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO1_EN _D_GPIO1_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

8.6.1.32 GPIO_3_Config Register (Address = 1Fh) [reset = 0h]

GPIO_3_Config is described in Table 43.

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GPIO3 and D_GPIO3 Configuration
If PORT1_SEL is set, this register controls the D_GPIO3 pin.

Table 43. GPIO_3_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved (No GPIO4)
3	GPIO3_OUTPUT _VALUE _D_GPIO3_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO3_REMOTE _ENABLE _D_GPIO3_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.

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Table 43. GPIO_3_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	GPIO3_DIR _D_GPIO3_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	GPIO3_EN _D_GPIO3_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

8.6.1.33 GPIO_5_6_Config Register (Address = 20h) [reset = 0h]

GPIO_5_6_Config is described in Table 44.

Return to Summary Table.

Table 44. GPIO_5_6_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO6_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
6	GPIO6_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
5	GPIO6_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO6_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
3	GPIO5_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO5_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO5_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

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Table 44. GPIO_5_6_Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	GPIO5_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input

8.6.1.34 GPIO_7_8_Config Register (Address = 21h) [reset = 0h]

GPIO_7_8_Config is described in Table 45.

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Table 45. GPIO_7_8_Config Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO8_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
6	GPIO8_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
5	GPIO8_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
4	GPIO8_EN	R/W	0h	The GPIO EN configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
3	GPIO7_OUTPUT _VALUE	R/W	0h	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled.
2	GPIO7_REMOTE _ENABLE	R/W	0h	Remote GPIO Control 1: Enable GPIO control from remote Serializer. The GPIO pin will be an output, and the value is received from the remote Serializer. 0: Disable GPIO control from remote Serializer.
1	GPIO7_DIR	R/W	0h	The GPIO DIR configures the pad in input direction or output direction for functional mode or GPIO mode. 00: Functional mode; output 10: Tri-state 01: GPIO mode; output 11: GPIO mode; input
0	RESERVED	R/W	0h	Reserved

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8.6.1.35 Datapath_Control Register (Address = 22h) [reset = 0h]

Datapath_Control is described in Table 46.

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Table 46. Datapath_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVERRIDE_FC_CONFIG	R/W	0h	1: Disable loading of this register from the forward channel, keeping locally witten values intact 0: Allow forward channel loading of this register
6	PASS_RGB	R/W	0h	Setting this bit causes RGB data to be sent independent of DE. This allows operation in systems which may not use DE to frame video data or send other data when DE is deasserted. Note that setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in DS90UB928 or in Backward Compatibility mode. 1: Pass RGB independent of DE 0: Normal operation Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
5	DE_POLARITY	R/W	0h	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high) 0: DE is positive (active high, idle low) Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
4	I2S_RPTR_REGEN	R/W	0h	This bit controls whether the HDCP Receiver outputs packetized Auxiliary/Audio data on the RGB video output pins. 1: Don't output packetized audio data on RGB video output pins 0: Output packetized audio on RGB video output pins. Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
3	I2S_4-CHANNEL _ENABLE_OVERRIDE	R/W	0h	1: Set I2S 4-Channel Enable from bit of of this register 0: Set I2S 4-Channel disabled Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
2	18-BIT_VIDEO_SELECT	R/W	0h	1: Select 18-bit video mode 0: Select 24-bit video mode Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
1	I2S_TRANSPORT _SELECT	R/W	0h	1: Enable I2S In-Band Transport 0: Enable I2S Data Island Transport Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.
0	I2S_4-CHANNEL _ENABLE	R/W	0h	I2S 4-Channel Enable 1: Enable I2S 4-Channel 0: Disable I2S 4-Channel Note: this bit is automatically loaded from the remote serializer unless bit 7 of this register is set.

8.6.1.36 RX_Mode_Status Register (Address = 23h) [reset = Strap]

RX_Mode_Status is described in Table 47.

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Table 47. RX_Mode_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RX_RGB_CHECKSUM	R/W	0h	RX RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the HDCP_STS register.

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Table 47. RX_Mode_Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	BC_FREQ_SELECT	R/W	0h	Back Channel Frequency Select 0: Divide-by-4 frequency based on the OSC CLOCK DIVIDER in Register 0x32 1: Divide-by-2 frequency based on the OSC CLOCK DIVIDER in Register 0x32 This bit will be ignored if BC_HIGH_SPEED is set to a 1. Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer.
5	AUTO_I2S	R/W	1h	Auto I2S Determine I2S mode from the AUX data codes.
4	BC_HIGH_SPEED	R/W/S	Strap	Back-Channel High-Speed control Enables high-speed back-channel at 20Mbps This bit will override the BC_FREQ_SELECT setting Note that changing this setting will result in some errors on the back channel for a short period of time. If set over the control channel, the Serializer should first be programmed to Auto-Ack operation (Serializer register 0x03, bit 5) to avoid a control channel timeout due to lack of response from the Deserializer. BC_HIGH_SPEED is loaded from the MODE_SEL1 pin strap options.
3	COAX_MODE	R/W/S	Strap	Coax Mode Configures the FPD3 Receiver for operation over Coax or STP cabling: 0 : Shielded Twisted pair (STP) 1 : Coax Coax Mode is loaded from the MODE_SEL1 pin strap options.
2	REPEATER_MODE	R/S	Strap	Repeater Mode Indicates device is strapped to repeater mode. Repeater Mode is loaded from the MODE_SEL1 pin strap options.
1	RESERVED	R/W	0h	Reserved
0	RESERVED	R/W	0h	Reserved

8.6.1.37 BIST_Control Register (Address = 24h) [reset = 8h]

BIST_Control is described in Table 48.

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Table 48. BIST_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R/W	0h	Reserved
5-4	AUTO_OSC_FREQ	R/W	0h	When register 0x02 bit 5 (AUTO)CLOCK_EN) is set, this field controls the nominal frequency of the oscillator-based receive clock. 00: 50 MHz 01: 25 MHz 10: 10 MHz 11: Reserved
3	BIST_PIN_CONFIG	R/W	1h	Bist Configured through Pin. 1: Bist configured through pin. 0: Bist configured through bits 2:0 in this register
2-1	BIST_CLOCK_SOURCE	R/W	0h	BIST Clock Source This register field selects the BIST Clock Source at the Serializer. These register bits are automatically written to the CLOCK SOURCE bits (register offset 0x14) in the Serializer after BIST is enabled. See the appropriate Serializer register descriptions for details. 00: External Pixel Clock 01: Internal Pixel Clock 1x: Internal Pixel Clock

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Table 48. BIST_Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	BIST_EN	R/W	0h	BIST Control 1: Enabled 0: Disabled

8.6.1.38 BIST_ERROR_COUNT Register (Address = 25h) [reset = 0h]

BIST_ERROR_COUNT is described in Table 49.

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Table 49. BIST_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIST_ERROR_COUNT	R	0h	Bist Error Count

8.6.1.39 SCL_High_Time Register (Address = 26h) [reset = 83h]

SCL_High_Time is described in Table 50.

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Table 50. SCL_High_Time Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCL_HIGH_TIME	R/W	83h	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.

8.6.1.40 SCL_Low_Time Register (Address = 27h) [reset = 84h]

SCL_Low_Time is described in Table 51.

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Table 51. SCL_Low_Time Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SCL_LOW_TIME	R/W	84h	I2C SCL Low Time This field configures the low pulse width of the SCL output when the De-Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26 MHz rather than the nominal 20 MHz.

8.6.1.41 Datapath_Control_2 Register (Address = 28h) [reset = Loaded from SER]

Datapath_Control_2 is described in Table 52.

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Table 52. Datapath_Control_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OVERRIDE_FC_CONFIG	R/W	0h	1: Disable loading of this register from the forward channel, keeping locally witten values intact 0: Allow forward channel loading of this register
6	RESERVED	R/W	0h	Reserved

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Table 52. Datapath_Control_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	VIDEO_DISABLED	R/W	Loaded from SER	Forward channel video disabled (Load from remote Serializer) 0 : Normal operation 1 : Video is disabled, control channel is enabled This is a status bit indicating the forward channel is not sending active video. In this mode, the control channel and GPIO functions are enabled. Setting OVERRIDE_FC_CONFIG will prevent this bit from changing.
4	DUAL_LINK	R	Loaded from SER	1: Dual-Link mode enabled 0: Single-Link mode enabled This bit indicates whether the FPD-Link III serializer is in single link or dual link mode. This control is used for recovering forward channel data when the FPD-Link III Receiver is in auto-detect mode. This bit will always be loaded from forward channel and cannot be written locally. To force DUAL_LINK receive mode, use the RX_PORT_SEL register (address 0x34)
3	ALTERNATE_I2S _ENABLE	R/W	Loaded from SER	1: Enable alternate I2S output on GPIO1 (word clock) and GPIO0 (data) 0: Normal Operation
2	I2S_DISABLED	R/W	Loaded from SER	1: I2S DISABLED 0: Normal Operation
1	28BIT_VIDEO	R/W	Loaded from SER	1: 28 bit Video enable. i.e. HS, VS, DE are present in forward channel. 0: Normal Operation
0	I2S_SURROUND	R/W	Loaded from SER	1: I2S Surround enabled 0: I2S Surround disabled

8.6.1.42 I2S_Control Register (Address = 2Bh) [reset = 0h]

I2S_Control is described in Table 53.

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Table 53. I2S_Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3	I2S_FIFO _OVERRUN_STATUS	R	0h	I2S FIFO Overrun Status
2	I2S_FIFO _UNDERRUN_STATUS	R	0h	I2S FIFO Underrun Status
1	I2S_FIFO _ERROR_RESET	R/W	0h	I2S Fifo Error Reset 1: Clears FIFO Error
0	I2S_DATA _FALLING_EDGE	R/W	0h	I2S Clock Edge Select 1: I2S Data is strobed on the Rising Clock Edge. 0: I2S Data is strobed on the Falling Clock Edge.

8.6.1.43 PCLK_Test_Mode Register (Address = 2Eh) [reset = 0h]

PCLK_Test_Mode is described in Table 54.

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Table 54. PCLK_Test_Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EXTERNAL_PCLK	R/W	0h	Select pixel clock from BISTC input
6-0	RESERVED	R/W	0h	Reserved

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8.6.1.44 DUAL_RX_CTL Register (Address = 34h) [reset = 1h]

DUAL_RX_CTL is described in Table 55.

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Table 55. DUAL_RX_CTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	RX_LOCK_MODE	R/W	0h	RX Lock Mode: Determines operating conditions for indication of RX_LOCK and generation of video data. 0 : RX_LOCK asserted only when receiving active video (Forward channel VIDEO_DISABLED bit is 0) 1 : RX_LOCK asserted when device is linked to a Serializer even if active video is not being sent. This allows indication of valid link where Bidirectional Control Channel is enabled, but Deserializer is not receiving Audio/Video data.
5	RAW_2ND_BC	R/W	0h	Enable Raw Secondary Back channel if this bit is set to a 1, the secondary back channel will operate in a raw mode, passing D_GPIO0 from the Deserializer to the Serializer, without any oversampling or filtering.
4-3	FPD3_INPUT_MODE	R/W	0h	FPD-Link III Input Mode Determines operating mode of dual FPD-Link III Receive interface 00: Auto-detect based on received data 01: Forced Mode: Dual link 10: Forced Mode: Single link, primary input 11: Forced Mode: Single link, secondary input
2	RESERVED	R/W	0h	Reserved
1	PORT1_SEL	R/W	0h	Selects Port 1 for Register Access from primary I2C Address For writes, port1 registers and shared registers will both be written. For reads, port1 registers and shared registers will be read. This bit must be cleared to read port0 registers.
0	PORT0_SEL	R/W	1h	Selects Port 0 for Register Access from primary I2C Address For writes, port0 registers and shared registers will both be written. For reads, port0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then port1 registers will be read.

8.6.1.45 AEQ_CTL1 Register (Address = 35h) [reset = 0h]

AEQ_CTL1 is described in Table 56.

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Table 56. AEQ_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	AEQ_RESTART	R/W	0h	Set high to restart AEQ adaptation from initial value. Method is write HIGH then write LOW - not self clearing. Adaption will be restarted on both ports.
5	OVERRIDE_AEQ _FLOOR	R/W	0h	Enable operation of SET_AEQ_FLOOR
4	SET_AEQ_FLOOR	R/W	0h	Enable the ADAPTIVE_EQ_FLOOR_VALUE set in the AEQ_CTL2 register 0x45.
3-0	RESERVED	R/W	0h	Reserved

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8.6.1.46 MODE_SEL Register (Address = 37h) [reset = 0h]

MODE_SEL is described in Table 57.

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Table 57. MODE_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MODE1_DONE	R	0h	MODE_SEL1 Done: If set, indicates the MODE_SEL1 decode has completed and latched into the MODE_SEL1 status bits.
6-4	MODE_SEL1	R	0h	MODE_SEL1 Decode 3-bit decode from MODE_SEL1 pin
3	MODE0_DONE	R	0h	MODE_SEL0 Done: If set, indicates the MODE_SEL0 decode has completed and latched into the MODE_SEL0 status bits.
2-0	MODE_SEL0	R	0h	MODE_SEL0 Decode 3-bit decode from MODE_SEL0 pin

8.6.1.47 I2S_DIVSEL Register (Address = 3Ah) [reset = 0h]

I2S_DIVSEL is described in Table 58.

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Table 58. I2S_DIVSEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REG_OV_MDIV	R/W	0h	0: No override for MCLK divider 1: Override divider select for MCLK
6-4	REG_MDIV	R/W	0h	Divide ratio select for VCO output (32*REF/M) 000: Divide by 32 (=REF/M) 001: Divide by 16 (=2*REF/M) 010: Divide by 8 (=4*REF/M) 011: Divide by 4 (=8*REF/M) 100, 101: Divide by 2 (=16*REF/M) 110, 111: Divide by 1 (32*REF/M)
3	RESERVED	R	0h	Reserved
2	REG_OV_MSELECT	R/W	0h	0: Divide ratio of reference clock VCO selected by PLL-SM 1: Override divide ratio of clock to VCO
1-0	REG_MSELECT	R/W	0h	Divide ratio select for VCO input (M) 00: Divide by 1 01: Divide by 2 10: Divide by 4 11: Divide by 8

8.6.1.48 Adaptive_EQ_Status Register (Address = 3Bh) [reset = 0h]

Adaptive_EQ_status is described in Table 59.

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Table 59. Adaptive_EQ_Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0h	Reserved
5-0	EQ_STATUS	R	0h	Adaptive EQ Status

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8.6.1.49 LINK_ERROR_COUNT Register (Address = 41h) [reset = 3h]

LINK_ERROR_COUNT is described in Table 60.

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Table 60. LINK_ERROR_COUNT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	Reserved
4	LINK_ERROR_COUNT _ENABLE	R/W	0h	Enable serial link data integrity error count 1: Enable error count 0: DISABLE
3-0	LINK_ERROR_COUNT	R/W	3h	Link error count threshold. Counter is pixel clock based. clk0, clk1 and DCA are monitored for link errors, if error count is enabled, deserializer loose lock once error count reaches threshold. If disabled, Deserializer loses lock with one error.

8.6.1.50 HSCC_CONTROL Register (Address = 43h) [reset = 0h]

HSCC_CONTROL is described in Table 61.

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Table 61. HSCC_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0h	Reserved
4	SPI_MISO_MODE	R/W	0h	SPI MISO pin mode during Reverse SPI mode During Reverse SPI mode, SPI_MISO is typically an output signal. For bused SPI applications, it may be necessary to tri-state the SPI_MISO output if the device is not selected (SPI_SS = 0). 0 : Always enable SPI_MISO output driver 1 : Tri-state SPI_MISO output if SPI_SS is not asserted (low)
3	SPI_CPOL	R/W	0h	SPI Clock Polarity Control 0 : SPI Data driven on Falling clock edge, sampled on Rising clock edge 1 : SPI Data driven on Rising clock edge, sampled on Falling clock edge
2-0	HSCC_MODE	R/W	0h	High-Speed Control Channel Mode Enables high-speed modes for the secondary link back-channel, allowing higher speed signaling of GPIOs or SPI interface: These bits indicates the High Speed Control Channel mode of operation: 000: Normal frame, GPIO mode 001: High Speed GPIO mode, 1 GPIO 010: High Speed GPIO mode, 2 GPIOs 011: High Speed GPIO mode: 4 GPIOs 100: Normal frame, Forward Channel SPI mode 101: Normal frame, Reverse Channel SPI mode 110: High Speed, Forward Channel SPI mode 111: High Speed, Reverse Channel SPI mode

8.6.1.51 ADAPTIVE_EQ_BYPASS Register (Address = 44h) [reset = 60h]

ADAPTIVE_EQ_BYPASS is described in Table 62.

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Table 62. ADAPTIVE_EQ_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	EQ_STAGE_1 _SELECT_VALUE	R/W	3h	EQ select value[5:3] - Used if adaptive EQ is bypassed.
4	RESERVED	R/W	0h	Reserved.

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Table 62. ADAPTIVE_EQ_BYPASS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	EQ_STAGE_2 _SELECT_VALUE	R/W	0h	EQ select value [2:0] - Used if adaptive EQ is bypassed.
0	ADAPTIVE_EQ _BYPASS	R/W	0h	1: Disable adaptive EQ 0: Enable adaptive EQ

8.6.1.52 AEQ_CTL2 Register (Address = 45h) [reset = 88h]

AEQ_CTL2 is described in Table 63.

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If PORT1_SEL is set, this register sets Port1 AEQ configuration

Table 63. AEQ_CTL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved
3-0	ADAPTIVE_EQ _FLOOR_VALUE	R/W	8h	AEQ adaptation starts from a pre-set floor value rather than from zero - good in long cable situations.

8.6.1.53 CML_OUTPUT_CTL1 Register (Address = 52h) [reset = 0h]

areg12_2 is described in Table 64.

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Table 64. CML_OUTPUT_CTL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CML_CHANNEL _SELECT_1	R/W	0h	Selects between PORT0 and PORT1 to output onto CMLOUT±. 0: Recovered forward channel data from RIN0± is output on CMLOUT± 1: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This bit must match 0x57[2:1] setting for PORT0 or PORT1.
6-0	RESERVED	R/W	0h	Reserved

8.6.1.54 CML_OUTPUT_ENABLE Register (Address = 56h) [reset = 0h]

CML_OUTPUT_ENABLE is described in Table 65.

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Table 65. CML_OUTPUT_ENABLE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved.
3	CMLOUT_ENABLE	R/W	0h	Enable CMLOUT± Loop-through Driver 0: Disabled (Default) 1: Enabled
2-0	RESERVED	R/W	0h	Reserved.

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8.6.1.55 CML_OUTPUT_CTL2 Register (Address = 57h) [reset = 0h]

CML_OUTPUT_CTL2 is described in Table 66.

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Table 66. CML_OUTPUT_CTL2 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved.
2-1	CML_CHANNEL_SELECT_2	R/W	0h	Selects between PORT0 and PORT1 to output onto CMLOUT±. 01: Recovered forward channel data from RIN0± is output on CMLOUT± 10: Recovered forward channel data from RIN1± is output on CMLOUT± CMLOUT driver must be enabled by setting 0x56[3] = 1. Note: This must match 0x52[7] setting for PORT0 or PORT1.
0	RESERVED	R/W	0h	Reserved.

8.6.1.56 CML_OUTPUT_CTL3 Register (Address = 63h) [reset = 0h]

CML_OUTPUT_CTL3 is described in Table 67.

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Table 67. CML_OUTPUT_CTL3 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0h	Reserved.
0	CML_TX_PWDN	R/W	0h	Powerdown CML TX 0: CML TX powered up 1: CML TX powered down **NOTE:** CML TX must be powered down prior to enabling Pattern Generator.

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8.6.1.57 PGCTL Register (Address = 64h) [reset = 10h]

PGCTL is described in Table 68.

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Table 68. PGCTL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	PATGEN_SEL	R/W	1h	Fixed Pattern Select: This field selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. The following table shows the color selections in non-inverted followed by inverted color mode: 0000: Reserved 0001: White/Black 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontally Scaled Black to White/White to Black 0111: Horizontally Scaled Black to Red/White to Cyan 1000: Horizontally Scaled Black to Green/White to Magenta 1001: Horizontally Scaled Black to Blue/White to Yellow 1010: Vertically Scaled Black to White/White to Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertically Scaled Black to Green/White to Magenta 1101: Vertically Scaled Black to Blue/White to Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: ReservedSee TI App Note AN-2198 (SNLA132).
3	PATGEN_UNH	R/W	0h	Enables the UNH-IOL compliance test pattern: 0: Pattern type selected by PATGEN_SEL 1: Compliance test pattern is selected. Value of PATGEN_SEL is ignored.
2	PATGEN_COLOR_BARS	R/W	0h	Enable Color Bars: 0: Color Bars disabled 1: Color Bars enabled (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black)
1	PATGEN_VCOM_REV	R/W	0h	Reverse order of color bands in VCOM pattern: 0: Color sequence from top left is (Yellow, Cyan, Blue, Red) 1: Color sequence from top left is (Blue, Cyan, Yellow, Red)
0	PATGEN_EN	R/W	0h	Pattern Generator Enable: 1: Enable Pattern Generator 0: Disable Pattern Generator **NOTE:** CML TX must be powered down prior to enabling Pattern Generator by setting register bit 0x63[0]=1.

8.6.1.58 PGCFG Register (Address = 65h) [reset = 0h]

PGCFG is described in Table 69.

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Table 69. PGCFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	PATGEN_18B	R/W	0h	18-bit Mode Select: 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits. 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness.

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Table 69. PGCFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PATGEN_EXTCLK	R/W	0h	Select External Clock Source: 1: Selects the external pixel clock when using internal timing. 0: Selects the internal divided clock when using internal timing This bit has no effect in external timing mode (PATGEN_TSEL = 0).
2	PATGEN_TSEL	R/W	0h	Timing Select Control: 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size, Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals.
1	PATGEN_INV	R/W	0h	Enable Inverted Color Patterns: 1: Invert the color output. 0: Do not invert the color output.
0	PATGEN_ASCRL	R/W	0h	Auto-Scroll Enable: 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. 0: The Pattern Generator retains the current pattern.

8.6.1.59 PGIA Register (Address = 66h) [reset = 0h]

PGIA is described in Table 70.

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Table 70. PGIA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_IA	R/W	0h	Indirect Address: This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198 (SNLA132).

8.6.1.60 PGID Register (Address = 67h) [reset = 0h]

PGID is described in Table 71.

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Table 71. PGID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATGEN_ID	R/W	0h	Indirect Data: When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the readback value. See TI App Note AN-2198 (SNLA132).

8.6.1.61 PGDBG Register (Address = 68h) [reset = 0h]

PGDBG is described in Table 72.

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Table 72. PGDBG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0h	Reserved.

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Table 72. PGDBG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	PATGEN_BIST_EN	R/W	0h	Pattern Generator BIST Enable: Enables Pattern Generator in BIST mode. Pattern Generator will compare received video data with local generated pattern. Upstream device must be programmed to the same pattern.
2-0	RESERVED	R/W	0h	Reserved.

8.6.1.62 PGTSTDAT Register (Address = 69h) [reset = 0h]

PGTSTDAT is described in Table 73.

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Table 73. PGTSTDAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PATGEN_BIST_ERR	R	0h	Pattern Generator BIST Error Flag During Pattern Generator BIST mode, this bit indicates if the BIST engine has detected errors. If the BIST Error Count (available in the Pattern Generator indirect registers) is non-zero, this flag will be set.
6-0	RESERVED	R	0h	Reserved

8.6.1.63 CSICFG0 Register (Address = 6Ah) [reset = 0h]

CSICFG0 is described in Table 74.

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Table 74. CSICFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RSV	R/W	0h	Reserved
5-4	LANE_COUNT	R/W	0h	Setup number of data lanes for the CSI ports. 00/01: 4 data lanes 10: 2 data lanes 11: 1 data lane
3	ULPM	R/W	0h	When set, put the data lanes in ultra-low power mode (LP00) by sending out a LP signalling sequence
2	ULPS	R/W	0h	When set with ULPM, put the clock lane into ultra-low power mode. No effect if ULPM is not set.
1	CONTS_CLK	R/W	0h	When set, keep the clock lane running (in HS mode) during line blank (DE=0) and frame blank (VS not active)
0	CSI_DIS	R/W	0h	When set, disable the CSI state machine. Function as a soft reset

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8.6.1.64 CSICFG1 Register (Address = 6Bh) [reset = 0h]

CSICFG1 is described in Table 75.

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Table 75. CSICFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OFMT	R/W	0h	Program the output CSI data formats 0000: RGB888 0001: RGB666 0010: RGB565 0011: YUV420 Legacy 0100: YUV420 0101: YUV422_8 0110: RAW8 0111: RAW10 1000: RAW12 1001: YUV420 (CSPS)
3-2	IFMT	R/W	0h	Program the input data format in HDMI terminology 00: RGB444 01: YUV422 10: YUV444 11: RAW
1	INV_VS	R/W	0h	When set, the VS received from the digital receiver will be inverted. Because the CSI logic works on active-high VS, this bit is typically set when the VS from the data source is active-low
0	INV_DE	R/W	0h	When set, the DE received from the digital receiver will be inverted. Because the CSI logic works on active-high DE, this bit is typically set when the DE from the data source is active-low

8.6.1.65 CSIIA Register (Address = 6Ch) [reset = 0h]

CSIIA is described in Table 76.

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Table 76. CSIIA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CSI_IA	R/W	0h	Indirect address port for accessing CSI registers

8.6.1.66 CSIID Register (Address = 6Dh) [reset = 0h]

CSIID is described in Table 77.

Return to Summary Table.

Table 77. CSIID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CSI_ID	R/W	0h	Indirect data port for accessing CSI registers

8.6.1.67 GPIO_Pin_Status_1 Register (Address = 6Eh) [reset = 0h]

GPIO_Pin_Status_1 is described in Table 78.

Return to Summary Table.

Table 78. GPIO_Pin_Status_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO7_Pin_Status	R	0h	GPIO7/I2S_WC pin status
6	GPIO6_Pin_Status	R	0h	GPIO6/I2S_DA pin status

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Table 78. GPIO_Pin_Status_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	GPIO5_Pin_Status	R	0h	GPIO5/I2S_DB pin status
4	RESERVED	R	0h	Reserved
3	GPIO3_Pin_Status	R	0h	GPIO3 / I2S_DD pin status
2	GPIO2_Pin_Status	R	0h	GPIO2 / I2S_DC pin status
1	GPIO1_Pin_Status	R	0h	GPIO1 pin status
0	GPIO0_Pin_Status	R	0h	GPIO0 pin status

8.6.1.68 GPIO_Pin_Status_2 Register (Address = 6Fh) [reset = 0h]

GPIO_Pin_Status_2 is described in Table 79.

Return to Summary Table.

Table 79. GPIO_Pin_Status_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	GPIO9_Pin_Status	R	0h	GPIO9/MCLK pin status
0	GPIO8_Pin_Status	R	0h	GPIO8/I2S_CLK pin status

8.6.1.69 RX_BKSV0 Register (Address = 80h) [reset = 0h]

RX_BKSV0 is described in Table 80.

Return to Summary Table.

Table 80. RX_BKSV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV0	R	0h	BKSV0: Value of byte0 of the Receiver KSV.

8.6.1.70 RX_BKSV1 Register (Address = 81h) [reset = 0h]

RX_BKSV1 is described in Table 81.

Return to Summary Table.

Table 81. RX_BKSV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV1	R	0h	BKSV1: Value of byte1 of the Receiver KSV.

8.6.1.71 RX_BKSV2 Register (Address = 82h) [reset = 0h]

RX_BKSV2 is described in Table 82.

Return to Summary Table.

Table 82. RX_BKSV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV2	R	0h	BKSV2: Value of byte2 of the Receiver KSV.

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8.6.1.72 RX_BKSV3 Register (Address = 83h) [reset = 0h]

RX_BKSV3 is described in Table 83.

Return to Summary Table.

Table 83. RX_BKSV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV3	R	0h	BKSV3: Value of byte3 of the Receiver KSV.

8.6.1.73 RX_BKSV4 Register (Address = 84h) [reset = 0h]

RX_BKSV4 is described in Table 84.

Return to Summary Table.

Table 84. RX_BKSV4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BKSV4	R	0h	BKSV4: Value of byte4 of the Receiver KSV.

8.6.1.74 TX_KSV0 Register (Address = 90h) [reset = 0h]

TX_KSV0 is described in Table 85.

Return to Summary Table.

Table 85. TX_KSV0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV0	R	0h	TX_KSV0: Value of byte0 of the Transmitter KSV.

8.6.1.75 TX_KSV1 Register (Address = 91h) [reset = 0h]

TX_KSV1 is described in Table 86.

Return to Summary Table.

Table 86. TX_KSV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV1	R	0h	TX_KSV1: Value of byte1 of the Transmitter KSV.

8.6.1.76 TX_KSV2 Register (Address = 92h) [reset = 0h]

TX_KSV2 is described in Table 87.

Return to Summary Table.

Table 87. TX_KSV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV2	R	0h	TX_KSV2: Value of byte2 of the Transmitter KSV.

8.6.1.77 TX_KSV3 Register (Address = 93h) [reset = 0h]

TX_KSV3 is described in Table 88.

Return to Summary Table.

Table 88. TX_KSV3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV3	R	0h	TX_KSV3: Value of byte3 of the Transmitter KSV.

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8.6.1.78 TX_KSV4 Register (Address = 94h) [reset = 0h]

TX_KSV4 is described in Table 89.

Return to Summary Table.

Table 89. TX_KSV4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TX_KSV4	R	0h	TX_KSV4: Value of byte4 of the Transmitter KSV.

8.6.1.79 HDCP_DBG Register (Address = C0h) [reset = 0h]

HDCP_DBG is described in Table 90.

Return to Summary Table.

Table 90. HDCP_DBG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved.
6	HDCP_I2C_TO_DIS	R	0h	HDCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second. Set via the HDCP_DBG register in the HDCP Transmitter.
5-4	RESERVED	R	0h	Reserved
3	RGB_CHKSUM_EN	R	0h	Enable RBG video line checksum: Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line. Set via the HDCP_DBG register in the HDCP Transmitter.
2	FAST_LV	R	0h	Fast Link Verification: HDCP periodically verifies that the HDCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames. Set via the HDCP_DBG register in the HDCP Transmitter.
1	TMR_SPEEDUP	R	0h	Timer Speedup: Speed up HDCP authentication timers. Set via the HDCP_DBG register in the HDCP Transmitter.
0	HDCP_I2C_FAST	R	0h	HDCP I2C Fast mode Enable: Setting this bit to a 1 will enable the HDCP I2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing. Set via the HDCP_DBG register in the HDCP Transmitter.

8.6.1.80 HDCP_DBG2 Register (Address = C1h) [reset = 0h]

HDCP_DBG2 is described in Table 91.

Return to Summary Table.

Table 91. HDCP_DBG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0h	Reserved
1	NO_DECRYPT	R/W	0h	No Decrypt: When set to a 1, the HDCP Receiver will output the encrypted data on the RGB pins. All other functions will work normally. This provides a simple way of showing that the link is encrypted.

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Table 91. HDCP_DBG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	HDCP_EN_MODE	R/W	0h	HDCP Enable Mode: This bit controls whether the HDCP Repeater function will enable HDCP in attached HDCP Transmitters if it detects HDCP is already enabled 1 : Don't re-enable HDCP if already enabled 0 : Re-enable HDCP at start of authentication, even if HDCP Transmitter already has HDCP enabled

8.6.1.81 HDCP_STS Register (Address = C4h) [reset = 0h]

HDCP_STS is described in Table 92.

Return to Summary Table.

Table 92. HDCP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	RGB_CHKSUM_ERR	R	0h	RGB Checksum Error Detected: If RGB Checksum in enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register
0	AUTHED	R	0h	HDCP Authenticated: Indicates the HDCP authentication has completed suc-cessfully. The controller may now send video data re-quiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authen-tication.

8.6.1.82 KSV_FIFO_DATA Register (Address = C9h) [reset = 0h]

KSV_FIFO_DATA is described in Table 93.

Return to Summary Table.

Table 93. KSV_FIFO_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KSV_FIFO_DATA	R/W	0h	KSV_FIFO_DATA: During External Repeater Control mode, the External HDCP controller writes KSV data to the KSV FIFO through this register. A byte written to this register location will write one byte of KSV data to the KSV FIFO at the location indicated by the KSV_FIFO_ADDR registers.

8.6.1.83 KSV_FIFO_ADDR0 Register (Address = CAh) [reset = 0h]

KSV_FIFO_ADDR0 is described in Table 94.

Return to Summary Table.

Table 94. KSV_FIFO_ADDR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KSV_FIFO_ADDR0	R/W	0h	KSV FIFO Address Register 0: This register contains the lower 8 bits of the KSF FIFO Address. This value should be set to 0 before writing the first byte of KSV data to the KSV FIFO. The KSV FIFO Address will automatically increment for each write to the KSV_FIFO_DATA register.

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8.6.1.84 KSV_FIFO_ADDR1 Register (Address = CBh) [reset = 0h]

KSV_FIFO_ADDR1 is described in Table 95.

Return to Summary Table.

Table 95. KSV_FIFO_ADDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	KSV_FIFO_ADDR1	R/W	0h	KSV FIFO Address Register 1: This register contains the most significant bit of the KSF FIFO Address. This value should be set to 0 before writing the first byte of KSV data to the KSV FIFO. The KSV FIFO Address will automatically increment for each write to the KSV_FIFO_DATA register.

8.6.1.85 RPTR_TX0 Register (Address = E0h) [reset = 0h]

RPTR_TX0 is described in Table 96.

Return to Summary Table.

Table 96. RPTR_TX0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT0_ADDR	R	0h	HDCP Repeater Transmit Port 0 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT0_VALID	R	0h	HDCP Repeater Transmit Port 0 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

8.6.1.86 RPTR_TX1 Register (Address = E1h) [reset = 0h]

RPTR_TX1 is described in Table 97.

Return to Summary Table.

Table 97. RPTR_TX1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT1_ADDR	R	0h	HDCP Repeater Transmit Port 1 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT1_VALID	R	0h	HDCP Repeater Transmit Port 1 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

8.6.1.87 RPTR_TX2 Register (Address = E2h) [reset = 0h]

RPTR_TX2 is described in Table 98.

Return to Summary Table.

Table 98. RPTR_TX2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT2_ADDR	R	0h	HDCP Repeater Transmit Port 2 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT2_VALID	R	0h	HDCP Repeater Transmit Port 2 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

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8.6.1.88 RPTR_TX3 Register (Address = E3h) [reset = 0h]

RPTR_TX3 is described in Table 99.

Return to Summary Table.

Table 99. RPTR_TX3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	PORT3_ADDR	R	0h	HDCP Repeater Transmit Port 3 I2C Address Indicates the I2C address for the Repeater Transmit Port.
0	PORT3_VALID	R	0h	HDCP Repeater Transmit Port 3 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register

8.6.1.89 HDCP_RX_ID0 Register (Address = F0h) [reset = 5Fh]

HDCP_RX_ID0 is described in Table 100.

Return to Summary Table.

Table 100. HDCP_RX_ID0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID0	R	5Fh	HDCP_RX_ID0: First byte ID code, '_ '

8.6.1.90 HDCP_RX_ID1 Register (Address = F1h) [reset = 55h]

HDCP_RX_ID1 is described in Table 101.

Return to Summary Table.

Table 101. HDCP_RX_ID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID1	R	55h	HDCP_RX_ID1: 2nd byte of ID code, 'U '

8.6.1.91 HDCP_RX_ID2 Register (Address = F2h) [reset = 48h]

HDCP_RX_ID2 is described in Table 102.

Return to Summary Table.

Table 102. HDCP_RX_ID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID2	R	48h	HDCP_RX_ID2: 3rd byte of ID code. Value will be either 'B ' or 'H '. 'H ' indicates an HDCP capable device.

8.6.1.92 HDCP_RX_ID3 Register (Address = F3h) [reset = 39h]

HDCP_RX_ID3 is described in Table 103.

Return to Summary Table.

Table 103. HDCP_RX_ID3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID3	R	39h	HDCP_RX_ID3: 4th byte of ID code: '9 '

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8.6.1.93 HDCP_RX_ID4 Register (Address = F4h) [reset = 34h]

HDCP_RX_ID4 is described in Table 104.

Return to Summary Table.

Table 104. HDCP_RX_ID4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID4	R	34h	HDCP_RX_ID4: 5th byte of ID code: '4 '

8.6.1.94 HDCP_RX_ID5 Register (Address = F5h) [reset = 30h]

HDCP_RX_ID5 is described in Table 105.

Return to Summary Table.

Table 105. HDCP_RX_ID5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HDCP_RX_ID5	R	30h	HDCP_RX_ID5: 6th byte of ID code: '0 '

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8.6.2 CSI-2 Indirect Registers

Table 106 summarizes the DS90UH940N-Q1 CSI-2 indirect registers. All register offset addresses not listed in Table 106 should be considered as reserved locations and the register contents should not be modified.

In the register definitions under the *TYPE* heading, the following definitions apply:

- R = Read only access
- R/W = Read / Write access

Table 106. CSI-2 Indirect Registers Summary

Address	Acronym	Register Name	Section
2h	CSI_TCK_TRAIL		Go
9h	RAW_ALIGN		Go
13h	CSI_EN_PORT0		Go
14h	CSI_EN_PORT1		Go
16h	CSIPASS		Go
2Eh	CSI_VC_ID		Go

8.6.2.1 CSI_TCK_TRAIL Register (Address = 2h) [reset = 0h]

CSI_TCK_TRAIL is described in Table 107.

Return to Summary Table.

Table 107. CSI_TCK_TRAIL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CSI_TCK_TRAIL_OV	R/W	0h	Override CSI Tsk Trail Parameter 0: Tsk Trail is automatically determined. 1: Override Tsk Trail parameter with a value in bits [3:0] in this register.
6-5	RESERVED	R/W	0h	Reserved
3-0	CSI_TCK_TRAIL	R/W	0h	Tsk Trail Value.

8.6.2.2 RAW_ALIGN Register (Address = 9h) [reset = 0h]

RAW_ALIGN is described in Table 108.

Return to Summary Table.

Table 108. RAW_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	RAW_ALIGN	R/W	0h	Raw Align. 0: RAW Output onto LSB's of RGB Bus 1: RAW Output onto MSB's of RGB Bus
3-0	RESERVED	R/W	0h	Reserved

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8.6.2.3 CSI_EN_PORT0 Register (Address = 13h) [reset = 3Fh]

CSI_EN_PORT0 is described in Table 109.

Return to Summary Table.

Table 109. CSI_EN_PORT0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RCTL_PORT0	R/W	0h	Register Control 0 = Disable 1 = Enable
6	RESERVED	R/W	0h	Reserved
5-0	EN_PORT0	R/W	3Fh	0x00 = Disable CSI Port 0 0x3F = Enable CSI Port 0

8.6.2.4 CSI_EN_PORT1 Register (Address = 14h) [reset = 0h]

CSI_EN_PORT1 is described in Table 110.

Return to Summary Table.

Table 110. CSI_EN_PORT1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RCTL_PORT1	R/W	0h	Register Control 0 = Disable 1 = Enable
6	RESERVED	R/W	0h	Reserved
5-0	EN_PORT1	R/W	0h	0x00 = Disable CSI Port 1 0x3F = Enable CSI Port 1

8.6.2.5 CSIPASS Register (Address = 16h) [reset = 2h]

CSIPASS is described in Table 111.

Return to Summary Table.

Table 111. CSIPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2	CSI_PASS_toGP3	R/W	0h	CSI_PASS to GPIO3. Configures GPIO3 to output the PASS signal when this bit is set HIGH.
1	CSI_PASS_toGP0	R/W	1h	CSI_PASS to GPIO0. Configures GPIO0 to output the PASS signal when this bit is set HIGH. This is the default.
0	CSI_PASS	R/W	0h	CSI_PASS. This bit reflects the status of the PASS signal.

8.6.2.6 CSI_VC_ID Register (Address = 2Eh) [reset = 0h]

CSI_VC_ID is described in Table 112.

Return to Summary Table.

Table 112. CSI_VC_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CSI_VC_ID	R/W	0h	CSI Virtual Channel Identifier. 00: CSI-2 outputs with ID as virtual channel 0. 01: CSI-2 outputs with ID as virtual channel 1. 10: CSI-2 outputs with ID as virtual channel 2. 11: CSI-2 outputs with ID as virtual channel 3.
5-0	RESERVED	R/W	0h	Reserved.

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

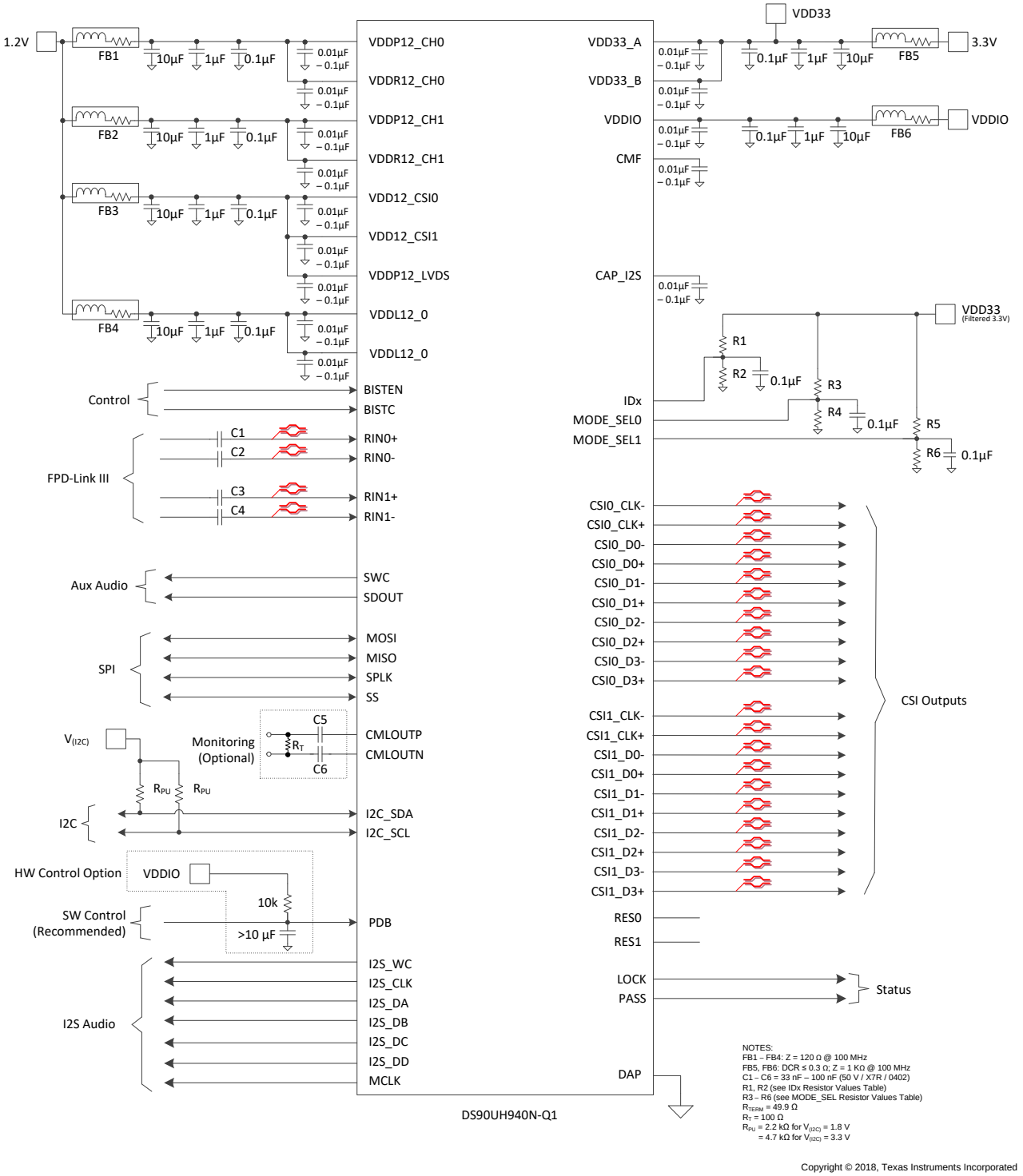
The DS90UH940N-Q1 is a FPD-Link III deserializer which, in conjunction with the DS90UH949/947-Q1 serializers, converts 1-lane or 2-lane FPD-Link III streams into a MIPI CSI-2 interface. The deserializer can operate over cost-effective 50-Ω single-ended coaxial or 100-Ω differential shielded twisted-pair (STP) cables. The deserializer recovers the data from two FPD-Link III serial streams and translates it into a camera serial interface (CSI-2) format compatible with MIPI DPHY/CSI-2 supporting video resolutions up to WUXGA and 1080p60 with 24-bit color depth.

9.2 Typical Applications

Bypass capacitors must be placed near the power supply pins. At a minimum, use four (4) 10-µF capacitors for local device bypassing. Ferrite beads are placed on the two sets of supply pins (VDD33 and VDDIO) for effective noise suppression. The interface to the graphics source is LVDS. The VDDIO pins may be connected to 3.3 V or 1.8 V. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See 図 38 for a typical STP connection diagram and 図 39 for a typical coax connection diagram.

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Typical Applications (continued)



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図 38. Typical Connection Diagram (STP)

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Typical Applications (continued)

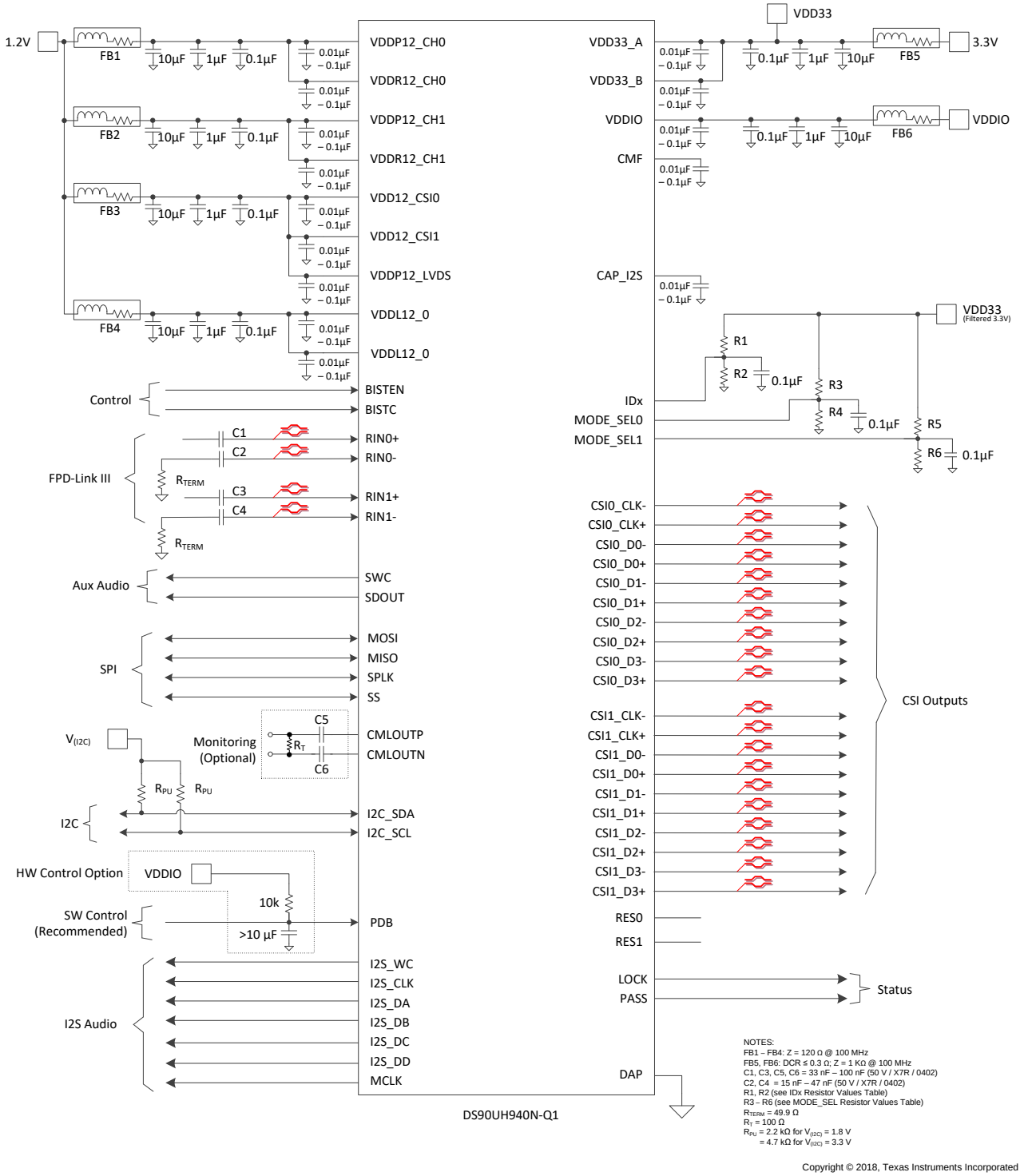


図 39. Typical Connection Diagram (Coax)

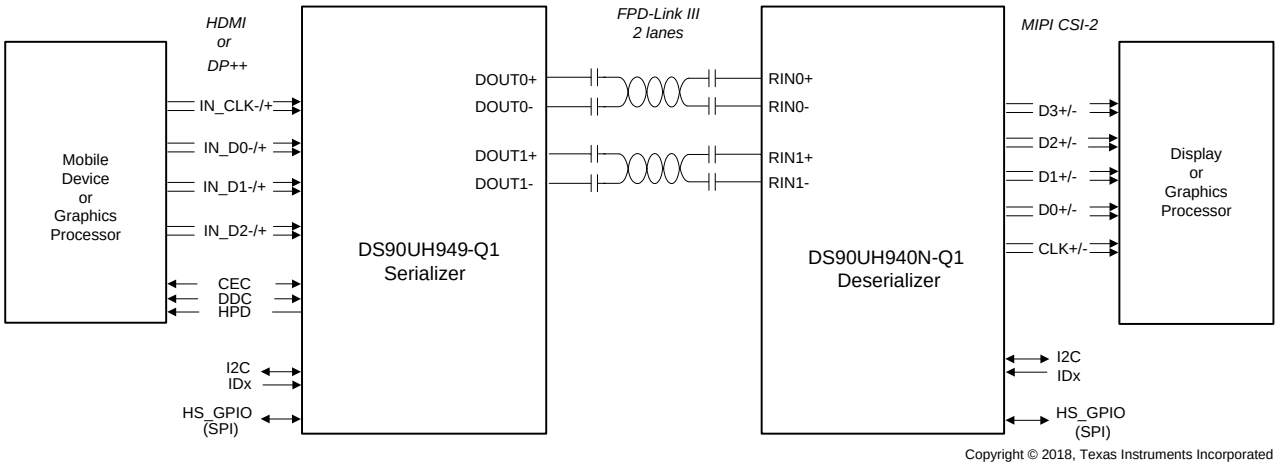


図 40. Typical Display System Diagram

9.2.1 Design Requirements

For the typical design application, use the following as input parameters.

表 113. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDD33	3.3 V
VDDIO	1.8 or 3.3 V
VDD12	1.2 V
AC-coupling capacitor for STP with 925/927: RIN[1:0]±	100 nF
AC-coupling capacitor for STP with 929/947/949: RIN[1:0]±	33 nF - 100 nF
AC-coupling capacitor for Coax with 921: RIN[1:0]+	100 nF
AC-coupling capacitor for Coax with 921: RIN[1:0]-	47 nF
AC-coupling capacitor for Coax with 929/947/949: RIN[1:0]+	33 nF - 100 nF
AC-coupling capacitor for Coax with 929/947/949: RIN[1:0]+	15 nF - 47 nF

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC-coupling capacitors must be placed in series in the FPD-Link III signal path as shown in 図 41. For applications using single-ended 50-Ω coaxial cable, the unused data pins (RIN0– and RIN1–) must use a 15-nF to 47-nF capacitor and must be terminated with a 50-Ω resistor.

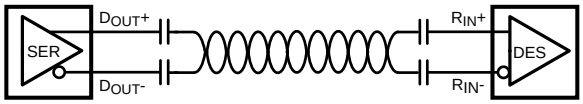


図 41. AC-Coupled Connection (STP)

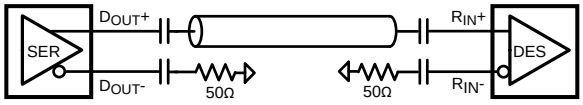


図 42. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, use the smallest available package for the AC-coupling capacitor. This minimizes degradation of signal quality due to package parasitics.

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9.2.2 Detailed Design Procedure

9.2.2.1 FPD-Link III Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER Operation and Application Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187) available in PDF format from the Texas Instruments web site.

9.2.3 Application Curves

The plots below correspond to 1080p60 video application with a 2-lane FPD-Link III input and MIPI 4-lane output.

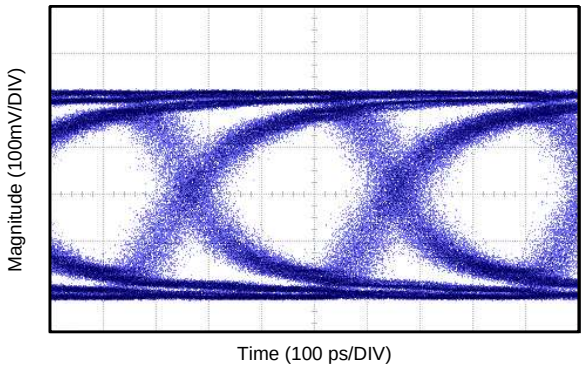


図 43. Loop-Through CML Output at 2.6-Gbps Serial Line Rate

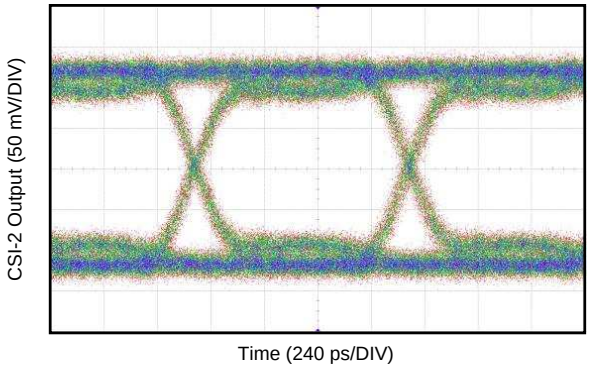


図 44. CSI-2 Data Output at 1040 Mbps

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10 Power Supply Recommendations

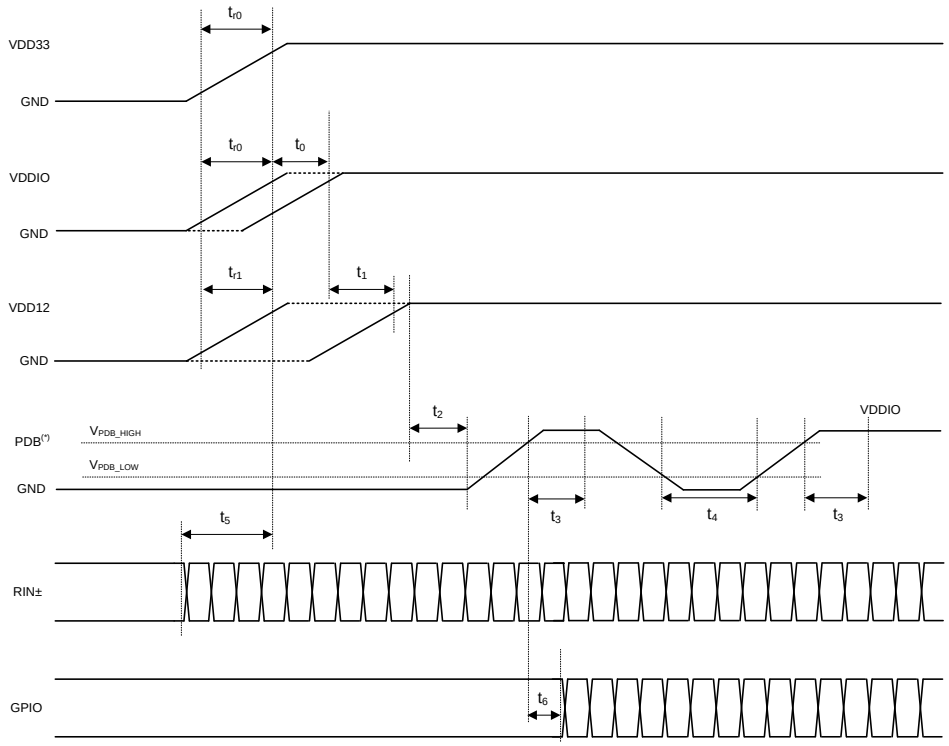
This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. provides guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

10.1 Power-Up Requirements and PDB Pin

When power is applied, power from the highest voltage rail to the lowest voltage rail on any of the supply pins. For 3.3-V IO operation, VDDIO and VDD33 can be powered by the same supply and ramped simultaneously. Use a large capacitor on the PDB pin to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to VDD33, a 10-kΩ pullup and a > 10–μF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until both VDD33 and VDDIO has reached steady state. Pins VDD33_A and VDD33_B must both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

10.2 Power Sequence

The power-up sequence for the DS90UB940N-Q1 is as follows:



(*) It is recommended to assert PDB (active High) with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.

図 45. Power-Up Sequencing

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Power Sequence (continued)

表 114. Power-Up Sequence Timing Parameters

PARAMETER		MIN	TYP	MAX	UNIT	NOTES
t_{r0}	VDD33 / VDDIO rise time	0.2			ms	@10/90%
t_{r1}	VDD12 rise time	0.05			ms	@10/90%
t_0	VDD33 to VDDIO delay	0			ms	
t_1	VDD33 / VDDIO to VDD12 delay	0			ms	
t_2	VDDx to PDB delay	0			ms	Release PDB after all supplies are up and stable.
t_3	PDB to I2C ready delay	2			ms	
t_4	PDB pulse width	2			ms	Hard reset
t_5	Valid data on RIN± to VDDx delay	0			ms	Provide valid data from a compatible Serializer before power-up or apply reset as described in (1).
t_6	PDB to GPIO delay	2			ms	Keep GPIOs low or high until PDB is high.

(1) DS90UH940N-Q1 should be powered up after a compatible Serializer has started sending valid video data. If this condition is not satisfied, then a digital (software) reset or hard reset (toggling PDB pin) is required after receiving the input data. This requirement prevents the DS90UH940N-Q1 from locking to any random or noise signal, ensures DS90UH940N-Q1 has a deterministic startup behavior, specified lock time, and optimal adaptive equalizer setting.

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11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the FPD-Link III devices must be designed to provide low-noise power feed to the device. Good layout practice also separates high frequency or high-level inputs and outputs to minimize unwanted stray noise pick-up, feedback, and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mils) for power/ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which has proven especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 0.1 µF. Ceramic capacitors may be in the 2.2-µF to 10-µF range. The voltage rating of the ceramic capacitors must be at least 5× the power supply voltage being used

TI recommends surface-mount capacitors due to their smaller parasitics. When using multiple capacitors per supply pin, place the smaller value closer to the pin. A large bulk capacitor is recommend at the point of power entry. This is typically in the 50-µF to 100-µF range, which smooths low frequency switching noise. TI recommends connecting power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor increases the inductance of the path.

A small body size X7R chip capacitor, such as 0603 or 0402, is recommended for external bypass. The small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also common practice to use two vias from power and ground pins to the planes to reduce the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter may be used to provide clean power to sensitive circuits such as PLLs.

Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines. Differential impedance of 100 Ω are typically recommended for STP interconnect and single-ended impedance of 50 Ω for coaxial interconnect. The closely coupled lines help to ensure that coupled noise appears as common-mode and thus is rejected by the receivers. The tightly coupled lines also radiate less.

Information on the WQFN package is provided *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

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11.2 Ground

TI recommends that a consistent ground plane reference for the high-speed signals in the PCB design to provide the best image plane for signal traces running parallel to the plane. Connect the thermal pad of the device to this plane with vias.

At least 32 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the WQFN style package, including PCB design and manufacturing requirements, is provided in *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

11.3 Routing FPD-Link III Signal Traces

Routing the FPD-Link III signal traces between the R_{IN} pins and the connector is the most critical pieces of a successful PCB layout. 図 47 shows an example PCB layout. For additional PCB layout details of the example, refer to the *DS90UH940-Q1EVM User's Guide* (SNLU162).

The following list provides essential recommendations for routing the FPD-Link III signal traces between the receiver input pins (R_{IN}) and the connector.

- The routing of the FPD-Link III traces may be all on the top layer or partially embedded in middle layers if EMI is a concern.
- The AC-coupling capacitors should be on the top layer and very close to the receiver input pins.
- Route the RIN traces between the AC-coupling capacitor and the connector as a 100-Ω differential micro-strip with tight impedance control (±10%). Calculate the proper width of the traces for a 100-Ω differential impedance based on the PCB stack-up.
- When choosing to implement a common mode choke for common mode noise reduction, minimize the effects of any impedance mismatch.
- Consult with connector manufacturer for optimized connector footprint. If the connector is mounted on the same side as the IC, minimize the impact of the thru-hole connector stubs by routing the high-speed signal traces on the opposite side of the connector mounting side.

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11.4 CSI-2 Guidelines

1. Route CSI_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep intra-pair length mismatch to < 5 mils.
4. Keep inter-pair length mismatch to < 50 mils within a single CSI-2 TX port. CSI-2 TX Port 0 differential traces do not need to match CSI-2 Port 1 differential traces.
5. Length matching should be near the location of mismatch.
6. Each pair should be separated at least by 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer.
9. Keep the number of VIAS to a minimum — TI recommends keeping the VIA count to 2 or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.
12. Adding Test points causes impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

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11.5 Layout Example

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown in 図 46:

表 115. No Pullback WQFN Stencil Aperture Summary

DEVICE	PIN COUNT	MKT DWG	PCB I/O Pad SIZE (mm)	PCB PITCH (mm)	PCB DAP SIZE(mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP APERTURE (mm)	NUMBER OF DAP APERTURE OPENINGS	GAP BETWEEN DAP APERTURE (Dim A mm)
DS90UH940N-Q1	64	NKD	0.25 × 0.6	0.5	7.2 x 7.2	0.25 x 0.6	1.16 × 1.16	25	0.2

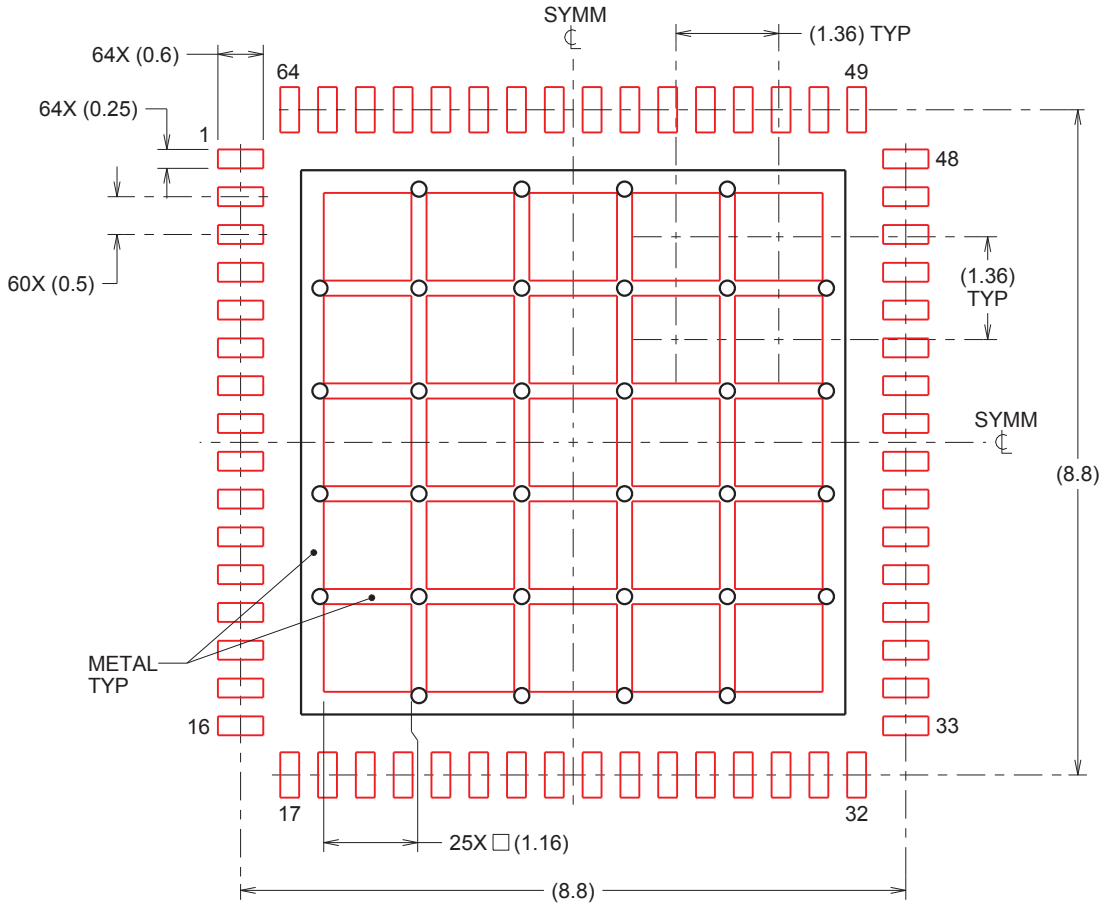


図 46. 64-Pin WQFN Stencil Example of Via and Opening Placement (Dimensions in mm)

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図 47 (PCB layout example) is derived from a layout design of the DS90UH940N-Q1. This graphic and additional layout description are used to demonstrate both proper routing and proper solder techniques when designing in the Deserializer.

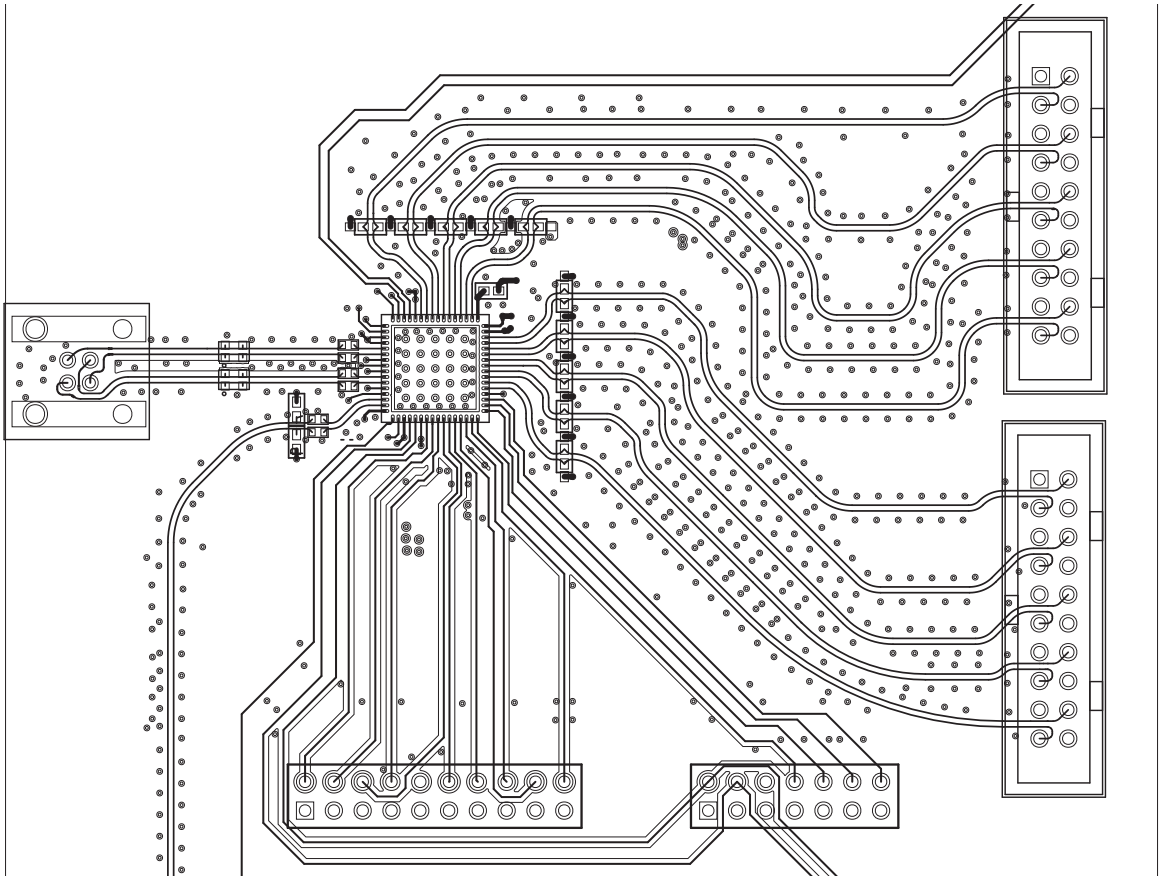


図 47. DS90UH940N-Q1 Deserializer Example Layout

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『ハンダ付け仕様』アプリケーション・レポート*(SNOA549)
- *『半導体およびICパッケージの熱指標』アプリケーション・レポート*(SPRA953)
- *『AN-1108 チャネル・リンクPCBと相互接続デザイン・インのガイドライン』*(SNLA008)
- *『AN-905 転送ラインRAPIDESIGNER操作およびアプリケーション・ガイド』*(SNLA035)
- *『AN-1187 リードレス・リードフレーム・パッケージ(LLP)』*(SNOA401)
- *『LVDSオーナー・マニュアル』*(SNLA187)
- *『AN-2173 双方向制御チャネルによるFPD-Link III上のI2C通信』*(SNLA131)
- *『DS90Ux92x FPD-Link IIIデバイスのI2Sオーディオ・インターフェイスの使用法』*(SNLA221)
- *『AN-2198 720p FPD-Link IIIデバイスの内部テスト・パターン生成機能の解説』*(SNLA132)
- *『I2Cバスのプルアップ抵抗値の計算』*(SLVA689)
- FPD-Link学習センタ
- *『FPD-Link III SerDesを対象とするEMC/EMIのシステム設計とテストに関する方法論』*(SLYT719)
- *『車載EMC/EMI要件設計のための10のヒント』*(SLYT636)

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12.3 コミュニティ・リソース

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 メカニカル、パッケージ、および注文情報

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UH940NTNKDRQ1	Active	Production	WQFN (NKD) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1
DS90UH940NTNKDRQ1.A	Active	Production	WQFN (NKD) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1
DS90UH940NTNKDRQ1.B	Active	Production	WQFN (NKD) | 64	2000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1
DS90UH940NTNKDTQ1	Active	Production	WQFN (NKD) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1
DS90UH940NTNKDTQ1.A	Active	Production	WQFN (NKD) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1
DS90UH940NTNKDTQ1.B	Active	Production	WQFN (NKD) | 64	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	90UH940NQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

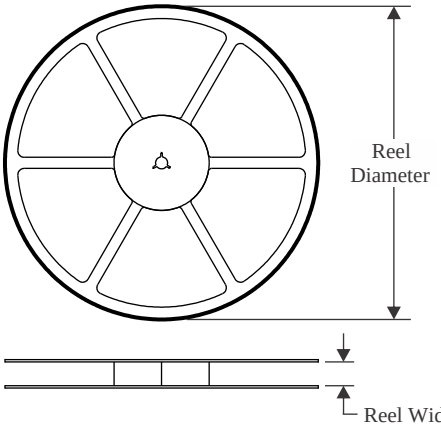
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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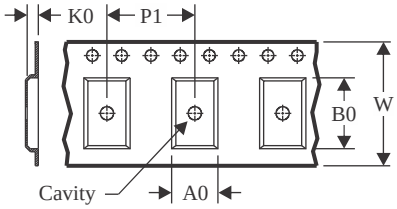
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

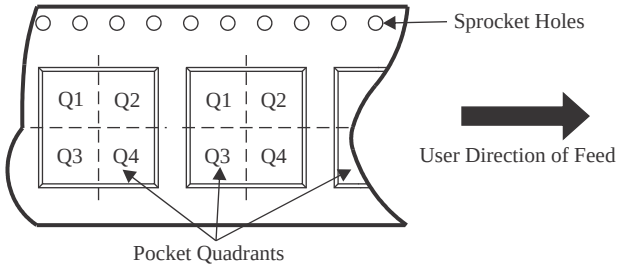


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

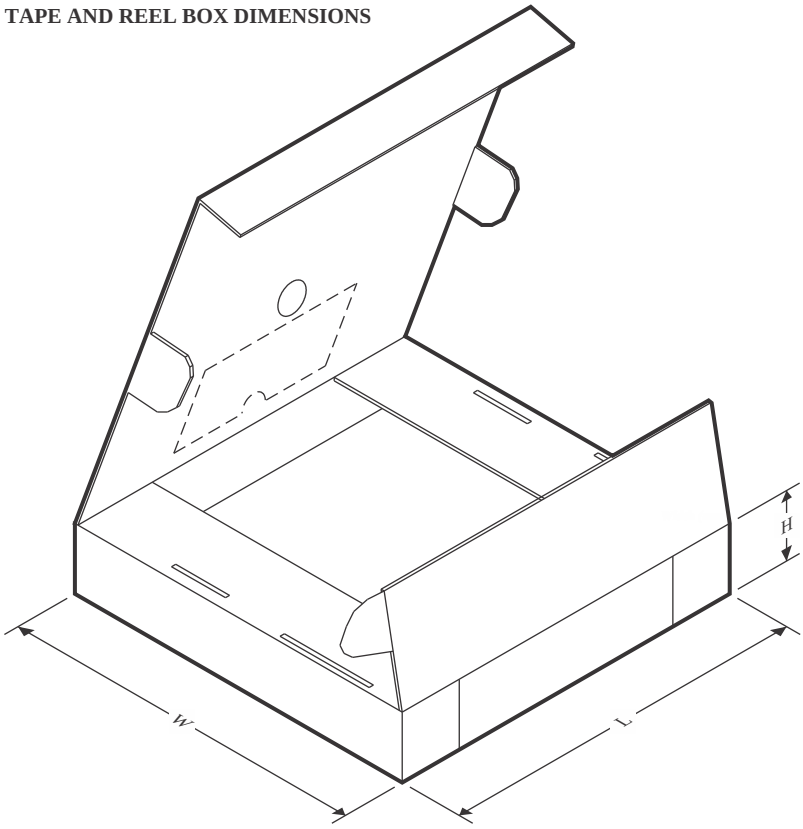
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH940NTNKDRQ1	WQFN	NKD	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q2
DS90UH940NTNKDTQ1	WQFN	NKD	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH940NTNKDRQ1	WQFN	NKD	64	2000	356.0	356.0	36.0
DS90UH940NTNKDTQ1	WQFN	NKD	64	250	208.0	191.0	35.0

GENERIC PACKAGE VIEW

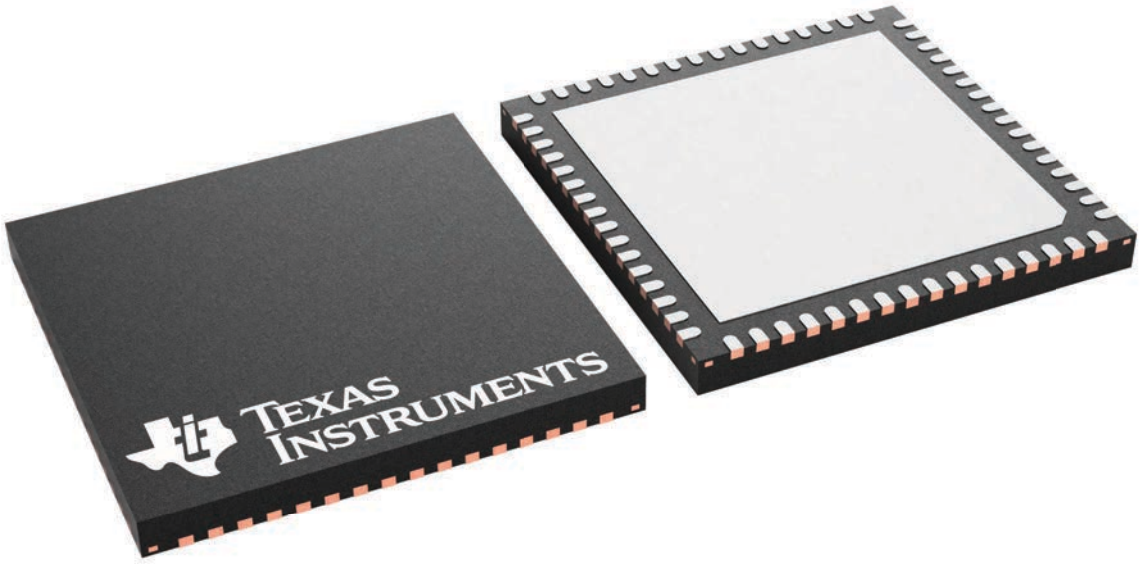
NKD 64

WQFN - 0.8 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

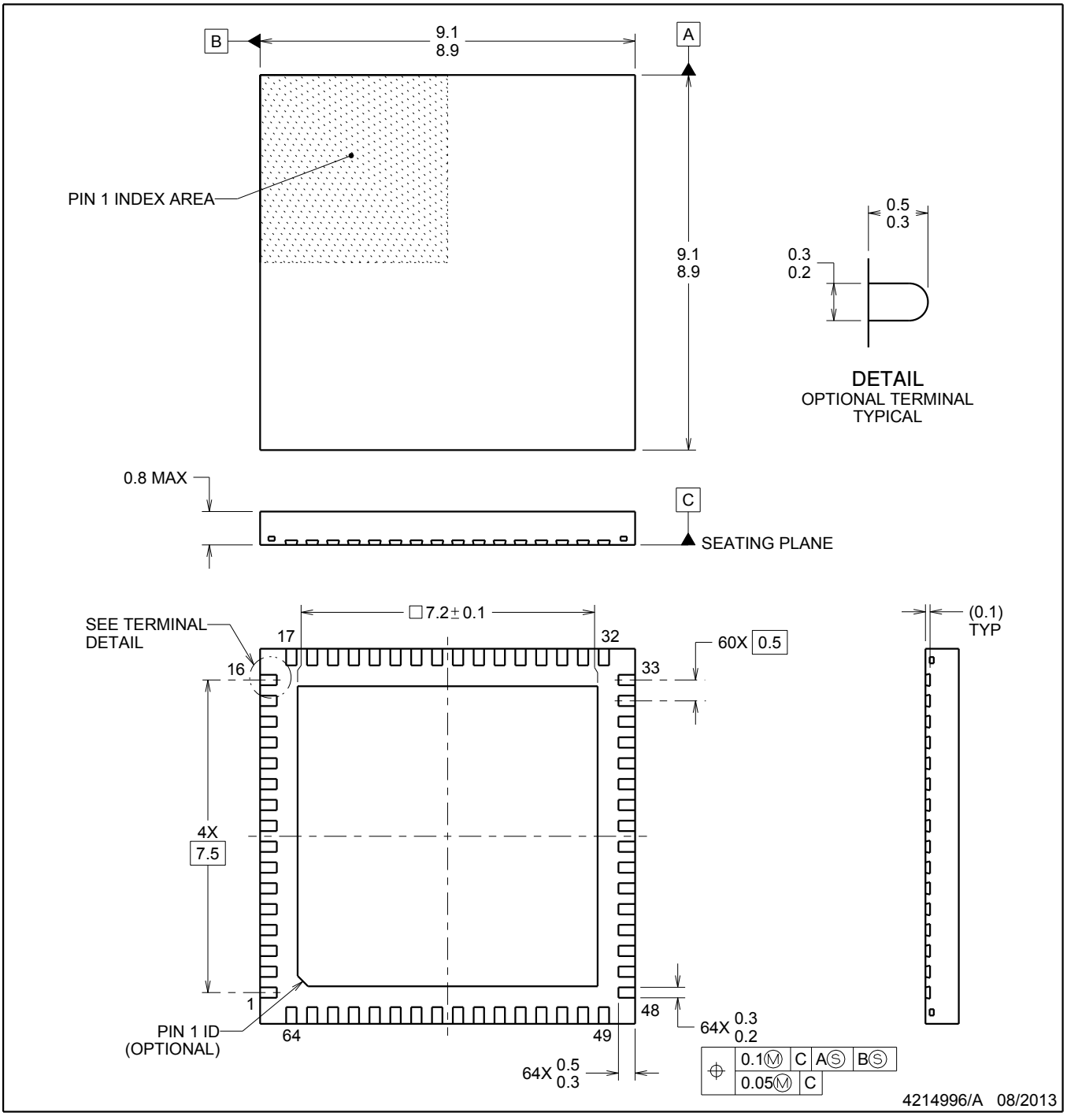


4229637/A

NKD0064A

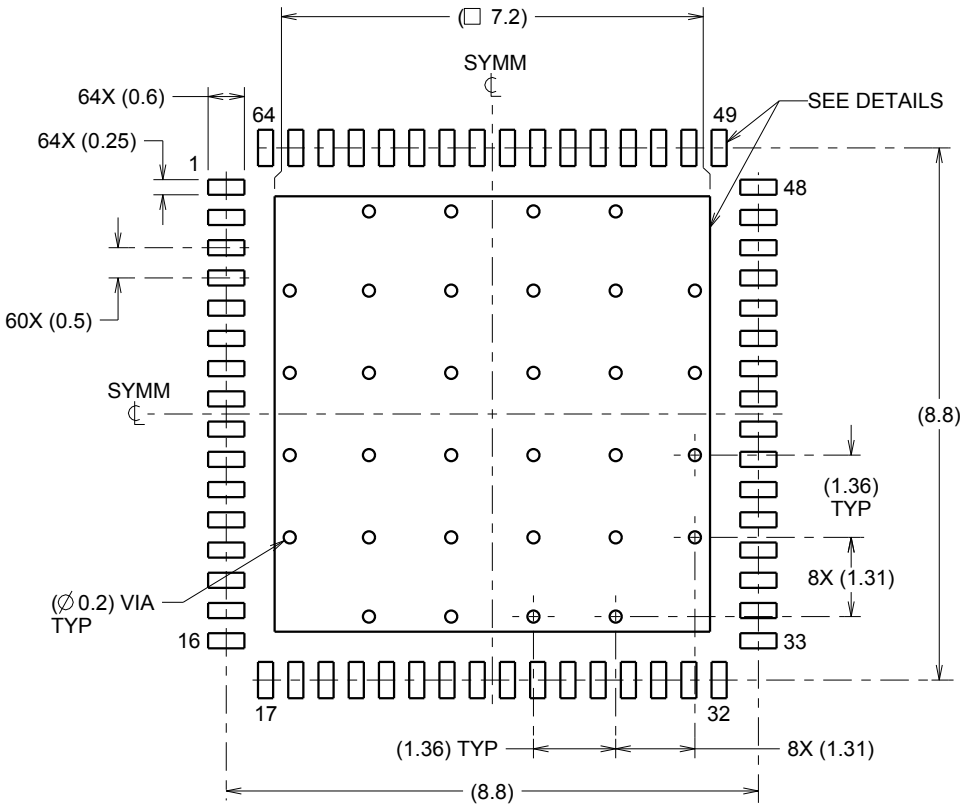
WQFN - 0.8 mm max height

WQFN

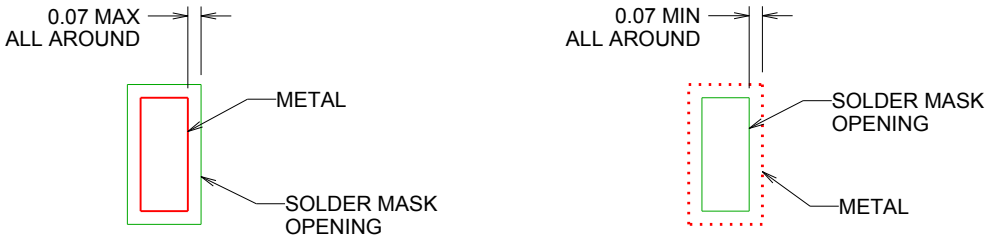


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:8X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214996/A 08/2013

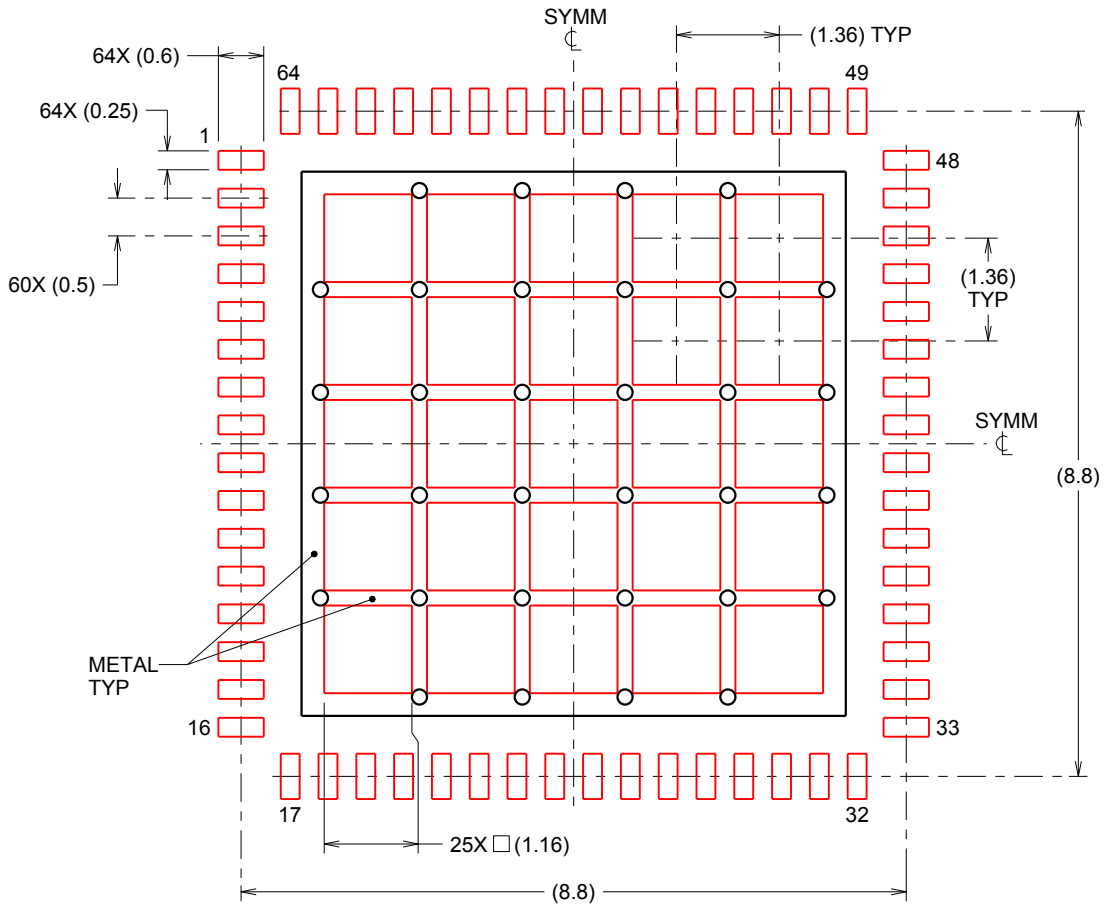
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

NKD0064A

WQFN - 0.8 mm max height

WQFN



SOLDERPASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

4214996/A 08/2013

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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