TEXAS INSTRUMENTS
ESD351
JAJSFV0 – JULY 2018

ESD351 0402パッケージでクランプ電圧の低い 1チャネル、30kV ESD保護ダイオード

1 特長

- IEC 61000-4-2 レベル4 ESD保護
  - 接触放電 ±30kV
  - 空気ギャップ放電 ±30kV
- IEC 61000-4-4 EFT保護
  - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
  - 6A (8/20µs)
- IO容量：1.8pF（標準値）
- DC降伏電圧: 4.5V (最小値)
- 低いリーク電流: 0.1nA (標準値)
- 非常に低いESDクランプ電圧
  - 16A TLPで6.5V（I/OからGNDへ）
  - R_{DYN}:0.1Ω（I/OピンからGNDへ）
- 工業用温度範囲: -40℃～+125℃
- 業界標準の0402パッケージ(DFN1006P2)

2 アプリケーション

- 最終製品
  - ウェアラブル
  - 産業用およびサービス用ロボット
  - ラップトップおよびデスクトップPC
  - モバイルおよびタブレット
  - セットトップ・ボックス
  - DVRおよびNVR
  - TVおよびモニタ
  - EPOS (電子販売時点情報管理)
- インターフェイス
  - USB 2.0/1.1
  - GPIO
  - プッシュボタン
  - オーディオ

3 概要

ESD351は単方向TVS ESD保護ダイオードで、低い動的抵抗R_{DYN}と、低いクランプ電圧が特長です。ESD351は、IEC 61000-4-2標準に従い、最高30kVのESD衝撃（接触および空中）を放散できることが規定されています。動的抵抗(0.1Ω)とクランプ電圧（16A TLPで6.5V）が非常に低いため、過渡事象に対するシステム・レベルの保護が保証されます。このデバイスの容量は1.8pF（標準値）で、USB 2.0などのインターフェイスの保護に理想的です。

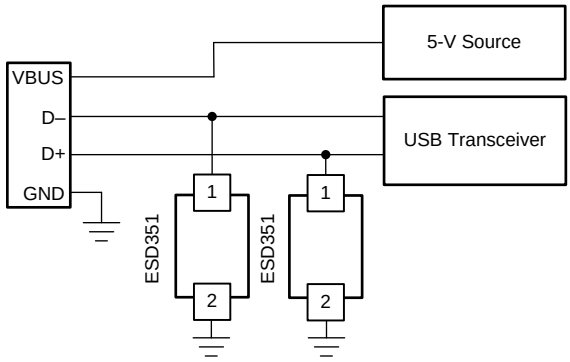
ESD351は、業界標準の0402 (DPY/DFN1006P2)パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
ESD351	X1SON (2)	0.60mm×1.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なUSB 2.0アプリケーションの回路図



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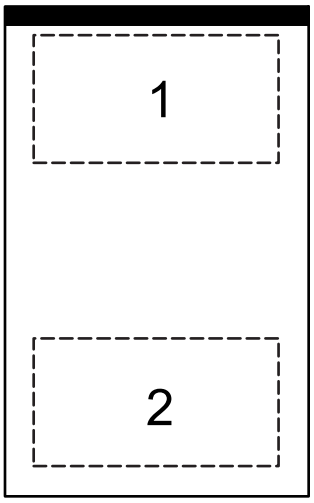
4 改訂履歴

日付	リビジョン	注
2018年7月	*	初版

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5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. Connect this pin to the line being protected.
2	GND	GND	Connect this pin to Ground

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical Fast Transient	IEC 61000-4-4 Peak Current at 25 °C		80	A
Surge Pulse	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Power at 25 °C		36	W
	IEC 61000-4-5 Surge (tp 8/20 µs) Peak Current at 25 °C		6	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings -JEDEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2500	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	±30000	V
		IEC 61000-4-2 Air Discharge, all pins	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0		3.6	V
T_A	Operating Free Air Temperature	–40		125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD351 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	409.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	216.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	140.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	81.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	140.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.6 Electrical Characteristics

At TA = 25°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 50 nA, across operating temperature range			3.6	V
$I_{LEAKAGE}$	Leakage current at 3.6 V	V_{IO} = 3.6 V, I/O to GND		0.1	10	nA
V_{BRF}	Breakdown voltage, I/O to GND (1)	I_{IO} = 1 mA	4.5		7.5	V
V_{FWD}	Forward Voltage, GND to I/O (1)	I_{IO} = 1 mA		0.8		V
V_{HOLD}	Holding voltage, I/O to GND (2)	I_{IO} = 1 mA		5.1		V
V_{CLAMP}	Clamping voltage	I_{PP} = 6 A (8/20 µs Surge), I/O to GND		6.1		V
		I_{PP} = 16 A (100 ns TLP), I/O to GND		6.5		V
		I_{PP} = 16 A (100 ns TLP), GND to I/O		2.5		V
R_{DYN}	Dynamic resistance	I/O to GND, 100 ns TLP, between 10 to 20 A I_{PP}		0.1		Ω
		GND to I/O , 100 ns TLP, between 10 to 20 A I_{PP}		0.08		Ω
C_{LINE}	Line capacitance, IO to GND	V_{IO} = 0 V, V_{p-p} = 30 mV, f = 1 MHz		1.8	2.2	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state

(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

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6.7 Typical Characteristics



図 1. TLP I-V Curve, I/O Pin to GND (t_p = 100 ns)

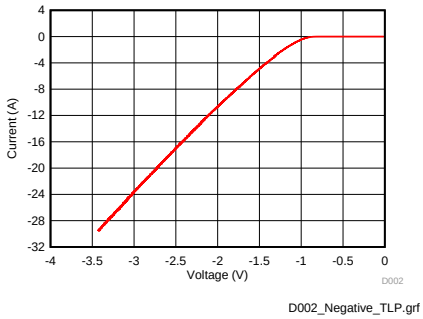


図 2. TLP I/V Curve, GND to I/O Pin (t_p = 100 ns)

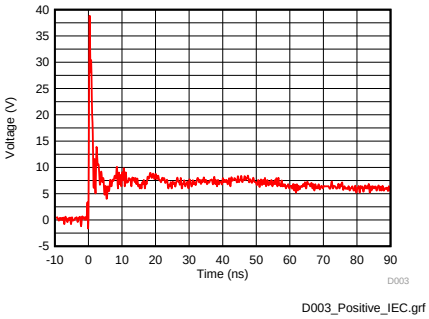


図 3. 8-kV IEC 61000-4-2 Clamping Voltage, I/O pin to GND

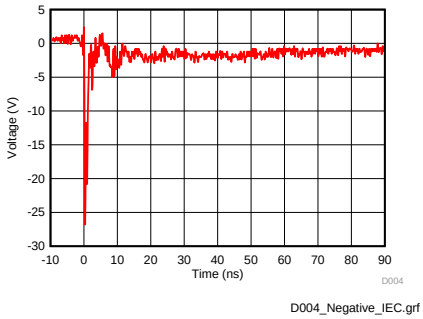


図 4. 8-kV IEC 61000-4-2 Clamping Voltage, GND to I/O Pin

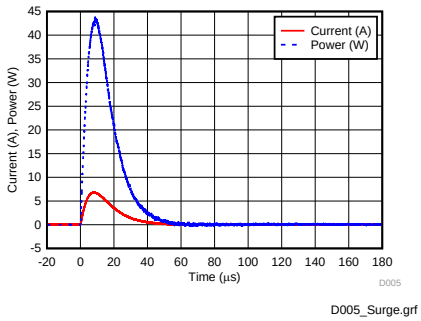


図 5. Surge Curve (IEC 61000-4-5, t_p = 8/20 µs), I/O Pin to GND

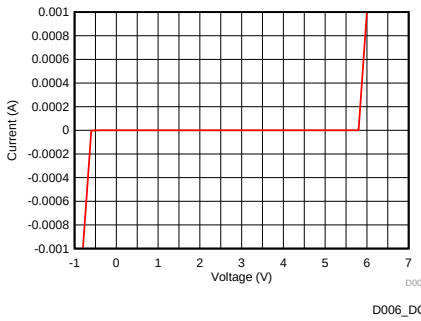


図 6. DC IV-Curve, I/O Pin to GND

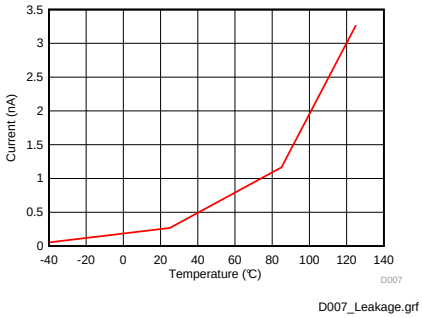


図 7. Leakage Current at 3.6 V Bias Voltage Across Temperature, I/O Pin to GND

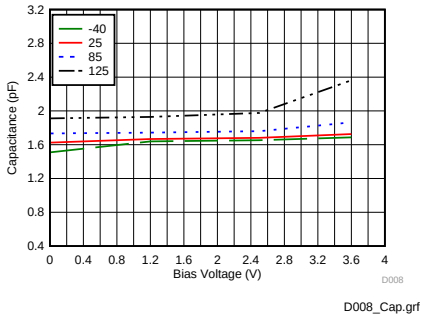


図 8. Capacitance Vs. Bias Voltage at Different Temperatures (°C)

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Typical Characteristics (continued)

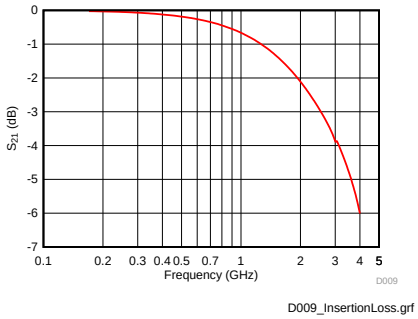


図 9. Insertion Loss Vs. Frequency

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7 Detailed Description

7.1 Overview

The ESD351 is a uni-directional ESD Protection Diode with 30 kV IEC 61000-4-2 level (Contact and Air) with ultra-low clamping voltage in a 1 mm × 0.6 mm package. The ultra-low clamping makes this device capable of protecting any ESD-sensitive pins.

7.2 Functional Block Diagram



7.3 Feature Description

ESD351 provides ESD protection up to ±30-kV contact and ±30-kV air gap per IEC 61000-4-2 standard. During an ESD event, ESD diode connected to the I/O pin turns on and diverts the current to ground. Additionally, ESD351 also provides protection against IEC 61000-4-5 Surge currents up to 6 A (8/20µs waveform) and up to 80 A per IEC 61000-4-4 (5/50 ns waveform, 4 kV with 50-Ω impedance) electrical fast transient (EFT) standard. The capacitance between the I/O pin and ground is 1.8 pF (typical) and 2.2 pF (maximum). The device features a low leakage current of 0.1 nA (typical) and 50 nA (maximum, across operating temperature range) with a bias of 3.6 V. The ESD diode at the I/O pin protects the ESD-sensitive devices by clamping the voltage to a low value of 6.5 V (I_{PP} = 16 A 100 ns TLP). The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The ESD351 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{FWD}. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD351 (usually within 10s of nano-seconds) the device reverts to passive.

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD351 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

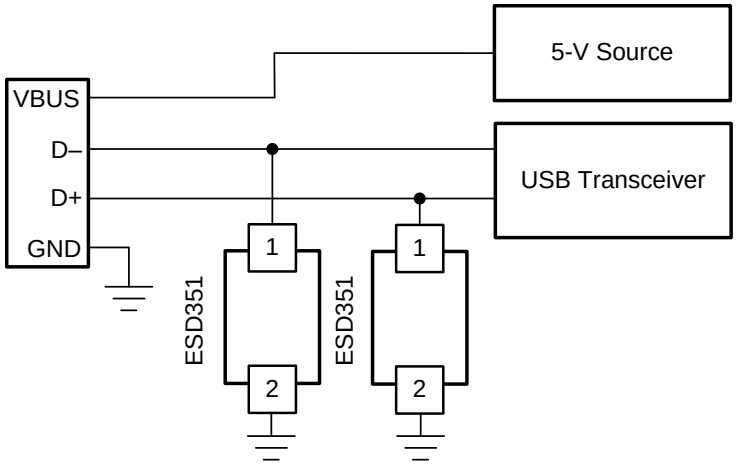


図 10. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two ESD351 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD351 supports signal ranges between 0 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

8.2.2.2 Operating Frequency

The ESD351 has a 1.8 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

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8.2.3 Application Curve

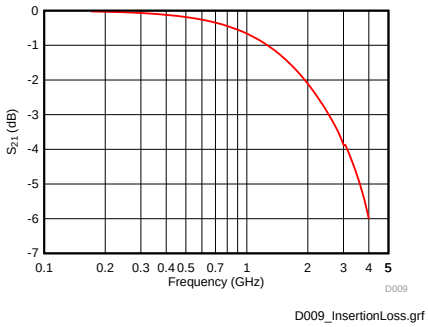


図 11. Insertion Loss

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9 Power Supply Recommendations

The ESD351 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (0 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

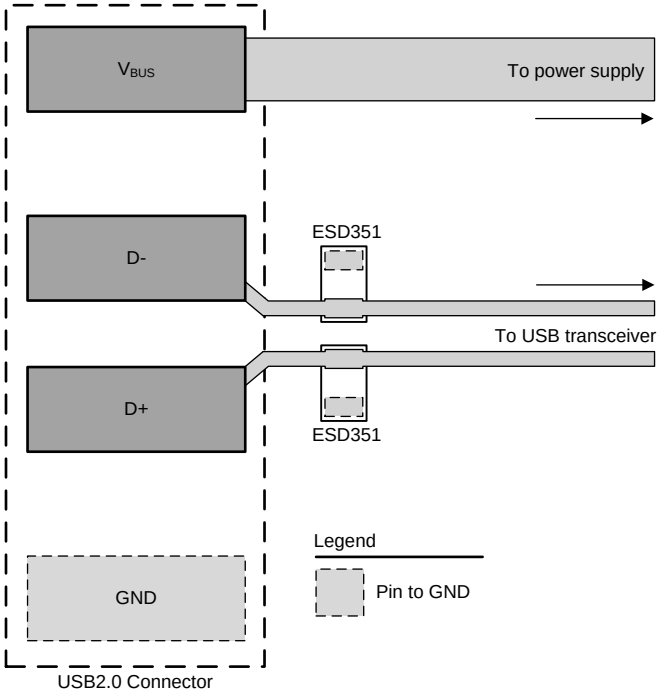


図 12. USB 2.0 ESD Layout

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11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『汎用ESDデバイス評価モジュール』、SLVUBG5

11.2 ドキュメントの更新通知を受け取る方法

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ESD351DPYR	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYR.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYRG4	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DE
ESD351DPYRG4.B	Active	Production	X1SON (DPY) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DE

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

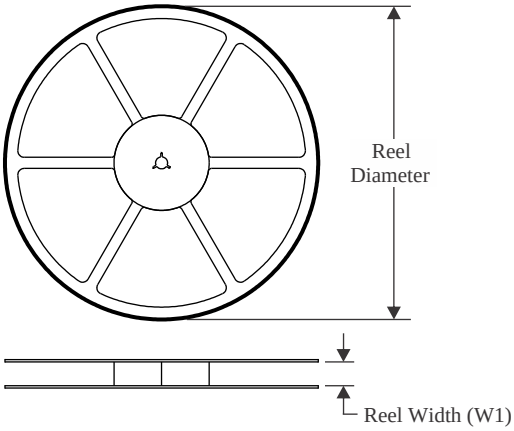
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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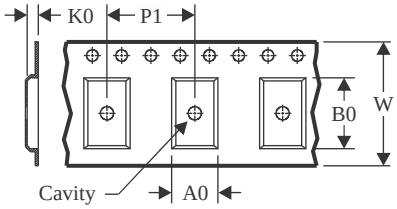
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

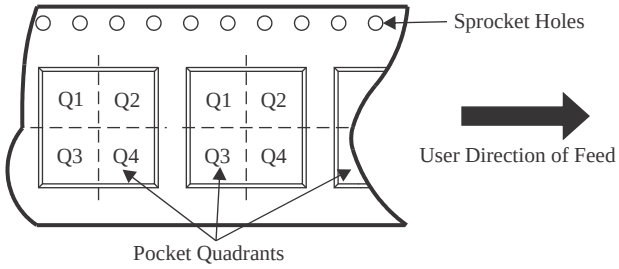


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

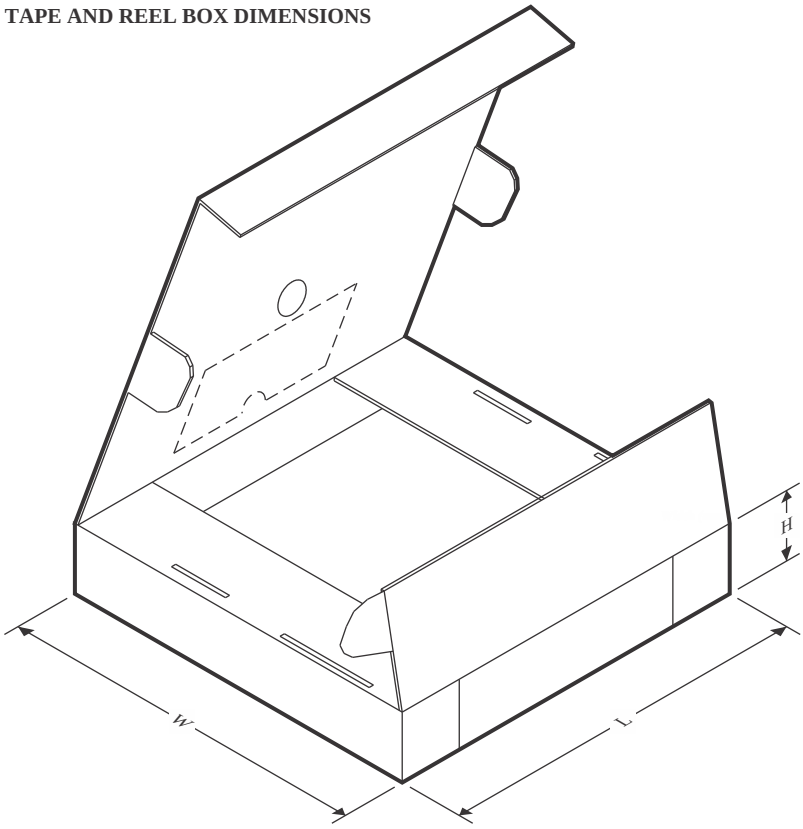
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD351DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
ESD351DPYR	X1SON	DPY	2	10000	178.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
ESD351DPYRG4	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD351DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
ESD351DPYR	X1SON	DPY	2	10000	208.0	191.0	35.0
ESD351DPYRG4	X1SON	DPY	2	10000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



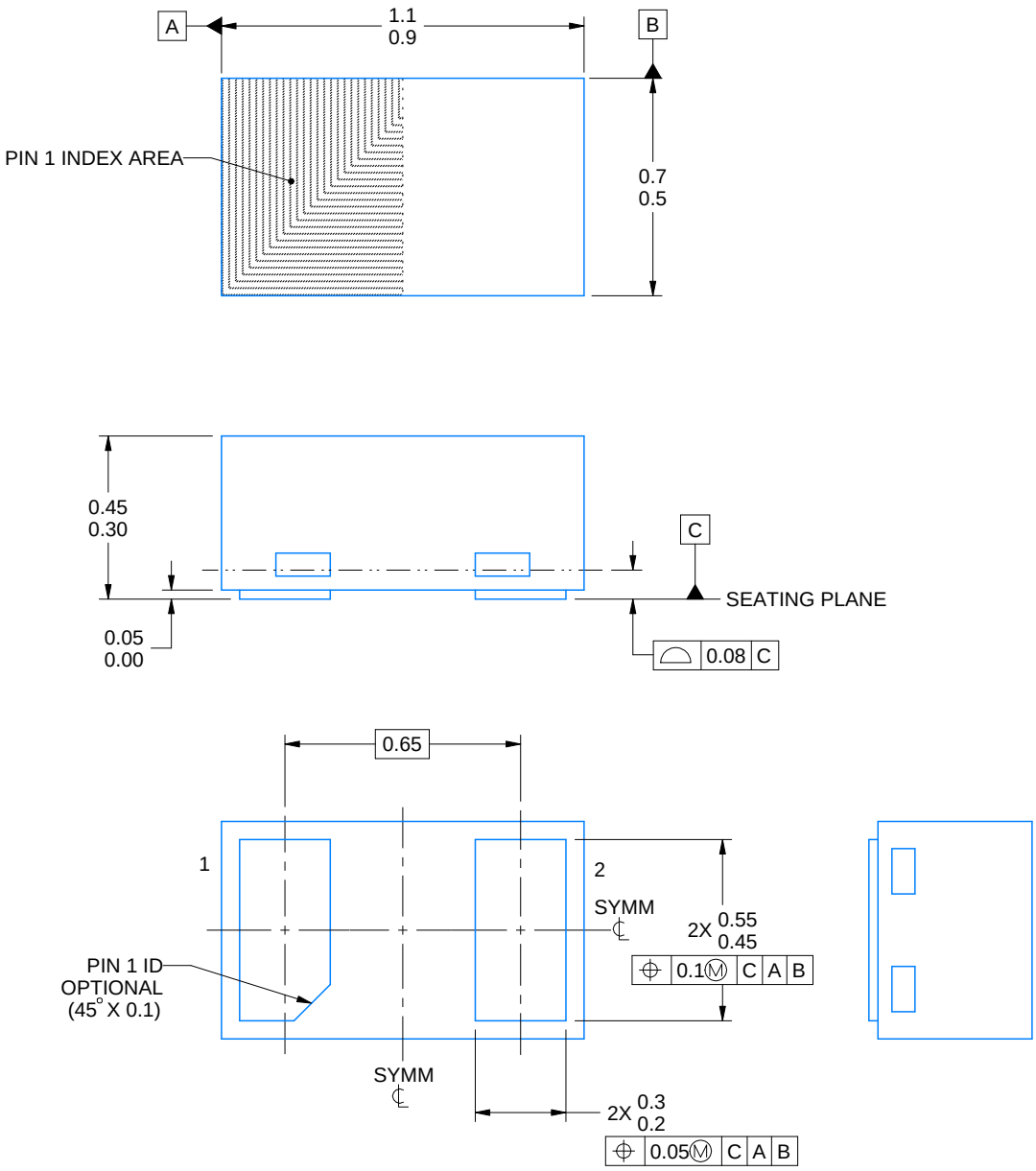
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

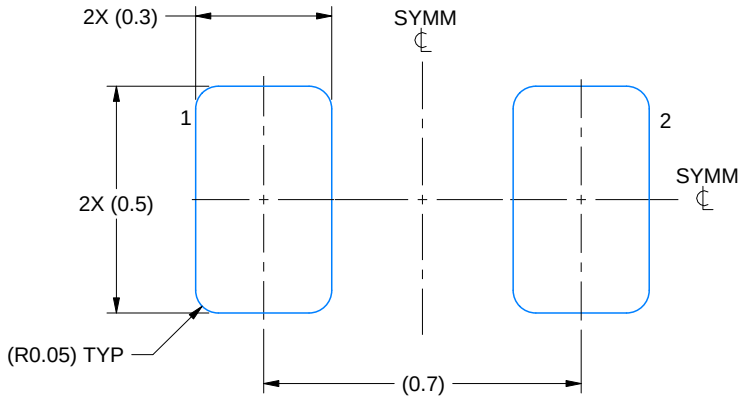
PLASTIC SMALL OUTLINE - NO LEAD



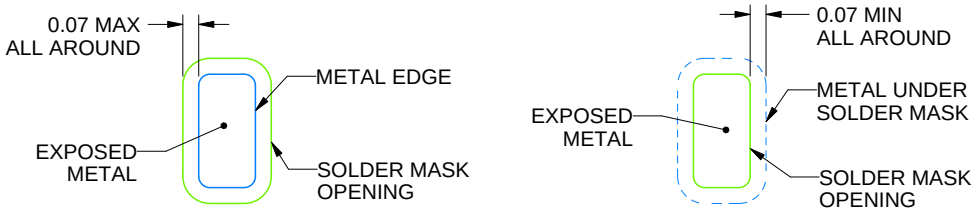
4224561/C 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X

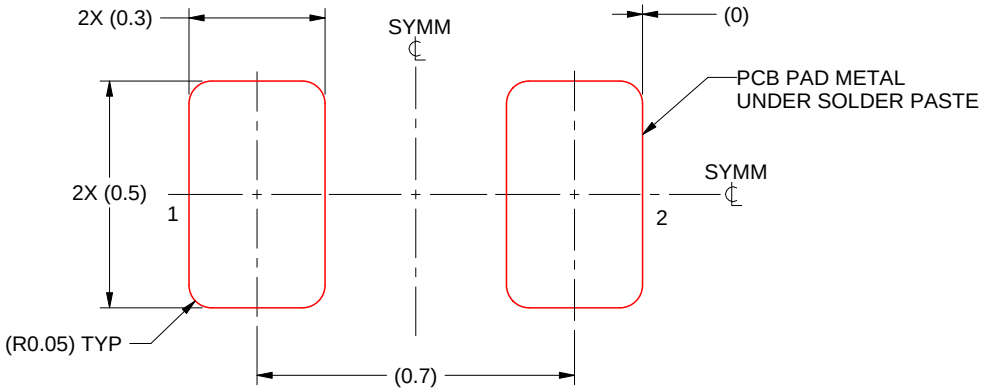


SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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