TEXAS INSTRUMENTS
INA199-Q1
JAJSDQ1E – MARCH 2016 – REVISED MAY 2021

# INA199-Q1 車載用、26V、双方向、ゼロドリフト、ローサイドまたはハイサイド、電圧出力、電流シャント・モニタ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - 温度グレード 1:–40℃～125℃、$T_A$
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 広い同相電圧範囲:-0.1V ～ 26V
- オフセット電圧:±150µV (最大値)
  (10mV フルスケールのシャント降下に対応)
- 精度
  - ゲイン誤差 (温度範囲全体での最大値)
    - ±1% (C バージョン)
    - ±1.5% (B バージョン)
  - オフセット・ドリフト:0.5µV/℃以下
  - ゲイン・ドリフト:10ppm/℃以下
- 選択可能なゲイン
  - INA199x1-Q1 :50V/V
  - INA199x2-Q1 :100V/V
  - INA199x3-Q1 :200V/V
- 静止電流:100µA 以下
- パッケージ:6 ピン SC70

## 2 アプリケーション

- ミラー
- ブレーキ・システム
- EGR バルブ
- パワー・シート
- 車体制御モジュール
- パワー・ウィンドウ
- シート・ヒーター
- ワイヤレス充電

## 3 概要

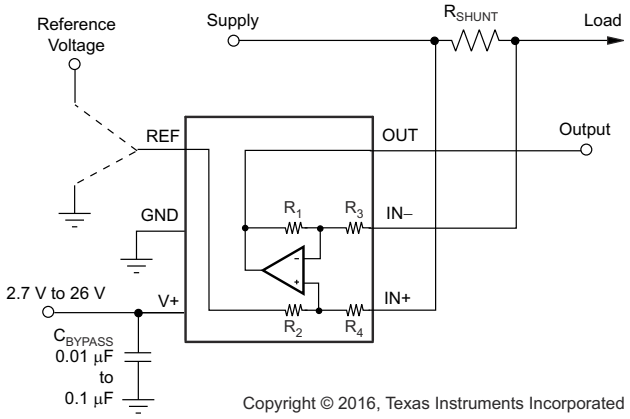
INA199-Q1 は、電源電圧にかかわらず -0.1V～26V の同相電圧でシャント両端の電圧降下を検出できる、電圧出力電流検出アンプです。3 つの固定ゲインを利用可能:50V/V、100V/V、200V/V。ゼロ・ドリフト・アーキテクチャの低いオフセットにより、シャントでの最大電圧降下がわずか 10mV フルスケールで電流センシングが可能です。

このデバイスは 2.7V～26V の単電源で動作し、消費電流は最大 100µA です。すべてのゲイン・オプションについて、-40℃～+125℃での動作が規定されており、6 ピンの SC70 パッケージで供給されます。

**製品情報**(1)

| 部品番号 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| INA199-Q1 | SC70 (6) | 2.00mm × 1.25mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。




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**概略回路図**

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision D (August 2019) to Revision E (May 2021)** — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新.....1
- 機能安全の箇条書き項目を追加.....1

**Changes from Revision C (August 2017) to Revision D (August 2019)** — **Page**

- Changed $V_S$ and $V_{IN}$ maximum values from 26 V to 28 V in *Absolute Maximum Ratings* table.....4
- Changed differential $V_{IN}$ minimum value from –26 V to –28 V in *Absolute Maximum Ratings* table.....4
- Added new Note 2 with caution regarding operation between 26 V and 28 V.....4

**Changes from Revision B (July 2016) to Revision C (August 2017)** — **Page**

- C バージョンのデバイスと関連コンテンツをデータシートに追加.....1
- Changed location of $V_S$ voltage range from *Electrical Characteristics* table to *Recommended Operating Conditions* table.....5
- Deleted redundant *Temperature Range* section from *Electrical Characteristics* table; all information already shown in *Thermal Information* and *Recommended Operating Conditions* tables.....5

**Changes from Revision A (May 2016) to Revision B (July 2016)** — **Page**

- Changed *ESD Ratings* table: changed HBM value and deleted machine model row .....4

**Changes from Revision * (March 2016) to Revision A (May 2016)** — **Page**

- 量産用にリリース.....1


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# 5 Device Comparison

表 5-1. Device Comparison

| PRODUCT | GAIN | $R_3$ AND $R_4$ | $R_1$ AND $R_2$ |
|---|---|---|---|
| INA199B1-Q1 | 50 V/V | 20 kΩ | 1 MΩ |
| INA199C1-Q1 | | | |
| INA199B2-Q1 | 100 V/V | 10 kΩ | 1 MΩ |
| INA199C2-Q1 | | | |
| INA199B3-Q1 | 200 V/V | 5 kΩ | 1 MΩ |
| INA199C3-Q1 | | | |

# 6 Pin Configuration and Functions

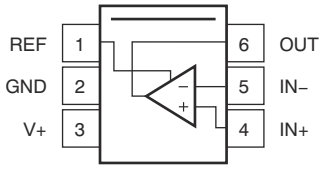



図 6-1. DCK Package 6-Pin SC70 Top View

表 6-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 2 | Analog | Ground |
| IN– | 5 | Analog input | Connect to load side of shunt resistor |
| IN+ | 4 | Analog input | Connect to supply side of shunt resistor |
| OUT | 6 | Analog output | Output voltage |
| REF | 1 | Analog input | Reference voltage, 0 V to V+ |
| V+ | 3 | Analog | Power supply, 2.7 V to 26 V |

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage(2) | | | 28 | V |
| Analog inputs, $V_{IN+}$, $V_{IN-}$ (2) (3) | Differential ($V_{IN+}$) – ($V_{IN-}$) | –28 | 28 | V |
| | Common-mode | GND – 0.1 | 28 | |
| REF input | | GND – 0.3 | (V+) + 0.3 | V |
| Output | | GND – 0.3 | (V+) + 0.3 | V |
| Temperature | Operating, $T_A$ | –40 | 125 | °C |
| | Junction, $T_J$ | | 150 | |
| | Storage, $T_{stg}$ | –65 | 150 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Sustained operation between 26 V and 28 V for more than a few minutes may cause permanent damage to the device.
(3) $V_{IN+}$ and $V_{IN-}$ are the voltages at the IN+ and IN– pins, respectively.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1)<br>HBM ESD classification level 2 | ±3500 | V |
| | | Charged-device model (CDM), per AEC Q100-002<br>CDM ESD classification level C6 | ±1000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CM}$ | Common-mode input voltage | | 12 | | V |
| $V_S$ | Operating supply voltage (applied to V+) | 2.7 | 5 | 26 | V |
| $T_A$ | Operating free-air temperature | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | INA199-Q1<br>DCK (SC70)<br>6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 227.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 79.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 72.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 3.6 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 70.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.


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## 7.5 Electrical Characteristics

at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, $V_{SENSE}$ = $V_{IN+}$ – $V_{IN–}$, and $V_{REF}$ = $V_S$ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | |
| $V_{CM}$ | Common-mode input voltage | $T_A$ = –40°C to +125°C | | –0.1 | | 26 | V |
| CMR | Common-mode rejection | $V_{IN+}$ = 0 V to 26 V, $V_{SENSE}$ = 0 mV, $T_A$ = –40°C to +125°C | | 100 | 120 | | dB |
| $V_{OS}$ | Offset voltage, RTI(1) | $V_{SENSE}$ = 0 mV | | | ±5 | ±150 | µV |
| $dV_{OS}/dT$ | $V_{OS}$ vs. temperature | $T_A$ = –40°C to +125°C | | | 0.1 | 0.5 | µV/°C |
| PSR | Power-supply rejection | $V_S$ = 2.7 V to 18 V, $V_{IN+}$ = 18 V, $V_{SENSE}$ = 0 mV | | | ±0.1 | | µV/V |
| $I_B$ | Input bias current | $V_{SENSE}$ = 0 mV | | | 28 | | µA |
| $I_{OS}$ | Input offset current | $V_{SENSE}$ = 0 mV | | | ±0.02 | | µA |
| **OUTPUT** | | | | | | | |
| G | Gain | INA199x1-Q1 | | | 50 | | V/V |
| | | INA199x2-Q1 | | | 100 | | |
| | | INA199x3-Q1 | | | 200 | | |
| | Gain error | $V_{SENSE}$ = –5 mV to 5 mV, $T_A$ = –40°C to +125°C | B version | | ±0.03% | ±1.5% | |
| | | | C version | | ±0.03% | ±1% | |
| | Gain error vs. temperature | $T_A$ = –40°C to +125°C | | | 3 | 10 | ppm/°C |
| | Nonlinearity error | $V_{SENSE}$ = –5 mV to +5 mV | | | ±0.01% | | |
| | Maximum capacitive load | No sustained oscillation | | | 1 | | nF |
| **VOLTAGE OUTPUT**(2) | | | | | | | |
| | Swing to V+ power-supply rail | $R_L$ = 10 kΩ to GND, $T_A$ = –40°C to +125°C | | | (V+) – 0.05 | (V+) – 0.2 | V |
| | Swing to GND | $R_L$ = 10 kΩ to GND, $T_A$ = –40°C to +125°C | | | ($V_{GND}$) + 0.005 | ($V_{GND}$) + 0.05 | V |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Bandwidth | $C_{LOAD}$ = 10 pF | INA199x1-Q1 | | 80 | | kHz |
| | | | INA199x2-Q1 | | 30 | | |
| | | | INA199x3-Q1 | | 14 | | |
| SR | Slew rate | | | | 0.4 | | V/µs |
| **NOISE, RTI**(1) | | | | | | | |
| | Voltage noise density | | | | 25 | | nV/√Hz |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current | $V_{SENSE}$ = 0 mV | | | 65 | 100 | µA |
| | $I_Q$ over temperature | $T_A$ = –40°C to +125°C | | | | 115 | µA |

(1) RTI = referred-to-input.
(2) See typical characteristic curve, *Output Voltage Swing vs. Output Current* (図 7-6).

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## 7.6 Typical Characteristics

performance measured with the INA199B3-Q1 at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, and $V_{REF}$ = $V_S$ / 2 (unless otherwise noted)

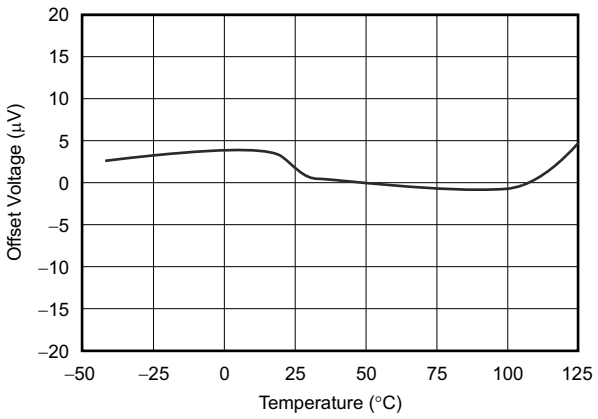



**図 7-1. Offset Voltage vs. Temperature**

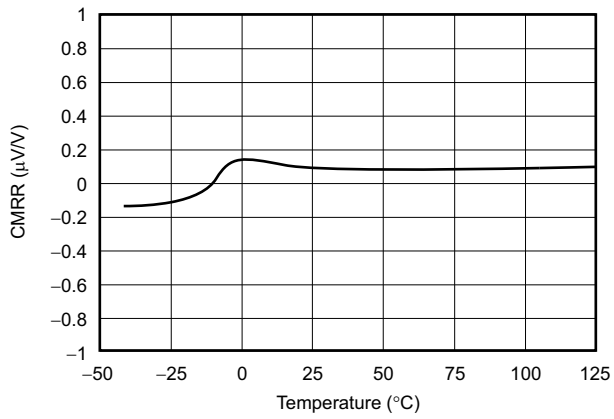
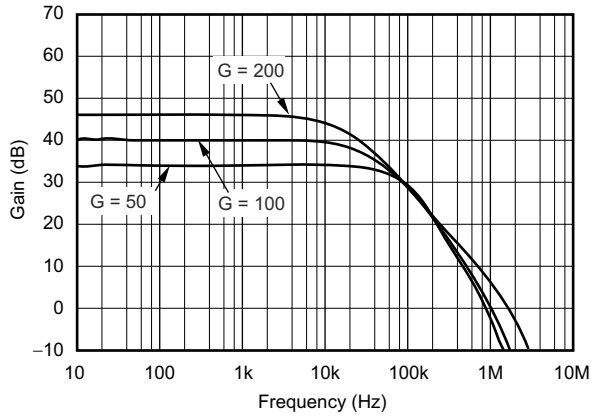
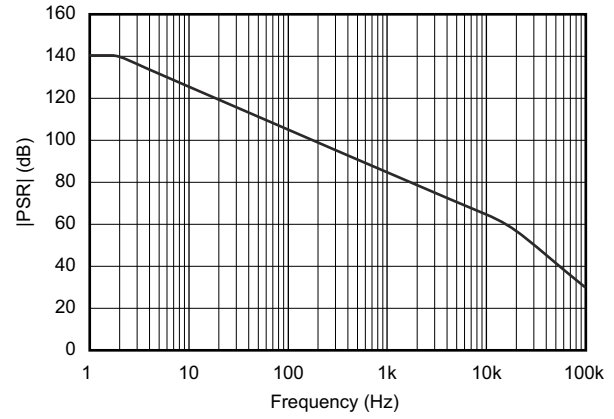



**図 7-2. Common-Mode Rejection Ratio vs. Temperature**



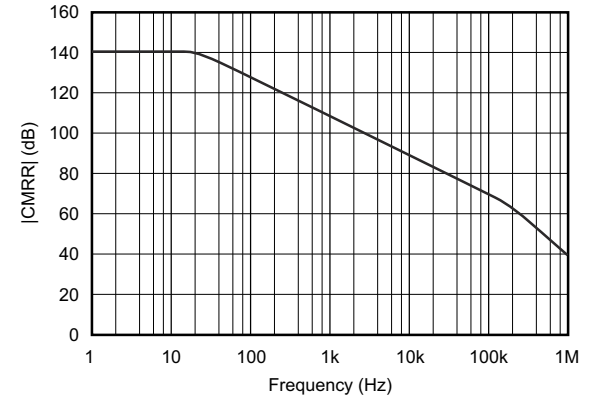

$V_{CM}$ = 0 V, $V_{DIF}$ = 15-$mV_{PP}$ sine

**図 7-3. Gain vs. Frequency**




$V_S$ = 5 V + 250-mV sine disturbance, $V_{CM}$ = 0 V, $V_{DIF}$ = shorted, $V_{REF}$ = 2.5 V

**図 7-4. Power-Supply Rejection Ratio vs. Frequency**




$V_S$ = 5 V, $V_{CM}$ = 1-V sine, $V_{DIF}$ = shorted, $V_{REF}$ = 2.5 V

**図 7-5. Common-Mode Rejection Ratio vs. Frequency**

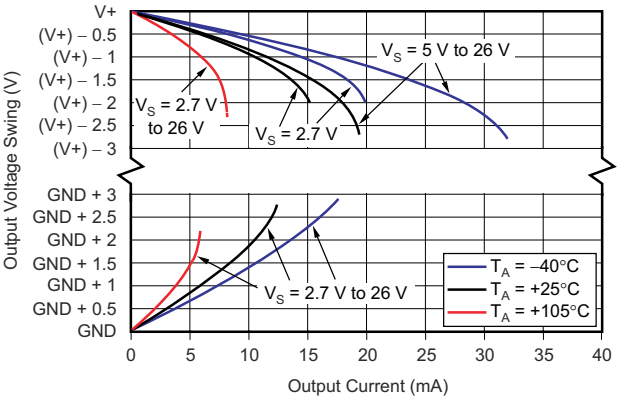
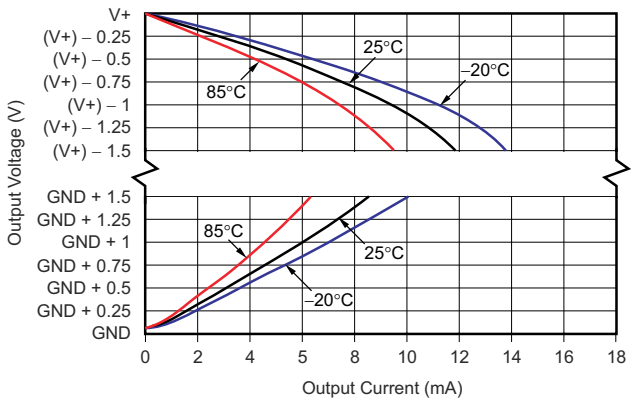



**図 7-6. Output Voltage Swing vs. Output Current**


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## 7.6 Typical Characteristics (continued)

performance measured with the INA199B3-Q1 at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, and $V_{REF}$ = $V_S$ / 2 (unless otherwise noted)




$V_S$ = 2.5 V

**図 7-7. Output Voltage Swing vs. Output Current**

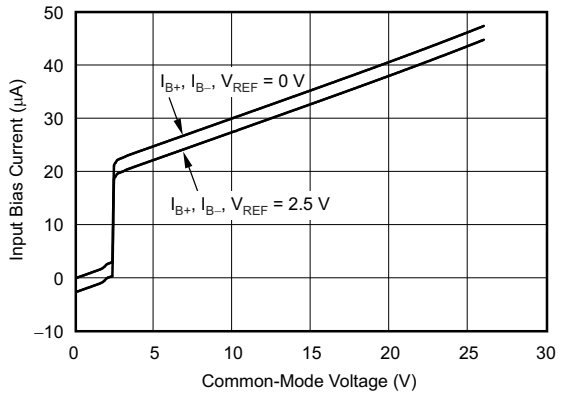



**図 7-8. Input Bias Current vs. Common-Mode Voltage With Supply Voltage = 5 V**

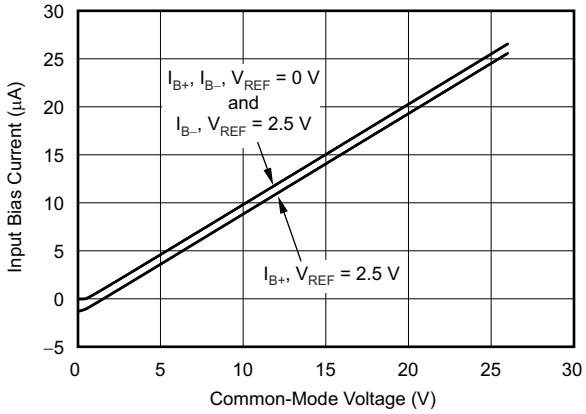



**図 7-9. Input Bias Current vs. Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)**

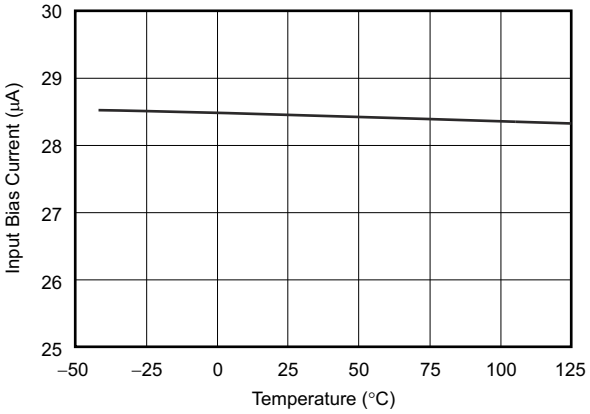



**図 7-10. Input Bias Current vs. Temperature**

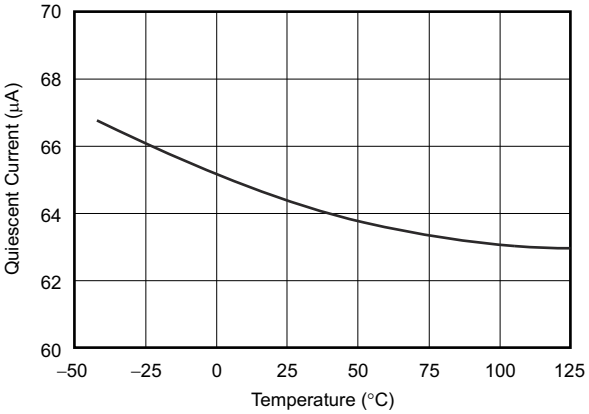
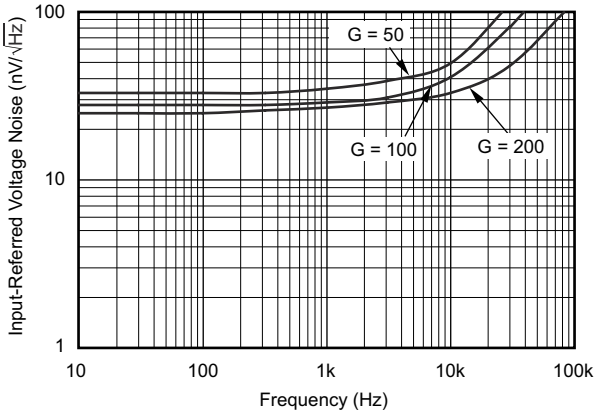



**図 7-11. Quiescent Current vs. Temperature**



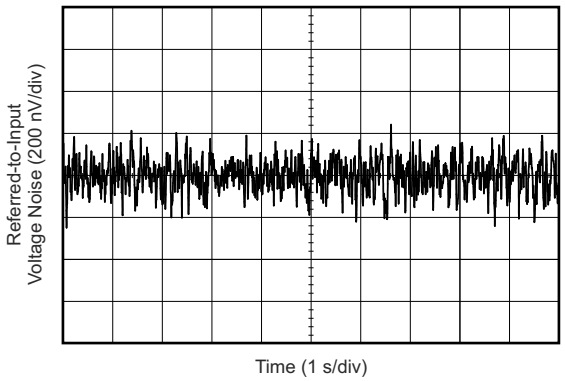

$V_S$ = ±2.5 V, $V_{REF}$ = 0 V, $V_{IN–}$ and $V_{IN+}$ = 0 V

**図 7-12. Input-Referred Voltage Noise vs. Frequency**

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## 7.6 Typical Characteristics (continued)

performance measured with the INA199B3-Q1 at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, and $V_{REF}$ = $V_S$ / 2 (unless otherwise noted)




$V_S$ = ±2.5 V, $V_{CM}$ = 0 V, $V_{DIF}$ = 0 V, $V_{REF}$ = 0 V

**図 7-13. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)**

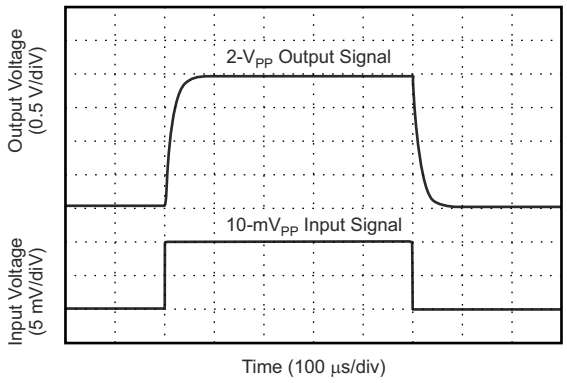



**図 7-14. Step Response (10-$mV_{PP}$ Input Step)**

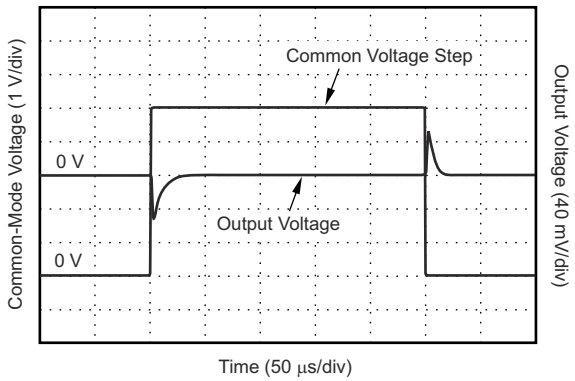
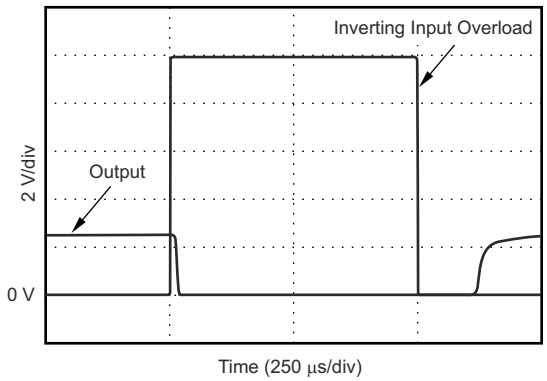
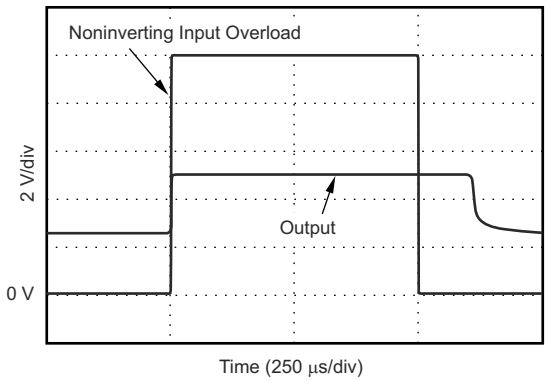



**図 7-15. Common-Mode Voltage Transient Response**



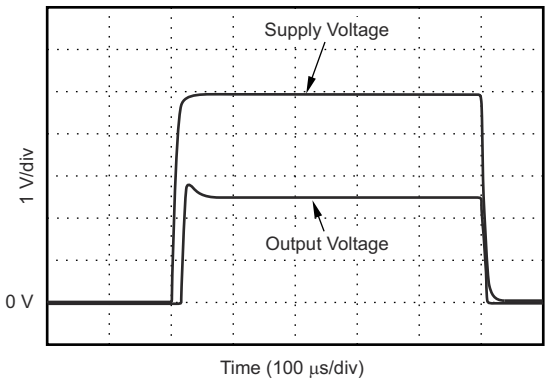

$V_S$ = 5 V, $V_{CM}$ = 12 V, $V_{REF}$ = 2.5 V

**図 7-16. Inverting Differential Input Overload**




$V_S$ = 5 V, $V_{CM}$ = 12 V, $V_{REF}$ = 2.5 V

**図 7-17. Noninverting Differential Input Overload**



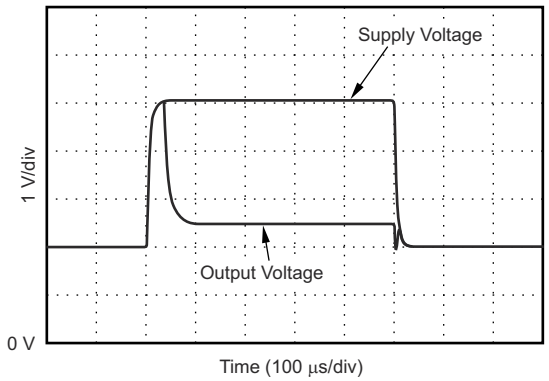

$V_S$ = 5 V, 1-kHz step with $V_{DIF}$ = 0 V, $V_{REF}$ = 2.5 V

**図 7-18. Start-Up Response**


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## 7.6 Typical Characteristics (continued)

performance measured with the INA199B3-Q1 at $T_A$ = 25°C, $V_S$ = 5 V, $V_{IN+}$ = 12 V, and $V_{REF}$ = $V_S$ / 2 (unless otherwise noted)




$V_S$ = 5 V, 1-kHz step with $V_{DIF}$ = 0 V, $V_{REF}$ = 2.5 V

**図 7-19. Brownout Recovery**

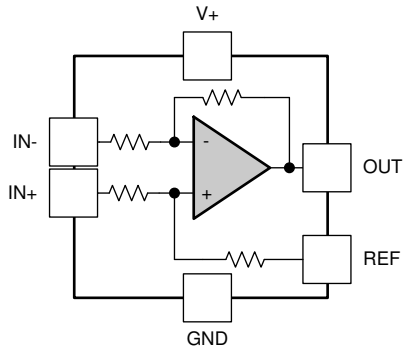
# 8 Detailed Description

## 8.1 Overview

The INA199-Q1 is a 26-V, common-mode, zero-drift topology, current-sensing amplifier that can be used in both low-side and high-side configurations. The device is a specially-designed, current-sensing amplifier that is able to accurately measure voltages developed across a current-sensing resistor on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 150 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to +125°C.

## 8.2 Functional Block Diagram




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## 8.3 Feature Description

### 8.3.1 Zero-Drift Offset

The zero-drift offset performance of the INA199-Q1 offers several benefits. Most often, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current-shunt monitors typically require a full-scale range of 100 mV.

### 8.3.2 Accuracy

The INA199-Q1 series gives equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

### 8.3.3 Choice of Gain Options

The INA199-Q1 series provides three gain options: 50 V/V, 100 V/V, and 200 V/V, Some applications must measure current over a wide dynamic range that can take advantage of the low offset on the low end of the measurement. Most often, these applications use the lower gain of 50 V/V or 100 V/V to accommodate larger shunt drops on the upper end of the scale. For instance, the INA199B1-Q1 (with a factory-set gain of 50 V/V) operating on a 3.3-V supply can easily handle a full-scale shunt drop of 60 mV, with only 150 µV of offset. See the *Electrical Characteristics* for more information.

## 8.4 Device Functional Modes

The INA199-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V. The maximum power supply voltage for this device is 26 V.


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# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

The INA199-Q1 measures the voltage developed across a current-sensing resistor when current passes through it. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout this section.

### 9.1.1 Basic Connections

図 9-1 shows the basic connections for the INA199-Q1. The input pins, IN+ and IN–, must be connected as close as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

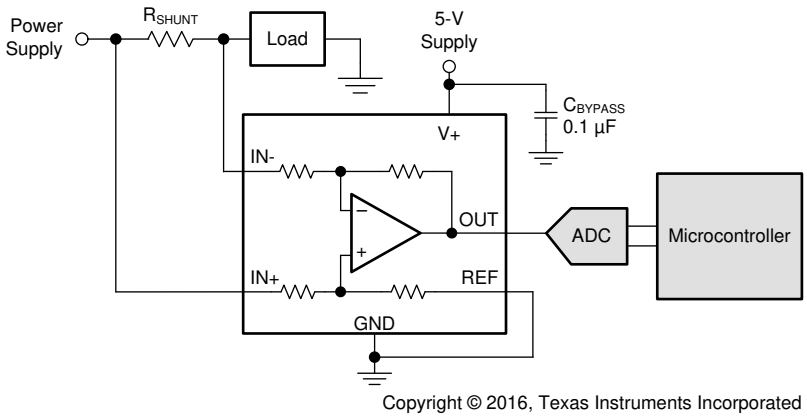
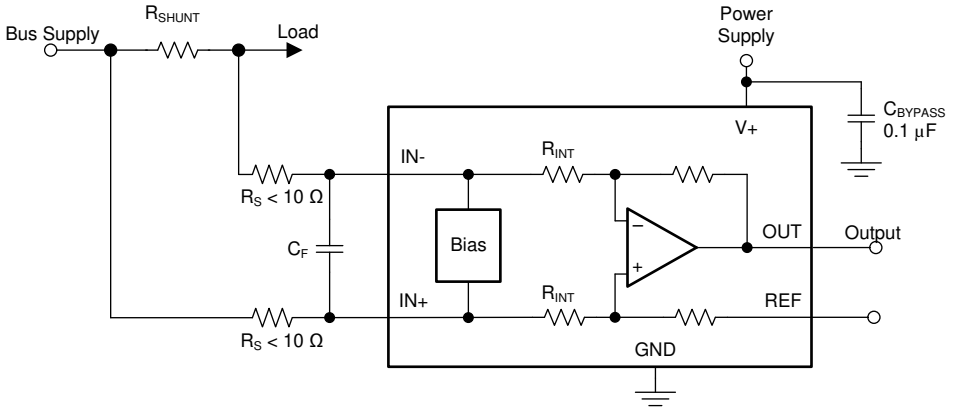



**図 9-1. Typical Application**

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

### 9.1.2 Input Filtering

An obvious and straightforward filtering location is at the device output. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the device input pins. This location, though, does require consideration of the ±30% tolerance of the internal resistances. 図 9-2 shows a filter placed at the inputs pins.




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**図 9-2. Filter at Input Pins**

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be 10 Ω (or less if possible) to reduce any affect to accuracy. The internal bias network shown in 図 9-2 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistor add to the measurement can be calculated using 式 1, where the gain error factor is calculated using 式 2.

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \tag{1}$$

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \tag{2}$$

where:

- $R_{INT}$ is the internal input resistor ($R_3$ and $R_4$) and
- $R_S$ is the external series resistance

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based on both the external series resistance value and the internal input resistors, $R_3$ and $R_4$ (or $R_{INT}$, as shown in 図 9-2). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. The equation used to calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given in 式 2.


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With the adjustment factor equation including the device internal input resistance, this factor varies with each gain version, as listed in 表 9-1. Each individual device gain error factor is listed in 表 9-2.

**表 9-1. Input Resistance**

| PRODUCT | GAIN (V/V) | $R_{INT}$ (kΩ) |
|---|---|---|
| INA199B1-Q1 | 50 | 20 |
| INA199C1-Q1 | | |
| INA199B2-Q1 | 100 | 10 |
| INA199C2-Q1 | | |
| INA199B3-Q1 | 200 | 5 |
| INA199C3-Q1 | | |

**表 9-2. Device Gain Error Factor**

| PRODUCT | SIMPLIFIED GAIN ERROR FACTOR |
|---|---|
| INA199B1-Q1 | $\frac{20{,}000}{(17 \times R_S) + 20{,}000}$ |
| INA199C1-Q1 | |
| INA199B2-Q1 | $\frac{10{,}000}{(9 \times R_S) + 10{,}000}$ |
| INA199C2-Q1 | |
| INA199B3-Q1 | $\frac{1000}{R_S + 1000}$ |
| INA199C3-Q1 | |

The gain error that can be expected from the addition of the external series resistors can then be calculated based on 式 1.

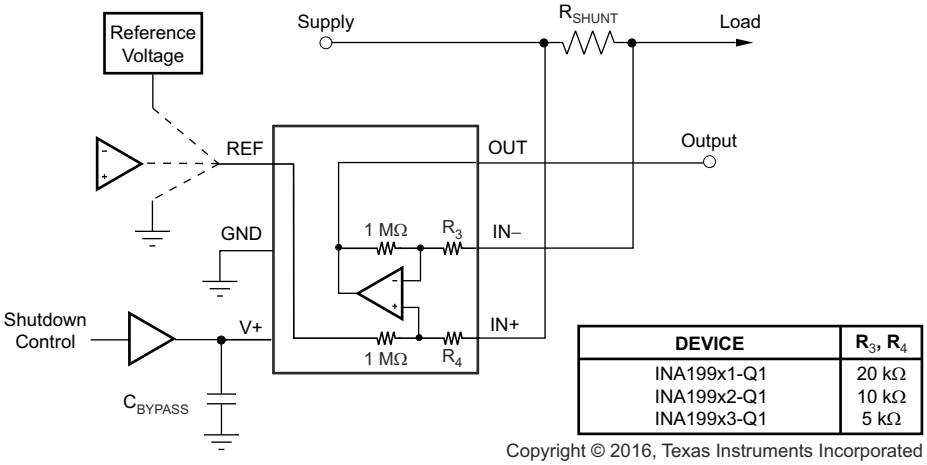
For example, when using an INA199B2-Q1 and the corresponding gain error equation from 表 9-2, a series resistance of 10-Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 式 1, resulting in a gain error of approximately 0.89% solely because of the external 10-Ω series resistors. Using an INA199B1-Q1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

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### 9.1.3 Shutting Down the INA199-Q1

Although the INA199-Q1 series does not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INA199-Q1. This gate or switch turns on and turns off the INA199-Q1 power-supply quiescent current.

However, in current-shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INA199-Q1 in shutdown mode as shown in 図 9-3.




1-MΩ paths from shunt inputs to the reference and the INA199-Q1 outputs.

**図 9-3. Basic Circuit for Shutting Down the INA199-Q1 With a Grounded Reference**

There is typically slightly more than a 1-MΩ impedance (from the combination of the 1-MΩ feedback and 5-kΩ input resistors) from each input of the INA199-Q1 to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or operational amplifier is powered when the INA199-Q1 is shut down, then the calculation is direct; instead of assuming a 1-MΩ impedance to ground, assume a 1-MΩ impedance to the reference voltage. If the reference or operational amplifier is also shut down, some knowledge of the reference or operational amplifier output impedance under shutdown conditions is required. For instance, if the reference source functions as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA199-Q1 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage applied across a 1-MΩ resistor.

**Note**

When the device is powered up, an additional, nearly constant, and well-matched 25 µA of current flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the resulting 1-MΩ resistors are the only effects from this current.


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### 9.1.4 REF Input Impedance Effects

As with any difference amplifier, the INA199-Q1 series common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, the REF pin must be buffered by an operational amplifier.

In systems where the INA199-Q1 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of the external impedance on the REF input can be cancelled. 図 9-4 shows a method of capturing the output from the INA199-Q1 by using the REF pin as a reference.

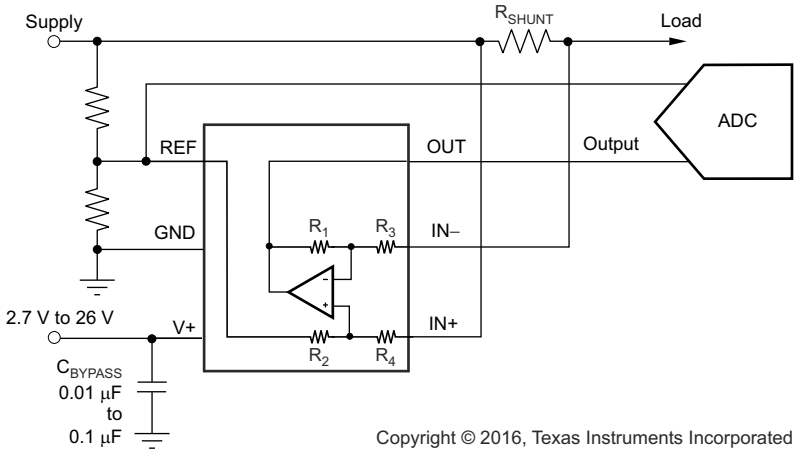



**図 9-4. Sensing the INA199-Q1 to Cancel Effects of Impedance on the REF Input**

### 9.1.5 Using the INA199-Q1 With Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA199-Q1 series can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only zener diodes or zener-type transient absorbers (sometimes referred to as *transzorbs*); any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors (as shown in 図 9-5) as a working impedance for the zener. Keeping these resistors as small as possible is preferable, most often approximately 10 Ω. Larger values can be used with an affect on gain as discussed in the *Input Filtering* section. Many applications are satisfied with a 10-Ω resistor along with conventional zener diodes of the lowest power rating that can be found because this circuit limits only short-term transients. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523. See the *TIDA-00302 Transient Robustness for Current Shunt Monitor* TI design (TIDU473) for more information on transient robustness and current-shunt monitor input protection.

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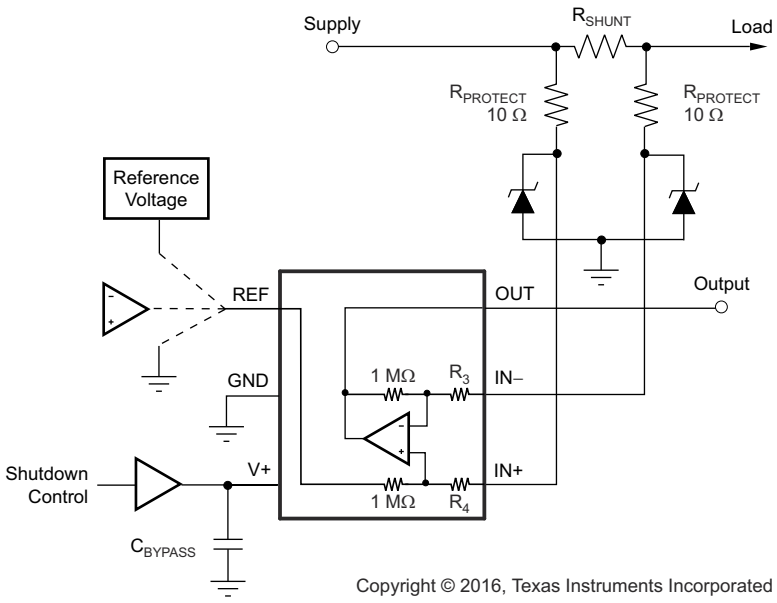



**図 9-5. INA199-Q1 Transient Protection Using Dual Zener Diodes**

In the event that low-power zeners do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. This method is illustrated in 図 9-6. In either of these examples, the total board area required by the INA199-Q1 with all protective components is less than that of an 8-pin SOIC package, and only slightly greater than that of an 8-pin VSSOP package.

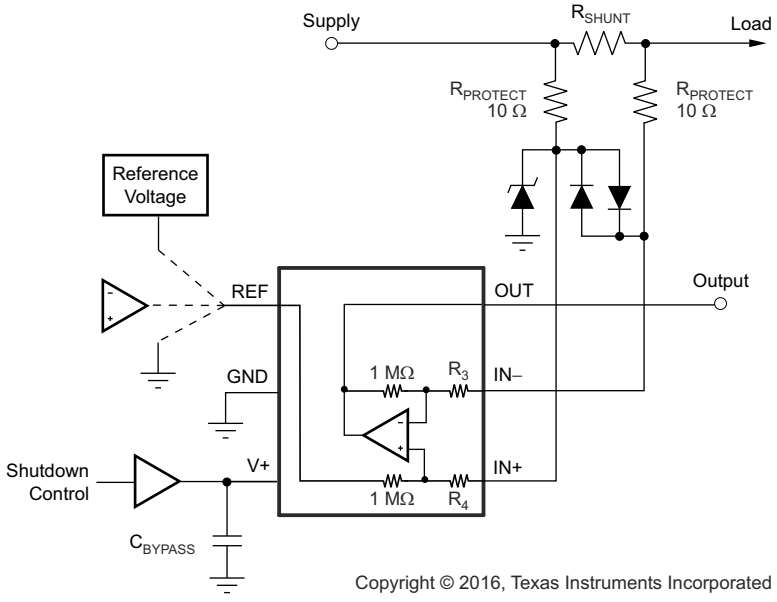
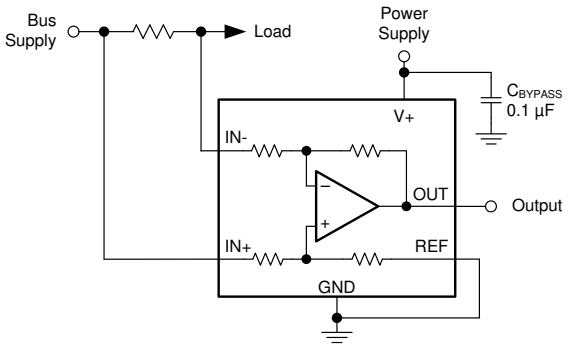



**図 9-6. INA199-Q1 Transient Protection Using a Single Transzorb and Input Clamps**


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## 9.2 Typical Applications

### 9.2.1 Unidirectional Operation




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**図 9-7. Unidirectional Application Schematic**

#### *9.2.1.1 Design Requirements*

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional), depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when current is not flowing by connecting the REF pin to ground; see 図 9-7. When the input signal increases, the output voltage at the OUT pin increases.

#### *9.2.1.2 Detailed Design Procedure*

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, buffering the reference voltage connected to the REF pin is recommended.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when a differential input signal is not present. This method is similar to the output-saturated low condition without an input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

#### *9.2.1.3 Application Curve*

An example output response of a unidirectional configuration is shown in 図 9-8. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

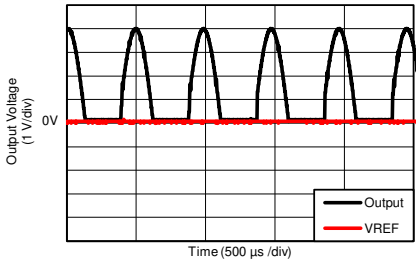



**図 9-8. Unidirectional Application Output Response**

### 9.2.2 Bidirectional Operation

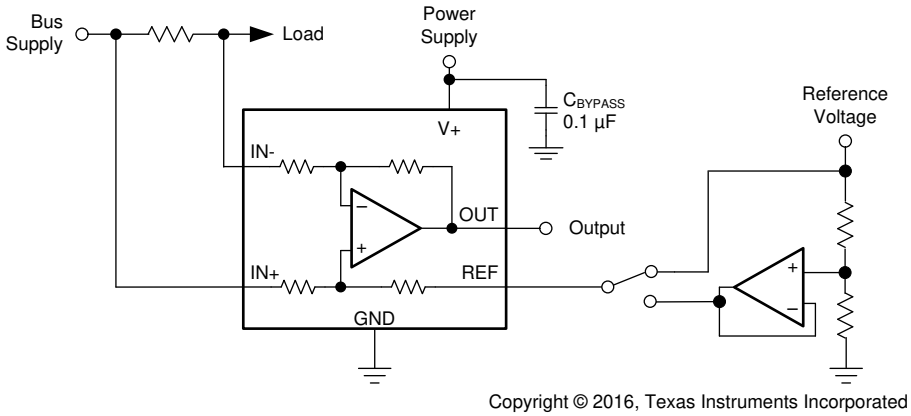



**図 9-9. Bidirectional Application Schematic**

#### *9.2.2.1 Design Requirements*

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

#### *9.2.2.2 Detailed Design Procedure*

The ability to measure this current flowing in both directions is enabled by applying a voltage on the REF pin, as shown in 図 9-9. The voltage applied to REF ($V_{REF}$) sets the output state that corresponds to the zero-input level state. The output then responds by rising above $V_{REF}$ for positive differential signals (relative to the IN– pin) and falling below $V_{REF}$ for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, $V_{REF}$ is typically set at mid-scale for an equal signal range in both current directions. In some cases, however, $V_{REF}$ is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal do not need to be symmetrical.

#### *9.2.2.3 Application Curve*

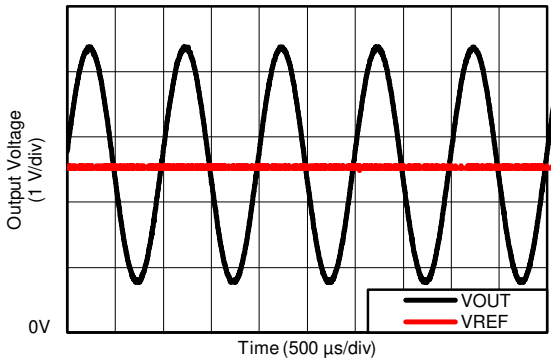



**図 9-10. Bidirectional Application Output Response**


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# 10 Power Supply Recommendations

The input circuitry of the INA199-Q1 can accurately measure beyond its power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. Furthermore, the INA199-Q1 can withstand the full input signal range up to the 26-V range in the input pins, regardless of whether the device has power applied or not.

# 11 Layout

## 11.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a kelvin or 4-wire connection. This connection technique makes certain that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the supply and ground pins. Using a bypass capacitor with a value of 0.1 µF is recommended. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

## 11.2 Layout Example

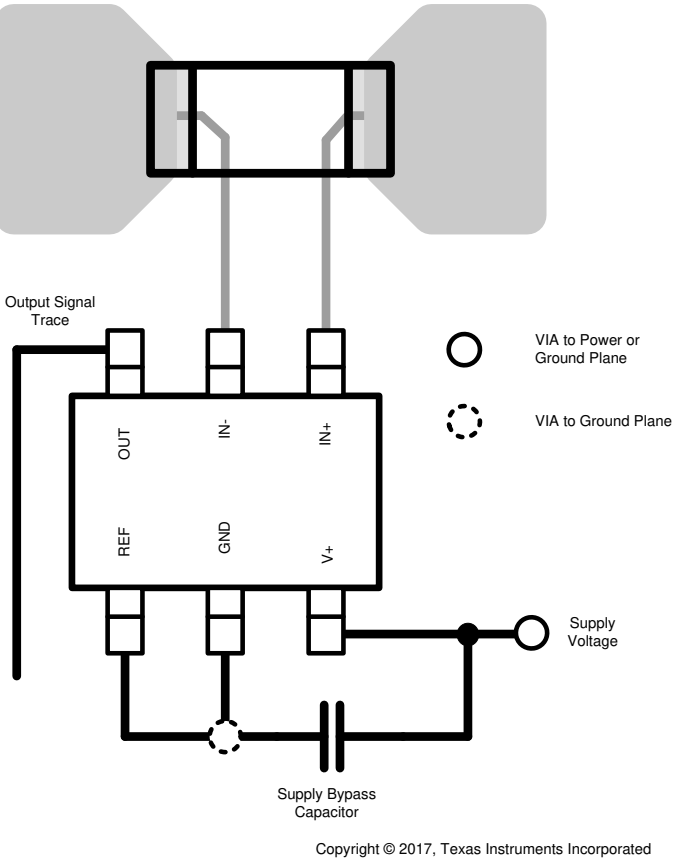



**図 11-1. Recommended Layout**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA199B1-B3EVM* user's guide
- Texas Instruments, *TIDA-00302 Transient Robustness for Current Shunt Monitor* TI design

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 サポート・リソース

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## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| INA199B1QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | - | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13C |
| INA199B1QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | - | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13C |
| INA199B2QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13D |
| INA199B2QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13D |
| INA199B3QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13E |
| INA199B3QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 13E |
| INA199C1QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17A |
| INA199C1QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17A |
| INA199C2QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17B |
| INA199C2QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17B |
| INA199C3QDCKRQ1 | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17C |
| INA199C3QDCKRQ1.B | Active | Production | SC70 (DCK) \| 6 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 17C |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF INA199-Q1 :**

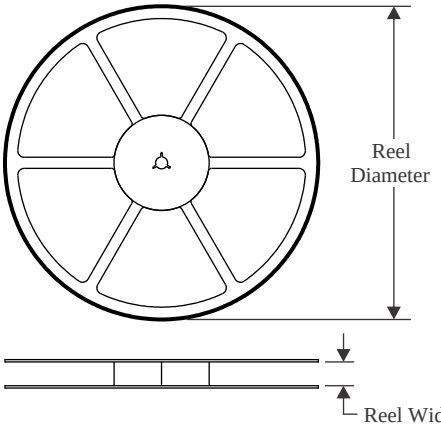
- Catalog : INA199

NOTE: Qualified Version Definitions:

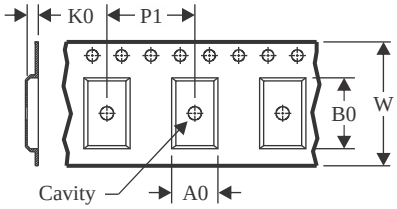
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

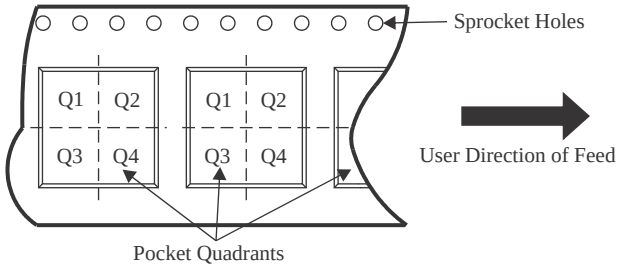



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

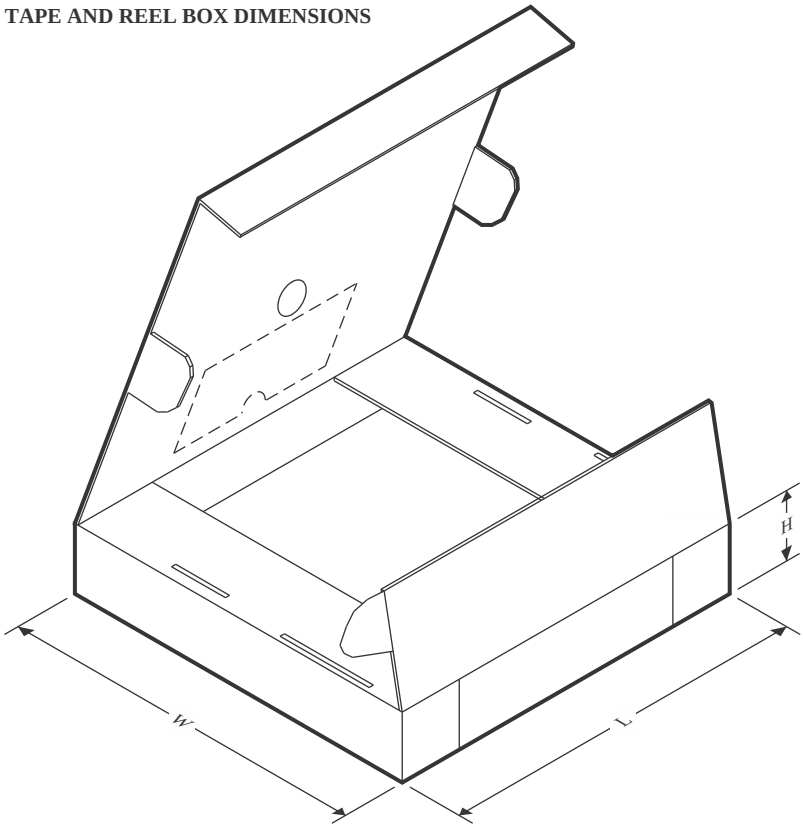
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INA199B1QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B2QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199B3QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199C1QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199C2QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| INA199C3QDCKRQ1 | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

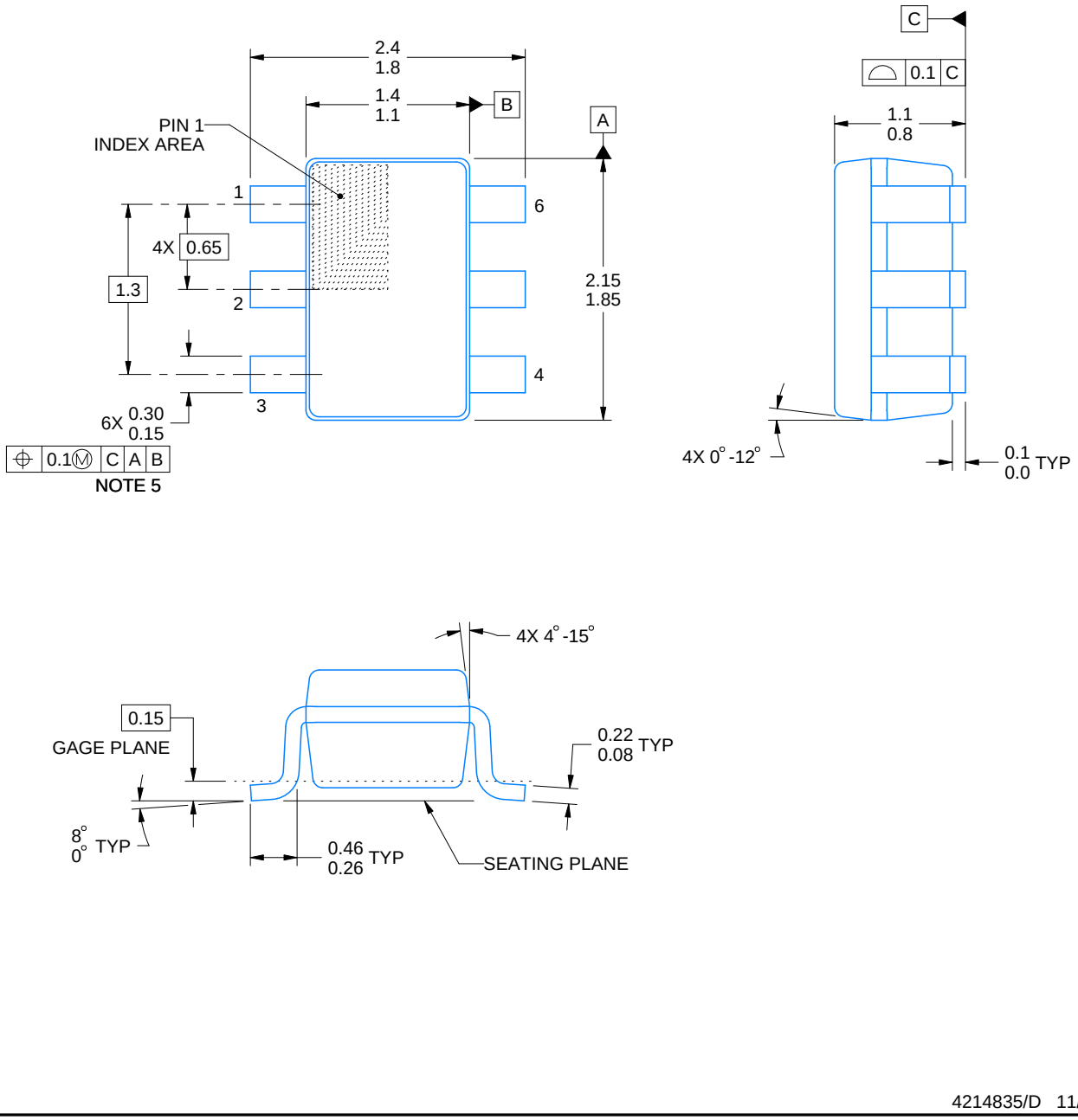
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| INA199B1QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199B2QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199B3QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199C1QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199C2QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| INA199C3QDCKRQ1 | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |

# PACKAGE OUTLINE

## DCK0006A

## SOT - 1.1 max height

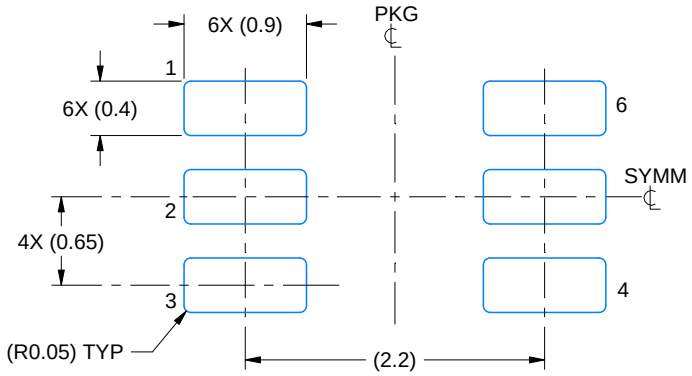
SMALL OUTLINE TRANSISTOR



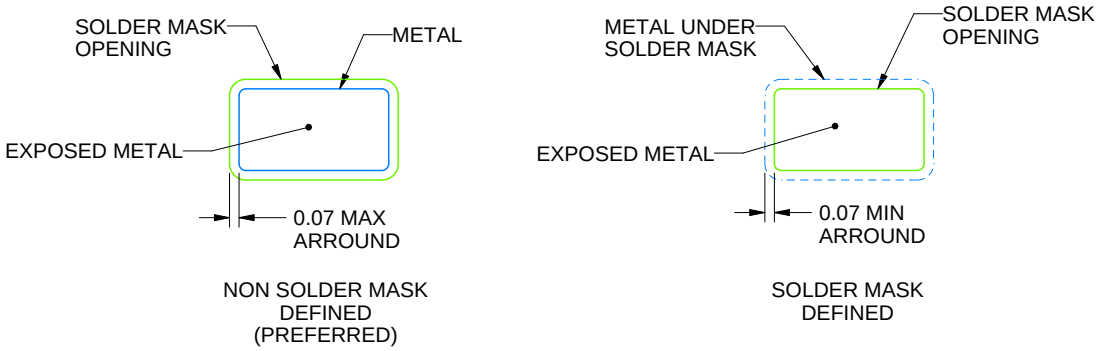

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

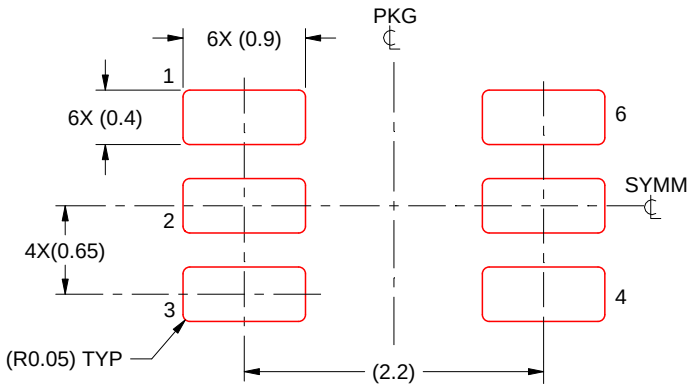



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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