TEXAS INSTRUMENTS

INA200, INA201, INA202

JAJSCM4E – NOVEMBER 2006 – REVISED SEPTEMBER 2017

INA20x オープン・ドレイン・コンパレータおよび基準電圧搭載のハイサイド測定、電流シャント・モニタ

1 特長

- 完全な電流検出ソリューション
- 3つのゲイン・オプションを利用可能:
  - INA200: 20V/V
  - INA201: 50V/V
  - INA202: 100V/V
- 0.6Vの内部基準電圧
- 内蔵のオープン・ドレイン・コンパレータ
- コンパレータのラッチ機能
- 同相範囲: -16V～80V
- 高精度: 温度範囲にわたって最大誤差3.5%
- 帯域幅: 500kHz (INA200)
- 静止電流: 1800µA (最大値)
- パッケージ: SOIC-8、VSSOP-8

2 アプリケーション

- ノートブック・コンピュータ
- 携帯電話
- 通信機器
- オートモーティブ（車載）
- パワー・マネージメント
- バッテリ充電器
- 溶接機器

3 概要

INA200、INA201、INA202デバイスは、ハイサイドの電圧出力、電流シャント・モニタで、コンパレータが内蔵されています。INA20xデバイスは、-16V～80Vの範囲の同相電圧において、シャントの両端の電圧降下を検出できます。INA20xシリーズは20V/V、50V/V、100V/Vの3つの出力電圧スケールで、500kHzまでの帯域幅で利用可能です。

INA200、INA201、INA202デバイスにはオープン・ドレインのコンパレータと、0.6Vのスレッショルドを提供する内部基準電圧が組み込まれています。外部の分圧抵抗により、電流トリップ点を設定します。コンパレータにはラッチ機能があり、$\overline{\text{RESET}}$ピンをグランドに接続(またはオープンに保持)することで透過的にできます。

INA200、INA201、INA202デバイスは2.7V～18Vの単一電源で動作し、消費電流は最大1800µAです。パッケージは、超小型のVSSOP-8とSOIC-8を選択できます。

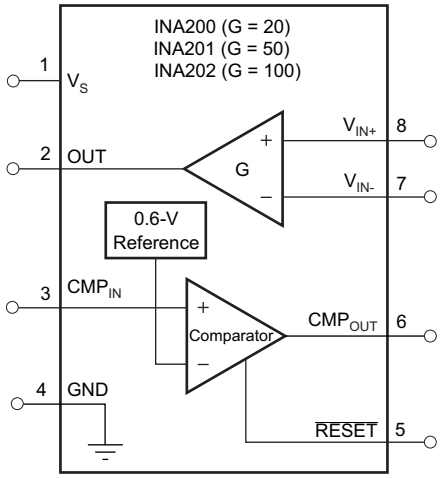
すべてのバージョンは、拡張動作温度範囲の-40℃～+125℃で動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
INA200	SOIC (8)	4.90mm×3.91mm
INA201 INA202	VSSOP (8)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (October 2015) から **Revision E** に変更 **Page**

- Reformatted *Thermal Information* table note ... 4
- Corrected typo in *Voltage Output* section in *Electrical Characteristics* table ... 6
- 追加 text to *Comparator* subsection in *Feature Description* section ... 14
- 追加 図 31 to *Feature Description* section ... 18
- 追加 *Output vs Supply Ramp Considerations* subsection in *Feature Description* section ... 23
- 追加 図 36, 図 37, and 図 38 ... 23

Revision C (October 2010) から **Revision D** に変更 **Page**

- Added *ESD Ratings* table, *Thermal Information* table, Feature Description section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

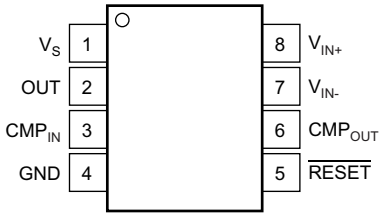
Revision B (October, 2007) から **Revision C** に変更 **Page**

- 表紙の図を修正 ... 1
- データシートのタイトルを 変更 ... 1
- 現行の標準に合わせてドキュメントのフォーマットを更新 ... 1

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5 Pin Configuration and Functions

DGK and D Packages
8-Pin VSSOP and SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CMP_{IN}	3	Analog input	Comparator input
CMP_{OUT}	6	Analog output	Comparator output
GND	4	Analog	Ground
OUT	2	Analog output	Output voltage
$\overline{RESET}$	5	Analog input	Comparator reset pin, active low
V_{IN-}	7	Analog input	Connect to shunt low side
V_{IN+}	8	Analog input	Connect to shunt high side
V_S	1	Analog	Power supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S		2.7	18	V
Current-shunt monitor analog inputs, V_{IN+}, V_{IN-}	Differential (V_{IN+}) – (V_{IN-})	–18	18	V
	Common-mode(2)	–16	80	V
Comparator analog input and reset pins(2)		GND – 0.3	(V_S) + 0.3	V
Analog output, OUT(2)		GND – 0.3	(V_S) + 0.3	V
Comparator output, OUT(2)		GND – 0.3	18	V
Input current into any pin(2)			5	mA
Operating temperature		–55	150	°C
Junction temperature		–65	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This voltage may exceed the ratings shown if the current at that pin is limited to 5 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	–16	12	80	V
V_S	Operating supply voltage	2.7	12	18	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		INA20x		UNIT
		D (SOIC)	DGK (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.5	162.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.4	37.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.7	82.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.8	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.9	81.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: Current-Shunt Monitor

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{SENSE}	Full-scale sense input voltage	$V_{SENSE} = V_{IN+} - V_{IN-}$		0.15	$(V_S - 0.25)$ / Gain	V
V_{CM}	Common-mode input range	T_A = –40°C to 125°C	–16		80	V
CMR	Common-mode rejection	V_{IN+} = –16 V to 80 V	80	100		dB
		V_{IN+} = 12 V to 80 V, T_A = –40°C to 125°C	100	123		dB
V_{OS}	Offset voltage, RTI(1)	T_A = 25°C		±0.5	±2.5	mV
		T_A = 25°C to 125°C			±3	mV
		T_A = –40°C to 25°C			±3.5	mV
dV_{OS}/dT	Offset voltage, RTI, vs temperature	T_{MIN} to T_{MAX}, T_A = –40°C to 125°C		5		µV/°C
PSR	Offset voltage, RTI, vs power supply	V_{OUT} = 2 V, V_{IN+} = 18 V, 2.7 V, T_A = –40°C to 125°C		2.5	100	µV/V
I_B	Input bias current, V_{IN-} pin	T_A = –40°C to 125°C		±9	±16	µA

(1) Offset is extrapolated from measurements of the output at 20-mV and 100-mV V_{SENSE}.

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Electrical Characteristics: Current-Shunt Monitor (continued)

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = GND, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT (V_{SENSE} ≥ 20 mV)							
G	Gain	INA200			20		V/V
		INA201			50		V/V
		INA202			100		V/V
	Gain error	V_{SENSE} = 20 mV to 100 mV			±0.2%	±1%	
		V_{SENSE} = 20 mV to 100 mV, T_A = –40°C to 125°C				±2%	
	Total output error(2)	V_{SENSE} = 120 mV, V_S = 16 V			±0.75%	±2.2%	
		V_{SENSE} = 120 mV, V_S = 16 V, T_A = –40°C to 125°C				±3.5%	
	Nonlinearity error(3)	V_{SENSE} = 20 mV to 100 mV			±0.002%		
R_O	Output impedance				1.5		Ω
	Maximum capacitive load	No sustained oscillation			10		nF
OUTPUT (V_{SENSE} < 20 mV)(4)							
	Output	INA200, INA201, INA202	–16 V ≤ V_{CM} < 0 V		300		mV
		INA200	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			0.4	V
		INA201	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			1	V
		INA202	0 V ≤ V_{CM} ≤ V_S, V_S = 5 V			2	V
		INA200, INA201, INA202	V_S < V_{CM} ≤ 80 V		300		mV
VOLTAGE OUTPUT(5)							
	Output swing to the positive rail	$V_{IN–}$ = 11 V, V_{IN+} = 12 V, T_A = –40°C to 125°C			(V_s) – 0.15	(V_s) – 0.25	V
	Output swing to GND(6)	$V_{IN–}$ = 0 V, V_{IN+} = –0.5 V, T_A = –40°C to 125°C			(GND) + 0.004	(GND) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	INA200	C_{LOAD} = 5 pF		500		kHz
		INA201	C_{LOAD} = 5 pF		300		kHz
		INA202	C_{LOAD} = 5 pF		200		kHz
	Phase margin	C_{LOAD} < 10 nF			40		°C
SR	Slew rate				1		V/µs
	Settling time (1%)	V_{SENSE} = 10 mV_{PP} to 100 mV_{PP}, C_{LOAD} = 5 pF			2		µs
NOISE, RTI							
	Voltage noise density				40		nV/√Hz

(2) Total output error includes effects of gain error and V_{OS}.
(3) Linearity is best fit to a straight line.
(4) For details on this region of operation, see *Accuracy Variations* section in *Device Functional Modes*.
(5) See 図 8.
(6) Specified by design.

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6.6 Electrical Characteristics: Comparator

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, and $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
	Threshold	T_A = 25°C	590	608	620	mV
		T_A = –40°C to 125°C	586		625	mV
	Hysteresis(1)	T_A = –40°C to 85°C		–8		mV
INPUT BIAS CURRENT(2)						
	Input bias current, CMP_{in} PIN			0.005	10	nA
	Input bias current, CMP_{in} PIN, vs temperature	T_A = –40°C to 125°C			15	nA
INPUT VOLTAGE RANGE						
	Input voltage range, CMP_{in} PIN		0 V to V_S – 1.5 V			V
OUTPUT (OPEN-DRAIN)						
	Large-signal differential voltage gain	CMP V_{OUT} 1 V to 4 V, R_L ≥ 15 kΩ connected to 5 V		200		V/mV
I_{LKG}	High-level leakage current(3)(4)	V_{ID} = 0.4 V, V_{OH} = V_S		0.0001	1	µA
V_{OL}	Low-level output voltage(3)	V_{ID} = –0.6 V, I_{OL} = 2.35 mA		220	300	mV
RESPONSE TIME						
	Response time(5)	R_L to 5 V, C_L = 15 pF, 100-mV Input Step with 5-mV overdrive		1.3		µs
$\overline{\text{RESET}}$						
	$\overline{\text{RESET}}$ threshold(6)			1.1		V
	Logic input impedance			2		MΩ
	Minimum $\overline{\text{RESET}}$ pulse width			1.5		µs
	$\overline{\text{RESET}}$ propagation delay			3		µs

(1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; refer to 図 1.
(2) Specified by design.
(3) V_{ID} refers to the differential voltage at the comparator inputs.
(4) Open-drain output can be pulled to the range of 2.7 to 18 V, regardless of V_S.
(5) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.
(6) The $\overline{\text{RESET}}$ input has an internal 2 MΩ (typical) pull-down. Leaving $\overline{\text{RESET}}$ open results in a LOW state, with transparent comparator operation.

6.7 Electrical Characteristics: General

at T_A = 25°C, V_S = 12 V, V_{CM} = 12 V, V_{SENSE} = 100 mV, R_L = 10 kΩ to GND, $R_{PULL-UP}$ = 5.1 kΩ connected from CMP_{OUT} to V_S, and CMP_{IN} = 1 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Operating power supply	T_A = –40°C to 125°C	2.7		18	V
I_Q	Quiescent current	V_{OUT} = 2 V		1350	1800	µA
		V_{SENSE} = 0 mV, T_A = –40°C to 125°C			1850	µA
	Comparator power-on reset threshold(1)			1.5		V
TEMPERATURE						
	Specified temperature		–40		125	°C
	Operating temperature		–55		150	°C
	Storage temperature		–65		150	°C
θ_{JA}	Thermal resistance	VSSOP-8 Surface-Mount		200		°C/W
		SOIC-8		150		°C/W

(1) The INA200, INA201, and INA202 are designed to power-up with the comparator in a defined reset state as long as $\overline{\text{RESET}}$ is open or grounded. The comparator is in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If $\overline{\text{RESET}}$ is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

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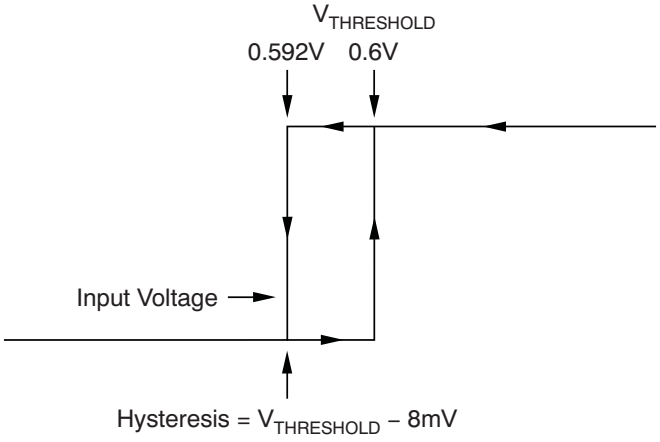


図 1. Typical Comparator Hysteresis

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6.8 Typical Characteristics

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

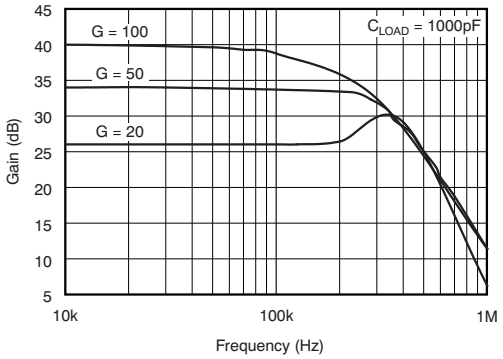


図 2. Gain vs Frequency

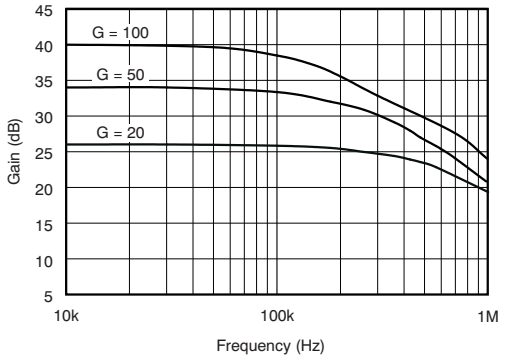


図 3. Gain vs Frequency

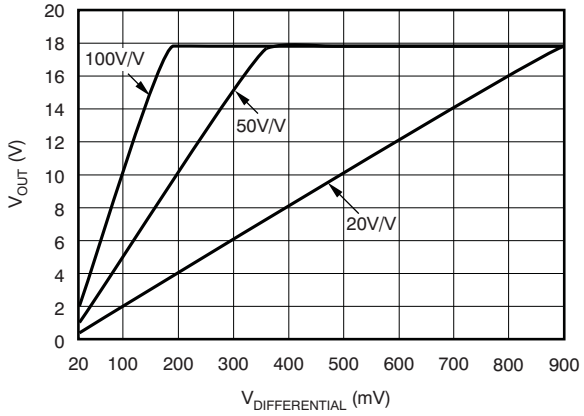


図 4. Gain Plot

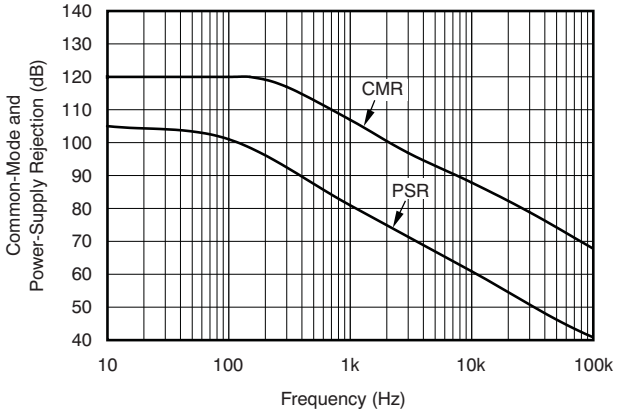


図 5. Common-Mode and Power-Supply Rejection vs Frequency

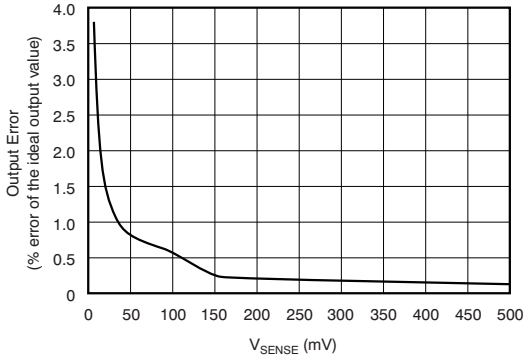


図 6. Output Error vs V_{SENSE}

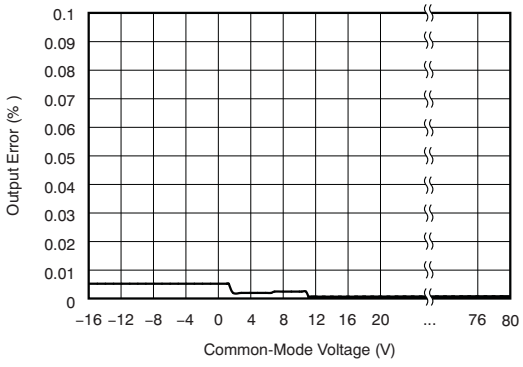


図 7. Output Error vs Common-Mode Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

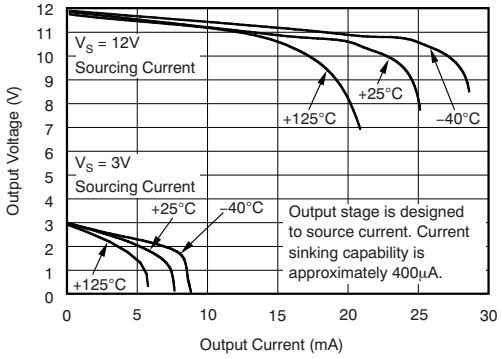


図 8. Positive Output Voltage Swing vs Output Current

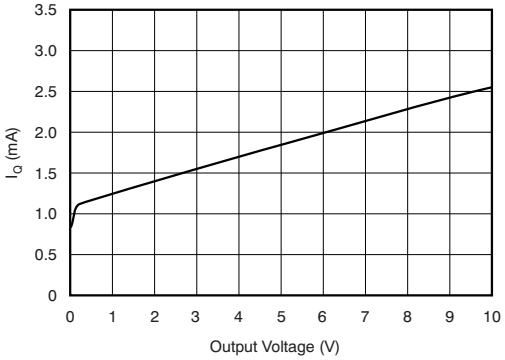


図 9. Quiescent Current vs Output Voltage

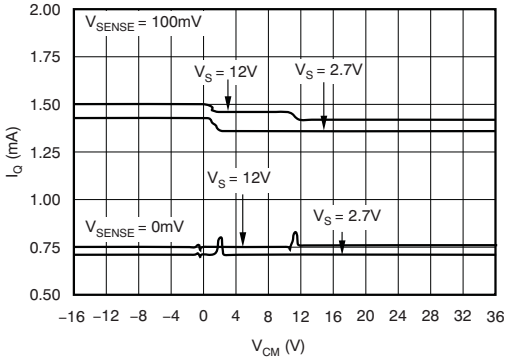


図 10. Quiescent Current vs Common-Mode Voltage

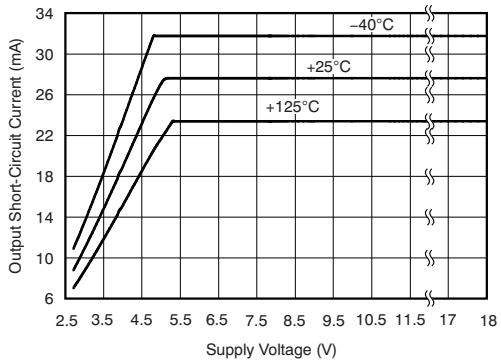


図 11. Output Short-Circuit Current vs Supply Voltage

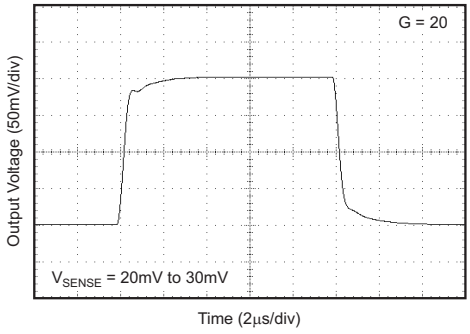


図 12. Step Response

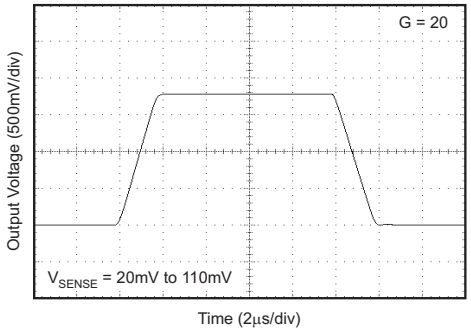


図 13. Step Response

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

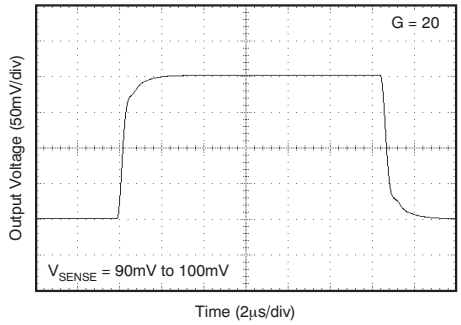


図 14. Step Response

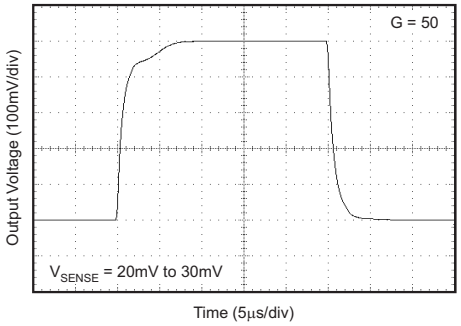


図 15. Step Response

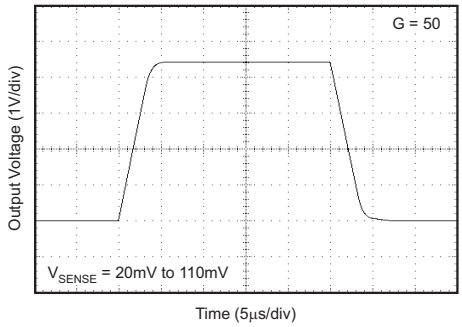


図 16. Step Response

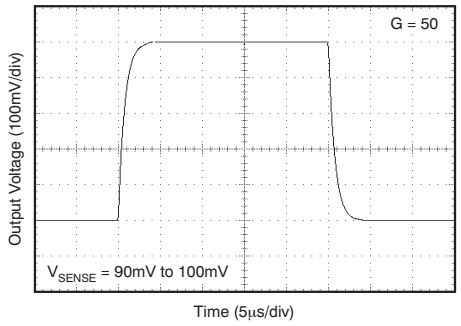


図 17. Step Response

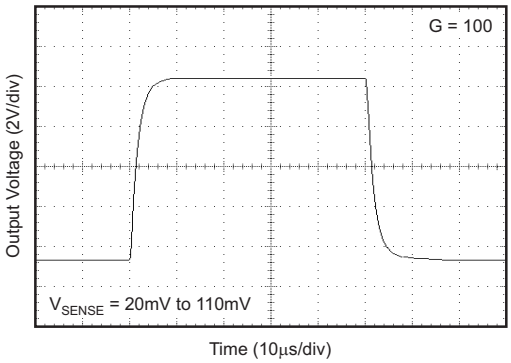


図 18. Step Response

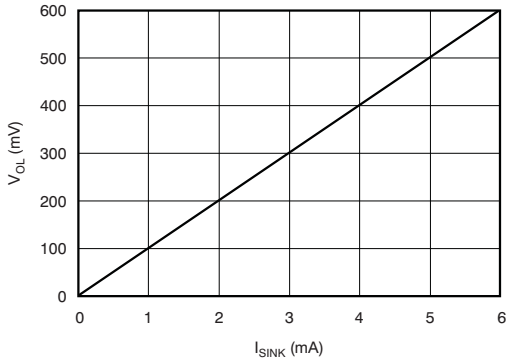


図 19. Comparator V_{OL} vs I_{SINK}

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 12 V, V_{IN+} = 12 V, and V_{SENSE} = 100 mV, (unless otherwise noted)

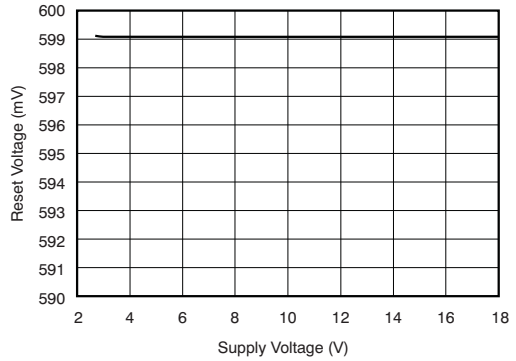


図 20. Comparator Trip Point vs Supply Voltage

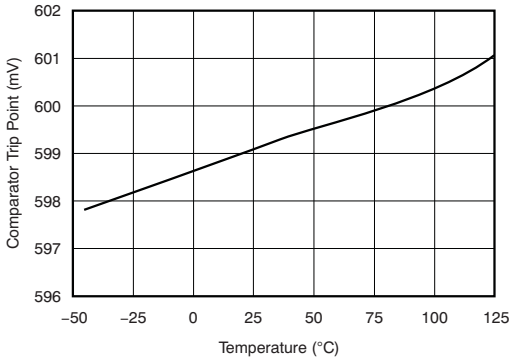


図 21. Comparator Trip Point vs Temperature

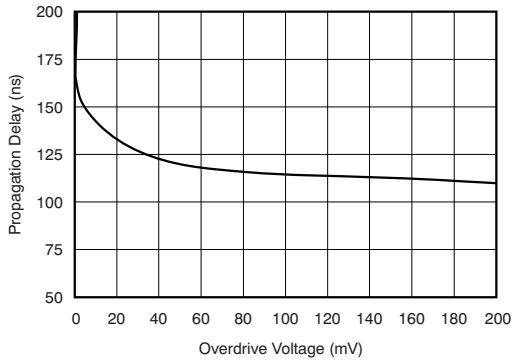


図 22. Comparator Propagation Delay vs Overdrive Voltage

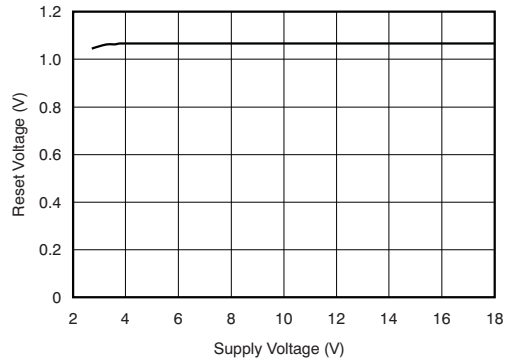


図 23. Comparator Reset Voltage vs Supply Voltage

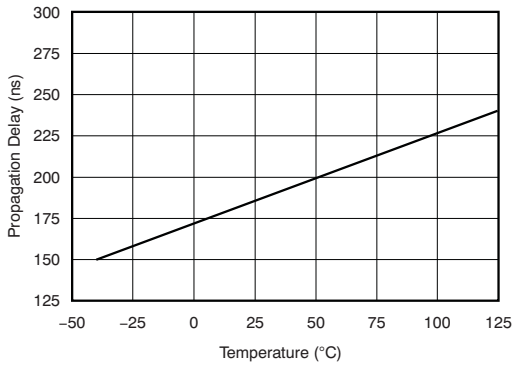


図 24. Comparator Propagation Delay vs Temperature

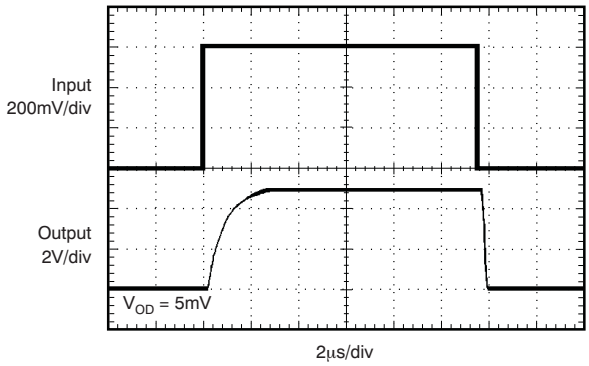


図 25. Comparator Propagation Delay

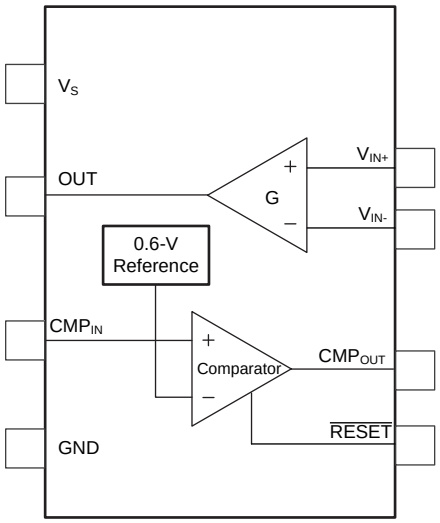
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7 Detailed Description

7.1 Overview

The INA200, INA201, and INA202 devices are high-side current-shunt monitors with voltage output. The INA20x devices can sense drops across shunts at common-mode voltages from –16 V to 80 V. The INA200–INA202 devices are available with three output voltage scales: 20 V/V, 50 V/V, and 100 V/V, with up to 500-kHz bandwidth. The INA200, INA201, and INA202 devices incorporate an open-drain comparator and internal reference providing a 0.6-V threshold. External dividers set the current trip point. The comparator includes a latching capability, that can be made transparent by grounding (or leaving open) the $\overline{\text{RESET}}$ pin. The INA200, INA201, and INA202 devices operate from a single 2.7 to 18-V supply, drawing a maximum of 1800 μA of supply current. Package options include the very small MSOP-8 and the SO-8. All versions are specified over the extended operating temperature range of –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Basic Connections

図 26 shows the basic connections of the INA20x devices. The input pins (V_{IN+} and $V_{IN–}$) must be connected as closely as possible with Kelvin connections to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

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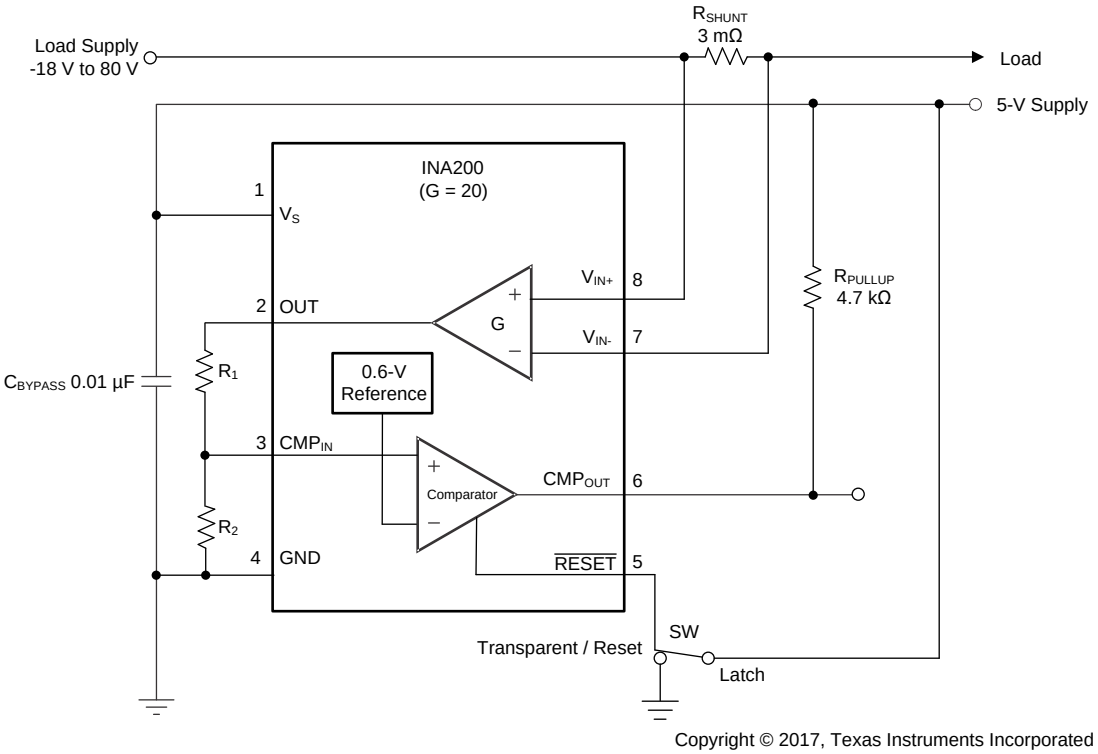


図 26. INA200 Basic Connections

7.3.2 Selecting R_S

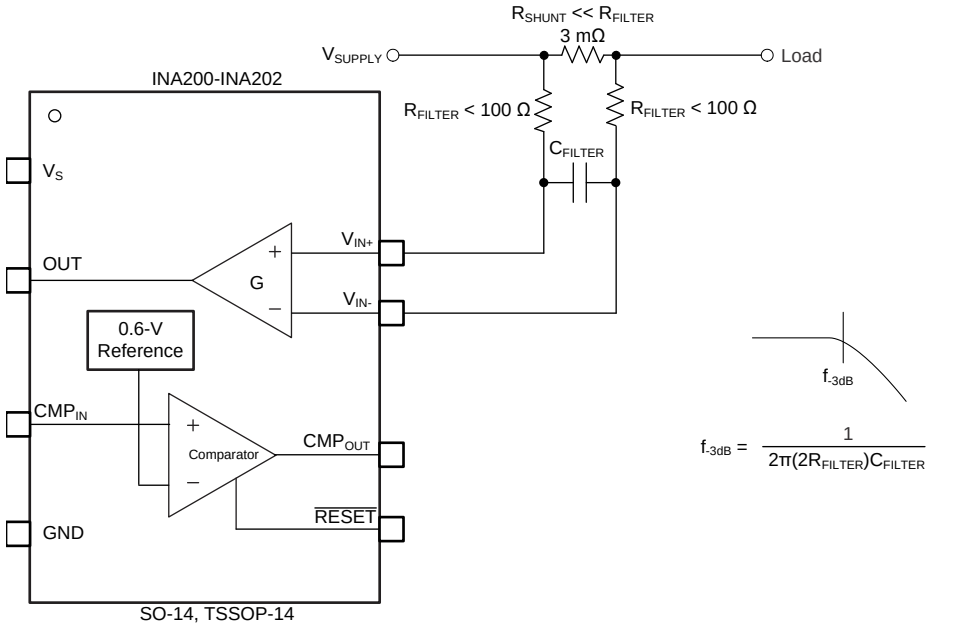
The selected value for the shunt resistor, R_S, depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_S provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_S minimize voltage loss in the supply line. For most applications, using an R_S value that provides a full-scale shunt voltage range of 50 mV to 100 mV results in the best performance. Maximum input voltage for accurate measurements is 500 mV, but output voltage is limited by supply.

7.3.3 Comparator

The INA200, INA201, and INA202 devices incorporate an open-drain comparator. This comparator typically has 2 mV of offset and a 1.3-µs (typical) response time. The output of the comparator latches and is reset through the $\overline{\text{RESET}}$ pin; see 図 28.

When V_s and $\overline{\text{RESET}}$ are different, TI recommends adding a low-pass filter (LPF) on the $\overline{\text{RESET}}$ pin to avoid comparator behavior inconsistent with the data sheet. For instance, with a 12-V supply and a 3.3-V RESET, a rise time of 400 ns is appropriate. Similarly, with an 18-V supply and a 2.7-V RESET, a 1-µs rise time is appropriate; see 図 31.

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図 27. Input Filter (Gain Error: 1.5% to 2.8%)

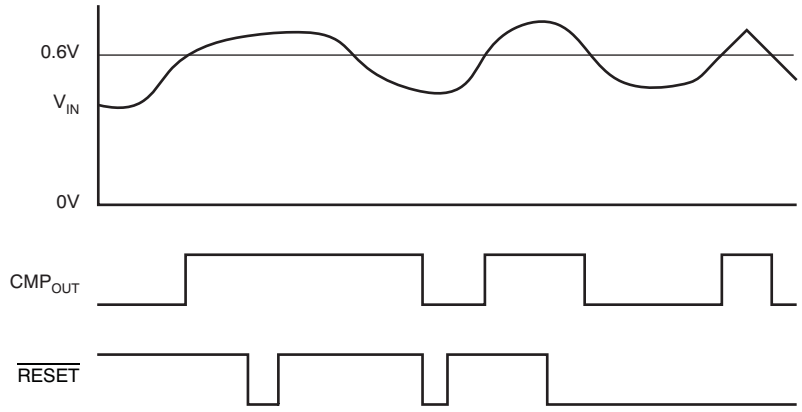
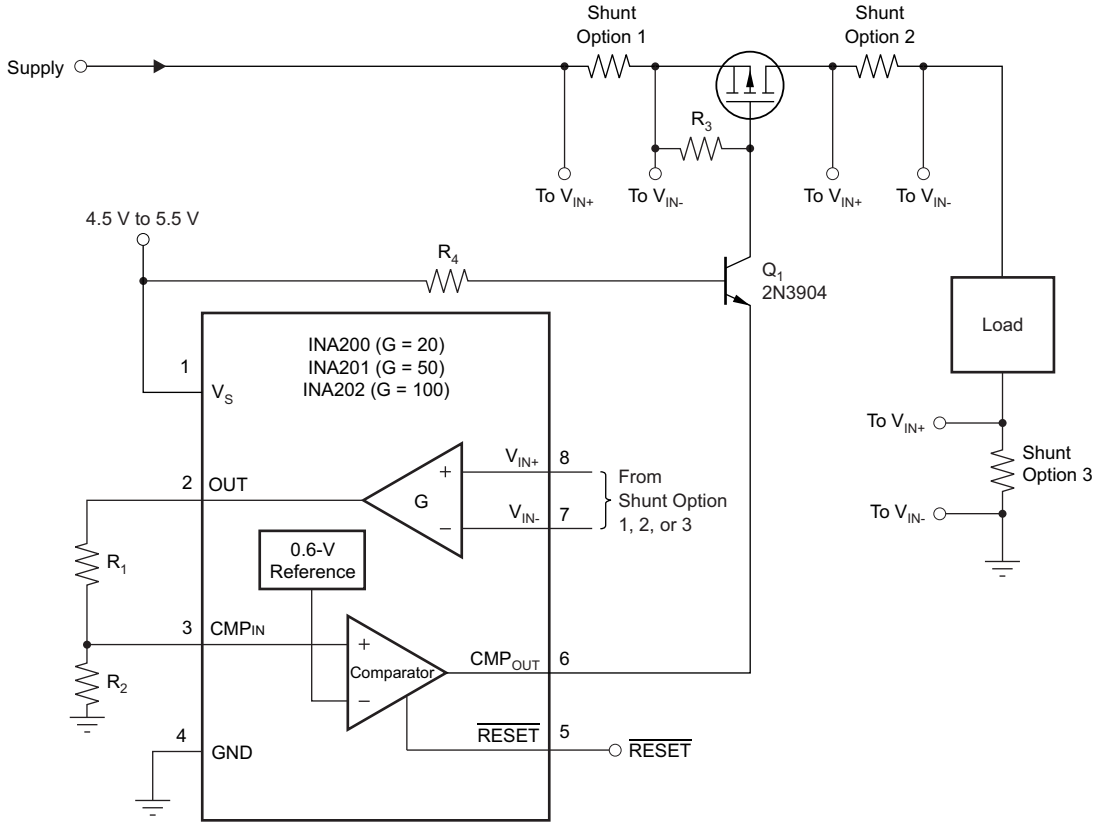


図 28. Comparator Latching Capability

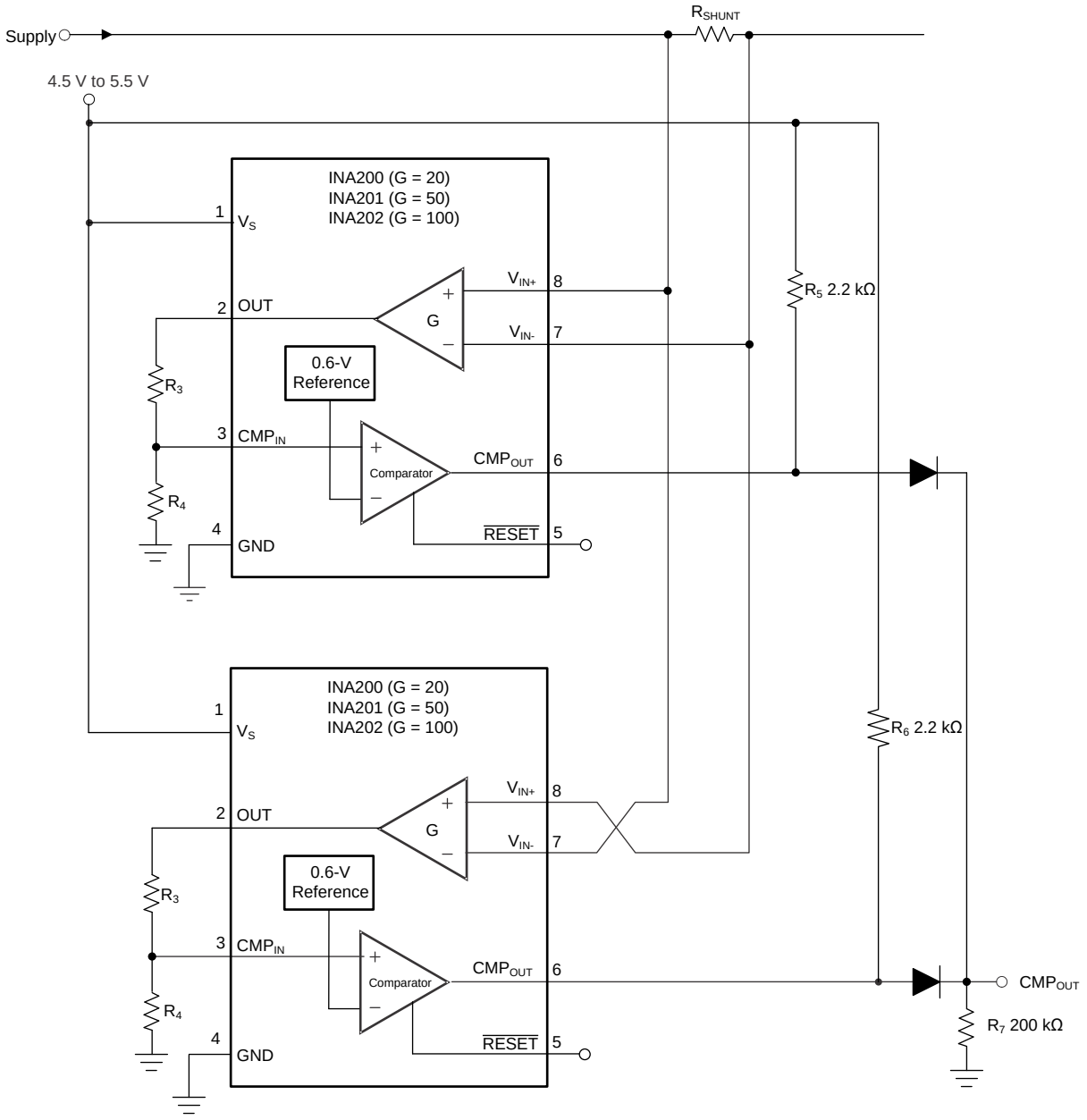


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(1) Q1 cascodes the comparator output to drive a high-side FET (the 2N3904) shown is good up to 60 V. The shunt can be located in any one of the three locations shown. The latching capability must be used in shutdown applications to prevent oscillation at the trip point.

図 29. High-Side Switch Overcurrent Shutdown

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(1) It is possible to set different limits for each direction.

図 30. Bidirectional Overcurrent Comparator

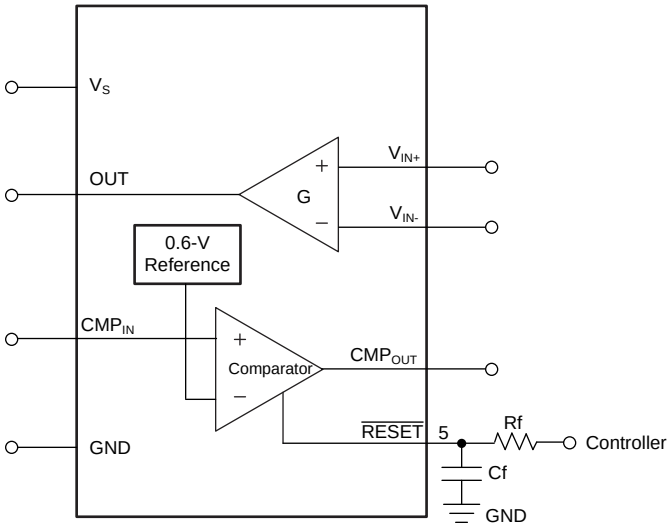


図 31. Filter on $\overline{RESET}$ Pin

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7.4 Device Functional Modes

7.4.1 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA20x series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA20x devices, which is complicated by the internal 5 kΩ + 30% input impedance. This is shown in 図 27. Using the lowest possible resistor values minimizes the initial shift in gain and effects of tolerance. The effect on initial gain is shown in 式 1:

$$\text{Gain Error \%} = 100 - \left(100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{FILT}}\right) \quad (1)$$

Total effect on gain error can be calculated by replacing the 5-kΩ term with 5 kΩ – 30%, (or 3.5 kΩ) or 5 kΩ + 30% (or 6.5 kΩ). The tolerance extremes of R_{FILT} can be inserted into the equation. If a pair of 100-Ω 1% resistors are used on the inputs, the initial gain error equals 1.96%. Worst-case tolerance conditions always occur at the lower excursion of the internal 5-kΩ resistor (3.5 kΩ), and the higher excursion of R_{FILT} – 3% in this case.

The specified accuracy of the INA20x devices must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

7.4.2 Accuracy Variations as a Result of V_{SENSE} and Common-Mode Voltage

The accuracy of the INA200, INA201, and INA202 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} – V_{IN–}$), common-mode voltage, (V_{CM}), relative to the supply voltage (V_S). V_{CM} is expressed as ($V_{IN+} + V_{IN–}$) / 2; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is typically small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20$ mV, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20$ mV, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $–16\text{ V} \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\text{ V} \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

7.4.2.1 Normal Case 1: $V_{SENSE} \geq 20$ mv, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by 式 2.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}}$$

where

- V_{OUT1} = output voltage with V_{SENSE} = 100 mV
- V_{OUT2} = output voltage with V_{SENSE} = 20 mV (2)

Then the offset voltage is measured at V_{SENSE} = 100 mV, and referred to the input (RTI) of the current shunt monitor, as shown in *Electrical Characteristics: Current-Shunt Monitor*.

$$V_{OS}\text{RTI (Referred-To-Input)} = \left(\frac{V_{OUT1}}{G}\right) - 100\text{mV} \quad (3)$$

In the *Typical Characteristics*, *図 7* shows the highest accuracy for the this region of operation. In this plot, V_S = 12 V. For $V_{CM} \geq 12$ V, the output error is at the minimum value. This case creates the $V_{SENSE} \geq 20$-mV output specifications in *Electrical Characteristics: Current-Shunt Monitor* .

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Device Functional Modes (continued)

7.4.2.2 Normal Case 2: $V_{SENSE} \geq 20$ mv, $V_{CM} < V_S$

This region of operation is less accurate than normal case 1 as a result of the common-mode operating area in which the part functions, as shown in the 図 7 curve (図 7). As noted, for this graph V_S = 12 V; for V_{CM} < 12 V, the output error increases as V_{CM} decreases to less than 12 V, with a typical maximum error of 0.005% at the most negative V_{CM} = –16 V.

7.4.2.3 Low V_{SENSE} Case 1: $V_{SENSE} < 20$ mV, $-16\ V \leq V_{CM} < 0$ and Low V_{SENSE} Case 3: $V_{SENSE} < 20$ mV, $V_S < V_{CM} \leq 80$ V

Although the INA200 family of devices are not designed for accurate operation in these regions, some applications are exposed to these conditions. For example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA20x devices, it is important to know what the behavior of the devices is in these regions.

As V_{SENSE} approaches 0 mV, in these V_{CM} regions, the accuracy of the device output degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of V_{OUT} = 300 mV for V_{SENSE} = 0 mV. As V_{SENSE} approaches 20 mV, V_{OUT} returns to the expected output value with accuracy as shown in *Electrical Characteristics: Current-Shunt Monitor*. 図 32 shows this effect using the INA202 (gain = 100).

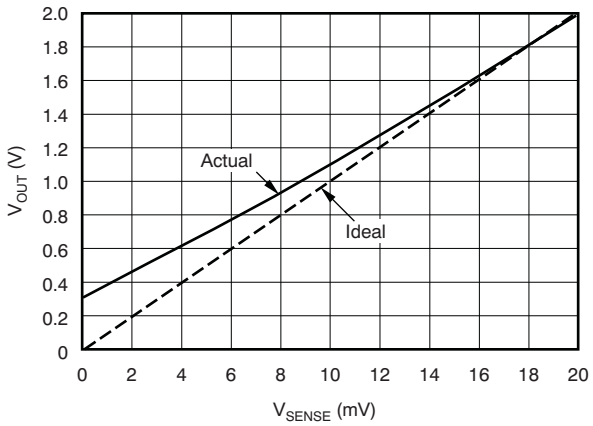


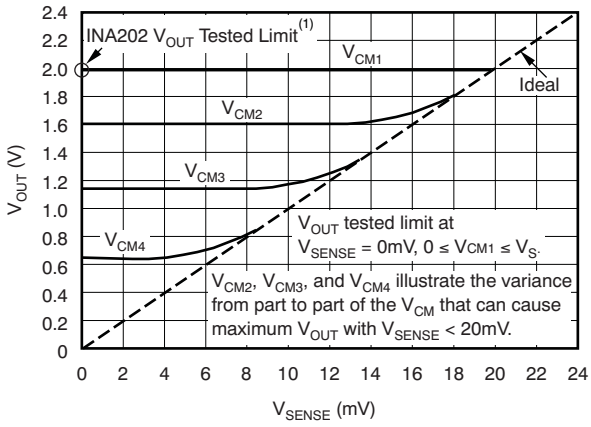
図 32. Example For Low V_{SENSE} Cases 1 and 3 (INA202, Gain = 100)

7.4.2.4 Low V_{SENSE} Case 2: $V_{SENSE} < 20$ mV, $0\ V \leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA20x family. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is low. Within this region, V_{OUT} approaches voltages close to linear operation levels for normal case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0 V. Within this region, as V_{SENSE} approaches 20 mV, device operation is closer to that is described in normal case 2. 図 33 shows this behavior for the INA202. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S, setting V_{SENSE} equal to 0 mV and sweeping V_{CM} from 0 V to V_S. The exact V_{CM} at which V_{OUT} peaks during this test varies from device to device, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} tested limit.

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Device Functional Modes (continued)



NOTE: (1) INA200 V_{OUT} Tested Limit = 0.4V. INA201 V_{OUT} Tested Limit = 1V.

図 33. Example For Low V_{SENSE} Case 2 (INA202, Gain = 100)

7.4.3 Transient Protection

The –16 to 80 V common-mode range of the INA20x devices is ideal for withstanding automotive fault conditions ranging from 12-V battery reversal up to 80-V transients, since no additional protective components are required up to those levels. In the event that the INA20x devices are exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (such as Zeners) are required. TI does not recommend using MOVs or VDRs, except when they are used in addition to a semiconductor transient absorber. Select the transient absorber so the absorber does not allow the INA20x devices to be exposed to transients greater than 80 V (that is, allow for transient absorber tolerance and additional voltage due to transient absorber dynamic impedance). Despite the use of internal Zener-type ESD protection, the INA20x devices do not lend themselves to using external resistors in series with the inputs since the internal gain resistors can vary up to ±30%. (If gain accuracy is not important, then resistors can be added in series with the INA200, INA201, and INA202 inputs with two equal resistors on each input.)

7.4.4 Output Voltage Range

The output of the INA20x devices is accurate within the output voltage swing range set by the power supply pin (V_S.) This performance is best illustrated when using the INA202 (a gain of 100 version), where a 100-mV full-scale input from the shunt resistor requires an output voltage swing of 10 V, and a power-supply voltage sufficient to achieve 10 V on the output.

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8 Application and Implementation

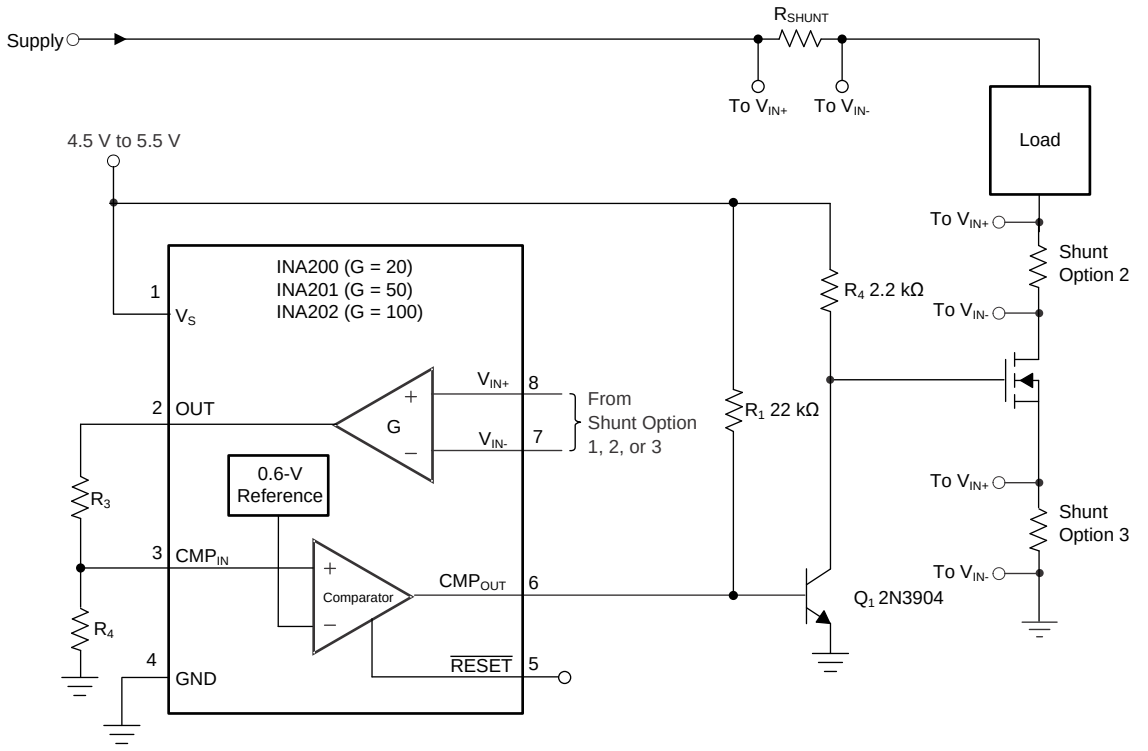
注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The INA20x series is designed to enable simple configuration for detecting overcurrent conditions and current monitoring in an application. This device is individually targeted towards overcurrent detection of a single threshold. However, this device can pair with additional devices and circuitry to create more complex monitoring functional blocks.

8.2 Typical Application



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(1) In this case, Q inverts the comparator output.

図 34. Low-Side Switch Overcurrent Shutdown

8.2.1 Design Requirements

The device measures current through a resistive shunt with current flowing in one direction that enables detection of an overcurrent event only when the differential input voltage exceeds the threshold limit. When the current reaches the set limit of the divider R_1 / R_2, the output of CMP_{OUT} transitions high, which turns Q1 on, pulls the gate of the pass-FET low, and turns off the flow off current.

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Typical Application (continued)

8.2.2 Detailed Design Procedure

図 34 shows the basic connections of the device. The input terminals (IN+ and IN –) must be connected as closely as possible to the current-sensing resistor to minimize any resistance in series with the shunt resistance. Additional resistance between the current-sensing resistor and input terminals results in errors in the measurement. When input current flows through this external input resistance, the voltage developed across the shunt resistor differs from the voltage reaching the input terminals.

Use the gain of the INA20x and shunt value to calculate the OUT voltage for the desired trip current. Configure R1 and R2 so that the current trip point is equal to the 0.6-V reference voltage.

8.2.3 Application Curve

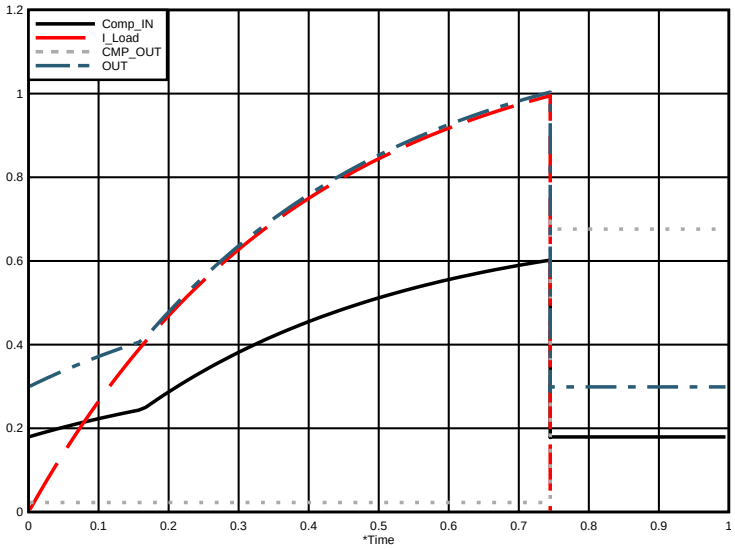


図 35. Low-Side Switch Overcurrent Shutdown Response

9 Power Supply Recommendations

The input circuitry of the INA20x devices can accurately measure beyond the power-supply voltage, V_S. For example, the V_S power supply is 5 V, whereas the load power-supply voltage is up to 80 V. However, the output voltage range of the OUT pin is limited by the voltages on the power supply pin.

9.1 Output vs Supply Ramp Considerations

図 36, 図 37, and 図 38 show the typical output voltages for high and low-side configurations with the given ramp supply voltage. These fluctuations on the output during power-up may require a controller to incorporate a blanking time to disregard the artifacts.

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Output vs Supply Ramp Considerations (continued)

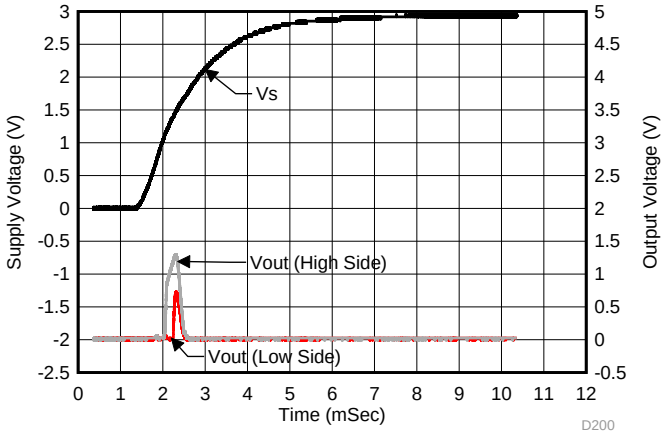


図 36. Analog Output vs Supply Ramp (INA200)

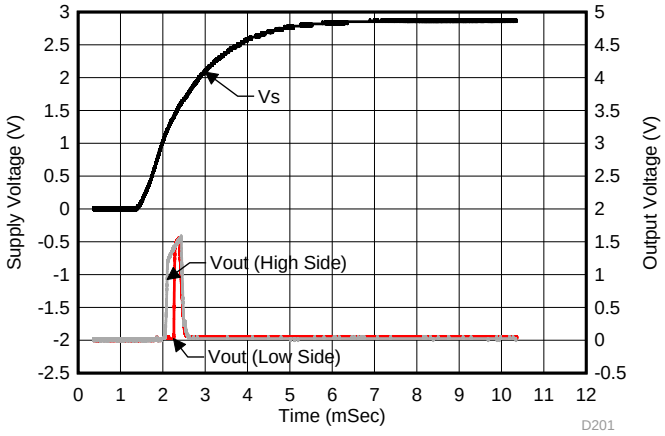


図 37. Analog Output vs Supply Ramp (INA201)

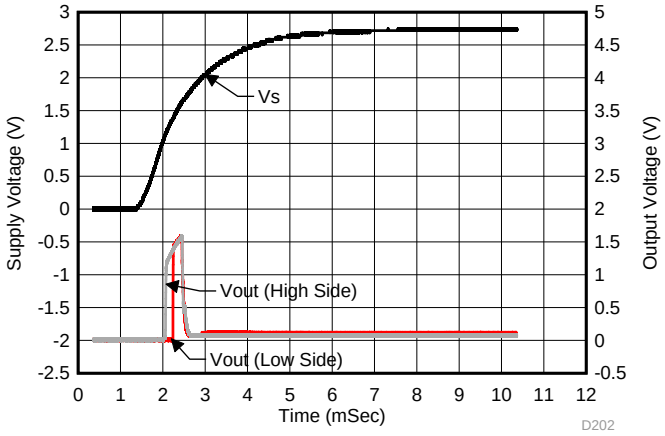


図 38. Analog Output vs Supply Ramp (INA202)

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10 Layout

10.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very-low-ohmic value of the current resistor, any additional high-current carrying impedance causes significant measurement errors.
- The power-supply bypass capacitor must be placed as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

10.2 Layout Example

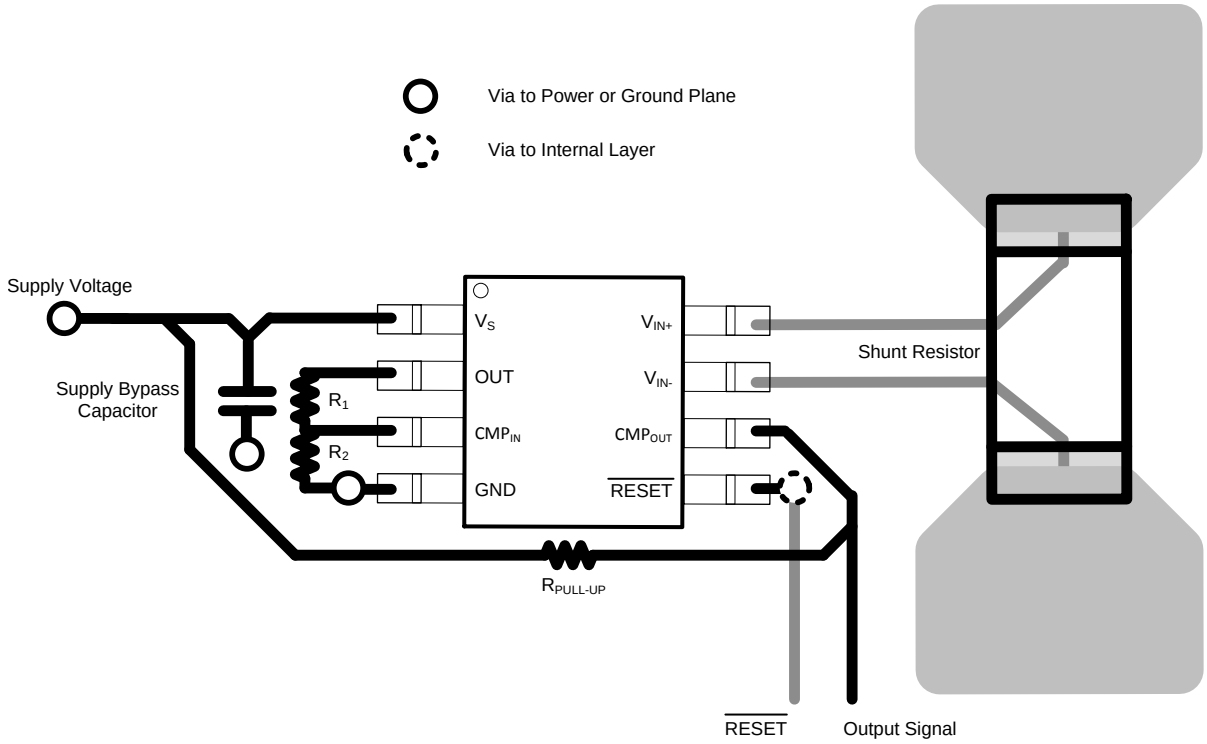


図 39. INA20x Layout Example

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11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 1. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
INA200	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
INA201	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
INA202	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

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11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA200AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	INA 200A
INA200AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQH
INA200AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQH
INA200AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A
INA200AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A
INA200AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A
INA200AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 200A
INA201AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	INA 201A
INA201AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI | Nipdauag	Level-2-260C-1 YEAR	-40 to 125	BQJ
INA201AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 125	BQJ
INA201AIDGKRG4	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	BQJ
INA201AIDGKT	Obsolete	Production	VSSOP (DGK) | 8	-	-	Call TI	Call TI	-40 to 125	BQJ
INA201AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A
INA201AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A
INA201AIDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A
INA201AIDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 201A
INA202AID	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	INA 202A
INA202AIDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BQL
INA202AIDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQL
INA202AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 202A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA202AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	INA 202A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF INA200, INA201, INA202 :

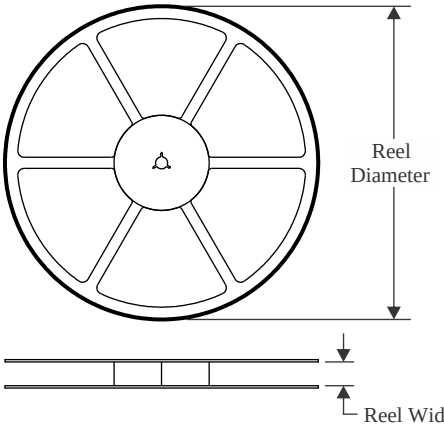
- Automotive : INA200-Q1, INA201-Q1, INA202-Q1

NOTE: Qualified Version Definitions:

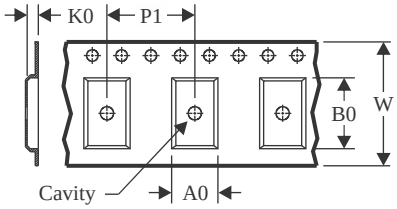
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

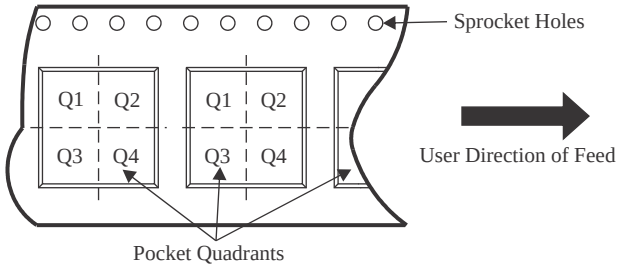


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

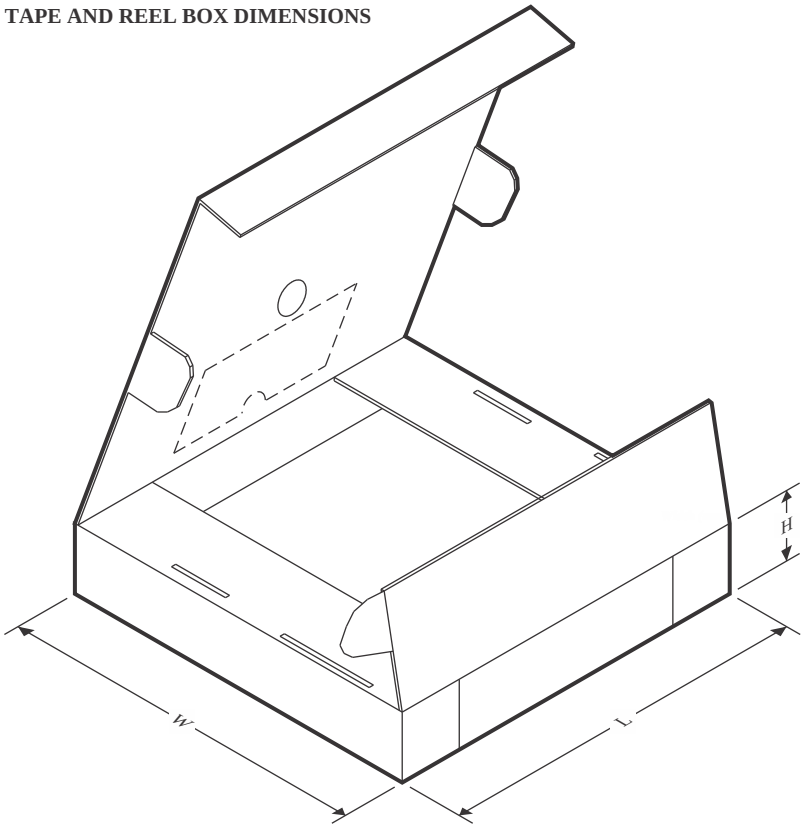
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

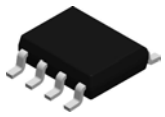
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA200AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA200AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA200AIDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA201AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA202AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA200AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA200AIDR	SOIC	D	8	2500	353.0	353.0	32.0
INA200AIDRG4	SOIC	D	8	2500	353.0	353.0	32.0
INA201AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA202AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA202AIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA202AIDR	SOIC	D	8	2500	353.0	353.0	32.0

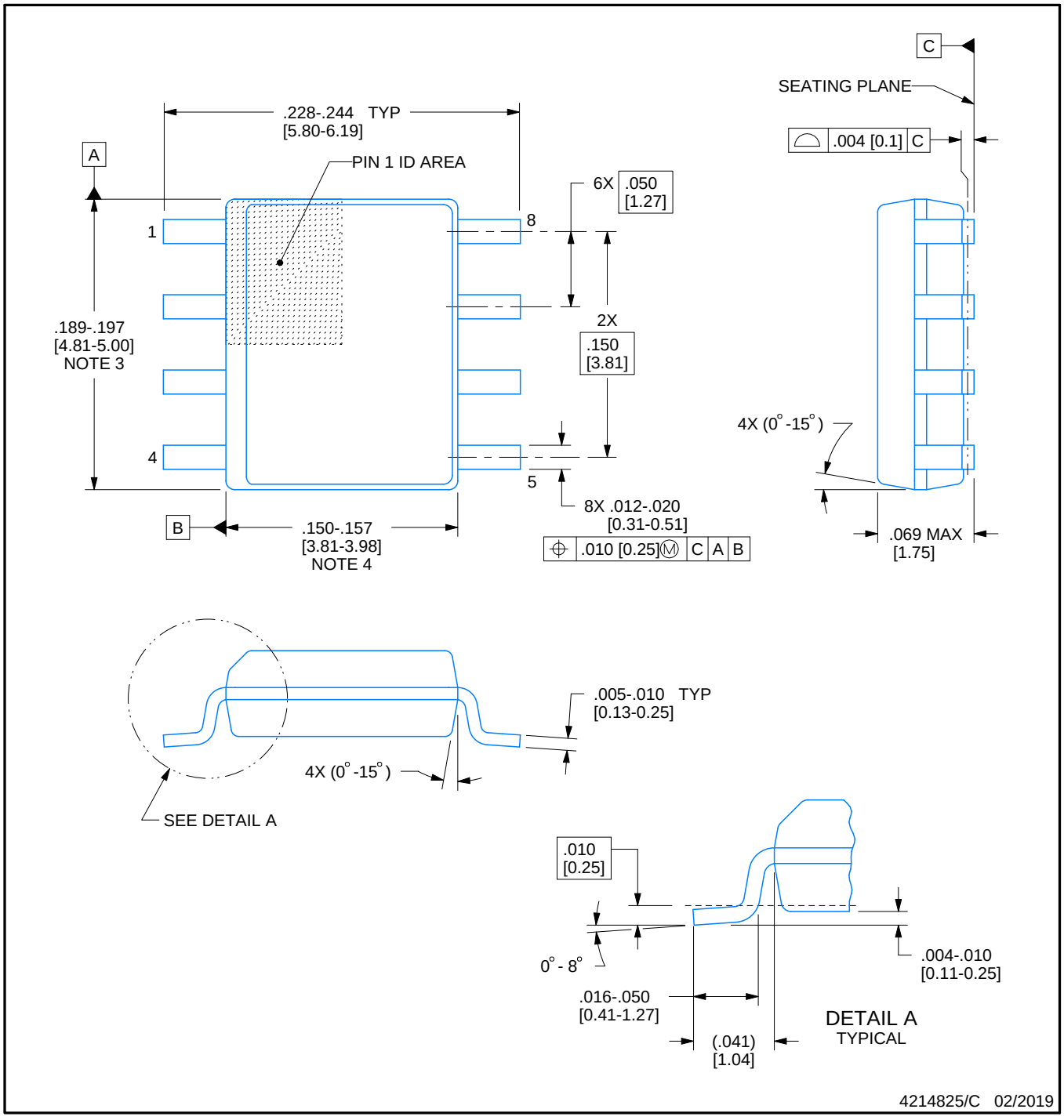


PACKAGE OUTLINE

D0008A

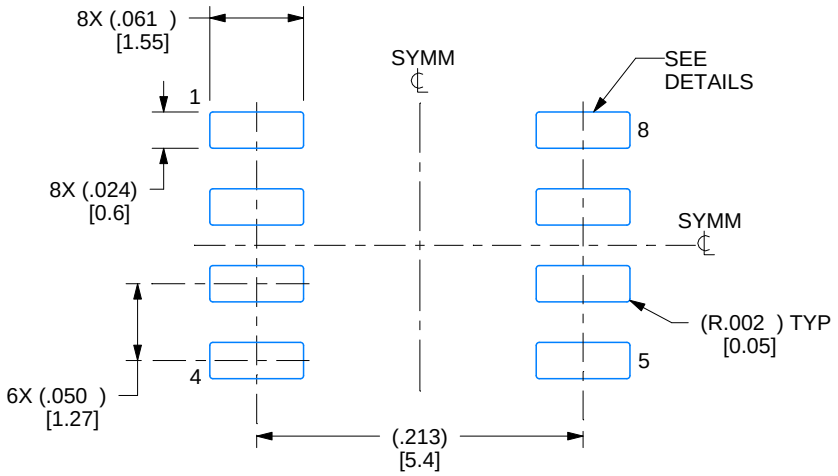
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

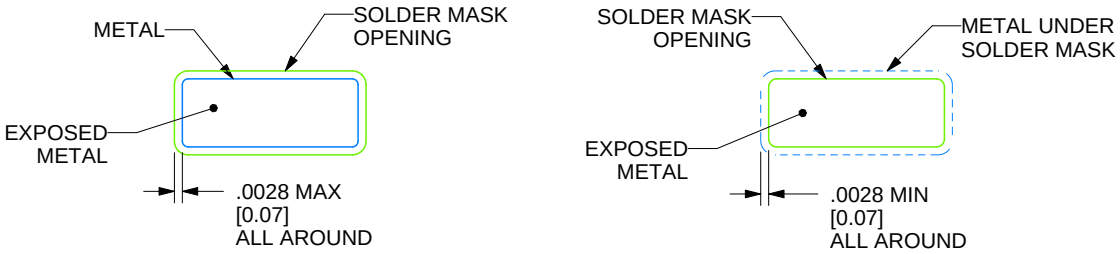


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

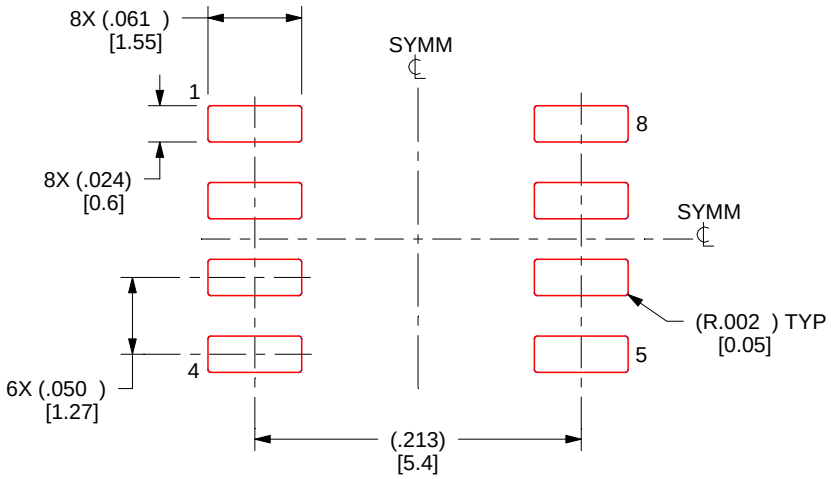
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

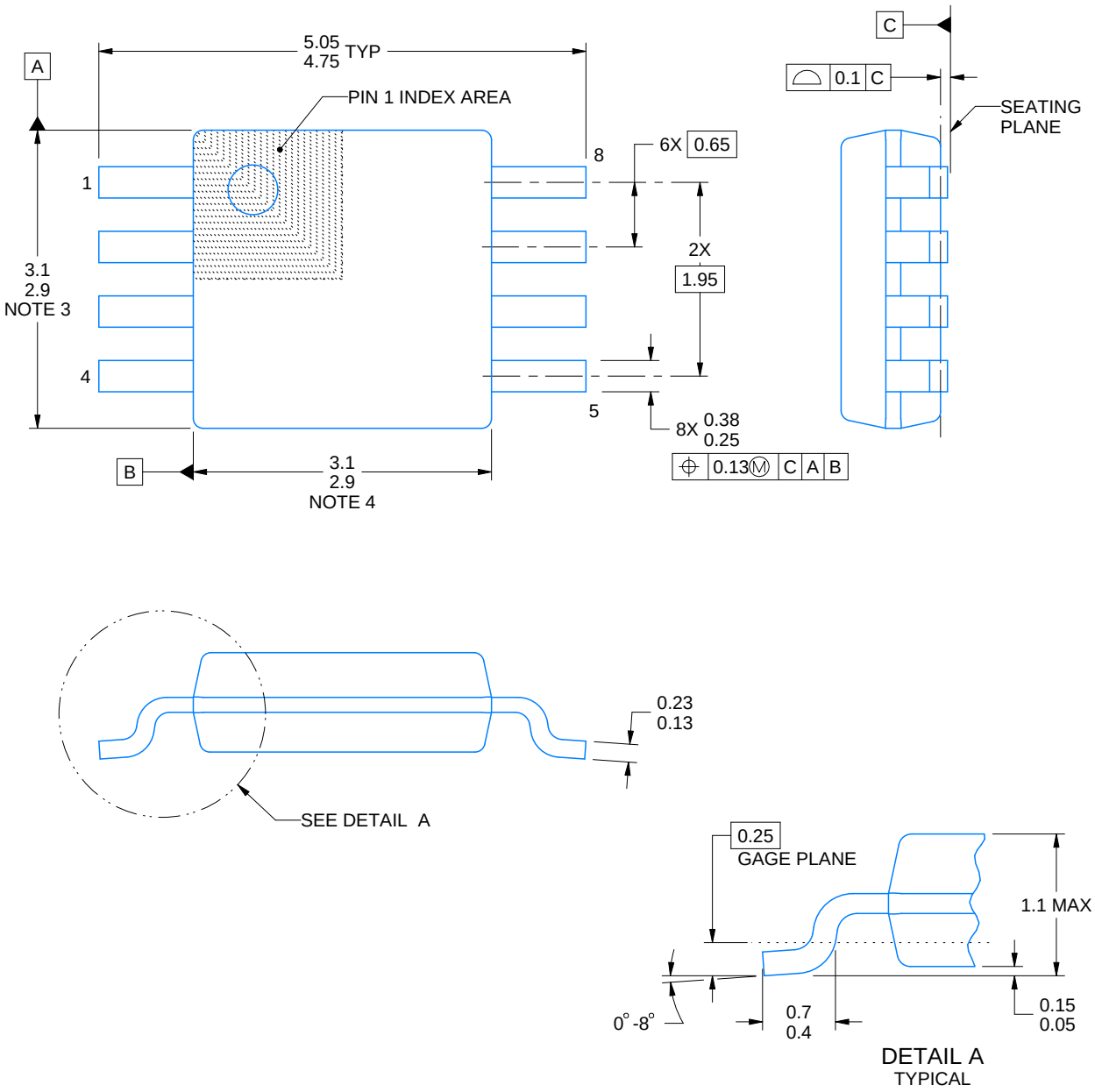
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

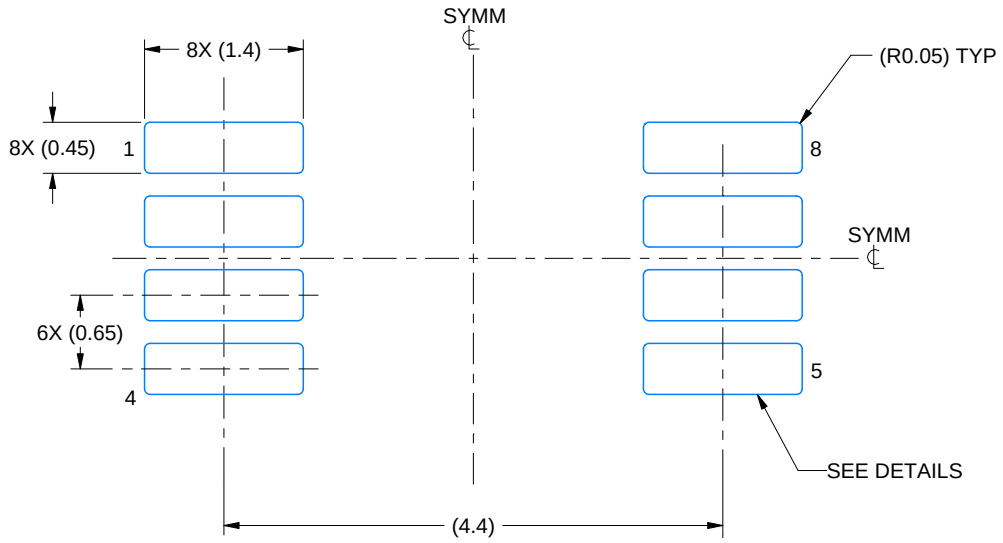
SMALL OUTLINE PACKAGE



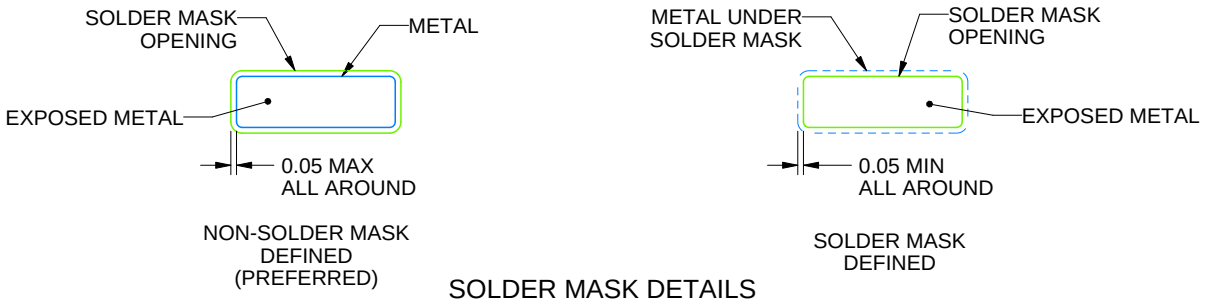
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

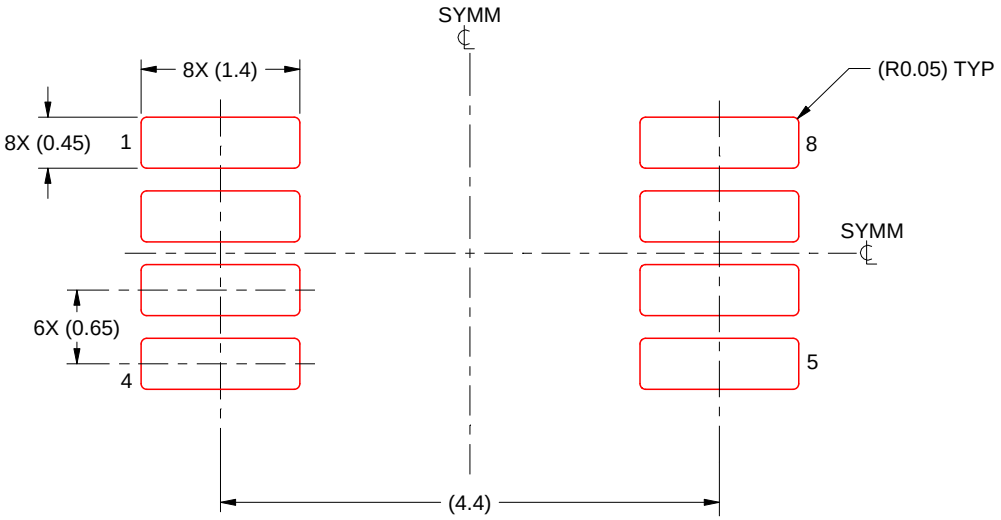


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月