INA180-Q1, INA2180-Q1, INA4180-Q1
JAJSFB6D – APRIL 2018 – REVISED JULY 2022

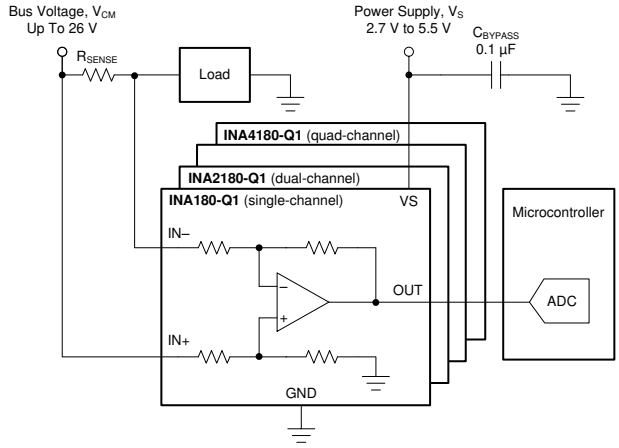
INAx180-Q1 車載用、ローサイドおよびハイサイド電圧出力、電流センス・アンプ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1：–40℃ ≤ T_A ≤ +125℃
  - HBM ESD 分類レベル 2
  - CDM ESD 分類レベル C6
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 同相範囲 (V_{CM})：–0.2V～+26V
- 広い帯域幅：350kHz/V (A1 デバイス)
- オフセット電圧：
  - V_{CM} = 0V で ±150µV 以下
  - V_{CM} = 12 V で ±500µV 以下
- 出力スルーレート：2V/µs
- 精度：
  - ゲイン誤差 1% (最大値)
  - オフセット・ドリフト 1µV/℃ (最大値)
- ゲイン・オプション：
  - 20V/V (A1 デバイス)
  - 50V/V (A2 デバイス)
  - 100V/V (A3 デバイス)
  - 200V/V (A4 デバイス)
- 静止電流：最大 260µA（INA180-Q1）

2 アプリケーション

- モータ制御
- バッテリ監視
- パワー・マネージメント
- 照明制御
- 過電流検出



代表的なアプリケーション回路

3 概要

INA180-Q1、INA2180-Q1、INA4180-Q1 (INAx180-Q1) 電流センス・アンプは、コスト最適化アプリケーション用に設計されています。これらのデバイスは、電流センス・アンプ (電流シャント・モニタとも呼ばれます) のファミリに属し、電源電圧にかかわらず、－0.2V～＋ 26V の同相電圧において、電流センス抵抗の両端の電圧降下を検出できます。INAx180-Q1 は、整合抵抗ゲイン回路を、4 つの固定ゲイン・デバイス・オプション(20V/V、50V/V、100V/V、または 200V/V) に統合しています。この整合ゲイン抵抗回路により、ゲイン誤差が最小限に抑えられ、温度ドリフトが低減されます。

これらのデバイスはすべて、単一の 2.7V～5.5V 電源で動作します。シングル・チャネルの INA180-Q1 は最大消費電流が 260µA で、デュアル・チャネルの INA2180-Q1 は 500µA、クワッド・チャネルは 900µA です。

INA180-Q1 は 5 ピンの SOT-23 パッケージで供給され、2 つの異なるピン構成を選択できます。INA2180-Q1 は 8 ピンの VSSOP パッケージで供給されます。INA4180-Q1 は 14 ピンの TSSOP パッケージで供給されます。すべてのデバイス・オプションは、拡張動作温度範囲の -40℃～+125℃ で動作が規定されています。

パッケージ情報(1)

部品番号	パッケージ	本体サイズ (公称)
INA180-Q1	SOT-23 (5)	2.90mm × 1.60mm
INA2180-Q1	VSSOP (8)	3.00mm × 3.00mm
INA4180-Q1	TSSOP (14)	5.00mm × 4.40mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (April 2020) to Revision D (July 2022) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section ... 25
- Changed pin 3 in 図 9-9 from: IN+2 to: IN+1 ... 27

Changes from Revision B (March 2019) to Revision C (April 2020) — **Page**

- 機能安全対応の情報を追加 ... 1

Changes from Revision A (July 2018) to Revision B (March 2019) — **Page**

- INA180-Q1 デバイスを製品プレビューから量産データ (アクティブ) に変更 ... 1
- Added new paragraph regarding phase reversal to end of *Input Differential Overload* section ... 18

Changes from Revision * (April 2018) to Revision A (July 2018) — **Page**

- INA4180-Q1 デバイスをプレビューから量産データ (アクティブ) に変更 ... 1

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5 Device Comparison

表 5-1. Device Comparison

PRODUCT	NUMBER OF CHANNELS	GAIN (V/V)
INA180A1-Q1 (1)	1	20
INA180A2-Q1 (1)	1	50
INA180A3-Q1 (1)	1	100
INA180A4-Q1 (1)	1	200
INA180B1-Q1 (1)	1	20
INA180B2-Q1 (1)	1	50
INA180B3-Q1 (1)	1	100
INA180B4-Q1 (1)	1	200
INA2180A1-Q1	2	20
INA2180A2-Q1	2	50
INA2180A3-Q1	2	100
INA2180A4-Q1	2	200
INA4180A1-Q1	4	20
INA4180A2-Q1	4	50
INA4180A3-Q1	4	100
INA4180A4-Q1	4	200

(1) INA180A devices use pinout A. INA180B devices use pinout B. See the *Pin Configuration and Functions* section for more information.

6 Pin Configuration and Functions

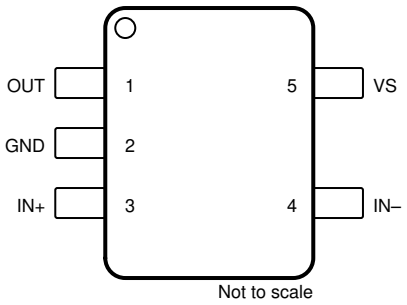

図 6-1. INA180-Q1: DBV Package 5-Pin SOT-23 (Pinout A) Top View

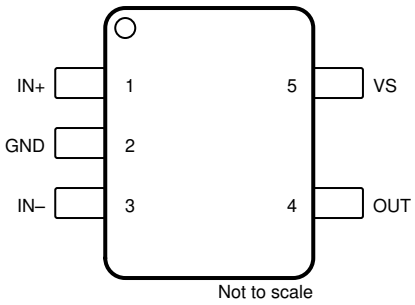

図 6-2. INA180-Q1: DBV Package 5-Pin SOT-23 (Pinout B) Top View

表 6-1. Pin Functions: INA180-Q1 (Single Channel)

PIN			TYPE	DESCRIPTION
NAME	SOT-23 Pinout A	SOT-23 Pinout B		
GND	2	2	Analog	Ground
IN–	4	3	Analog input	Current-sense amplifier negative input. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
IN+	3	1	Analog input	Current-sense amplifier positive input. For high-side applications, connect to bus-voltage side of sense resistor. For low-side applications, connect to load side of sense resistor.
OUT	1	4	Analog output	Output voltage
VS	5	5	Analog	Power supply, 2.7 V to 5.5 V

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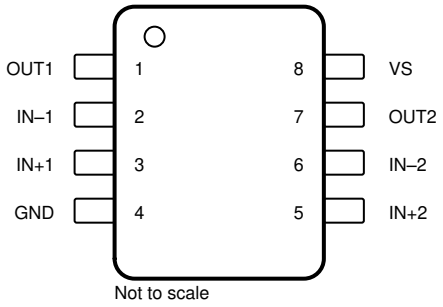

図 6-3. INA2180-Q1: DGK Package 8-Pin VSSOP Top View

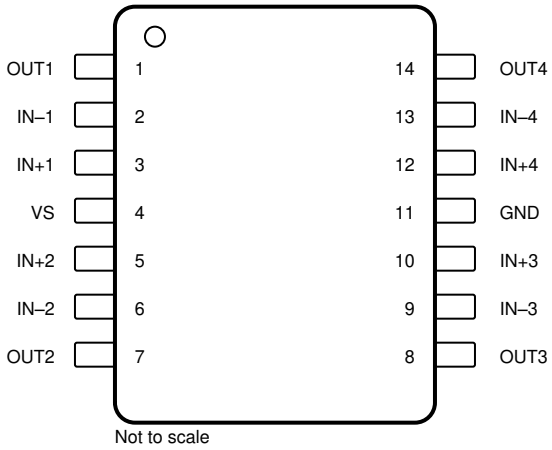

図 6-4. INA4180-Q1: PW Package 14-Pin TSSOP Top View

表 6-2. Pin Functions: INA2180-Q1 (Dual Channel) and INA4180-Q1 (Quad Channel)

PIN			TYPE	DESCRIPTION
NAME	INA2180-Q1	INA4180-Q1		
GND	4	11	Analog	Ground
IN–1	2	2	Analog input	Current-sense amplifier negative input for channel 1. For high-side applications, connect to load side of channel-1 sense resistor. For low-side applications, connect to ground side of channel-1 sense resistor.
IN+1	3	3	Analog input	Current-sense amplifier positive input for channel 1. For high-side applications, connect to bus-voltage side of channel-1 sense resistor. For low-side applications, connect to load side of channel-1 sense resistor.
IN–2	6	6	Analog input	Current-sense amplifier negative input for channel 2. For high-side applications, connect to load side of channel-2 sense resistor. For low-side applications, connect to ground side of channel-2 sense resistor.
IN+2	5	5	Analog input	Current-sense amplifier positive input for channel 2. For high-side applications, connect to bus-voltage side of channel-2 sense resistor. For low-side applications, connect to load side of channel-2 sense resistor.
IN–3	—	9	Analog input	Current-sense amplifier negative input for channel 3. For high-side applications, connect to load side of channel-3 sense resistor. For low-side applications, connect to ground side of channel-3 sense resistor.
IN+3	—	10	Analog input	Current-sense amplifier positive input for channel 3. For high-side applications, connect to bus-voltage side of channel-3 sense resistor. For low-side applications, connect to load side of channel-3 sense resistor.
IN–4	—	13	Analog input	Current-sense amplifier negative input for channel 4. For high-side applications, connect to load side of channel-4 sense resistor. For low-side applications, connect to ground side of channel-4 sense resistor.
IN+4	—	12	Analog input	Current-sense amplifier positive input for channel 4. For high-side applications, connect to bus-voltage side of channel-4 sense resistor. For low-side applications, connect to load side of channel-4 sense resistor.
OUT1	1	1	Analog output	Channel 1 output voltage
OUT2	7	7	Analog output	Channel 2 output voltage
OUT3	—	8	Analog output	Channel 3 output voltage
OUT4	—	14	Analog output	Channel 4 output voltage
VS	8	4	Analog	Power supply, 2.7 V to 5.5 V

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			6	V
Analog inputs, IN+, IN–(2) (4)	Differential (V_{IN+}) – ($V_{IN–}$)	–28	28	V
	Common-mode(3)	GND – 0.3	28	
Output voltage		GND – 0.3	V_S + 0.3	V
Maximum output current, I_{OUT}			8	mA
Operating free-air temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.
(4) Sustained operation between 26 V and 28 V for more than a few minutes may cause permanent damage to the device.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage (IN+ and IN–)	–0.2	12	26	V
V_S	Operating supply voltage	2.7	5	5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		INA180-Q1 DBV (SOT-23) 6 PINS	INA2180-Q1 DGK (VSSOP) 8 PINS	INA4180-Q1 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.1	177.9	115.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.8	65.6	44.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.1	99.3	59.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.4	10.5	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	97.9	58.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.5 Thermal Information

THERMAL METRIC (1)		INA180-Q1		INA2180-Q1	INA4180-Q1	UNIT
		DBV (SOT-23)	DCK (SC70)	DGS (VSSOP)	PW (TSSOP)	
		6 PINS	6 PINS	10 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.1	TBD	177.9	115.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.8	TBD	65.6	44.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.1	TBD	99.3	59.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.4	TBD	10.5	4.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.7	TBD	97.9	58.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	N/A	N/A	°C/W

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7.6 Electrical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{SENSE} = V_{IN+} – $V_{IN–}$ (unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
CMRR	Common-mode rejection ratio, RTI(1)	V_{IN+} = 0 V to 26 V, V_{SENSE} = 10 mV, T_A = –40°C to +125°C		84	100		dB
V_{OS}	Offset voltage(2), RTI				±100	±500	µV
		V_{IN+} = 0 V			±25	±150	
dV_{OS}/dT	Offset drift, RTI	T_A = –40°C to +125°C			0.2	1	µV/°C
PSRR	Power-supply rejection ratio, RTI	V_S = 2.7 V to 5.5 V, V_{SENSE} = 10 mV			±8	±40	µV/V
I_{IB}	Input bias current	V_{SENSE} = 0 mV, V_{IN+} = 0 V			0.1		µA
		V_{SENSE} = 0 mV			80		
I_{IO}	Input offset current	V_{SENSE} = 0 mV			±0.05		µA
OUTPUT							
G	Gain	A1 devices			20		V/V
		A2 devices			50		
		A3 devices			100		
		A4 devices			200		
E_G	Gain error	V_{OUT} = 0.5 V to V_S – 0.5 V, T_A = –40°C to +125°C			±0.1%	±1%	
	Gain error vs temperature	T_A = –40°C to +125°C			1.5	20	ppm/°C
	Nonlinearity error	V_{OUT} = 0.5 V to V_S – 0.5 V			±0.01%		
	Maximum capacitive load	No sustained oscillation			1		nF
VOLTAGE OUTPUT(3)							
V_{SP}	Swing to V_S power-supply rail(4)	R_L = 10 kΩ to GND, T_A = –40°C to +125°C			(V_S) – 0.02	(V_S) – 0.03	V
V_{SN}	Swing to GND(4)	R_L = 10 kΩ to GND, T_A = –40°C to +125°C			(V_{GND}) + 0.0005	(V_{GND}) + 0.005	V
FREQUENCY RESPONSE							
BW	Bandwidth	A1 devices, C_{LOAD} = 10 pF			350		kHz
		A2 devices, C_{LOAD} = 10 pF			210		
		A3 devices, C_{LOAD} = 10 pF			150		
		A4 devices, C_{LOAD} = 10 pF			105		
SR	Slew rate				2		V/µs
NOISE, RTI							
	Voltage noise density				40		nV/√Hz
POWER SUPPLY							
I_Q	Quiescent current	INA180-Q1	V_{SENSE} = 10 mV		197	260	µA
			V_{SENSE} = 10 mV, T_A = –40°C to +125°C			300	
		INA2180-Q1	V_{SENSE} = 10 mV		355	500	
			V_{SENSE} = 10 mV, T_A = –40°C to +125°C			520	
		INA4180-Q1	V_{SENSE} = 10 mV		690	900	
			V_{SENSE} = 10 mV, T_A = –40°C to +125°C			1000	

(1) RTI = referred-to-input.
(2) Offset voltage is obtained by linear extrapolation to V_{SENSE} = 0 V with V_{SENSE} = 10% to 90% of full-scale-range.
(3) See 図 7-19.
(4) Swing specifications are tested with an overdriven input condition.

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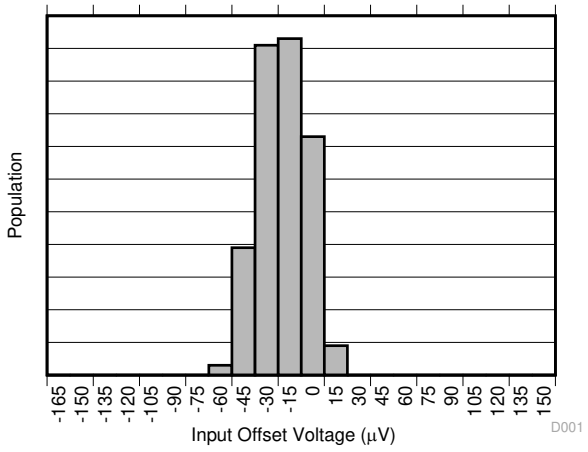
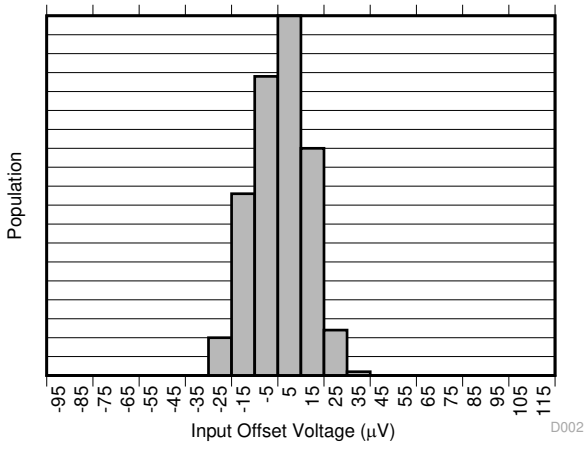
7.7 Typical Characteristics

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)



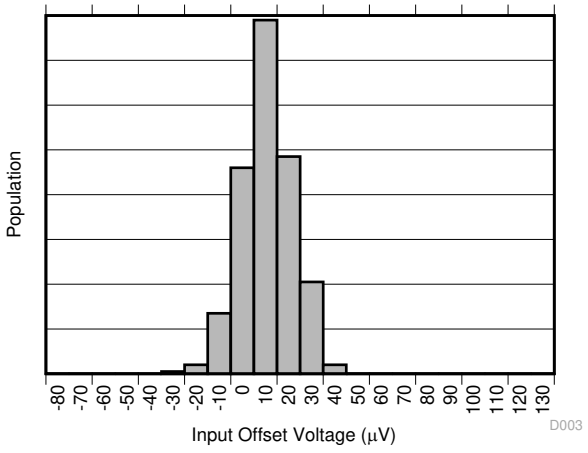
V_{IN+} = 0 V

図 7-1. Input Offset Voltage Production Distribution A1



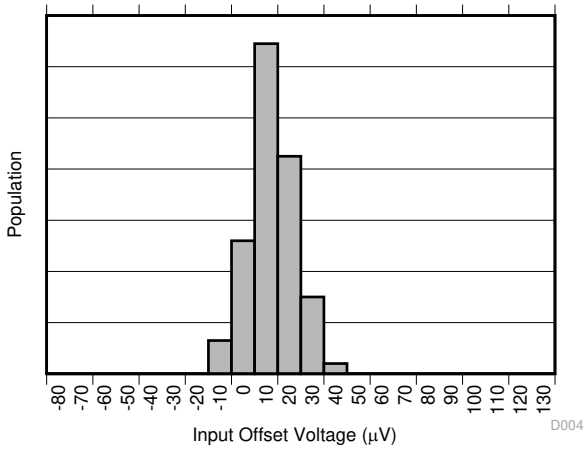
V_{IN+} = 0 V

図 7-2. Input Offset Voltage Production Distribution A2



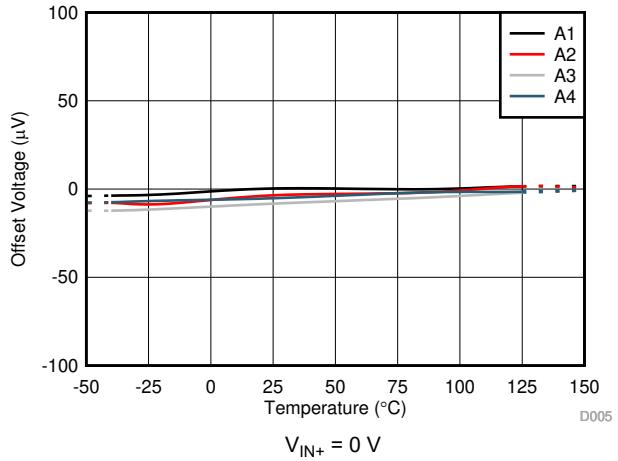
V_{IN+} = 0 V

図 7-3. Input Offset Voltage Production Distribution A3



V_{IN+} = 0 V

図 7-4. Input Offset Voltage Production Distribution A4



V_{IN+} = 0 V

図 7-5. Offset Voltage vs. Temperature

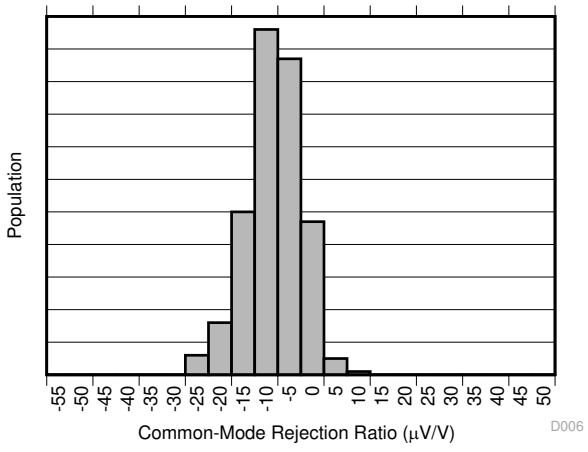


図 7-6. Common-Mode Rejection Production Distribution A1

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7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)

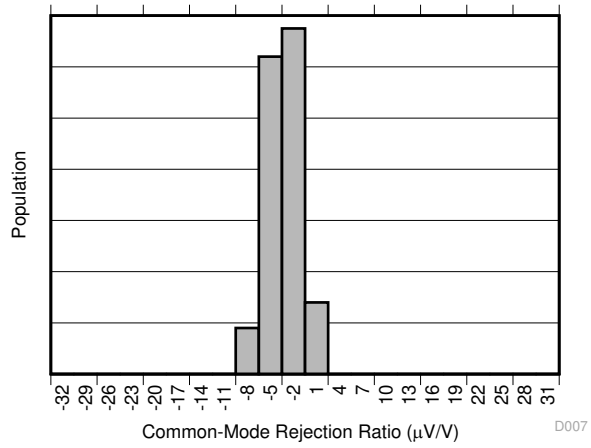

図 7-7. Common-Mode Rejection Production Distribution A2

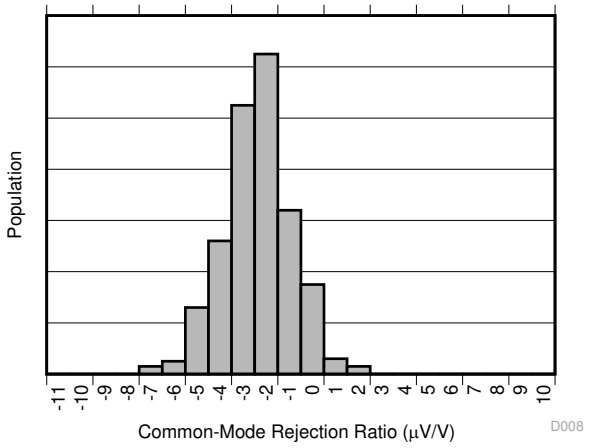

図 7-8. Common-Mode Rejection Production Distribution A3

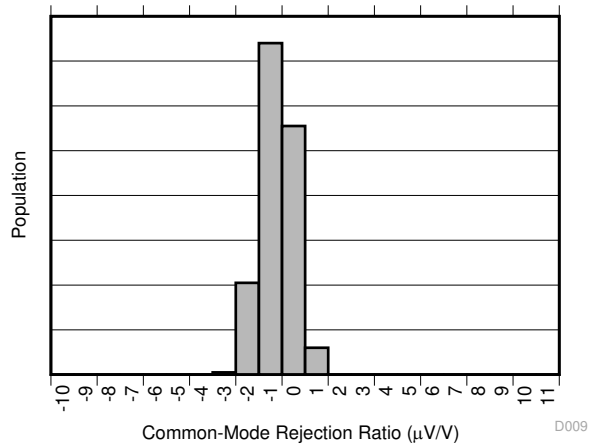

図 7-9. Common-Mode Rejection Production Distribution A4

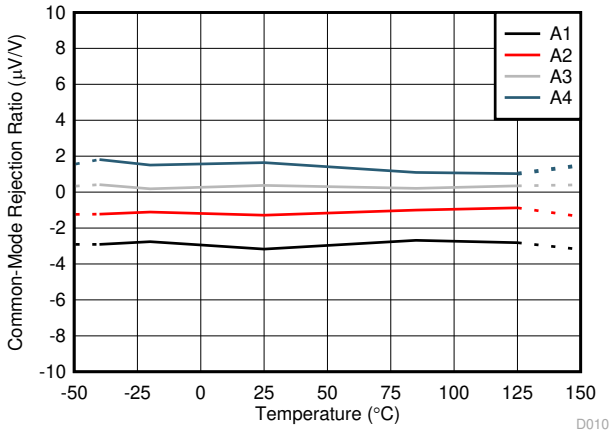

図 7-10. Common-Mode Rejection Ratio vs. Temperature

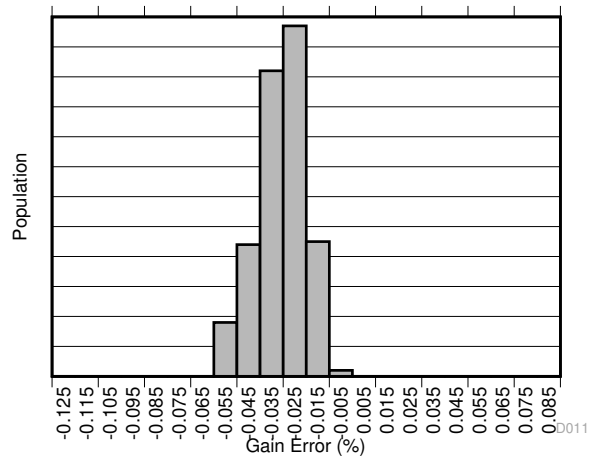

図 7-11. Gain Error Production Distribution A1

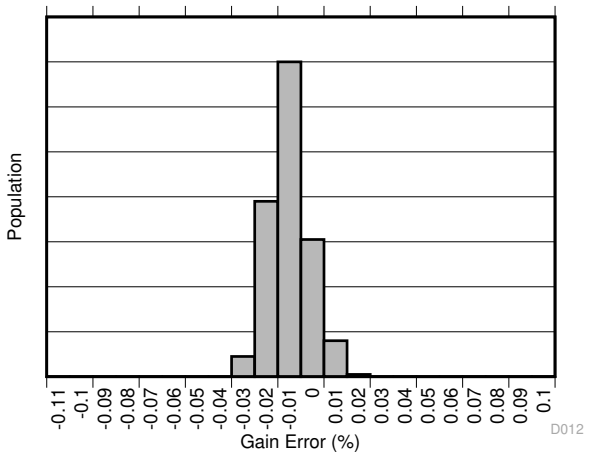

図 7-12. Gain Error Production Distribution A2

7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)

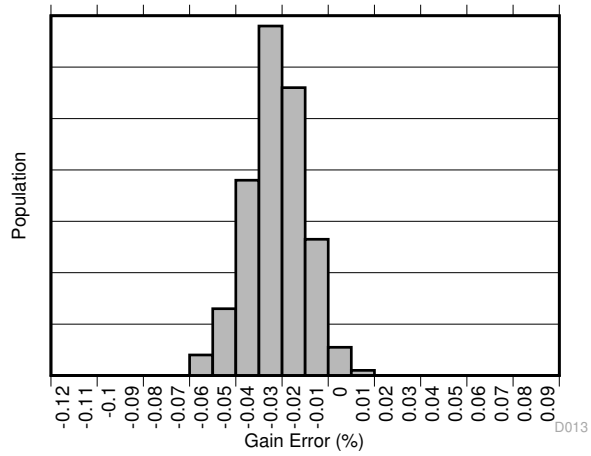

図 7-13. Gain Error Production Distribution A3

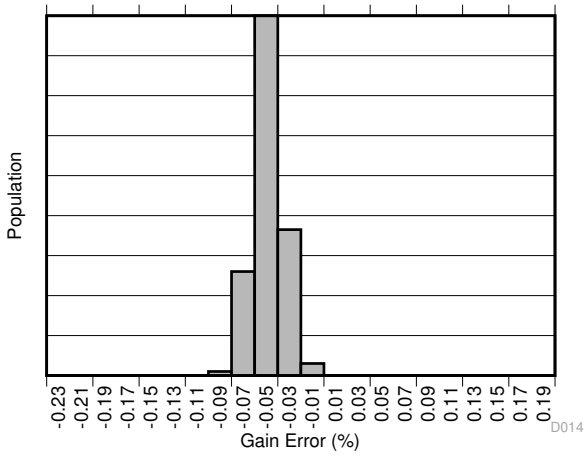

図 7-14. Gain Error Production Distribution A4

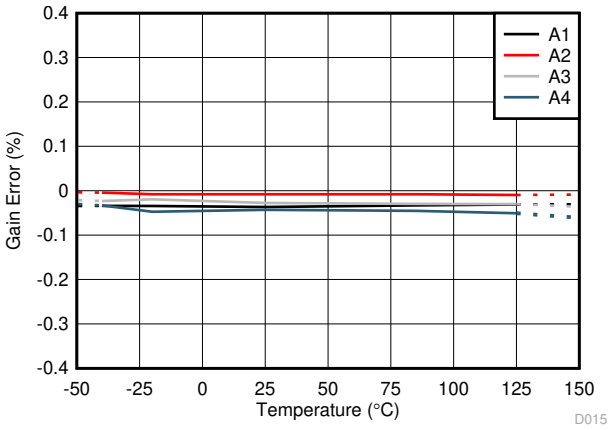

図 7-15. Gain Error vs. Temperature

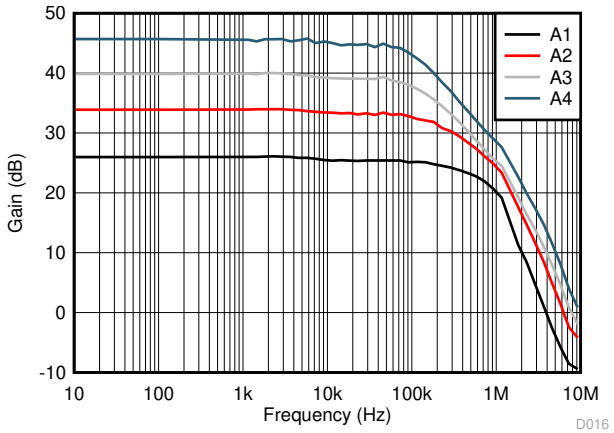

図 7-16. Gain vs. Frequency

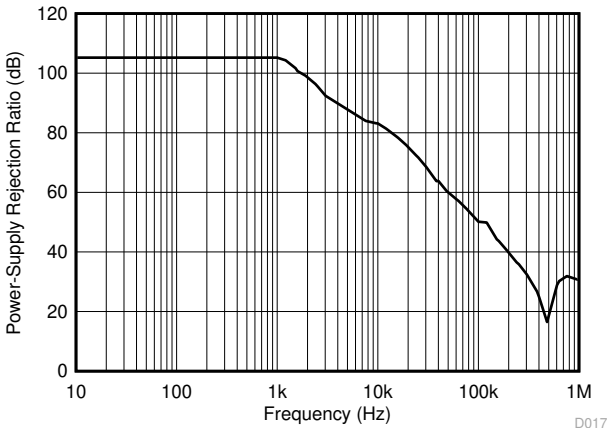

図 7-17. Power-Supply Rejection Ratio vs. Frequency

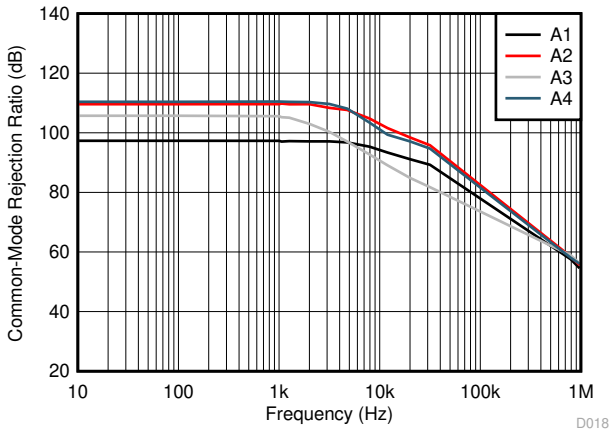

図 7-18. Common-Mode Rejection Ratio vs. Frequency

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7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)

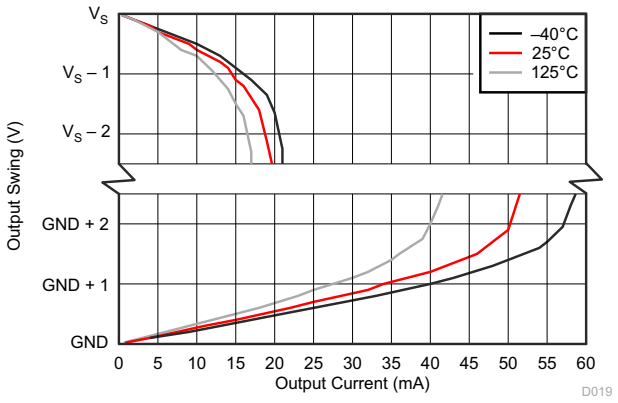
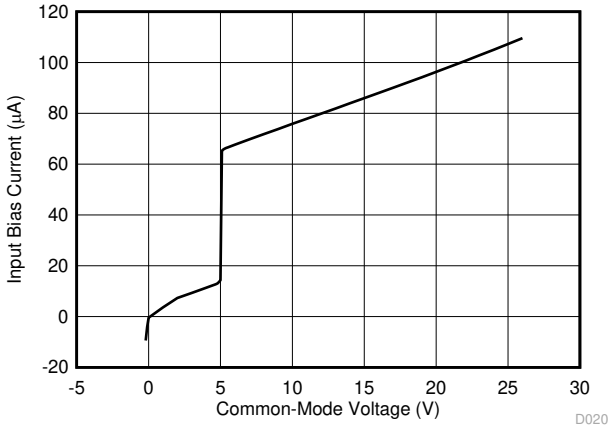
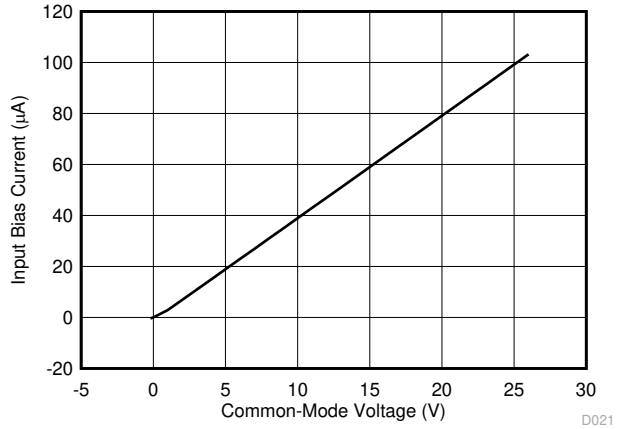


図 7-19. Output Voltage Swing vs. Output Current



Supply voltage = 5 V

図 7-20. Input Bias Current vs. Common-Mode Voltage



Supply voltage = 0 V

図 7-21. Input Bias Current vs. Common-Mode Voltage (Both Inputs, Shutdown)

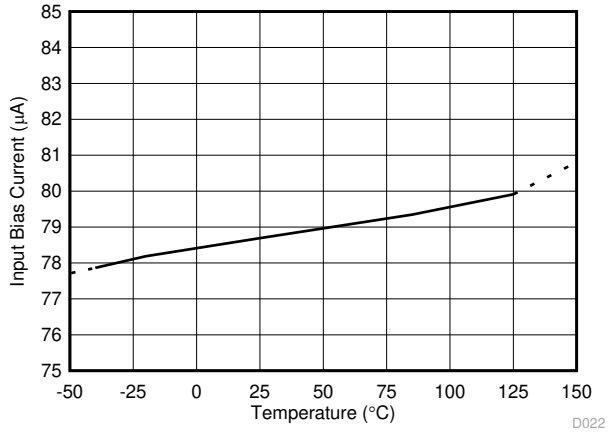


図 7-22. Input Bias Current vs. Temperature

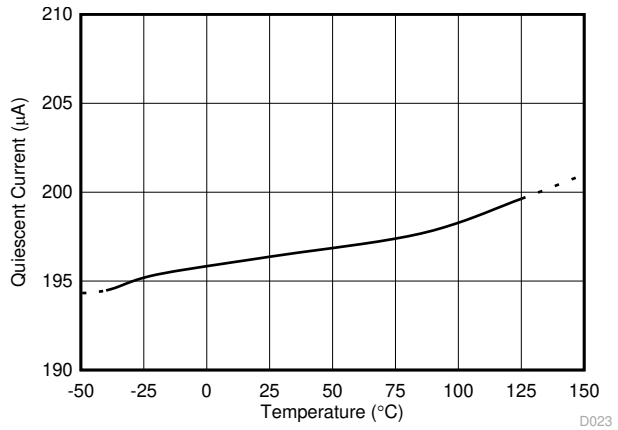


図 7-23. Quiescent Current vs. Temperature (INA180-Q1)

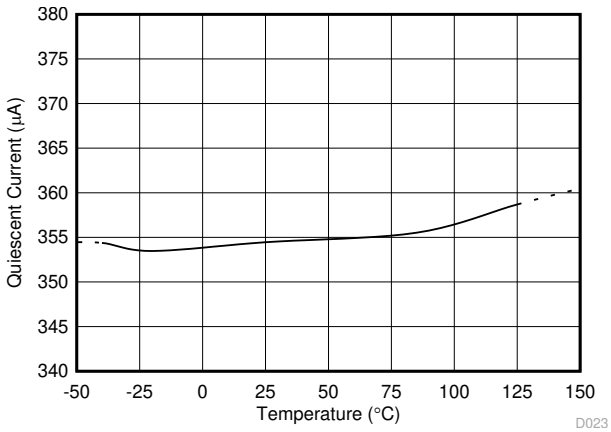


図 7-24. Quiescent Current vs. Temperature (INA2180-Q1)

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7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)

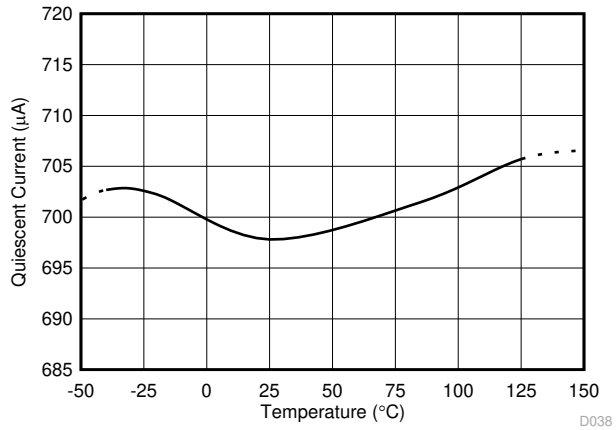

図 7-25. Quiescent Current vs. Temperature (INA4180-Q1)

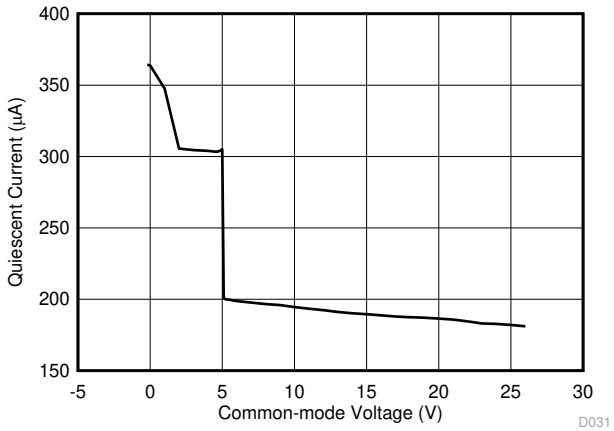

図 7-26. Quiescent Current vs. Common-Mode Voltage (INA180-Q1)

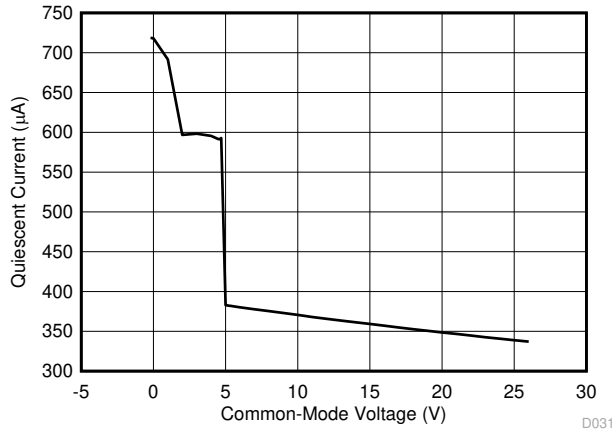

図 7-27. Quiescent Current vs. Common-Mode Voltage for All Amplifiers (INA2180-Q1)

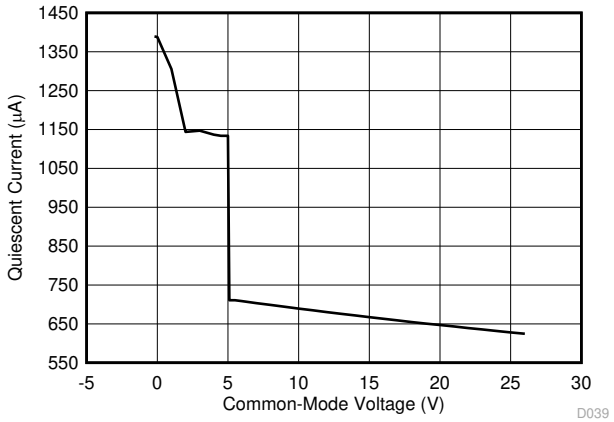

図 7-28. Quiescent Current vs. Common-Mode Voltage for All Amplifiers (INA4180-Q1)

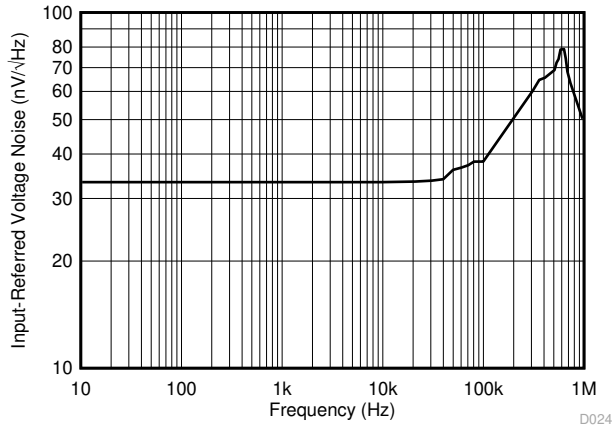

図 7-29. Input-Referred Voltage Noise vs. Frequency (A3 Devices)

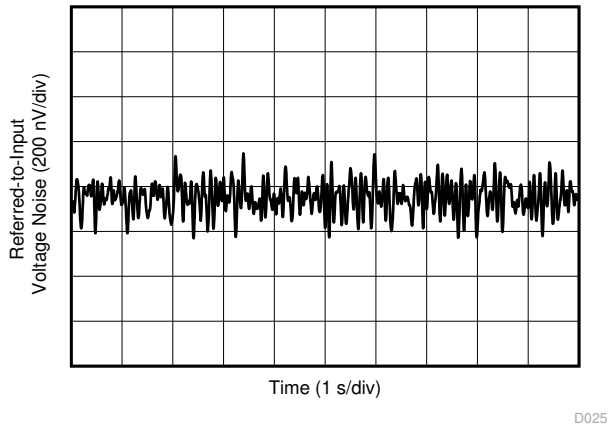

図 7-30. 0.1-Hz to 10-Hz Voltage Noise (Referred-to-Input)

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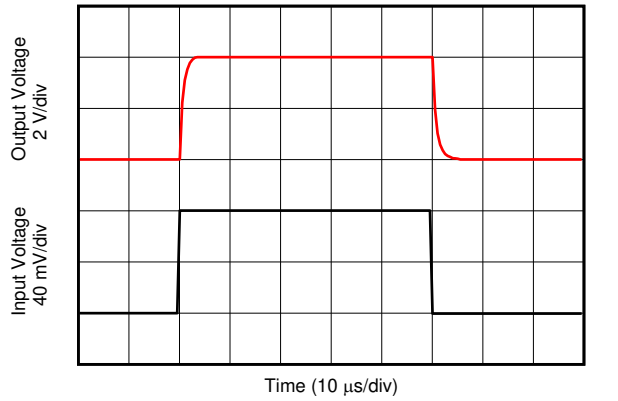
7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)



80-mV_{PP} input step

図 7-31. Step Response

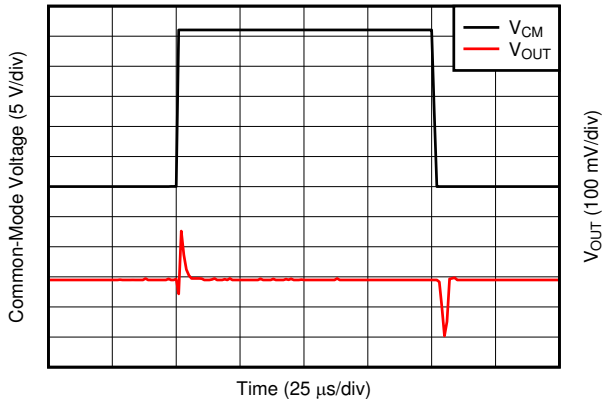


図 7-32. Common-Mode Voltage Transient Response

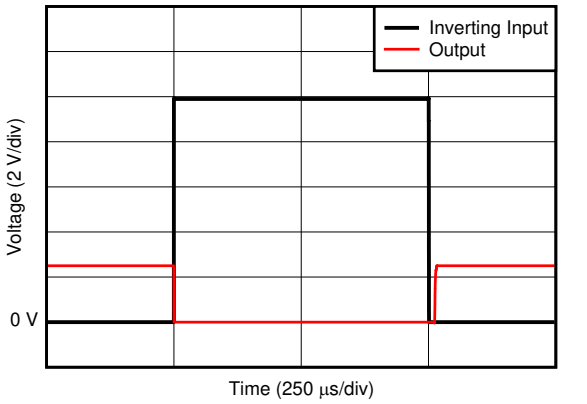


図 7-33. Inverting Differential Input Overload

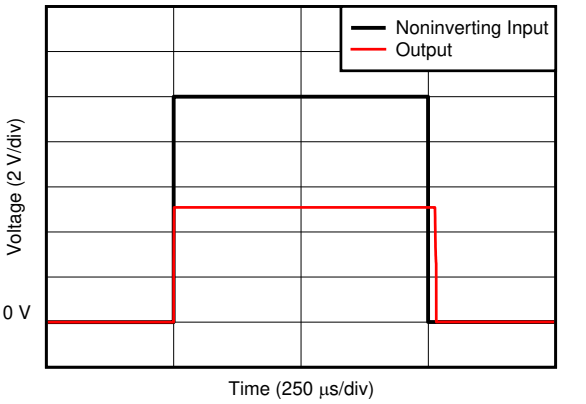


図 7-34. Noninverting Differential Input Overload

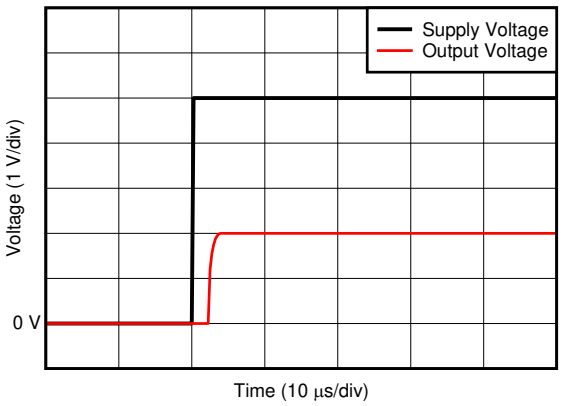


図 7-35. Start-Up Response

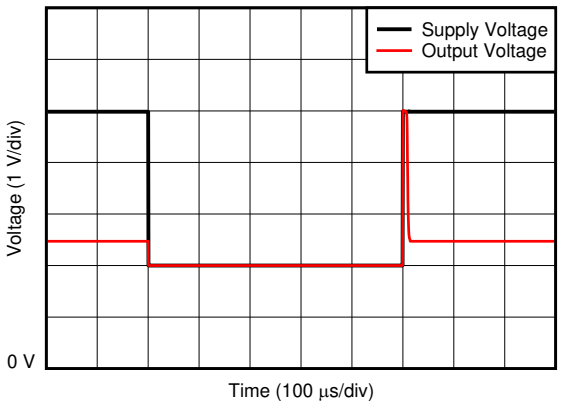


図 7-36. Brownout Recovery

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7.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, and V_{IN+} = 12 V (unless otherwise noted)

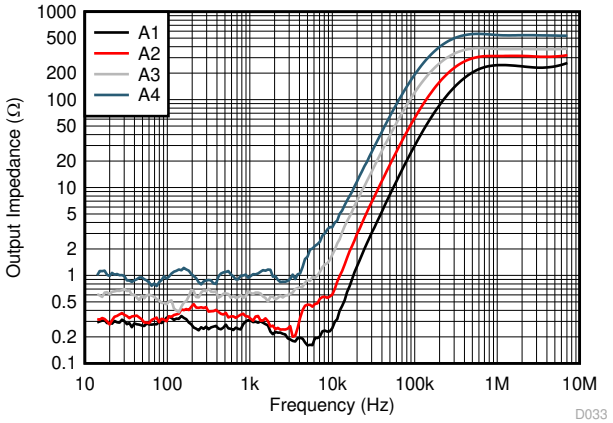

図 7-37. Output Impedance vs. Frequency

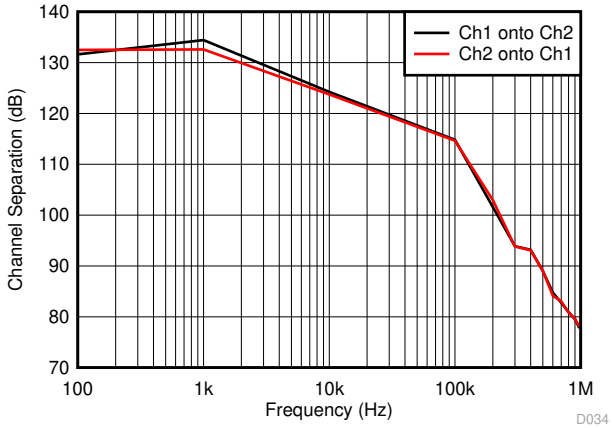

図 7-38. Channel Separation vs. Frequency (INA2180)

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8 Detailed Description

8.1 Overview

The INA180-Q1, INA2180-Q1, and INA4180-Q1 (INAx180-Q1) are automotive-grade, 26-V, common-mode, current-sensing amplifiers used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers accurately measures voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V, and the devices can be powered from supply voltages as low as 2.7 V.

8.2 Functional Block Diagrams

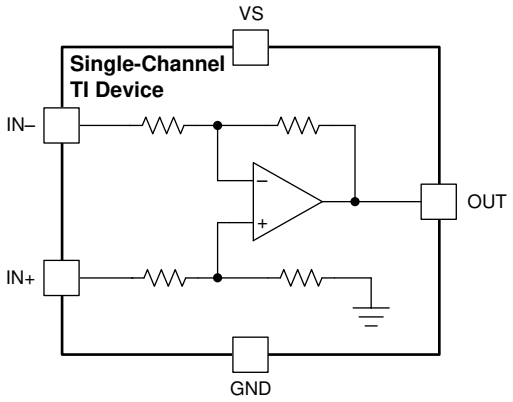

図 8-1. INA180-Q1 Functional Block Diagram

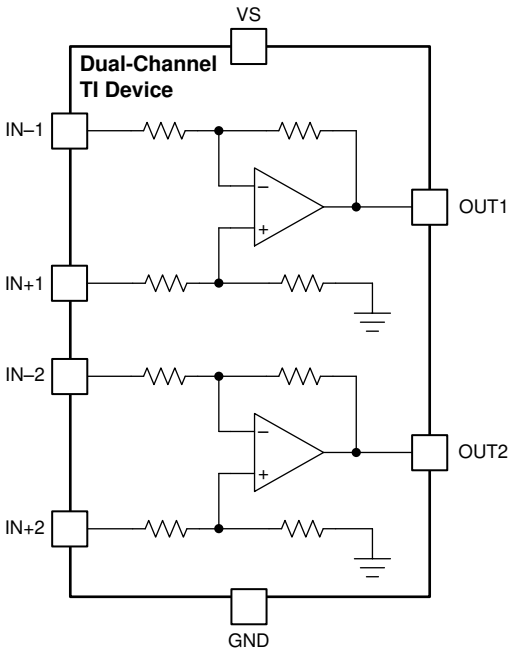

図 8-2. INA2180-Q1 Functional Block Diagram

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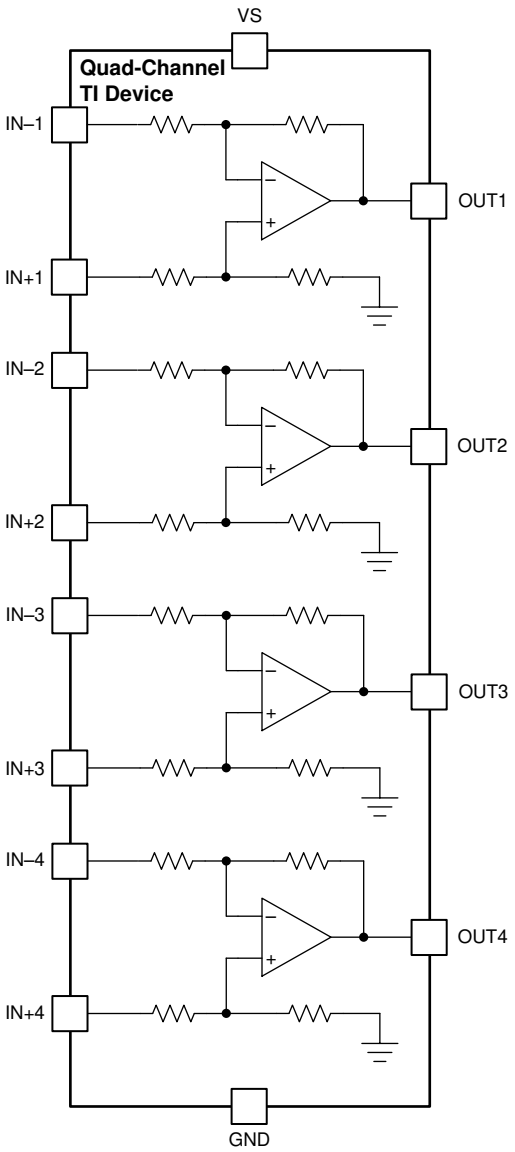

図 8-3. INA4180-Q1 Functional Block Diagram

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8.3 Feature Description

8.3.1 High Bandwidth and Slew Rate

The INAx180-Q1 support small-signal bandwidths as high as 350 kHz, and large-signal slew rates of 2 V/µs. The ability to detect rapid changes in the sensed current, as well as the ability to quickly slew the output, make the INAx180-Q1 a good choice for applications that require a quick response to input current changes. One application that requires high bandwidth and slew rate is low-side motor control, where the ability to follow rapid changing current in the motor allows for more accurate control over a wider operating range. Another application that requires higher bandwidth and slew rates is system fault detection, where the INAx180-Q1 are used with an external comparator and a reference to quickly detect when the sensed current is out of range.

8.3.2 Wide Input Common-Mode Voltage Range

The INAx180-Q1 support input common-mode voltages from –0.2 V to +26 V. Because of the internal topology, the common-mode range is not restricted by the power-supply voltage (V_S) as long as V_S stays within the operational range of 2.7 V to 5.5 V. The ability to operate with common-mode voltages greater or less than V_S allow the INAx180-Q1 to be used in high-side, as well as low-side, current-sensing applications, as shown in 図 8-4.

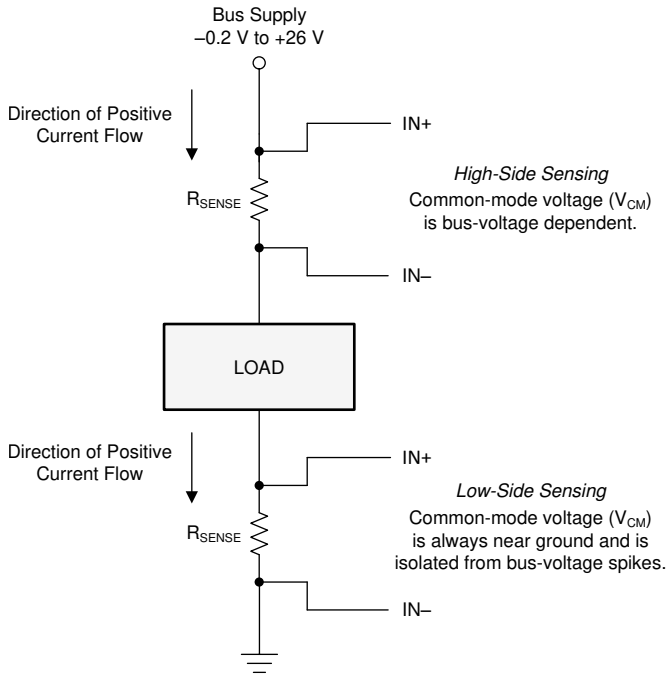

図 8-4. High-Side and Low-Side Sensing Connections

8.3.3 Precise Low-Side Current Sensing

When used in low-side current sensing applications the offset voltage of the INAx180-Q1 is within ±150 µV. The low offset performance of the INAx180-Q1 has several benefits. First, the low offset allows the device to be used in applications that must measure current over a wide dynamic range. In this case, the low offset improves the accuracy when the sensed currents are on the low end of the measurement range. Another advantage of low offset is the ability to sense lower voltage drop across the sense resistor accurately, thus allowing a lower-value shunt resistor. Lower-value shunt resistors reduce power loss in the current sense circuit, and help improve the power efficiency of the end application.

The gain error of the INAx180-Q1 is specified to be within 1% of the actual value. As the sensed voltage becomes much larger than the offset voltage, this voltage becomes the dominant source of error in the current sense measurement.

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8.3.4 Rail-to-Rail Output Swing

The INAx180-Q1 allow linear current sensing operation with the output close to the supply rail and GND. The maximum specified output swing to the positive rail is 30 mV, and the maximum specified output swing to GND is only 5 mV. To compare the output swing of the INAx180-Q1 to an equivalent operational amplifier (op amp), the inputs are overdriven to approximate the open-loop condition specified in op amp data sheets. The current-sense amplifier is a closed-loop system; therefore, the output swing to GND can be limited by the product of the offset voltage and amplifier gain.

For devices that have positive offset voltages, the swing to GND is limited by the larger of either the offset voltage multiplied by the gain or the swing to GND specified in the *Electrical Characteristics* table.

For example, in an application where the INA180A4-Q1 (gain = 200 V/V) is used for low-side current sensing and the device has an offset of 40 µV, the product of the device offset and gain results in a value of 8 mV, greater than the specified negative swing value. Therefore, the swing to GND for this example is 8 mV. If the same device has an offset of –40 µV, then the calculated zero differential signal is –8 mV. In this case, the offset helps overdrive the swing in the negative direction, and swing performance is consistent with the value specified in the *Electrical Characteristics* table.

The offset voltage is a function of the common-mode voltage as determined by the CMRR specification; therefore, the offset voltage increases when higher common-mode voltages are present. The increase in offset voltage limits how low the output voltage can go during a zero-current condition when operating at higher common-mode voltages. 図 8-5 shows the typical limitation of the zero-current output voltage vs common-mode voltage for each gain option.

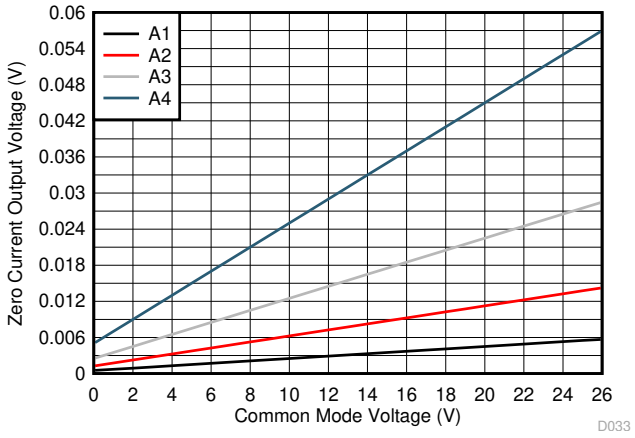

図 8-5. Zero-Current Output Voltage vs Common-Mode Voltage

8.4 Device Functional Modes

8.4.1 Normal Mode

The INAx180-Q1 is in normal operation when the following conditions are met:

- The power supply voltage (V_S) is between 2.7 V and 5.5 V.
- The common-mode voltage (V_{CM}) is within the specified range of –0.2 V to +26 V.
- The maximum differential input signal times gain is less than V_S minus the output voltage swing to V_S.
- The minimum differential input signal times gain is greater than the swing to GND (see the *Rail-to-Rail Output Swing* section).

During normal operation, the device produces an output voltage that is the *gained-up* representation of the difference voltage from IN+ to IN–.

8.4.2 Input Differential Overload

If the differential input voltage ($V_{IN+} – V_{IN–}$) times gain exceeds the voltage swing specification, the INAx180-Q1 drive the output as close as possible to the positive supply, and does not provide accurate measurement of the

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differential input voltage. If this input overload occurs during normal circuit operation, then reduce the value of the shunt resistor or use a lower-gain version with the chosen sense resistor to avoid this mode of operation. If a differential overload occurs in a fault event, then the output of the INAx180-Q1 return to the expected value approximately 20 µs after the fault condition is removed.

When the INAx180-Q1 output is driven to either the supply rail or ground, increasing the differential input voltage does not damage the device as long as the absolute maximum ratings are not violated. Following these guidelines, the INAx180-Q1 output maintains polarity, and does not suffer from phase reversal.

8.4.3 Shutdown Mode

Although the INAx180-Q1 do not have a shutdown pin, the low power consumption of the device allows the output of a logic gate or transistor switch to power the INAx180-Q1. This gate or switch turns on and off the INAx180-Q1 power-supply quiescent current.

However, in current shunt monitoring applications, there is also a concern for how much current is drained from the shunt circuit in shutdown conditions. Evaluating this current drain involves considering the simplified schematic of the INAx180-Q1 in shutdown mode, as shown in 図 8-6.

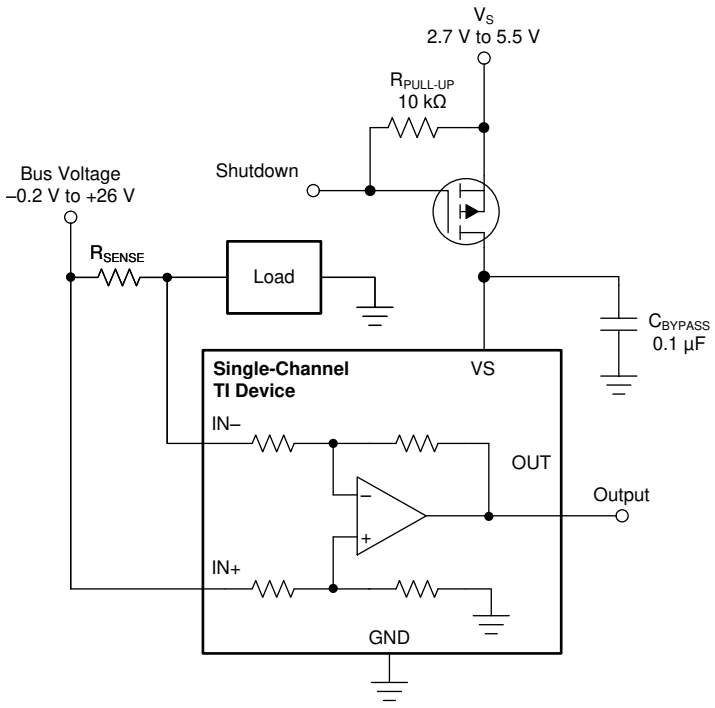

図 8-6. Basic Circuit to Shut Down the INxA180-Q1

There is typically more than 500 kΩ of impedance (from the combination of 500-kΩ feedback and input gain set resistors) from each input of the INAx180-Q1 to the OUT pin and to the GND pin. The amount of current flowing through these pins depends on the voltage at the connection.

Regarding the 500-kΩ path to the output pin, the output stage of a disabled INAx180-Q1 does constitute a good path to ground. Consequently, this current is directly proportional to a shunt common-mode voltage present across a 500-kΩ resistor.

As a final note, as long as the shunt common-mode voltage is greater than V_S when the device is powered up, there is an additional and well-matched 55-µA typical current that flows in each of the inputs. If less than V_S, the common-mode input currents are negligible, and the only current effects are the result of the 500-kΩ resistors.

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9 Application and Implementation

注

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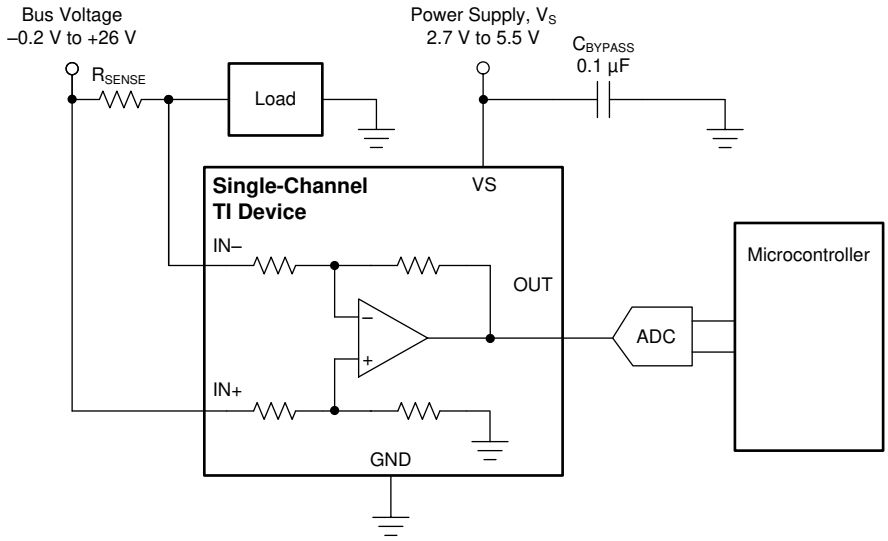
9.1 Application Information

The INAx180-Q1 amplify the voltage developed across a current-sensing resistor as current flows through the resistor to the load or ground.

9.1.1 Basic Connections

図 9-1 shows the basic connections of the INA180-Q1. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.



NOTE: For best measurement accuracy, connect analog-to-digital converter (ADC) reference or microcontroller ground as closely as possible to the INAx180-Q1 GND pin, and add an RC filter between the output of the INAx180-Q1 and the ADC. See *Closed-Loop Analysis of Load-Induced Amplifier Stability Issues Using Z_{OUT}* for more details.

図 9-1. Basic Connections for the INA180

A power-supply bypass capacitor of at least 0.1 µF is required for proper operation. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

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9.1.2 R_{SENSE} and Device Gain Selection

The accuracy of the INAx180-Q1 is maximized by choosing the current-sense resistor to be as large as possible. A large sense resistor maximizes the differential input signal for a given amount of current flow and reduces the error contribution of the offset voltage. However, there are practical limits as to how large the current-sense resistor can be in a given application. The INAx180-Q1 have a typical input bias currents of 80 µA for each input when operated at a 12-V common-mode voltage input. When large current-sense resistors are used, these bias currents cause increased offset error and reduced common-mode rejection. Therefore, using current-sense resistors larger than a few ohms is generally not recommended for applications that require current-monitoring accuracy. A second common restriction on the value of the current-sense resistor is the maximum allowable power dissipation that is budgeted for the resistor. 式 1 gives the maximum value for the current sense resistor for a given power dissipation budget:

$$R_{SENSE} < \frac{PD_{MAX}}{I_{MAX}^2} \tag{1}$$

where:

- PD_{MAX} is the maximum allowable power dissipation in R_{SENSE}.
- I_{MAX} is the maximum current that will flow through R_{SENSE}.

An additional limitation on the size of the current-sense resistor and device gain is due to the power-supply voltage, V_S, and device swing to rail limitations. In order to make sure that the current-sense signal is properly passed to the output, both positive and negative output swing limitations must be examined. 式 2 provides the maximum values of R_{SENSE} and GAIN to keep the device from hitting the positive swing limitation.

$$I_{MAX} \times R_{SENSE} \times GAIN < V_{SP} \tag{2}$$

where:

- I_{MAX} is the maximum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense-amplifier.
- V_{SP} is the positive output swing as specified in the data sheet.

To avoid positive output swing limitations when selecting the value of R_{SENSE}, there is always a trade-off between the value of the sense resistor and the gain of the device under consideration. If the sense resistor selected for the maximum power dissipation is too large, then it is possible to select a lower-gain device in order to avoid positive swing limitations.

The negative swing limitation places a limit on how small of a sense resistor can be used in a given application. 式 3 provides the limit on the minimum size of the sense resistor.

$$I_{MIN} \times R_{SENSE} \times GAIN > V_{SN} \tag{3}$$

where:

- I_{MIN} is the minimum current that will flow through R_{SENSE}.
- GAIN is the gain of the current sense amplifier.
- V_{SN} is the negative output swing of the device (see *Rail-to-Rail Output Swing*).

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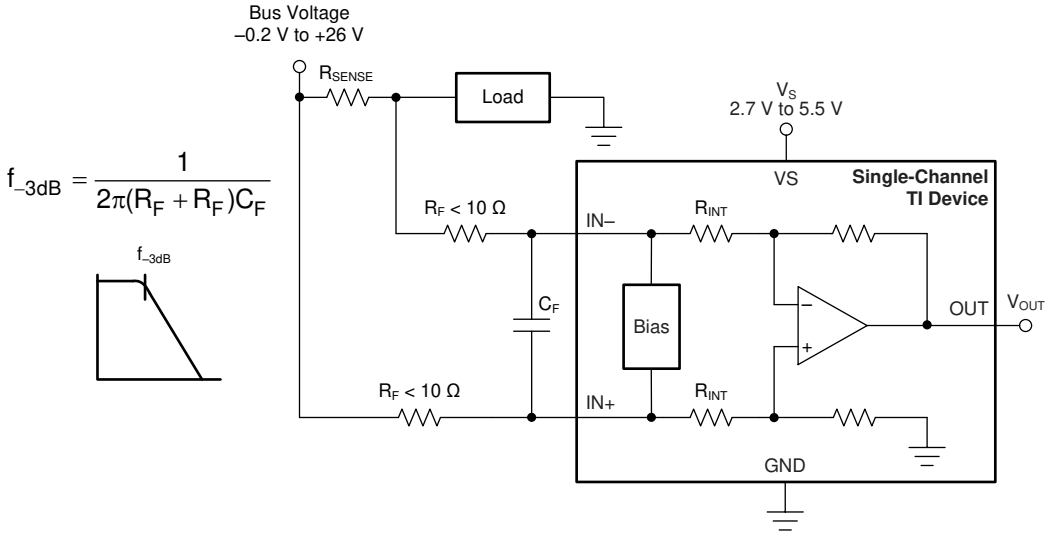
9.1.3 Signal Filtering

Provided that the INAx180-Q1 output is connected to a high impedance input, the best location to filter is at the device output using a simple RC network from OUT to GND. Filtering at the output attenuates high-frequency disturbances in the common-mode voltage, differential input signal, and INAx180-Q1 power-supply voltage. If filtering at the output is not possible, or filtering of only the differential input signal is required, it is possible to apply a filter at the input pins of the device. 図 9-2 provides an example of how a filter can be used on the input pins of the device.



$$f_{-3dB} = \frac{1}{2\pi(R_F + R_F)C_F}$$

図 9-2. Filter at Input Pins

The addition of external series resistance creates an additional error in the measurement; therefore, the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in 図 9-2 present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed across the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using 式 5, where the gain error factor is calculated using 式 4.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance (R_F) value as well as internal input resistor R_{INT}, as shown in 図 9-2. The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Calculate the expected deviation from the shunt voltage to what is measured at the device input pins is given using 式 4:

$$\text{Gain Error Factor} = \frac{1250 \times R_{INT}}{(1250 \times R_F) + (1250 \times R_{INT}) + (R_F \times R_{INT})} \quad (4)$$

where:

- R_{INT} is the internal input resistor.
- R_F is the external series resistance.

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With the adjustment factor from 式 4, including the device internal input resistance, this factor varies with each gain version, as shown in 表 9-1. Each individual device gain error factor is shown in 表 9-2.

表 9-1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INAx180A1-Q1	20	25
INAx180A2-Q1	50	10
INAx180A3-Q1	100	5
INAx180A4-Q1	200	2.5

表 9-2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INAx180A1-Q1	$\frac{25000}{(21 \times R_F) + 25000}$
INAx180A2-Q1	$\frac{10000}{(9 \times R_F) + 10000}$
INAx180A3-Q1	$\frac{1000}{R_F + 1000}$
INAx180A4-Q1	$\frac{2500}{(3 \times R_F) + 2500}$

The gain error that can be expected from the addition of the external series resistors can then be calculated based on 式 5:

$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (5)$$

For example, using an INA180A2-Q1 and the corresponding gain error equation from 表 9-2, a series resistance of
10 Ω results in a gain error factor of 0.991. The corresponding gain error is then calculated using 式 5, resulting in an additional gain error of approximately 0.89% solely because of the external 10-Ω series resistors.

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9.2 Typical Application

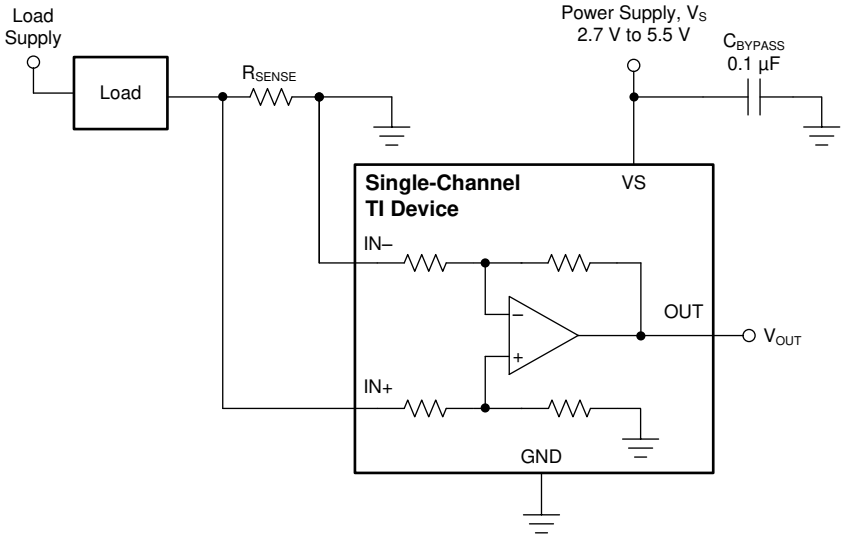

図 9-3. Low-Side Sensing

9.2.1 Design Requirements

The design requirements for the circuit shown in 図 9-3, are listed in 表 9-3

表 9-3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Power-supply voltage, V_S	5 V
Low-side current sensing	V_{CM} = 0 V
R_{SENSE} power loss	< 900 mW
Maximum sense current, I_{MAX}	40 A
Current sensing error	Less than 1.5% at maximum current, T_J = 25°C
Small-signal bandwidth	> 80 kHz

9.2.2 Detailed Design Procedure

The maximum value of the current sense resistor is calculated based on the maximum power loss requirement. By applying 式 1, the maximum value of the current-sense resistor is calculated to be 0.563 mΩ. This is the maximum value for sense resistor R_{SENSE}; therefore, select R_{SENSE} to be 0.5 mΩ because it is the closest standard resistor value that meets the power-loss requirement.

The next step is to select the appropriate gain and reduce R_{SENSE}, if needed, to keep the output signal swing within the V_S range. Using 式 2, and given that I_{MAX} = 40 A and R_{SENSE} = 0.5 mΩ, the maximum current-sense gain calculated to avoid the positive swing-to-rail limitations on the output is 248.5. To maximize the output signal range, the INA180A4-Q1 (gain = 200) device is selected for this application.

To calculate the accuracy at peak current, the two factors that must be determined are the gain error and the offset error. The gain error of the INAx180-Q1 is specified to be a maximum of 1%. The error due to the offset is constant, and is specified to be 125 µV (maximum) for the conditions where V_{CM} = 0 V and V_S = 5 V. Using 式 6, the percentage error contribution of the offset voltage is calculated to be 0.75%, with total offset error = 150 µV, R_{SENSE} = 0.5 mΩ, and I_{SENSE} = 40 A.

$$\text{Total Offset Error (\%)} = \frac{\text{Total Offset Error (V)}}{I_{SENSE} \times R_{SENSE}} \times 100\% \quad (6)$$

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One method of calculating the total error is to add the gain error to the percentage contribution of the offset error. However, in this case, the gain error and the offset error do not have an influence or correlation to each other. A more statistically accurate method of calculating the total error is to use the RSS sum of the errors, as shown in 式 7:

$$\text{Total Error (\%)} = \sqrt{\text{Total Gain Error (\%)}^2 + \text{Total Offset Error (\%)}^2} \quad (7)$$

After applying 式 7, the total current sense error at maximum current is calculated to be 1.25%, and that is less than the design example requirement of 1.5%.

The INA180A4-Q1 (gain = 200) also has a bandwidth of 105 kHz that meets the small-signal bandwidth requirement of 80 kHz. If higher bandwidth is required, lower-gain devices can be used at the expense of either reduced output voltage range or an increased value of R_{SENSE}.

9.2.3 Application Curve

図 9-4 shows an example output response of a unidirectional configuration. The device output swing is limited by ground; therefore, the output is biased to this zero output level. The output rises above ground for positive differential input signals, but cannot fall below ground for negative differential input signals.

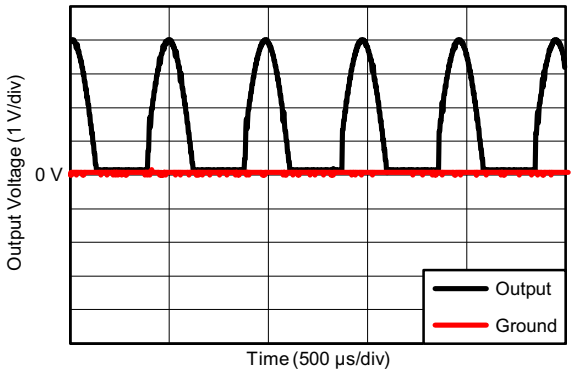

図 9-4. Output Response

9.3 Power Supply Recommendations

The input circuitry of the INAx180-Q1 accurately measures beyond the power-supply voltage, V_S. For example, V_S can be 5 V, whereas the bus supply voltage at IN+ and IN– can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the VS pin. The INAx180-Q1 also withstand the full differential input signal range up to 26 V at the IN+ and IN– input pins, regardless of whether or not the device has power applied at the VS pin.

9.3.1 Common-Mode Transients Greater Than 26 V

With a small amount of additional circuitry, the INAx180-Q1 can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diodes or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Start by adding a pair of resistors as a working impedance for the Zener diode, as shown 図 9-5. Keep these resistors as small as possible; most often, around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Signal Filtering* section. This circuit limits only short-term transients; therefore, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest acceptable power rating. This combination uses the least amount of board space. These diodes can be found in packages as small as
SOT-523 or SOD-523.

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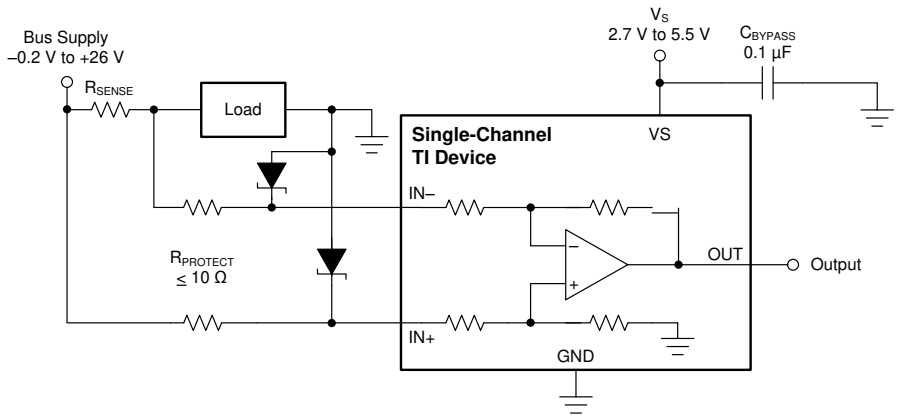

図 9-5. Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability, a higher-power transzorb must be used. The most package-efficient solution involves using a single transzorb and back-to-back diodes between the device inputs, as shown in 図 9-6. The most space-efficient solutions are dual, series-connected diodes in a single SOT-523 or SOD-523 package. In either of the examples shown in 図 9-5 and 図 9-6, the total board area required by the INAx180-Q1 with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

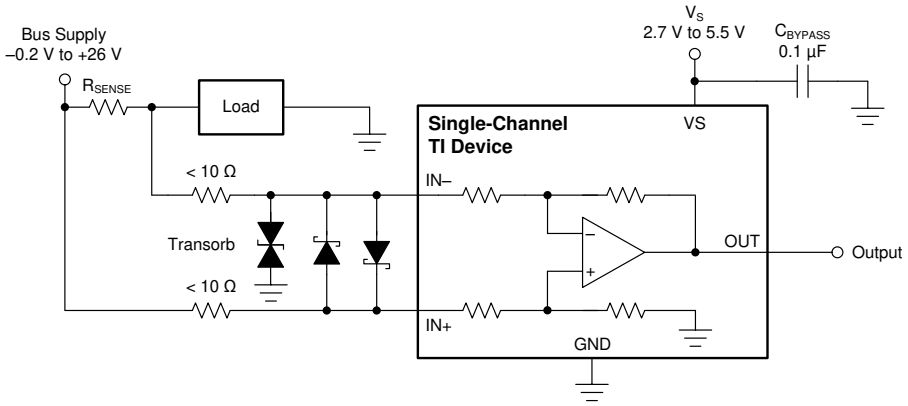

図 9-6. Transient Protection Using a Single Transzorb and Input Clamps

For a reference design example, see *Current Shunt Monitor With Transient Robustness Reference Design.*

9.4 Layout

9.4.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique makes sure that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as close as possible to the device power supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.
- When routing the connections from the current sense resistor to the device, keep the trace lengths as close as possible in order to minimize any impedance mismatch.

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9.4.2 Layout Examples

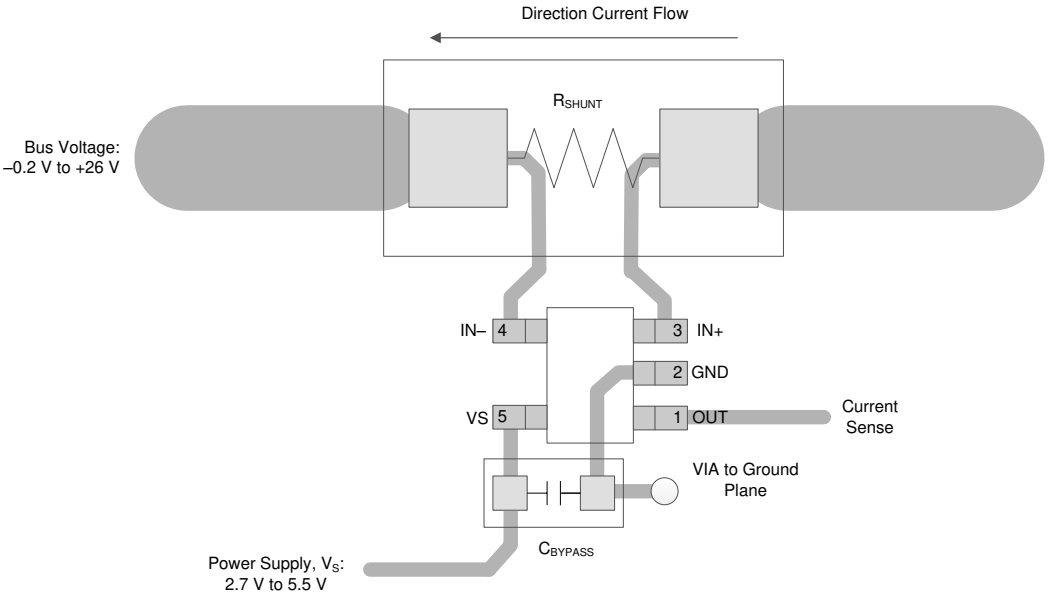

図 9-7. Single-Channel Recommended Layout (Pinout A)

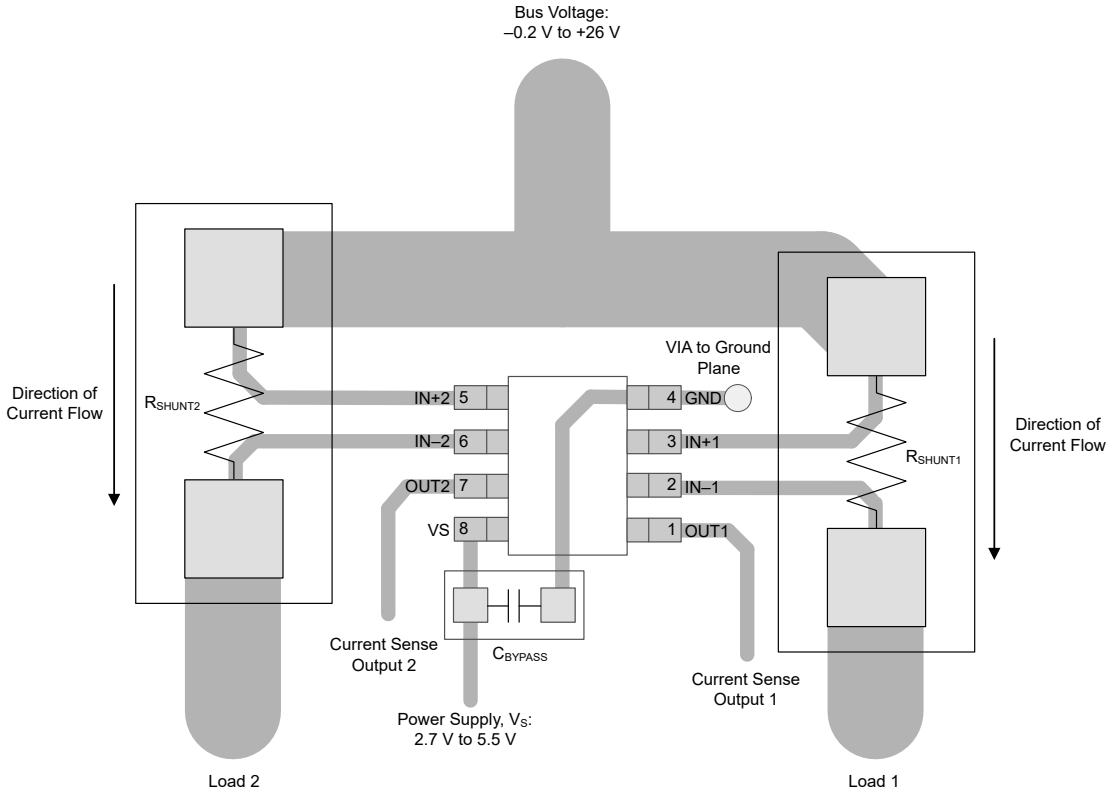

図 9-8. Dual-Channel Recommended Layout (VSSOP)

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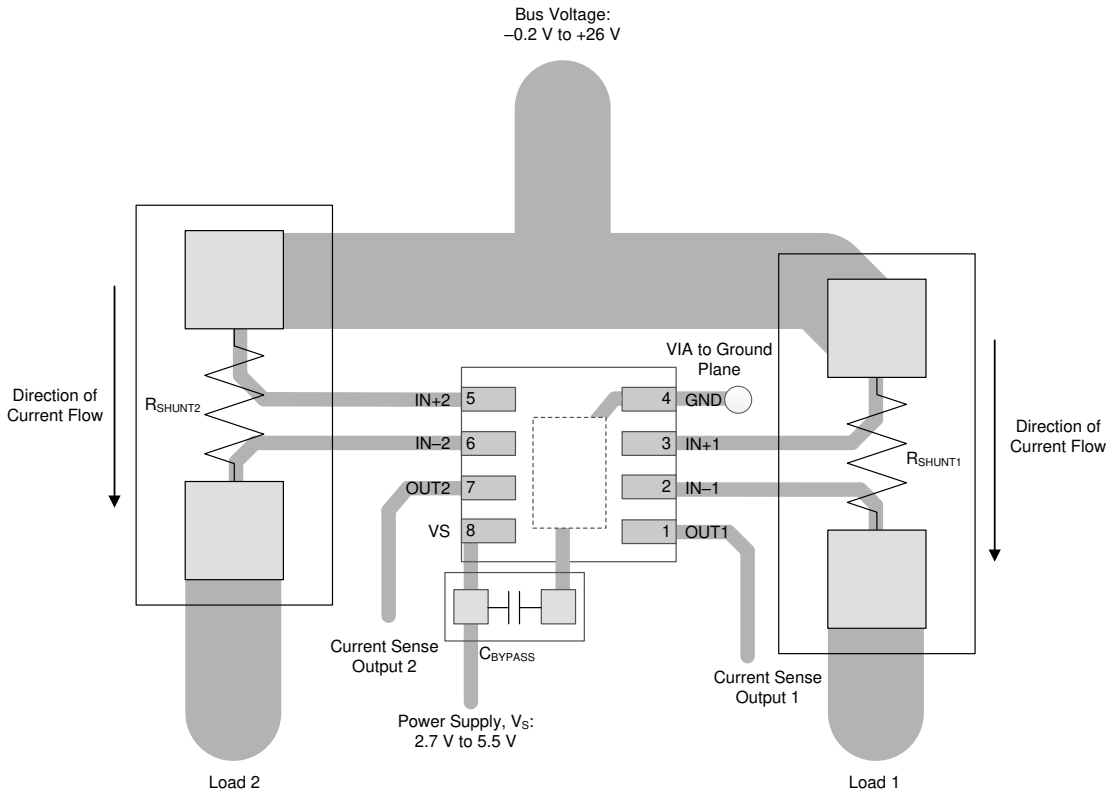

図 9-9. Dual-Channel Recommended Layout (WSON)

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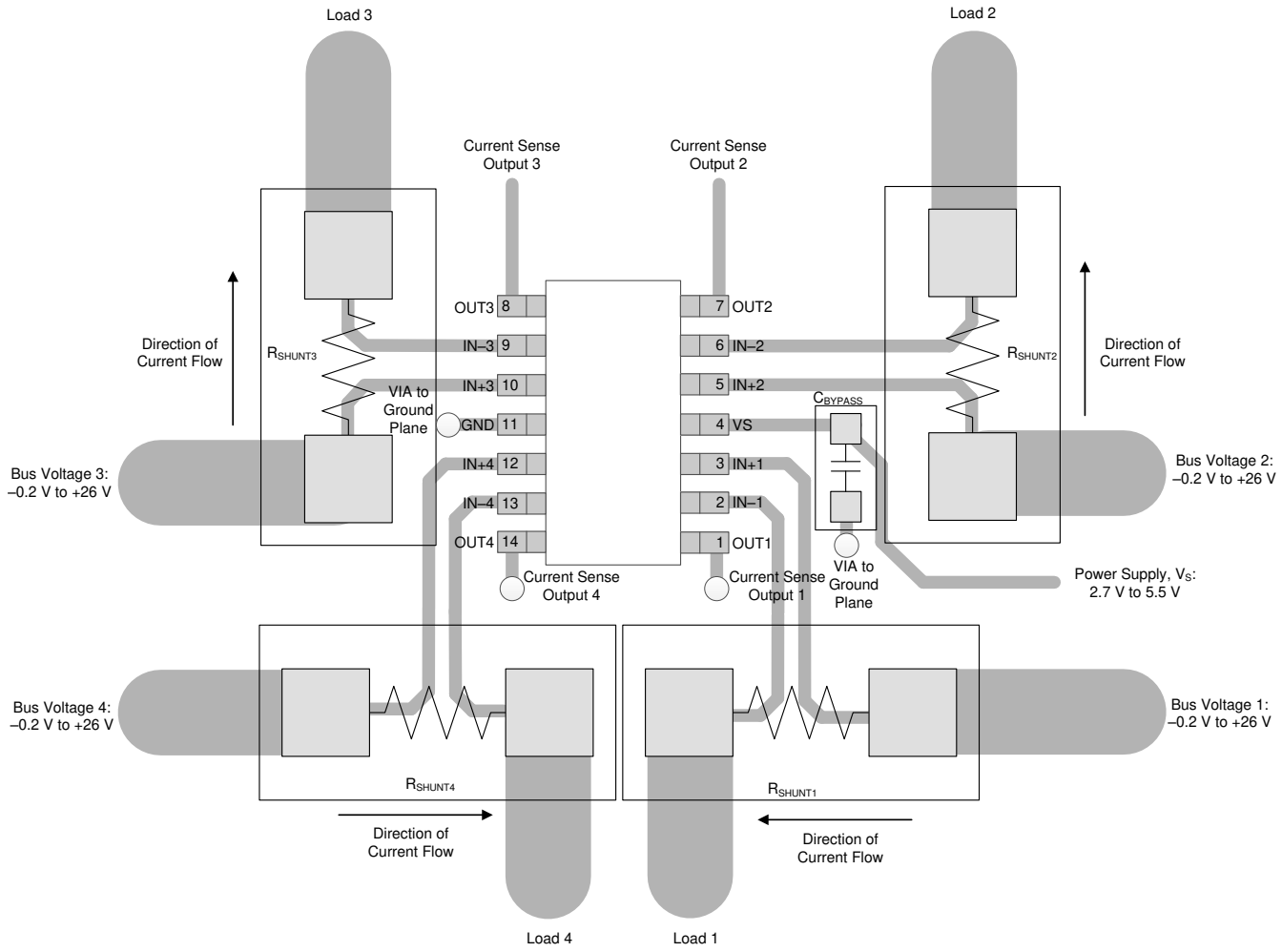

図 9-10. Quad-Channel Recommended Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *INA180-181EVM User's Guide*
- Texas Instruments, *INA2180-2181EVM User's Guide*
- Texas Instruments, *INA4180-4181EVM User's Guide*

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA180A1QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	18ID
INA180A1QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	18ID
INA180A2QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MN3
INA180A2QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MN3
INA180A3QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MO3
INA180A3QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MO3
INA180A4QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MP3
INA180A4QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MP3
INA180B1QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1MV3
INA180B1QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1MV3
INA180B2QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1MW3
INA180B2QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	1MW3
INA180B3QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MX3
INA180B3QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MX3
INA180B4QDBVRQ1	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MZ3
INA180B4QDBVRQ1.B	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1MZ3
INA2180A1QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O16
INA2180A1QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O16
INA2180A2QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O26
INA2180A2QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O26
INA2180A3QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O36
INA2180A3QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1O36
INA2180A4QDGKRQ1	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D26
INA2180A4QDGKRQ1.B	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1D26
INA4180A1QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	4180A1Q
INA4180A1QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4180A1Q
INA4180A2QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	4180A2Q
INA4180A2QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4180A2Q
INA4180A3QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4180A3Q

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
INA4180A3QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4180A3Q
INA4180A4QPWRQ1	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	4180A4Q
INA4180A4QPWRQ1.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4180A4Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA180-Q1, INA2180-Q1, INA4180-Q1 :

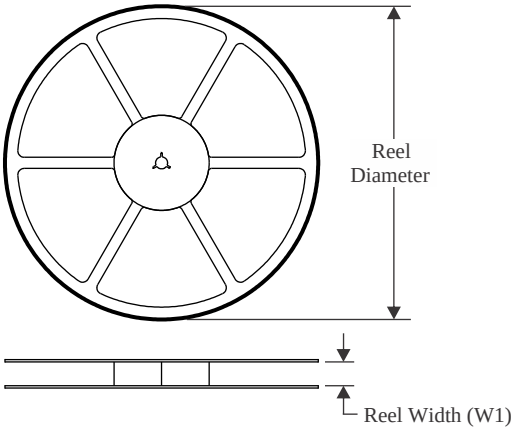
- Catalog : INA180, INA2180, INA4180

NOTE: Qualified Version Definitions:

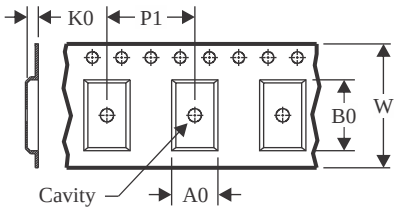
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

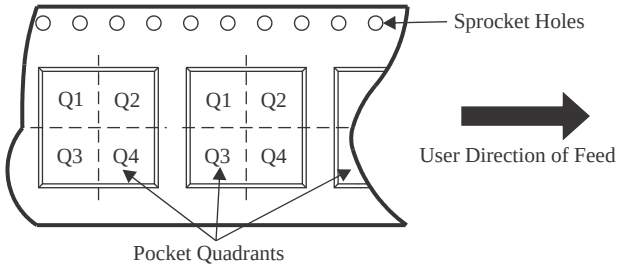


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

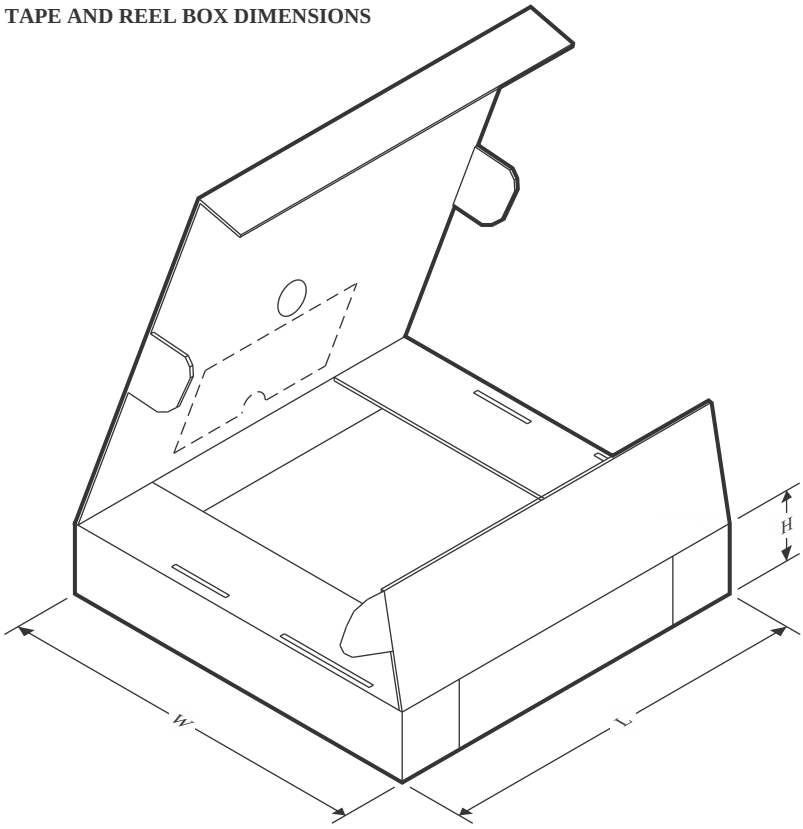


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA180A1QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A1QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A2QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A2QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A3QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A3QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A4QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180A4QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B1QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B1QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B2QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B2QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B3QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B3QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA180B4QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
INA2180A1QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA2180A1QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A2QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A2QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A3QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A3QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A4QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA2180A4QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA4180A1QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A1QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A2QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A2QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A3QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A4QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
INA4180A4QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA180A1QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A1QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A2QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A2QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A3QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A3QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A4QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180A4QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B1QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B1QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B2QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B2QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B3QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B3QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA180B4QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
INA2180A1QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA2180A1QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA2180A2QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

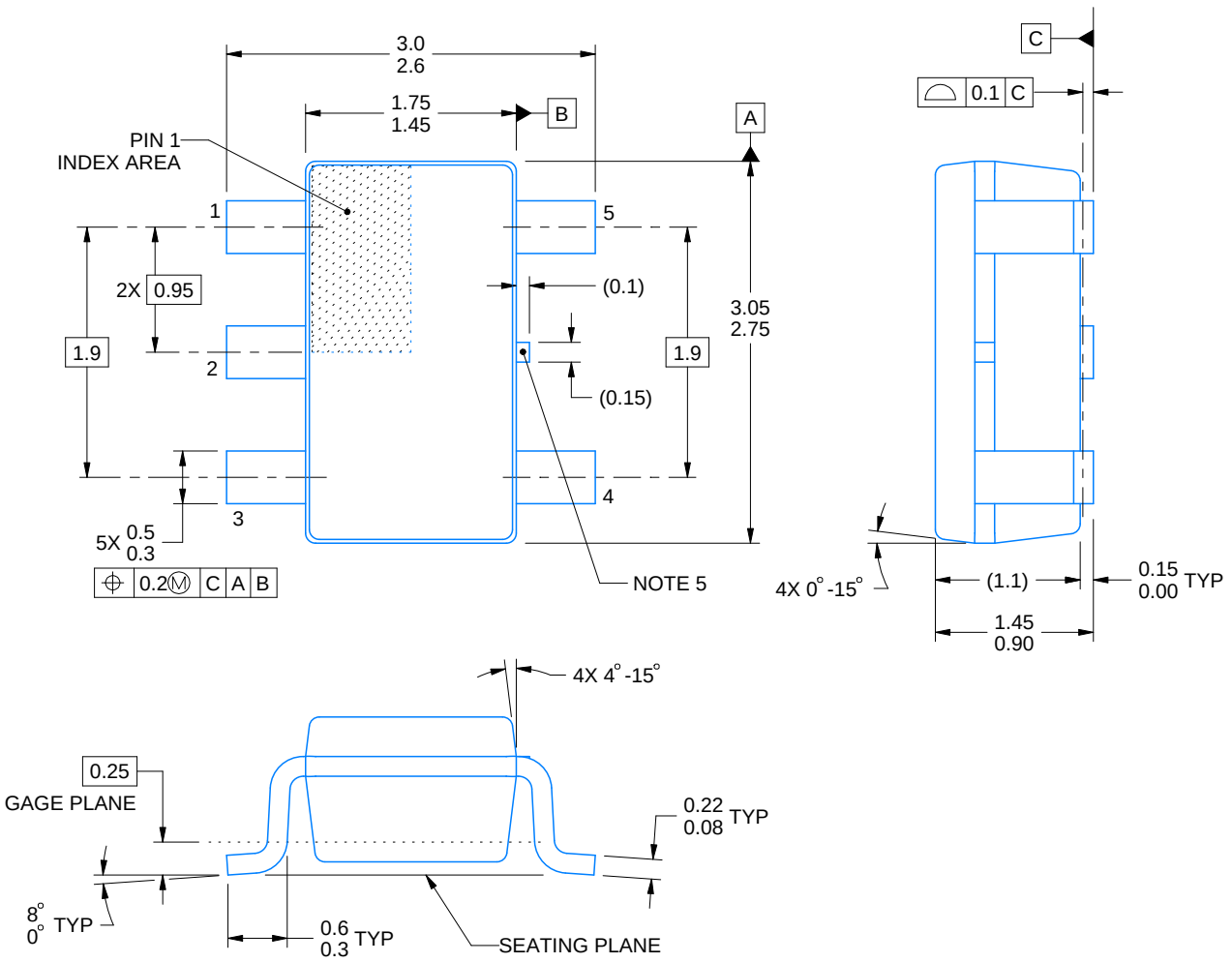
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA2180A2QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA2180A3QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA2180A3QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA2180A4QDGKRQ1	VSSOP	DGK	8	2500	353.0	353.0	32.0
INA2180A4QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
INA4180A1QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	36.0
INA4180A1QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
INA4180A2QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
INA4180A2QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	36.0
INA4180A3QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
INA4180A4QPWRQ1	TSSOP	PW	14	2000	353.0	353.0	32.0
INA4180A4QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	36.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

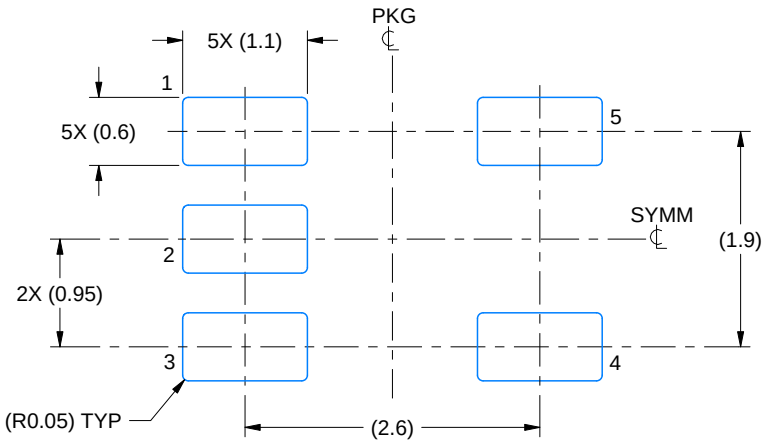
SMALL OUTLINE TRANSISTOR



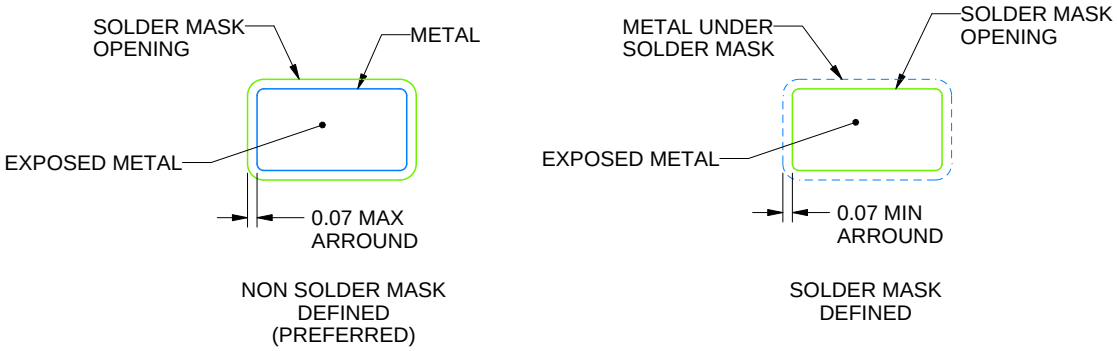
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

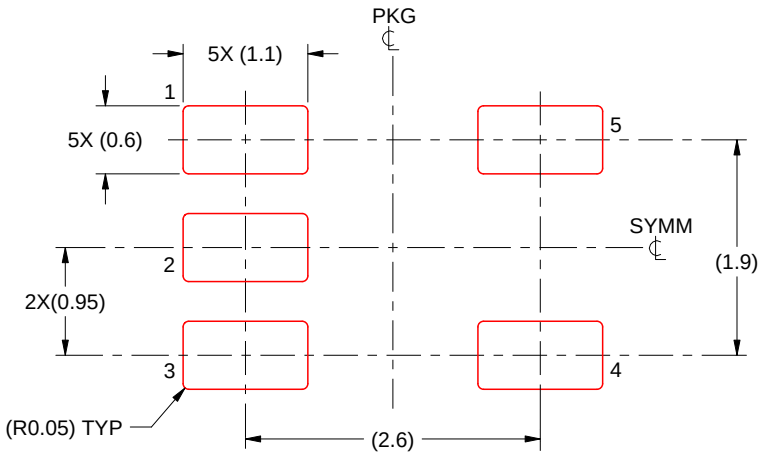


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

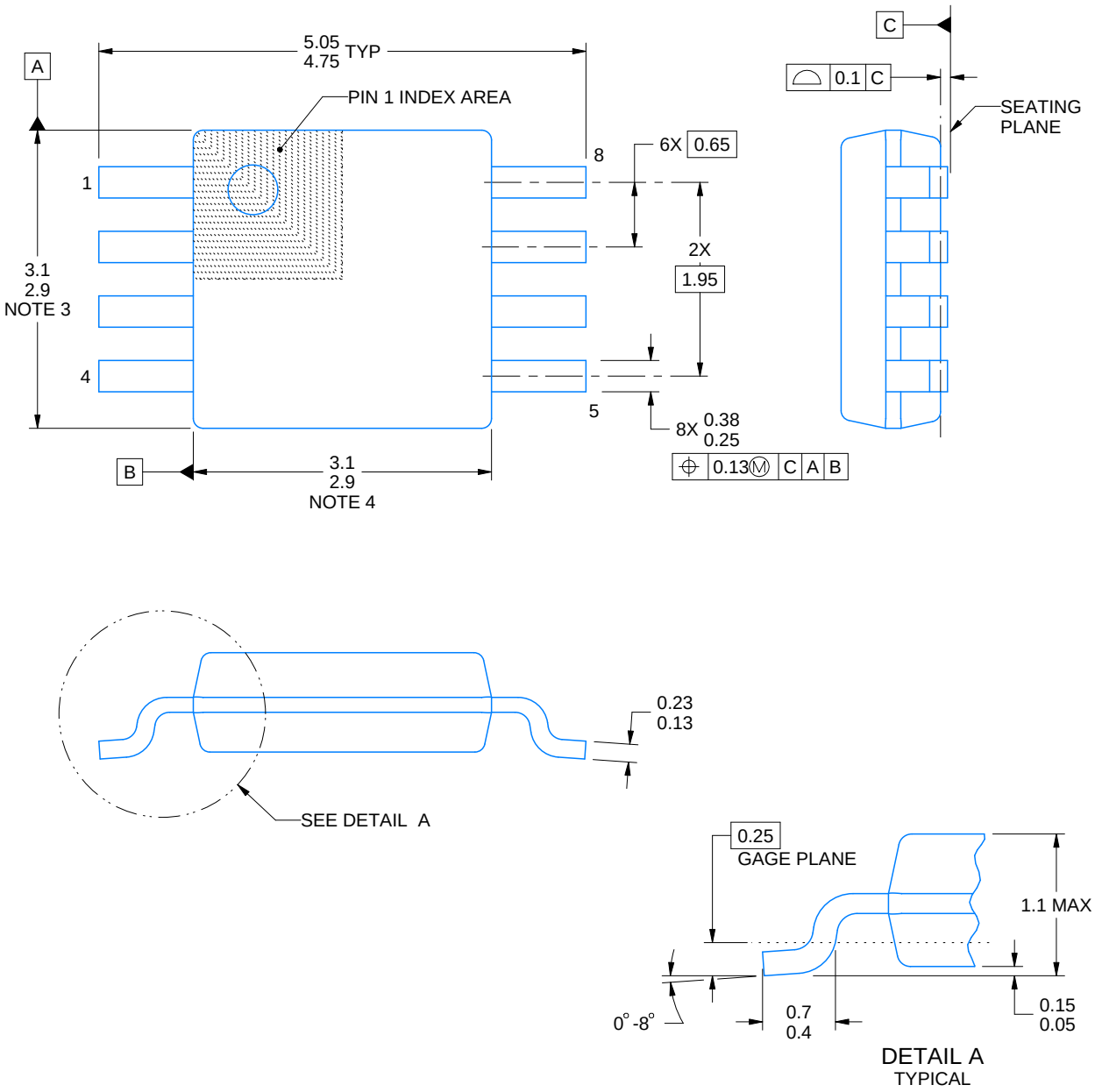
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

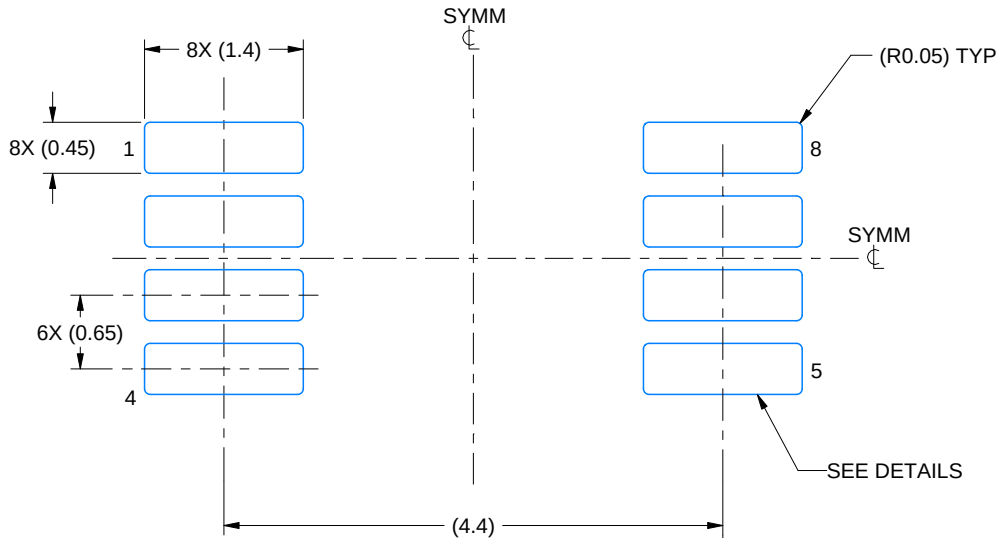
SMALL OUTLINE PACKAGE



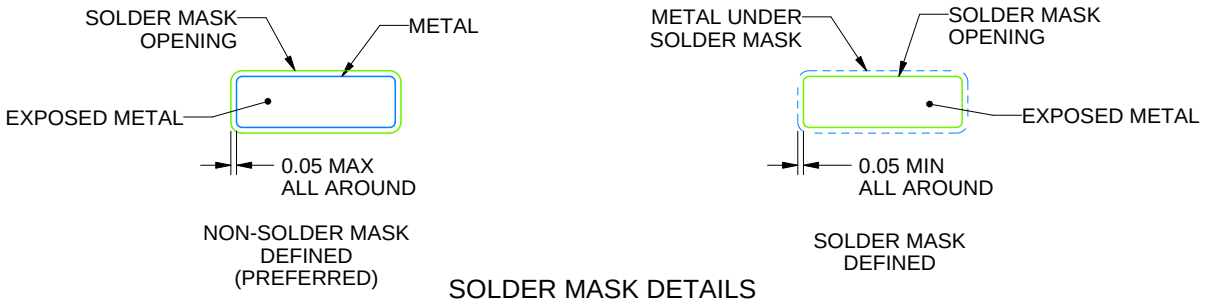
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

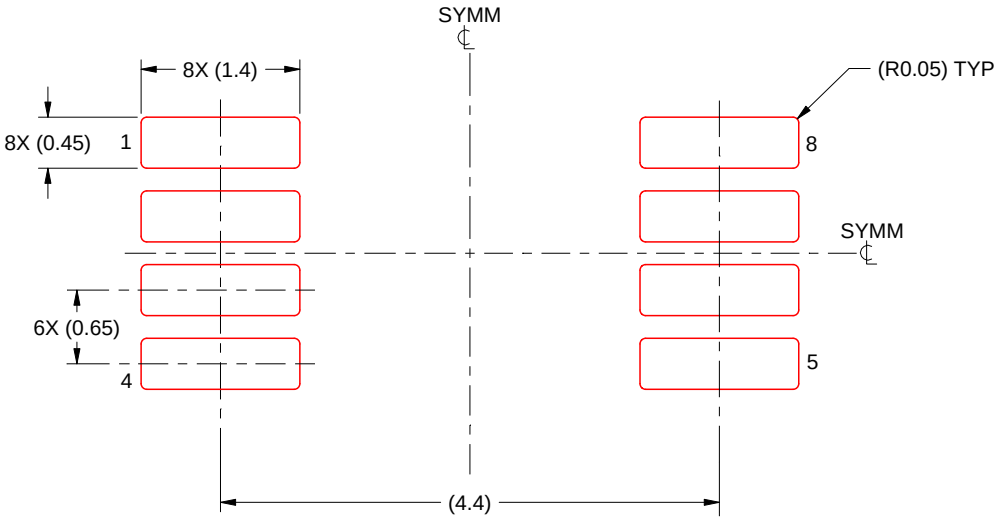


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

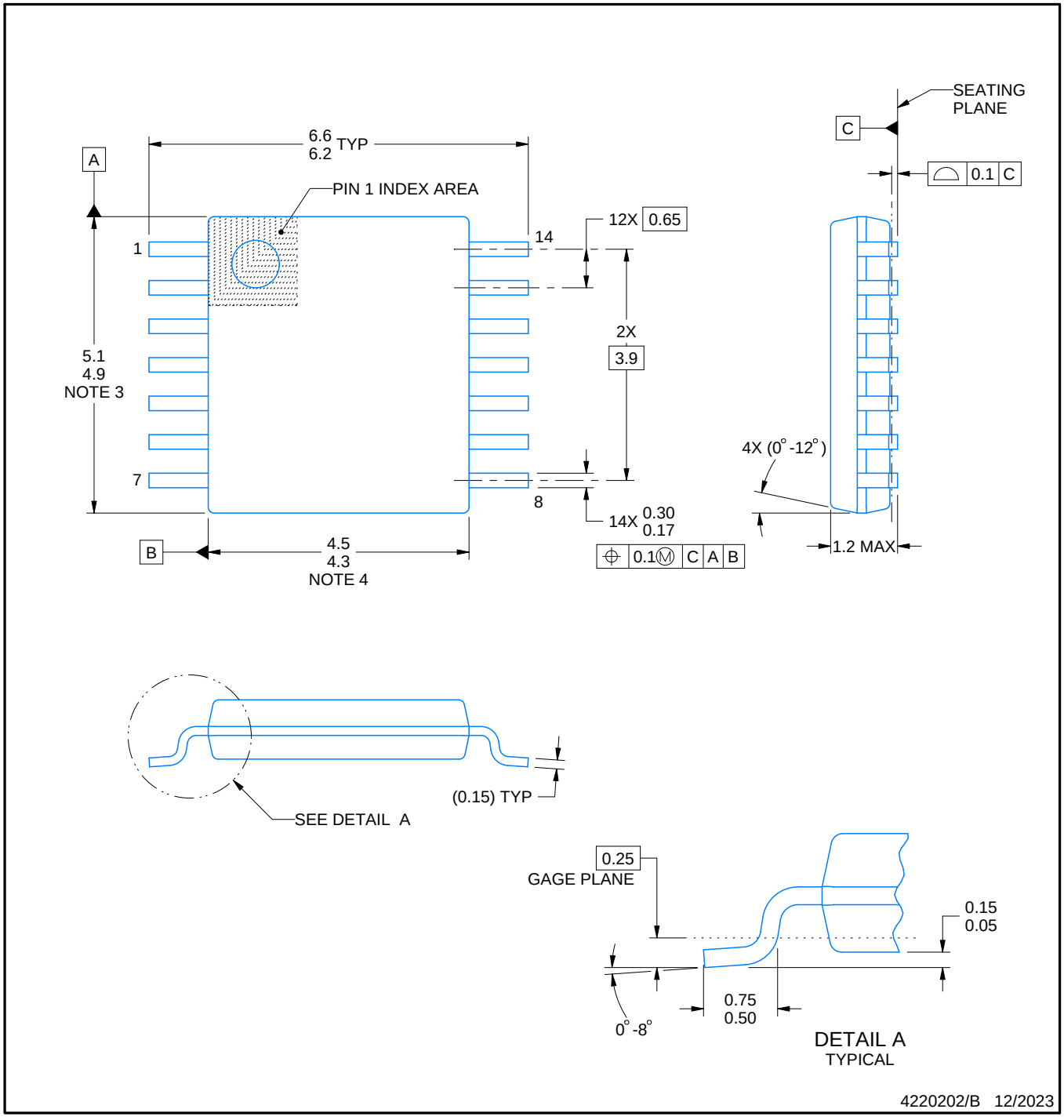
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

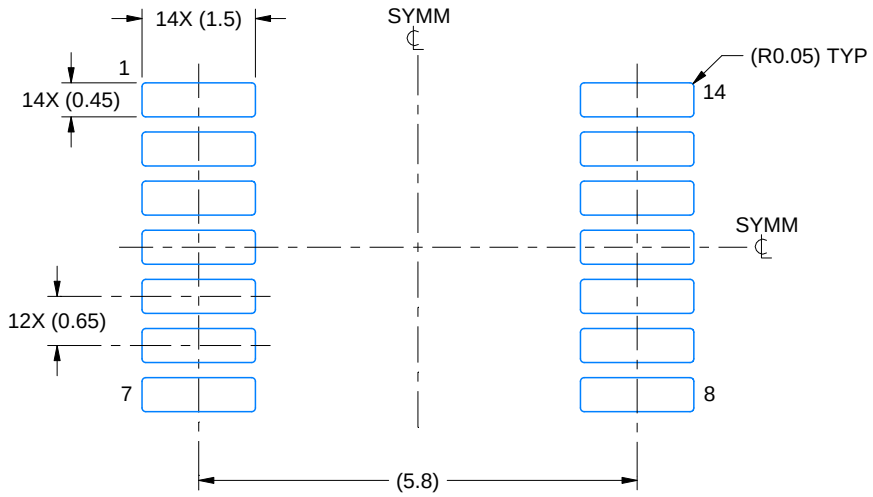
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

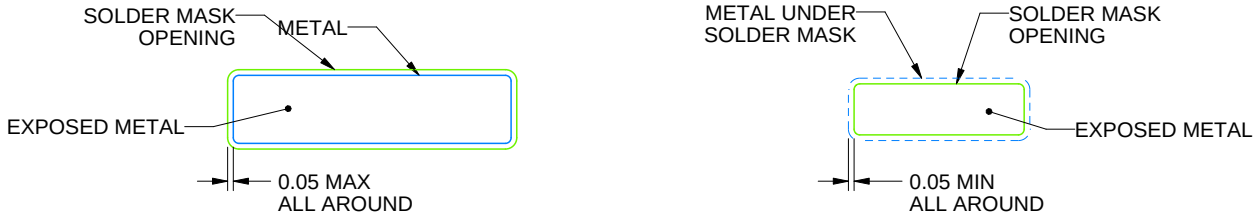


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

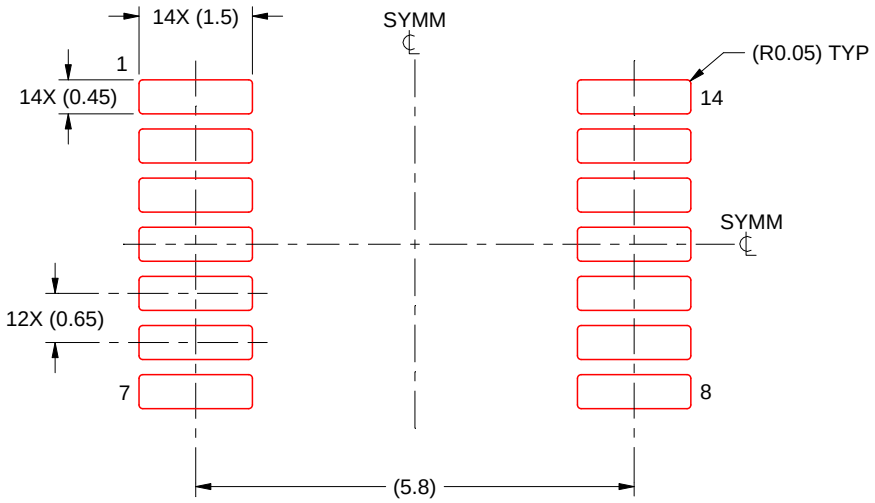


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月